

DLP651NE 0.65 インチ 1080p デジタル マイクロミラー デバイス

1 特長

- 対角 0.65 インチのマイクロミラー アレイ
 - ディスプレイ解像度: 1080p (1920 × 1080)
 - 7.6μm のマイクロミラー ピッチ
 - マイクロミラー傾斜角: ±12° (平面に対して)
 - コーナー照明
- 高速シリアル インターフェイス (High-Speed Serial Interface、HSSI) 入力データ バス
- 最大 240Hz の 1080p (フル HD) をサポート
- DLPC7530** ディスプレイ コントローラ、**DLPA100** パワー マネージメント、およびモータドライバ IC によってサポートされたレーザー蛍光 / LED / RGB レーザー / ランプ動作

2 アプリケーション

- レーザー TV
- スマート プロジェクタ
- 企業向けプロジェクタ

3 概要

DLP651NE デジタル マイクロミラー デバイス (DMD) は、デジタル制御型の MEMS (micro-electromechanical system) 空間光変調器 (SLM) で、色鮮やかな 1080p ディスプレイ システムを実現します。本 DLP® 製品の 0.65 インチ 1080p チップセットは、DMD、または **DLPC7530** ディスプレイ コントローラ、**DLPA100** パワーおよびモータドライバで構成されています。このコンパクトなチップセットは、小型の 1080p ディスプレイを実現する完全なシステム ソリューションを提供します。

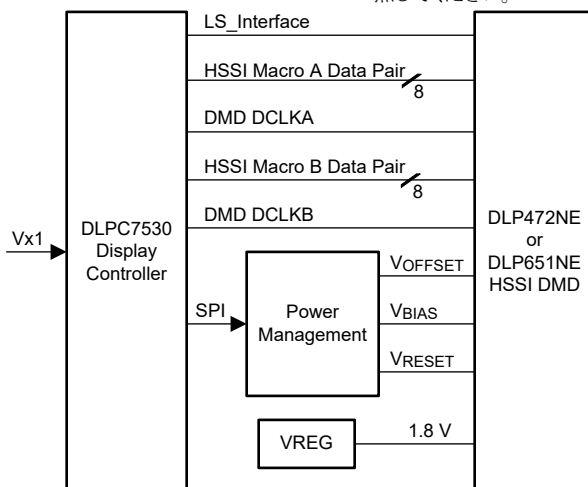
DMD のエコシステムに、設計期間の短縮に役立つ定評あるリソースが用意されています。承認済みの光学モジュール メーカーやサード パーティ プロバイダを探すには、[DLP® Products サード パーティ プロバイダ検索ツール](#)をご利用ください。

DMD を使用して設計を始める方法の詳細については、『[テキサス・インスツルメンツの DLP ディスプレイ テクノロジーを使用した設計の開始](#)』をご覧ください。

製品情報

| 部品番号 | パッケージ (1) | パッケージ サイズ |
|----------|-----------|-----------------|
| DLP651NE | FYP(149) | 32.2mm × 22.3mm |

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。



アプリケーション概略図



Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 特長 | 1 | 7 Application and Implementation | 32 |
| 2 アプリケーション | 1 | 7.1 Application Information..... | 32 |
| 3 概要 | 1 | 7.2 Typical Application..... | 32 |
| 4 Pin Configuration and Functions | 3 | 7.3 Temperature Sensor Diode..... | 34 |
| 5 Specifications | 6 | 8 Power Supply Recommendations | 35 |
| 5.1 Absolute Maximum Ratings..... | 6 | 8.1 Power Supply Sequence Requirements..... | 35 |
| 5.2 Storage Conditions..... | 6 | 8.2 DMD Power Supply Power-Up Procedure..... | 35 |
| 5.3 ESD Ratings..... | 7 | 8.3 DMD Power Supply Power-Down Procedure..... | 35 |
| 5.4 Recommended Operating Conditions..... | 7 | 9 Layout | 37 |
| 5.5 Thermal Information..... | 10 | 9.1 Layout Guidelines..... | 37 |
| 5.6 Electrical Characteristics..... | 10 | 9.2 Impedance Requirements..... | 37 |
| 5.7 Switching Characteristics..... | 11 | 9.3 Layers..... | 37 |
| 5.8 Timing Requirements..... | 12 | 9.4 Trace Width, Spacing..... | 38 |
| 5.9 System Mounting Interface Loads..... | 16 | 9.5 Power..... | 38 |
| 5.10 Micromirror Array Physical Characteristics..... | 17 | 9.6 Trace Length Matching Recommendations..... | 38 |
| 5.11 Micromirror Array Optical Characteristics..... | 19 | 10 Device and Documentation Support | 40 |
| 5.12 Window Characteristics..... | 20 | 10.1 サード・パーティ製品に関する免責事項..... | 40 |
| 5.13 Chipset Component Usage Specification..... | 20 | 10.2 Device Support..... | 40 |
| 6 Detailed Description | 21 | 10.3 Documentation Support..... | 40 |
| 6.1 Overview..... | 21 | 10.4 ドキュメントの更新通知を受け取る方法..... | 41 |
| 6.2 Functional Block Diagram..... | 22 | 10.5 サポート・リソース..... | 41 |
| 6.3 Feature Description..... | 23 | 10.6 Trademarks..... | 41 |
| 6.4 Device Functional Modes..... | 23 | 10.7 静電気放電に関する注意事項..... | 41 |
| 6.5 Optical Interface and System Image Quality Considerations..... | 23 | 10.8 用語集..... | 41 |
| 6.6 Micromirror Array Temperature Calculation..... | 24 | 11 Revision History | 41 |
| 6.7 Micromirror Power Density Calculation..... | 25 | 12 Mechanical, Packaging, and Orderable Information | 43 |
| 6.8 Window Aperture Illumination Overfill Calculation..... | 27 | 12.1 Package Option Addendum..... | 44 |
| 6.9 Micromirror Landed-On/Landed-Off Duty Cycle..... | 28 | | |

4 Pin Configuration and Functions

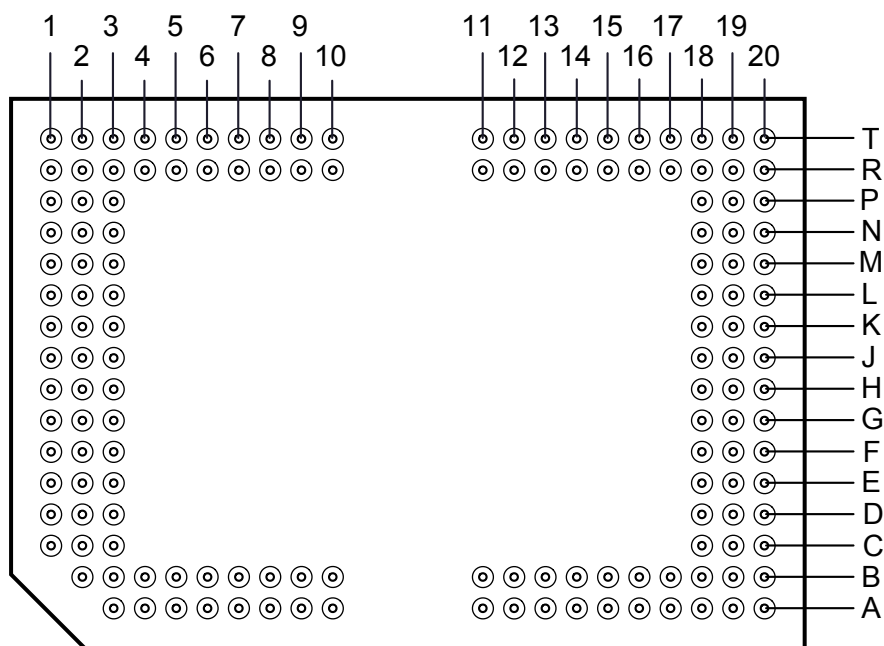


図 4-1. FYP Package 149-Pin CPGA Bottom View

表 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | TRACE LENGTH (mm) |
|---------|--------|---------------------|---|-------------------|
| NAME | PAD ID | | | |
| D_AP(0) | J1 | I | High-speed differential data pair lane A0 | 18.09088 |
| D_AN(0) | H1 | I | High-speed differential data pair lane A0 | 18.0916 |
| D_AP(1) | G1 | I | High-speed differential data pair lane A1 | 18.11696 |
| D_AN(1) | F1 | I | High-speed differential data pair lane A1 | 18.11641 |
| D_AP(2) | A3 | I | High-speed differential data pair lane A2 | 11.11822 |
| D_AN(2) | A4 | I | High-speed differential data pair lane A2 | 11.11745 |
| D_AP(3) | D2 | I | High-speed differential data pair lane A3 | 12.04461 |
| D_AN(3) | C2 | I | High-speed differential data pair lane A3 | 12.04491 |
| D_AP(4) | F2 | I | High-speed differential data pair lane A4 | 15.1345 |
| D_AN(4) | E2 | I | High-speed differential data pair lane A4 | 15.13457 |
| D_AP(5) | A5 | I | High-speed differential data pair lane A5 | 12.80888 |
| D_AN(5) | A6 | I | High-speed differential data pair lane A5 | 12.80825 |
| D_AP(6) | A7 | I | High-speed differential data pair lane A6 | 6.34763 |
| D_AN(6) | A8 | I | High-speed differential data pair lane A6 | 6.34706 |
| D_AP(7) | A9 | I | High-speed differential data pair lane A7 | 4.45653 |
| D_AN(7) | A10 | I | High-speed differential data pair lane A7 | 4.45875 |
| DCLK_AP | C1 | I | High-speed differential clock A | 15.08029 |
| DCLK_AN | D1 | I | High-speed differential clock A | 15.07977 |
| D_BP(0) | A11 | I | High-speed differential data pair lane B0 | 4.06642 |
| D_BN(0) | A12 | I | High-speed differential data pair lane B0 | 4.06697 |
| D_BP(1) | A13 | I | High-speed differential data pair lane B1 | 6.42676 |

表 4-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | TRACE LENGTH (mm) |
|------------------|---|---------------------|--|-------------------|
| NAME | PAD ID | | | |
| D_BN(1) | A14 | I | High-speed differential data pair lane B1 | 6.42716 |
| D_BP(2) | A15 | I | High-speed differential data pair lane B2 | 11.90485 |
| D_BN(2) | A16 | I | High-speed differential data pair lane B2 | 11.90509 |
| D_BP(3) | A18 | I | High-speed differential data pair lane B3 | 13.80223 |
| D_BN(3) | A19 | I | High-speed differential data pair lane B3 | 13.80269 |
| D_BP(4) | D19 | I | High-speed differential data pair lane B4 | 12.45294 |
| D_BN(4) | C19 | I | High-speed differential data pair lane B4 | 12.45252 |
| D_BP(5) | H20 | I | High-speed differential data pair lane B5 | 15.7909 |
| D_BN(5) | J20 | I | High-speed differential data pair lane B5 | 15.79026 |
| D_BP(6) | D20 | I | High-speed differential data pair lane B6 | 11.02899 |
| D_BN(6) | E20 | I | High-speed differential data pair lane B6 | 11.02947 |
| D_BP(7) | F20 | I | High-speed differential data pair lane B7 | 14.7517 |
| D_BN(7) | G20 | I | High-speed differential data pair lane B7 | 14.75085 |
| DCLK_BP | B17 | I | High-speed differential clock B | 9.17864 |
| DCLK_BN | B18 | I | High-speed differential clock B | 9.17821 |
| LS_WDATA_P | T10 | I | LVDS Data | 11.27905 |
| LS_WDATA_N | R11 | I | LVDS Data | 6.76474 |
| LS_CLK_P | R9 | I | LVDS CLK | 13.5461 |
| LS_CLK_N | R10 | I | LVDS CLK | 12.56934 |
| LS_RDATA_A_BISTA | T13 | O | LVC MOS Output | 3.12045 |
| BIST_B | T12 | O | LVC MOS Output | 5.63628 |
| AMUX_OUT | B20 | O | Analog Test Mux | 9.3849 |
| DMUX_OUT | R14 | O | Digital Test Mux | 3.85333 |
| DMD_DEN_ARSTZ | T11 | I | ARSTZ | 5.86593 |
| TEMP_N | R8 | I | Temp Diode N | 14.63792 |
| TEMP_P | R7 | I | Temp Diode P | 15.93219 |
| VDD | B7, B13, C18, E3, H3, J2, K3, L2, L19, M1, M2, N3, N19, P2, P18, R3, R5, R12, R17, R19, T2, T4, T6, T8, T18 | P | Digital core supply voltage | Plane |
| VDDA | B4, B9, B11, B16, C20, D3, E18, G2, G19 | P | HSSI supply voltage | Plane |
| VRESET | B3, R1 | P | Supply voltage for negative bias of micromirror reset signal | Plane |
| VBIAS | E1, P1 | P | Supply voltage for positive bias of micromirror reset signal | Plane |
| VOFFSET | A20, B2, T1, T20 | P | Supply voltage for HVCMOS logic, stepped up logic level | Plane |

表 4-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | TRACE LENGTH (mm) |
|------|--|---------------------|-----------------|-------------------|
| NAME | PAD ID | | | |
| VSS | A17, B6, B10, B14, D18, F3, F19, J3, K2, K19, L1, L3, M3, N2, N18, N20, P3, P20, R2, R4, R6, R13, R20, T5, T7, T16, T17, T19 | G | Ground | Plane |
| VSSA | B5, B8, B12, B15, B19, C3, E19, G3, H2, H19, K1, N1, P19, R18, T3, T9 | G | Ground | Plane |
| N/C | R15, T14, T15, R16, H18, J18, G18, J19, F18, K20, K18, M19, L20, M18, L18, M20 | | No connect | |

(1) I=Input, O=Output, P=Power, G=Ground, NC = No connect

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

| Parameter Name | Description | MIN | MAX | UNIT |
|---|---|------|-----------|------|
| Supply Voltage | | | | |
| V_{DD} | Supply voltage for LVCMOS core logic and LVCMOS low speed interface (LSIF) ⁽¹⁾ | −0.5 | 2.3 | V |
| V_{DDA} | Supply voltage for high speed serial interface (HSSI) receivers ⁽¹⁾ | −0.3 | 2.2 | V |
| V_{OFFSET} | Supply voltage for HVCMOS and micromirror electrode ^{(1) (2)} | −0.5 | 11 | V |
| V_{BIAS} | Supply voltage for micromirror electrode ⁽¹⁾ | −0.5 | 17 | V |
| V_{RESET} | Supply voltage for micromirror electrode ⁽¹⁾ | −13 | 0.5 | V |
| $ V_{DDA} - V_{DD} $ | Supply voltage delta (absolute value) ⁽³⁾ | | 0.3 | V |
| $ V_{BIAS} - V_{OFFSET} $ | Supply voltage delta (absolute value) ⁽⁴⁾ | | 11 | V |
| $ V_{BIAS} - V_{RESET} $ | Supply voltage delta (absolute value) ⁽⁵⁾ | | 30 | V |
| Input Voltage | | | | |
| | Input voltage for other inputs – LSIF and LVCMOS ⁽¹⁾ | −0.5 | 2.45 | V |
| | Input voltage for other inputs – HSSI ^{(1) (6)} | −0.2 | V_{DDA} | V |
| Low speed interface (LSIF) | | | | |
| f_{CLOCK} | LSIF clock frequency (LS_CLK) | | 130 | MHz |
| $ V_{ID} $ | LSIF differential input voltage magnitude ⁽⁶⁾ | | 810 | mV |
| I_{ID} | LSIF differential input current ⁽⁷⁾ | | 10 | mA |
| High speed serial interface (HSSI) | | | | |
| f_{CLOCK} | HSSI clock frequency (DCLK) | | 1.65 | GHz |
| $ V_{ID} $ | HSSI differential input voltage magnitude Data Lane ⁽⁶⁾ | | 700 | mV |
| $ V_{ID} $ | HSSI differential input voltage magnitude Clock Lane ⁽⁶⁾ | | 700 | mV |
| Environmental | | | | |
| T_{ARRAY} | Temperature, operating ⁽⁸⁾ | 0 | 90 | °C |
| T_{ARRAY} | Temperature, non-operating ⁽⁸⁾ | −40 | 90 | °C |
| T_{DP} | Dew point temperature, operating and non-operating (non-condensing) | | 81 | °C |

- (1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD} , V_{DDA} , V_{OFFSET} , V_{BIAS} , and V_{RESET} . All V_{SS} connections are also required.
- (2) V_{OFFSET} supply transients must fall within specified voltages.
- (3) Exceeding the recommended allowable absolute voltage difference between V_{DDA} and V_{DD} may result in excessive current draw.
- (4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
- (5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
- (6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS and HSSI differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (7) Differential inputs must not exceed the specified limit or damage may result to the internal termination resistors. Specification applies to both the High speed serial interface (HSSI) and the low speed interface (LSI).
- (8) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) in the package thermal resistances using the *Micromirror Array Temperature Calculation*.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------|--|-----|-----|------|
| T_{DMD} | DMD storage temperature | −40 | 80 | °C |
| T_{DP-AVG} | Average dew point temperature (non-condensing) ⁽¹⁾ | | 28 | °C |
| T_{DP-ELR} | Elevated dew point temperature range (non-condensing) ⁽²⁾ | 28 | 36 | °C |

5.2 Storage Conditions (続き)

Applicable for the DMD as a component or non-operating in a system.

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-------------------|---|-----|-----|--------|
| CT _{ELR} | Cumulative time in the elevated dew point temperature range | | 24 | Months |

- (1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

| SYMBOL | PARAMETER | DESCRIPTION | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| V _(ESD) | Electrostatic discharge | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | V |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the recommended operating conditions. No level of performance is implied when operating the device above or below the recommended operating conditions limits.

| | | MIN | TYP | MAX | UNIT |
|---|---|-----------------------|-----|-------|------|
| SUPPLY VOLTAGES ^{(1) (2)} | | | | | |
| V _{DD} | Supply voltage for LVCMOS core logic and low speed interface (LSIF) | 1.71 | 1.8 | 1.95 | V |
| V _{DDA} | Supply voltage for high speed serial interface (HSSI) receivers | 1.71 | 1.8 | 1.95 | V |
| V _{OFFSET} | Supply voltage for HVCMOS and micromirror electrode ⁽³⁾ | 9.5 | 10 | 10.5 | V |
| V _{BIAS} | Supply voltage for micromirror electrode | 17.5 | 18 | 18.5 | V |
| V _{RESET} | Supply voltage for micromirror electrode | −14.5 | −14 | −13.5 | V |
| V _{DDA} − V _{DD} | Supply voltage delta, absolute value ⁽⁴⁾ | | | 0.3 | V |
| V _{BIAS} − V _{OFFSET} | Supply voltage delta, absolute value ⁽⁵⁾ | | | 10.5 | V |
| V _{BIAS} − V _{RESET} | Supply voltage delta, absolute value | | | 33 | V |
| LVCMOS INPUT | | | | | |
| V _{IH} | High level input voltage ⁽⁶⁾ | 0.7 × V _{DD} | | | V |
| V _{IL} | Low level input voltage ⁽⁶⁾ | 0.3 × V _{DD} | | | V |
| LOW SPEED SERIAL INTERFACE (LSIF) | | | | | |
| f _{CLOCK} | LSIF clock frequency (LS_CLK) ⁽⁷⁾ | 108 | 120 | 130 | MHz |
| DCD _{IN} | LSIF duty cycle distortion (LS_CLK) | 44% | | 56% | |
| V _{ID} | LSIF differential input voltage magnitude ⁽⁷⁾ | 150 | 350 | 440 | mV |
| V _{LVDS} | LSIF voltage ⁽⁷⁾ | 575 | | 1520 | mV |
| V _{CM} | Common mode voltage ⁽⁷⁾ | 700 | 900 | 1300 | mV |
| Z _{LINE} | Line differential impedance (PWB/trace) | 90 | 100 | 110 | Ω |
| Z _{IN} | Internal differential termination resistance | 80 | 100 | 120 | Ω |
| HIGH SPEED SERIAL INTERFACE (HSSI) | | | | | |
| f _{CLOCK} | HSSI clock frequency (DCLK) ⁽⁸⁾ | 1.2 | | 1.6 | GHz |
| DCD _{IN} | HSSI duty cycle distortion (DCLK) | 44% | 50% | 56% | |
| V _{ID} Data | HSSI differential input voltage magnitude data lane ⁽⁸⁾ | 100 | | 600 | mV |

5.4 Recommended Operating Conditions (続き)

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the recommended operating conditions. No level of performance is implied when operating the device above or below the recommended operating conditions limits.

| | | MIN | TYP | MAX | UNIT |
|---------------------------------|--|-----|-----|--------------------------|--------------------|
| V _{ID} CLK | HSSI differential input voltage magnitude Clock lane ⁽⁸⁾ | 295 | | 600 | mV |
| VCM _{DC} Data | Input common mode voltage (DC) data lane ⁽⁸⁾ | 200 | 600 | 800 | mV |
| VCM _{DC} CLK | Input common mode voltage (DC) Clk lane ⁽⁸⁾ | 200 | 600 | 800 | mV |
| VCM _{ACp-p} | AC peak to peak (ripple) on common mode voltage of data lane and Clock lane ⁽⁸⁾ | | | 100 | mV |
| Z _{LINE} | Line differential impedance (PWB/trace) | | 100 | | Ω |
| Z _{IN} | Internal differential termination resistance (R _{Xterm}) | 80 | 100 | 120 | Ω |
| ENVIRONMENTAL | | | | | |
| T _{ARRAY} | Array temperature, long-term operational ^{(9) (10) (12)} | 10 | | 40 to 70 ⁽¹¹⁾ | °C |
| | Array temperature, short-term operational, 500 hr max ^{(10) (13)} | 0 | | 10 | °C |
| T _{DP-AVG} | Average dew point temperature (non-condensing) ⁽¹⁴⁾ | | | 28 | °C |
| T _{DP-ELR} | Elevated dew point temperature range (non-condensing) ⁽¹⁵⁾ | 28 | | 36 | °C |
| CT _{ELR} | Cumulative time in elevated dew point temperature range | | | 24 | months |
| Q _{AP-ILL} | Window aperture illumination overfill ^{(16) (17)} | | | 17 | W/cm ² |
| SOLID STATE ILLUMINATION | | | | | |
| ILL _{UV} | Illumination power at wavelengths < 410nm ^{(9) (19)} | | | 10 | mW/cm ² |
| ILL _{VIS} | Illumination power at wavelengths ≥ 410nm and ≤ 800nm ^{(18) (19)} | | | 34.7 | W/cm ² |
| ILL _{IR} | Illumination power at wavelengths > 800nm ⁽¹⁹⁾ | | | 10 | mW/cm ² |
| ILL _{BLU} | Illumination power at wavelengths ≥ 410nm and ≤ 475nm ^{(18) (19)} | | | 11.0 | W/cm ² |
| ILL _{BLU1} | Illumination power at wavelengths ≥ 410nm and ≤ 440nm ^{(18) (19)} | | | 1.8 | W/cm ² |
| LAMP ILLUMINATION | | | | | |
| ILL _{UV} | Illumination power at wavelengths < 395nm ^{(9) (19)} | | | 2.0 | mW/cm ² |
| ILL _{VIS} | Illumination power at wavelengths ≥ 395nm and ≤ 800nm ^{(18) (19)} | | | 29.3 | W/cm ² |
| ILL _{IR} | Illumination power at wavelengths > 800nm ⁽¹⁹⁾ | | | 10 | mW/cm ² |

- (1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
- (2) All voltage values are with respect to the V_{SS} ground pins.
- (3) V_{OFFSET} supply transients must fall within specified max voltages.
- (4) To prevent excess current, the supply voltage delta |V_{DDA} – V_{DD}| must be less than specified limit.
- (5) To prevent excess current, the supply voltage delta |V_{BIAS} – V_{OFFSET}| must be less than specified limit.
- (6) LVCMOS input pin is DMD_DEN_ARSTZ.
- (7) See the low speed interface (LSIF) timing requirements in [セクション 5.8](#).
- (8) See the high speed serial interface (HSSI) timing requirements in [セクション 5.8](#).
- (9) Simultaneous exposure of the DMD to the maximum [セクション 5.4](#) for temperature and UV illumination reduces device lifetime.
- (10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in [図 6-1](#) and the [セクション 5.5](#) using the [セクション 6.6](#).
- (11) Per [図 5-1](#), the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to [セクション 6.9](#) for a definition of micromirror landed duty cycle.
- (12) Long-term is defined as the usable life of the device.
- (13) Short-term is the total cumulative time over the useful life of the device.
- (14) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
- (15) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
- (16) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The

illumination optical system should be designed to minimize light flux incident outside the active array. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

- (17) Applies to the region in red in [図 5-2](#)
- (18) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
- (19) To calculate see [セクション 6.7](#).

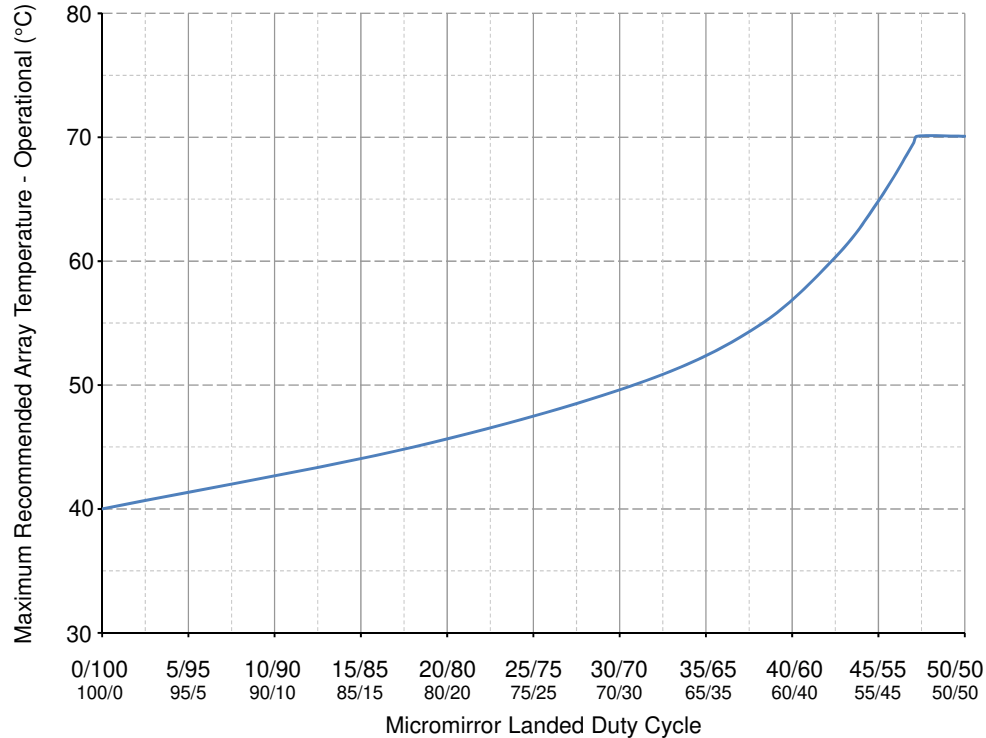


図 5-1. Maximum Recommended Array Temperature—Derating Curve

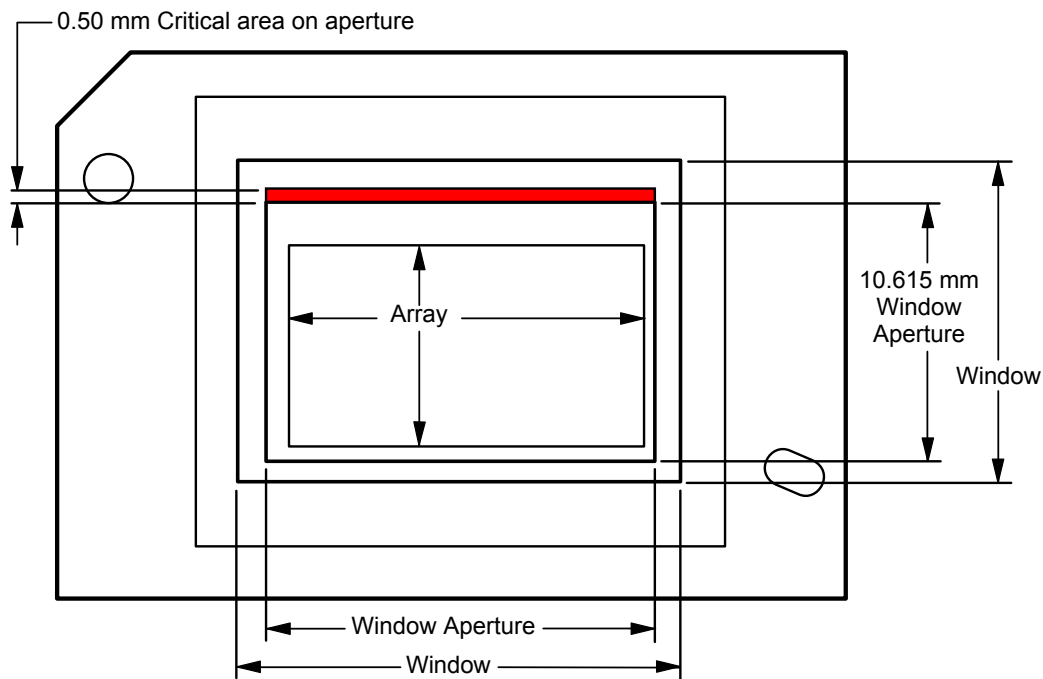


図 5-2. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

| THERMAL METRIC | DLP650TE | UNIT |
|--|-------------|------|
| | FYP Package | |
| | 149 PINS | |
| Thermal resistance, active area to test point 1 (TP1) ⁽¹⁾ | 0.60 | °C/W |

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the [セクション 5.4](#). The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems must be designed to minimize the light energy falling outside the window's clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

| SYMBOL | PARAMETER ^{(1) (2)} | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|--------------------------|--|--------------------------------|-------|------|--------|------|
| Current – Typical | | | | | | |
| I_{DD} | Supply current V_{DD} ⁽³⁾ | | | 800 | 1250 | mA |
| I_{DDA} | Supply current V_{DDA} ⁽³⁾ | | | 900 | 1200 | mA |
| I_{DDA} | Supply current V_{DDA} ⁽³⁾ | single macro mode | | 500 | 600 | mA |
| I_{OFFSET} | Supply current V_{OFFSET} ^{(4) (5)} | | | 23 | 35 | mA |
| I_{BIAS} | Supply current V_{BIAS} ^{(4) (5)} | | | 2.4 | 3.8 | mA |
| I_{RESET} | Supply current V_{RESET} ⁽⁵⁾ | | -10.5 | -7.7 | | mA |
| Power – Typical | | | | | | |
| P_{DD} | Supply power dissipation V_{DD} ⁽³⁾ | | | 1440 | 2437.5 | mW |
| P_{DDA} | Supply power dissipation V_{DDA} ⁽³⁾ | | | 1620 | 2340 | mW |
| P_{DDA} | Supply power dissipation V_{DDA} ⁽³⁾ | single macro mode | | 900 | 1170 | mW |
| P_{OFFSET} | Supply power dissipation V_{OFFSET} ^{(4) (5)} | | | 230 | 367.5 | mW |

5.6 Electrical Characteristics (続き)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

| SYMBOL | PARAMETER ^{(1) (2)} | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|---|-----------------------|-----------------------|---------|------|
| P _{BIAS} | Supply power dissipation V _{BIAS} ^{(4) (5)} | | | 38.4 | 62.7 | mW |
| P _{RESET} | Supply power dissipation V _{RESET} ⁽⁵⁾ | | | 92.4 | 131.25 | mW |
| P _{TOTAL} | Supply power dissipation Total | | | 3420.8 | 5338.95 | mW |
| LVC MOS Input | | | | | | |
| I _{IL} | Low level input current ⁽⁶⁾ | V _{DD} = 1.95V, V _I = 0V | –100 | | | nA |
| I _{IH} | High level input current ⁽⁶⁾ | V _{DD} = 1.95V, V _I = 1.95V | | | 135 | μA |
| LVC MOS Output | | | | | | |
| V _{OH} | DC output high voltage ⁽⁷⁾ | I _{OH} = –2mA | 0.8 × V _{DD} | | | V |
| V _{OL} | DC output low voltage ⁽⁷⁾ | I _{OL} = 2mA | | 0.2 × V _{DD} | | V |
| Receiver Eye Characteristics | | | | | | |
| A1 | Minimum data eye opening ⁽⁸⁾ | | 100 | | 600 | mV |
| A1 | Minimum clock eye opening ⁽⁸⁾ | | 295 | | 600 | mV |
| A2 | Maximum signal swing ^{(8) (9)} | | | | 600 | mV |
| X1 | Maximum eye closure ⁽⁸⁾ | | | | 0.275 | UI |
| X2 | Maximum eye closure ⁽⁸⁾ | | | | 0.4 | UI |
| t _{DRIFT} | Drift between Clock and Data between Training Patterns | | | | 20 | ps |
| Capacitance | | | | | | |
| C _{IN} | Input capacitance LVC MOS | f = 1MHz | | | 10 | pF |
| C _{IN} | Input capacitance LSIF (low speed interface) | f = 1MHz | | | 20 | pF |
| C _{IN} | Input capacitance HSSI (high speed serial interface) - Differential - Clock and Data pins | f = 1MHz | | | 5 | pF |
| C _{OUT} | Output capacitance | f = 1MHz | | | 10 | pF |

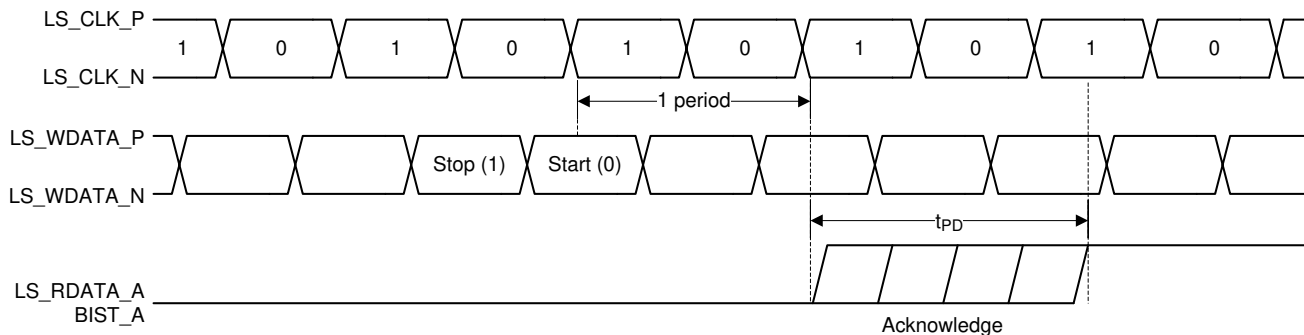
- (1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
- (2) All voltage values are with respect to the ground pins (V_{SS}).
- (3) To prevent excess current, the supply voltage delta | V_{DDA} – V_{DD} | must be less than specified limit.
- (4) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than specified limit.
- (5) Supply power dissipation based on three global resets in 200μs.
- (6) LVC MOS input specifications are for pin DMD_DEN_ARSTZ.
- (7) LVC MOS output specification is for pins LS_RDATA_A and LS_RDATA_B.
- (8) Refer to [Figure 6-12](#) (1e-12 BER).
- (9) Defined in the *Recommended Operating Conditions*.

5.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|---|------|-----|------|------|
| t _{pd} | Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. ⁽¹⁾ | C _L = 5pF | | | 11.1 | ns |
| t _{pd} | Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. ⁽¹⁾ | C _L = 10pF | | | 11.3 | ns |
| | Slew rate, LS_RDATA | 20% to 80%, C _L < 40p | 0.35 | | | V/ns |
| | Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B | 50 – (C2Q _{rise} – C2Q _{fall}) × 130e6 × 100 | 40% | | 60% | |

- (1) See [Figure 6-3](#).



5-3. Switching Characteristics

5.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------------------|--|-------|-----|-------|------|
| LVC MOS | | | | | | |
| t_r | Rise time ⁽¹⁾ | 20% to 80% reference points | | | 25 | ns |
| t_f | Fall time ⁽¹⁾ | 80% to 20% reference points | | | 25 | ns |
| Low Speed Interface (LSIF) | | | | | | |
| t_r | Rise time ⁽²⁾ | 20% to 80% reference points | | | 450 | ps |
| t_f | Fall time ⁽²⁾ | 80% to 20% reference points | | | 450 | ps |
| $t_{W(H)}$ | Pulse duration high ⁽³⁾ | LS_CLK. 50% to 50% reference points | 3.1 | | | ns |
| $t_{W(L)}$ | Pulse duration low ⁽³⁾ | LS_CLK. 50% to 50% reference points | 3.1 | | | ns |
| t_{su} | Setup time ⁽⁴⁾ | LS_WDATA valid before rising edge of LS_CLK (differential) | 1.5 | | | ns |
| t_h | Hold time ⁽⁴⁾ | LS_WDATA valid after rising edge of LS_CLK (differential) | 1.5 | | | ns |
| High Speed Serial Interface (HSSI) | | | | | | |
| t_r | Rise time ⁽⁵⁾ , Data | from -A1 to A1 minimum eye height specification | 50 | | 115 | ps |
| t_r | Rise time ⁽⁵⁾ , Clock | from -A1 to A1 minimum eye height specification | 50 | | 135 | ps |
| t_f | Fall time ⁽⁵⁾ , Data | from A1 to -A1 minimum eye height specification | 50 | | 115 | ps |
| t_f | Fall time ⁽⁵⁾ , Clock | from A1 to -A1 minimum eye height specification | 50 | | 135 | ps |
| $t_{W(H)}$ | Pulse duration high ⁽⁶⁾ | DCLK. 50% to 50% reference points | 0.275 | | | ns |
| $t_{W(L)}$ | Pulse duration low ⁽⁶⁾ | DCLK. 50% to 50% reference points | 0.275 | | | ns |
| t_c | Cycle time ⁽⁶⁾ | DCLK | 0.625 | | 0.833 | ns |

(1) See Figure 6-9 and Figure 6-10 LVC MOS Rise, Fall Time Slew Rate Figures. Specification is for DMD_DEN_ARSTZ pin (LVC MOS).

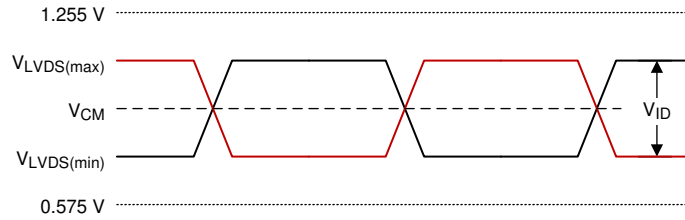
(2) See Figure 6-6 for rise and fall time for LSIF.

(3) See Figure 6-5 for pulse duration high and low time for LSIF.

(4) See Figure 6-5 for setup and hold time for LSIF.

(5) See Figure 6-11 for rise and fall time for HSSI.

(6) See Figure 6-13 for pulse duration high and low and cycle time for HSSI.



A. See 式 1 and 式 2

図 5-4. LSIF Waveform Requirements

$$V_{LVDS(max)} = V_{CM(max)} + \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (1)$$

$$V_{LVDS(min)} = V_{CM(min)} - \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (2)$$

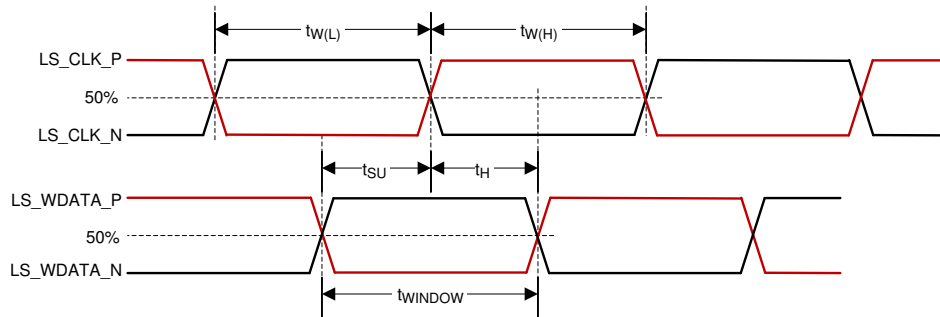


図 5-5. LSIF Timing Requirements

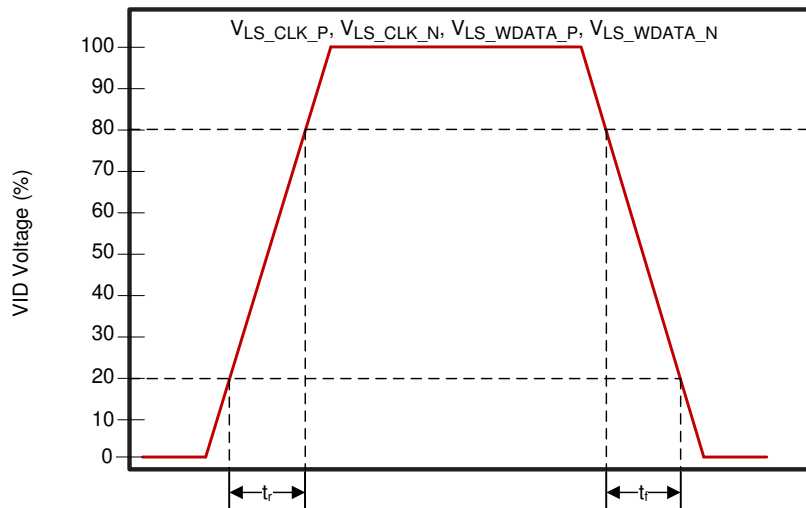


図 5-6. LSIF Rise, Fall Time Slew Rate

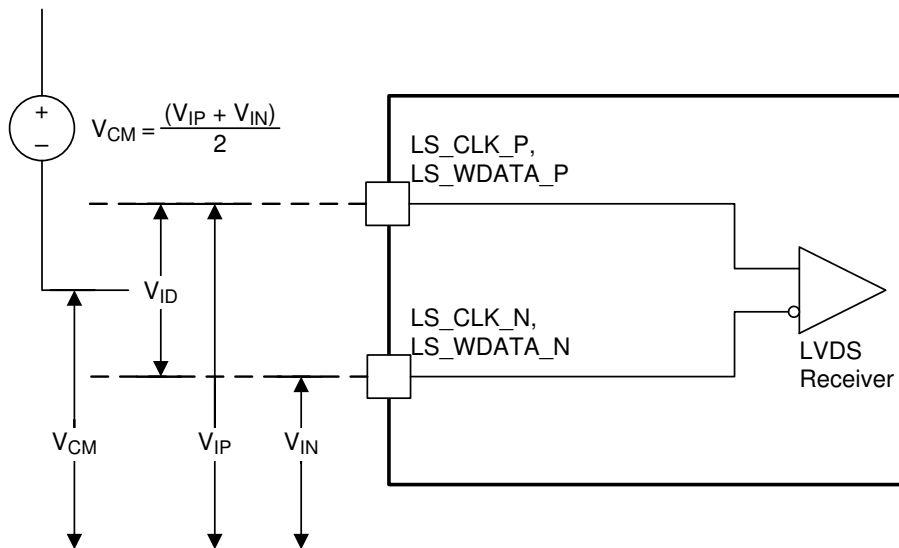


図 5-7. LSIF Voltage Requirements

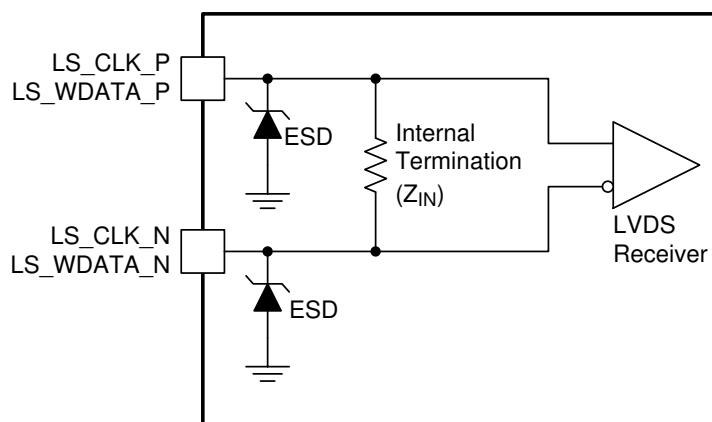


図 5-8. LSIF Equivalent Input

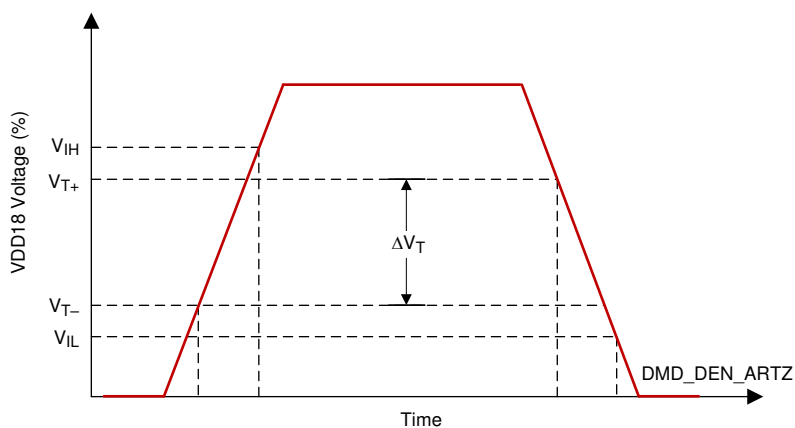


図 5-9. LVCMOS Input Hysteresis

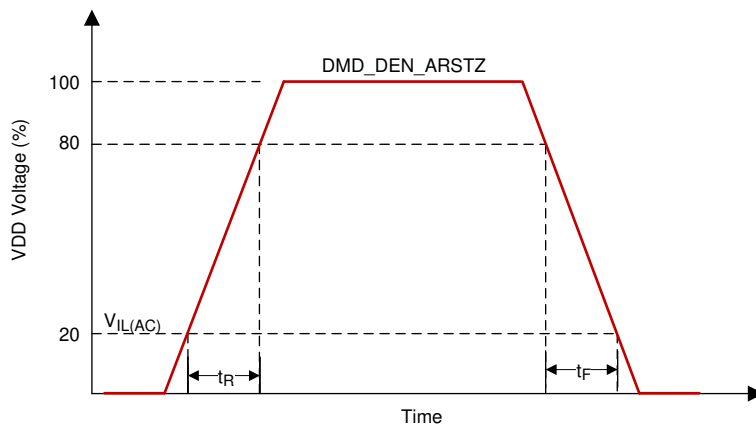
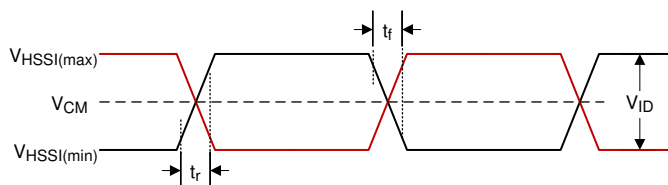


図 5-10. LVC MOS Rise, Fall Time Slew Rate



A. See 式 3 and 式 4

図 5-11. HSSI Waveform Requirements

$$V_{HSSI(max)} = V_{CM(max)} + \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (3)$$

$$V_{HSSI(min)} = V_{CM(min)} - \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (4)$$

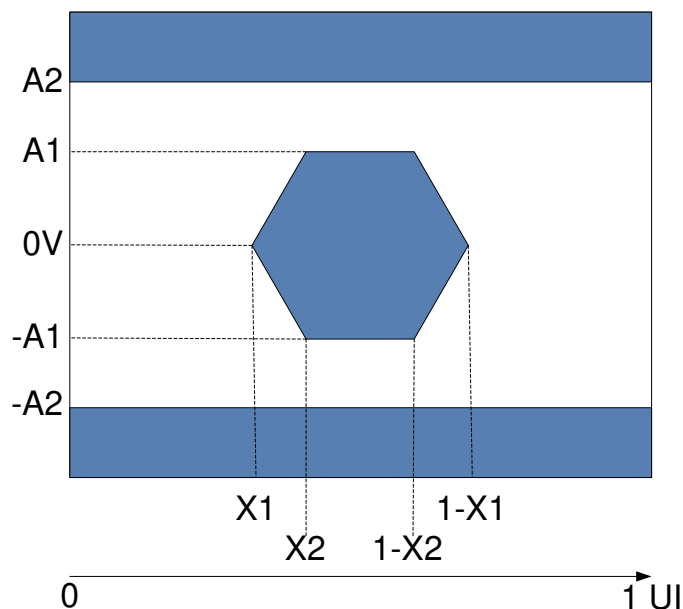


図 5-12. HSSI Eye Characteristics

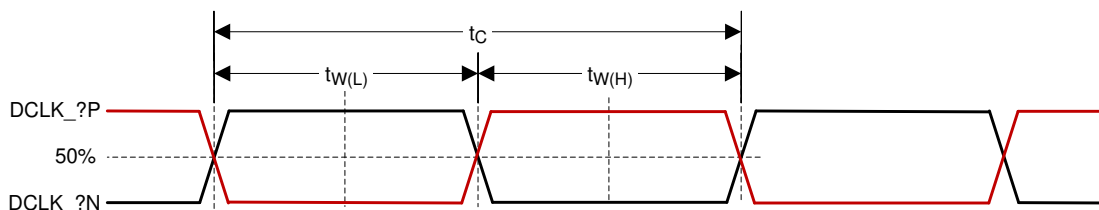


図 5-13. HSSI CLK Characteristics

5.9 System Mounting Interface Loads

| PARAMETER | MIN | TYP | MAX | UNIT |
|--|-----|-----|-----|------|
| When loads are applied on both the electrical and thermal interface areas | | | | |
| Maximum load to be applied to the electrical interface area ⁽¹⁾ | | | 111 | N |
| Maximum load to be applied to the thermal interface area ⁽¹⁾ | | | 111 | N |
| When load is applied on the electrical interface area only | | | | |
| Maximum load to be applied to the electrical interface area ⁽¹⁾ | | | 222 | N |
| Maximum load to be applied to the thermal interface area ⁽¹⁾ | | | 0 | N |

(1) The load should be applied uniformly in the corresponding areas shown in Figure 6-14.

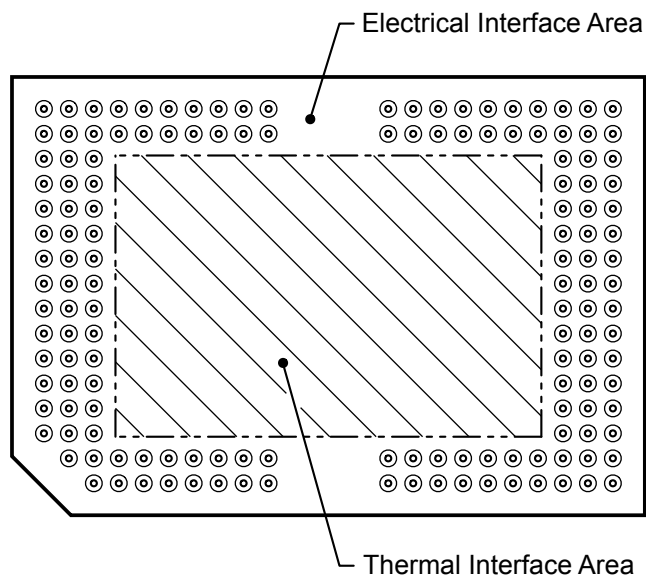


図 5-14. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

| SYMBOL | PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------|--|--|-----|--------|-----|-------------------|
| M | Number of active columns ⁽¹⁾ | | | 1920 | | micromirrors |
| N | Number of active rows ⁽¹⁾ | | | 1080 | | micromirrors |
| P | Micromirror (pixel) pitch ⁽¹⁾ | | | 7.6 | | um |
| | Micromirror active array width ⁽¹⁾ | (micromirror pitch) × (number of active columns) | | 14.592 | | mm |
| | Micromirror active array height ⁽¹⁾ | (micromirror pitch) × (number of active rows) | | 8.208 | | mm |
| | Micromirror active border ⁽²⁾ | Pond of micromirror (POM) | | 14 | | micromirrors/side |

(1) See [Figure 6-15](#).

(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

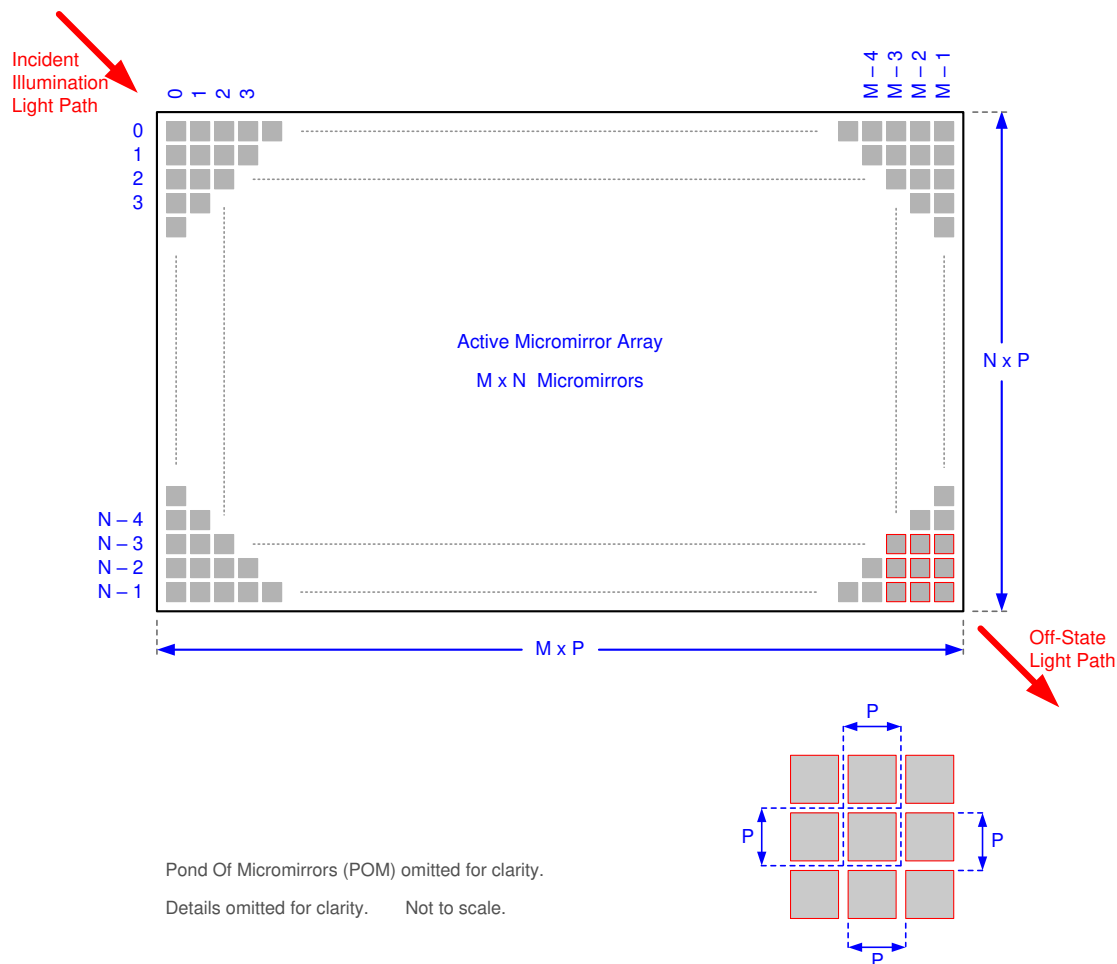
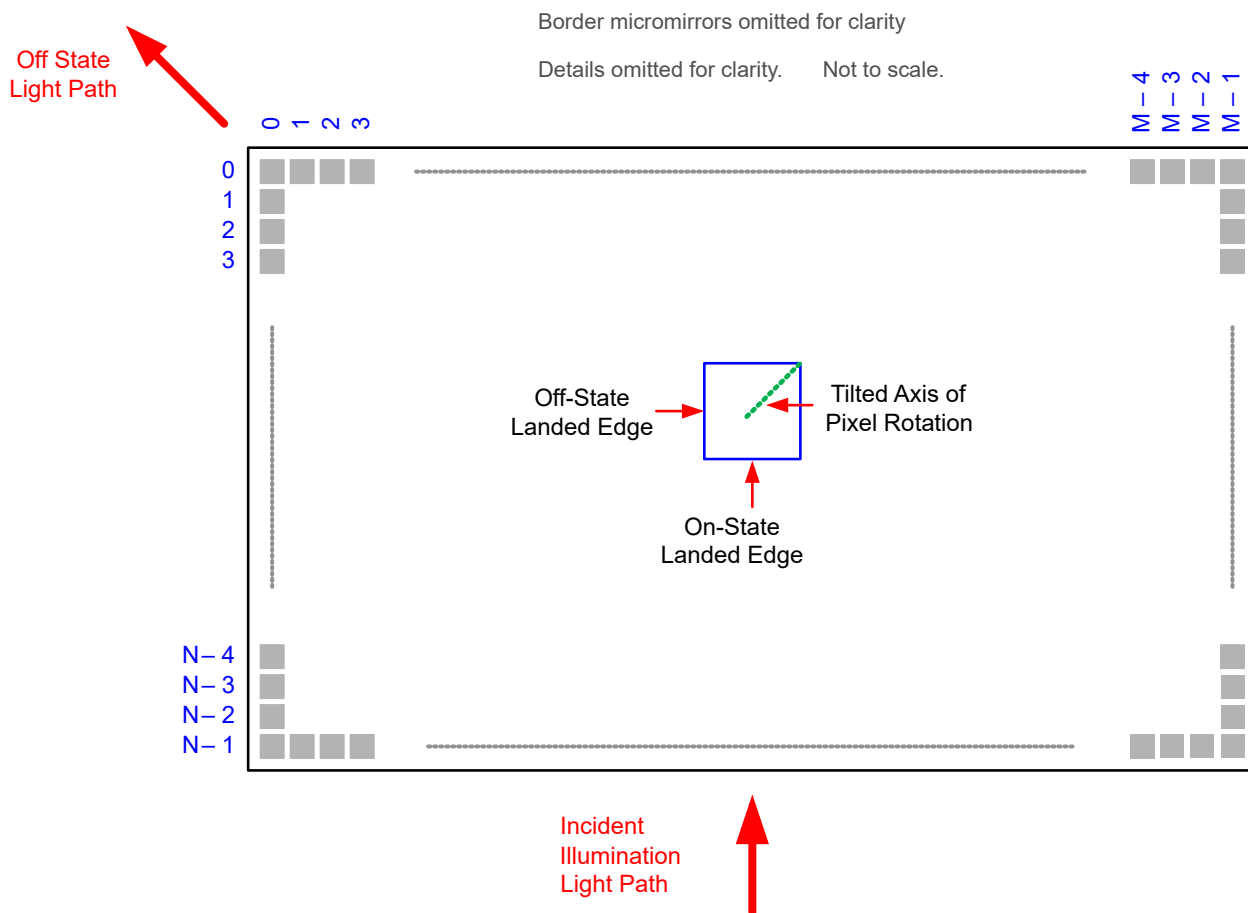


図 5-15. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

| PARAMETER | | TEST CONDITION | MIN | NOM | MAX | UNIT |
|--|--|--------------------------------|-----|-----|-----|--------------|
| Micromirror tilt angle, variation device to device ⁽²⁾ ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾ | | Landed State ⁽¹⁾ | 11 | 12 | 13 | degrees |
| Image performance ⁽⁶⁾ | Bright pixel(s) in active area ⁽⁷⁾ | Gray 10 screen ⁽¹⁰⁾ | | | 0 | micromirrors |
| | Bright pixel(s) in the POM ⁽⁷⁾ ⁽⁹⁾ | Gray 10 screen ⁽¹⁰⁾ | | | 1 | |
| | Dark pixel(s) in the active area ⁽⁸⁾ | White screen ⁽¹¹⁾ | | | 4 | |
| | Adjacent pixel(s) ⁽¹²⁾ | Any screen | | | 0 | |
| | Unstable pixel(s) in active area ⁽¹³⁾ | Any screen | | | 0 | |

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) This represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (4) For some applications it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs the micromirror tilt angle variations within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
- (5) See figure [5-16](#).
- (6) Conditions of acceptance. All DMD image performance returns are evaluated using the following projected image test conditions:
 - Test set degamma shall be linear.
 - Test set brightness and contrast shall be set to nominal.
 - The diagonal size of the projected image shall be a minimum of 60 inches.
 - The projections screen shall be a 1× gain.
 - The projected image shall be inspected from an 8 foot minimum viewing distance.
 - The image shall be in focus during all image performance tests.
- (7) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
- (8) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
- (9) POM definition: The rectangular border of off-state mirrors surrounding the active area.
- (10) Gray 10 screen definition: A full screen with RGB values set to R=10/255, G=10/255, B=10/255.
- (11) White screen definition: A full screen with RGB values set to R=255/255, G=255/255, B=255/255.
- (12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point. Also referred to as a cluster.
- (13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.



- A. Pond of micromirrors (POM) omitted for clarity.
 B. Refer to section [セクション 5.10](#) table for M, N, and P specifications.

図 5-16. Micromirror Landed Orientation and Tilt

5.12 Window Characteristics

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-----------------------------|------------------------|-----------------|-----|-----|------|
| Window material designation | WLP | Corning EagleXG | | | |
| Window refractive index | at wavelength 546.1 nm | 1.5119 | | | |

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP651NE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

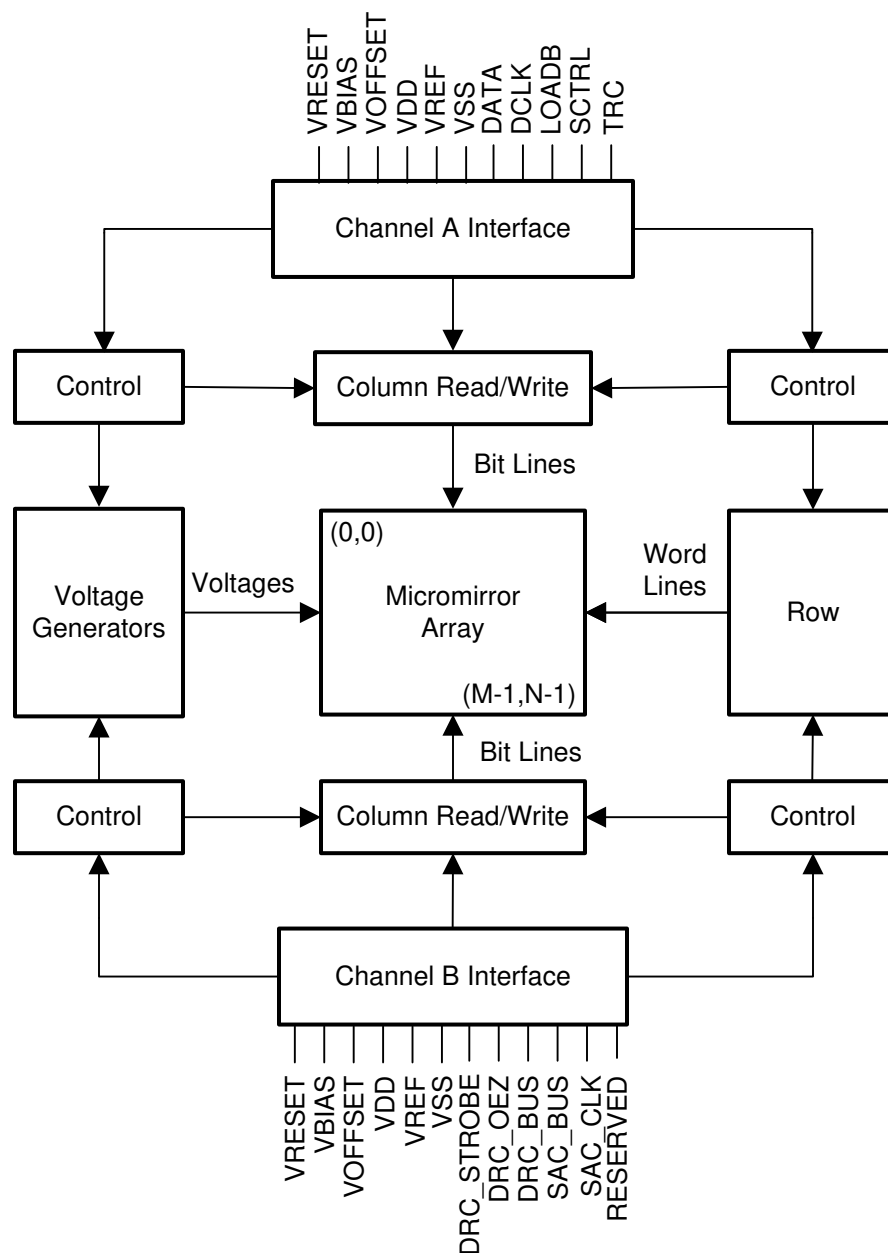
6 Detailed Description

6.1 Overview

The DMD is a 0.65-inch diagonal spatial light modulator that consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables frame rates of up to 240Hz to be displayed. The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to [セクション 6.2](#). The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.65" 1080p chipset is comprised of the DLP651NE DMD, [DLPC7530](#) display controller, the [DLPA100](#) power management and motor driver. To ensure reliable operation, the DLP651NE DMD must always be used with the DLP display controller and the power and motor specified in the chipset.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Interface

The DMD requires four DC voltages: 1.8V source, V_{OFFSET} , V_{RESET} , and V_{BIAS} . In a typical configuration, 3.3V is created by the [DLPA100](#) power management and motor driver and is used on the DMD board to create the 1.8V. The TI voltage regulator [TPS65145](#) takes in the 3.3V and outputs V_{OFFSET} , V_{RESET} , V_{BIAS} .

6.3.2 Timing

The data sheet specifies the timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depict the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC7530 display controller. See the [DLPC7530 Display Controller Data Sheet](#) or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and active area could occur.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level to be acceptable.

6.6 Micromirror Array Temperature Calculation

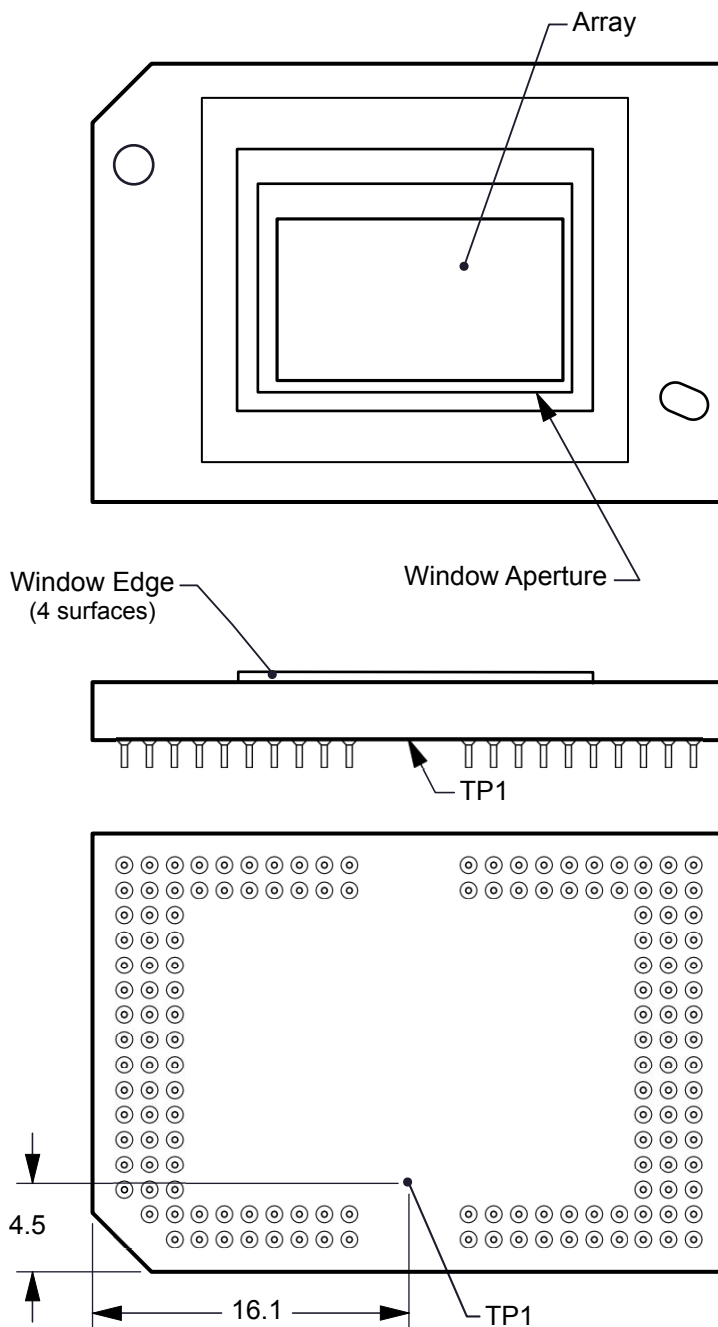


図 6-1. DMD Thermal Test Point

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1) is provided by the following equations:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}}) \quad (5)$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}} \quad (6)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- T_{CERAMIC} = Measured ceramic temperature (°C) (TP1 location)
- $R_{\text{ARRAY-TO-CERAMIC}}$ = Thermal resistance of package specified in [Thermal Information](#) from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{\text{ELECTRICAL}}$ = Nominal electrical power (W)
- Q_{INCIDENT} = Incident illumination optical power (W)
- $Q_{\text{ILLUMINATION}}$ = (DMD average thermal absorptivity \times Q_{INCIDENT}) (W)
- DMD average thermal absorptivity = 0.45

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 3.0W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multi-chip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{\text{INCIDENT}} = 48\text{W (measured)} \quad (7)$$

$$T_{\text{CERAMIC}} = 55.0^{\circ}\text{C (measured)} \quad (8)$$

$$Q_{\text{ELECTRICAL}} = 3.0\text{W} \quad (9)$$

$$Q_{\text{ARRAY}} = 3.0\text{W} + (0.50 \times 48\text{W}) = 24.6\text{W} \quad (10)$$

$$T_{\text{ARRAY}} = 55.0^{\circ}\text{C} + (24.6\text{W} \times 0.6^{\circ}\text{C/W}) = 69.8^{\circ}\text{C} \quad (11)$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{\text{UV}} = [OP_{\text{UV-RATIO}} \times Q_{\text{INCIDENT}}] \times 1000\text{mW/W} \div A_{\text{ILL}} \text{ (mW/cm}^2\text{)}$
- $ILL_{\text{VIS}} = [OP_{\text{VIS-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $ILL_{\text{IR}} = [OP_{\text{IR-RATIO}} \times Q_{\text{INCIDENT}}] \times 1000\text{mW/W} \div A_{\text{ILL}} \text{ (mW/cm}^2\text{)}$
- $ILL_{\text{BLU}} = [OP_{\text{BLU-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $ILL_{\text{BLU1}} = [OP_{\text{BLU1-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $A_{\text{ILL}} = A_{\text{ARRAY}} \div (1 - OV_{\text{ILL}}) \text{ (cm}^2\text{)}$

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV-RATIO}$ = ratio of the optical power for wavelengths $<410nm$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS-RATIO}$ = ratio of the optical power for wavelengths $\geq 410nm$ and $\leq 800nm$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR-RATIO}$ = ratio of the optical power for wavelengths $>800nm$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU-RATIO}$ = ratio of the optical power for wavelengths $\geq 410nm$ and $\leq 475nm$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1-RATIO}$ = ratio of the optical power for wavelengths $\geq 410nm$ and $\leq 440nm$ to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$$Q_{INCIDENT} = 48W \text{ (measured)}$$

$$A_{ARRAY} = (14.5920mm \times 8.2080mm) \div 100mm^2/cm^2 = 1.1977cm^2 \text{ (data sheet)}$$

$$OV_{ILL} = 16.3\% \text{ (optical model)}$$

$$OP_{UV-RATIO} = 0.00017 \text{ (spectral measurement)}$$

$$OP_{VIS-RATIO} = 0.99977 \text{ (spectral measurement)}$$

$$OP_{IR-RATIO} = 0.00006 \text{ (spectral measurement)}$$

$$OP_{BLU-RATIO} = 0.28100 \text{ (spectral measurement)}$$

$$OP_{BLU1-RATIO} = 0.03200 \text{ (spectral measurement)}$$

$$A_{ILL} = 1.1977cm^2 \div (1 - 0.163) = 1.4310cm^2$$

$$ILL_{UV} = [0.00017 \times 48W] \times 1000mW/W \div 1.4310cm^2 = 5.702mW/cm^2$$

$$ILL_{VIS} = [0.99977 \times 48W] \div 1.4310cm^2 = 33.54W/cm^2$$

$$ILL_{IR} = [0.00006 \times 48W] \times 1000mW/W \div 1.4310cm^2 = 2.013mW/cm^2$$

$$ILL_{BLU} = [0.28100 \times 48W] \div 1.4310cm^2 = 9.43W/cm^2$$

$$ILL_{BLU1} = [0.03200 \times 48W] \div 1.4310cm^2 = 1.07W/cm^2$$

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

$$Q_{AP-ILL} = [Q_{INCIDENT} \times OP_{AP_ILL_RATIO}] + A_{AP_ILL} (W/cm^2)$$

where:

- Q_{AP-ILL} = window aperture illumination overfill (W/cm^2)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP_ILL_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- A_{AP-ILL} = size of the window aperture critical area (cm^2) (data sheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

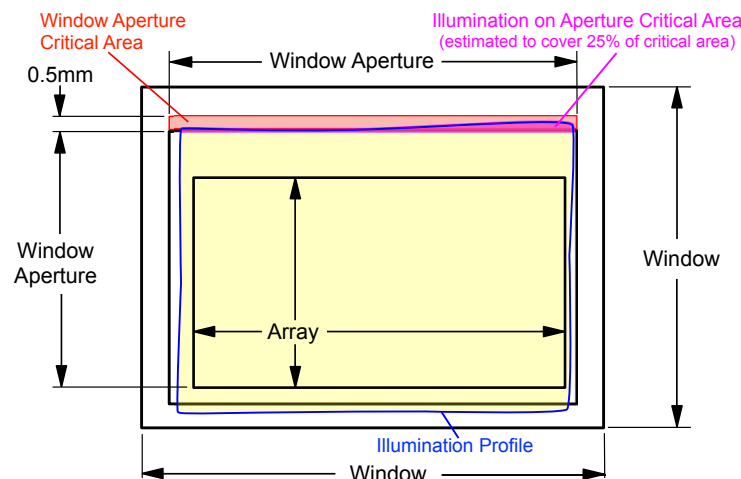


図 6-2. Illumination Overfill Diagram - Critical Area

$Q_{INCIDENT}=48W$ (measured)

$OP_{AP_ILL_RATIO}=0.312\%$ (optical model)

$OV_{CA_RATIO}=25\%$ (optical model)

Length of the window aperture for critical area =1.5998cm (data sheet mechanical icd)

Width of critical area=0.050cm (data sheet)

$$A_{AP-ILL}=1.5998\text{cm} \times 0.050\text{cm}=0.079990\text{cm}^2$$

$$Q_{AP-ILL}=(48\text{W} \times 0.00312)+(0.079990\text{cm}^2 \times 0.25)=7.5\text{W}/\text{cm}^2$$

6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in *Maximum Recommended Array Temperature—Derating Curve*. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 6-1.

表 6-1. Grayscale Value and Landed Duty Cycle

| GRAYSCALE VALUE | LANDED DUTY CYCLE |
|-----------------|-------------------|
| 0% | 0/100 |
| 10% | 10/90 |
| 20% | 20/80 |
| 30% | 30/70 |
| 40% | 40/60 |
| 50% | 50/50 |
| 60% | 60/40 |
| 70% | 70/30 |
| 80% | 80/20 |
| 90% | 90/10 |
| 100% | 100/0 |

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use this equation to calculate the landed duty cycle of a given pixel during a given time period:

Landed Duty Cycle =

(Red_Cycle_% × Red_Scale_Value) +

(Green_Cycle_% × Green_Scale_Value) +

(Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities are shown in 表 6-2 and 表 6-3.

**表 6-2. Example Landed Duty Cycle for Full-Color,
Color Percentage**

| CYCLE PERCENTAGE | | |
|------------------|-------|------|
| RED | GREEN | BLUE |
| 30% | 50% | 20% |

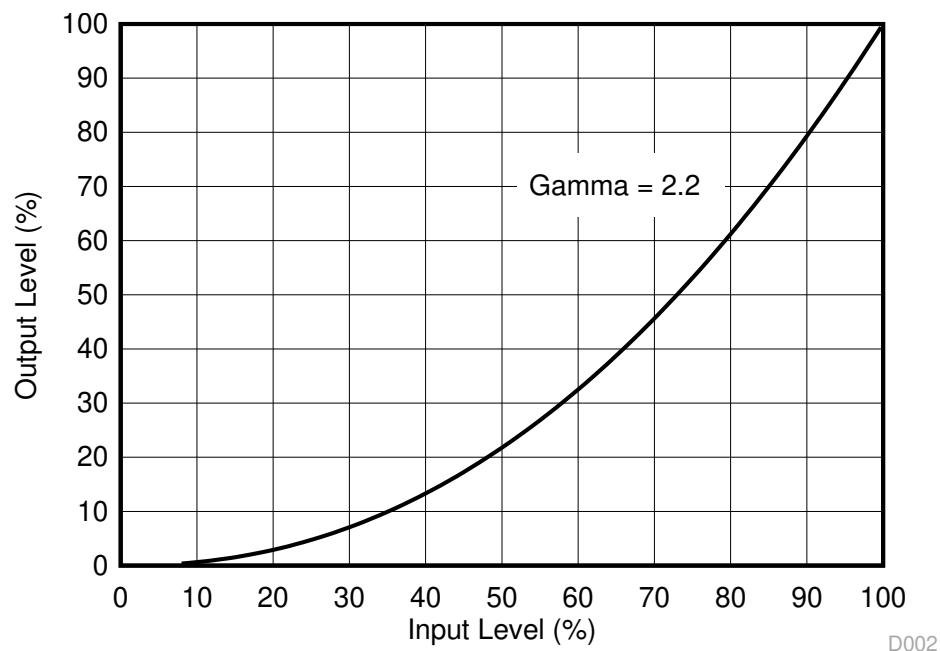
表 6-3. Example Landed Duty Cycle for Full-Color

| SCALE VALUE | | | LANDED DUTY CYCLE |
|-------------|-------|------|-------------------|
| RED | GREEN | BLUE | |
| 0% | 0% | 0% | 0/100 |
| 100% | 0% | 0% | 30/70 |
| 0% | 100% | 0% | 50/50 |
| 0% | 0% | 100% | 20/80 |
| 0% | 12% | 0% | 6/94 |
| 0% | 0% | 35% | 7/93 |
| 60% | 0% | 0% | 18/82 |
| 0% | 100% | 100% | 70/30 |
| 100% | 0% | 100% | 50/50 |
| 100% | 100% | 0% | 80/20 |
| 0% | 12% | 35% | 13/87 |
| 60% | 0% | 35% | 25/75 |
| 60% | 12% | 0% | 24/76 |
| 100% | 100% | 100% | 100/0 |

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC7530 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form $\text{Output_Level} = A \times \text{Input_Level}^{\text{Gamma}}$, where A is a scaling factor that is typically set to 1.

In the DLPC7530 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 6-3.

**図 6-3. Example of Gamma = 2.2**

From [Figure 6-3](#), if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing that occurs before the DLPC7530 controller.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

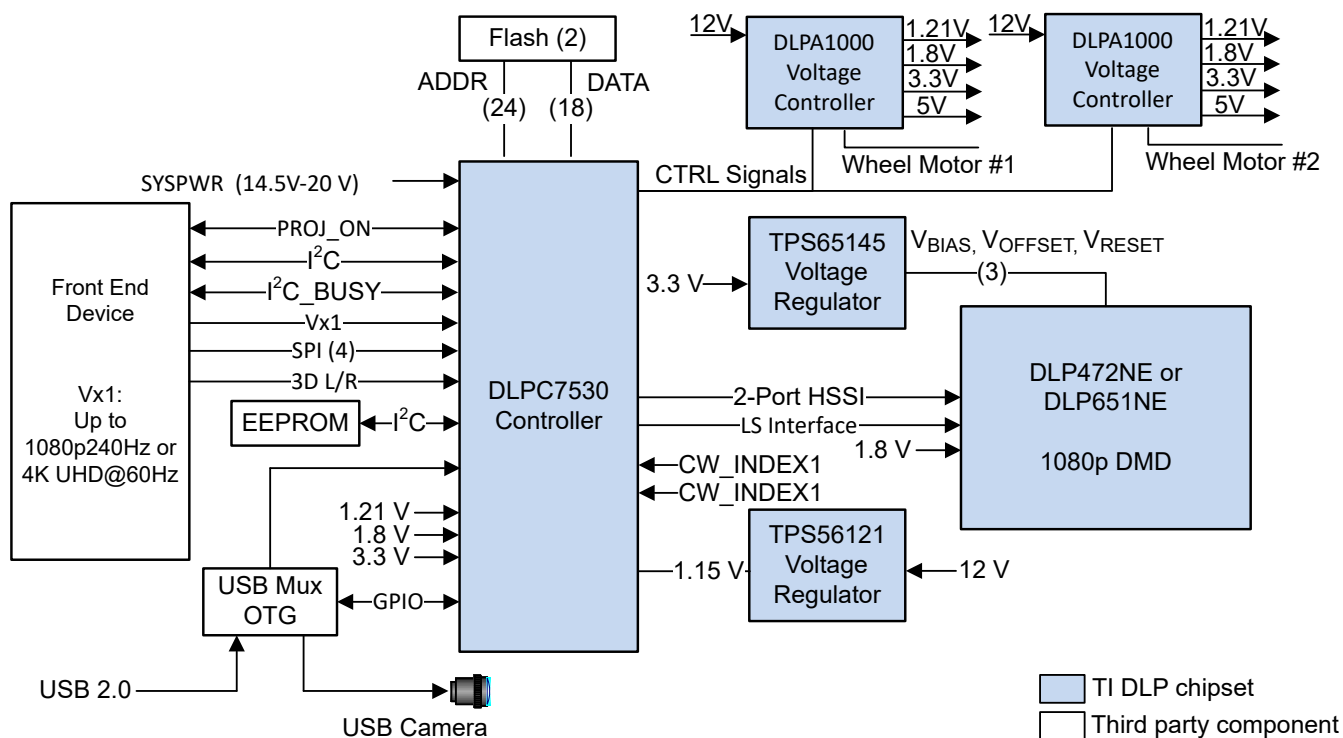
7.1 Application Information

DMDs are spatial light modulators, which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC7530 controller. Typical applications using the DLP651NE DMD include Laser TVs, smart projectors, and enterprise projectors.

DMD power-up and power-down sequencing is strictly controlled by the DLPC7530 through the TPS65145 PMIC. Refer to [セクション 8](#) for power-up and power-down specifications. To ensure reliable operation, the DLP651NE DMD must always be used with [DLPC7530](#) controller, a [DLPA100](#) PMIC/motor driver, and a [TPS65145](#) PMIC.

7.2 Typical Application

The DLP651NE DMD combined with DLPC7530 digital controller and a power management device provides full 1080p resolution for bright, colorful display applications. A typical display system using laser phosphor illumination combines the DLP651NE DMD, [DLPC7530](#) display controller, [TPS65145](#) voltage regulator and [DLPA100](#) PMIC and motor driver. The diagram below shows a system block diagram for the Laser Phosphor configuration of the DLP 0.65" 1080p chipset. [Figure 7-2](#) shows a system block diagram for the LED configuration of the DLP 0.65" 1080p chipset. The components include DLP651NE DMD, [DLPC7530](#) display controller and [DLPA100](#) PMIC and motor driver and a [TPS65145](#) PMIC.



7-1. Typical Full HD Laser Phosphor Application Diagram

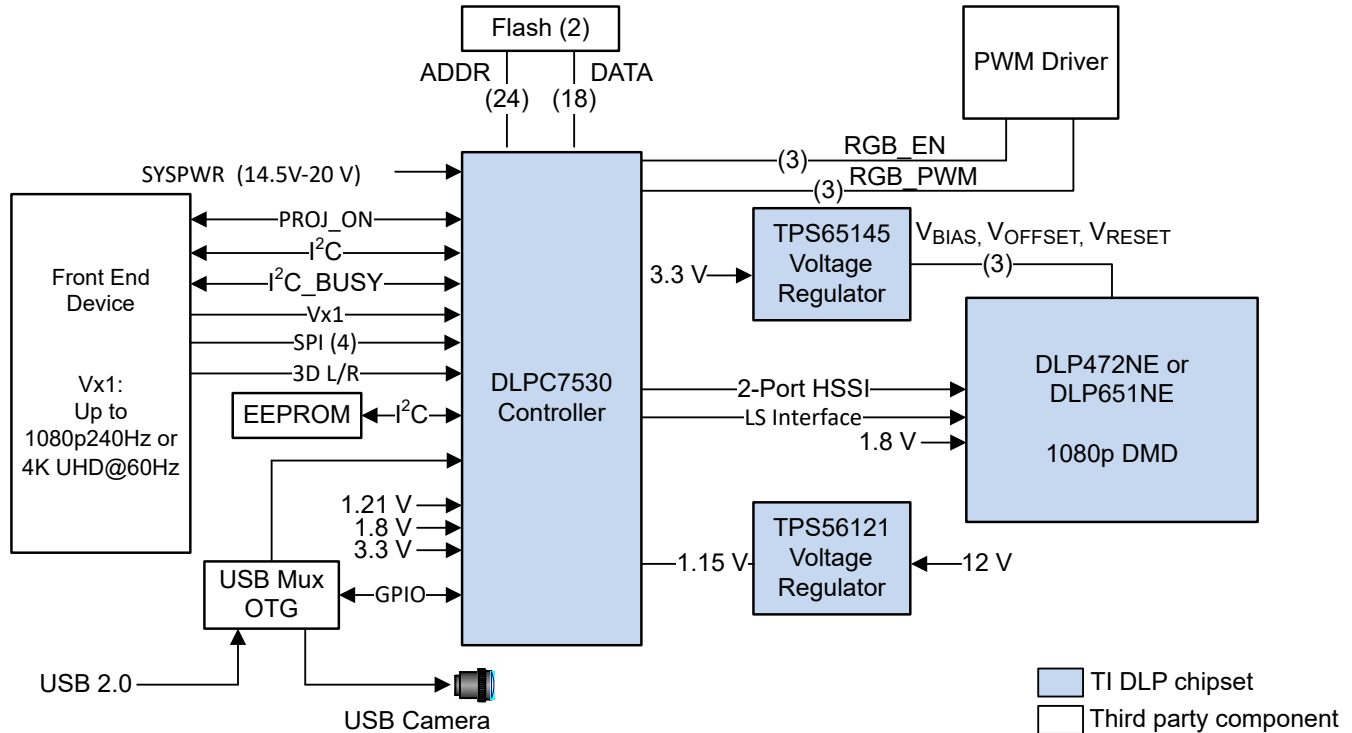


図 7-2. Typical Full HD LED Application Diagram

7.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness have a major effect on the overall system design and size.

The display system uses the DLP651NE DMD as the core imaging device and contains a 0.65-inch array of micromirrors. The DLPC7530 controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The DLPA100 PMIC serves as a voltage regulator for the controller, and color filter wheel and phosphor wheel motor control. The TPS65145 provides the DMD reset, offset, and bias voltages. The LMR33630C provides 1.8V power to the DLP651NE DMD.

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP651NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with DLPC7530 display controller and the TPS65145 PMIC and DLPA100. Refer to the DMD board reference design and DLPC7530 reference design for layout and design recommendations.

7.2.3 Application Curve

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determines the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. 図 7-3 describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit.

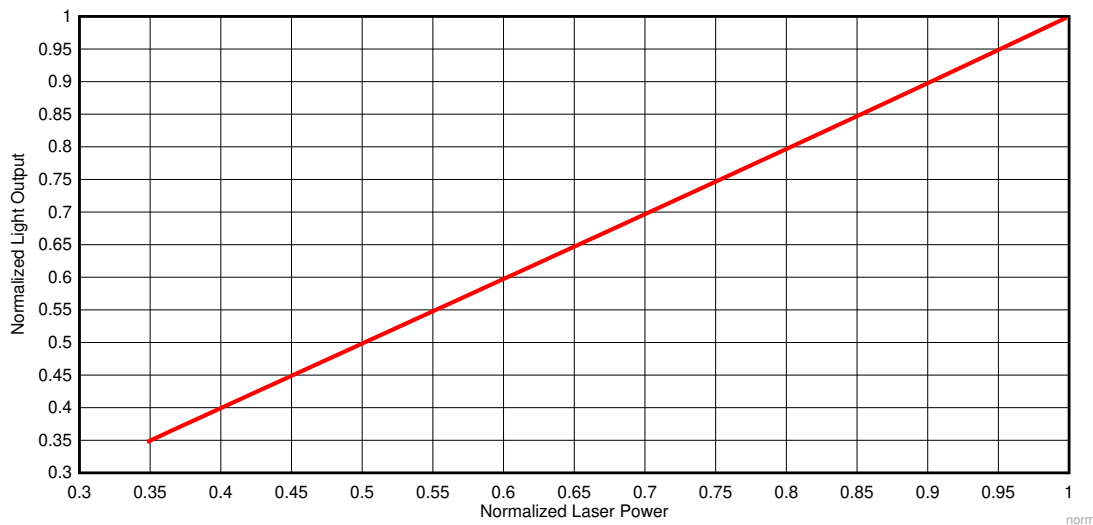
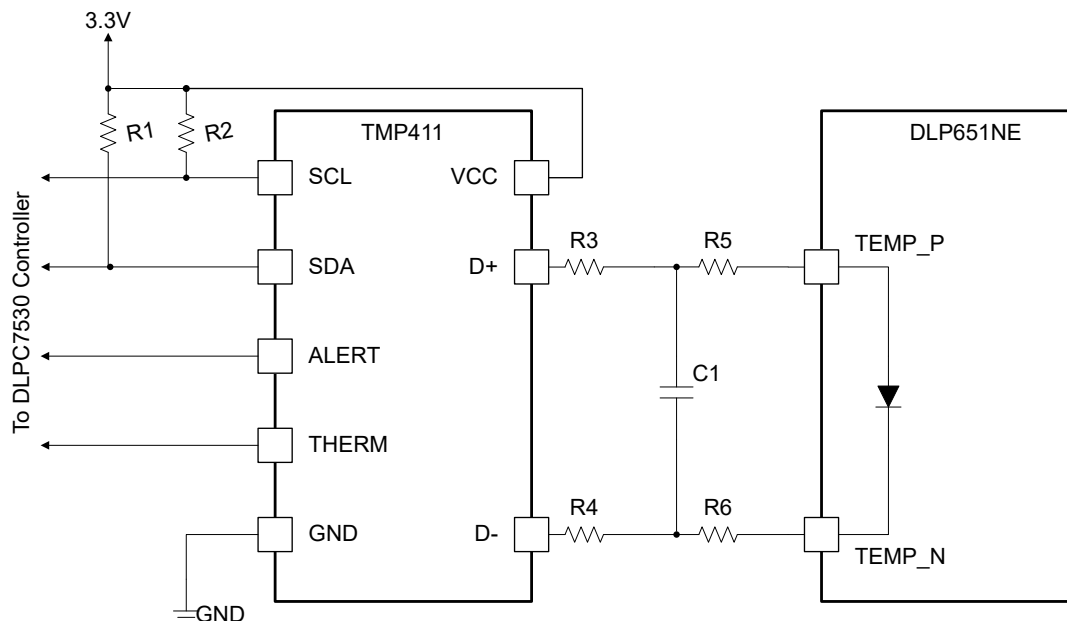


図 7-3. Normalized Light Output vs Normalized Laser Power for Laser Phosphor Illumination

7.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in the sample schematic. The software application contains functions to configure the TMP411 to read the DLP651NE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so on. All communication between the TMP411 and the DLPC7530 controller happens over the I²C interface. The TMP411 connects to the DMD through the pins outlined in *Pin Functions*.

Leave TEMP_N and TEMP_P pins unconnected (NC) if the temp sensor is not used.



- A. Details are omitted for clarity.
- B. See the [TMP411](#) data sheet for the system board layout recommendation.
- C. See the [TMP411](#) data sheet for suggested component values for R1, R2, R3, R4, and C1.
- D. R5 = 0Ω. R6 = 0Ω. Place 0Ω resistors close to the DMD package pins.

図 7-4. TMP411 Sample Schematic

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

注意

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in [図 8-1](#).

V_{BIAS} , V_{DD} , V_{OFFSET} , and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

8.1 Power Supply Sequence Requirements

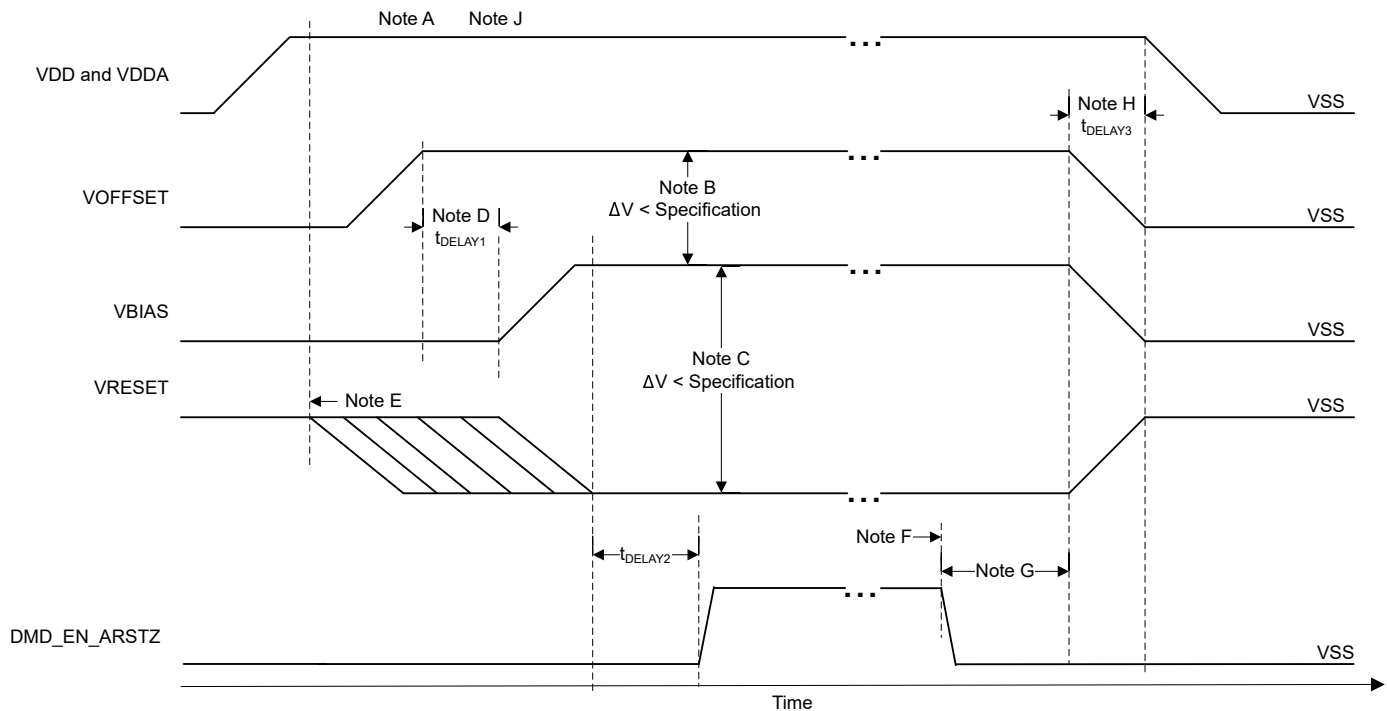
| SYMBOL | PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------------|-------------------|---|-----|-----|-----|---------|
| t_{DELAY1} | Delay requirement | from V_{OFFSET} power up to V_{BIAS} power up | 1 | 2 | | ms |
| t_{DELAY2} | Delay requirement | from V_{BIAS} and V_{RESET} powered on and stable to DMD_EN_ARSTZ going high | 20 | | | μ s |
| t_{DELAY3} | Delay requirement | from V_{OFFSET} , V_{BIAS} and V_{RESET} powered down to when VDD and VDDA can power down | 50 | | | μ s |

8.2 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} must always start and settle before V_{OFFSET} plus t_{DELAY1} specified in the *Power Supply Sequence Requirements*, V_{BIAS} , and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} .
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the *Absolute Maximum Ratings*, *Recommended Operating Conditions*, and the *DMD Power Supply Requirements*.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} has settled at operating voltage listed in the *Recommended Operating Conditions*.

8.3 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} must be supplied until after V_{BIAS} , V_{RESET} , and V_{OFFSET} are discharged to within the specified limit of ground. See the *Power Supply Sequence Requirements*.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} .
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the *Absolute Maximum Ratings*, the *Recommended Operating Conditions*, and the *DMD Power Supply Requirements*.
- During power-down, LVCMOS input pins must be less than specified in the *Recommended Operating Conditions*.



- A. See the *Pin Functions* table.
- B. To prevent excess current, the supply voltage difference $|V_{BIAS} - V_{OFFSET}|$ must be less than the specified limit in the *Recommended Operating Conditions*.
- C. To prevent excess current, the supply difference $|V_{BIAS} - V_{RESET}|$ must be less than the specified limit in the *Recommended Operating Conditions*.
- D. V_{BIAS} must power up after V_{OFFSET} has powered up, per t_{DELAY1} specification in the *Power Supply Sequence Requirements*.
- E. V_{RESET} , V_{OFFSET} and V_{BIAS} ramps must start after VDD and VDDA are powered up and stable.
- F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS} , V_{RESET} and V_{OFFSET} .
- G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware DMD_EN_ARSTZ goes low.
- H. V_{DD} must remain powered on and stable until after V_{OFFSET} , V_{BIAS} , and V_{RESET} are powered off, per t_{DELAY3} specification in the *Power Supply Sequence Requirements*.
- I. To prevent excess current, the supply voltage delta $|V_{DDA} - V_{DD}|$ must be less than specified limit in the *Recommended Operating Conditions*.
- J. Not to scale. Details are omitted for clarity.

図 8-1. DMD Power Supply Requirements

9 Layout

9.1 Layout Guidelines

The DLP651NE DMD is part of a chipset that is controlled by the [DLPC7530](#) display controller in conjunction with the [TPS65145](#) PMIC and the [DLPA100](#) power and motor controller. These guidelines are targeted at designing a PCB board with the DLP651NE DMD. The DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic including double data rate 3.2Gbps and 250Mbps differential data buses run to the DMD. TI recommends that full or mini power planes are used for V_{OFFSET} , V_{RESET} , and V_{BIAS} . Solid planes are required for ground (V_{SS}). The target impedance for the PCB is $50\Omega \pm 10\%$ with exceptions listed in [表 9-1](#). TI recommends a 10-layer stack-up as described in [表 9-2](#). TI recommends manufacturing the PCB with a high quality FR-4 material.

9.2 Impedance Requirements

TI recommends a target impedance for the PCB of $50\Omega \pm 10\%$ for all signals. The exceptions are listed in [表 9-1](#).

表 9-1. Special Impedance Requirements

| SIGNAL TYPE | SIGNAL NAME | IMPEDANCE (Ω) |
|---------------------------------|---|--|
| DMD High Speed Data Signals | DMD_HSSI0_N_(0...7), DMD_HSSI0_P_(0...7), DMD_HSSI1_N_(0...7), DMD_HSSI1_P_(0...7), DMD_HSSI0_CLK_N, DMD_HSSI0_CLK_P, DMD_HSSI1_CLK_N, DMD_HSSI1_CLK_P | 100 Ω differential (50 Ω single ended) |
| DMD Low Speed Interface Signals | DMD_LS0_WDATA_N, DMD_LS0_WDATA_P, DMD_LS0_CLK_N, DMD_LS0_CLK_P | 100 Ω differential (50 Ω single ended) |

9.3 Layers

[表 9-2](#) shows the layer stack-up and copper weight for each layer.

表 9-2. Layer Stack-Up

| LAYER NO. | LAYER NAME | COPPER WT. (oz.) | COMMENTS |
|-----------|---|--------------------------|--|
| 1 | Side A—DMD, primary components, power mini-planes | 0.5 oz. (before plating) | DMD and escapes. Two data input connectors. Top components including power generation and two data input connectors. Low frequency signals routing. Should have copper fill (GND) plated up to 1 oz. |
| 2 | Ground | 0.5 | Solid ground plane (net GND) reference for signal layers #1, 3 |
| 3 | Signal (high frequency) | 0.5 | High speed signal layer. High speed differential data busses from input connector to DMD |
| 4 | Ground | 0.5 | Solid ground plane (net GND) reference for signal layers #3, #5 |
| 5 | Power | 0.5 | Primary split power planes for 1.8 V, 3.3 V, 10 V, -14 V, 18 V |
| 6 | Power | 0.5 | Primary split power planes for 1.8 V, 3.3 V, 10 V, -14 V, 18 V |
| 7 | Ground | 0.5 | Solid ground plane (net GND) reference for signal layer #8 |
| 8 | Signal (high frequency) | 0.5 | High speed signal layer. High speed differential data buses from input connector to DMD |
| 9 | Ground | 0.5 | Solid ground plane (net GND) Reference for signal layers #8, 10 |
| 10 | Side B—Secondary components, power mini-planes | 0.5 oz. (before plating) | Discrete components if necessary. Low frequency signals routing. Should be copper fill plated up to 1 oz. |

9.4 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005"/0.015" (Trace-Width/Spacing) design rule. Use an analysis of impedance and stack-up requirements to determine and calculate actual trace widths.

Maximize the width of all voltage signals as space permits. Follow the width and spacing requirements listed in [表 9-3](#).

表 9-3. Special Trace Widths, Spacing Requirements

| SIGNAL NAME | MINIMUM TRACE WIDTH (MIL) | MINIMUM TRACE SPACING (MIL) | LAYOUT REQUIREMENT |
|---------------------|---------------------------|-----------------------------|---|
| GND | MAXIMIZE | 5 | Maximize trace width to connecting pin as a minimum. |
| P3P3V | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias. |
| P1P8V | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias. |
| V _{OFFSET} | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary. |
| V _{RESET} | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary. |
| V _{BIAS} | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary. |

9.5 Power

TI strongly discourages signal routing on power planes or on planes adjacent to power planes. If signals must be routed on layers adjacent to power planes, they must not cross splits in power planes to prevent EMI and preserve signal integrity.

Connect all internal digital ground (GND) planes in as many places as possible. Connect all internal ground planes with a minimum distance between connections of 0.5". Extra vias may not be required if there are sufficient ground vias due to normal ground connections of devices.

Connect power and ground pins of each component to the power and ground planes with at least one via for each pin. Minimize trace lengths for component power and ground pins. (ideally, less than 0.100").

Ground plane slots are strongly discouraged.

9.6 Trace Length Matching Recommendations

[表 9-4](#) and [表 9-5](#) describe recommended signal trace length matching requirements. Follow these guidelines to avoid routing long traces over large areas of the PCB:

- Match the trace lengths so that longer signals route in a serpentine pattern
- Minimize the number of turns.
- Ensure that the turn angles are no sharper than 45 degrees.

[図 9-1](#) shows an example of the HSSI signal pair routing.

Signals listed in [表 9-4](#) are specified for data rate operation at up to 3.2Gbps. Minimize the layer changes for these signals. Minimize the number of vias. Avoid sharp turns and layer switching while minimizing the lengths. When layer changes are necessary, place GND vias around the signal vias to provide a signal return path. The distance from one pair of differential signals to another must be at least two times the distance within the pair.

表 9-4. HSSI High Speed DMD Data Signals

| SIGNAL NAME | REFERENCE SIGNAL | ROUTING SPECIFICATION | UNIT |
|---|------------------------------------|-----------------------|------|
| DMD_HSSI0_N(0...7), DMD_HSSI0_P(0...7) | DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P | ±0.25 | inch |
| DMD_HSSI1_N(0...7), DMD_HSSI1_P(0...7) | DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P | ±0.25 | inch |
| DMD_HSSI0_CLK_P | DMD_HSSI1_CLK_P | ±0.05 | inch |
| Intra-pair P | Intra-pair N | ±0.01 | inch |

表 9-5. Other Timing Critical Signals

| SIGNAL NAME | CONSTRAINTS | ROUTING LAYERS |
|---|---|----------------|
| LS_CLK_P, LS_CLK_N LS_WDATA_P, LS_WDATA_N LS_RDATA_A | Intra-pair (P to N) Matched to 0.01 inches Signal-to-signal Matched to +/- 0.25 inches | Layers 3, 8 |

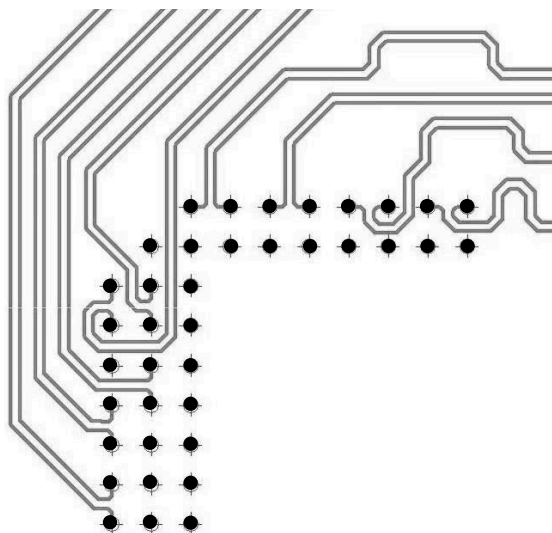


図 9-1. Example HSSI PCB Routing

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.2 Device Support

10.2.1 Device Nomenclature

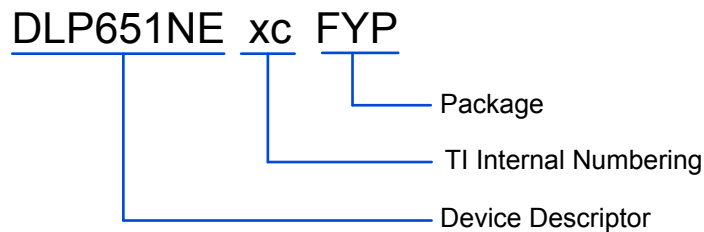


図 10-1. Part Number Description

10.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 10-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

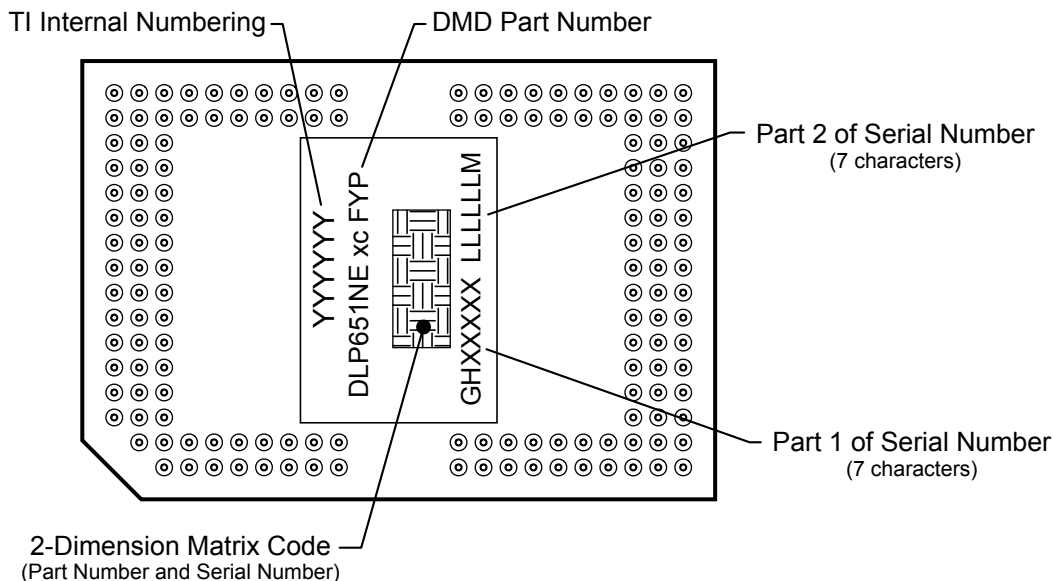


図 10-2. DMD Marking Locations

10.3 Documentation Support

10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- [DLPC7530 Display Controller Data Sheet](#)

- [TPS65145 Data Sheet](#)
- [DLPA100 Power and Motor Driver Data Sheet](#)

10.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.5 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

10.6 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

DLP® is a registered trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.7 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.8 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision A (May 2022) to Revision B (January 2025) | Page |
|--|------|
| ドキュメント全体を通してコントローラを DLPC7530 に更新..... | 1 |
| DLP 製品のサードパーティ検索ツールおよび『テキサス インスツルメンツの DLP ディスプレイ テクノロジーを使用した設計の開始』へのリンクを追加。..... | 1 |
| Added sections SOLID STATE ILLUMINATION and LAMP ILLUMINATION to Recommended Operating Conditions table..... | 7 |
| Deleted entry Environmental ILL ₀ and added Q _{AP-ILL} | 7 |
| Added figure Window Aperture Illumination Overfill Example..... | 7 |
| Updated Micromirror Array Optical Characteristics Table..... | 19 |
| Updated Micromirror Array Temperature Calculation..... | 24 |
| Added the Micromirror Power Density Calculation section..... | 25 |
| Added the topic Window Aperture Illumination Overfill Calculation..... | 27 |
| Updated the equation to calculate the landed duty cycle..... | 28 |
| Changes to Typical Application re: Laser Phosphor configuration and LED configuration..... | 32 |

Changes from Revision * (March 2021) to Revision A (May 2022)**Page**

- このドキュメントは、最新の テキサス・インスツルメンツおよび業界データシート標準に準拠して更新されています。 **1**
- Updated [DMD Power Supply Power-Down Procedure](#) **35**

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish ⁽⁴⁾ | MSL Peak Temp ⁽³⁾ | Op Temp (°C) | Device Marking ⁽⁵⁾ ⁽⁶⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|---------------------------------|------------------------------|--------------|---|
| DLP651NEA0FYP | ACTIVE | CPGA | FYP | 149 | 33 | RoHS & Green | Call TI | Call TI | | see 10-2 |

- (1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| DLP651NEA0FYP | Active | Production | CPGA (FYP) 149 | 33 JEDEC TRAY (5+1) | Yes | NI-AU | N/A for Pkg Type | 0 to 70 | |
| DLP651NEA0FYP.A | Active | Production | CPGA (FYP) 149 | 33 JEDEC TRAY (5+1) | Yes | NI-AU | N/A for Pkg Type | 0 to 70 | |
| DLP651NEA0FYP.B | Active | Production | CPGA (FYP) 149 | 33 JEDEC TRAY (5+1) | - | Call TI | Call TI | 0 to 70 | |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

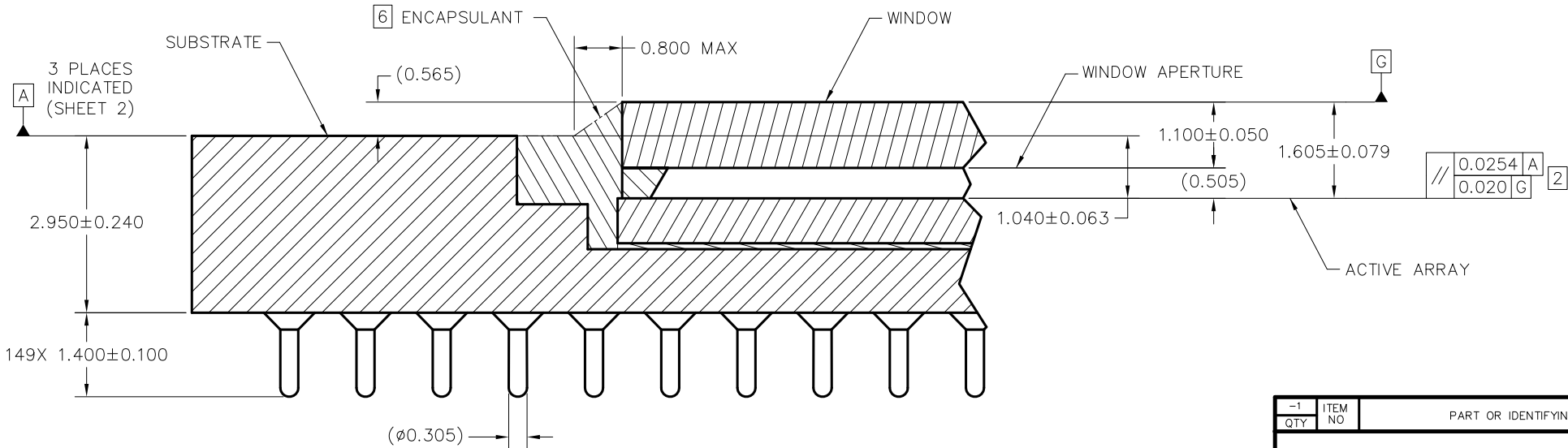
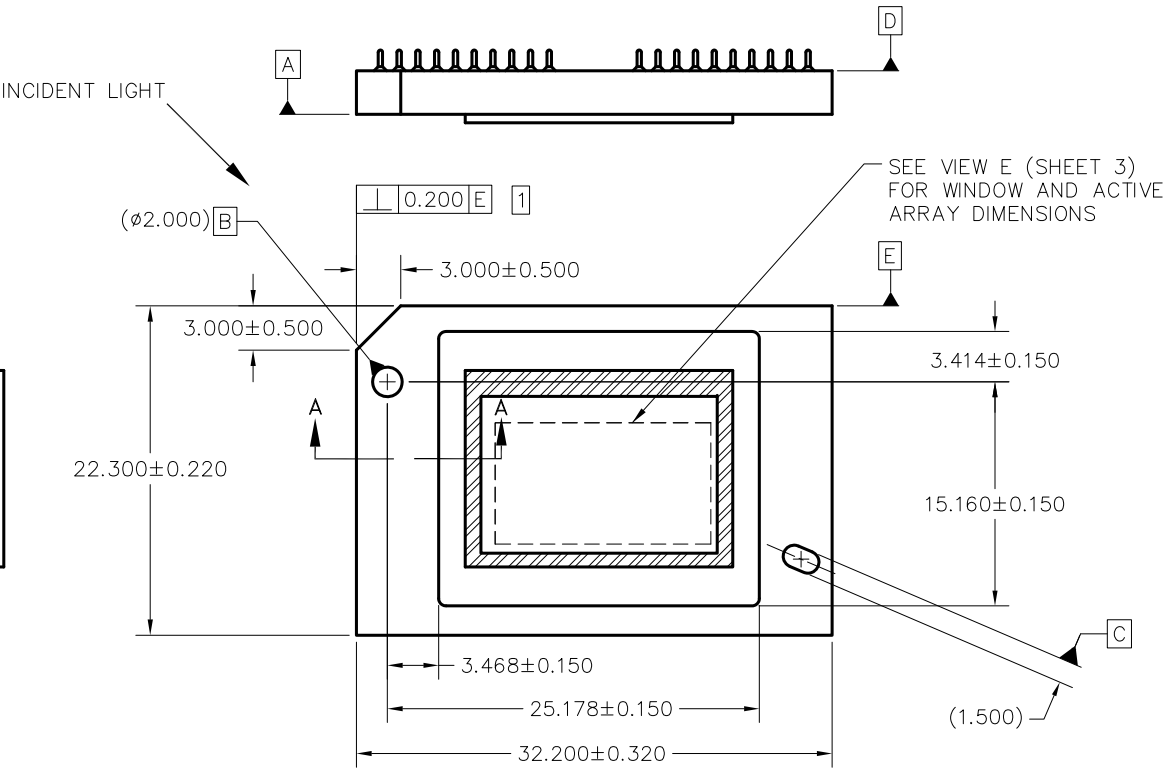
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|-----------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| DLP651NEA0FYP | FYP | CPGA | 149 | 33 | 3 x 11 | 150 | 315 | 135.9 | 12190 | 27.5 | 20 | 27.45 |
| DLP651NEA0FYP.A | FYP | CPGA | 149 | 33 | 3 x 11 | 150 | 315 | 135.9 | 12190 | 27.5 | 20 | 27.45 |


© COPYRIGHT 2019 TEXAS INSTRUMENTS UN-
PUBLISHED, ALL RIGHTS RESERVED.

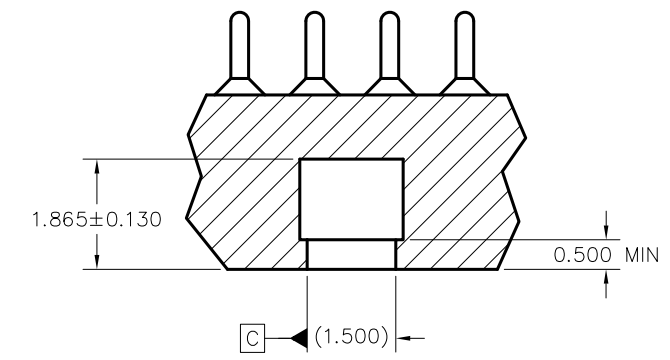
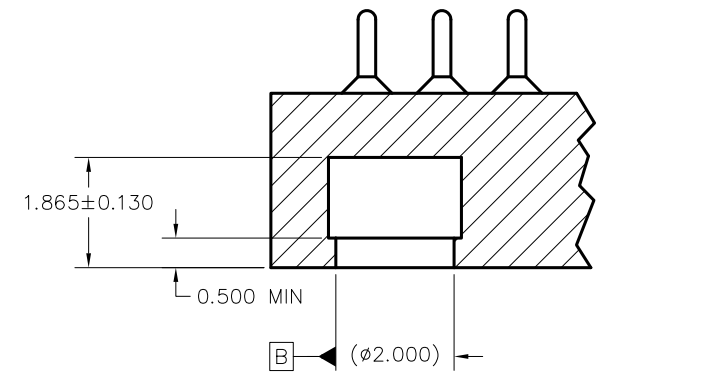
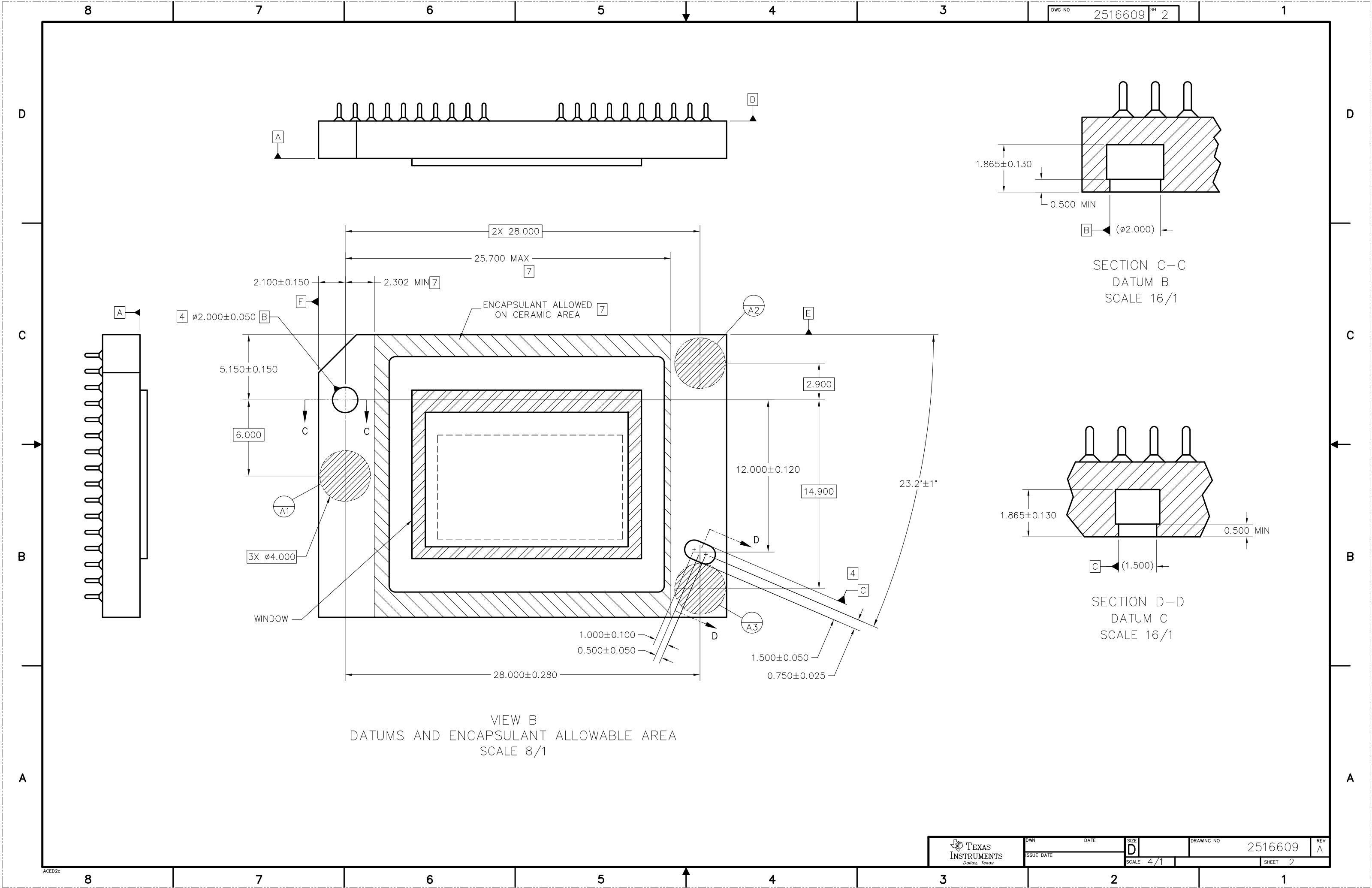
| DWG NO 2516609 | | SH 1 | 1 | |
|----------------|------------------------------|----------|--------------|--|
| REVISIONS | | | | |
| REV | DESCRIPTION | DATE | APPROVED | |
| A | ECO 2180591, INITIAL RELEASE | 04/04/19 | F. ARMSTRONG | |

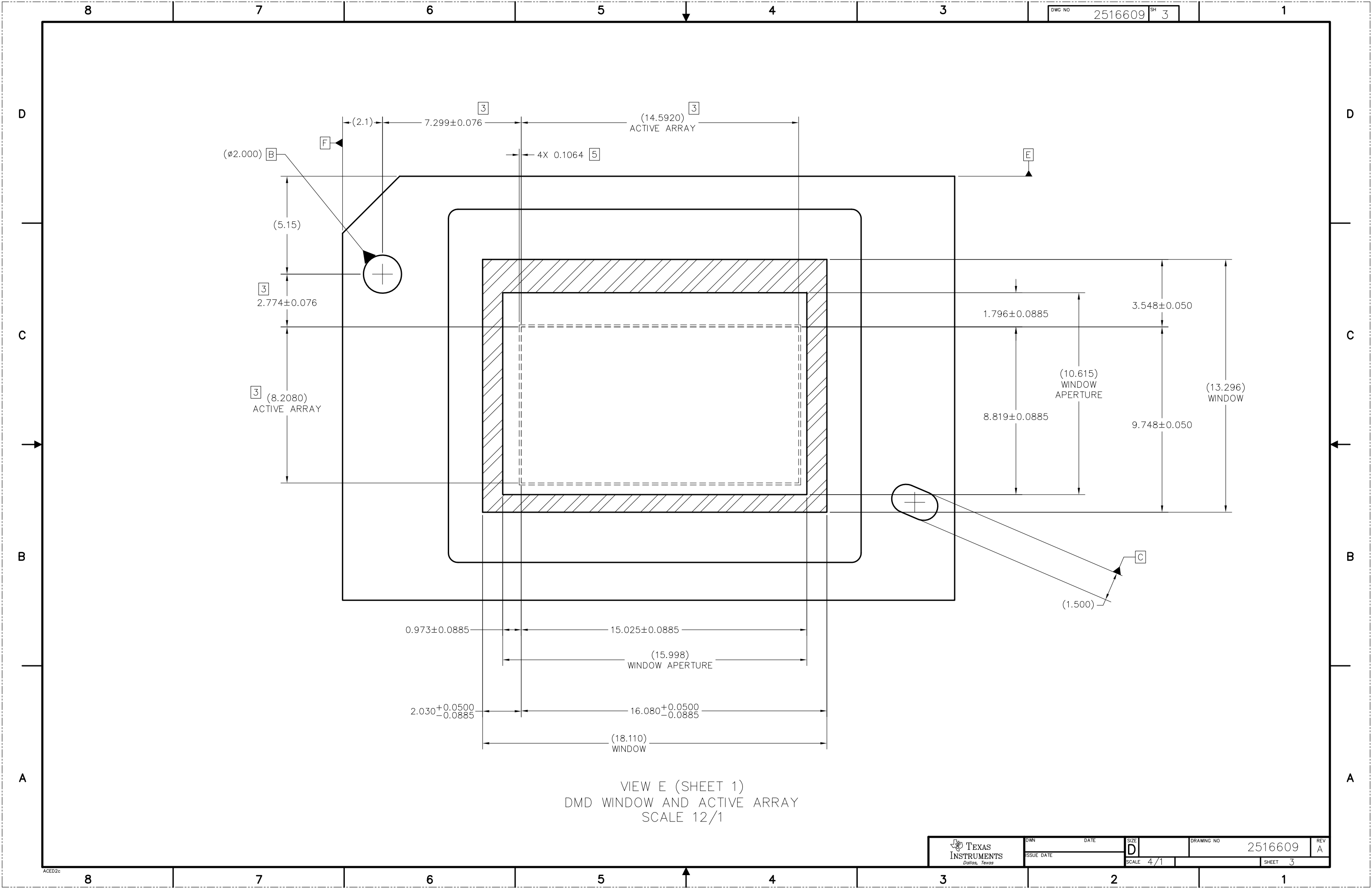
NOTES: UNLESS OTHERWISE SPECIFIED:

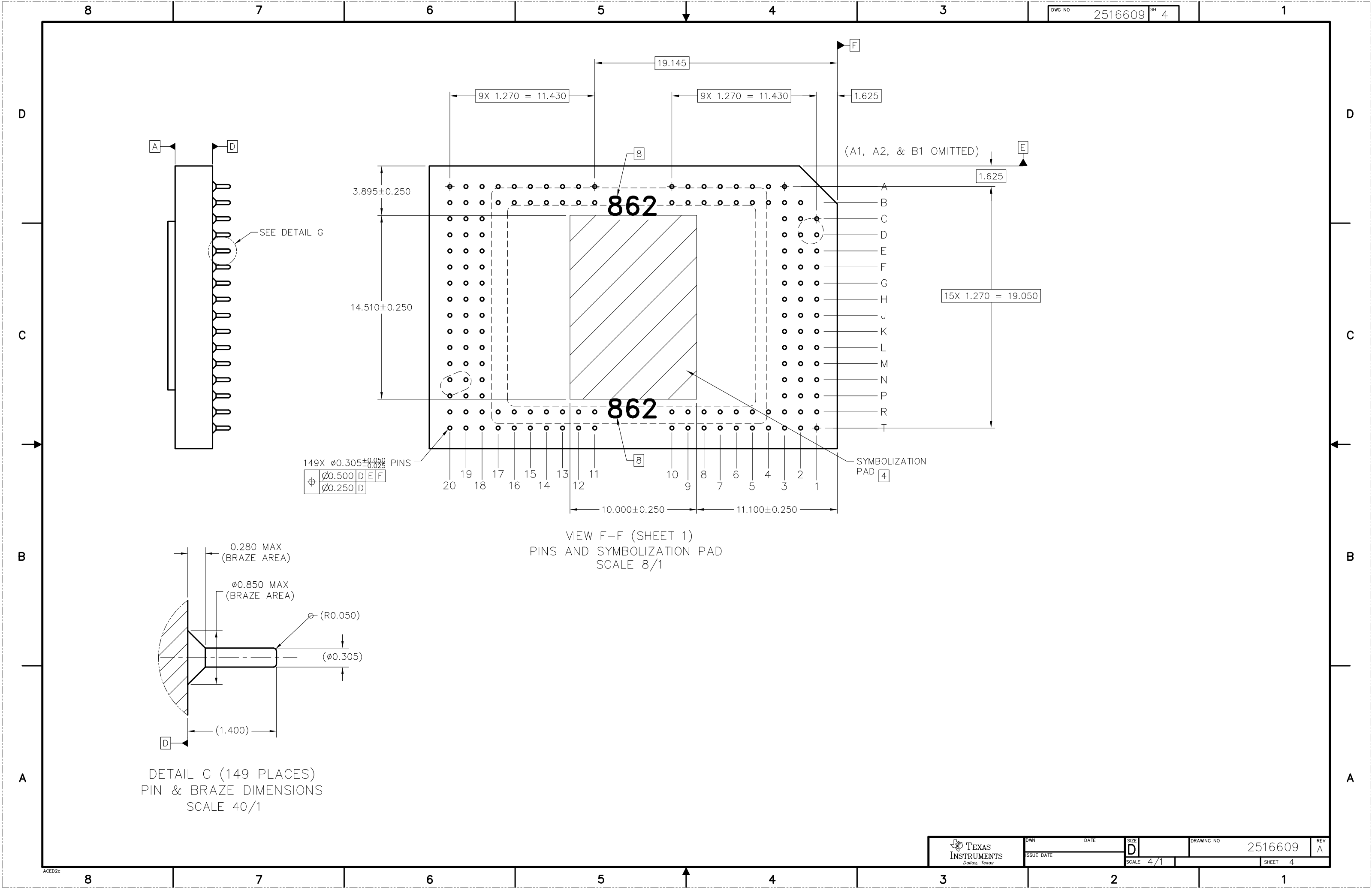
- 1
- SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
- 2
- DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
- 3
- ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
- 4
- SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
- 5
- BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
- 6
- MAXIMUM ENCAPSULANT PROFILE SHOWN
- 7
- ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
- 8
- SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.



| -1 QTY | ITEM NO | PART OR IDENTIFYING NUMBER | NOMENCLATURE OR DESCRIPTION | | | | NOTES |
|-------------|------------|---|-----------------------------|------------------|---|---------|----------|
| PARTS LIST | | | | | | | |
| | | UNLESS OTHERWISE SPECIFIED • DIMENSIONS ARE IN MILLIMETERS • TOLERANCES: ANGLES ± 1° 2 PLACE DECIMALS ±0.25 3 PLACE DECIMALS ±0.50 | DWN F. ARMSTRONG | DATE 04/04/19 |  TEXAS INSTRUMENTS <i>Dallas, Texas</i> | | |
| | | • REMOVE ALL BURRS AND SHARP EDGES • INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994 • DIMENSIONAL LIMITS APPLY BEFORE PROCESSES • PARENTHETICAL INFO FOR REF ONLY | ENGR F. ARMSTRONG | 04/04/19 | | | |
| | | | QA S. HUDGENS | 04/12/2019 | | | |
| | | | CQE M. DORAK | 04/12/2019 | | | |
| | 0314DA | | | | ICD, MECHANICAL, DMD .65 1080p / UHD HSSI SERIES 450 (FYP PACKAGE) | | |
| | USED ON | | | | | | |
| APPLICATION | | | SIZE D | | DRAWING NO | 2516609 | REV A |
| | | | SCALE 4/1 | | SHEET 1 OF 4 | | |







DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

VIEW F-F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated