DLP650TE 0.65 4-K UHD DMD

1 特長

- 対角 0.65 インチのマイクロミラー・アレイ
  - ディスプレイ解像度:4-K UHD (3840 × 2160)
  - マイクロミラー・ピッチ:7.6µm
  - マイクロミラー傾斜角:±12° (水平面に対して)
  - コーナー照明
- 高速シリアル・インターフェイス (High speed serial interface、HSSI) 入力データ・バス
- 4K UHD で 60Hz、フル HD で 240Hz をサポート
- DLPC7540 ディスプレイ・コントローラ、DLPA100 パワー・マネージメント、モータ・ドライバ IC によってサポートされたレーザー蛍光 / LED / RGB レーザー / ランプ動作

2 アプリケーション

- レーザー TV
- スマート・プロジェクタ
- 法人向けプロジェクタ s

3 概要

DLP650TE デジタル・マイクロミラー・デバイス (DMD) は、デジタル制御型の MEMS (micro-electromechanical system) 空間光変調器 (SLM) で、色鮮やかな 4-K UHD ディスプレイ・システムを実現します。本 DLP® 製品の 0.65 インチ 4-K UHD チップセットは、DMD、DLPC7540 ディスプレイ・コントローラ、DLPA100 パワーおよびモータ・ドライバで構成されています。このコンパクトなチップセットは、小型の 4-K UHD ディスプレイを実現する完全なシステム・ソリューションを提供します。

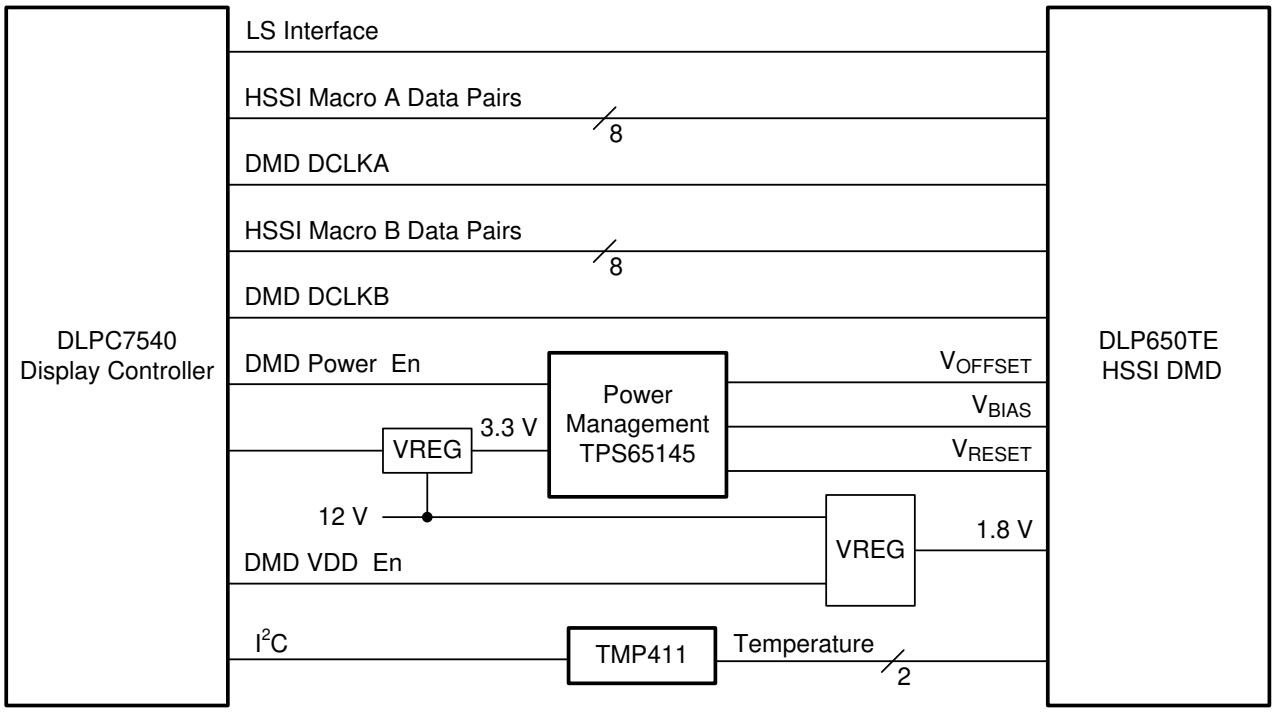
本 DMD のエコシステムは、設計期間の短縮に役立つ定評あるリソースで構成されており、これにはすぐに購入可能な光モジュール、光モジュール・メーカー、デザインハウスなどが含まれます。

DLP DMD を使用して設計を始める方法の詳細については、「TI の DLP ディスプレイ・テクノロジーを使用した設計の開始」のページをご覧ください。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
DLP650TE	FYP(149)	32.2mm × 22.3mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2021) to Revision A (May 2022)	Page
• このドキュメントは、最新のテキサス・インスツルメンツおよび業界データシート標準に準拠して更新されています。	1
• Updated DMD Power Supply Requirements	32

5 Pin Configuration and Functions

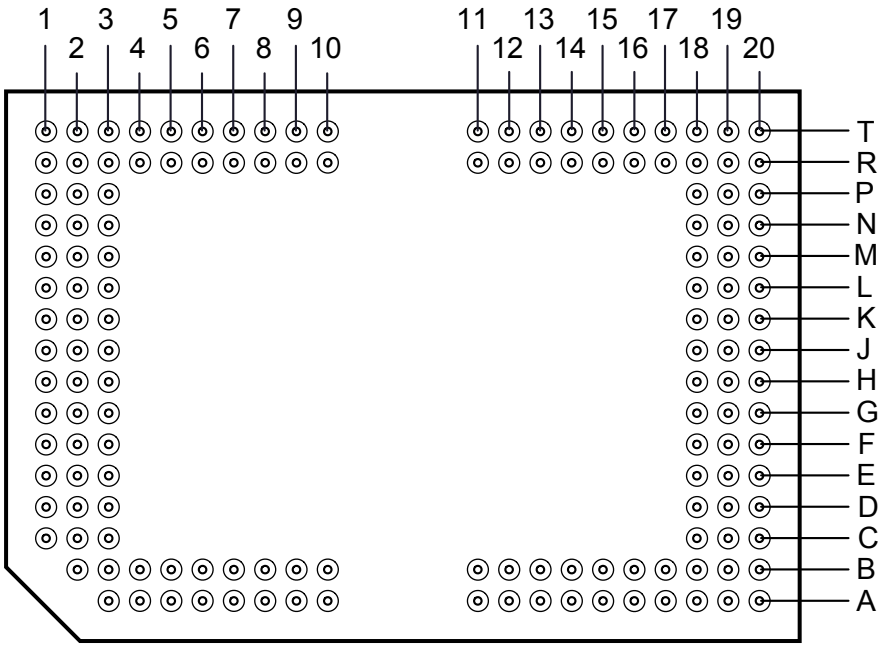


図 5-1. FYP Package 149-Pin CPGA Bottom View

表 5-1. Pin Functions

PIN		TYPE(1)	PIN DESCRIPTION	TRACE LENGTH (mm)
NAME	PAD ID			
D_AP(0)	J1	I	High-speed differential data pair lane A0	18.09088
D_AN(0)	H1	I	High-speed differential data pair lane A0	18.0916
D_AP(1)	G1	I	High-speed differential data pair lane A1	18.11696
D_AN(1)	F1	I	High-speed differential data pair lane A1	18.11641
D_AP(2)	A3	I	High-speed differential data pair lane A2	11.11822
D_AN(2)	A4	I	High-speed differential data pair lane A2	11.11745
D_AP(3)	D2	I	High-speed differential data pair lane A3	12.04461
D_AN(3)	C2	I	High-speed differential data pair lane A3	12.04491
D_AP(4)	F2	I	High-speed differential data pair lane A4	15.1345
D_AN(4)	E2	I	High-speed differential data pair lane A4	15.13457
D_AP(5)	A5	I	High-speed differential data pair lane A5	12.80888
D_AN(5)	A6	I	High-speed differential data pair lane A5	12.80825
D_AP(6)	A7	I	High-speed differential data pair lane A6	6.34763
D_AN(6)	A8	I	High-speed differential data pair lane A6	6.34706
D_AP(7)	A9	I	High-speed differential data pair lane A7	4.45653
D_AN(7)	A10	I	High-speed differential data pair lane A7	4.45875
DCLK_AP	C1	I	High-speed differential clock A	15.08029
DCLK_AN	D1	I	High-speed differential clock A	15.07977
D_BP(0)	A11	I	High-speed differential data pair lane B0	4.06642
D_BN(0)	A12	I	High-speed differential data pair lane B0	4.06697
D_BP(1)	A13	I	High-speed differential data pair lane B1	6.42676

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	PIN DESCRIPTION	TRACE LENGTH (mm)
NAME	PAD ID			
D_BN(1)	A14	I	High-speed differential data pair lane B1	6.42716
D_BP(2)	A15	I	High-speed differential data pair lane B2	11.90485
D_BN(2)	A16	I	High-speed differential data pair lane B2	11.90509
D_BP(3)	A18	I	High-speed differential data pair lane B3	13.80223
D_BN(3)	A19	I	High-speed differential data pair lane B3	13.80269
D_BP(4)	D19	I	High-speed differential data pair lane B4	12.45294
D_BN(4)	C19	I	High-speed differential data pair lane B4	12.45252
D_BP(5)	H20	I	High-speed differential data pair lane B5	15.7909
D_BN(5)	J20	I	High-speed differential data pair lane B5	15.79026
D_BP(6)	D20	I	High-speed differential data pair lane B6	11.02899
D_BN(6)	E20	I	High-speed differential data pair lane B6	11.02947
D_BP(7)	F20	I	High-speed differential data pair lane B7	14.7517
D_BN(7)	G20	I	High-speed differential data pair lane B7	14.75085
DCLK_BP	B17	I	High-speed differential clock B	9.17864
DCLK_BN	B18	I	High-speed differential clock B	9.17821
LS_WDATA_P	T10	I	LVDS Data	11.27905
LS_WDATA_N	R11	I	LVDS Data	6.76474
LS_CLK_P	R9	I	LVDS CLK	13.5461
LS_CLK_N	R10	I	LVDS CLK	12.56934
LS_RDATA_A_BISTA	T13	O	LVCMOS Output	3.12045
BIST_B	T12	O	LVCMOS Output	5.63628
AMUX_OUT	B20	O	Analog Test Mux	9.3849
DMUX_OUT	R14	O	Digital Test Mux	3.85333
DMD_DEN_ARSTZ	T11	I	ARSTZ	5.86593
TEMP_N	R8	I	Temp Diode N	14.63792
TEMP_P	R7	I	Temp Diode P	15.93219
VDD	B7, B13, C18, E3, H3, J2, K3, L2, L19, M1, M2, N3, N19, P2, P18, R3, R5, R12, R17, R19, T2, T4, T6, T8, T18	P	Digital core supply voltage	Plane
VDDA	B4, B9, B11, B16, C20, D3, E18, G2, G19	P	HSSI supply voltage	Plane
VRESET	B3, R1	P	Supply voltage for negative bias of micromirror reset signal	Plane
VBIAS	E1, P1	P	Supply voltage for positive bias of micromirror reset signal	Plane
VOFFSET	A20, B2, T1, T20	P	Supply voltage for HVCMOS logic, stepped up logic level	Plane

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	PIN DESCRIPTION	TRACE LENGTH (mm)
NAME	PAD ID			
VSS	A17, B6, B10, B14, D18, F3, F19, J3, K2, K19, L1, L3, M3, N2, N18, N20, P3, P20, R2, R4, R6, R13, R20, T5, T7, T16, T17, T19	G	Ground	Plane
VSSA	B5, B8, B12, B15, B19, C3, E19, G3, H2, H19, K1, N1, P19, R18, T3, T9	G	Ground	Plane
N/C	R15,T14,T15, R16,H18,J18, G18,J19,F18, K20,K18,M19, L20,M18,L18, M20		No connect	

(1) I=Input, O=Output, P=Power, G=Ground, NC = No connect

6 Specifications

6.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure above or below the Recommended Operating Conditions for extended periods may affect device reliability.

Parameter Name	Description	MIN	MAX	UNIT
Supply Voltage				
V_{DD}	Supply voltage for LVCMOS core logic and LVCMOS low speed interface (LSIF) (1)	–0.5	2.3	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers (1)	–0.3	2.2	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (1) (2)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode (1)	–0.5	17	V
V_{RESET}	Supply voltage for micromirror electrode (1)	–13	0.5	V
$\lvert V_{DDA} - V_{DD} \rvert$	Supply voltage delta (absolute value) (3)		0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value) (4)		11	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value) (5)		30	V
Input Voltage				
	Input voltage for other inputs – LSIF and LVCMOS (1)	–0.5	2.45	V
	Input voltage for other inputs – HSSI (1) (6)	–0.2	V_{DDA}	V
Low speed interface (LSIF)				
f_{CLOCK}	LSIF clock frequency (LS_CLK)		130	MHz
$\lvert V_{ID} \rvert$	LSIF differential input voltage magnitude (6)		810	mV
I_{ID}	LSIF differential input current(7)		10	mA
High speed serial interface (HSSI)				
f_{CLOCK}	HSSI clock frequency (DCLK)		1.65	GHz
$\lvert V_{ID} \rvert$	HSSI differential input voltage magnitude Data Lane (6)		700	mV
$\lvert V_{ID} \rvert$	HSSI differential input voltage magnitude Clock Lane (6)		700	mV
Environmental				
T_{ARRAY}	Temperature, operating(8)	0	90	°C
T_{ARRAY}	Temperature, non-operating(8)	–40	90	°C
T_{DP}	Dew point temperature, operating and non-operating (non-condensing)		81	ºC

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDA} and V_{DD} may result in excessive current draw.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS and HSSI differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) Differential inputs must not exceed the specified limit or damage may result to the internal termination resistors. Specification applies to both the High speed serial interface (HSSI) and the low speed interface (LSI).
(8) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 7-1 and the package thermal resistances using the Micromirror Array Temperature Calculation.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	ºC
T_{DP-AVG}	Average dew point temperature (non-condensing) (1)		28	ºC
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	ºC

6.2 Storage Conditions (continued)

Applicable for the DMD as a component or non-operating in a system.

SYMBOL	PARAMETER	MIN	MAX	UNIT
CT_{ELR}	Cumulative time in the elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

SYMBOL	PARAMETER	DESCRIPTION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted) (1)

Parameter Name		MIN	NOM	MAX	UNIT
Supply Voltages (2) (3)					
V_{DD}	Supply voltage for LVCMOS core logic and low speed interface (LSIF)	1.71	1.8	1.95	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers	1.71	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (4)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for micromirror electrode	15.5	16	16.5	V
V_{RESET}	Supply voltage for micromirror electrode	–12.5	–12	–11.5	V
$\lvert V_{DDA} - V_{DD} \rvert$	Supply voltage delta, absolute value (5)			0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta, absolute value (6)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta, absolute value			29	V
LVCMOS Input					
V_{IH}	High level input voltage (7)	0.7 x V_{DD}			V
V_{IL}	Low level input voltage (7)			0.3 x V_{DD}	V
Low Speed Interface (LSIF)					
f_{CLOCK}	LSIF clock frequency (LS_CLK) (8)	108	120	130	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK)	44%		56%	
$\lvert V_{ID} \rvert$	LSIF differential input voltage magnitude (8)	150	350	440	mV
V_{LVDS}	LSIF voltage. (8)	575		1520	mV
V_{CM}	Common mode voltage. (8)	700	900	1300	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
High Speed Serial Interface (HSSI)					
f_{CLOCK}	HSSI clock frequency (DCLK) (9)	1.2		1.6	GHz
DCD_{IN}	HSSI duty cycle distortion (DCLK)	44%	50%	56%	
$\lvert V_{ID} \rvert$ Data	HSSI differential input voltage magnitude Data Lane (9)	100		600	mV
$\lvert V_{ID} \rvert$ CLK	HSSI differential input voltage magnitude Clock Lane (9)	295		600	mV
VCM_{DC} Data	Input common mode voltage (DC) Data Lane (9)	200	600	800	mV
VCM_{DC} CLK	Input common mode voltage (DC) Clk Lane (9)	200	600	800	mV

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted) (1)

Parameter Name		MIN	NOM	MAX	UNIT
VCM_{ACp-p}	AC peak to peak (ripple) on common mode voltage of Data Lane and Clock Lane (9)			100	mV
Z_{LINE}	Line differential impedance (PWB/trace)		100		Ω
Z_{IN}	Internal differential termination resistance. (R_{Xterm})	80	100	120	Ω
Environmental					
T_{ARRAY}	Array temperature, long-term operational. (10) (11) (12) (13)	10		40 to 70	°C
	Array temperature, short-term operational, 500 hr max. (11) (14)	0		10	°C
T_{DP-AVG}	Average dew point temperature (non-condensing)(15)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(16)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
Q_{AP-ILL}	Window aperture illumination overfill(17) (18)			17	W/cm^2
LAMP ILLUMINATION					
ILL_{UV}	Illumination wavelength < 395 nm (10)		0.68	2	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 395 nm and 800 nm			29.3	W/cm2
ILL_{IR}	Illumination wavelength > 800 nm			10	mW/cm^2
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination wavelength < 410 nm (10)			3	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 410 nm and 800 nm			34.7	W/cm2
ILL_{IR}	Illumination wavelength > 800 nm			10	mW/cm^2

(1) Recommended Operating Conditions are applicable after the DMD is installed in the final product.
(2) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(3) All voltage values are with respect to the V_{SS} ground pins.
(4) V_{OFFSET} supply transients must fall within specified max voltages.
(5) To prevent excess current, the supply voltage delta | $V_{DDA} – V_{DD}$ | must be less than specified limit.
(6) To prevent excess current, the supply voltage delta | $V_{BIAS} – V_{OFFSET}$ | must be less than specified limit.
(7) LVCMOS input pin is DMD_DEN_ARSTZ.
(8) See the low speed interface (LSIF) timing requirements in Timing Requirements.
(9) See the high speed serial interface (HSSI) timing requirements in Timing Requirements.
(10) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination will reduce device lifetime.
(11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 7-1 and the package thermal resistances using the Micromirror Array Temperature Calculation.
(12) Per Figure 6-1, the maximum operational array temperature should be de-rated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to Micromirror Landed Duty Cycle for a definition of micromirror landed duty cycle.
(13) Long-term is defined as the usable life of the device.
(14) Short-term is the total cumulative time over the useful life of the device.
(15) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(16) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(17) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to minimize light flux incident outside the active array. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.
(18) Applies to the region in red in Figure 6-2.

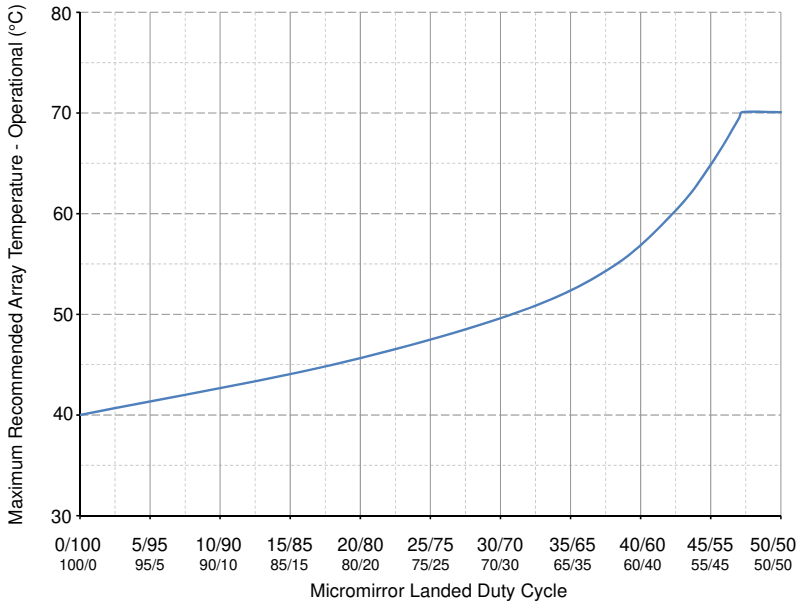


図 6-1. Maximum Recommended Array Temperature - Derating Curve

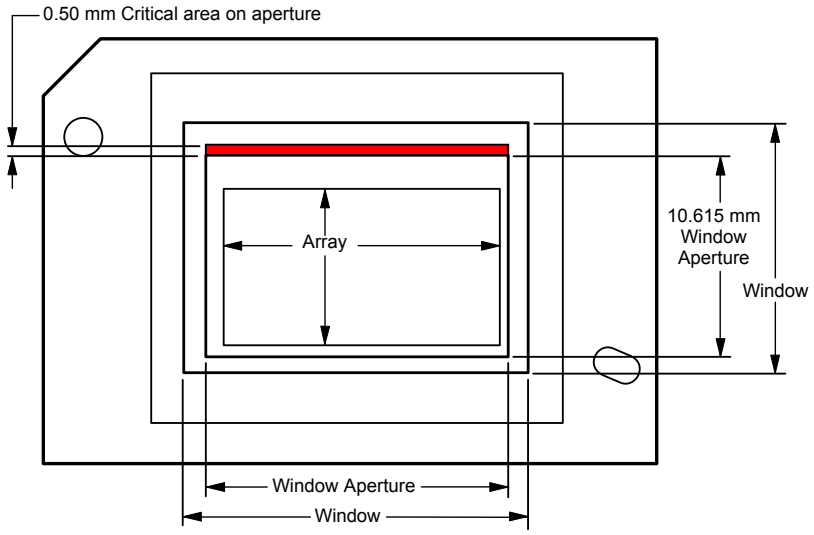


図 6-2. Illumination Overfill Diagram - Critical Area

6.5 Thermal Information

symbol	Thermal Metric	DLP650TE FYP Package 149 Pins	Unit
$R_{ARRAY\_TO\_CERAMIC}$	Thermal resistance, active area to test point 1 (TP1)(1)	0.6	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the Recommend Operating Conditions. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER (1) (2)	TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
Current – Typical						
I_{DD}	Supply current V_{DD} (3)			800	1250	mA
I_{DDA}	Supply current V_{DDA} (3)			900	1200	mA
I_{DDA}	Supply current V_{DDA} (3)	single macro mode		500	600	mA
I_{OFFSET}	Supply current V_{OFFSET} (4) (5)			23	35	mA
I_{BIAS}	Supply current V_{BIAS} (4) (5)			2.4	3.8	mA
I_{RESET}	Supply current V_{RESET} (5)		-10.5	-7.7		mA
Power – Typical						
P_{DD}	Supply power dissipation V_{DD} (3)			1440	2437.5	mW
P_{DDA}	Supply power dissipation V_{DDA} (3)			1620	2340	mW
P_{DDA}	Supply power dissipation V_{DDA} (3)	single macro mode		900	1170	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} (4) (5)			230	367.5	mW
P_{BIAS}	Supply power dissipation VBIAS (4) (5)			38.4	62.7	mW
P_{RESET}	Supply power dissipation V_{RESET} (5)			92.4	131.25	mW
P_{TOTAL}	Supply power dissipation Total			3420.8	5338.95	mW
LVCMOS Input						
I_{IL}	Low level input current (6)	V_{DD} = 1.95 V , V_I = 0 V	–100			nA
I_{IH}	High level input current (6)	V_{DD} = 1.95 V , V_I = 1.95 V			135	µA
LVCMOS Output						
V_{OH}	DC output high voltage (7)	I_{OH} = -2 mA	0.8 x V_{DD}			V
V_{OL}	DC output low voltage (7)	I_{OL} = 2 mA			0.2 x V_{DD}	V
Receiver Eye Characteristics						
A1	Minimum data eye opening (8)		100		600	mV
A1	Minimum clock eye opening (8)		295		600	mV
A2	Maximum signal swing (8) (9)				600	mV
X1	Maximum eye closure (8)				0.275	UI
X2	Maximum eye closure (8)				0.4	UI
$\lvert t_{DRIFT} \rvert$	Drift between Clock and Data between Training Patterns				20	ps
Capacitance						
C_{IN}	Input capacitance LVCMOS	f = 1 MHz			10	pF
C_{IN}	Input capacitance LSIF (low speed interface)	f = 1 MHz			20	pF
C_{IN}	Input capacitance HSSI (high speed serial interface) - Differential - Clock and Data pins	f = 1 MHz			5	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF

(1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta | V_{DDA} – V_{DD} | must be less than specified limit.
(4) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than specified limit.
(5) Supply power dissipation based on 3 global resets in 200 µs.
(6) LVCMOS input specifications are for pin DMD_DEN_ARSTZ.
(7) LVCMOS output specification is for pins LS_RDATA_A and LS_RDATA_B.
(8) Refer to Figure 6-12 (1e-12 BER).
(9) Defined in Recommended Operation Conditions.

6.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. (1)	C_L = 5 pF			11.1	ns
t_{pd}	Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. (1)	C_L = 10 pF			11.3	ns
	Slew rate, LS_RDATA	20% to 80%, C_L <40p	0.35			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B	50 − (C2Q_rise − C2Q_fall) x 130e6 x 100	40%		60%	

(1) See Figure 6-3.

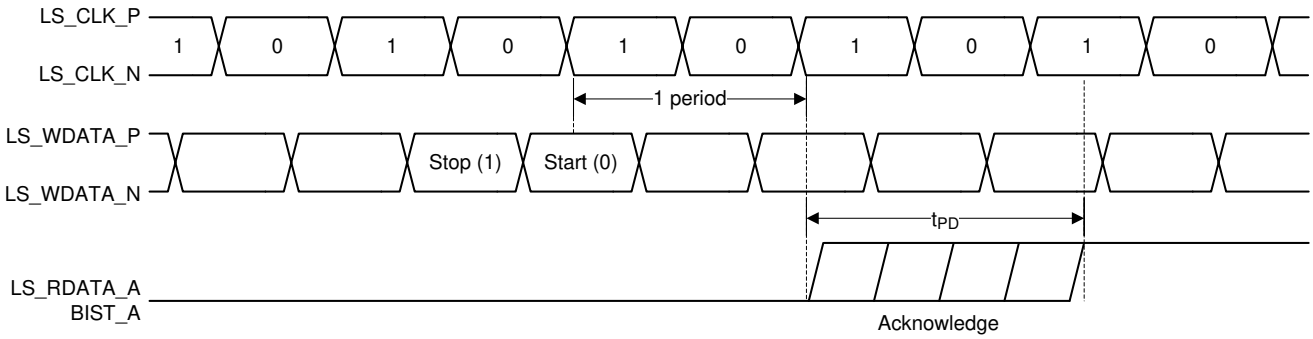


図 6-3. Switching Characteristics

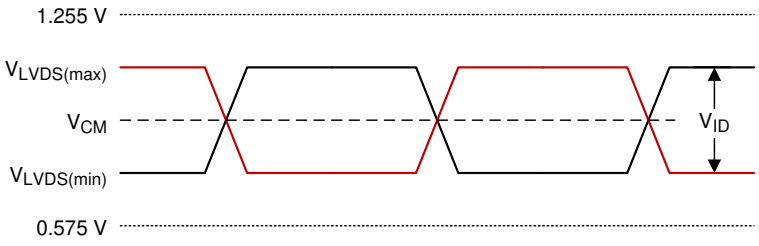
6.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS						
t_r	Rise time (1)	20% to 80% reference points			25	ns
t_f	Fall time (1)	80% to 20% reference points			25	ns
Low Speed Interface (LSIF)						
t_r	Rise time (2)	20% to 80% reference points			450	ps
t_f	Fall time (2)	80% to 20% reference points			450	ps
$t_{W(H)}$	Pulse duration high (3)	LS_CLK. 50% to 50% reference points	3.1			ns
$t_{W(L)}$	Pulse duration low (3)	LS_CLK. 50% to 50% reference points	3.1			ns
t_{su}	Setup time (4)	LS_WDATA valid before rising edge of LS_CLK (differential)	1.5			ns
t_h	Hold time (4)	LS_WDATA valid after rising edge of LS_CLK (differential)	1.5			ns
High Speed Serial Interface (HSSI)						
t_r	Rise time(5), Data	from -A1 to A1 minimum eye height specification	50		115	ps
t_r	Rise time(5), Clock	from -A1 to A1 minimum eye height specification	50		135	ps
t_f	Fall time(5), Data	from A1 to -A1 minimum eye height specification	50		115	ps
t_f	Fall time(5), Clock	from A1 to -A1 minimum eye height specification	50		135	ps
$t_{W(H)}$	Pulse duration high (6)	DCLK. 50% to 50% reference points	0.275			ns
$t_{W(L)}$	Pulse duration low (6)	DCLK. 50% to 50% reference points	0.275			ns
t_c	Cycle time (6)	DCLK	0.625		0.833	ns

(1) See Figure 6-9 and Figure 6-10 LVCMOS Rise, Fall Time SLew Rate Figures. Specification is for DMD_DEN_ARSTZ pin (LVCMOS).
(2) See Figure 6-6 for rise and fall time for LSIF.

(3) See Figure 6-5 for pulse duration high and low time for LSIF.
(4) See Figure 6-5 for setup and hold time for LSIF.
(5) See Figure 6-11 for rise and fall time for HSSI.
(6) See Figure 6-13 for pulse duration high and low and cycle time for HSSI.



A. See 式 1 and 式 2

図 6-4. LSIF Waveform Requirements

$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (1)$$

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (2)$$

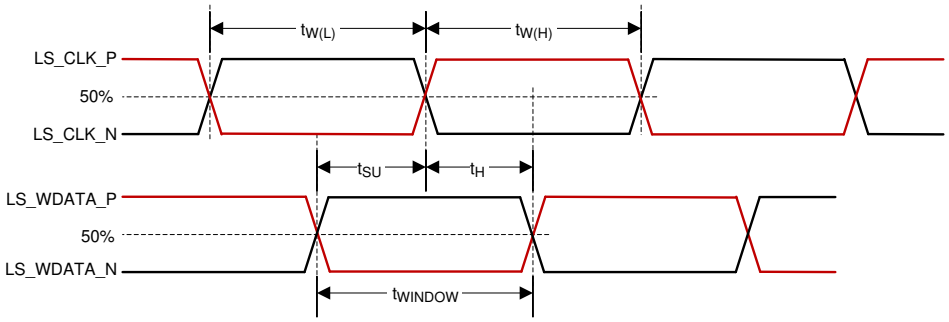


図 6-5. LSIF Timing Requirements

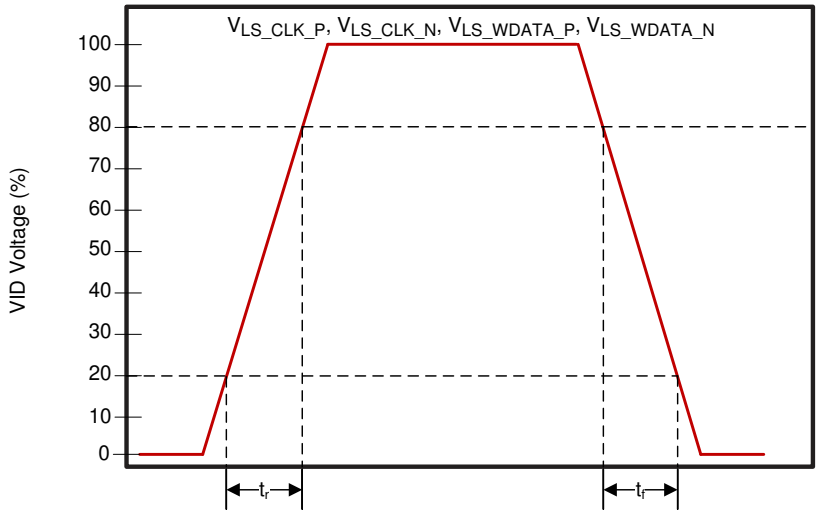


図 6-6. LSIF Rise, Fall Time Slew Rate

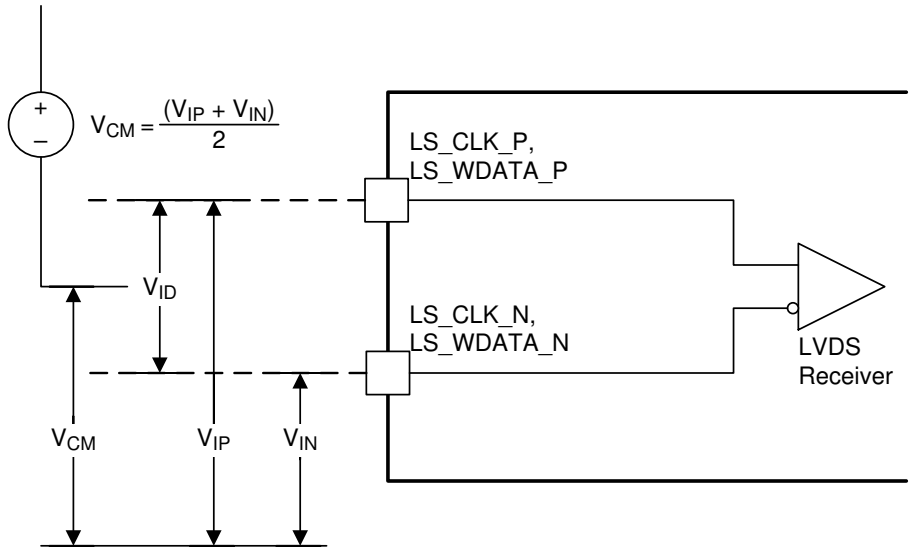


図 6-7. LSIF Voltage Requirements

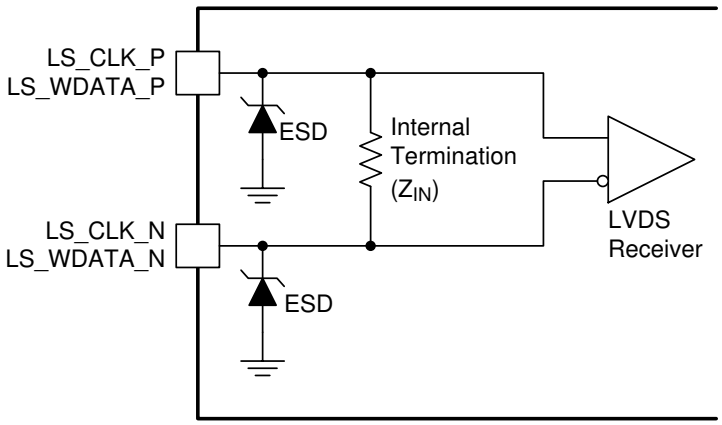


図 6-8. LSIF Equivalent Input

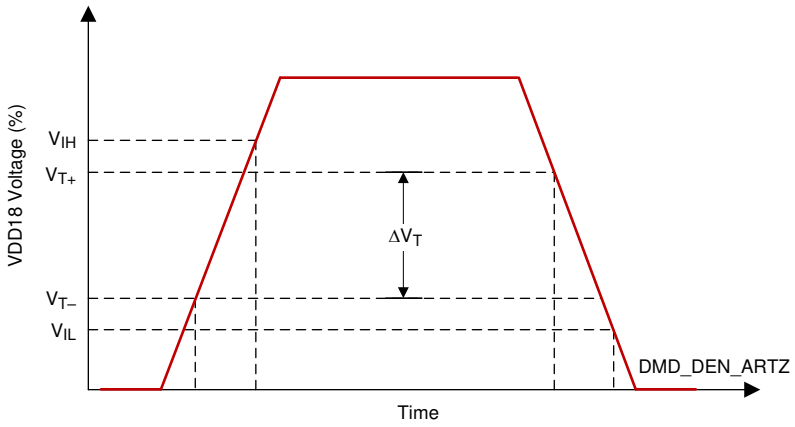


図 6-9. LVCMOS Input Hysteresis

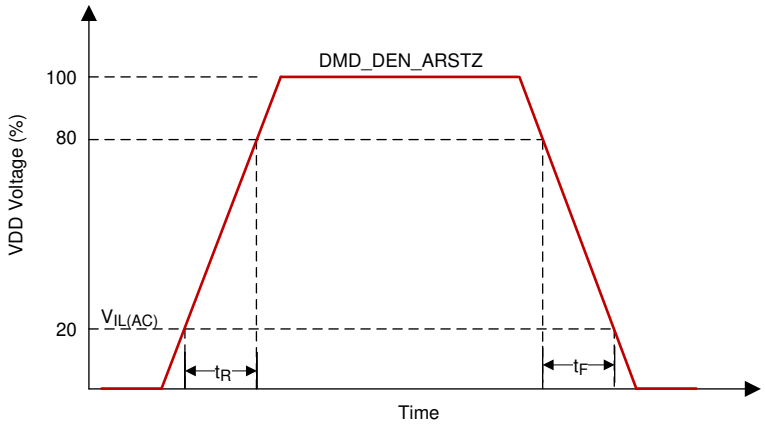
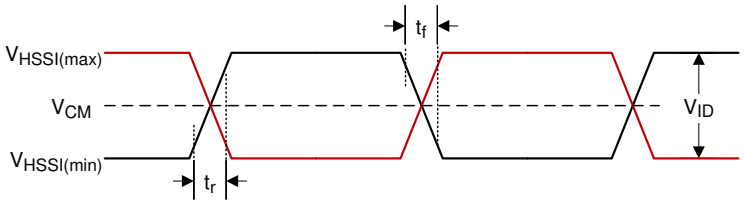


図 6-10. LVCMOS Rise, Fall Time Slew Rate



A. See 式 3 and 式 4

図 6-11. HSSI Waveform Requirements

$$V_{HSSI(max)} = V_{CM(max)} + \left|\frac{1}{2} \times V_{ID(max)}\right| \quad (3)$$

$$V_{HSSI(min)} = V_{CM(min)} - \left|\frac{1}{2} \times V_{ID(max)}\right| \quad (4)$$

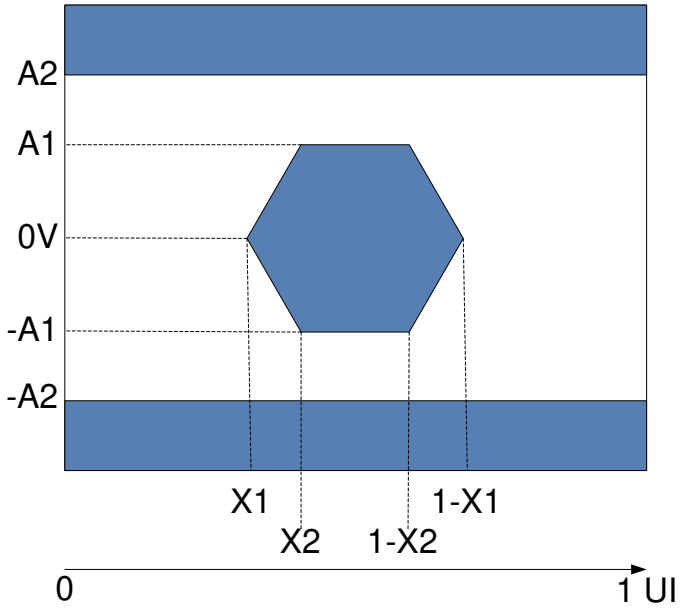


図 6-12. HSSI Eye Characteristics

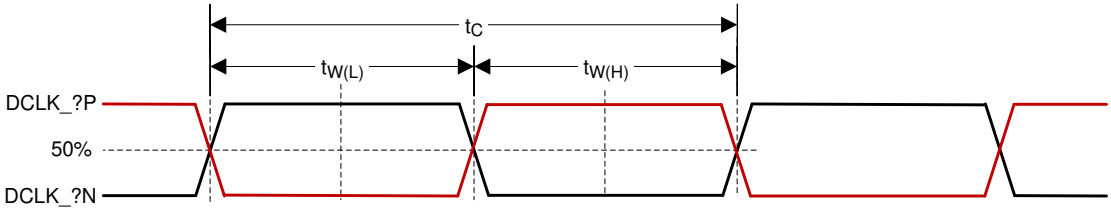


図 6-13. HSSI CLK Characteristics

6.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
When loads are applied on both the electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area(1)			111	N
Maximum load to be applied to the thermal interface area(1)			111	N
When load is applied on the electrical interface area only				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) The load should be applied uniformly in the corresponding areas shown in Figure 6-14.

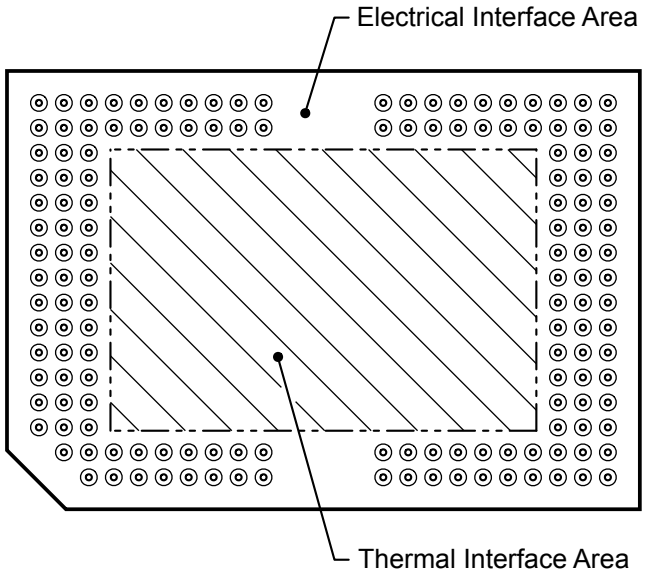


図 6-14. System Mounting Interface Loads

6.10 Micromirror Array Physical Characteristics

SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
M	Number of active columns(1)			1920		micromirrors
N	Number of active rows(1)			1080		micromirrors
P	Micromirror (pixel) pitch(1)			7.6		um
	Micromirror active array width(1)	(micromirror pitch) x (number of active columns)		14.592		mm
	Micromirror active array height (1)	(micromirror pitch) x (number of active rows)		8.208		mm
	Micromirror active border(2)	Pond of micromirror (POM)		14		micromirrors/side

(1) See Figure 6-15.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

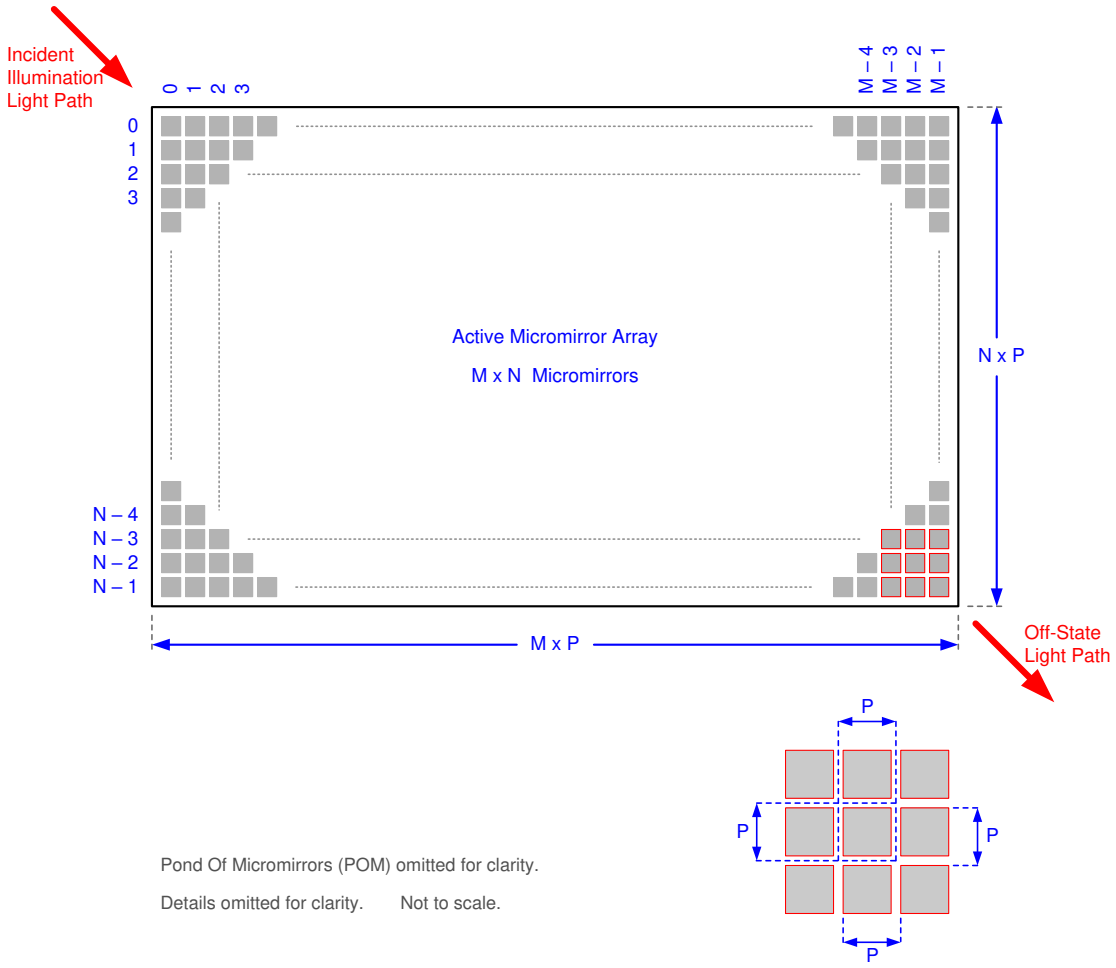


図 6-15. Micromirror Array Physical Characteristics

6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle(1) (2) (3) (4) (5)		landed state	11	12	13	°
Micromirror crossover time(6)		typical performance		2.5		us
Micromirror switching time(7)		typical performance	8			us
Image performance(8)	Bright pixels(s) in active area(9)	Gray 10 Screen(10)			0	micromirrors
	Bright pixes(s) in POM(11)	Gray 10 Screen(10)			1	micromirrors
	Dark pixel(s) in active area(12)	White Screen			4	micromirrors
	Adjacent pixels(13)	Any Screen			0	micromirrors
	Unstable pixel(s) in active area(14)	Any Screen			0	micromirrors

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(3) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.

(5) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction, see Figure 6-16.
(6) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(7) The minimum time between successive transitions of a micromirror.
(8) Conditions of Acceptance: All DMD image performance returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 60 inches
The projection screen shall be 1x gain
The projected image shall be inspected from an 8 foot minimum viewing distance
The image shall be in focus during all image performance tests
(9) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter that the surrounding pixels
(10) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(11) POM definition: Rectangular border of off-state mirror surrounding the active area.
(12) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(13) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(14) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with the parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

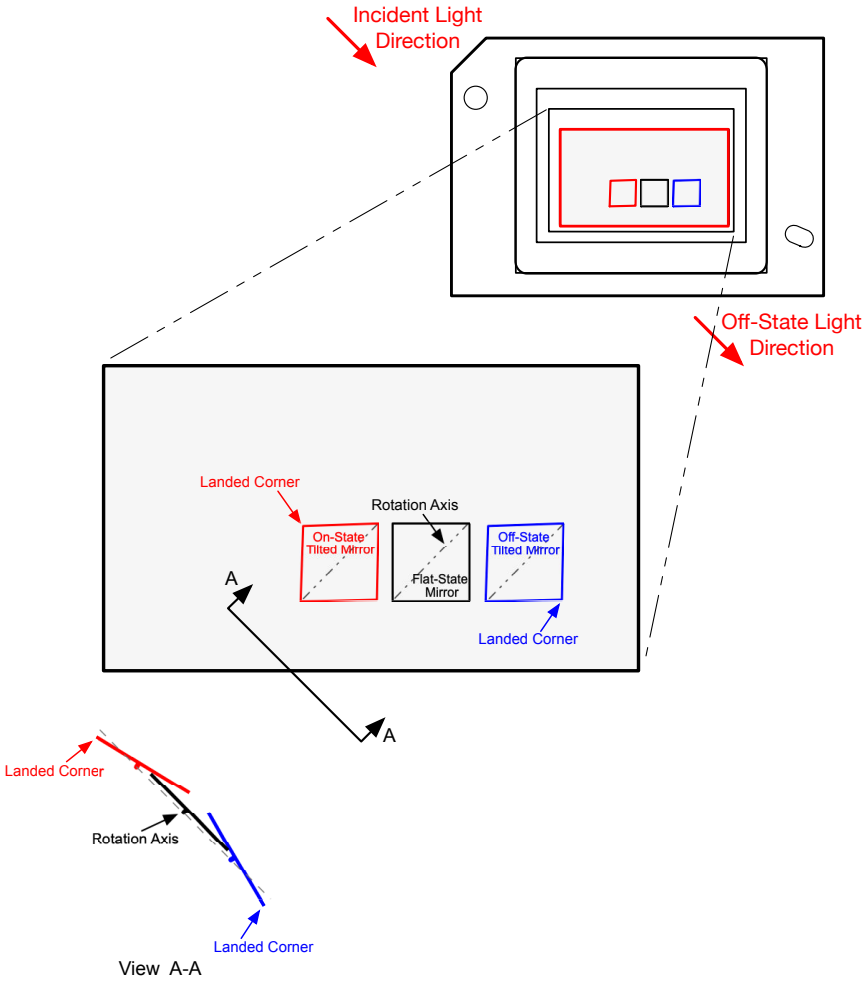


図 6-16. Micromirror Landed Orientation and Tilt

6.12 Window Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Window material designation			Corning EagleXG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window transmittance, average over the wavelength range 420-680 nm	Applies to all angles 0-30 AOI (1) (2)	97.8%			
Window transmittance, average over the wavelength range 420-680 nm	Applies to all angles 30-45 AOI (1) (2)	96.4%			

(1) Single-pass-through both surfaces and glass
(2) AOI - angle of incidence is the angle between an incident ray and the normal to a reflecting or refracting surface

6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP650TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

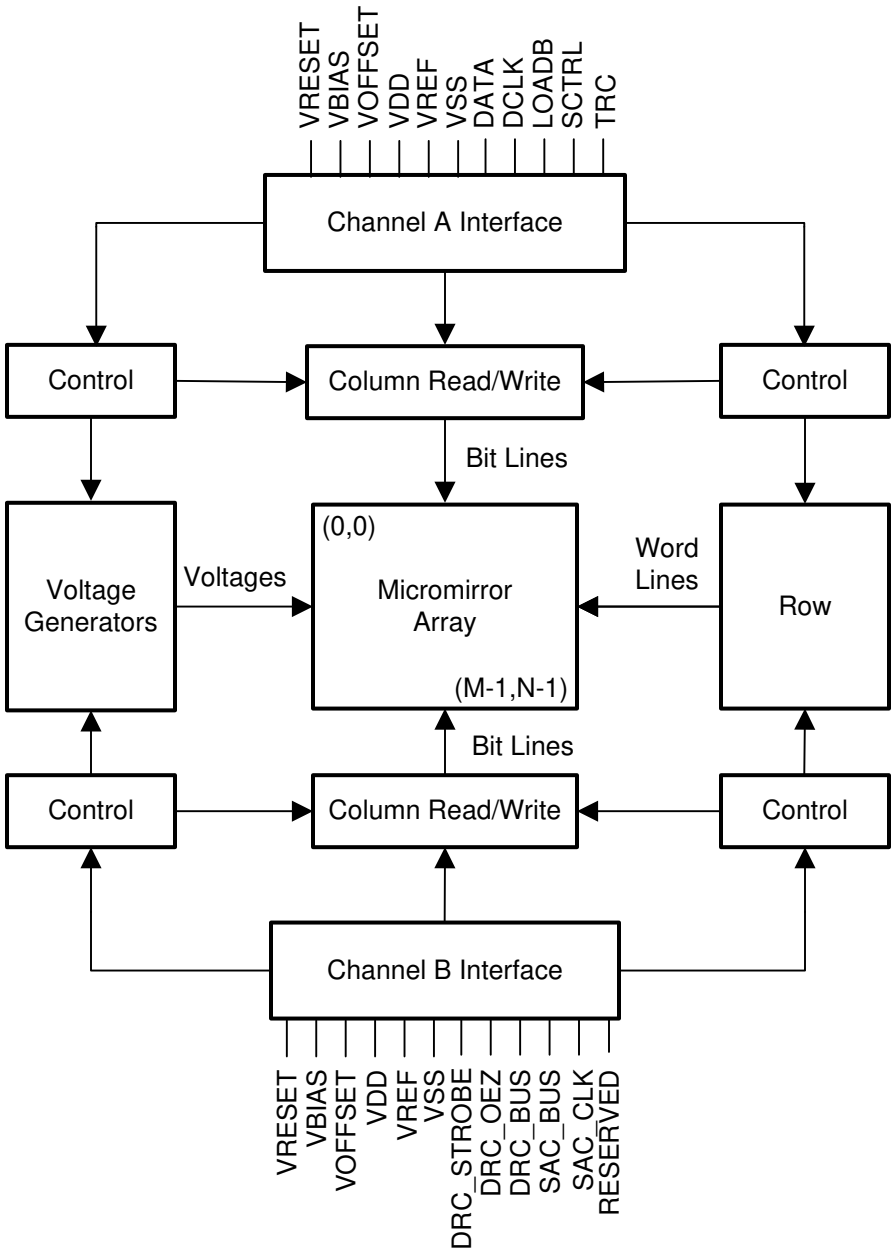
7 Detailed Description

7.1 Overview

The DMD is a 0.65-inch diagonal spatial light modulator that consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to セクション 7.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.65” 4-K UHD chipset is comprised of the DLP650TE DMD, DLPC7540 display controller, the DLPA100 power management and motor driver. To ensure reliable operation, the DLP650TE DMD must always be used with the DLP display controller and the power and motor specified in the chipset.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Interface

The DMD requires 4 DC voltages: 1.8 V source, V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical configuration, 3.3 V is created by the DLPA100 power management and motor driver and is used on the DMD board to create the 1.8 V. The TI voltage regulator TPS65145 takes in the 3.3 V and outputs V_{OFFSET}, V_{RESET}, V_{BIAS}.

7.3.2 Timing

The data sheet specifies timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC7540 display controller. See the *DLPC7540 Display Controller Data Sheet* or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and active area could occur.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

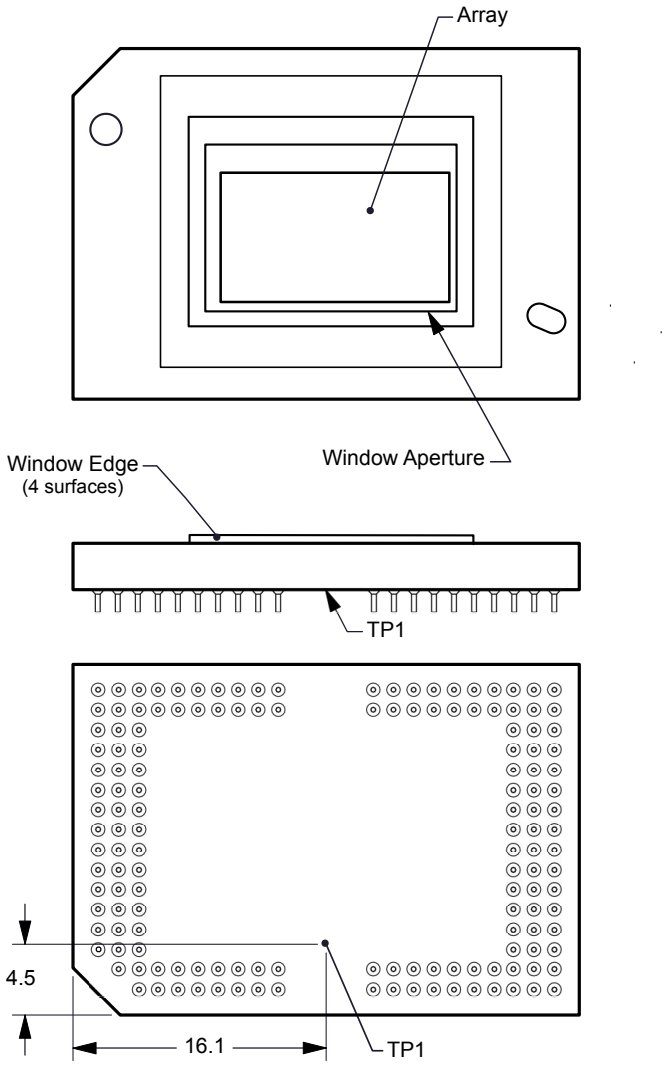


図 7-1. DMD Thermal Test Point

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in 図 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (5)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (6)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in セクション 6.5 from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)

- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.42

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 3.0 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multi-chip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 25 \text{ W (measured)} \quad (7)$$

$$T_{CERAMIC} = 55.0°C \text{ (measured)} \quad (8)$$

$$Q_{ELECTRICAL} = 3.0 \text{ W} \quad (9)$$

$$Q_{ARRAY} = 3.0W + (0.42 \times 25 \text{ W}) = 13.5 \text{ W} \quad (10)$$

$$T_{ARRAY} = 55.0°C + (13.5W \times 0.6°C/W) = 63.1°C \quad (11)$$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the de-rating curve shown in 図 6-1. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).

- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use this information to calculate the landed duty cycle of a given pixel during a given time period:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities are shown in 表 7-2 and 表 7-3.

表 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
30%	50%	20%

表 7-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	30/70
0%	100%	0%	50/50
0%	0%	100%	20/80
0%	12%	0%	6/94
0%	0%	35%	7/93
60%	0%	0%	18/82
0%	100%	100%	70/30
100%	0%	100%	50/50
100%	100%	0%	80/20
0%	12%	35%	13/87
60%	0%	35%	25/75
60%	12%	0%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC7540 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC7540 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 7-2.

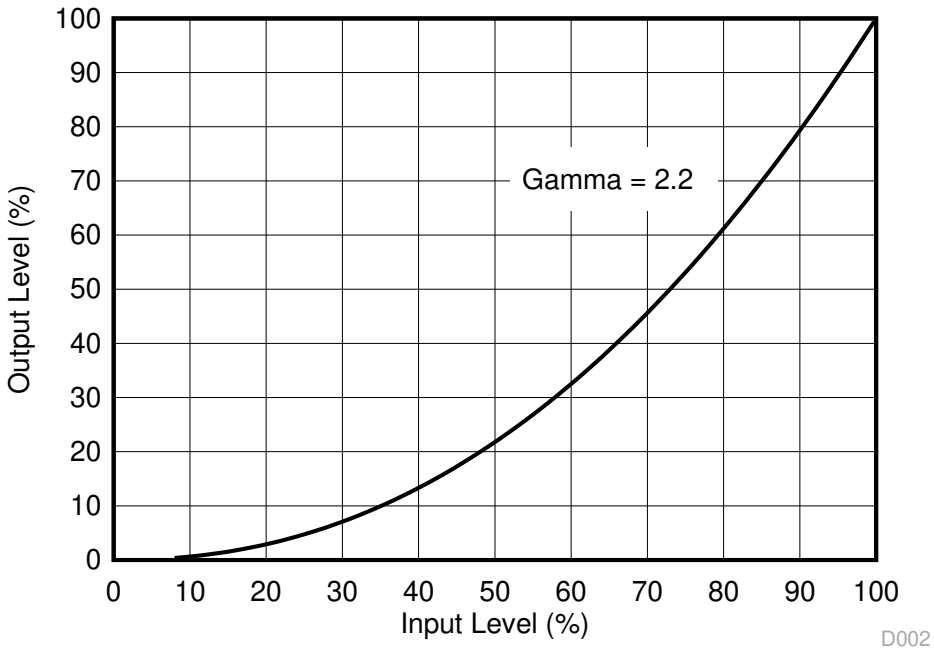


図 7-2. Example of Gamma = 2.2

From 図 7-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing which occurs before the DLPC7540 controllers.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

DMDs are spatial light modulators, which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC7540 controller. Typical applications using the DLP650TE DMD include Laser TVs, smart projectors, and enterprise projectors.

DMD power-up and power-down sequencing is strictly controlled by the DLPC7540 through the TPS65145 PMIC. Refer to セクション 9 for power-up and power-down specifications. To ensure reliable operation, the DLP650TE DMD must always be used with DLPC7540 controller, a DLPA100 PMIC/motor driver, and a TPS65145 PMIC.

8.2 Typical Application

The DLP650TE DMD combined with DLPC7540 digital controller and a power management device provides full 4-K UHD resolution for bright, colorful display applications. A typical display system using laser phosphor illumination combines the DLP650TE DMD, DLPC7540 display controller, TPS65145 voltage regulator and DLPA100 PMIC and motor driver. 図 8-1 shows a system block diagram for this configuration of the DLP 0.65” 4-K UHD chipset and additional system components needed. See 図 8-2 for a block diagram showing the system components needed along with the lamp configuration of the DLP 0.65” 4-K UHD chipset. The components include DLP650TE DMD, DLPC7540 display controller and DLPA100 PMIC and motor driver and a TPS65145 PMIC.

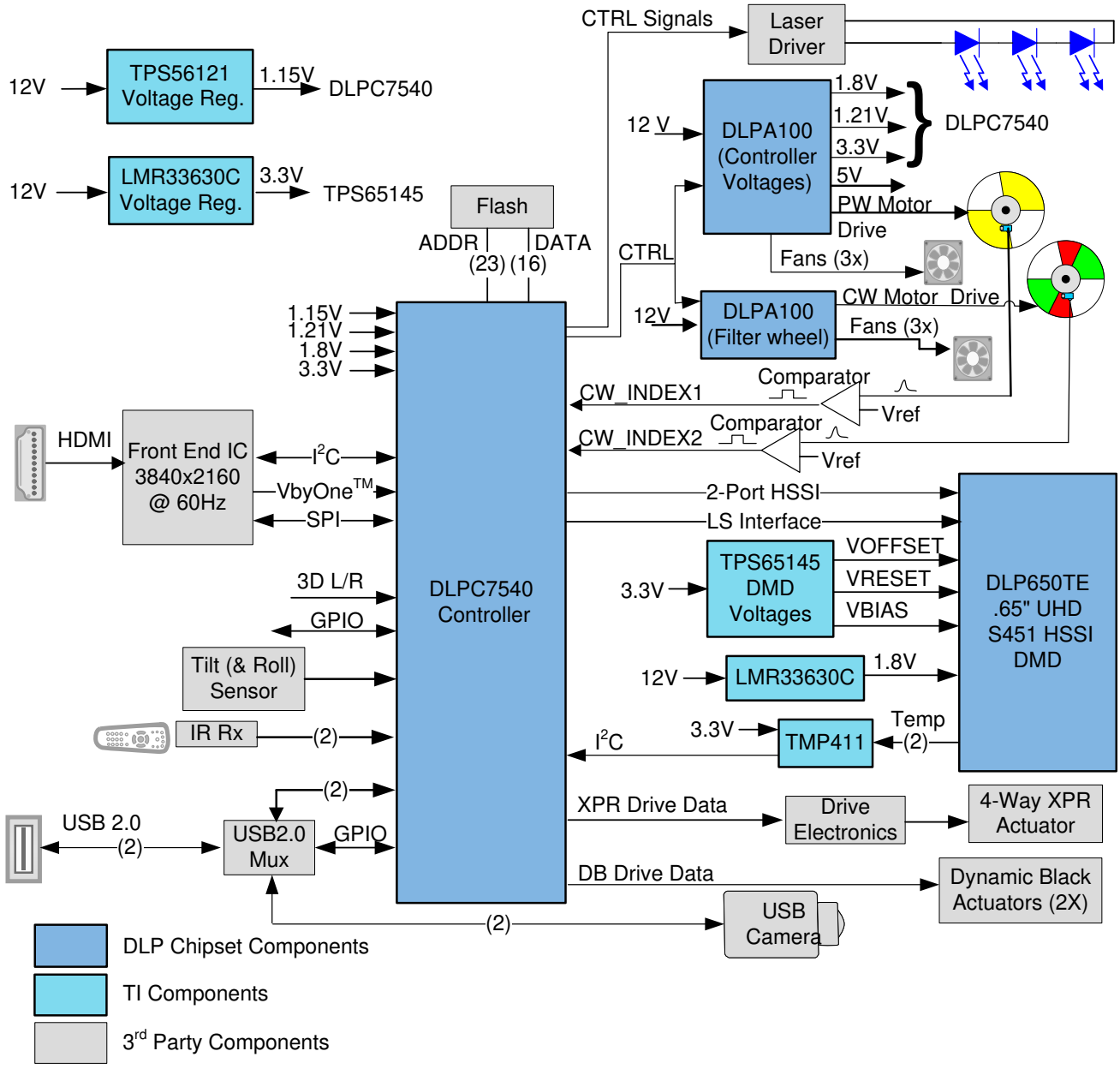


図 8-1. Typical 4K UHD Laser Phosphor Application Diagram

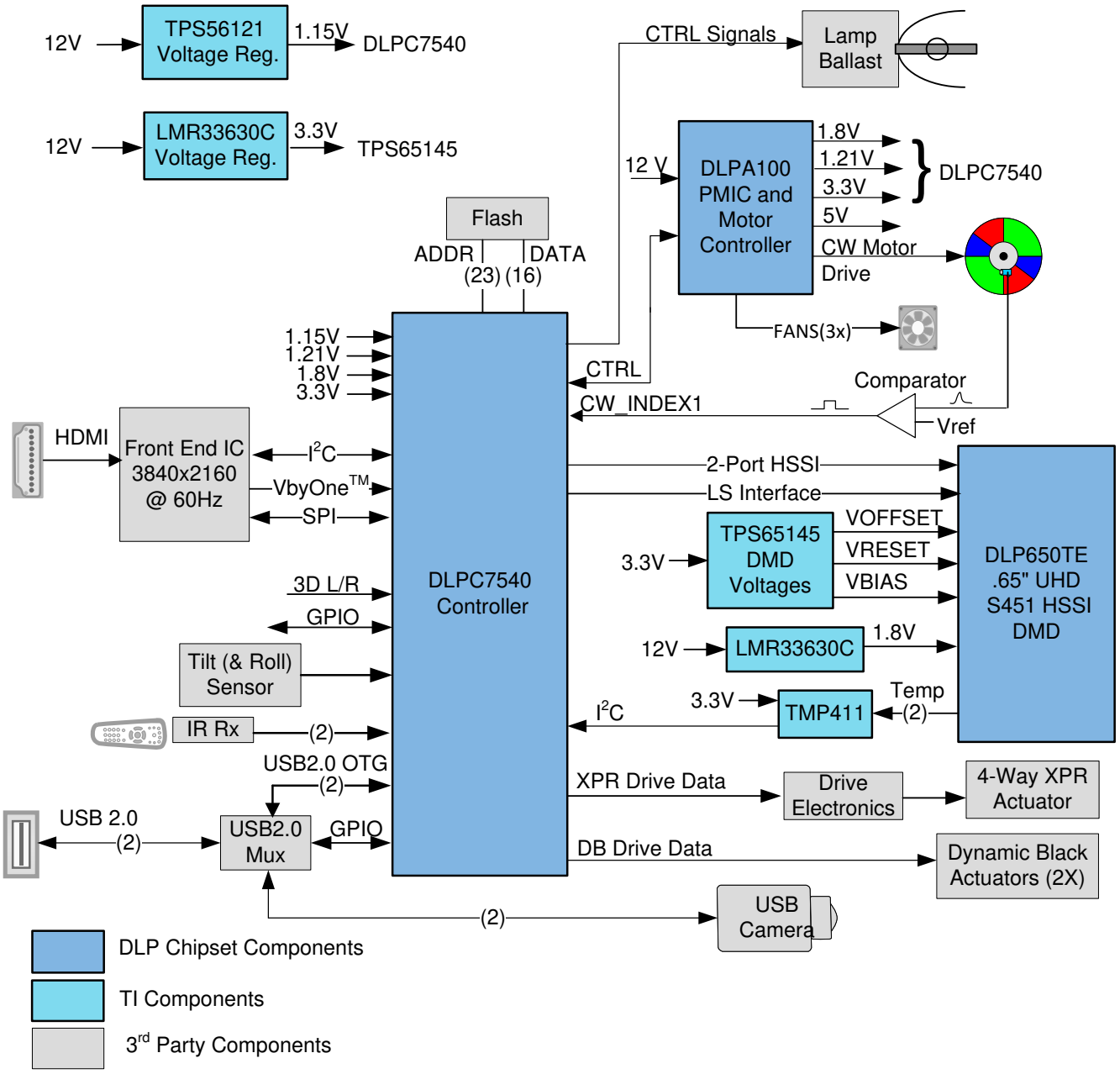


図 8-2. Typical 4K UHD Lamp Phosphor Application Diagram

8.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness has a major effect on the overall system design and size.

The display system uses the DLP650TE DMD as the core imaging device and contains a 0.65-inch array of micromirrors. The DLPC7540 controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver and driving the DMD over a high-speed interface. The DLPA100 PMIC serves as a voltage regulator for the controller, and color filter wheel and phosphor wheel motor control. The TPS65145 provide the DMD reset, offset and bias voltages. The LMR33630C provides 1.8-V power to the DLP650TE DMD.

8.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP650TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with DLPC7540 display controller and the TPS65145 PMIC and DLPA100. Refer to the DMD board reference design and DLPC7540 reference design for layout and design recommendations.

8.2.3 Application Curve

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determines the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. 図 8-3 describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit. .

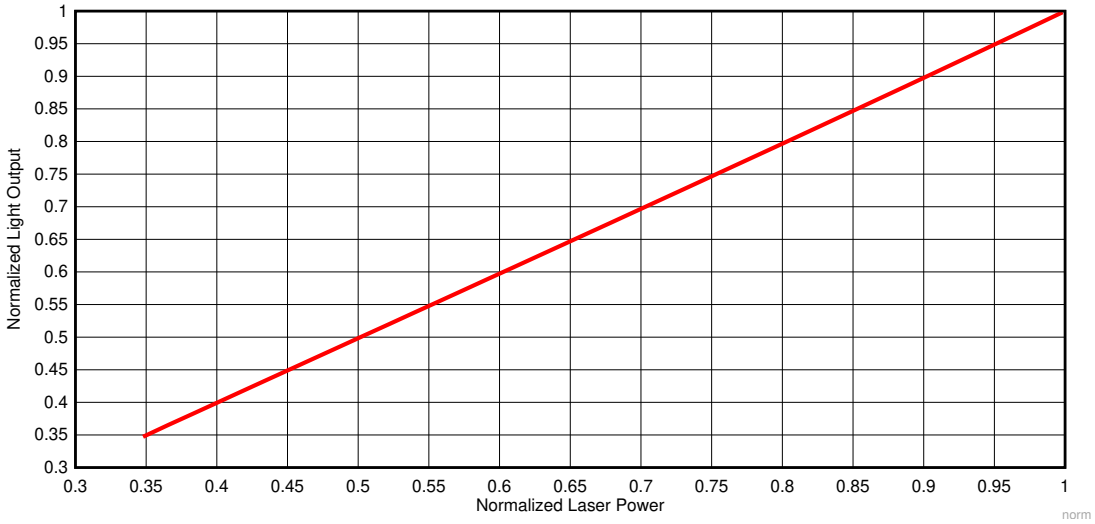
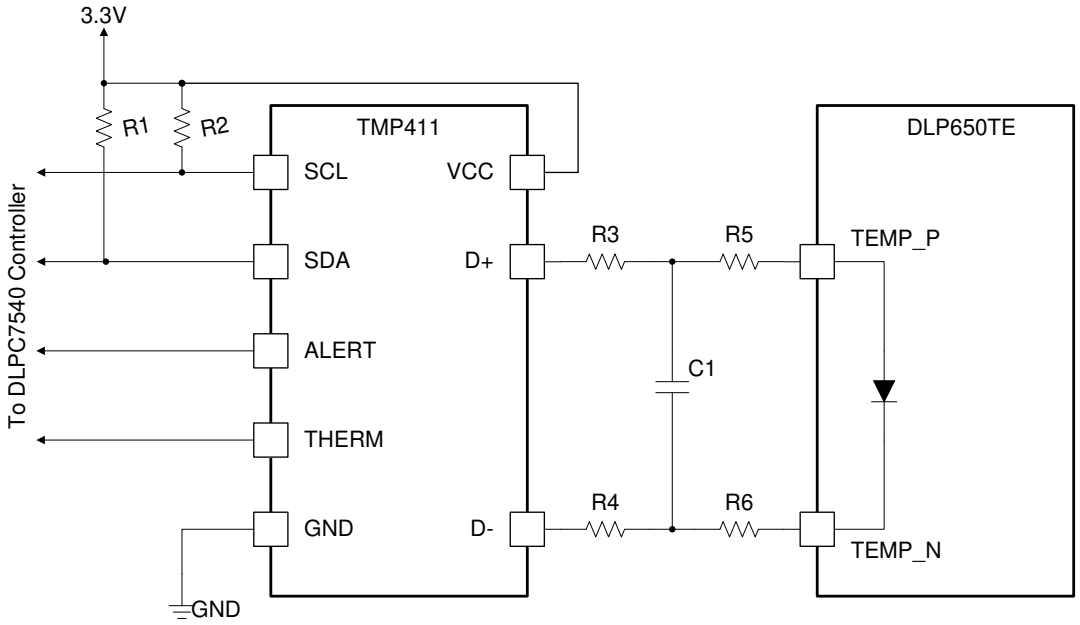


図 8-3. Normalized Light Output vs Normalized Laser Power for Laser Phosphor Illumination

8.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in 図 8-4. The software application contains functions to configure the TMP411 to read the DLP650TE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so on. All communication between the TMP411 and the DLPC7540 controller happens over the I^2C interface. The TMP411 connects to the DMD via pins outlined in 表 5-1.

Leave TEMP_N and TEMP_P pins unconnected (NC) if the temp sensor is not used.



A. Details omitted for clarity.
B. See the TMP411 data sheet for system board layout recommendation.
C. See the TMP411 data sheet for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0 Ω. R6 = 0 Ω. Place 0-Ω resistors close to the DMD package pins.

図 8-4. TMP411 Sample Schematic

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in 図 9-1.

V_{BIAS}, V_{DD}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

9.1 Power Supply Sequence Requirements

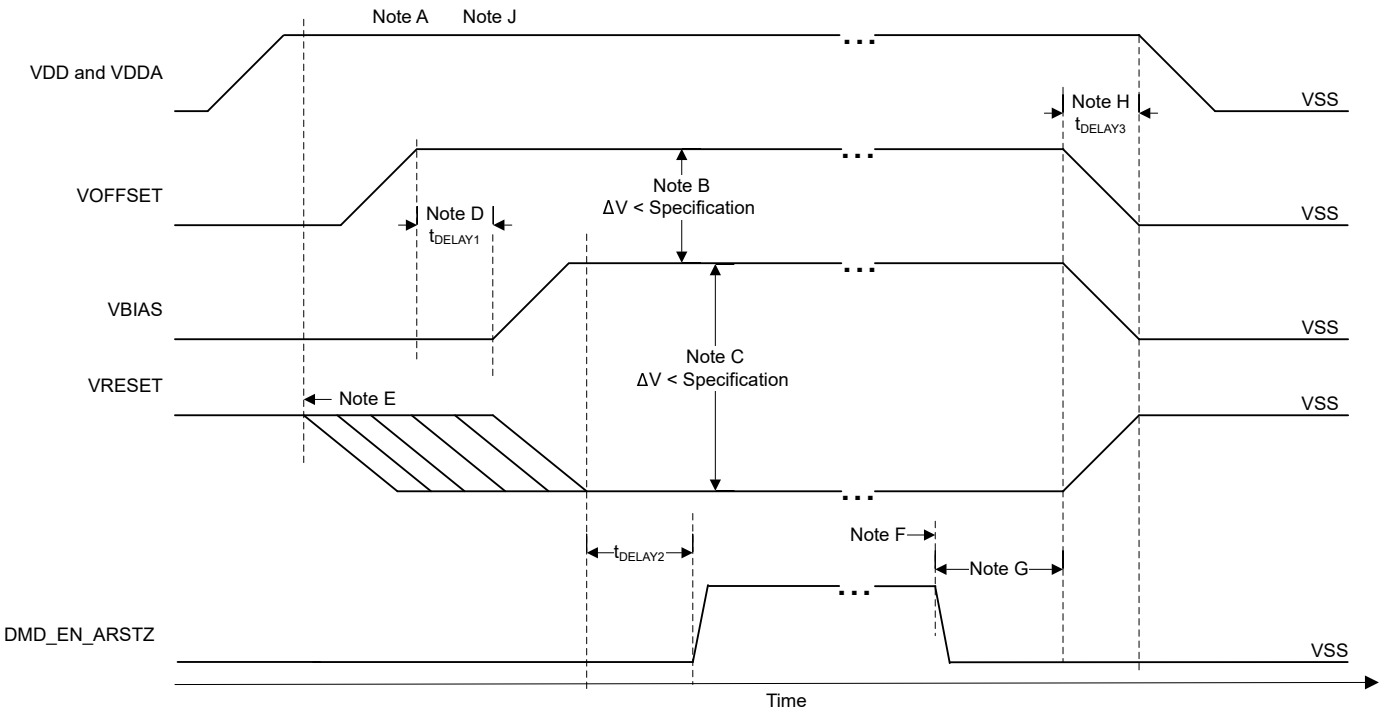
SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY1}	Delay requirement	from V_{OFFSET} power up to V_{BIAS} power up	1	2		ms
t_{DELAY2}	Delay requirement	from V_{BIAS} and V_{RESET} powered on and stable to DMD_EN_ARSTZ going high	20			µs
t_{DELAY3}	Delay requirement	from V_{OFFSET}, V_{BIAS} and V_{RESET} powered down to when VDD and VDDA can power down	50			µs

9.2 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} must always start and settle before V_{OFFSET} plus t_{DELAY1} specified in セクション 9.1, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in セクション 6.4.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in セクション 6.1, in セクション 6.4, and in 図 9-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} has settled at operating voltage listed in セクション 6.4.

9.3 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See セクション 9.1.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in セクション 6.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in セクション 6.1, in セクション 6.4, and in 図 9-1.
- During power-down, LVCMOS input pins must be less than specified in セクション 6.4.



A. See the *Pin Functions* table.
B. To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit in セクション 6.4.
C. To prevent excess current, the supply difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit in セクション 6.4.
D. V_{BIAS} must power up after V_{OFFSET} has powered up, per t_{DELAY1} specification in セクション 9.1.
E. V_{RESET}, V_{OFFSET} and V_{BIAS} ramps must start after VDD and VDDA are powered up and stable.
F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET} and V_{OFFSET}.
G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware DMD_EN_ARSTZ goes low.
H. V_{DD} must remain powered on and stable until after V_{OFFSET}, V_{BIAS}, and V_{RESET} are powered off, per t_{DELAY3} specification in セクション 9.1.
I. To prevent excess current, the supply voltage delta $|V_{DDA} – V_{DD}|$ must be less than specified limit in セクション 6.4.
J. Not to scale. Details omitted for clarity.

図 9-1. DMD Power Supply Requirements

10 Layout

10.1 Layout Guidelines

The DLP650TE DMD is part of a chipset that is controlled by the DLPC7540 display controller in conjunction with theTPS65145 PMIC and the DLPA100 power and motor controller. These guidelines are targeted at designing a PCB board with the DLP650TE DMD. The DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic including double data rate 3.2 Gbps and 250 Mbps differential data buses run to the DMD. TI recommends that full or mini power planes are used for V_{OFFSET}, V_{RESET}, and V_{BIAS}. Solid planes are required for ground (V_{SS}). The target impedance for the PCB is 50 Ω ±10% with exceptions listed in 表 10-1. TI recommends a 10 layer stack-up as described in 表 10-2. TI recommends manufacturing the PCB with a high quality FR-4 material.

10.2 Impedance Requirements

TI recommends a target impedance for the PCB of 50 Ω ±10% for all signals. The exceptions are listed in 表 10-1.

表 10-1. Special Impedance Requirements

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (Ω)
DMD High Speed Data Signals	DMD_HSSI0_N_(0…7), DMD_HSSI0_P_(0…7), DMD_HSSI1_N_(0…7), DMD_HSSI1_P_(0…7), DMD_HSSI0_CLK_N, DMD_HSSI0_CLK_P, DMD_HSSI1_CLK_N, DMD_HSSI1_CLK_P	100-Ω differential (50-Ω single ended)
DMD Low Speed Interface Signals	DMD_LS0_WDATA_N, DMD_LS0_WDATA_P, DMD_LS0_CLK_N, DMD_LS0_CLK_P	100-Ω differential (50-Ω single ended)

10.3 Layers

表 10-2 shows the layer stack-up and copper weight for each layer.

表 10-2. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A—DMD, primary components, power mini-planes	0.5 oz. (before plating)	DMD and escapes. Two data input connectors. Top components including power generation and two data input connectors. Low frequency signals routing. Should have copper fill (GND) plated up to 1 oz.
2	Ground	0.5	Solid ground plane (net GND) reference for signal layers #1, 3
3	Signal (high frequency)	0.5	High speed signal layer. High speed differential data busses from input connector to DMD
4	Ground	0.5	Solid ground plane (net GND) reference for signal layers #3, #5
5	Power	0.5	Primary split power planes for 1.8 V, 3.3 V, 10 V, -14 V, 18 V
6	Power	0.5	Primary split power planes for 1.8 V, 3.3 V, 10 V, -14 V, 18 V
7	Ground	0.5	Solid ground plane (net GND) reference for signal layer #8
8	Signal (high frequency)	0.5	High speed signal layer. High speed differential data buses from input connector to DMD
9	Ground	0.5	Solid ground plane (net GND) Reference for signal layers #8, 10
10	Side B—Secondary components, power mini-planes	0.5 oz. (before plating)	Discrete components if necessary. Low frequency signals routing. Should be copper fill plated up to 1 oz.

10.4 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005”/0.015” (Trace-Width/Spacing) design rule. Use an analysis of impedance and stack-up requirements to determine and calculate actual trace widths.

Maximize the width of all voltage signals as space permits. Follow the width and spacing requirements listed in 表 10-3.

表 10-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH (MIL)	MINIMUM TRACE SPACING (MIL)	LAYOUT REQUIREMENT
GND	MAXIMIZE	5	Maximize trace width to connecting pin as a minimum.
P3P3V	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias.
P1P8V	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias.
V_{OFFSET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{RESET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{BIAS}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.

10.5 Power

TI strongly discourages signal routing on power planes or on planes adjacent to power planes. If signals must be routed on layers adjacent to power planes, they must not cross splits in power planes to prevent EMI and preserve signal integrity.

Connect all internal digital ground (GND) planes in as many places as possible. Connect all internal ground planes with a minimum distance between connections of 0.5”. Extra vias may not be required if there are sufficient ground vias due to normal ground connections of devices.

Connect power and ground pins of each component to the power and ground planes with at least one via for each pin. Minimize trace lengths for component power and ground pins. (ideally, less than 0.100”).

Ground plane slots are strongly discouraged.

10.6 Trace Length Matching Recommendations

表 10-4 and 表 10-5 describe recommended signal trace length matching requirements. Follow these guidelines to avoid routing long traces over large areas of the PCB:

- Match the trace lengths so that longer signals route in a serpentine pattern
- Minimize the number of turns.
- Ensure that the turn angles no sharper than 45 degrees.

図 10-1 shows an example of the HSSI signal pair routing.

Signals listed in 表 10-4 are specified for data rate operation at up to 3.2 Gbps. Minimize the layer changes for these signals. Minimize the number of vias. Avoid sharp turns and layer switching while minimizing the lengths. When layer changes are necessary, place GND vias around the signal vias to provide a signal return path. The distance from one pair of differential signals to another must be at least 2 times the distance within the pair.

表 10-4. HSSI High Speed DMD Data Signals

SIGNAL NAME	REFERENCE SIGNAL	ROUTING SPECIFICATION	UNIT
DMD_HSSI0_N(0...7), DMD_HSSI0_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	±0.25	inch

表 10-4. HSSI High Speed DMD Data Signals (continued)

SIGNAL NAME	REFERENCE SIGNAL	ROUTING SPECIFICATION	UNIT
DMD_HSSI1_N(0...7), DMD_HSSI1_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	±0.25	inch
DMD_HSSI0_CLK_P	DMD_HSSI1_CLK_P	±0.05	inch
Intra-pair P	Intra-pair N	±0.01	inch

表 10-5. Other Timing Critical Signals

SIGNAL NAME	Constraints	Routing Layers
LS_CLK_P, LS_CLK_N LS_WDATA_P, LS_WDATA_N LS_RDATA_A	Intra-pair (P to N) Matched to 0.01 inches Signal-to-signal Matched to +/- 0.25 inches	Layers 3, 8

-

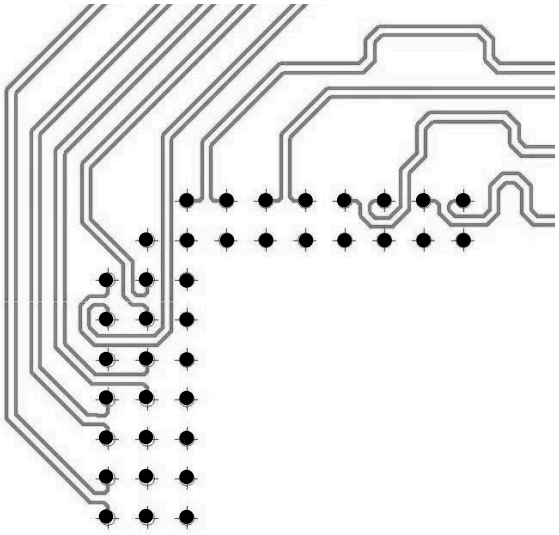


図 10-1. Example HSSI PCB Routing

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Device Support

11.2.1 Device Nomenclature

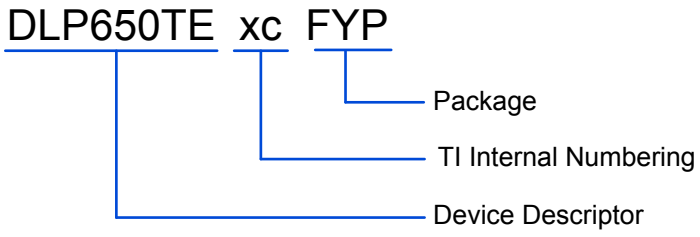

図 11-1. Part Number Description

11.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 11-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

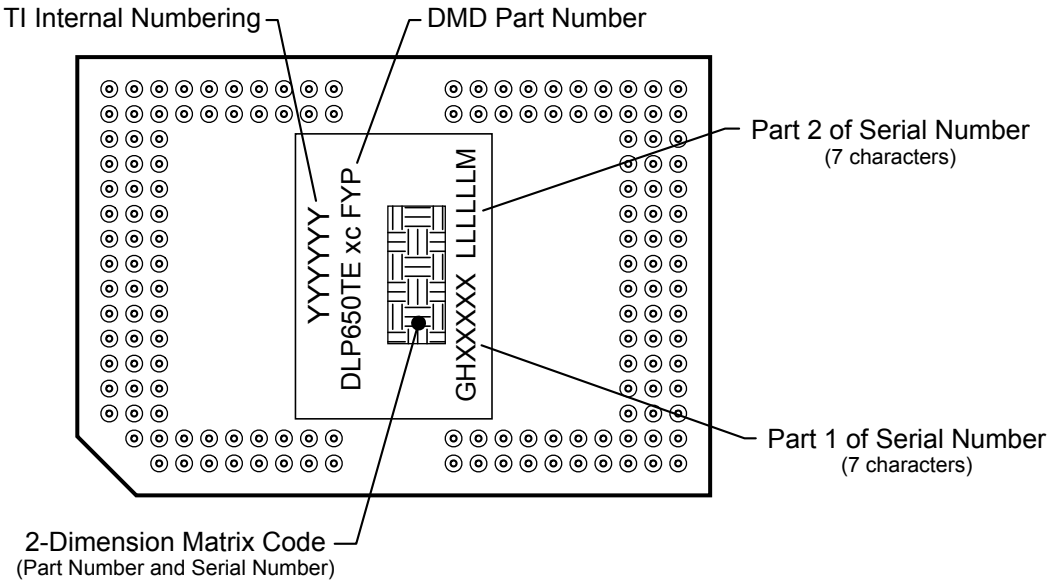

図 11-2. DMD Marking Locations

11.3 Documentation Support

11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- *DLPC7540 Display Controller Data Sheet*
- *TPS65145 Data Sheet*

- *DLPA100 Power and Motor Driver Data Sheet*

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 サポート・リソース

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
DLP650TEA0FYP	ACTIVE	CPGA	FYP	149	33	RoHS & Green	Call TI	Call TI		see 図 11-2

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP650TEA0FYP	Active	Production	CPGA (FYP) | 149	33 | JEDEC TRAY (5+1)	Yes	NI-AU	N/A for Pkg Type	0 to 70	
DLP650TEA0FYP.A	Active	Production	CPGA (FYP) | 149	33 | JEDEC TRAY (5+1)	Yes	NI-AU	N/A for Pkg Type	0 to 70	
DLP650TEA0FYP.B	Active	Production	CPGA (FYP) | 149	33 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

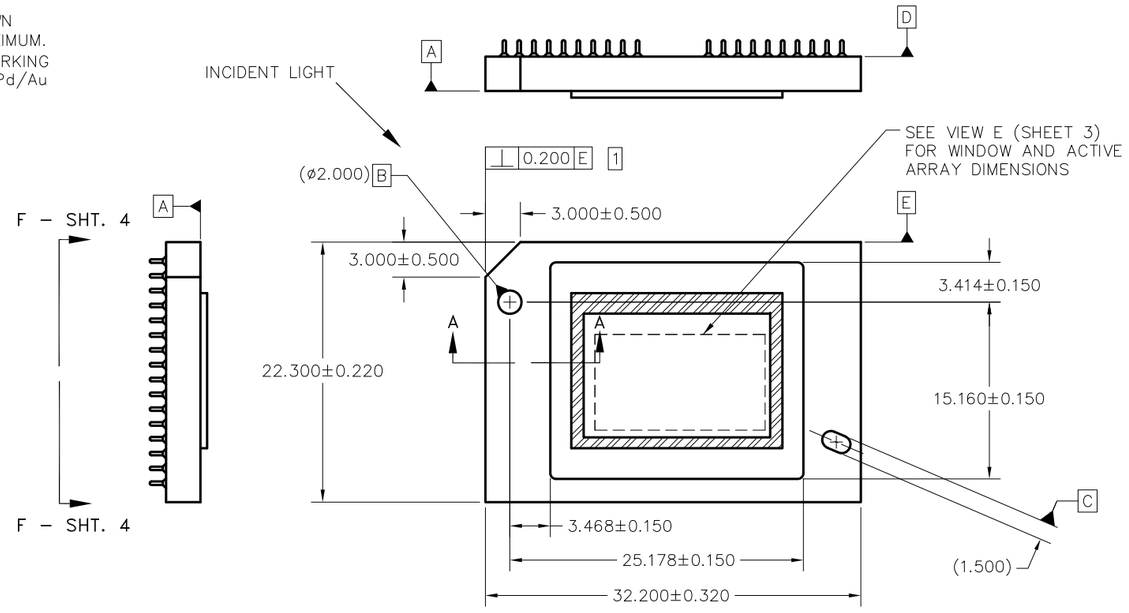
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

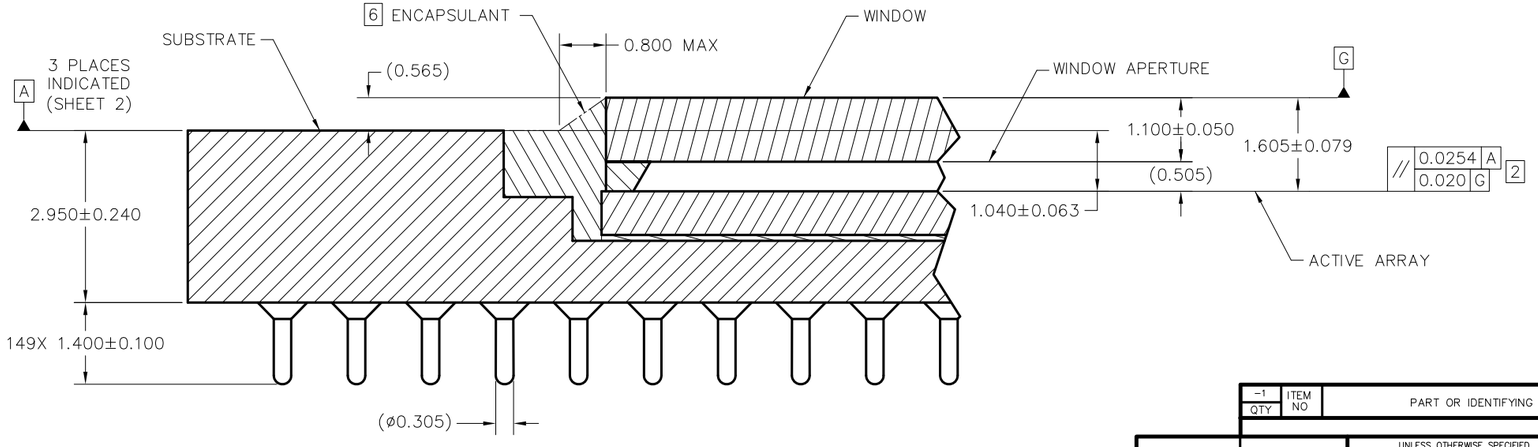
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2180591, INITIAL RELEASE	04/04/19	F. ARMSTRONG

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

ITEM NO	QTY	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
-1		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

DWN	F. ARMSTRONG	DATE 04/04/19
ENGR	F. ARMSTRONG	04/04/19
QA	S. HUDGENS	04/12/2019
CQE	M. DORAK	04/12/2019

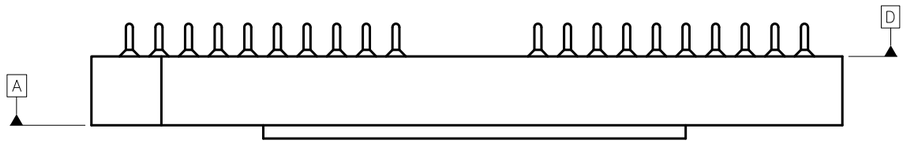
TEXAS INSTRUMENTS
Dallas, Texas

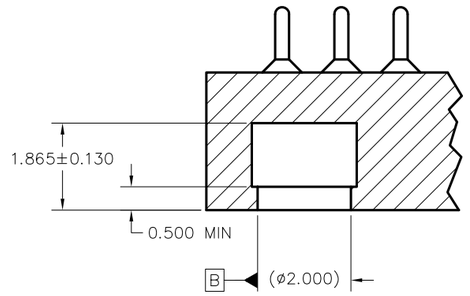
ICD, MECHANICAL, DMD
.65 1080p / UHD HSSI
SERIES 450 (FYP PACKAGE)

SIZE	DRAWING NO	REV
D	2516609	A

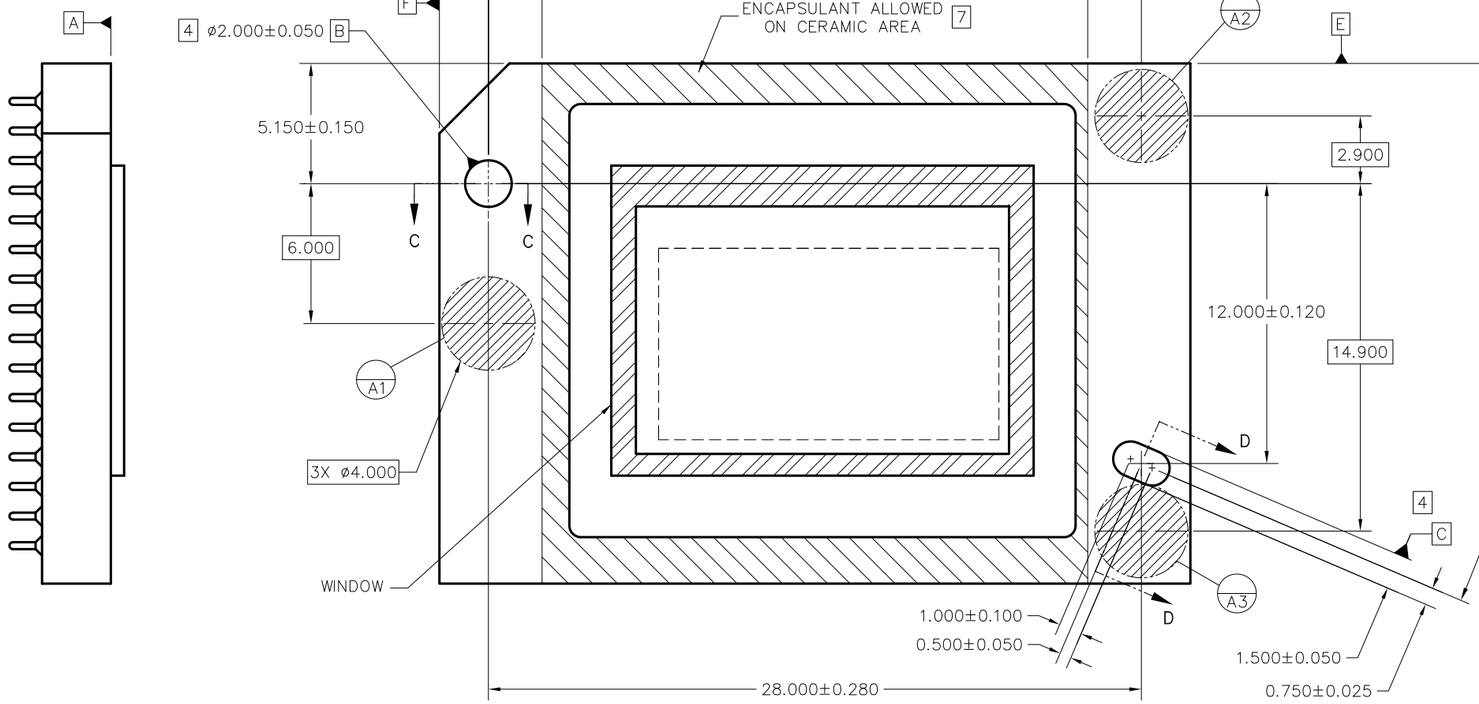
SCALE 4/1 SHEET 1 OF 4

ACED1g

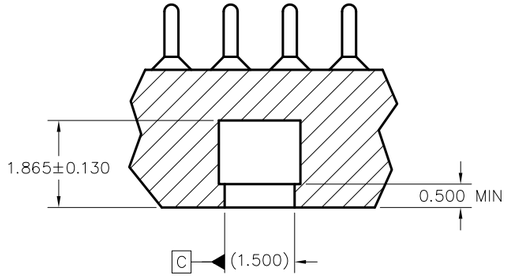




SECTION C–C
DATUM B
SCALE 16/1



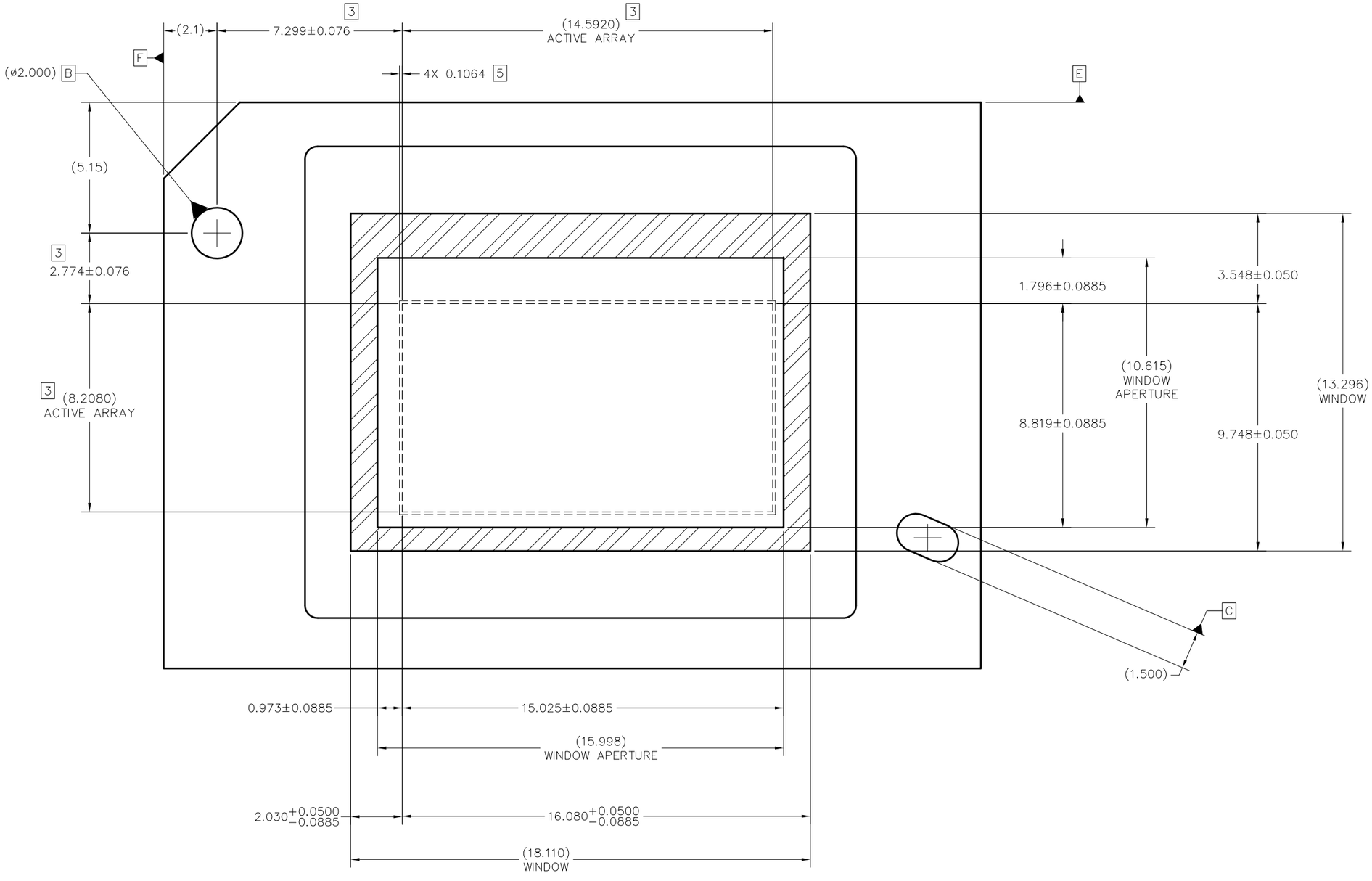
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2516609	REV A
		SCALE 4/1	SHEET 2	

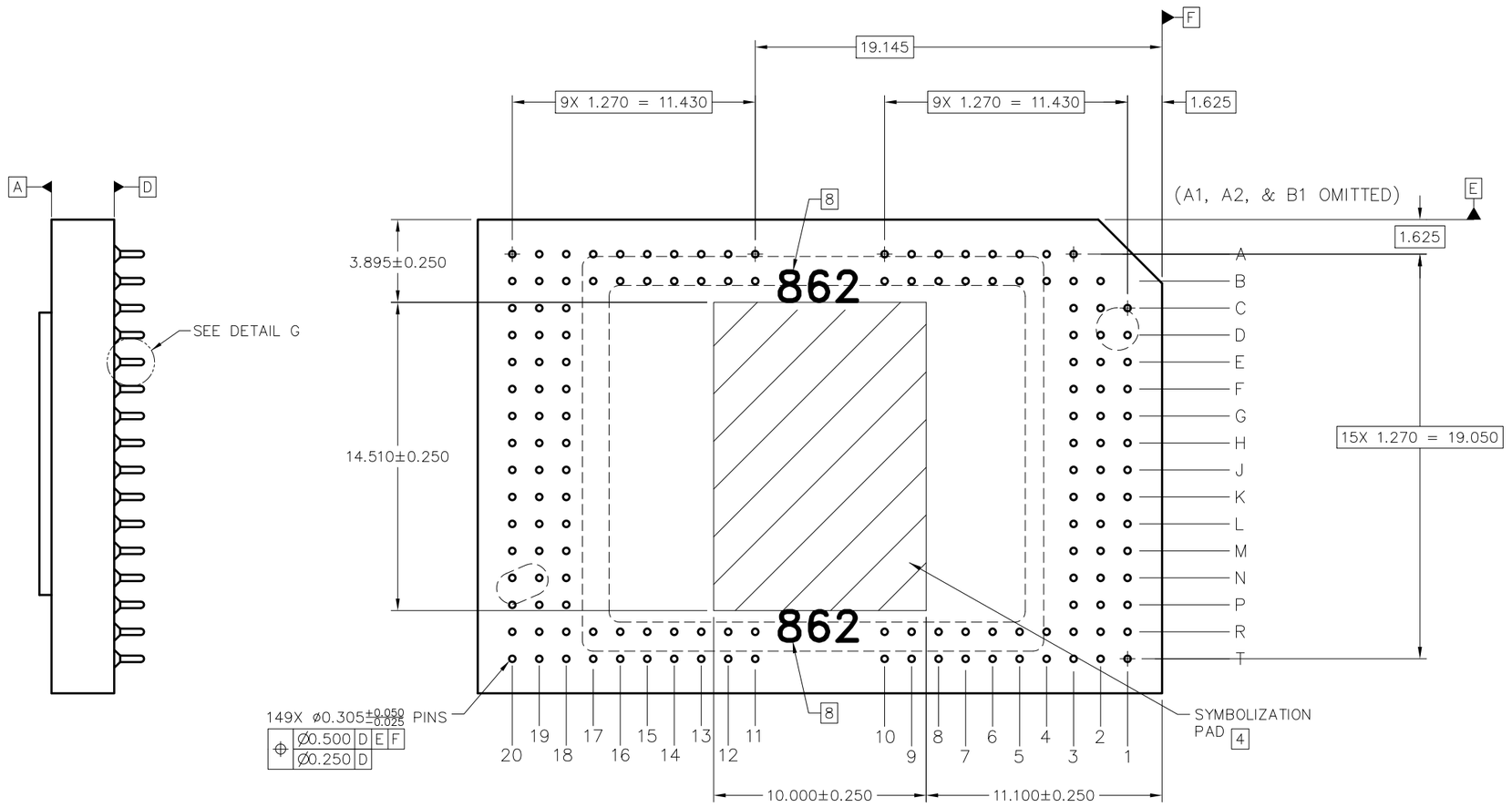
ACED2c



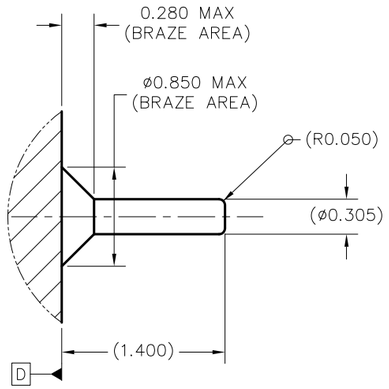
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12/1

Texas Instruments, Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2516609	REV A
	ISSUE DATE	SCALE 4/1	SHEET 3	

ACED2c



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

Texas Instruments, Dallas, Texas	DWN / DATE	SIZE D	DRAWING NO 2516609 REV A
	ISSUE DATE	SCALE 4/1	SHEET 4

ACED2c

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