DLP472TE 0.47 インチ 4K UHD デジタル マイクロミラー デバイス

1 特長

- 対角 0.47 インチのマイクロミラー アレイ
  - ディスプレイ解像度：4K UHD (3840 × 2160)
  - 5.4μm のマイクロミラー ピッチ
  - マイクロミラー傾斜角：±14.5° (平面に対して)
  - コーナー照明
- 高速シリアル インターフェイス (High-Speed Serial Interface、HSSI) 入力データ バス
- 4K UHD で 60Hz、フル HD で 240Hz をサポート
- DLPC7540 ディスプレイ コントローラ、DLPA100 パワー マネージメント、およびモータ ドライバ IC によってサポートされたレーザー蛍光 / LED / RGB レーザー / ランプ動作

2 アプリケーション

- スマート プロジェクタ
- 企業向けプロジェクタ
- レーザー TV

3 概要

DLP472TE デジタル マイクロミラー デバイス (DMD) は、デジタル制御の MEMS (micro-electromechanical system) 空間光変調器 (SLM) で、色鮮やかな 4K UHD ディスプレイ システムを実現します。TI の DLP® 製品である 0.47 インチ 4K UHD チップセットは、DMD、DLPC7540 ディスプレイ コントローラ、DLPA100 パワーおよびモータ ドライバで構成されています。このコンパクトなチップセットは、小型の 4K UHD ディスプレイを実現する完全なシステム ソリューションを提供します。
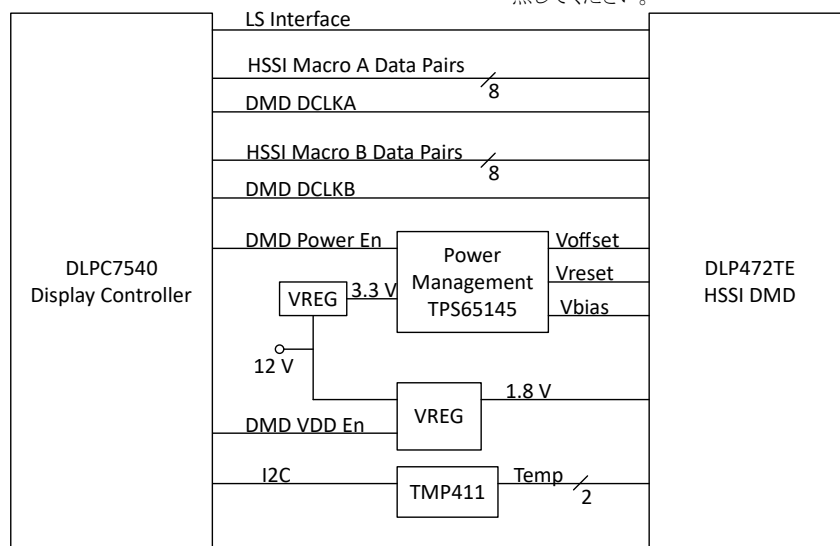
DMD のエコシステムに、設計期間の短縮に役立つ定評あるリソースが用意されています。承認済みの光学モジュール メーカーやサード パーティー プロバイダを探すには、DLP® Products サード パーティー プロバイダ検索ツールをご利用ください。

DMD を使用して設計を始める方法の詳細については、「TI の DLP ディスプレイ テクノロジーを使用した設計の開始」のページをご覧ください。

製品情報

部品番号	パッケージ[1]	パッケージ サイズ
DLP472TE	FYW (149)	32.2mm × 22.3mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。

アプリケーション概略図

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4 Pin Configuration and Functions

図 4-1. FYW Package 149-Pin PGA Bottom View

注意

Properly manage the layout and the operation of signals identified in the Pin Functions table to make sure there is reliable, long-term operation of the 0.47" 4K UHD S453 DMD. Refer to the *PCB Design Requirements for TI DLP Digital Micromirror Devices* application report for specific details and guidelines before designing the board.

表 4-1. Pin Functions

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TRACE LENGTH (mm)
NAME	No.			
D_AP(0)	J1	I	High-speed differential data pair lane A0	16.316
D_AN(0)	H1	I	High-speed differential data pair lane A0	16.316
D_AP(1)	G1	I	High-speed differential data pair lane A1	16.469
D_AN(1)	F1	I	High-speed differential data pair lane A1	16.468
D_AP(2)	F2	I	High-speed differential data pair lane A2	15.661
D_AN(2)	E2	I	High-speed differential data pair lane A2	15.661
D_AP(3)	D2	I	High-speed differential data pair lane A3	15.053
D_AN(3)	C2	I	High-speed differential data pair lane A3	15.054
D_AP(4)	A3	I	High-speed differential data pair lane A4	12.948
D_AN(4)	A4	I	High-speed differential data pair lane A4	12.948
D_AP(5)	A5	I	High-speed differential data pair lane A5	10.644
D_AN(5)	A6	I	High-speed differential data pair lane A5	10.644
D_AP(6)	A7	I	High-speed differential data pair lane A6	8.558
D_AN(6)	A8	I	High-speed differential data pair lane A6	8.557
D_AP(7)	A9	I	High-speeddifferential data pair lane A7	6.688

表 4-1. Pin Functions (続き)

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TRACE LENGTH (mm)
NAME	No.			
D_AN(7)	A10	I	High-speed differential data pair lane A7	6.688
DCLK_AP	C1	I	High-speed differential clock A	17.975
DCLK_AN	D1	I	High-speed differential clock A	17.795
D_BP(0)	A11	I	High-speed differential data pair lane B0	4.592
D_BN(0)	A12	I	High-speed differential data pair lane B0	4.591
D_BP(1)	A13	I	High-speed differential data pair lane B1	6.440
D_BN(1)	A14	I	High-speed differential data pair lane B1	6.440
D_BP(2)	A15	I	High-speed differential data pair lane B2	8.838
D_BN(2)	A16	I	High-speed differential data pair lane B2	8.838
D_BP(3)	A18	I	High-speed differential data pair lane B3	12.117
D_BN(3)	A19	I	High-speed differential data pair lane B3	12.118
D_BP(4)	D19	I	High-speed differential data pair lane B4	11.078
D_BN(4)	C19	I	High-speed differential data pair lane B4	11.078
D_BP(5)	H20	I	High-speed differential data pair lane B5	14.504
D_BN(5)	J20	I	High-speed differential data pair lane B5	14.504
D_BP(6)	D20	I	High-speed differential data pair lane B6	11.647
D_BN(6)	E20	I	High-speed differential data pair lane B6	11.646
D_BP(7)	F20	I	High-speed differential data pair lane B7	12.305
D_BN(7)	G20	I	High-speed differential data pair lane B7	12.305
DCLK_BP	B17	I	High-speed differential clock B	10.064
DCLK_BN	B18	I	High-speed differential clock B	10.243
LS_WDATA_P	T10	I	LVDS data	8.752
LS_WDATA_N	R11	I	LVDS data	1.475
LS_CLK_P	R9	I	LVDS CLK	8.656
LS_CLK_N	R10	I	LVDS CLK	7.805
LS_RDATA_A_BISTA	T13	O	LVCMOS output	2.804
BIST_B	T12	O	LVCMOS output	3.075
AMUX_OUT	B20	O	Analog test mux	10.712
DMUX_OUT	R14	O	Digital test mux	2.997
DMD_DEN_ARSTZ	T11	I	ARSTZ	2.982
TEMP_N	R8	I	Temp diode N	9.806
TEMP_P	R7	I	Temp diode P	11.986
VDD	B13, B7, C18, E3, H3, J2, K3, L2, L19, M1, M2, N3, N19, P2, P18, R3, R5, R12, R17, R19, T2, T4, T6, T8, T18	P	Digital Core supply voltage	Plane
VDDA	B11, B16, B4, B9, C20, D3, E18, G2, G19	P	HSSI supply voltage	Plane
VRESET	B3, R1	P	Supply voltage for negative bias of micromirror reset signal	Plane
VBIAS	E1, P1	P	Supply voltage for positive bias of micromirror reset signal	Plane

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English Data Sheet: DLPS273

表 4-1. Pin Functions (続き)

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TRACE LENGTH (mm)
NAME	No.			
VOFFSET	A20, B2, T1, T20	P	Supply voltage for HVCMOS logic,stepped up logic level	Plane
VSS	A17, B10, B14, B6, D18, F3, F19, J3, K19, K2, L1, L3, M3, N2, N18, N20, P3, P20, R2, R4, R6, R13, R20, T5, T7, T16, T17, T19	G	Ground	Plane
VSSA	B12, B15, B19, B5, B8, C3, E19, G3, H2, H19, K1, N1, P19, R18, T3, T9	G	Ground	Plane
N/C	F18, G18, H18, J18, J19, K18, K20, L18, L20, M18, M19, M20, R15, R16, T14, T15		No connect	

(1)   I=Input, O=Output, P=Power, G=Ground, NC = No Connect

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic and LVCMOS low-speed interface (LSIF)[1]	−0.5	2.3	V
V_{DDA}	Supply voltage for high-speed serial interface (HSSI) receivers[1]	−0.3	2.2	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[1] [2]	−0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode[1]	−0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode[1]	−15	0.5	V
$\mid V_{DDA} - V_{DD} \mid$	Supply voltage delta (absolute value)[3]		0.3	V
$\mid V_{BIAS} - V_{OFFSET} \mid$	Supply voltage delta (absolute value)[4]		11	V
$\mid V_{BIAS} - V_{RESET} \mid$	Supply voltage delta (absolute value)[5]		34	V
INPUT VOLTAGE				
	Input voltage for other inputs – LSIF and LVCMOS[1]	−0.5	2.46	V
	Input voltage for other inputs – HSSI[1] [6]	−0.2	V_{DDA}	V
LOW SPEED INTERFACE (LSIF)				
f_{CLOCK}	LSIF clock frequency (LS_CLK)		130	MHz
$\mid V_{ID} \mid$	LSIF differential input voltage magnitude[6]		810	mV
I_{ID}	LSIF differential input current		10	mA
HIGH SPEED SERIAL INTERFACE (HSSI)				
f_{CLOCK}	HSSI clock frequency (DCLK)		1.65	GHz
$\mid V_{ID} \mid$	HSSI differential input voltage magnitude Data Lane[6]		700	mV
$\mid V_{ID} \mid$	HSSI differential input voltage magnitude Clock Lane[6]		700	mV
ENVIRONMENTAL				
T_{ARRAY}	Temperature, operating[7]	0	90	°C
	Temperature, non-operating[7]	−40	90	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDA} and V_{DD} may result in excessive current draw.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS and HSSI differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in the *Micromirror Array Temperature Calculation* section.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD temperature	−40	80	°C
T_{DP-AVG}	Average dew point temperature, non-condensing[1]		28	°C
T_{DP-ELR}	Elevated dew point temperature range, non-condensing[2]	28	36	°C

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5.2 Storage Conditions (続き)

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	months

(1) The average temperature over time (including storage and operating temperatures) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±250	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES [1] [2]					
V_{DD}	Supply voltage for LVCMOS core logic and low speed interface (LSIF)	1.71	1.8	1.95	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers	1.71	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[3]	9.5	10	10.5	V
V_{BIAS}	Supply voltage for micromirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	−14.5	−14	−13.5	V
$\mid V_{DDA} - V_{DD} \mid$	Supply voltage delta, absolute value[4]			0.3	V
$\mid V_{BIAS} - V_{OFFSET} \mid$	Supply voltage delta, absolute value[5]			10.5	V
$\mid V_{BIAS} - V_{RESET} \mid$	Supply voltage delta, absolute value			33	V
LVCMOS INPUT					
V_{IH}	High level input voltage[6]	$0.7 \times V_{DD}$			V
V_{IL}	Low level input voltage[6]			$0.3 \times V_{DD}$	V
LOW SPEED SERIAL INTERFACE (LSIF)					
f_{CLOCK}	LSIF clock frequency (LS_CLK)[8]	108	120	130	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK)	44		56	%
$\mid V_{ID} \mid$	LSIF differential input voltage magnitude[8]	150	350	440	mV
V_{LVDS}	LSIF voltage[8]	575		1520	mV
V_{CM}	Common mode voltage[8]	700	900	1300	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
HIGH SPEED SERIAL INTERFACE (HSSI)					
f_{CLOCK}	HSSI clock frequency (DCLK)[7]	1.2		1.6	GHz
DCD_{IN}	HSSI duty cycle distortion (DCLK)	44	50	56	%
$\mid V_{ID} \mid$ Data	HSSI differential input voltage magnitude Data Lane[7]	100		600	mV
$\mid V_{ID} \mid$ CLK	HSSI differential input voltage magnitude Clock Lane[7]	295		600	mV
VCM_{DC} Data	Input common mode voltage (DC) Data Lane[7]	200	600	800	mV

資料に関するフィードバック(ご意見やお問い合わせ) を送信

5.4 Recommended Operating Conditions (続き)

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
VCM_{DC} CLK	Input common mode voltage (DC) Clk Lane[7]	200	600	800	mV
VCM_{ACp-p}	AC peak to peak (ripple) on common mode voltage of Data Lane and Clock Lane[7]			100	mV
Z_{LINE}	Line differential impedance (PWB/trace)		100		Ω
Z_{IN}	Internal differential termination resistance. (R_{Xterm})	80	100	120	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long–term operational[9] [10] [11]	10		40 to 70 [12]	°C
	Array temperature, short-term operational, 500 hr max[10] [13]	0		10	°C
T_{DP-AVG}	Average dew point temperature (non–condensing)[14]			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)[15]	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	months
Q_{AP-LL}	Window Aperture illumination overfill[16] [17] [18]			17	W/cm^2
LAMP ILLUMINATION					
ILL_{UV}	Illumination power at wavelength < 395 nm[9] [20]		0.68	2	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ≥395 nm and ≤800 nm[19] [20]			36.8	W/cm^2
ILL_{IR}	Illumination power at wavelength > 800 nm[20]			10	mW/cm^2
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination power at wavelength < 410 nm[9] [20]			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths between ≥410 nm and ≤800 nm[19] [20]			46.8	W/cm2
ILL_{IR}	Illumination power at wavelength > 800 nm[20]			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths between ≥410 nm and ≤475 nm[19] [20]			14.9	W/cm2
ILL_{BLU1}	Illumination power at wavelengths between ≥410 nm and ≤440 nm[19] [20]			2.4	W/cm2

(1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the V_{SS} ground pins.
(3) V_{OFFSET} supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta | $V_{DDA} - V_{DD}$ | must be less than specified limit.
(5) To prevent excess current, the supply voltage delta | $V_{BIAS} - V_{OFFSET}$ | must be less than specified limit.
(6) LVCMOS input pin is DMD_DEN_ARSTZ.
(7) See the high speed serial interface (HSSI) timing requirements in the *Timing Requirements*.
(8) See the low speed interface (LSIF) timing requirements in the *Timing Requirements*.
(9) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination reduces device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), using the *Micromirror Array Temperature Calculation*.
(11) Long-term is defined as the usable life of the device.
(12) The maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See the *Micromirror Landed-On/Landed-Off Duty Cycle* section for a definition of micromirror landed duty cycle
(13) Short-term is the total cumulative time over the useful life of the device.
(14) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(15) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR}.
(16) Applies to region defined in Illumination Overfill Diagram—Critical Area.
(17) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Minimizing the

light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system, the amount of overfill light on the outside of the active array may cause system performance degradation.

(18) To calculate see the *Window Aperture Illumination Overfill Calculation* section.

(19) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).

(20) To calculate see the *Micromirror Power Density Calculation* section.
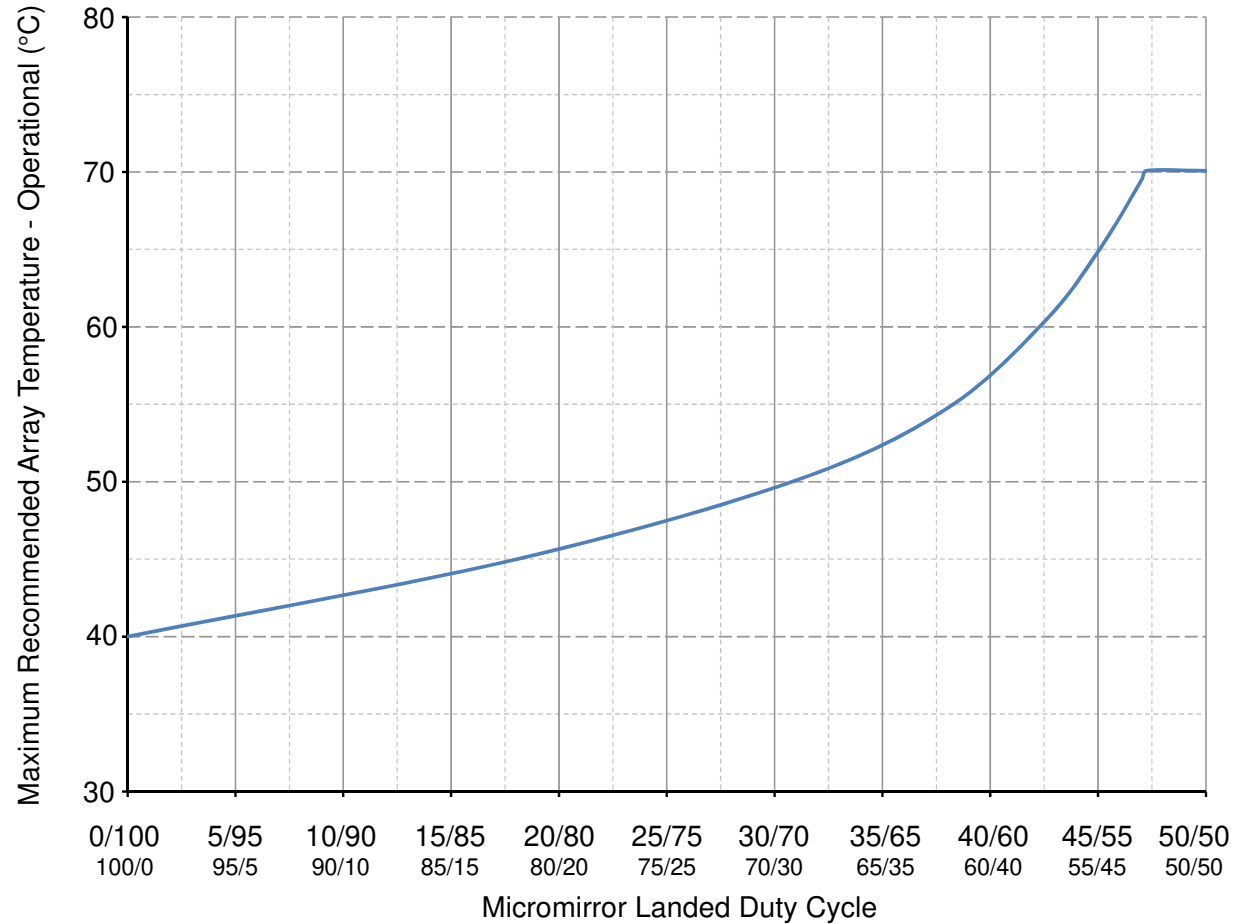
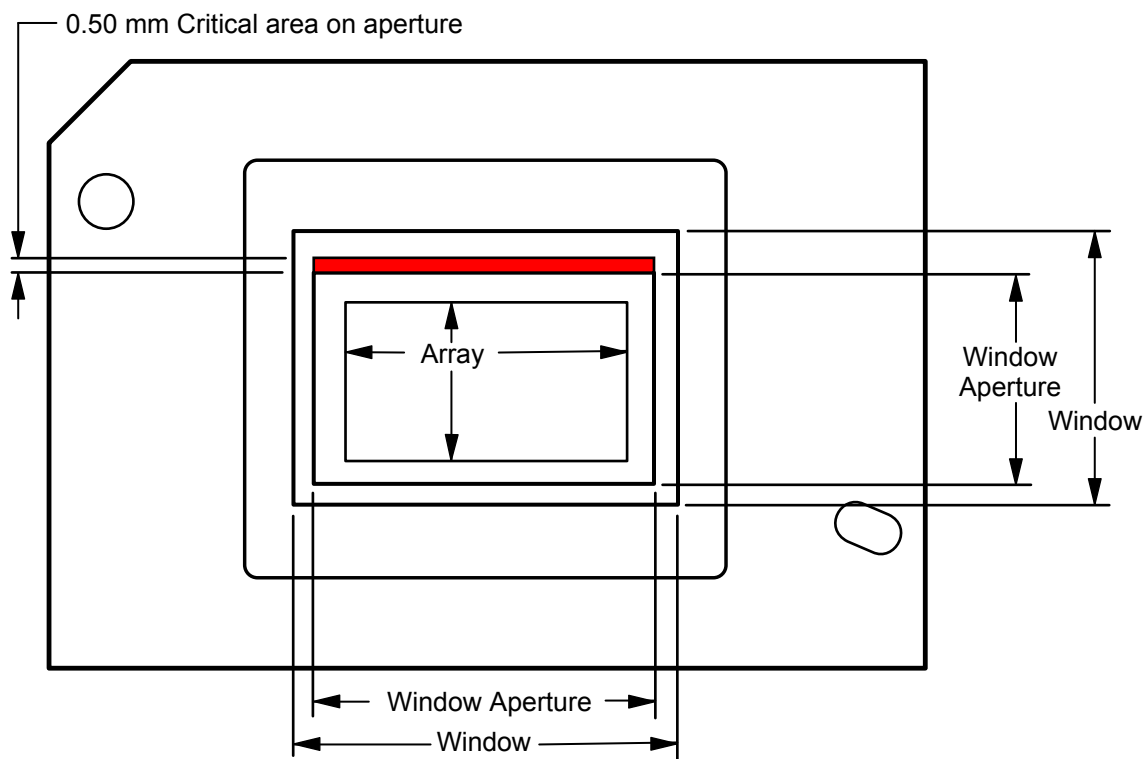**図 5-1. Maximum Recommended Array Temperature—Derating Curve**

0.50 mm Critical area on aperture

図 5-2. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

THERMAL METRIC	DLP472TE	UNIT
	FYW PACKAGE	
	149 PINS	
Thermal Resistance, active area to test point 1 (TP1)[1]	1.0	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems must be designed to minimize the light energy falling outside the window's clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER[1] [2]		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
CURRENT – TYPICAL						
I_{DD}	Supply current V_{DD} [3]			800	1200	mA
I_{DDA}	Supply current V_{DDA} [3]			1000	1200	mA
I_{DDA}	Supply current V_{DDA} [3]	Single macro mode		500	600	mA
I_{OFFSET}	Supply current V_{OFFSET} [4] [5]			20	25	mA
I_{BIAS}	Supply current V_{BIAS} [4] [5]			2.5	4.0	mA
I_{RESET}	Supply current V_{RESET} [5]		−9.3	−6.9		mA
POWER – TYPICAL						
P_{DD}	Supply power dissipation V_{DD} [3]			1440	2437.5	mW

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5.6 Electrical Characteristics (続き)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER[1] [2]		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
P_{DDA}	Supply power dissipation V_{DDA} [3]			1620	2340	mW
P_{DDA}	Supply power dissipation V_{DDA} [3]	single macro mode		900	1170	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} [4] [5]			230	367.5	mW
P_{BIAS}	Supply power dissipation V_{BIAS} [4] [5]			43.2	70.3	mW
P_{RESET}	Supply power dissipation V_{RESET} [5]			107.8	152.25	mW
P_{TOTAL}	Supply power dissipation Total			3441	5367.55	mW
LVCMOS INPUT						
I_{IL}	Low level input current [6]	V_{DD} = 1.95V, V_I = 0V	−100			nA
I_{IH}	High level input current [6]	V_{DD} = 1.95V, V_I = 1.95V			135	µA
LVCMOS OUTPUT						
V_{OH}	DC output high voltage [7]	I_{OH} = −2mA	$0.8 \times V_{DD}$			V
V_{OL}	DC output low voltage [7]	I_{OL} = 2mA			$0.2 \times V_{DD}$	V
RECEIVER EYE CHARACTERISTICS						
A1	Minimum data eye opening[8] [9]		100		600	mV
A1	Minimum clock eye opening[8] [9]		295		600	mV
A2	Maximum data signal swing[8] [9]				600	mV
X1	Maximum data eye closure [8]				0.275	UI
X2	Maximum data eye closure[8]				0.4	UI
| t_{DRIFT} |	Drift between Clock and Data between Training Patterns				20	ps
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	f = 1MHz			10	pF
C_{IN}	Input capacitance LSIF (low-speed interface)	f = 1MHz			20	pF
C_{IN}	Input capacitance HSSI (high-speed serial interface)	f = 1MHz			20	pF
C_{OUT}	Output capacitance	f = 1MHz			10	pF

(1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are concerning the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta \| $V_{DDA} - V_{DD}$ \| must be less than the specified limit.
(4) To prevent excess current, the supply voltage delta \| $V_{BIAS} - V_{OFFSET}$ \| must be less than the specified limit.
(5) Supply power dissipation based on 3 global resets in 200µs.
(6) LVCMOS input specifications are for pin DMD_DEN_ARSTZ.
(7) LVCMOS output specification is for pins LS_RDATA_A and LS_RDATA_B.
(8) Refer to the HSSI eye characteristics, Receiver Eye Mask (1e-12 BER).
(9) Defined in the recommended operating conditions

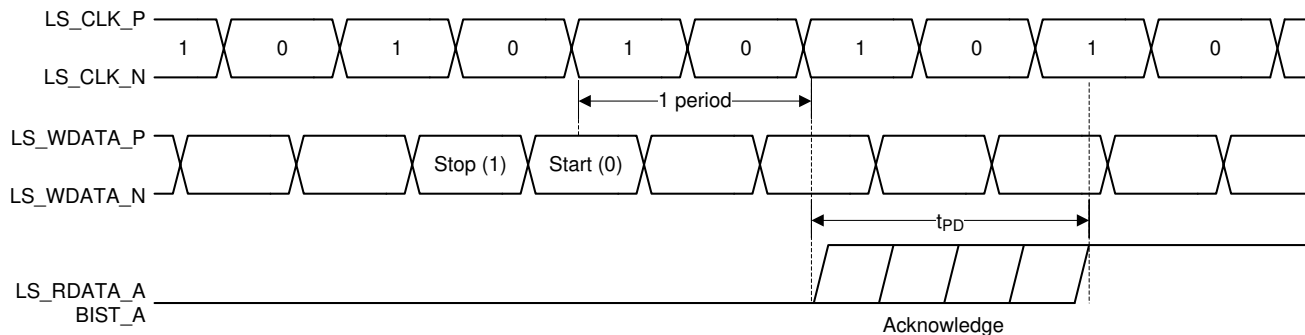## 5.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Output propagation, Clock to Q (C2Q), rising edge of LS_CLK (differential clock signal) input to LS_RDATA output.[1]	C_L = 5pF			11.1	ns
		C_L = 10pF			11.3	ns
	Slew rate, LS_RDATA	20%–80%, C_L <10pF		0.5		V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B	50–(C2Q rise – C2Q fall) × 130e6 × 100	40%		60%	

(1)   See 図 5-3.

図 5-3. Switching Characteristics

5.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS						
t_r	Rise time[1]	20% to 80% reference points			25	ns
t_f	Fall time[1]	80% to 20% reference points			25	ns
LOW SPEED INTERFACE (LSIF)						
t_r	Rise time[2]	20% to 80% reference points			450	ps
t_f	Fall time[2]	80% to 20% reference points			450	ps
$t_{W(H)}$	Pulse duration high[3]	LS_CLK. 50% to 50% reference points	3.1			ns
$t_{W(L)}$	Pulse duration low[3]	LS_CLK. 50% to 50% reference points	3.1			ns
t_{su}	Setup time[4]	LS_WDATA valid before rising edge of LS_CLK (differential)			1.5	ns
t_h	Hold time[4]	LS_WDATA valid after rising edge of LS_CLK (differential)			1.5	ns
HIGH SPEED SERIAL INTERFACE (HSSI)						
t_r	Rise time[5] [6]—data	from -A1 to A1 minimum eye height specification	50		115	ps
	Rise time[5] [6]—clock	from -A1 to A1 minimum eye height specification	50		135	ps
t_f	Fall time[5] [6]—data	from A1 to -A1 minimum eye height specification	50		115	ps
	Fall time[5] [6]—clock	from A1 to -A1 minimum eye height specification	50		135	
$t_{W(H)}$	Pulse duration high[7]	DCLK. 50% to 50% reference points	0.275			ns
$t_{W(L)}$	Pulse duration low[7]	DCLK. 50% to 50% reference points	0.275			ns

(1) See 図 5-10 for rise time and fall time for LVCMOS.
(2) See 図 5-6 for rise time and fall time for LSIF.
(3) See 図 5-5 for pulse duration high and low time for LSIF.
(4) See 図 5-5 for setup and hold time for LSIF.
(5) See 図 5-12 for rise time and fall time for HSSI Eye Characteristics.
(6) See 図 5-11 for rise time and fall time for HSSI.
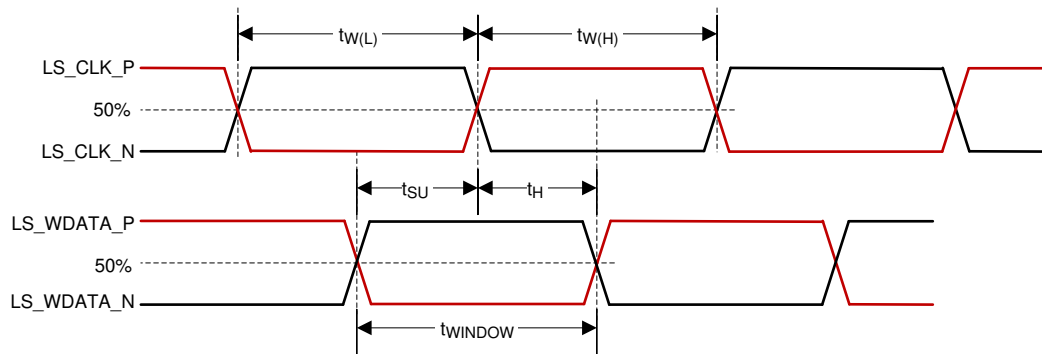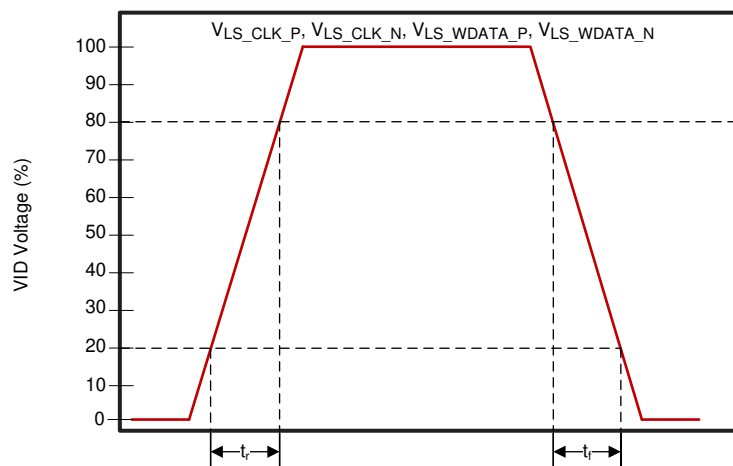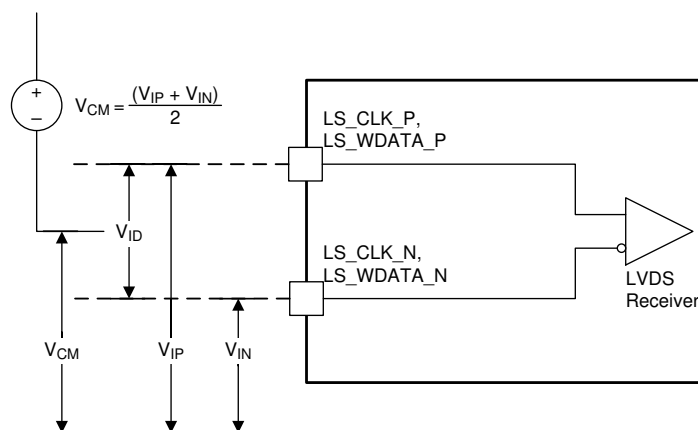(7) See 図 5-13 for pulse duration high and low for HSSI.

A.   See 式 1 and 式 2.
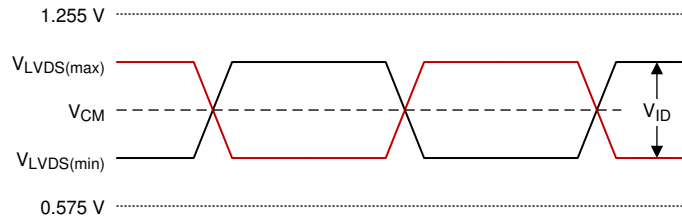
図 5-4. LSIF Waveform Requirements

$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left| \frac{1}{2} \times V_{ID\,(max)} \right|$$

(1)

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left| \frac{1}{2} \times V_{ID\,(max)} \right|$$

(2)

図 5-5. LSIF Timing Requirements

図 5-6. LSIF Rise, Fall Time Slew
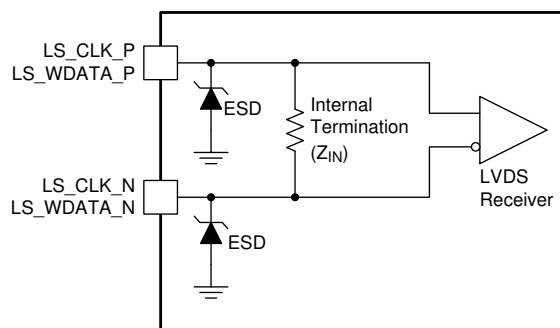

図 5-7. LSIF Voltage Requirements
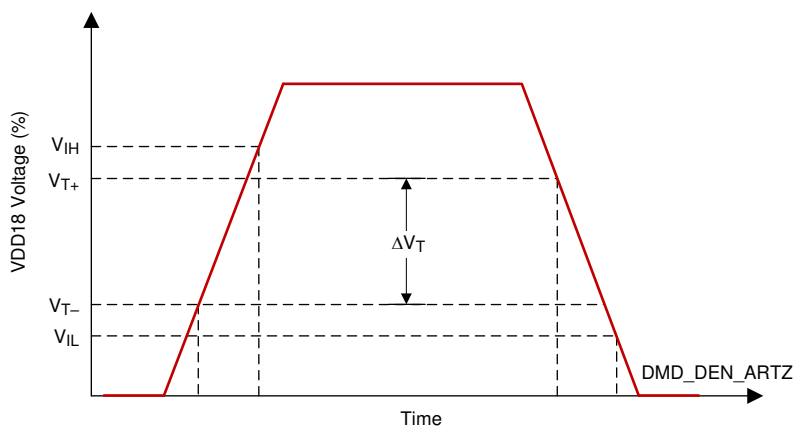
図 5-8. LSIF Equivalent Input

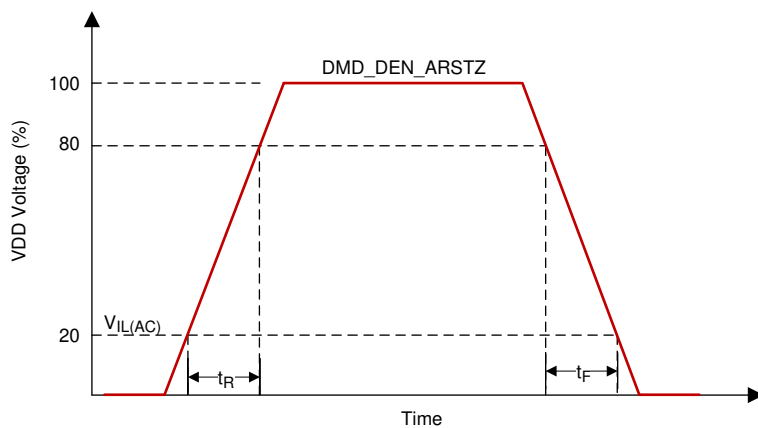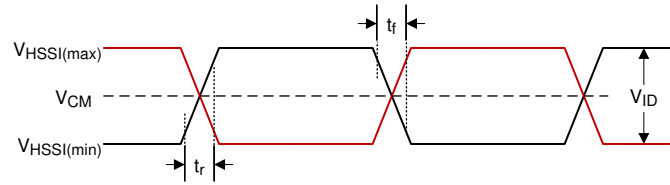**図 5-9. LVCMOS Input Hysteresis**

図 5-10. LVCMOS Rise, Fall Time Slew Rate

A.   See Equation 1 and Equation 2.

図 5-11. HSSI Waveform Requirements

$$V_{HSSI(max)} = V_{CM(max)} + \left| \frac{1}{2} \times V_{ID(max)} \right|$$

(3)

$$V_{HSSI(min)} = V_{CM(min)} - \left| \frac{1}{2} \times V_{ID(max)} \right|$$

(4)

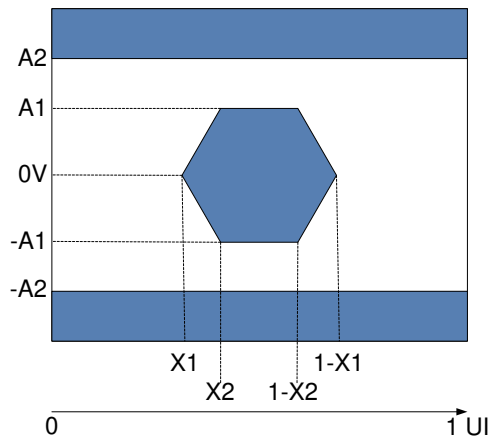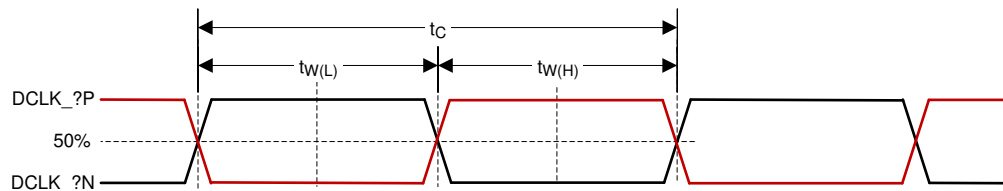**図 5-12. HSSI Eye Characteristics**

図 5-13. HSSI CLK Characteristics

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5.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
When loads are applied to the electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area[1]			111	N
Maximum load to be applied to the thermal interface area[1]			111	N
When a load is applied to only the electrical interface area				
Maximum load to be applied to the electrical interface area[1]			222	N
Maximum load to be applied to the thermal interface area[1]			0	N

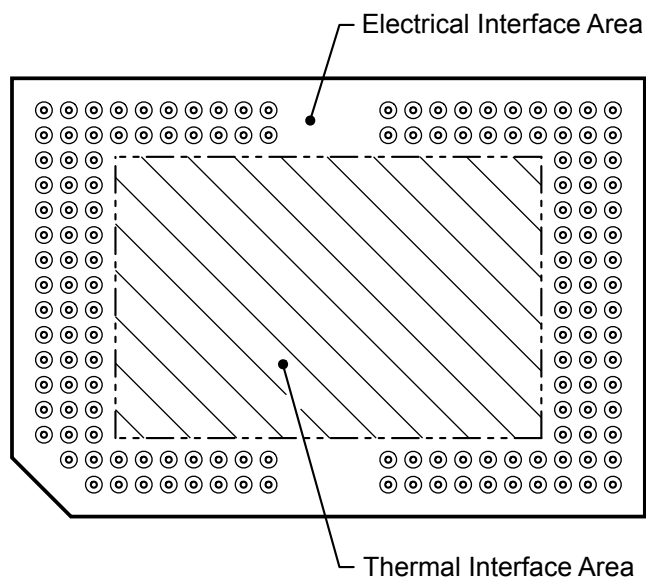(1) The load should be uniformly applied in the corresponding areas shown in 図 5-14.

図 5-14. System Mounting Interface Loads

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5.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns[1] [2]	M	1920	micromirrors
Number of active rows[1] [2]	N	1080	micromirrors
Micromirror (pixel) pitch [1]	P	5.4	µm
Micromirror active array width[1]	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height[1]	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border[3]	Pond of micromirror (POM)	20	micromirrors/side

(1) See 図 5-15.
(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed.
(3) The structure and qualities of the border around the active array include a band of partially functional micromirrors referred to as the *Pond Of Micromirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.
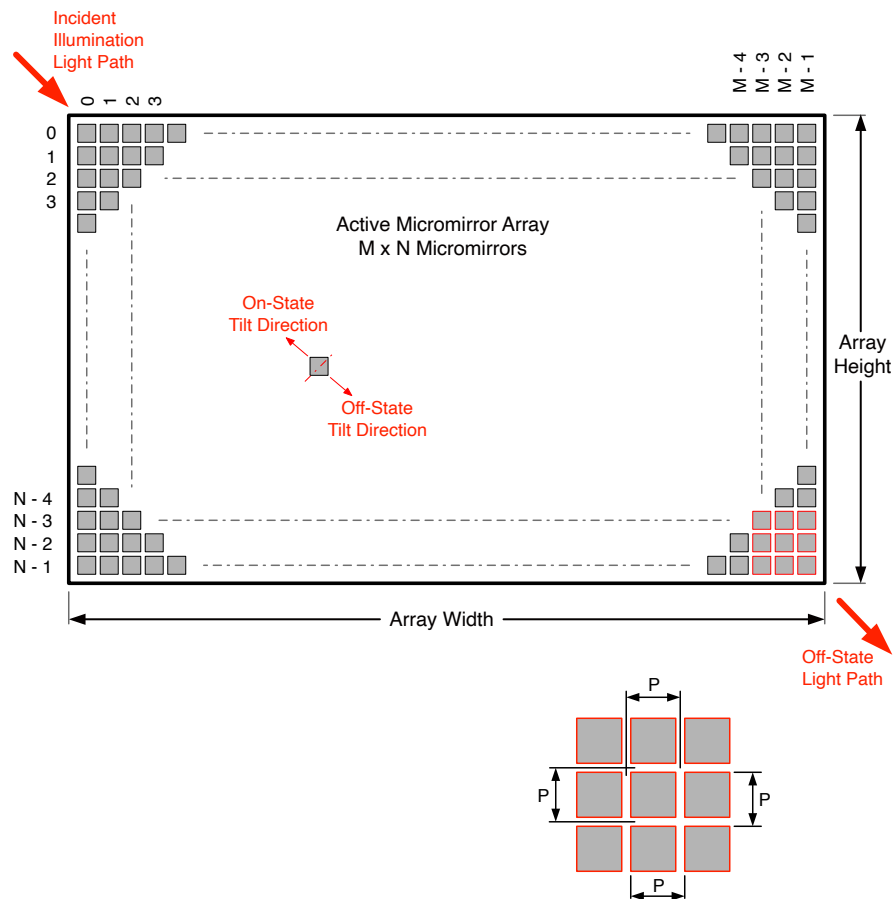

図 5-15. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle [1] [2] [3] [4]		Landed state	13.5	14.5	15.5	degrees
Micromirror crossover time [5]		Typical performance		3		μs
Micromirror switching time [6]		Typical performance	6			
Image performance[7]	Bright pixel(s) in active area [8]	Gray 10 Screen [9]			0	micromirrors
	Bright pixel(s) in the POM [10]	Gray 10 Screen [9]			1	
	Dark pixel(s) in the active area [11]	White Screen			4	
	Adjacent pixel(s) [12]	Any Screen			0	
	Unstable pixel(s) in active area [13]	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(3) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(4) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(6) The minimum time between successive transitions of a micromirror.
(7) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
   Test set degamma shall be linear.
   Test set brightness and contrast shall be set to nominal.
   The diagonal size of the projected image shall be a minimum of 60 inches.
   The projections screen shall be 1X gain.
   The projected image shall be inspected from a 8 foot minimum viewing distance.
   The image shall be in focus during all image quality tests.
(8) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
(9) Gray 10 screen definition: All areas of the screen are colored with the following settings:
   Red = 10/255
   Green = 10/255
   Blue = 10/255
(10) POM definition: Rectangular border of off-state mirrors surrounding the active area.
(11) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

5.12 Window Characteristics

DESCRIPTION[1]		MIN	TYP	MAX
Window material			Corning Eagle XG	
Window refractive index	At wavelength 546.1nm		1.5119	

(1)   See セクション 6.5 for more information.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP472TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding the limits described previously.

6 Detailed Description

6.1 Overview

The DLP472TE digital micromirror device (DMD) is a 0.47-inch diagonal spatial light modulator, which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the *Functional Block Diagram*. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.47" 4K UHD chipset is comprised of the DLP472TE DMD, DLPC7540 display controller and the DLPA100 power management and motor driver. For reliable operation, always use the DLP472TE DMD with the DLP display controller and the power management and motor driver specified in the chipset.

6.2 Functional Block Diagram

資料に関するフィードバック(ご意見やお問い合わせ)を送信   21
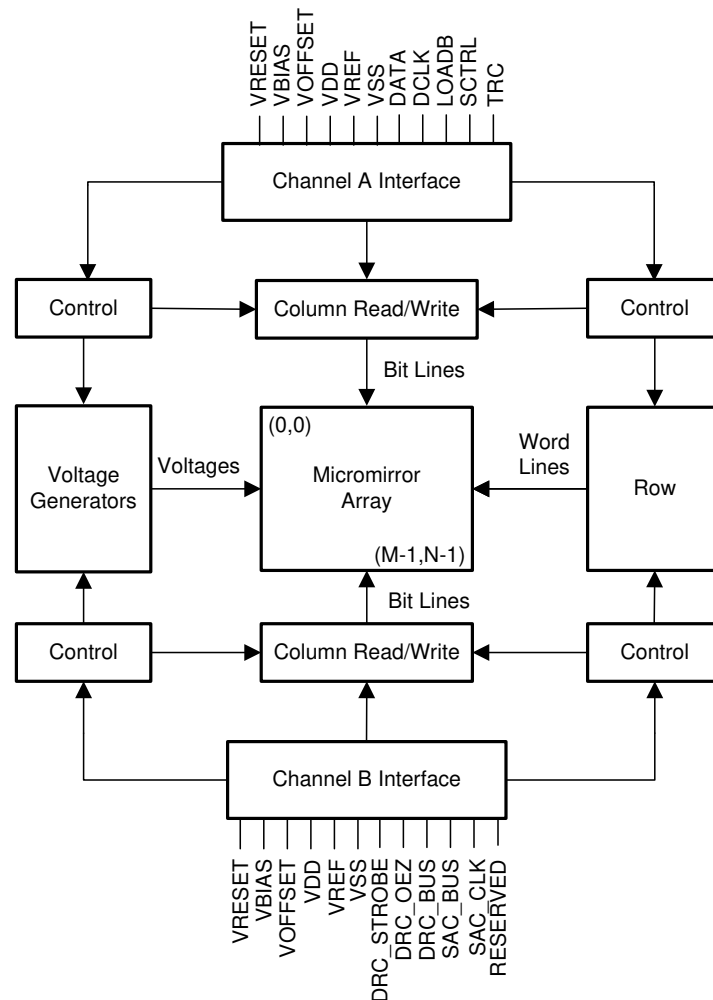
6.3 Feature Description

6.3.1 Power Interface

The DMD requires four DC voltages: 1.8V source, V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical configuration, 3.3V is created by the DLPA100 power management and motor driver and is used on the DMD board to create the 1.8V. The TI voltage regulator TPS65145 takes in the 3.3V and outputs V_{OFFSET}, V_{RESET}, V_{BIAS}.

6.3.2 Timing

The data sheet specifies the timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC7540 display controller. See the DLPC7540 display controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance with the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level to be acceptable.

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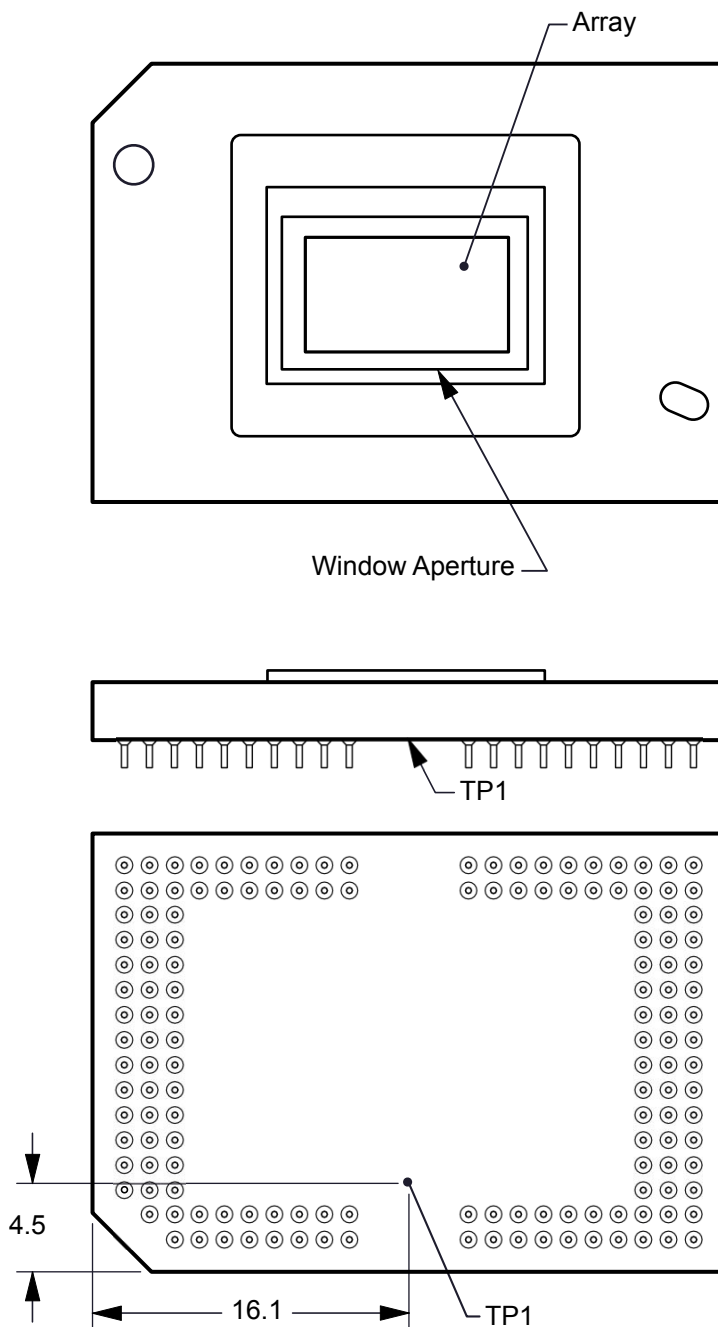## 6.6 Micromirror Array Temperature Calculation

図 6-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1, shown above.

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \tag{5}$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \tag{6}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in *Section 6.5* from array to ceramic TP1 (°C/ Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.54

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 2.5W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single-chip or multi-chip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 25W \text{ (measured)} \tag{7}$$

$$T_{CERAMIC} = 50.0°C \text{ (measured)} \tag{8}$$

$$Q_{ELECTRICAL} = 2.5W \tag{9}$$

$$Q_{ARRAY} = 2.5W + (0.54 \times 25 \text{ W}) = 16W \tag{10}$$

$$T_{ARRAY} = 50.0°C + (16W \times 1.0°C/W) = 66.0°C \tag{11}$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \text{ (mW/W)} \div A_{ILL} \text{ (mW/cm}^2)$

- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL} \text{ (W/cm}^2)$

- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \text{ (mW/W)} \div A_{ILL} \text{ (mW/cm}^2)$

- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL} \text{ (W/cm}^2)$

- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL} \text{ (W/cm}^2)$

- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL}) \text{ (cm}^2)$

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where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)

- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)

- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)

- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)

- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)

- A_{ILL} = illumination area on the DMD (cm^2)

- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)

- A_{ARRAY} = area of the array (cm^2) (data sheet)

- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)

- $OP_{UV-RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{VIS-RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{IR-RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{BLU-RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{BLU1-RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤440nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$$Q_{INCIDENT} = 25W \text{ (measured)} \tag{12}$$

$$A_{ARRAY} = (10.368mm \times 5.832mm) \div 100cm^2/mm^2 = 0.6047cm^2 \text{ (data sheet)} \tag{13}$$

$$OV_{ILL} = 16.3\% \text{ (optical model)} \tag{14}$$

$$OP_{UV-RATIO} = 0.00017 \text{ (spectral measurement)} \tag{15}$$

$$OP_{VIS-RATIO} = 0.99977 \text{ (spectral measurement)} \tag{16}$$

$$OP_{IR-RATIO} = 0.00006 \text{ (spectral measurement)} \tag{17}$$

$$OP_{BLU-RATIO} = 0.28100 \text{ (spectral measurement)} \tag{18}$$

$$OP_{BLU1-RATIO} = 0.03200 \text{ (spectral measurement)} \tag{19}$$

$$A_{ILL} = 0.6047cm^2 \div (1 - 0.163) = 0.7224cm^2 \tag{20}$$

$$ILL_{UV} = [0.00017 \times 25W] \times 1000mW/W \div 0.7224cm^2 = 5.883mW/cm^2 \tag{21}$$

$$ILL_{VIS} = [0.99977 \times 25W] \div 0.7224cm^2 = 34.60W/cm^2 \tag{22}$$

$$ILL_{IR} = [0.00006 \times 25W] \times 1000mW/W \div 0.7224cm^2 = 2.076mW/cm^2 \tag{23}$$

$$ILL_{BLU} = [0.28100 \times 25W] \div 0.7224cm^2 = 9.72W/cm^2 \tag{24}$$

$$ILL_{BLU1} = [0.03200 \times 25W] \div 0.7224cm^2 = 1.11W/cm^2 \tag{25}$$

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array, the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

- $Q_{AP\text{-}ILL} = [Q_{INCIDENT} \times OP_{AP\_ILL\_RATIO}] \div A_{AP\_ILL}$ (W/cm^2)

where:

- $Q_{AP\text{-}ILL}$ = window aperture illumination overfill (W/cm^2)

- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)

- $OP_{AP\_ILL\_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)

- $A_{AP\text{-}ILL}$ = size of the window aperture critical area (cm^2) (datasheet)

- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)
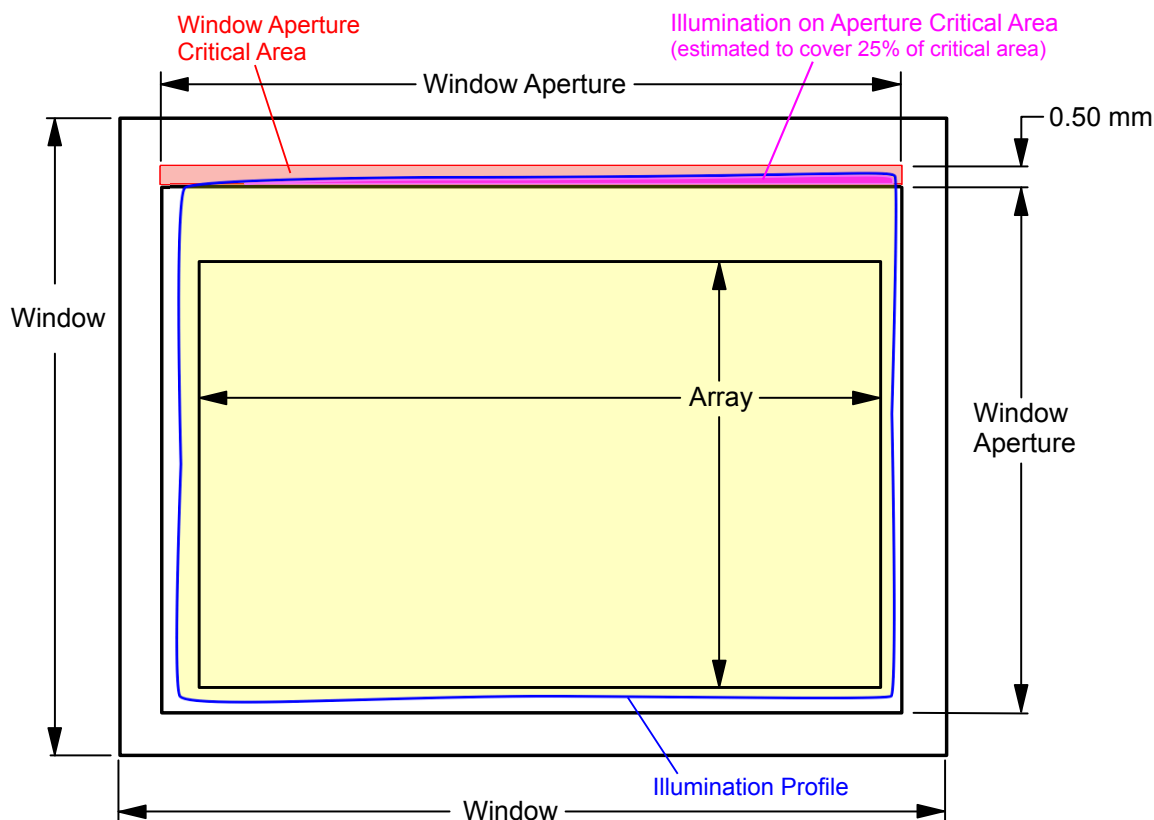
Sample calculation:

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図 6-2. Window Aperture Overfill Example

See the figure for the length of the critical aperture.

$Q_{INCIDENT}$ = 25W (measured)   (26)

$OP_{AP\_ILL\_RATIO}$ = 0.312% (optical model)   (27)

OV_{CA_RATIO} = 25% (optical model)   (28)

Length of the window aperture for critical area = 1.2496cm (data sheet)   (29)

Width of critical area = 0.050cm (data sheet)   (30)

A_{AP-ILL} = 1.2496cm × 0.050cm = 0.6248 (cm^2)   (31)

Q_{AP-ILL} = (25W × 0.00312) ÷ (0.6248cm^2 × 0.25) = 5.0 (W/cm^2)   (32)

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6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the de-rating curve shown in 図 5-1. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 6-1.

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表 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use 式 33 to calculate the landed duty cycle of a given pixel during a given time period

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (33)$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in 表 6-2 and 表 6-3.

表 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	**GREEN**	**BLUE**
30%	50%	20%

表 6-3. **Example Landed Duty Cycle for Full-Color**

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	30/70
0%	100%	0%	50/50
0%	0%	100%	20/80
0%	12%	0%	6/94
0%	0%	35%	7/93
60%	0%	0%	18/82
0%	100%	100%	70/30
100%	0%	100%	50/50
100%	100%	0%	80/20
0%	12%	35%	13/87
60%	0%	35%	25/75
60%	12%	0%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC7540 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC7540 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 6-3.
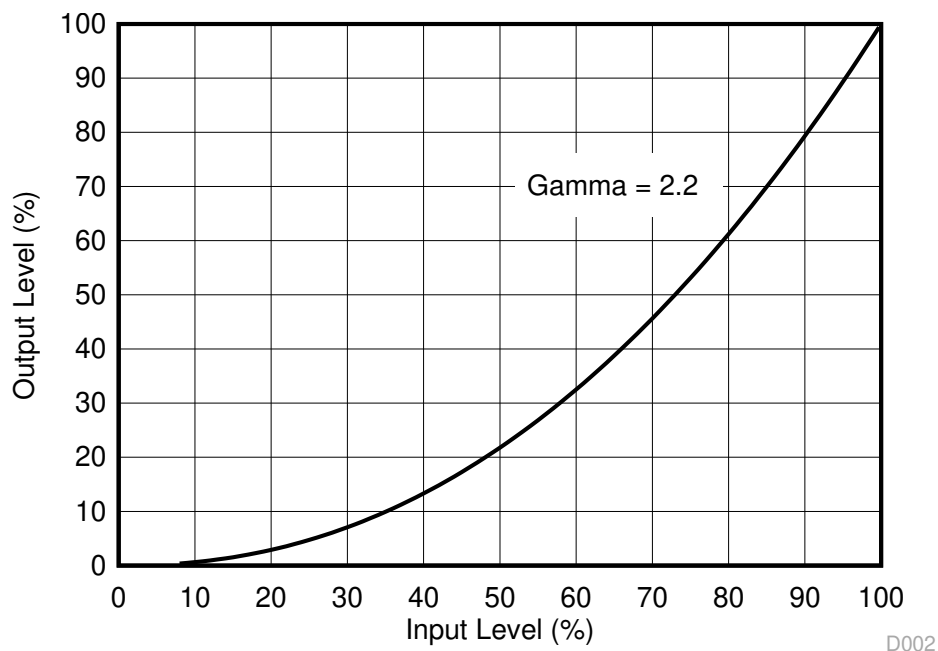

図 6-3. **Example of Gamma = 2.2**

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From 図 6-3, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing which occurs before the DLPC7540 controllers.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

DMDs are spatial light modulators that reflect incoming light from an illumination source in one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC7540 controller. The high tilt pixel in the corner-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Typical applications using the DLP472TE include Laser TVs, home cinemas, and business projectors.

DMD power-up and power-down sequencing are strictly controlled by the DLPC7540 through the TPS65145 PMIC. Refer to セクション 8 for power-up and power-down specifications. To ensure reliable operation, the DLP472TE DMD must always be used with the DLPC7540 controller, the DLPA100 PMIC/Motor driver, and the TPS65145 PMIC.

7.2 Typical Application

The DLP472TE DMD combined with the DLPC7540 digital controller and a power management device provides full 4K UHD resolution for bright, colorful display applications. A typical display system using laser phosphor illumination combines the DLP472TE DMD, DLPC7540 display controller, TPS65145 voltage regulator, and DLPA100 PMIC and motor driver. 図 7-1 shows a system block diagram for the Laser Phosphor configuration of the DLP 0.47" 4K UHD chipset. 図 7-2, shows a system block diagram for the LED configuration of the DLP 0.47" 4K UHD chipset. The components include the DLP472TE DMD, DLPC7540 display controller, DLPA100 PMIC and motor driver, and the TPS65145 PMIC.
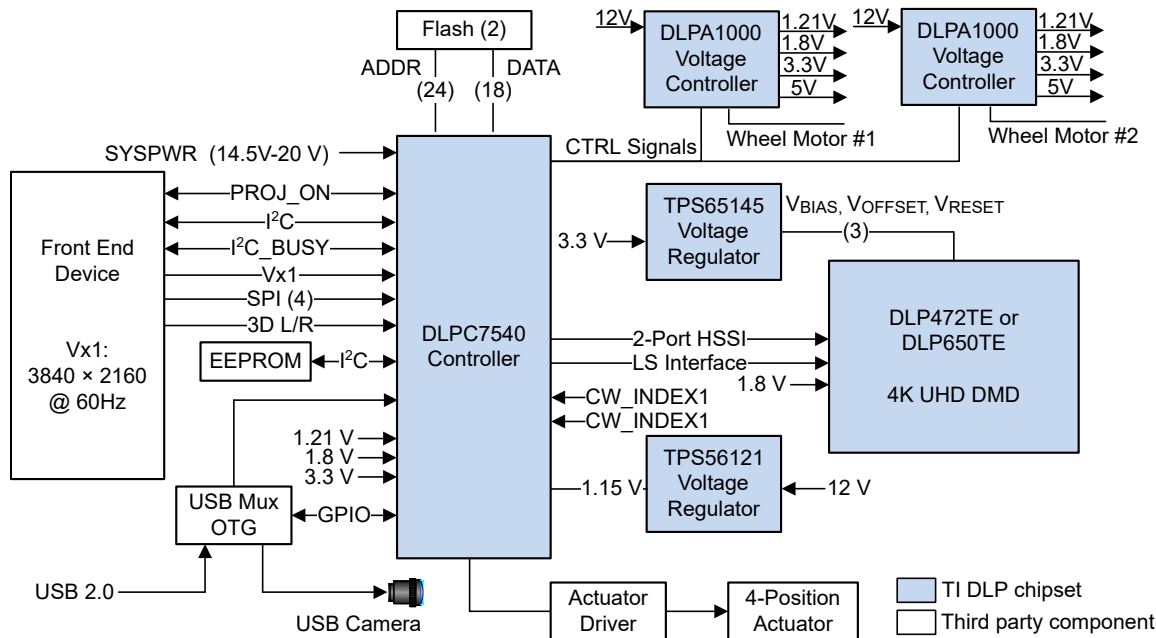
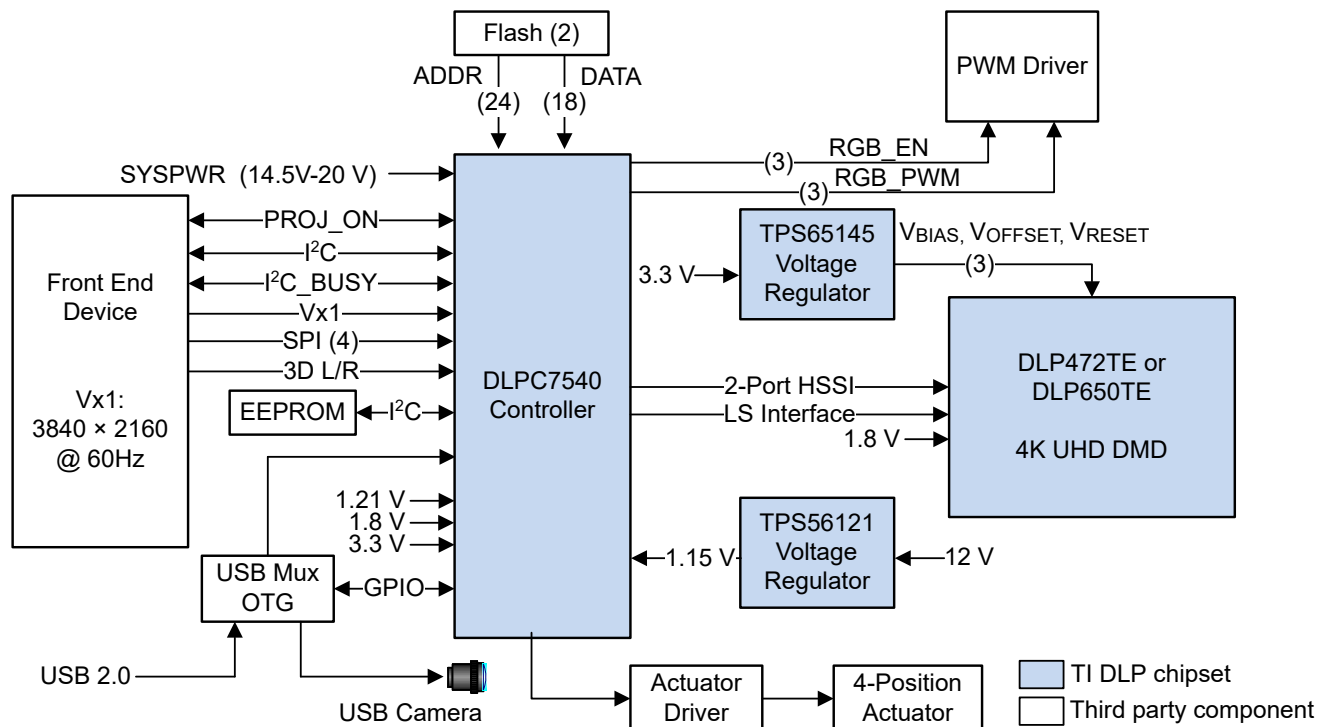図 7-1. **Typical 4K UHD Laser Phosphor Application Diagram**

図 7-2. **Typical 4K UHD LED Application Diagram**

7.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness have a major effect on the overall system design and size.

The display system uses the DLP472TE as the core imaging device and contains a 0.47-inch array of micromirrors. The DLPC7540 controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The DLPA100 PMIC serves as a voltage regulator for the controller, and color filter wheel and phosphor wheel motor control. The TPS65145 provides the DMD reset, offset, and bias voltages. The LMR33630C provides 1.8V power to the DLP472TE.

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP472TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with the DLPC7540 display controller and the TPS65145 PMIC and DLPA100. Refer to PCB Design Requirements for TI DLP Digital Micromirror Devices for the DMD board design and manufacturing handling of the DMD sub-assemblies.

7.2.3 Application Curve

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determine the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. 図 7-3 describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit.
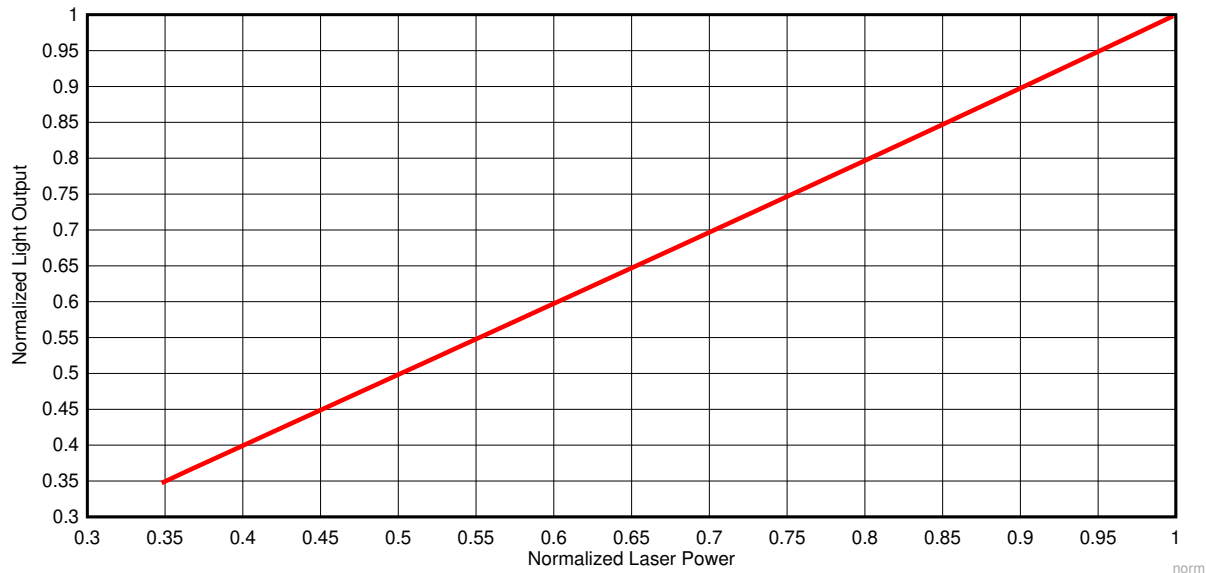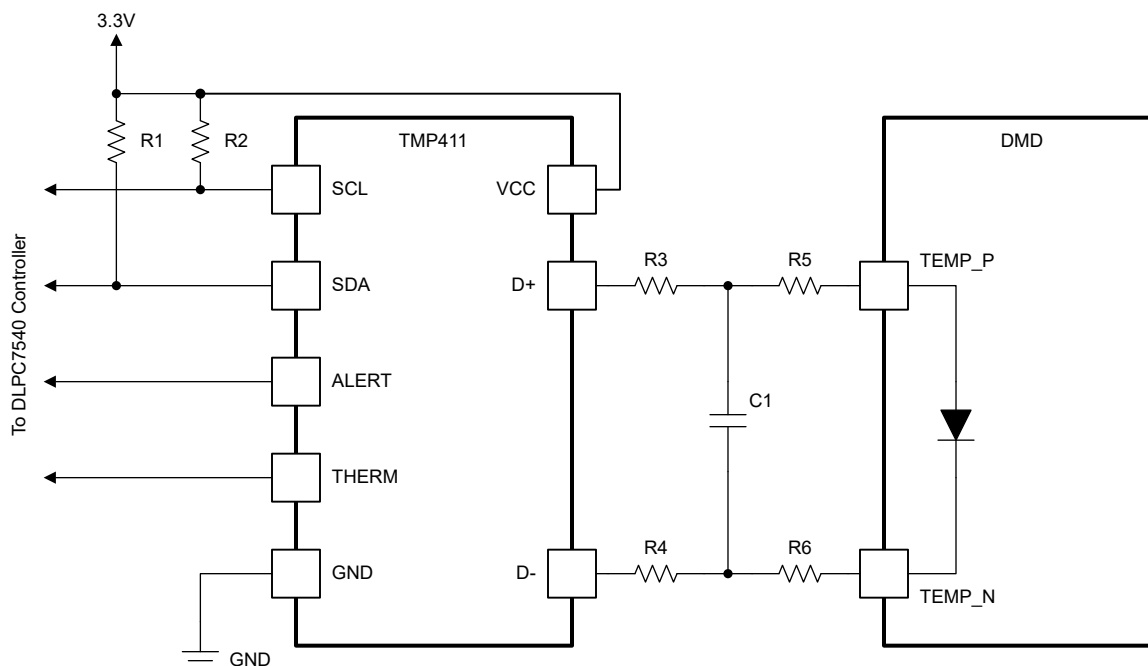

図 7-3. Normalized Light Output vs Normalized Laser Power for Laser Phosphor Illumination

7.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in 図 7-4. The software application contains functions to configure the TMP411 to read the DLP472TE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the TMP411 and the DLPC7540 controller happens over the I^{2}C interface. The TMP411 connects to the DMD via pins outlined in 表 4-1.

If the temp sensor is not used, TEMP_N and TEMP_P pins should be left unconnected (NC).

資料に関するフィードバック (ご意見やお問い合わせ) を送信

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A. Details omitted for clarity.

B. See the TMP411 data sheet for the system board layout recommendation.

C. See the TMP411 data sheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.

D. R5 = 0Ω. R6 = 0Ω. Place 0Ω resistors close to the DMD package pins.

図 7-4. TMP411 Sample Schematic

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

注意

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in 図 8-1.

V_{BIAS}, V_{DD}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.


表 8-1. **Power Supply Sequence Requirements**

SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY1}	Delay requirement	from V_{OFFSET} power up to V_{BIAS} power up	1	2		ms
t_{DELAY2}	Delay requirement	from V_{BIAS} and V_{RESET} powered on and stable to DMD_EN_ARSTZ going high	20			µs
t_{DELAY3}	Delay requirement	from V_{OFFSET}, V_{BIAS}, and V_{RESET} power down to when VDD and VDDA can power down	50			µs

8.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} must always start and settle before V_{OFFSET} plus t_{DELAY1} specified in 表 8-1, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the recommended operating conditions.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the absolute maximum ratings, in the recommended operating conditions, and in 表 8-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} has settled at the operating voltage listed in the recommended operating conditions.

8.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See 表 8-1.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the recommended operating conditions.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the absolute maximum ratings, in the recommended operating conditions, and in 表 8-1.
- During power-down, LVCMOS input pins must be less than specified in the recommended operating conditions.
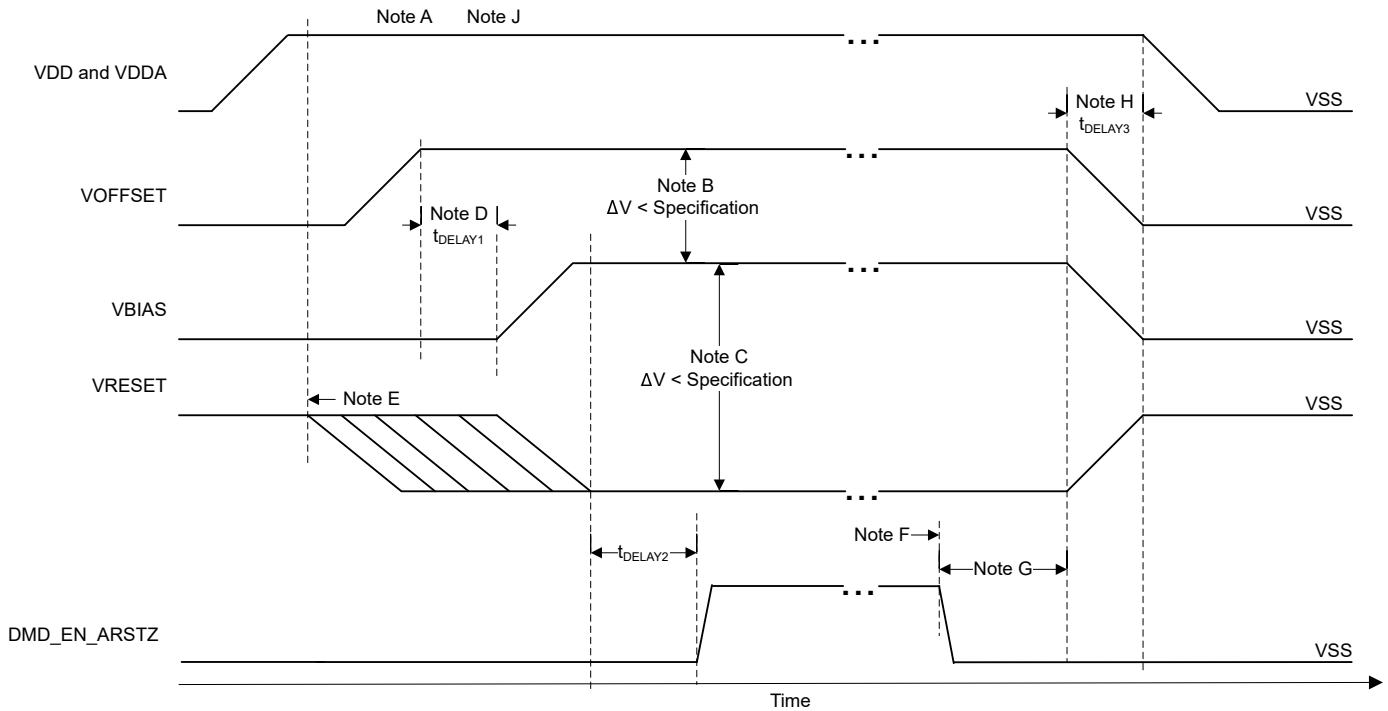
A. See 表 4-1 for pin functions.
B. To prevent excess current, the supply voltage difference $|V_{BIAS} - V_{OFFSET}|$ must be less than the specified limit in the recommended operating conditions.
C. To prevent excess current, the supply difference $|V_{BIAS} - V_{RESET}|$ must be less than the specified limit in the recommended operating conditions.
D. V_{BIAS} must power up after V_{OFFSET} has powered up, per the t_{DELAY1} specification in 表 8-1.
E. V_{RESET}, V_{OFFSET}, V_{BIAS} ramps must start after VDD and BDDA are powered up and stable.
F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET} and V_{OFFSET}.
G. Under power-loss conditions where emergency DMD micromirror park procedures are enacted by the DLP controller hardware, DMD_EN_ARSTZ goes low.
H. V_{DD} must remain high until after V_{OFFSET}, V_{BIAS}, and V_{RESET} go low, per Delay2 specification in the 表 8-1.
I. To prevent excess current, the supply voltage delta $|V_{DDA} - V_{DD}|$ must be less than specified limit in the recommended operating conditions.
J. Not to scale. Details are omitted for clarity.

図 8-1. DMD Power Supply Requirements

9 Layout

9.1 Layout Guidelines

The DLP472TE DMD is part of a chipset that is controlled by the DLPC7540 display controller in conjunction with the TPS65145 PMIC and the DLPA100 power and motor controller. These guidelines are targeted at designing a PCB board with the DLP472TE DMD. The DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic including double data rate 3.2Gbps and 250Mbps differential data buses run to the DMD. TI recommends that full or mini power planes are used for V_{OFFSET}, V_{RESET}, and V_{BIAS}. Solid planes are required for ground (V_{SS}). The target impedance for the PCB is 50Ω ±10% with exceptions listed in 表 9-1. TI recommends a 10-layer stack-up as described in 表 9-2. TI recommends manufacturing the PCB with a high quality FR-4 material.

9.2 Impedance Requirements

TI recommends a target impedance for the PCB of 50Ω ±10% for all signals. The exceptions are listed in 表 9-1.

表 9-1. Special Impedance Requirements

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (ohms)
DMD High-Speed Data Signals	DMD_HSSI0_N_(0…7), DMD_HSSI0_P_(0…7), DMD_HSSI1_N_(0…7), DMD_HSSI1_P_(0…7), DMD_HSSI0_CLK_N, DMD_HSSI0_CLK_P, DMD_HSSI1_CLK_N, DMD_HSSI1_CLK_P	100Ω differential (50Ω single-ended)
DMD Low-Speed Interface Signals	DMD_LS0_WDATA_N, DMD_LS0_WDATA_P, DMD_LS0_CLK_N, DMD_LS0_CLK_P	100Ω differential (50Ω single ended)

9.3 Layers

The layer stack-up and copper weight for each layer is shown in 表 9-2 .

表 9-2. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A – DMD, primary components, power mini-planes	0.5 oz (before plating)	DMD and escapes. Two data input connectors. Top components including power generation and two data input connectors. Low frequency signals routing. Use copper fill (GND) plated up to 1 oz.
2	Ground	0.5	Solid ground plane (net GND) reference for signal layers #1, 3.
3	Signal (High frequency)	0.5	High speed signal layer. High Speed differential data buses from input connector to DMD.
4	Ground	0.5	Solid ground plane (net GND) reference for signal layers #3, #5.
5	Power	0.5	Primary split power planes for 1.8V, 3.3V, 10V, −14V, 18V
6	Power	0.5	Primary split power planes for 1.8V, 3.3V, 10V, −14V, 18V
7	Ground	0.5	Solid ground plane (net GND) Reference for signal layer #8
8	Signal (high frequency)	0.5	High speed signal layer. High speed differential data buses from input connector to DMD.
9	Ground	0.5	Solid ground plane (net GND) Reference for signal layers #8, 10.
10	Side B—Secondary components, power mini-planes	0.5 oz (before plating)	Discrete components if necessary. Low frequency signals routing. Use copper fill plated up to 1 oz.

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9.4 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005"/ 0.015" (Trace-Width/Spacing) design rule. Use an analysis of impedance and stack-up requirements to determine and calculate actual trace widths.

Maximized the width of all voltage signals as space permits. Follow the width and spacing requirements listed in 表 9-3.

表 9-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH (MIL)	MINIMUM TRACE SPACING (MIL)	LAYOUT REQUIREMENT
GND	MAXIMIZE	5	Maximize trace width to connecting pin as a minimum.
V_{DD}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias.
V_{DDA}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias.
V_{OFFSET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{RESET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{BIAS}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.

9.5 Power

TI strongly discourages signal routing on power planes or on planes adjacent to power planes. If signals must be routed on layers adjacent to power planes, they must not cross splits in power planes to prevent EMI and preserve signal integrity.

Connect all internal digital ground (GND) planes in as many places as possible. Connect all internal ground planes with a minimum distance between connections of 0.5". Extra vias may not required if there are sufficient ground vias due to normal ground connections of devices.

Connect power and ground pins of each component to the power and ground planes with at least one via for each pin. Minimize trace lengths for component power and ground pins. (ideally, less than 0.100").

Ground plane slots are strongly discouraged.

9.6 Trace Length Matching Recommendations

表 9-4 and 表 9-5 describe recommended signal trace length matching requirements. Follow these guidelines to avoid routing long traces over large areas of the PCB:

- Match the trace lengths so that longer signals route in a serpentine pattern
- Minimize the number of turns.
- Ensure that the turn angles are no sharper than 45 degrees.

図 9-1 shows an example of the HSSI signal pair routing.

Signals listed in 表 9-4 are specified for the data rate operation at up to 3.2Gbps. Minimize the layer changes for these signals. Minimize the number of vias. Avoid sharp turns and layer switching while minimizing the lengths. When layer changes are necessary, place GND vias around the signal vias to provide a signal return path. The distance from one pair of differential signals to another must be at least two times the distance within the pair.

表 9-4. HSSI High-Speed DMD Data Signals

SIGNAL NAME	REFERENCE SIGNAL	ROUTING SPECIFICATION	UNIT
DMD_HSSI0_N(0...7), DMD_HSSI0_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	±0.25	inch
DMD_HSSI1_N(0...7), DMD_HSSI1_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	±0.25	inch
DMD_HSSI0_CLK_P	DMD_HSSI1_CLK_P	±0.05	inch
Intra-pair P	Intra-pair N	±0.01	inch

表 9-5. Other Timing Critical Signals

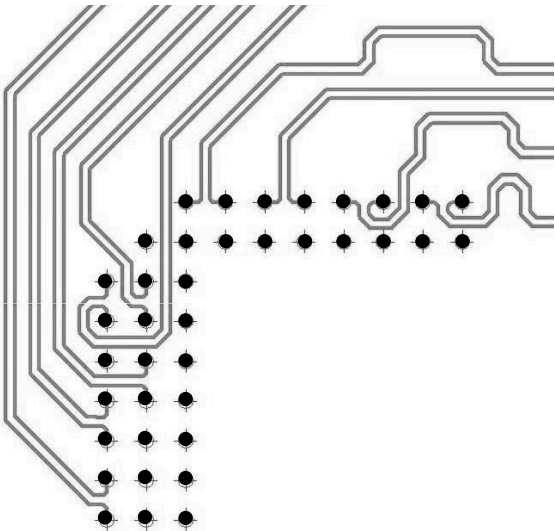| SIGNAL NAME	CONSTRAINTS	ROUTING LAYERS
LS_CLK_P, LS_CLK_N LS_WDATA_P, LS_WDATA_N LS_RDATA_A	Intra-pair (P to N) Matched to 0.01 inches Signal-to-signal Matched to +/- 0.25 inches	Layers 3, 8

図 9-1. Example HSSI PCB Routing

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

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10.2 Device Support
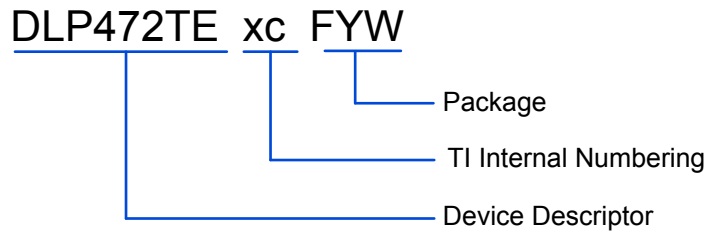
10.2.1 Device Nomenclature

図 10-1. Part Number Description

10.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 10-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:
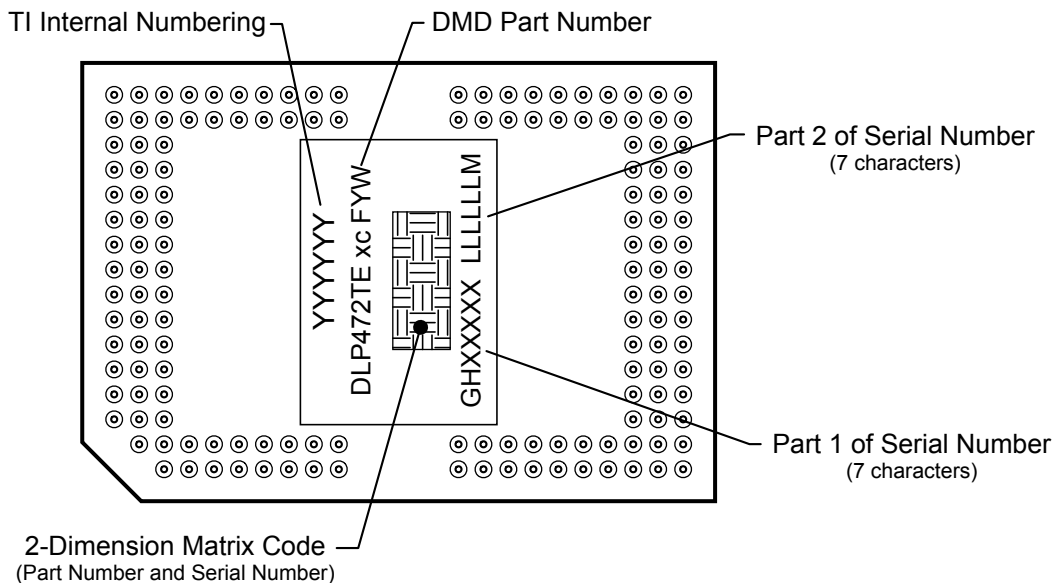
図 10-2. DMD Marking Locations

10.3 Documentation Support

10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

*   Texas Instruments, DLPC7540 High Resolution Controller data sheet
*   Texas Instruments, TPS6514x Triple Output LCD Supply With Linear Regulator and Power Good data sheet
*   Texas Instruments, DLPA100 Power and Motor Driver Data Sheet data sheet

10.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.5 サポート・リソース

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10.8 用語集

テキサス・インスツルメンツ用語集　　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Changed the document status from Advance Information to Production Data

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
DLP472TE0FYW	ACTIVE	CPGA	FYW	149	33	RoHS & Green	Call TI	Call TI		see *Device Marking* section

(1)   The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2)   Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and the leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3)   MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4)   Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5)   There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6)   Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP472TE0FYW	Active	Production	CPGA (FYW) | 149	33 | JEDEC TRAY (5+1)	Yes	NI-PD-AU	N/A for Pkg Type	0 to 70	
DLP472TE0FYW.A	Active	Production	CPGA (FYW) | 149	33 | JEDEC TRAY (5+1)	Yes	NI-PD-AU	N/A for Pkg Type	0 to 70	
DLP472TE0FYW.B	Active	Production	CPGA (FYW) | 149	33 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 70	
XDLP472TE0FYW	Active	Preproduction	CPGA (FYW) | 149	33 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 70	
XDLP472TE0FYW.A	Active	Preproduction	CPGA (FYW) | 149	33 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 70	
XDLP472TE0FYW.B	Active	Preproduction	CPGA (FYW) | 149	33 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY

L - Outer tray length without tabs

KO - Outer tray height

W - Outer tray width

P1 - Tray unit pocket pitch

CW - Measurement for tray edge (Y direction) to corner pocket center

CL - Measurement for tray edge (X direction) to corner pocket center

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP472TE0FYW	FYW	CPGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45
DLP472TE0FYW.A	FYW	CPGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

NOTES UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.

2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.

3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM VALUE OF 0.8 DEGREES.

4. SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE.

5. BOUNDARY MIRRORS SURROUNDING THE ACTIVE ARRAY.

6. MAXIMUM ENCAPSULANT PROFILE SHOWN.

7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULATION SHALL NOT EXCEED 0.2 THICKNESS MAXIMUM.

8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

INCIDENT LIGHT

(Ø2.000)

3.000 ± 0.500

3.000 ± 0.500

22.300 ± 0.220

SEE VIEW E (SHEET 3) FOR WINDOW AND ACTIVE ARRAY DIMENSIONS

1.517 ± 0.150

13.797 ± 0.150

(1.500)

OFF STATE LIGHT

5.046 ± 0.150

17.770 ± 0.150

32.200 ± 0.320

⊥ 0.200 E

SECTION A-A
SCALE 20 : 1

SUBSTRATE

ENCAPSULANT (0.367)

0.800 MAX

WINDOW

WINDOW APERTURE

3 PLACES INDICATED (SHEET 2)

2.950 ± 0.240

149X 1.400 ± 0.100

1.100 ± 0.050

1.407 ± 0.079

1.040 ± 0.080

(0.307)

(Ø0.305)

∥ 0.0254 A
0.020 G

ACTIVE ARRAY

INV2013-DLPa

8 7 6 5 4 3 2 1

D

| A |

28.000 ± 0.280
(DATUM B TO CENTER OF DATUM C SLOT)

25.696 MAX
7

| F |

| A |

2.100 ± 0.150
Ø2.000±0.050 | B |
4

2.300 MIN 7

ENCAPSULANT ALLOWED
ON CERAMIC AREA 7

| A2 |

| E |

2.900

5.150 ± 0.150

6.000

| D |

(Ø2.000) | B |

0.500 MIN

1.865 ± 0.130

SECTION C-C
DATUM B
SCALE 16 : 1

12.000 ± 0.120

14.900

23.2° ± 1°

| A1 |

3X Ø4.000

WINDOW

| D |

| D |

| C |
4

1.000 ± 0.100

0.500 ± 0.050

| A3 |

1.500 ± 0.050

0.750 ± 0.025

2X 28.000
(DATUM B TO A2 AND A3)

(1.500) | C |

0.500 MIN

1.865 ± 0.130

SECTION D-D
DATUM C
(VIEW ROTATED FOR CLARITY)
SCALE 16 : 1

VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 10 : 1

INV2013-DLPa

(2.100)

3 8.816 ± 0.076

3 (10.3680)
ACTIVE ARRAY

(Ø2.000) B F

5 2X (0.108)

E

(5.150)

1.057 ± 0.0885

3 3.684 ± 0.076

2.562 ± 0.050

3 (5.8320)
ACTIVE ARRAY

(7.745)
WINDOW APERTURE

(10.036)
WINDOW

6.688 ± 0.0885

7.474 ± 0.050

5 2X 0.108

C

(1.500)

1.208 ± 0.0885

11.288 ± 0.0885

(12.496)
WINDOW APERTURE

1.970 +0.0500 / -0.0885

12.200 +0.0500 / -0.0885

(14.170)
WINDOW

VIEW E
ACTIVE ARRAY AND WINDOW
SCALE 12 : 1

INV2013-DLPa

D

C

B

A

A | D

G

19.145

9 X 1.270 = 11.430 | 9 X 1.270 = 11.430 | 1.625

F

8

(A1, A2, & B1 OMITTED)

1.625 E

20 19 18 17 16 15 14 13 12 11   10 9 8 7 6 5 4 3 2 1

3.895 ± 0.250

A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
T

14.510 ± 0.250

15 X 1.270 = 19.050

149X Ø0.305 $^{+0.050}_{-0.025}$ PINS

⌖ | Ø0.500 | D | E | F
   | Ø0.250 | D

8

8   10.000 ± 0.250 | 11.100 ± 0.250

SYMBOLIZATION PAD 4 | 8
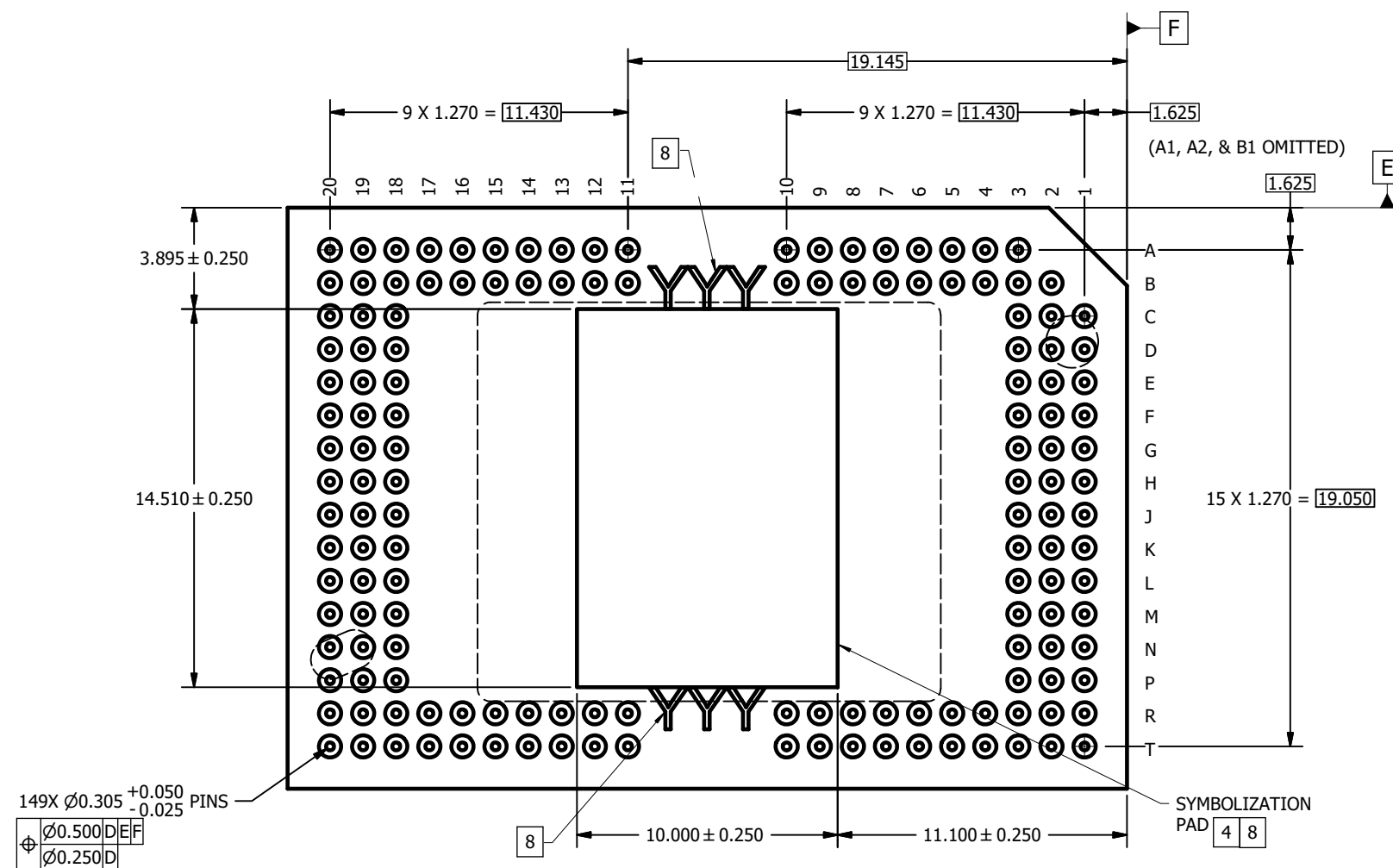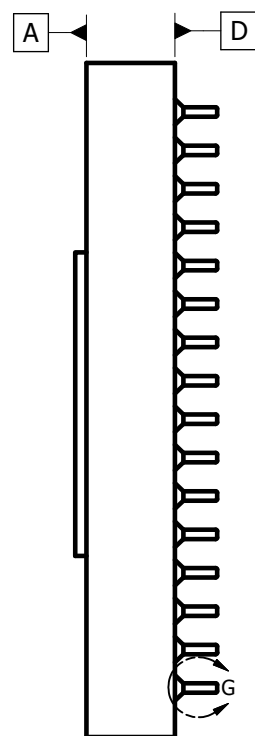
VIEW F
PINS AND SYMBOLIZATION PAD
SCALE 8 : 1

0.280 MAX
(BRAZE AREA)

Ø0.850 MAX
(BRAZE AREA)

(R0.050)

(Ø0.305)

(1.400)

D
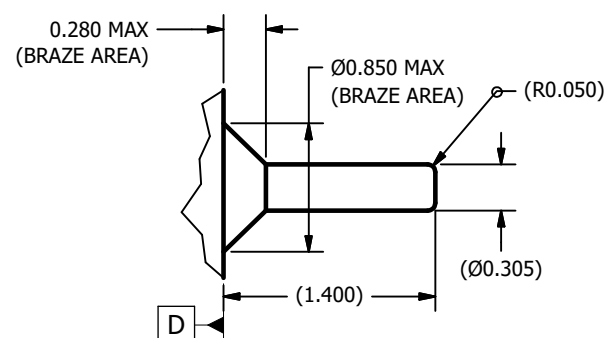
DETAIL G
PIN AND BRAZE DIMENSIONS
149 PLACES
SCALE 40 : 1

INV2013-DLPa