DLP2021-Q1 0.2 インチ、16:9 デジタル・マイクロミラー・デバイス

1 特長

- 車載アプリケーション向け認定済み
  - DMD アレイ温度範囲は -40℃～105℃
- 対角 0.2 インチのマイクロミラー・アレイ
  - マイクロミラー・ピッチ：7.6µm
  - マイクロミラー傾斜角：±12° (フラット状態に対して)
  - 側面照明によるシステム・サイズの低減
- 16:9 (588 × 330) の入力分解能
- 偏光無依存の空間光変調器
- LED またはレーザー光源と互換
- 低い消費電力：±260mW (最大値)
- 気密パッケージ
- 80MHz のダブル・データ・レート (DDR) デジタル・マイクロミラー・デバイス (DMD) インターフェイス

2 アプリケーション

- ダイナミック・グラウンド・プロジェクション
- 車内および車外の車両映像投影

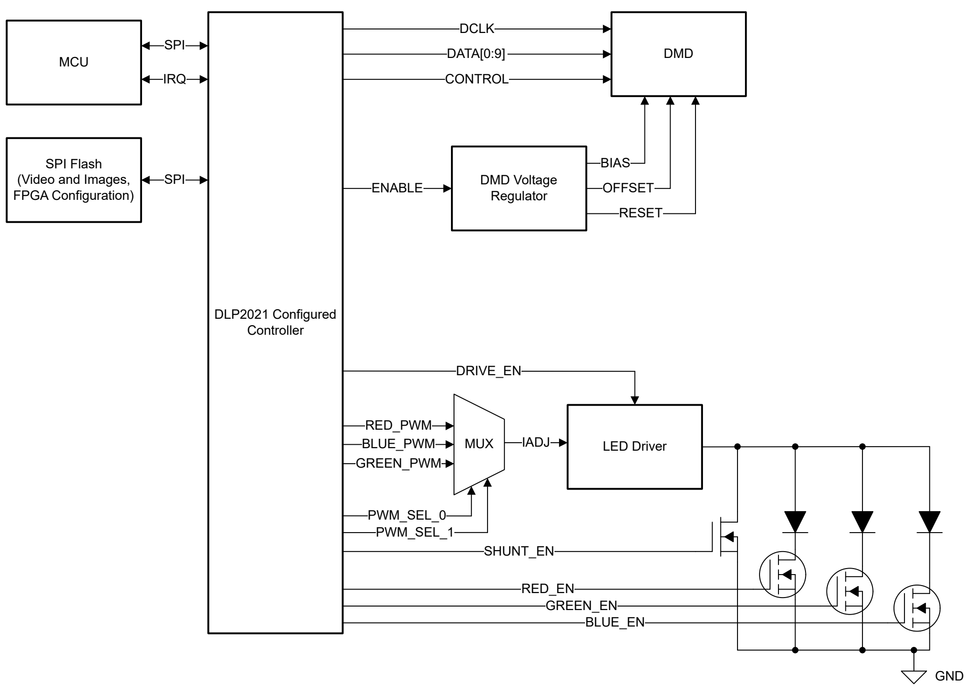
3 概要

DLP2021-Q1 車載用デジタル・マイクロミラー・デバイス (DMD) は、車載用の車外照明制御およびディスプレイ・アプリケーション向けに設計されています。アプリケーションには、フルカラー、アニメーション、動的コンテンツを表示するグラウンド・プロジェクションが含まれます。グラウンド・プロジェクションにより、バック警告やドア開警告などの車両と歩行者 (V2P) との通信が容易になるとともに、車両の通信システムや車両のパーソナライズ・オプションを制御できます。DLP2021-Q1 チップセット搭載のプロジェクタは、小型で低消費電力動作が可能であり、さまざまなプロジェクション・アプリケーションをサポートします。サイド・ミラー、ドア・パネル、テール・ライト、フロント・グリルなどを含め、車両内のさまざまな場所に配置できます。

製品情報

部品番号 (1)	パッケージ	本体サイズ (公称)
DLP2021-Q1	FQU (64)	8.55mm × 16.80mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



DLP2021-Q1 のシステム・ブロック図

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4 概要 (続き)

このチップセットは、LED またはレーザーとの組み合わせにより、125% を超える NTSC (National Television System Committee) 色域の飽和度の高い色を作成でき、RGB または白色の光源で使用できます。DLP2021-Q1 の FPGA (フィールド・プログラマブル・ゲート・アレイ) 構成は、DLP2021-Q1 車載用 DMD を駆動するために使用されています。このコントローラ・アーキテクチャは、小型のプロジェクタ用に設計されており、コンテンツ作成にビデオ・バスまたはグラフィックス処理ユニット (GPU) は不要です。ビデオおよび画像コンテンツは、ローカル・フラッシュに保存され、電源投入時またはコマンド実行時に再生できます。

5 Pin Configuration and Functions

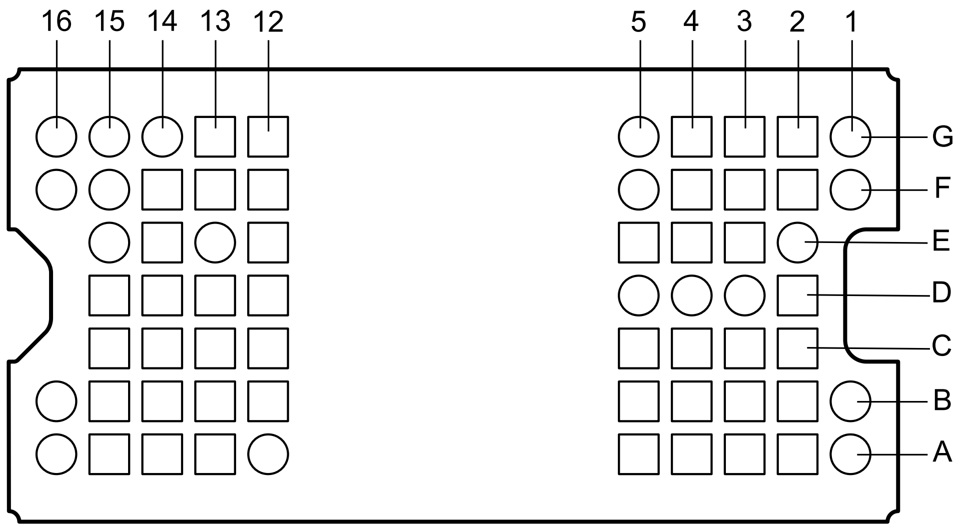


図 5-1. FQU Package 64-Pin LGA Bottom View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
DATA(0)	A2	LVCMOS input	Data bus. Synchronous to rising edge and falling edge of DCLK
DATA(1)	A4		
DATA(2)	B2		
DATA(3)	B3		
DATA(4)	B5		
DATA(5)	C2		
DATA(6)	C3		
DATA(7)	B4		
DATA(8)	C5		
DATA(9)	D2		
DCLK	F4		Data clock
LOADB	F3		Parallel latch load enable. Synchronous to rising edge and falling edge of DCLK
SCTRL	E4		Serial control (sync). Synchronous to rising edge and falling edge of DCLK
TRC	F2		Toggle rate control. Synchronous to rising edge and falling edge of DCLK
DAD_BUS	B15		Reset control serial bus. Synchronous to rising edge of SAC_CLK
RESET_OEZ	C15		Active low. Output enable signal for internal reset driver circuitry
RESET_STROBE	B13		Rising edge on RESET_STROBE latches in the control signals
SAC_BUS	A15		Stepped address control serial bus. Synchronous to rising edge of SAC_CLK
SAC_CLK	A14		Stepped address control clock
TEMP_MINUS	G13	Analog input	Calibrated temperature diode used to assist accurate temperature measurements of DMD die
TEMP_PLUS	G2		
V_{BIAS}	D15	Power	Power supply for positive bias level of mirror reset signal
V_{CC}	A5, B12, C14, D12, F13, G3		Power supply for low voltage CMOS logic. Power supply for normal high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal during power down
V_{OFFSET}	E14		Power supply for high voltage CMOS logic. Power supply for stepped high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal
V_{RESET}	D14		Power supply for negative reset level of mirror reset signal
V_{SS}	A3, A13, B14, C4, C12, C13, D13, E3, E5, E12, F12, F14, G4, G12		Common return for all power
RESERVED	A1, A12, A16,B1, B16, D3, D4, D5, E2, E13,E15, F1, F5, F15, F16, G1, G5, G14, G15, G16	Reserved	Do not connect.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE					
V_{DD}	LVCMOS logic supply voltage	–0.5		2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode	–0.5		8.75	V
V_{BIAS}	Supply voltage for micromirror electrode	–0.5		17	V
V_{RESET}	Supply voltage for micromirror electrode	–11		0.5	V
$\| V_{BIAS}–V_{OFFSET} \|$	Supply voltage delta (absolute value)			8.75	V
$\| V_{BIAS}–V_{RESET} \|$	Supply voltage delta (absolute value)			28	V
INPUT VOLTAGE					
Input voltage for LVCMOS Pins		–0.5		V_{DD} + 0.5	V
TEMPERATURE DIODE					
I_{TEMP_DIODE}	Max current source into temperature diode			500	µA
ENVIRONMENTAL					
T_{ARRAY}	Operating DMD array temperature	–40		105	°C
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in Illumination Overfill Diagram			50	mW/mm²

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	–40	125	°C

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.7	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode	8.25	8.5	8.75	V
V_{BIAS}	Supply voltage for mirror electrode	15.5	16	16.5	V
V_{RESET}	Supply voltage for micromirror electrode	–9.5	–10	–10.5	V
$\| V_{BIAS}–V_{OFFSET} \|$	Supply voltage delta (absolute value)			8.75	V
$\| V_{BIAS}–V_{FRESET} \|$	Supply voltage delta (absolute value)			28	V
LVCMOS Buffers					

6.4 Recommended Operating Conditions (続き)

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	NOM	MAX	UNIT
V_{IH}	Positive going threshold voltage	0.7		VDD+0.3	x V_{DD}
V_{IL}	Negative going threshold voltage	–0.3		0.3	x V_{DD}
CLOCK FREQUENCY					
f_{max}	Clock frequency for high speed interface SAC_CLK	20	76.2	80	MHz
DCD_{IN}	Duty Cycle Distortion tolerance SAC_CLK	30%		70%	
f_{max}	Clock frequency for high speed interface DCLK	20	76.2	80	MHz
DCD_{IN}	Duty Cycle Distortion tolerance DCLK	30%		70%	
TEMPERATURE DIODE					
I_{TEMP_DIODE}	Max current source into temperature diode			120	µA
ENVIRONMENTAL					
T_{ARRAY}	Operating DMD array temperature[3]	–40		105	°C
ILL_{UV}	Illumination, wavelength < 395 nm [2]			2	mW/cm ^{2}
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in Illumination Overfill Diagram			40	mW/mm ^{2}

(1) *Recommended Operating Conditions* are applicable after the DMD is installed in the final product.
(2) The maximum operation conditions for operating temperature and UV illumination shall not be implemented simultaneously.
(3) Operating profile information for device micromirror landed duty-cycle and temperature may be provided if requested.

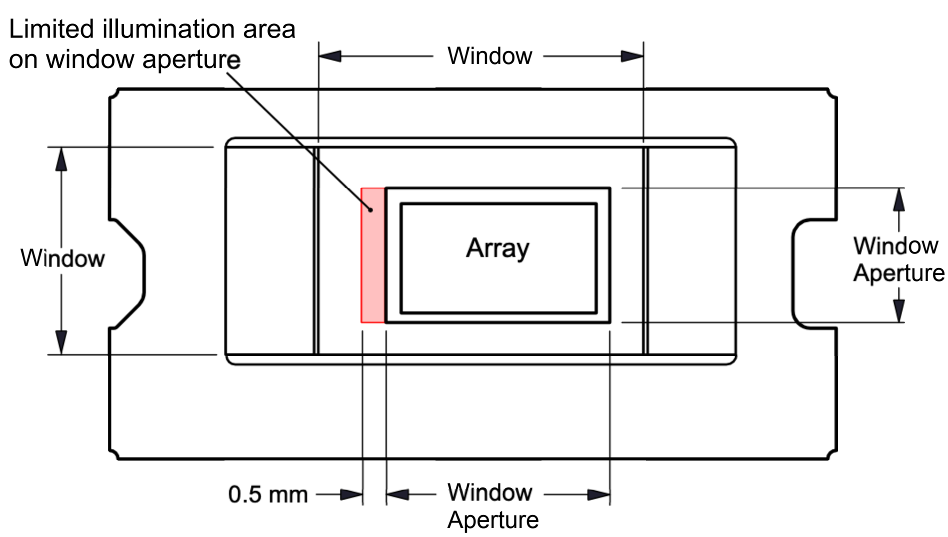


図 6-1. Illumination Overfill Diagram

6.5 Thermal Information

THERMAL METRIC		VALUE	UNIT
Thermal resistance	Active area-to-test point 1 (TP1) [1]	5	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the Recommended Operating Conditions. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD}	V_{DD} = 1.95 V			30	mA
I_{OFFSET}	Supply current: V_{OFFSET}	V_{OFFSET} = 8.75 V			15	mA
I_{BIAS}	Supply current: V_{BIAS}	V_{BIAS} = 16.5 V			2.3	mA
I_{RESET}	Supply current: V_{RESET}	V_{RESET} = –10.5 V			3.3	mA
POWER						
P_{DD}	Supply power dissipation: V_{DD}	V_{DD} = 1.95 V			60	mW
P_{OFFSET}	Supply power dissipation: V_{OFFSET}	V_{OFFSET} = 8.75 V			132	mW
P_{BIAS}	Supply power dissipation: V_{BIAS}	V_{BIAS} = 16.5 V			38	mW
P_{RESET}	Supply power dissipation: V_{RESET}	V_{RESET} = –10.5 V			30	mW
P_{TOTAL}	Supply power dissipation: Total				260	mW
LVCMOS Buffers						
V_{OH}	High level output voltage	I_{OH} = –2 mA	0.8 × V_{DD}			V
V_{OL}	Low level output voltage	I_{OH} = 2 mA			0.2 × V_{DD}	V
I_{IL}	Low level input current(2)	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High level output current(2)	VDD = 1.95 V; V_I = 1.95 V			135	uA
I_{IL2}	Low level input current(3)	V_{DD} = 0.0 V	–5			uA
I_{IH2}	High level output current(3)	V_{DD} = 1.95 V			785	uA
CAPACITANCE						
C_{IN}	Input capacitance	f = 1 MHz			10	pF
C_{OUT}	Output capacitance	f = 1 MHz			15	pF
C_{TEMP}	Temperature sense diode capacitance	f = 1 MHz			25	pF

(1) Device electrical characteristics are over Recommended Operating Conditions unless otherwise noted.
(2) Specification is for LVCMOS input pins which do not have pull up or pull down resistors.
(3) Specification is for LVCMOS input pins which do have pull down resistors.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

		MIN	NOM	MAX	UNIT
DMD MIRROR AND SRAM CONTROL LOGIC SIGNALS					
t_{su}	Setup time SAC_BUS low before SAC_CLK ↑	1			ns
t_h	Hold time SAC_BUS low after SAC_CLK ↑	1			ns
t_{su}	Setup time DAD_BUS high before SAC_CLK ↑	1			ns
t_h	Hold time DAD_BUS high after SAC_CLK ↑	1			ns
DMD DATA PATH AND LOGIC CONTROL SIGNALS					
t_{su}	Setup time DATA(9:0) before DCLK ↑ or DCLK ↓	1.0			ns
t_h	Hold time DATA(9:0) after DCLK ↑ or DCLK ↓	1.0			ns
t_{su}	Setup time SCTRL before DCLK ↑ or DCLK ↓	1.0			ns
t_h	Hold time SCTRL after DCLK ↑ or DCLK ↓	1.0			ns
t_{su}	Setup time TRC before DCLK ↑ or DCLK ↓	1.0			ns
t_h	Hold time TRC after DCLK ↑ or DCLK ↓	1.0			ns
t_{su}	Setup time LOADB low before DCLK ↑ or DCLK ↓	1.0			ns

6.7 Timing Requirements (続き)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

		MIN	NOM	MAX	UNIT
t_h	Hold time LOADB low after DCLK↑ or DCLK↓	1.0			ns
t_{su}	Setup time RESET_STROBE high before DCLK ↑ or DCLK↓	1.5			ns
t_h	Hold time RESET_STROBE high after DCLK↑ or DCLK↓	1.5			ns
t_w	Pulse width 50% to 50% reference points: DCLK high or low	5			ns
t_w	pulse width 50% to 50% reference points: LOADB low	7			ns
t_w	pulse width 50% to 50% reference points: RESET_STROBE high	7			ns
t_r	Rise time 20% to 80% reference points: DCLK, DATA, SCTRL, TRC, LOADB,SAC_CLK			2.5	ns
t_f	Fall time 80% to 20% reference points: DCLK, DATA, SCTRL, TRC, LOADB,SAC_CLK			2.5	ns

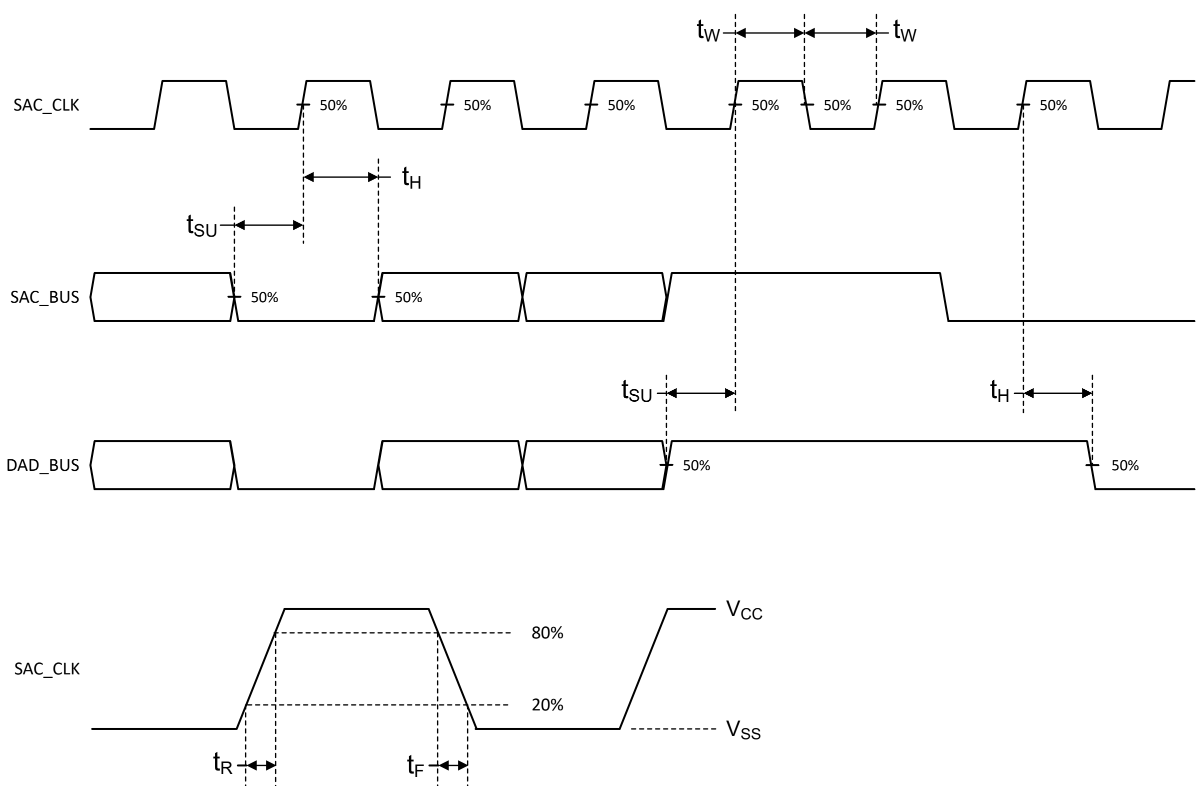


図 6-2. DMD Mirror and SRAM Control Logic Timing Requirements

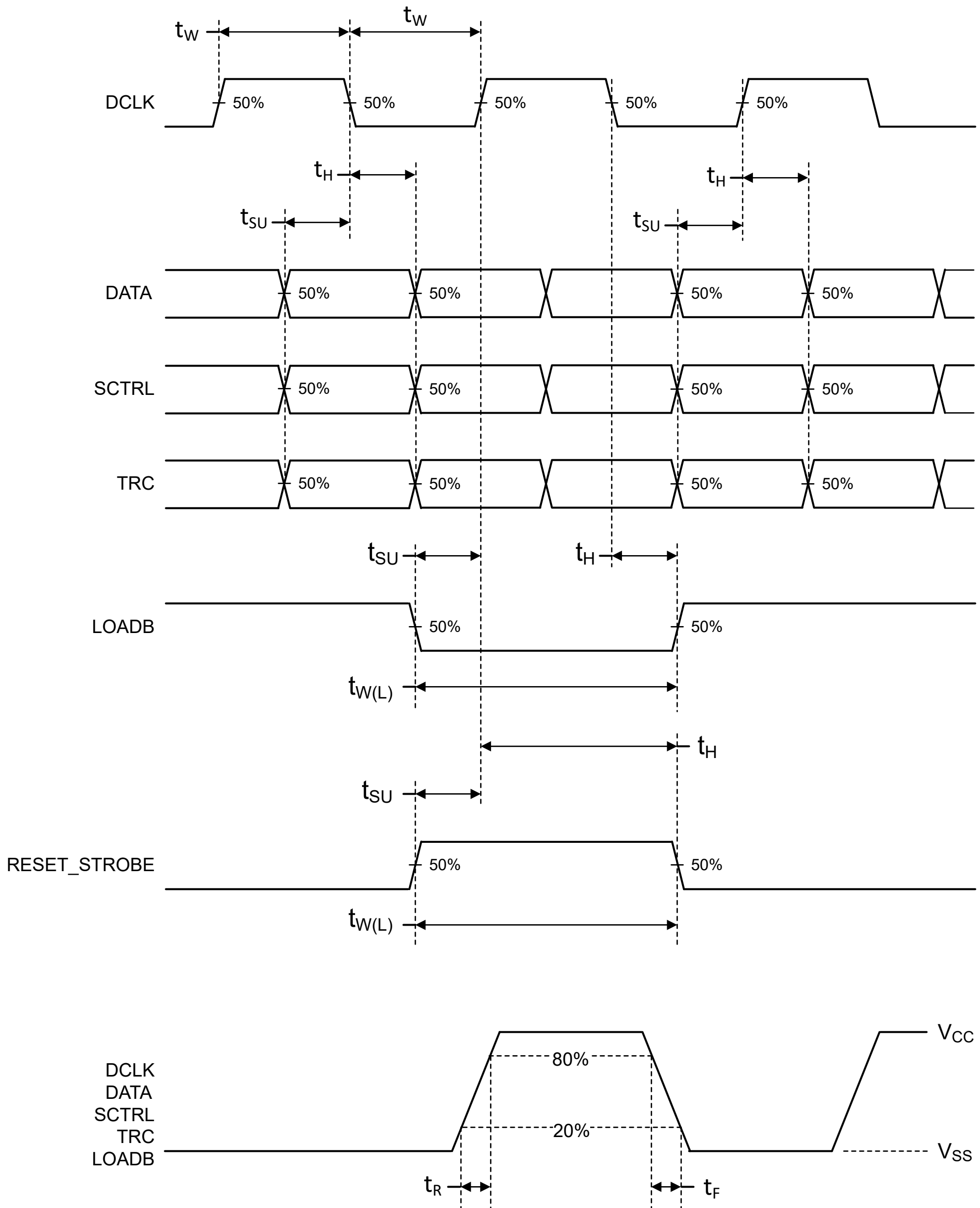


図 6-3. DMD Data Path and Control Logic Timing Requirements

6.8 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Thermal Interface Area	Uniformly distributed within the Thermal Interface Area shown in 図 6-4			70	N
Electrical Interface Area	Uniformly distributed within the Electrical Interface Area shown in 図 6-4			100	N

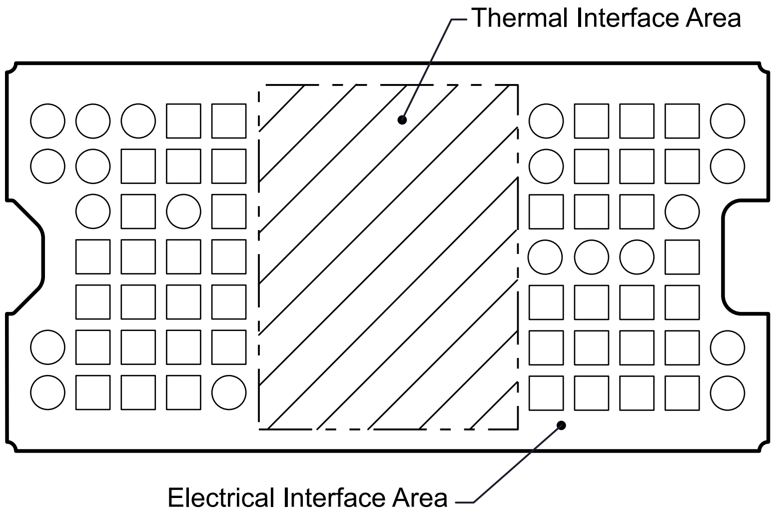


図 6-4. System Interface Loads

6.9 Micromirror Array Physical Characteristics

PARAMETER			VALUE	UNIT
M	Number of active columns(1)		416	micromirrors
N	Number of active rows(1)		468	micromirrors
ε	Micromirror Pitch (diagonal)(2)		7.6	µm
P	Micromirror Pitch (horizontal and vertical)(2)		10.8	µm
	Micromirror active array width	(P × M) + (P / 2)	4.498	mm
	Micromirror active array height	(P × N) / 2 + (P / 2)	2.533	mm
	Micromirror active border	Pond of micromirrors (POM) (3)	10	micromirrors/side

(1) See Array Physical Characteristics.
(2) See Pixel Pitch.
(3) The structure and qualities of the border around the active array include a band of partially functional micromirrors called the POM. These micromirrors are structurally and electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

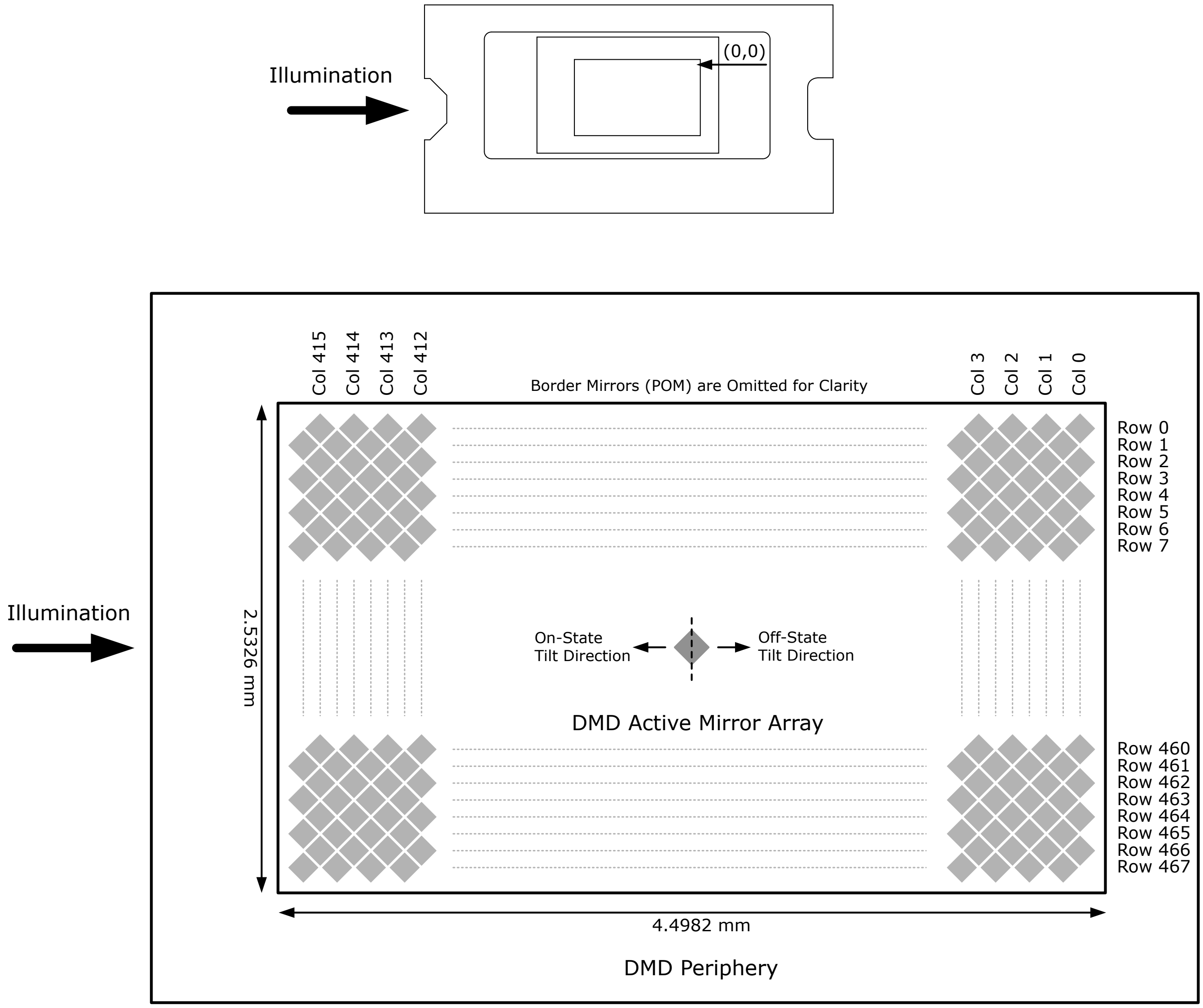


図 6-5. Micromirror Array Physical Characteristics

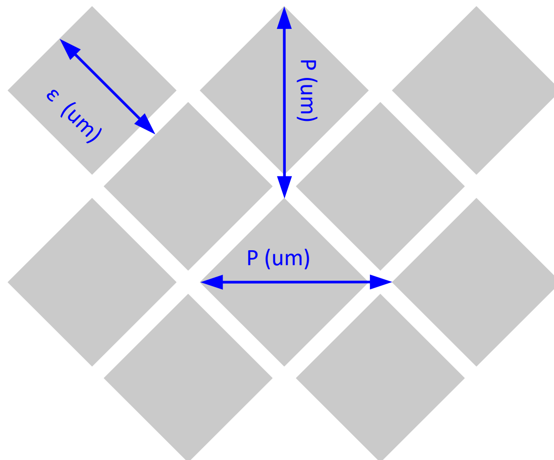


図 6-6. Mirror (Pixel) Pitch

6.10 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)	11	12	13	degree
DMD efficiency(2)	420 nm – 700 nm		66%		

(1) Measured relative to the plane formed by the overall micromirror array at 25°C
(2) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic micromirror landed duty-cycle and do not include system optical efficiency or overfill loss. This number is measured under conditions described above and deviations from these specified conditions could result in a different efficiency value in a different optical system. The factors that can influence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. DLPA083A describes the interaction of these system factors, as well as the DMD efficiency factors that are not system dependent.

6.11 Window Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture (1)				See (1)	

(1) See the mechanical package ICD for details regarding the size and location of the window aperture.

6.12 Chipset Component Usage Specification

The DLP2021-Q1 DMD is a component of a Texas Instruments DLP® chipset including a DLP products controller. Reliable function and operation of the DMD requires that it be used in conjunction with a DLP products controller.

注

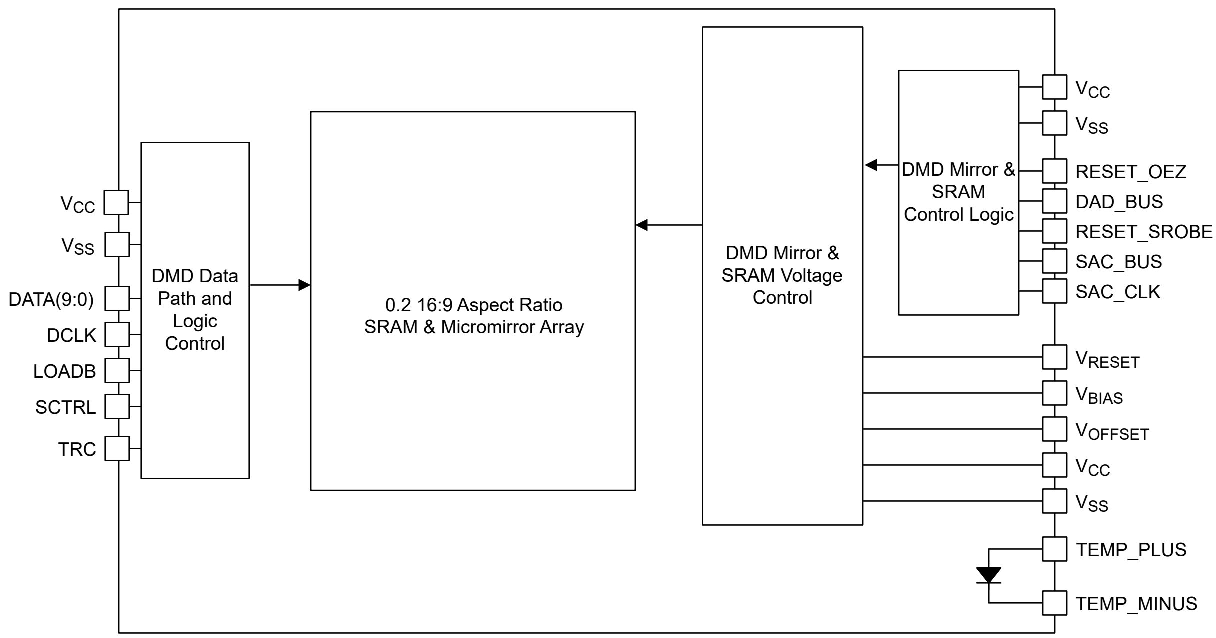
TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7 Detailed Description

7.1 Overview

The DLP2021-Q1 DMD has a resolution of 416 × 468 mirrors configured in a diamond format that results in an aspect ratio of 16:9 which creates an effective resolution of 588 × 330 square pixels. By configuring the pixels in a diamond format, the illumination input to the DMD enters from the side allowing for smaller mechanical packaging of the optical system.

7.2 Functional Block Diagram



7.3 Feature Description

To ensure reliable operation, the DLP2021-Q1 DMD must be used with a DLP products controller.

7.3.1 Micromirror Array

The DLP2021-Q1 DMD consists of a two-dimensional array of 1-bit CMOS memory cells that determine the state of the each of the 416 × 468 micromirrors in the array. Refer to セクション 6.9 section for a calculation of how the 416 × 468 micromirror array represents a 16:9 dimensional aspect ratio to the user. Each micromirror is either ON (tilted +12°) or OFF (tilted –12°). Combined with appropriate projection optical system the DMD can be used to create sharp, colorful, and vivid digital images.

7.3.2 Double Data Rate (DDR) Interface

Each DMD micromirror and its associated SRAM memory cell is loaded with data from the DLP controller via the DDR interface (DATA(9:0), DCLK, LOADB, SCRTL, and TRC). These signals are low voltage CMOS nominally operating at 1.8-V level to reduce power and switching noise. This high speed data input to the DMD allows for a maximum update rate of the entire micromirror array to be nearly 5 kHz, enabling the creation of seamless digital images using Pulse Width Modulation (PWM).

7.3.3 Micromirror Switching Control

Once data is loaded onto the DMD, the mirrors switch position (+12° or –12°) based on the timing signal sent to the DMD Mirror and SRAM control logic. The DMD mirrors will be switched from OFF to ON or ON to OFF, or stay in the same position based on control signals DAD_BUS, RESET_STROBE, SAC_BUS, and SAC_CLK, which are coordinated with the data loading by the DLP controller. In general, the DLP controller loads the DMD SRAM memory cells over the DDR interface, and then commands to the micromirrors to switch position.

At power down, the DMD Mirrors are commanded by the DLP controller to move to a near flat (0°) position as shown in セクション 9. The flat state position of the DMD mirrors are referred to as the “Parked” state. To maintain long-term DMD reliability, the DMD must be properly “Parked” prior to every power down of the DMD power supplies.

7.3.4 DMD Voltage Supplies

The micromirrors switching requires unique voltage levels to control the mechanical switching. These voltages levels are nominally 16 V, 8.5 V, and –10 V (V_{BIAS}, V_{OFFSET}, and V_{RESET}). The specification values for V_{BIAS}, V_{OFFSET}, and V_{RESET} are shown in セクション 6.4.

7.3.5 Logic Reset

Reset of the DMD is required and controlled by the DLP products controller.

7.3.6 Temperature Sensing Diode

The DMD includes a temperature sensing diode designed to be used with the TMP411-Q1 or equivalent temperature monitoring device.

図 7-1 shows the typical connection between the DLP products controller, TMP411-Q1, and the DLP2021-Q1 DMD. The signals to the temperature sense diode are sensitive to system noise, and care should be taken in the routing and implementation of this circuit. See the *TMP411-Q1 Data Sheet* for detailed PCB layout recommendations.

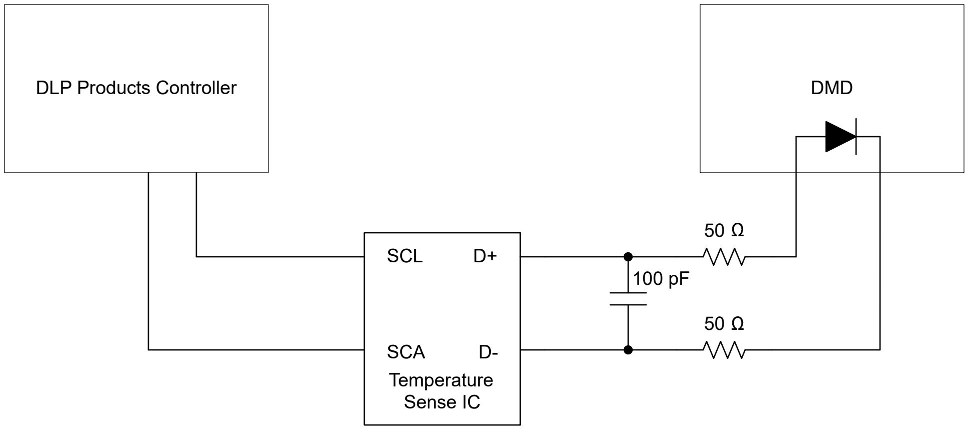


図 7-1. Temperature Sense Diode Typical Circuit Configuration

It is recommended that the host controller manage parking of the DMD based on the allowable temperature specifications and temperature measurements.

7.3.6.1 Temperature Sense Diode Theory

A temperature sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Two different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in the base-emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the *TMP411-Q1 Data Sheet* for detailed information about temperature diode theory and measurement. 図 7-2 and 図 7-3 illustrate the relationship between the current and voltage through the diode.

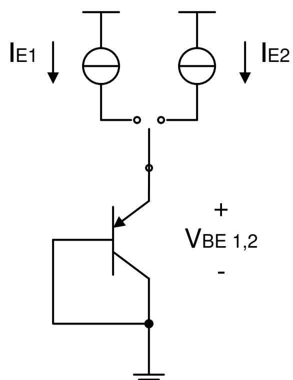


図 7-2. Temperature Measurement Theory

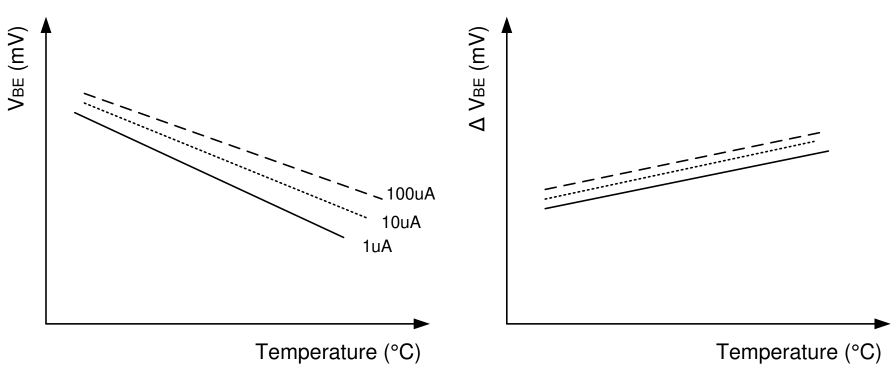


図 7-3. Example of Delta VBE vs. Temperature

7.4 System Optical Considerations

Optimizing system optical performance and image performance strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.4.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block flat-state and stray light from passing through the projection lens. The mirror tilt angle defines DMD capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, contrast ratio can be reduced and objectionable artifacts in the image border and/or active area could occur.

7.4.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the image border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.4.3 Illumination Overfill and Alignment

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. The illumination optical system should be designed to minimize light flux incident outside the active array and on the window aperture. Depending on the particular system’s optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible. Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Refer to セクション 6.4 for a specification on this maximum allowable heat load due to illumination overfill.

7.5 DMD Image Performance Specification

PARAMETER		MIN	NOM	MAX	UNIT
Number of non-operational micromirrors[1]	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	
Optical performance		See セクション 7.4 .			

(1) A non-operational micromirror is defined as a micromirror that is unable to transition between the on-state and off-state positions.

7.6 Micromirror Array Temperature Calculation

Active array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load.

Relationship between array temperature and the reference ceramic temperature (thermocouple location TP1 in 図 7-4) is provided by the following equations.

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

where

- T_{ARRAY} = computed DMD array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (TP1 location in 図 7-4) (°C)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = DMD package thermal resistance from array to TP1 (°C/watt) (see セクション 6.5)
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (watts)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (watts)
- $Q_{ILLUMINATION}$ = ($C_{L2W} \times S_L$)
- C_{L2W} = conversion constant for screen lumens to power on the DMD (watts/lumen)
- S_L = measured screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies.

Absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source.

Equations shown previous are valid for a 1-chip DMD system with total projection efficiency from DMD to the screen of 87%.

The constant C_{L2W} is based on the DMD array characteristics. It assumes a spectral efficiency of 300 lumens/watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

Sample calculation:

- S_L = 50 lm
- C_{L2W} = 0.00293 W/lm
- $Q_{ELECTRICAL}$ = 0.105 W
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = 5°C/W
- $T_{CERAMIC}$ = 55°C

$$Q_{ARRAY} = 0.105\ W + (0.00293 \times 50\ lm) = 0.252\ W \quad (3)$$

$$T_{ARRAY} = 55°C + (0.252\ W \times 5°C/W) = 56.26°C \quad (4)$$

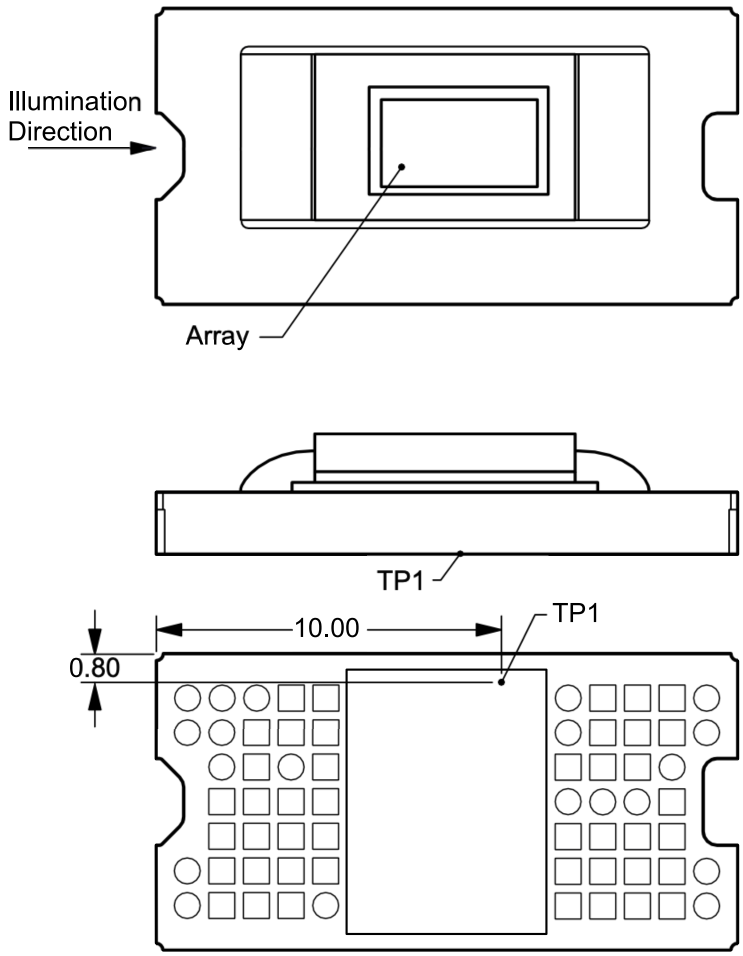


図 7-4. Thermocouple Location

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, assuming a fully saturated white pixel, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The DLP2021-Q1 DMD was designed to be used in automotive applications such as dynamic ground projection. The information shown in this section describes the dynamic ground projection application.

8.2 Typical Application

The DLP2021-Q1 DMD combined with a DLP products controller are the primary devices that make up the reference design for a dynamic ground projection system as shown in the block diagram 図 8-1.

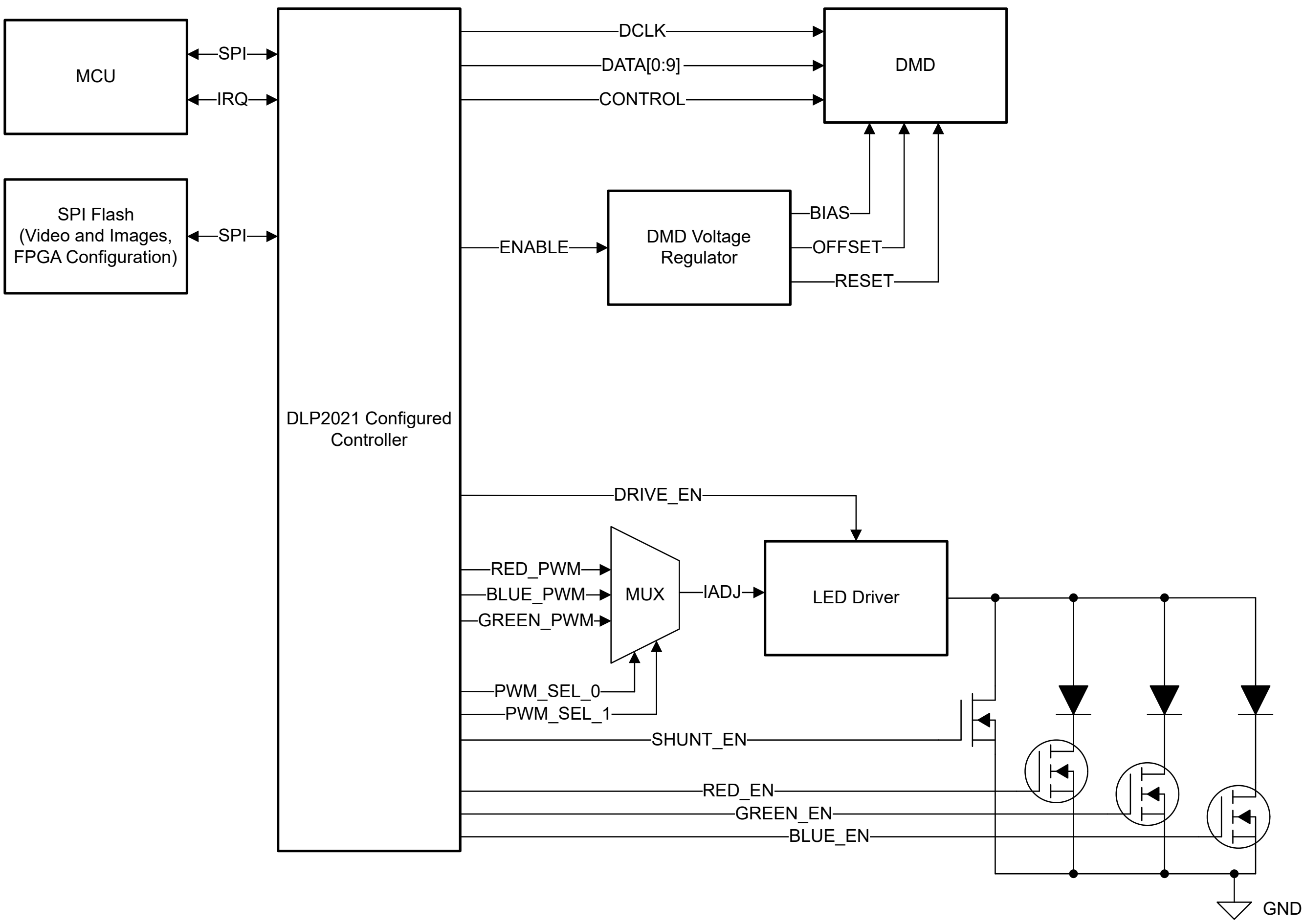


図 8-1. Dynamic Ground Projection System Block Diagram

In this architecture, video content is compressed and stored in external flash memory. Low speed SPI commands are sent from a microcontroller or other processor to the DLP products controller to indicate what video content to read from external memory. Storing the video content in memory removes the need for a high speed video interface to the module which improves compatibility with typical vehicle infrastructures. It also decreases overall system size and cost by removing graphics generation and interfaces. The controller decompresses each bit plane of the video data (416 × 468 resolution) and displays them on the DMD in rapid succession to create the full video image. Due to the diamond format of the DMD pixels, the output image has an effective resolution of 588 × 330. The controller synchronizes the DMD bit plane data with the RGB enable timing for the LED color controller and driver circuit.

The controller may connect to a TMP411-Q1 to measure the DLP2021-Q1 temperature using the built-in temperature sensing diode.

The controller combined with the DLP2021-Q1 may be used in RGB LED or laser illumination systems, or in single-color systems as shown in 図 8-2.

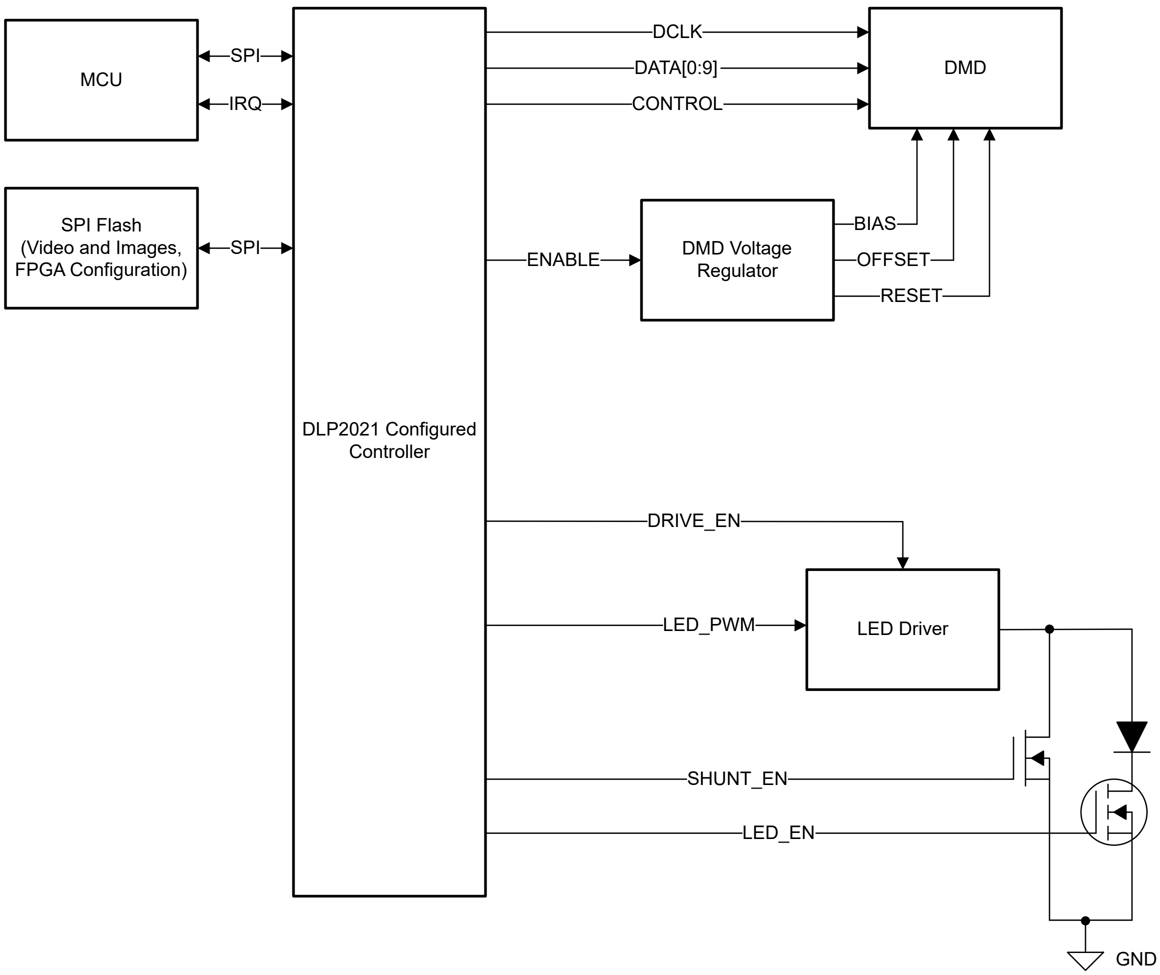


図 8-2. Dynamic Ground Projection System Block Diagram - Single Color

8.3 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles, or number of operating hours at different temperatures. To assist in evaluation, the automotive DMD reliability lifetime estimates Application Report may be provided. See the TI Application team for more information.

9 Power Supply Recommendations

9.1 Power Supply Sequencing Requirements

- V_{BIAS}, V_{CC}, V_{OFFSET}, V_{RESET}, V_{SS} are required to operate the DMD.

> 注意
>
> - For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power up and power down procedures may affect device reliability.
> - The V_{CC}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power up and power down operations. Failure to meet any of the following requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to 図 9-1. V_{SS} must also be connected.

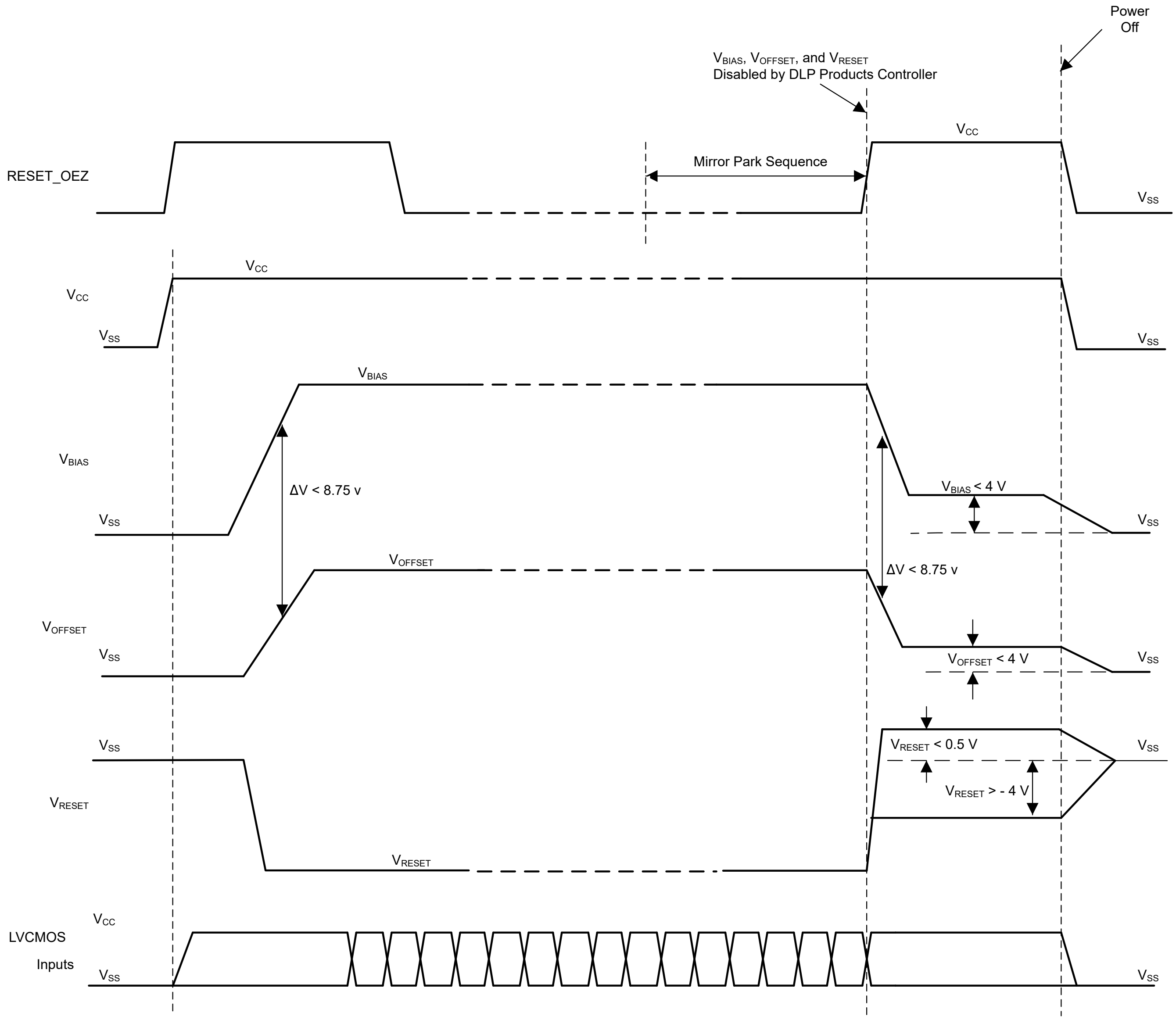
DMD Power Supply Power Up Procedure:

- During power up, V_{CC} must always start and settle before V_{OFFSET}, V_{BIAS} and V_{RESET} voltages are applied to the DMD.
- During power up, V_{BIAS} does not have to start after V_{OFFSET}. However, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ±8.75 V (refer to Note 1 for 図 9-1).
- During power up, the DMD's LVCMOS input pins shall not be driven high until after V_{CC} has settled at operating voltage.
- During power up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power up are flexible, provided that the transient voltage levels follow the requirements listed previously in セクション 6.4 and in 図 9-1.

DMD Power Supply Power Down Procedure

- V_{CC} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within 4 V of ground.
- During power down it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}, but it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ±8.75 V (refer to Note 1 for 図 9-1).
- During power down, the DMD's LVCMOS input pins must be less than V_{CC} + 0.3 V.
- During power down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power down are flexible, provided that the transient voltage levels follow the requirements listed previously in セクション 6.4 and in 図 9-1.

9.1.1 Power Up and Power Down



A. ±8.75-V delta, ΔV, shall be considered the max operating delta between V_{BIAS} and V_{OFFSET}. Customers may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power up and to remove V_{BIAS} prior to V_{OFFSET} during power down.

図 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)

10 Layout

10.1 Layout Guidelines

For specific DMD PCB guidelines, use the following:

- V_{CC} should have at least 1 × 2.2-µF and 4 × 0.1-µF capacitors evenly distributed among the 6 V_{CC} pins.
- A 0.1-µF, X7R rated capacitor should be placed near every pin for V_{BIAS}, V_{RSET}, and V_{OFF}.

10.2 Temperature Diode Pins

The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411-Q1 or equivalent temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411-Q1 are sensitive to noise. See the *TMP411-Q1 data sheet* for specific routing recommendations.

Avoid routing the temperature diodes signals near other traces to reduce coupling of noise onto these signals.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

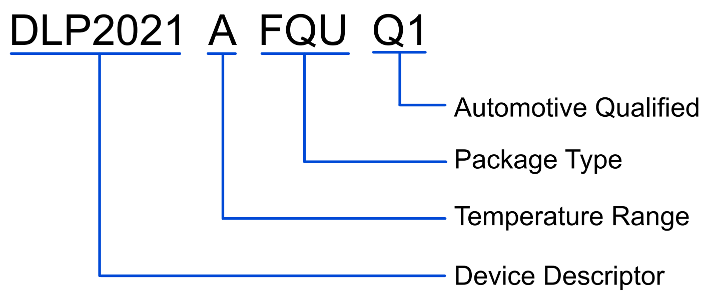


図 11-1. Part Number Description

11.1.2 Device Markings

The device marking is shown in 図 11-2. The marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 11-1. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number and lot trace code.

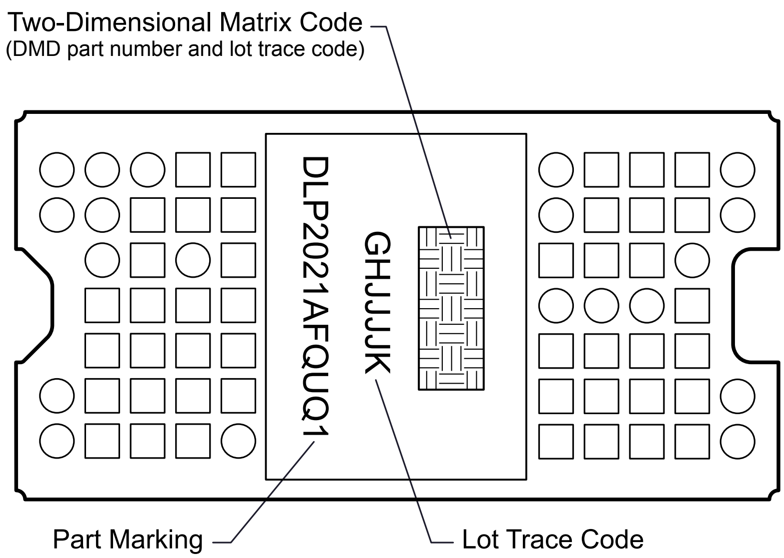


図 11-2. DMD Marking

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMP411-Q1 ±1°C Remote and Local Temperature Sensor With N-Factor and Series Resistance Correction* data sheet
- Texas Instruments, *DMD Optical Efficiency for Visible Wavelengths* application report

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 Device Handling

The DMD is an optical device so precautions should be taken to avoid damaging the glass window. Please see the DMD Handling application note for instructions on how to properly handle the DMD.

11.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2022) to Revision B (December 2023) **Page**

- データシートを「事前情報」から「量産データ」に変更 1
- Changed figure link of human-readable information 24

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP2021AFQUQ1	Active	Production	CLGA (FQU) | 64	126 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-40 to 105	
DLP2021AFQUQ1.A	Active	Production	CLGA (FQU) | 64	126 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

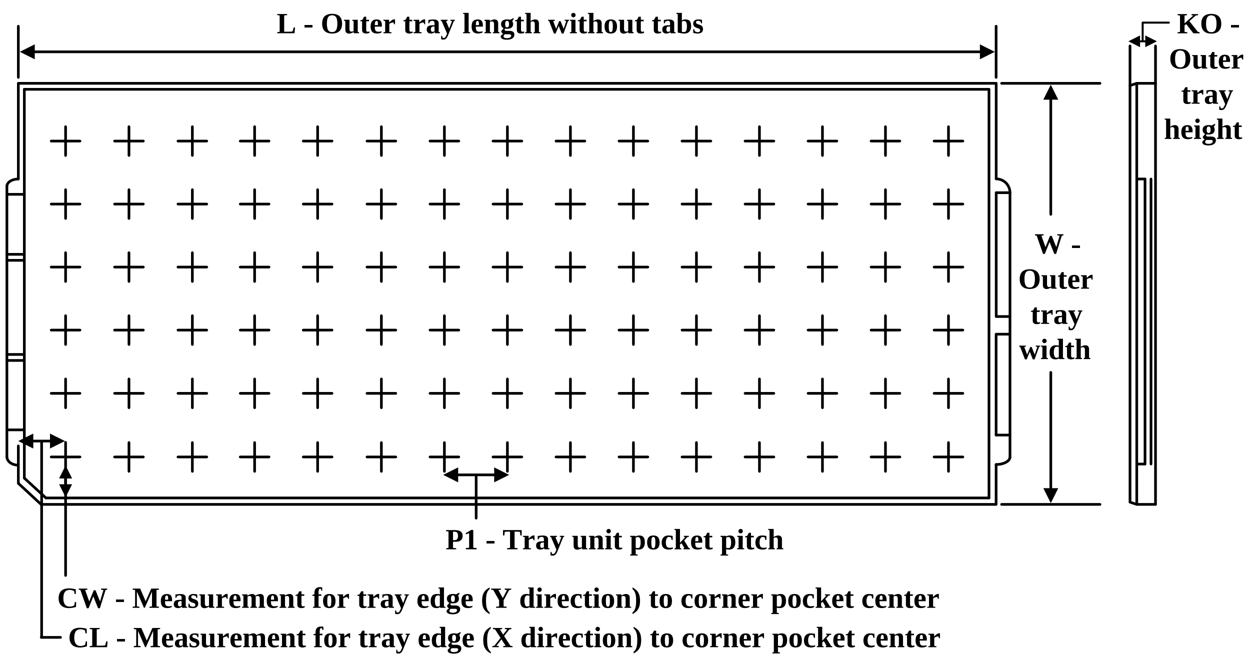
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP2021AFQUQ1	FQU	CLGA	64	126	9 x 14	150	315	135.9	12190	21.9	15.15	16.95
DLP2021AFQUQ1.A	FQU	CLGA	64	126	9 x 14	150	315	135.9	12190	21.9	15.15	16.95

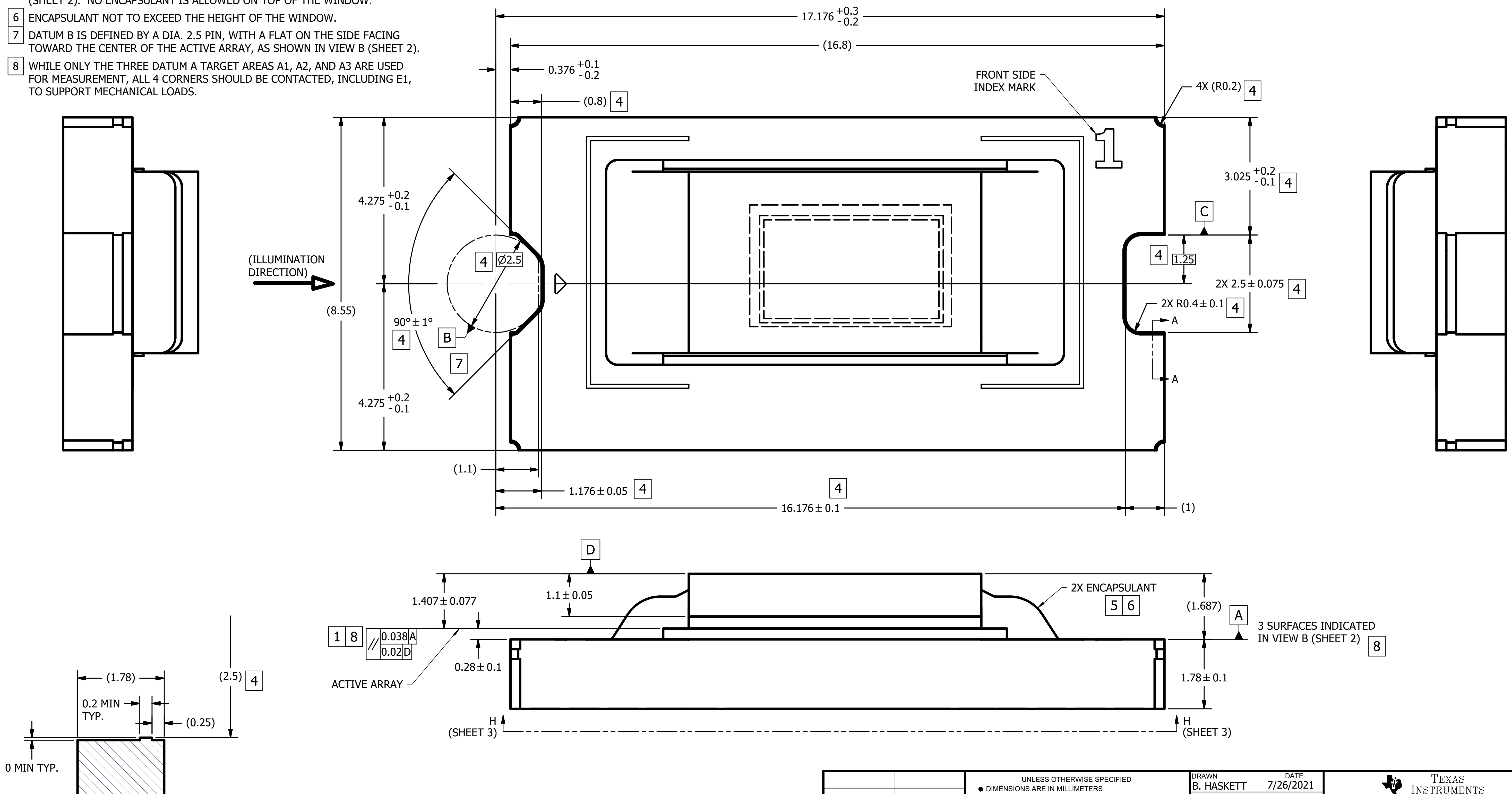
8	7	6	5	4	3	DWG NO. 2517857	SH 1	1

REVISIONS

REV	DESCRIPTION	DATE	BY
A	ECO 2196032: INITIAL RELEASE	7/26/2021	BMH
B	ECO 2199613: CORRECT WINDOW SIZE	4/11/2022	PPC
C	ECO 2201377: TOLERANCE RIGHT & BOTTOM EDGES FROM DATUMS B/C, INSTEAD OF FROM LEFT & TOP EDGES	10/11/2022	PPC

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY SECOND LAYER OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.



SECTION A-A
NOTCH OFFSETS
SCALE 25:1

	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	7/26/2021
ENGINEER	P. CREERY	7/26/2021
QA/CE	M. DOUGLASS	7/29/2021
CM	B. MENDOZA	7/26/2021
	B. RAY	7/26/2021
APPROVED	J. McKINLEY	7/26/2021

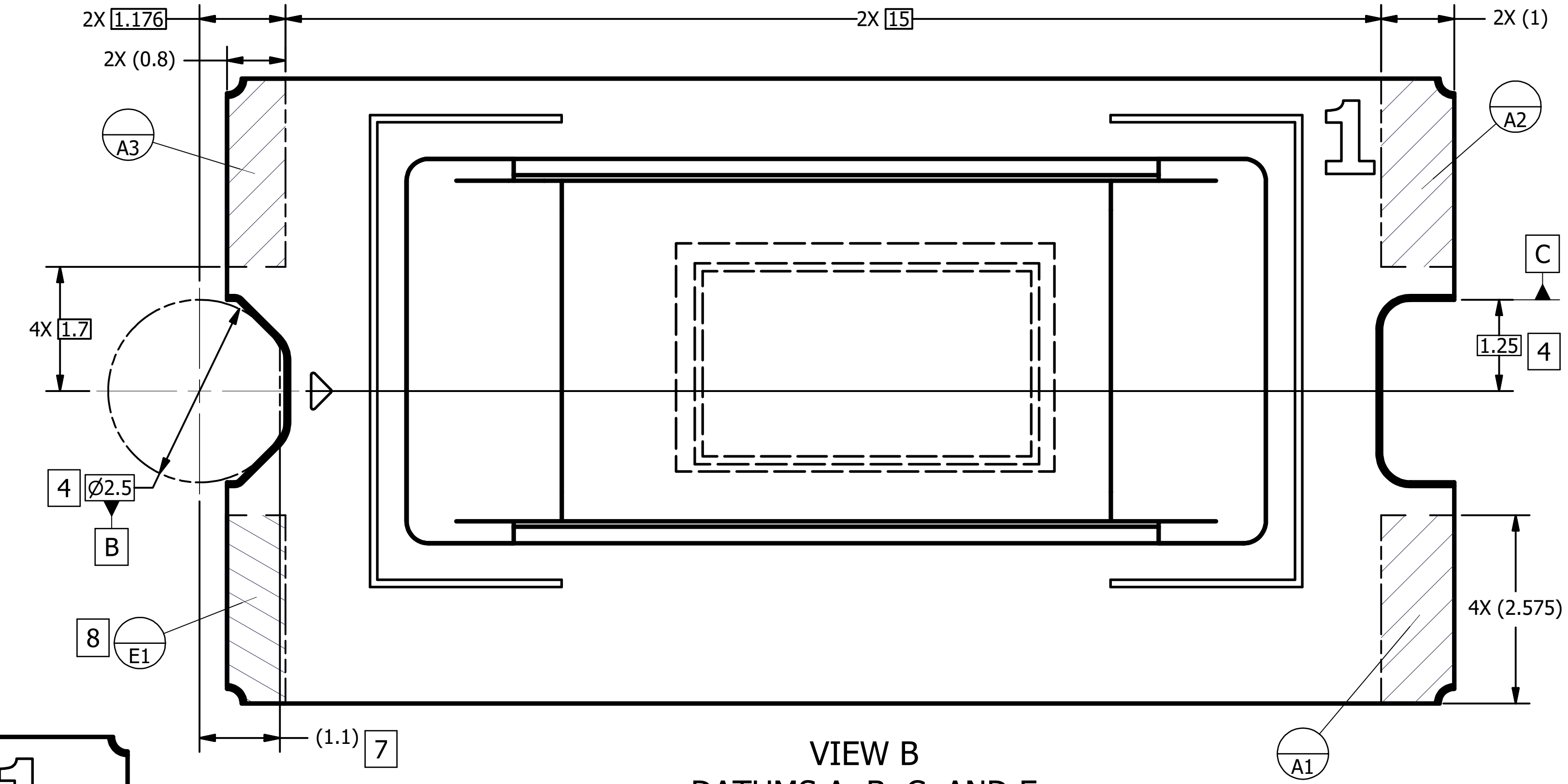
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.2 AUTO 16:9 SERIES 249
(FQU PACKAGE)

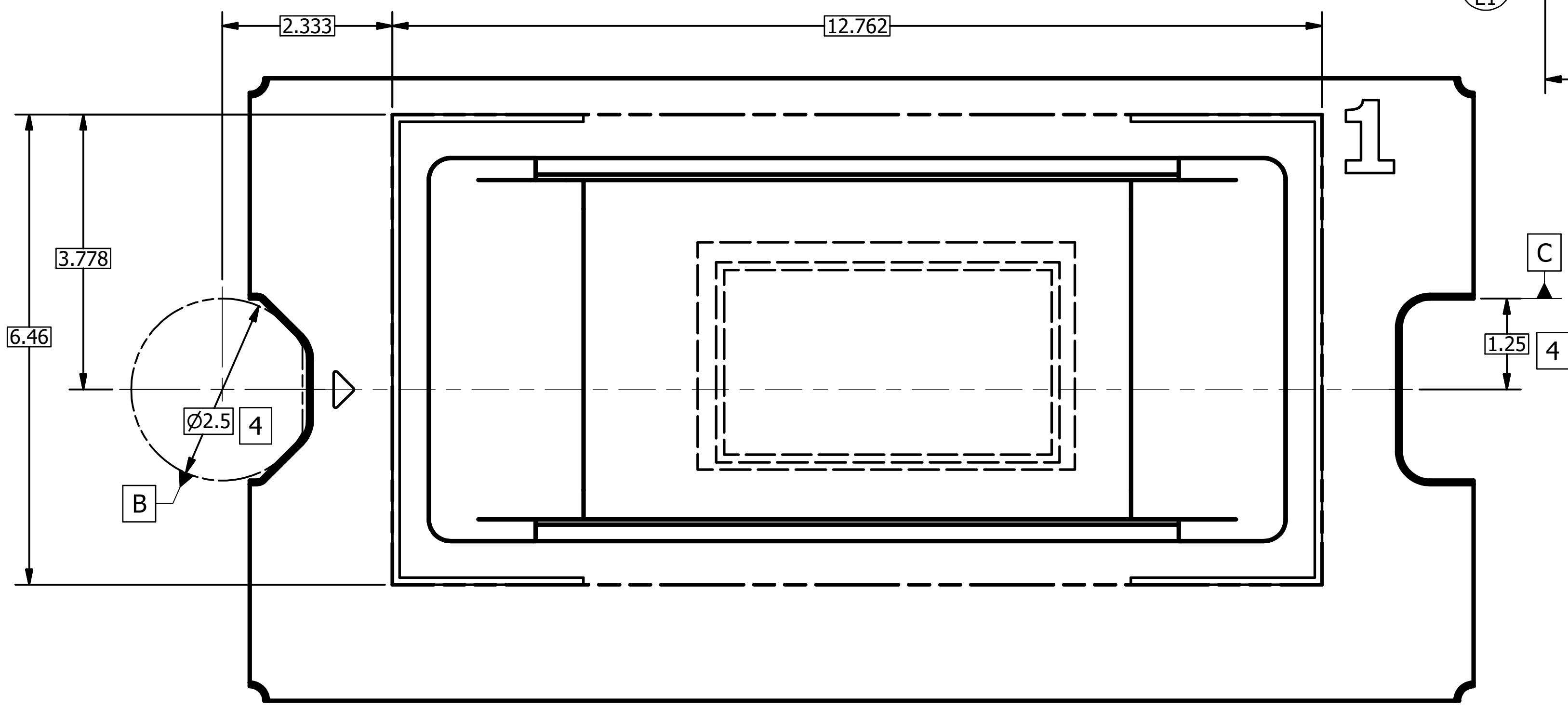
SIZE D | DWG NO 2517857 | REV C
SCALE 20:1 | SHEET 1 OF 3

INV11-2006a

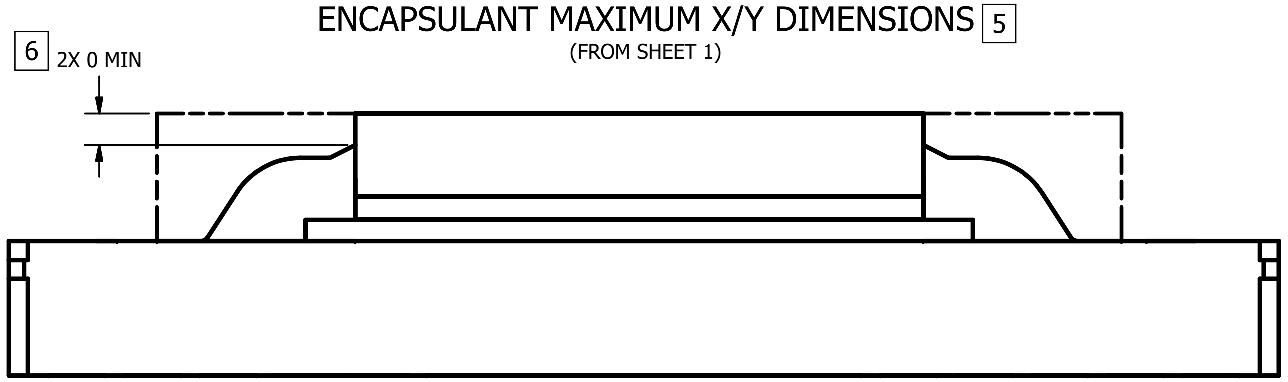
8	7	6	5	4	3	2	1



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



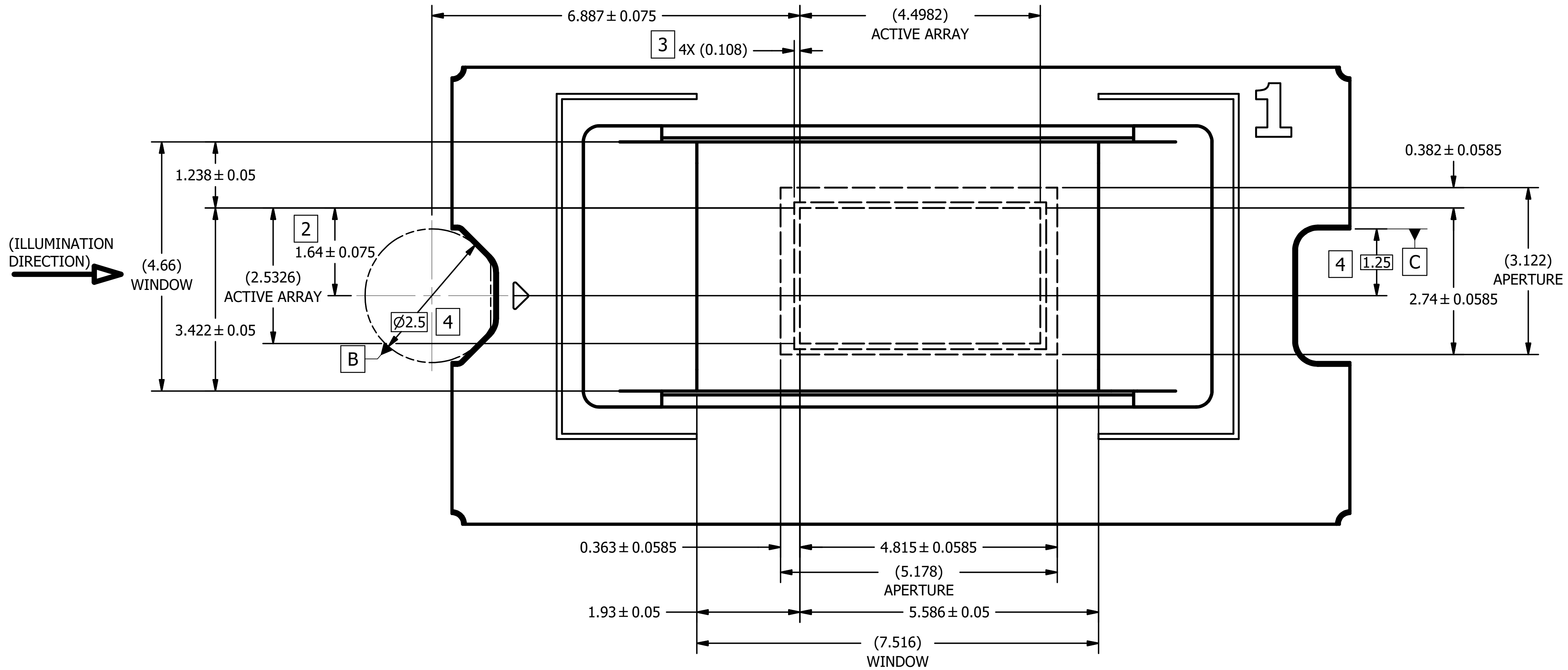
VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)



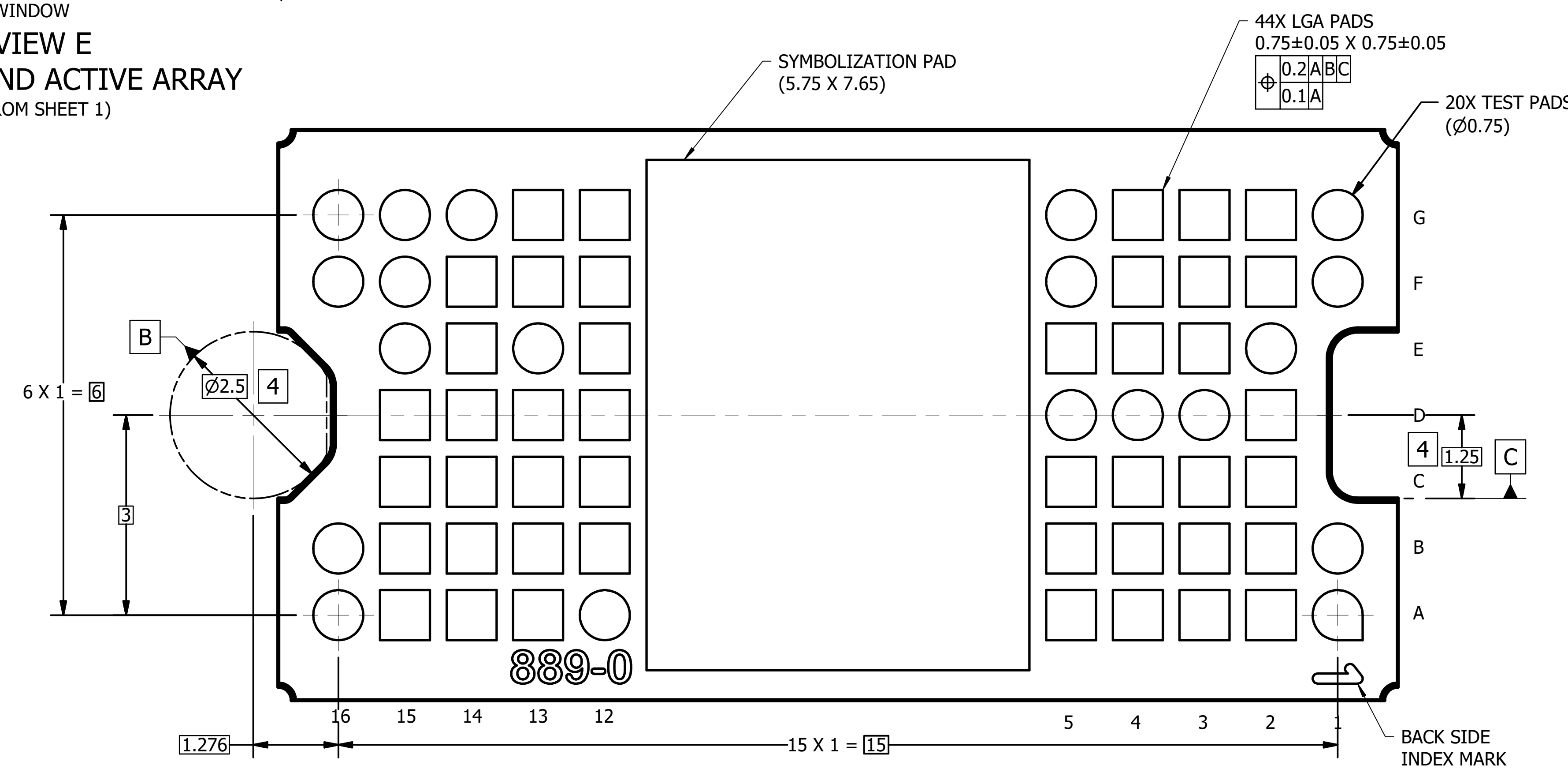
VIEW D
ENCAPSULANT MAXIMUM HEIGHT

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 7/26/2021	SIZE D	DWG NO 2517857	REV C
			SCALE		SHEET 2 OF 3

INV11-2006a



VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 7/26/2021	SIZE D	DWG NO 2517857	REV C
			SCALE	SHEET 3 OF 3	

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