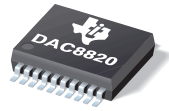


16-Bit, Parallel Input Multiplying Digital-to-Analog Converter

FEATURES

- **±0.5 LSB DNL**
- **±1 LSB INL**
- **16-Bit Monotonic**
- **Low Noise: 10 nV/√Hz**
- **Low Power: I_{DD} = 2 μA**
- **Analog Power Supply: +2.7 V to +5.5 V**
- **1.66 mA Full-Scale Current, with V_{REF} = 10 V**
- **Settling Time: 0.5 μs**
- **4-Quadrant Multiplying Reference**
- **Reference Bandwidth: 8 MHz**
- **Reference Input: ±15 V**
- **Reference Dynamics: –105 dB THD**
- **SSOP-28 Package**
- **Industry-Standard Pin Configuration**

APPLICATIONS

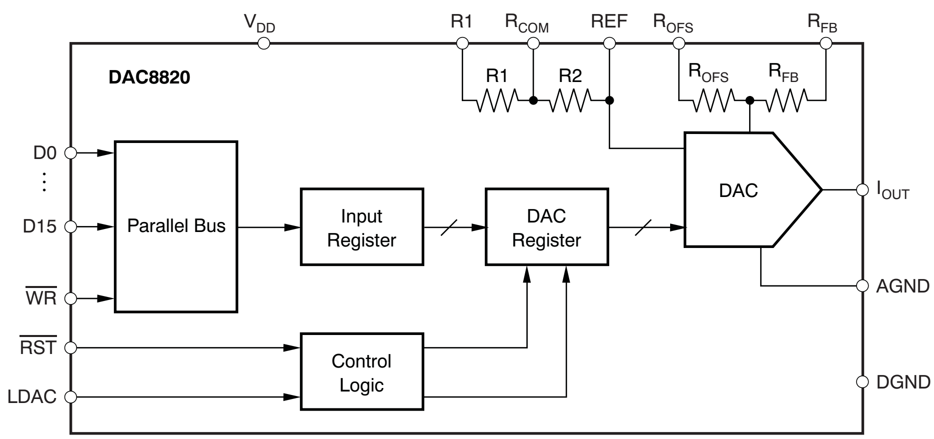
- **Automatic Test Equipment**
- **Instrumentation**
- **Digitally Controlled Calibration**
- **Industrial Control PLCs**

DESCRIPTION

The DAC8820, a multiplying digital-to-analog converter (DAC), is designed to operate from a single 2.7 V to 5.5 V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external, current-to-voltage (I/V) precision amplifier.

A parallel interface offers high-speed communications. The DAC8820 is packaged in a space-saving SSOP-28 package and has an industry-standard pinout.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8820IB	±2	±1	DB-28 (SSOP)	–40°C to +85°C	DAC8820	DAC8820IBDB	Tubes, 48
						DAC8820IBDBR	Tape and Reel, 2000
DAC8820IC	±1	±1	DB-28 (SSOP)	–40°C to +85°C	DAC8820	DAC8820ICDB	Tubes, 48
						DAC8820ICDBR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

		DAC8820	UNIT
V_{DD} to GND		–0.3 to +7	V
Digital input voltage to GND		–0.3 to $+V_{DD}$ + 0.3	V
V (I_{OUT}) to GND		–0.3 to $+V_{DD}$ + 0.3	V
REF, R_{OFS}, R_{FB}, R1, R_{COM} to AGND, DGND		±25	V
Operating temperature range		–40 to +85	°C
Storage temperature range		–65 to +150	°C
Junction temperature range (T_J max)		+125	°C
Power dissipation		(T_J max – T_A) / $R_{\theta JA}$	W
Thermal impedance, $R_{\theta JA}$		55	°C/W
ESD rating	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +85C, V_{DD} = +2.7 V to +5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, and T_A = full operating temperature, unless otherwise noted.

PARAMETER		CONDITIONS	DAC8820 MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			16			Bits
Relative accuracy		DAC8820IB			±2	LSB
Relative accuracy		DAC8820IC			±1	LSB
Differential nonlinearity				±0.5	±1	LSB
Output leakage current		Data = 0000h, T_A = +25°C			5	nA
Output leakage current		Data = 0000h, $T_A = T_{MAX}$			10	nA
Full-scale gain error		Unipolar, data = FFFFh		2	±16	LSB
		Bipolar, data = FFFFh		2	±16	LSB
Full-scale temperature coefficient				1	2	ppm/°C
Bipolar zero scale error		T_A = +25°C			±5	LSB
		$T_A = T_{MAX}$			±8	LSB
PSRR		Power-supply rejection ratio; V_{DD} = 5 V ±10%		±0.2	±2.0	LSB/V
OUTPUT CHARACTERISTICS(1)						
Output current				1.66		mA
Output capacitance		Code dependent		50		pF
REFERENCE INPUT						
V_{REF} Range			–15		15	V
R_{REF}		Input resistance (unipolar)	4.5	6	7.5	kΩ
Input capacitance				5		pF
R1/R2		R1/R2 resistance (bipolar)	9	12	15	kΩ
R_{OFS}, R_{FB}		Feedback and offset resistance	9	12	15	kΩ
LOGIC INPUTS AND OUTPUT(1)						
Input low voltage	V_{IL}	V_{DD} = +2.7 V			0.6	V
	V_{IL}	V_{DD} = +5 V			0.8	V
Input high voltage	V_{IH}	V_{DD} = +2.7 V	2.1			V
	V_{IH}	V_{DD} = +5 V	2.4			V
Input leakage current	I_{IL}			0.001	1	µA
Input capacitance	C_{IL}				8	pF
INTERFACE TIMING, V_{DD} = +5.0V(1) **(See Figure 40 and Table 1)**						
	t_{DS}	Data to $\overline{WR}$ setup time	20			ns
	t_{DH}	Data to $\overline{WR}$ hold time	0			ns
	t_{WR}	$\overline{WR}$ pulse width	20			ns
	t_{LDAC}	LDAC pulse width	20			ns
Data setup time	t_{RST}	$\overline{RST}$ pulse width	20			ns
Data hold time	t_{LWD}	$\overline{WR}$ to LDAC delay time	0			ns
INTERFACE TIMING, V_{DD} = +2.7V(1) **(See Figure 40 and Table 1)**						
	t_{DS}	Data to $\overline{WR}$ setup time	35			ns
	t_{DH}	Data to $\overline{WR}$ hold time	0			ns
	t_{WR}	$\overline{WR}$ pulse width	35			ns
	t_{LDAC}	LDAC pulse width	35			ns
Data setup time	t_{RST}	$\overline{RST}$ pulse width	35			ns
Data hold time	t_{LWD}	$\overline{WR}$ to LDAC delay time	0			ns

(1) Specified by design and characterization; not production tested.

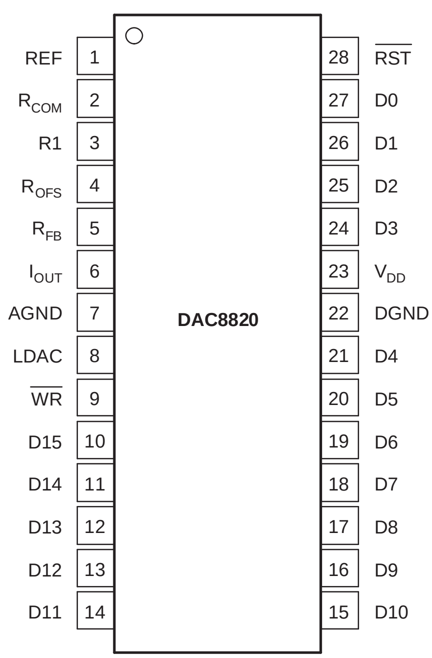
ELECTRICAL CHARACTERISTICS (continued)

All specifications at –40°C to +85C, V_{DD} = +2.7 V to +5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, and T_A = full operating temperature, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8820 MIN	TYP	MAX	UNITS
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD} (normal operation)	Logic inputs = 0 V			5	µA
V_{DD} = +4.5 V to +5.5 V	V_{IH} = V_{DD} and V_{IL} = GND		3	5	µA
V_{DD} = +2.7 V to +3.6 V	V_{IH} = V_{DD} and V_{IL} = GND		1	2.5	µA
AC CHARACTERISTICS(2)					
Output current settling time			0.5		µs
Reference multiplying BW	V_{REF} = 5 V_{PP}, Data = FFFFh		8		MHz
DAC glitch impulse	V_{REF} = 0 V to 10 V, Data = 7FFFh to 8000h to 7FFFh		2		nV–s
Feedthrough error V_{OUT}/V_{REF}	Data = 0000h, V_{REF} = 10 kHz, ±10 V_{PP}		–70		dB
Digital feedthrough	LDAC = Logic low, V_{REF} = –10 V to + 10 V Any code change		1		nV–s
Total harmonic distortion	V_{REF} = 6 V_{RMS}, Data = FFFFh, f = 1 kHz		–105		dB
Output spot noise voltage			10		nV/√Hz

(2) Specified by design and characterization; not production tested.

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

PIN #	NAME	DESCRIPTION
1	REF	Reference input and 4-quadrant resistor (R2).
2	R_{COM}	Center tap of two 4-quadrant resistors (R1 and R2).
3	R1	4-quadrant resistor (R1).
4	R_{OFS}	Bipolar offset resistor
5	R_{FB}	Internal matching feedback resistor
6	I_{OUT}	DAC current output
7	AGND	Analog ground
8	LDAC	Digital input load DAC control. When LDAC is high, data is loaded from input register into a DAC register, updating the DAC output.
9	$\overline{WR}$	Write control digital input. Active low. When $\overline{WR}$ is taken to logic low, data is loaded from the digital input pins (D0–D15) into a16-bit input register.
10–21	D15–D4	Digital input data bits. D15 is MSB.
22	DGND	Digital ground
23	V_{DD}	Positive power supply
24–27	D3–D0	Digital Input data bits. D0 is LSB.
28	$\overline{RST}$	Reset. Active low. When $\overline{RST}$ is taken to logic low, the DAC register is set to zero code, resulting in the DAC output being set to 0 V.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V

At T_A = +25°C, unless otherwise noted.

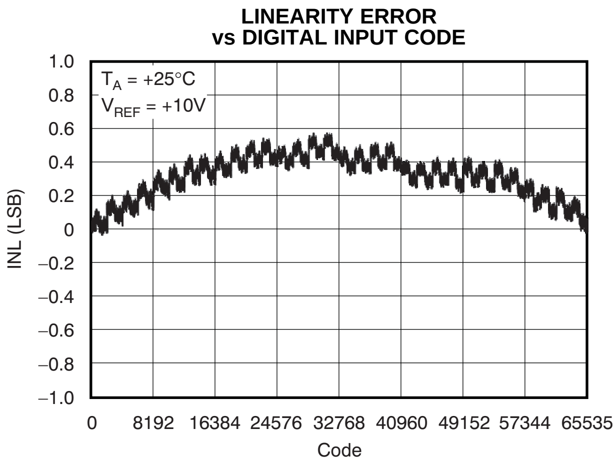


Figure 1.

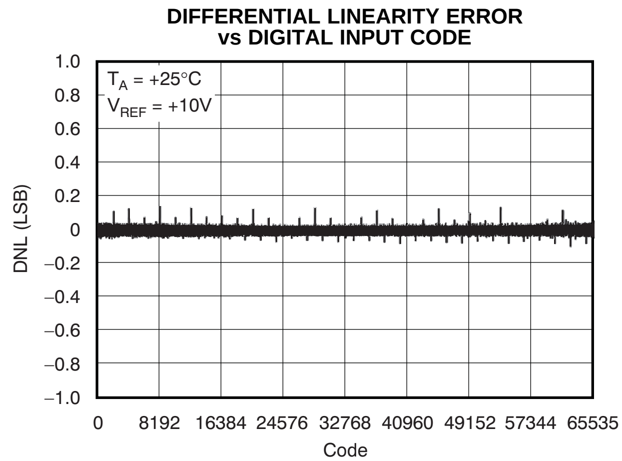


Figure 2.

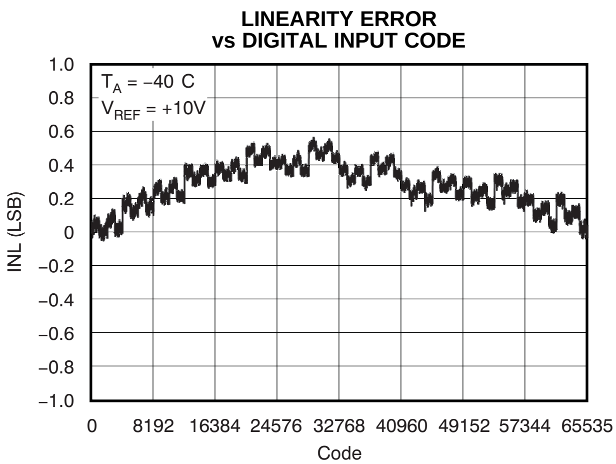


Figure 3.

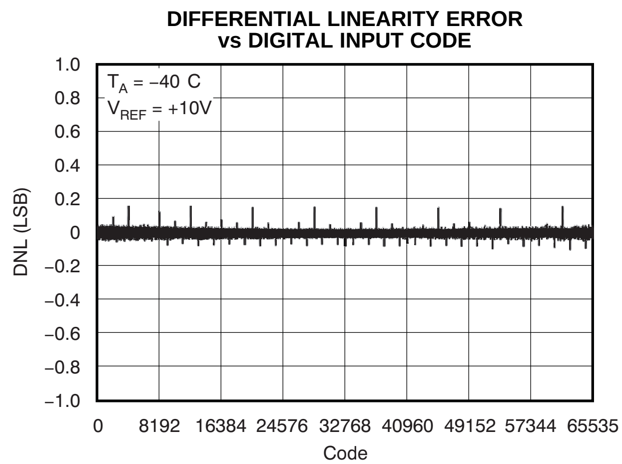


Figure 4.

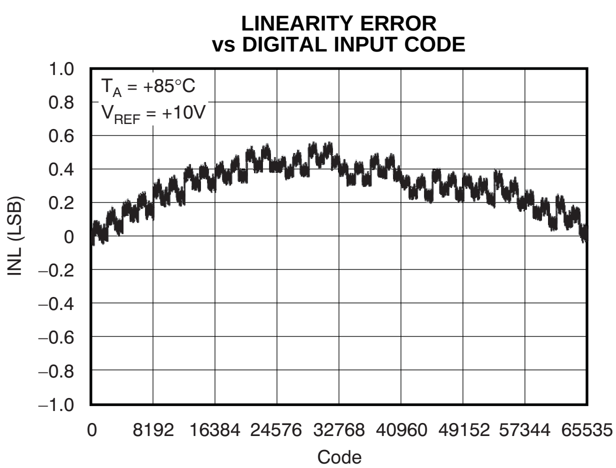


Figure 5.

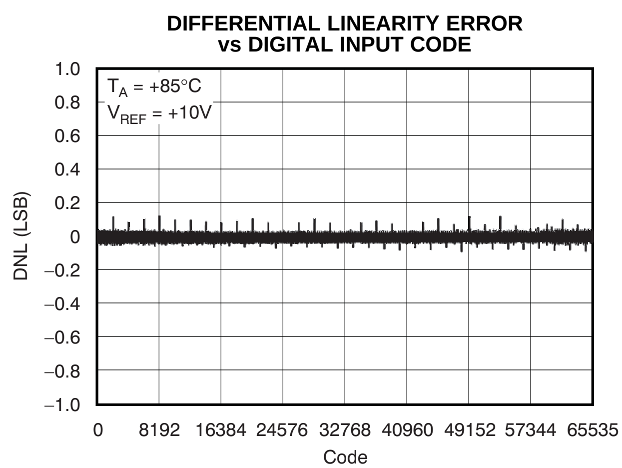


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

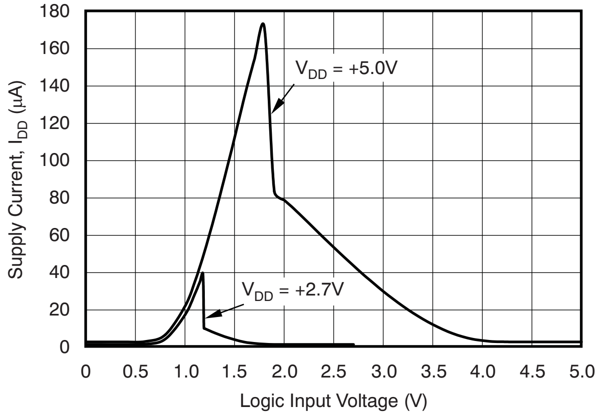


Figure 7.

REFERENCE MULTIPLYING BANDWIDTH UNIPOLAR MODE

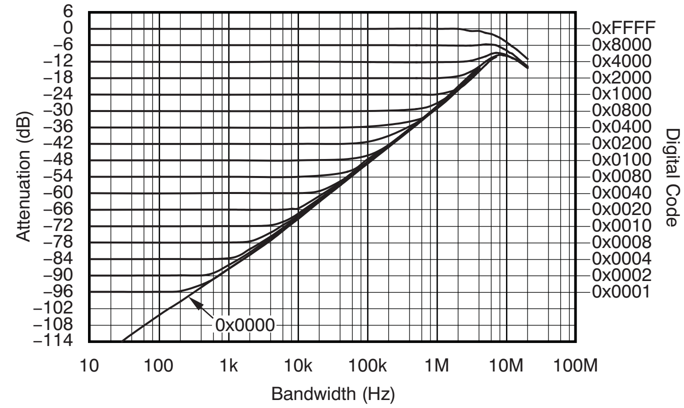


Figure 8.

REFERENCE MULTIPLYING BANDWIDTH BIPOLAR MODE

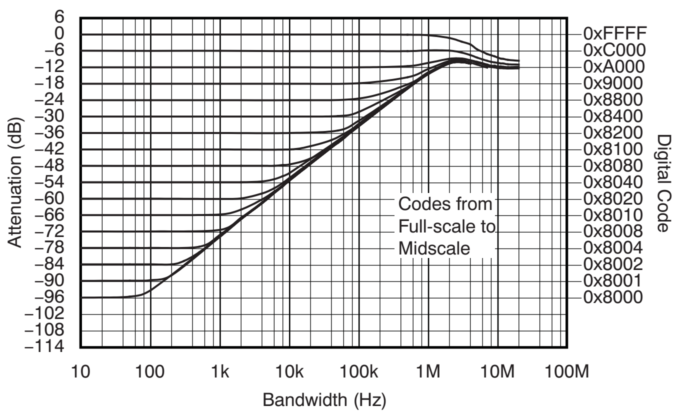


Figure 9.

REFERENCE MULTIPLYING BANDWIDTH BIPOLAR MODE

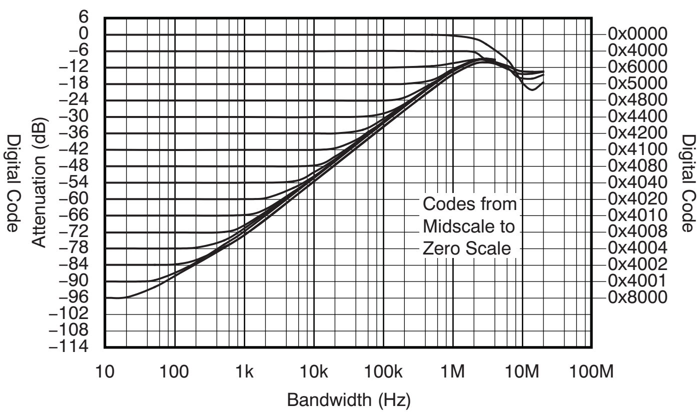


Figure 10.

MIDSCALE DAC GLITCH

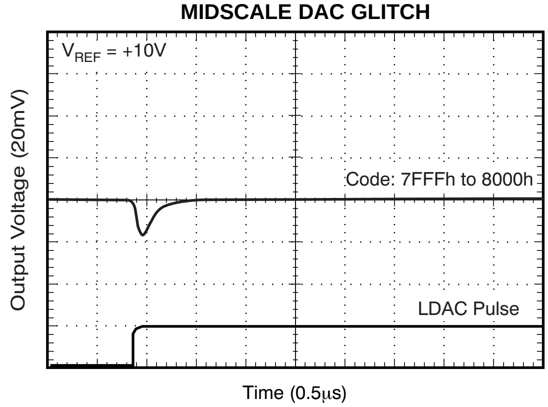


Figure 11.

MIDSCALE DAC GLITCH

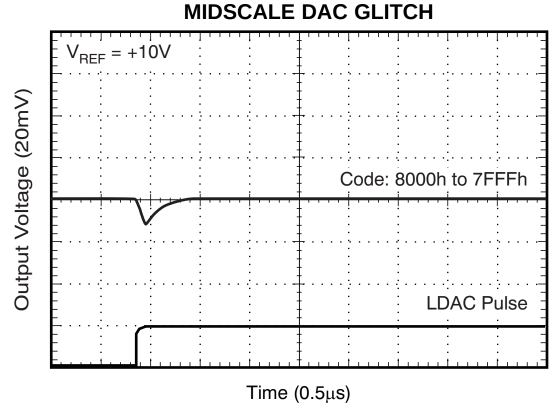


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, unless otherwise noted.

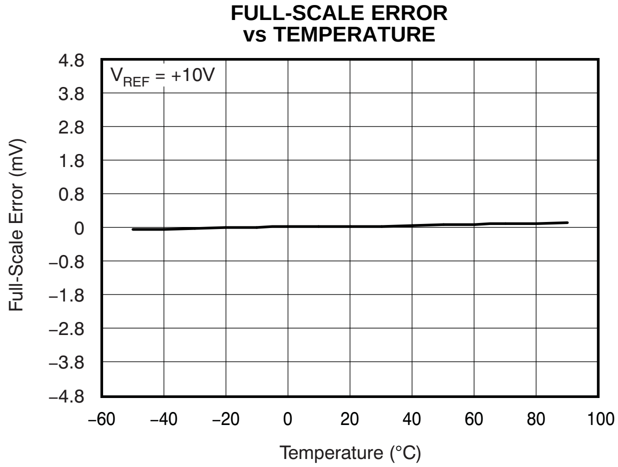


Figure 13.

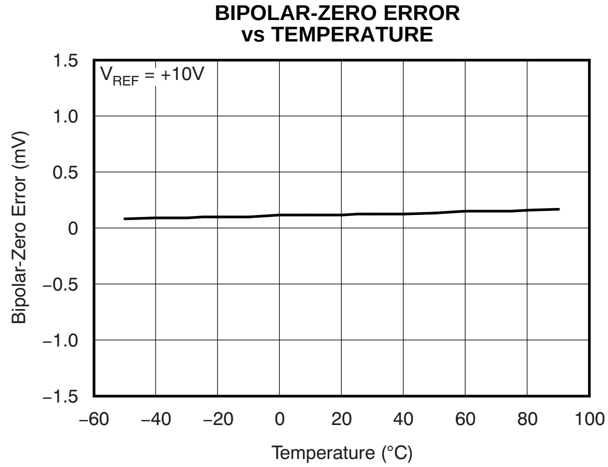


Figure 14.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

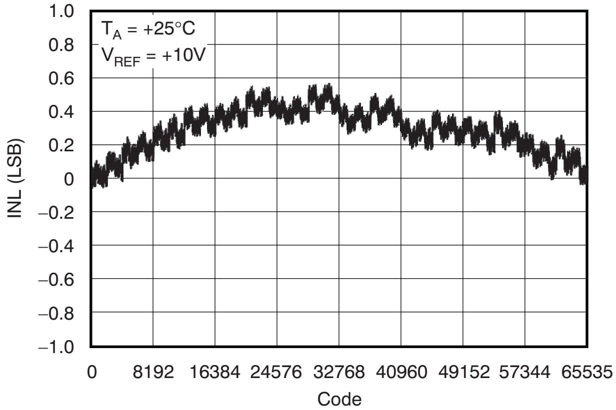


Figure 15.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

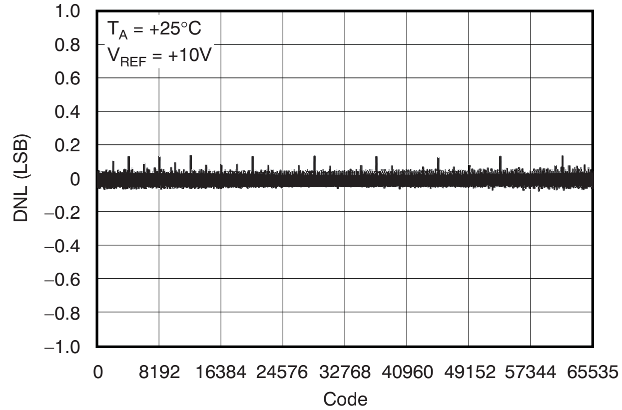


Figure 16.

LINEARITY ERROR vs DIGITAL INPUT CODE

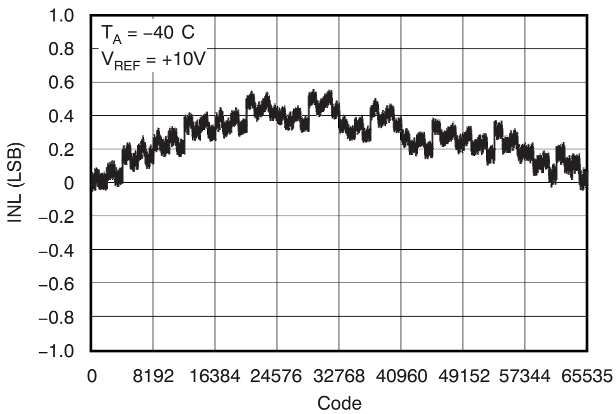


Figure 17.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

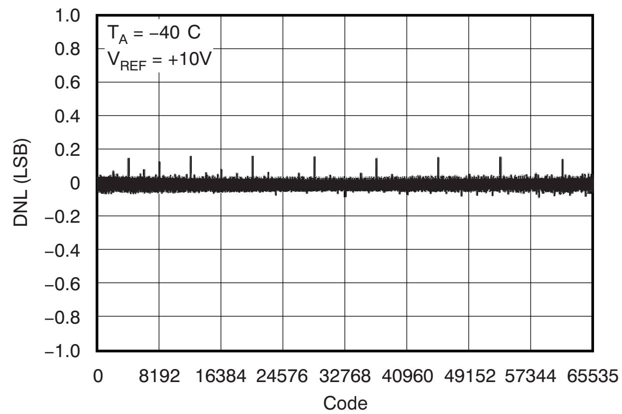


Figure 18.

LINEARITY ERROR vs DIGITAL INPUT CODE

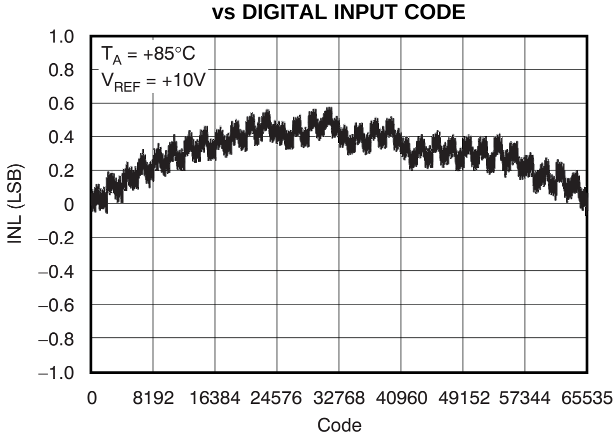


Figure 19.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

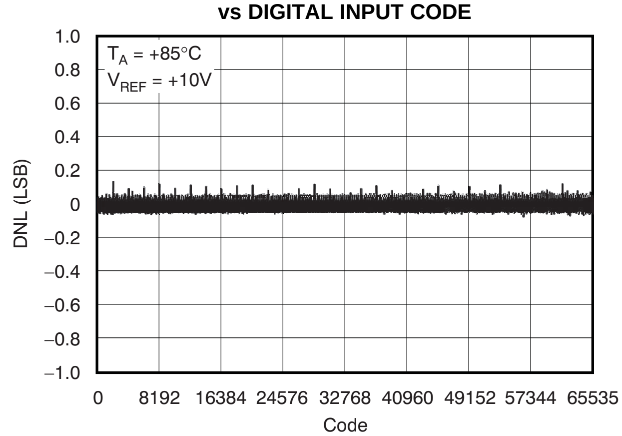


Figure 20.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, unless otherwise noted.

DAC GLITCH

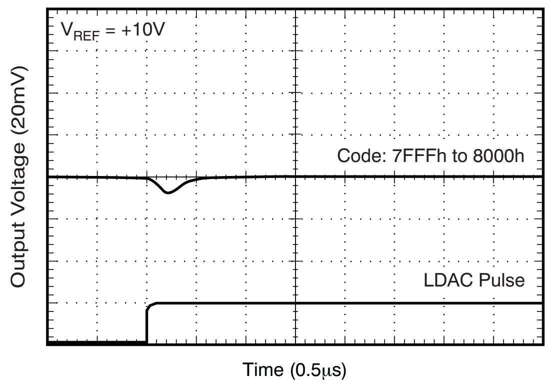


Figure 21.

DAC GLITCH

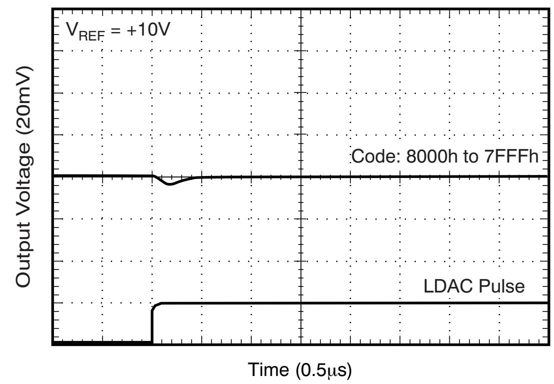


Figure 22.

FULL-SCALE ERROR vs TEMPERATURE

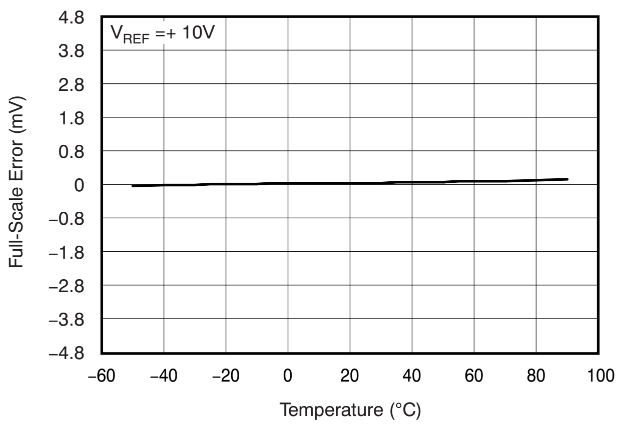


Figure 23.

BIPOLAR-ZERO ERROR vs TEMPERATURE

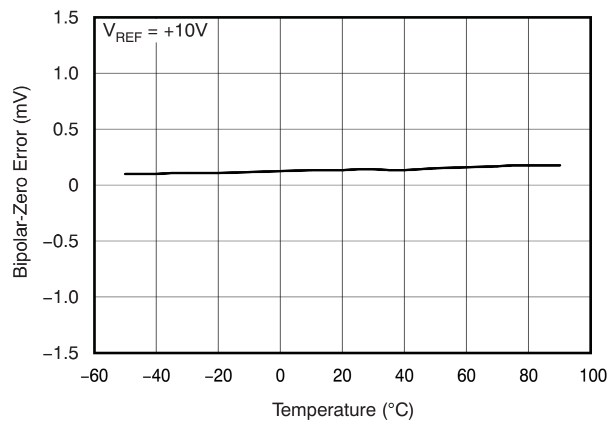


Figure 24.

TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

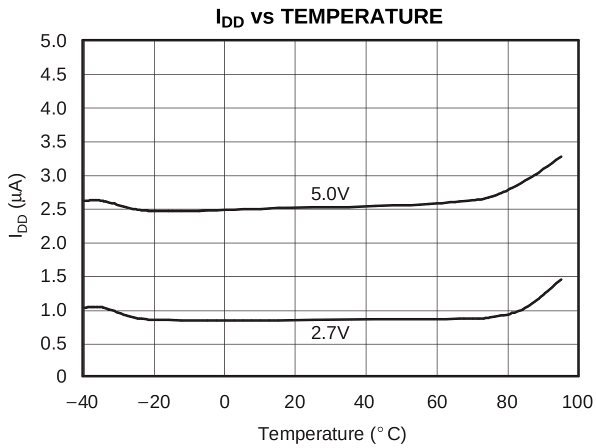


Figure 25.

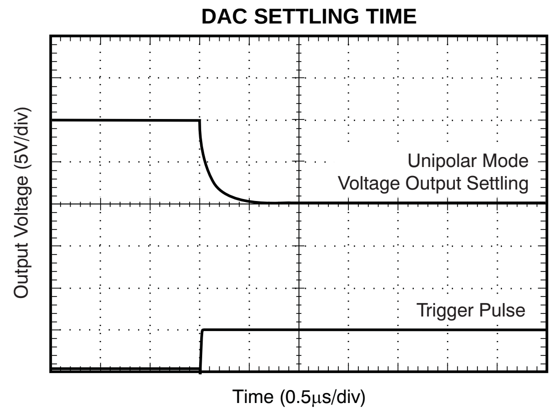


Figure 26.

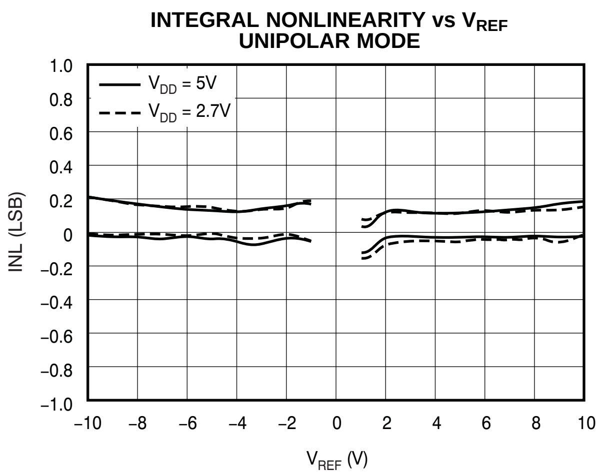


Figure 27.

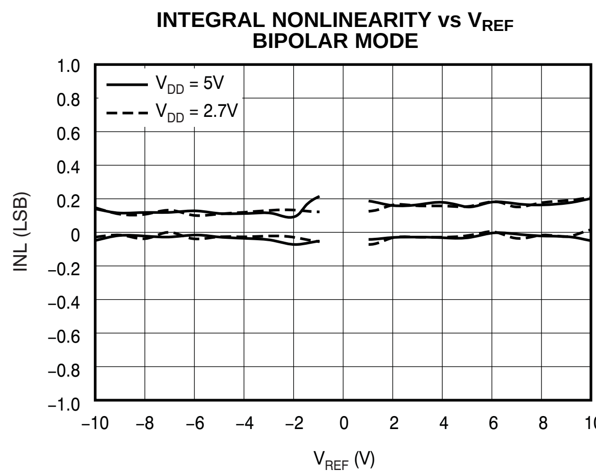


Figure 28.

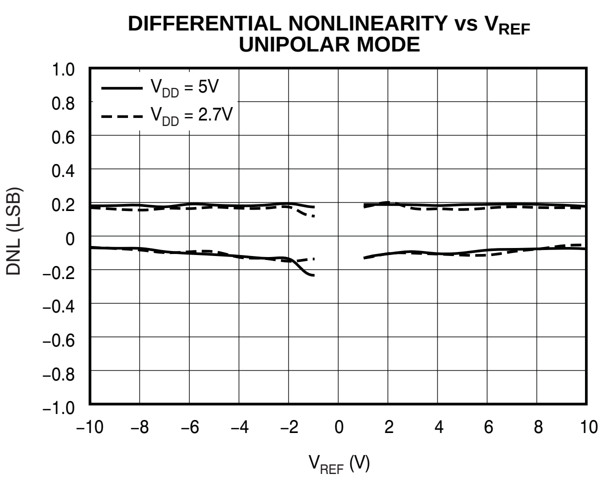


Figure 29.

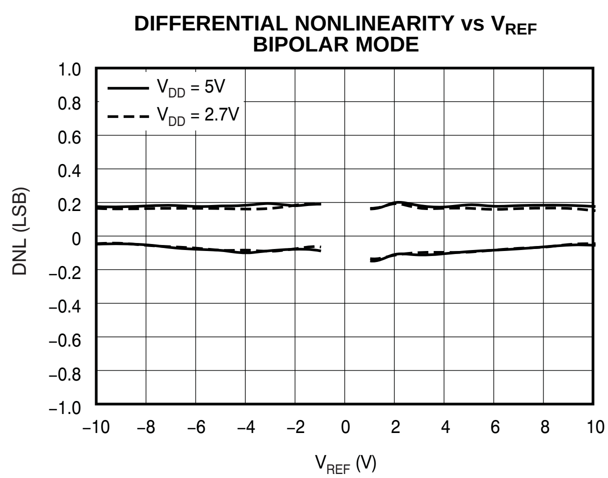


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

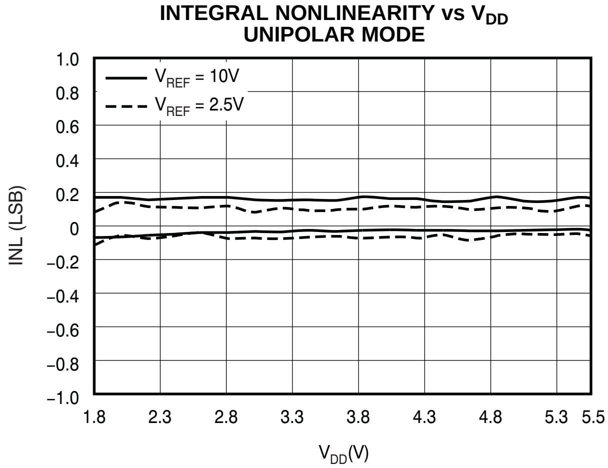


Figure 31.

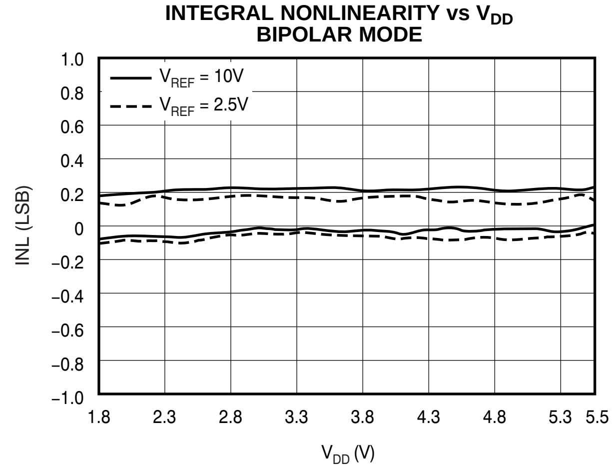


Figure 32.

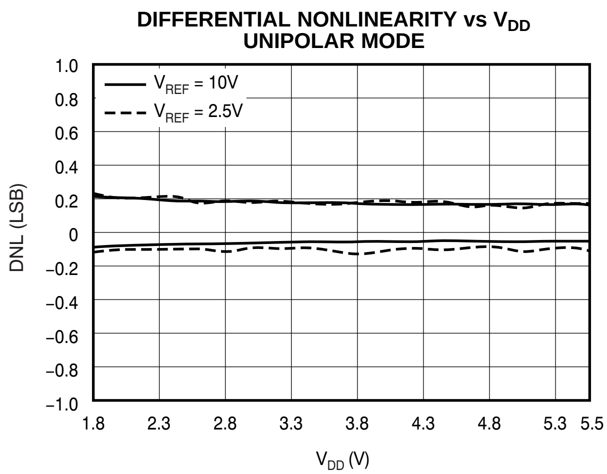


Figure 33.

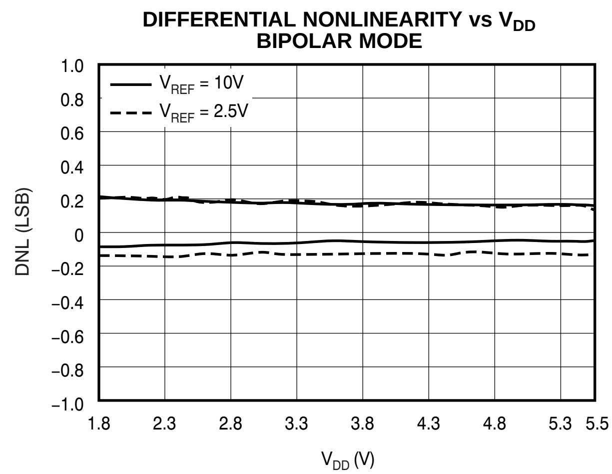


Figure 34.

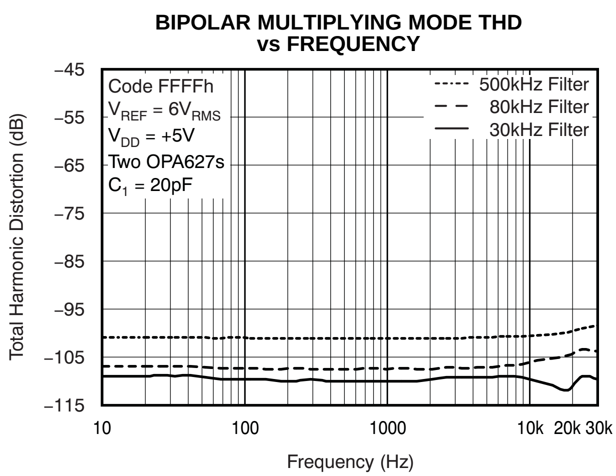


Figure 35.

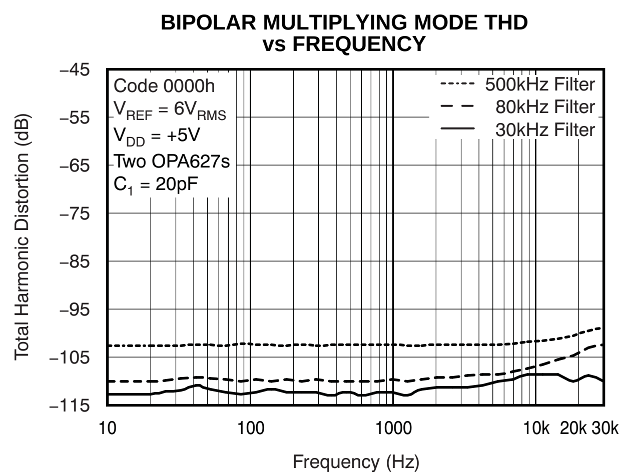


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

UNIPOLAR MULTIPLYING MODE THD vs FREQUENCY

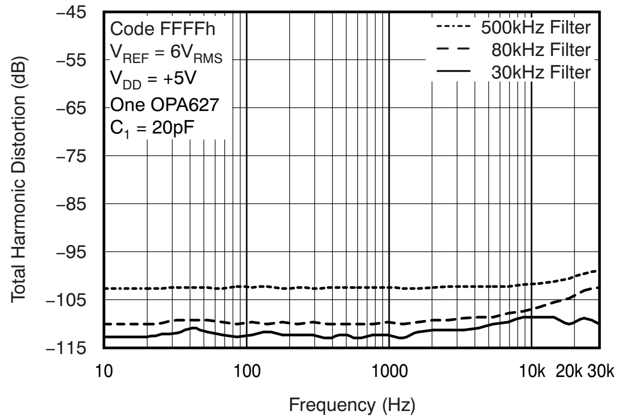


Figure 37.

THEORY OF OPERATION

The DAC8820 is a multiplying, single-channel current output, 16-bit DAC. The architecture, illustrated in Figure 38, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or to the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input (V_{REF}) that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 6 kΩ ±25%. The external reference voltage can vary in a range of –15 V to +15 V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter op amp and the R_{FB} resistor in the DAC8820, an output voltage range of –V_{REF} to +V_{REF} can be generated.

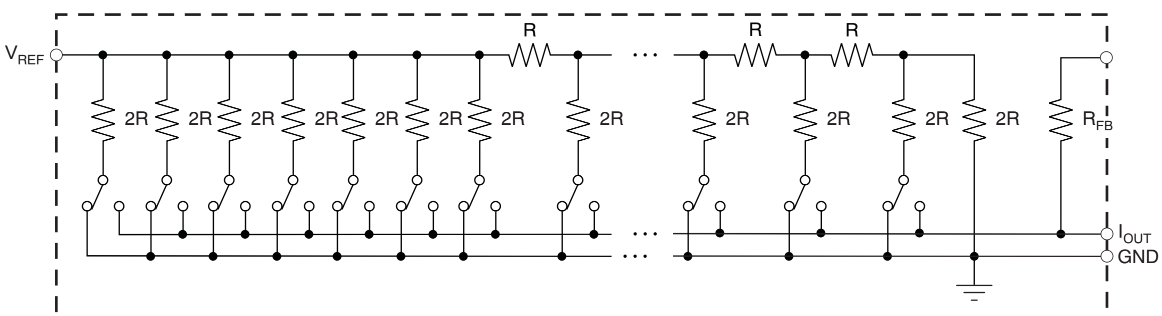


Figure 38. Equivalent R-2R DAC Circuit

The DAC output voltage is determined by V_{REF} and the digital data (D) according to Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{65536} \tag{1}$$

Each DAC code determines the 2R-leg switch position to either GND or I_{OUT}. The external I/V converter op amp noise gain will also change because the DAC output impedance (as seen looking into the I_{OUT} terminal) changes versus code. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8820 because of offset modulation versus DAC code. For best linearity performance of the DAC8820, an op amp (OPA277) is recommended, as shown in Figure 39. This circuit allows V_{REF} to swing from –10 V to +10 V.

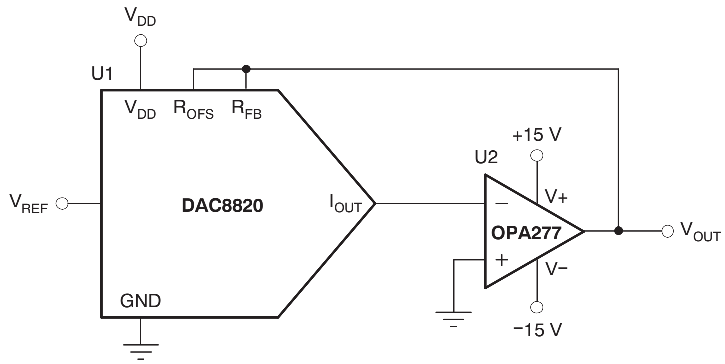


Figure 39. Voltage Output Configuration

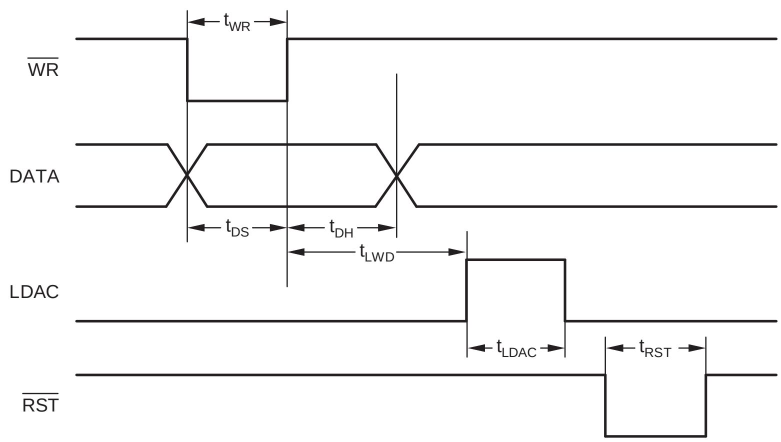


Figure 40. DAC8820 Timing Diagram

Table 1. Function of Control Inputs

CONTROL INPUTS			REGISTER OPERATION
$\overline{RST}$	$\overline{WR}$	LDAC	
0	X	X	Asynchronous operation. The DAC register is set to zero code, resulting in the DAC output being set to 0 V. The DAC input register contents are not reset by the $\overline{RST}$ signal.
1	0	0	Load the input register with all 16 data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC register are transparent.
1	⊔	⊔	LDAC and $\overline{WR}$ are tied together and programmed as a pulse. The 16 data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

APPLICATION INFORMATION

Multiplying Mode THD vs Frequency

Figure 35 and Figure 36 show the DAC8820 bipolar 4-quadrant multiplying mode total harmonic distortion (THD) versus frequency. Figure 35 shows the bipolar multiplying mode THD with the DAC8820 set to a full-scale code of FFFFh. Figure 36 shows the bipolar multiplying mode THD with the DAC8820 set to a minus full scale code of 0000h. In both graphs, two OPA627s are used for both the DAC output op amp and the reference inverting amplifier. A 6 V_{RMS} sine wave is used for the reference input V_{REF} and is swept in frequency from 10 Hz to 30 kHz. The THD levels versus frequency are illustrated at various DAC output filtering levels using an external ac-coupled low-pass filter.

Figure 37 illustrates the DAC8820 unipolar 2-quadrant multiplying mode THD versus frequency. The DAC8820 is set to a full-scale code of FFFFh. A single OPA627 is used for the DAC output op amp.

Stability Circuit

For a current-to-voltage (I/V) design, as shown in Figure 41, the DAC8820 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and laid out according to correct printed circuit board (PCB) layout design. For each code change there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, a compensation capacitor C1 (4 pF to 20 pF, typ) can be added to the design for circuit stability, as shown in Figure 41.

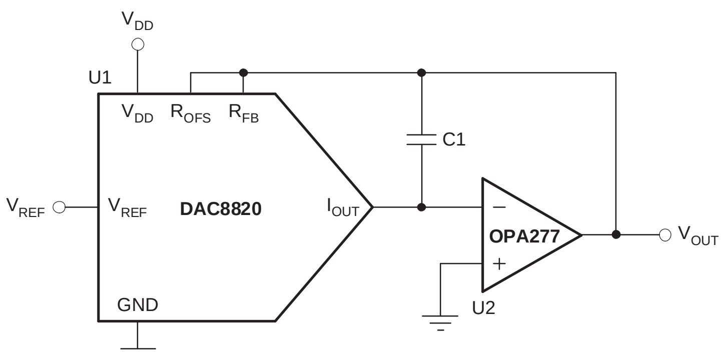


Figure 41. Gain Peaking Prevention Circuit with Compensation Capacitor

Bipolar Output Circuit

The DAC8820, as a 4-quadrant multiplying DAC, can be used to generate a bipolar output. The polarity of the full-scale output (I_{OUT}) is the inverse of the input reference voltage at V_{REF}.

Using a dual op amp, such as the OPA2277, full 4-quadrant operation can be achieved with minimal components. Figure 42 demonstrates a ±10 V_{OUT} circuit with a fixed +10 V reference.

$$V_{OUT} = \left(\frac{D}{32,768} - 1\right) \times V_{REF} \tag{2}$$

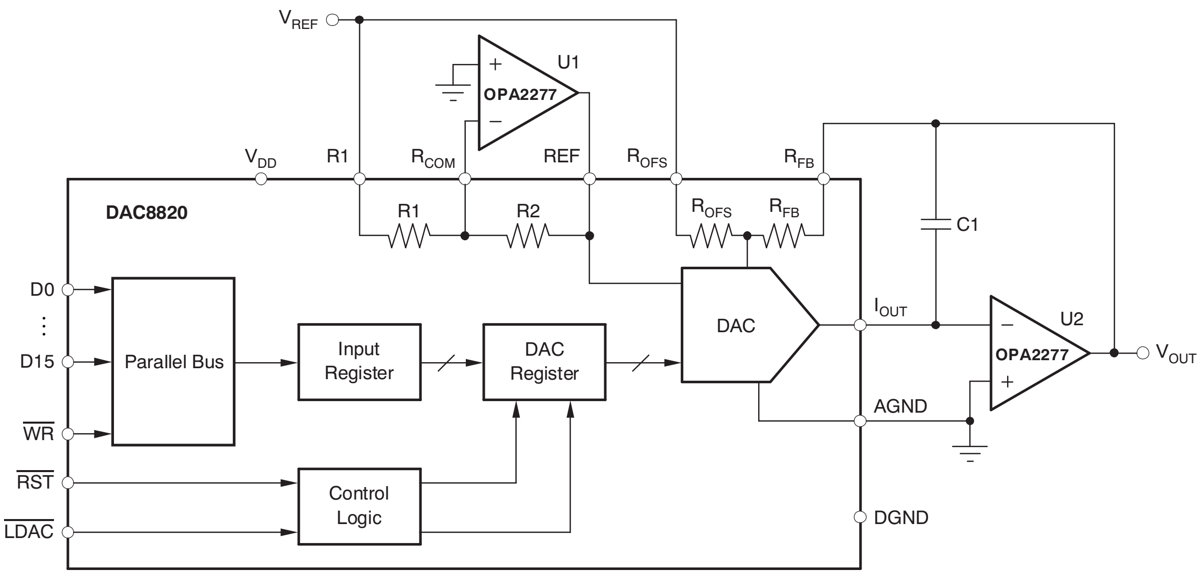


Figure 42. Bipolar Output Circuit

Programmable Current Source Circuit

A DAC8820 can be integrated into the circuit in Figure 43 to implement an improved Howland current pump for precise V/I conversions. Bidirectional current flow and high-voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_L = \frac{(R2 + R3)\ /\ R1}{R3} \times V_{REF} \times D \tag{3}$$

The value of R3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive ±20 mA in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor (C1) in the circuit is not suggested as a result of the change in the output impedance (Z_O), according to Equation 4:

$$Z_O = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \tag{4}$$

As shown in Equation 4, Z_O with matched resistors is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

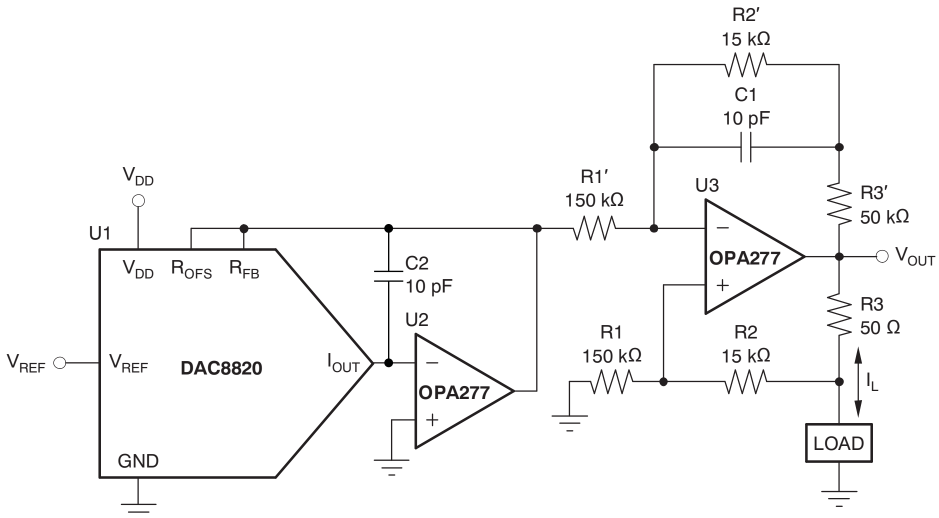


Figure 43. Programmable Bidirectional Current Source Circuit

Cross-Reference

The DAC8820 has an industry-standard pinout. Table 2 provides the cross-reference information.

Table 2. Cross-Reference

PRODUCT	BIT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8820IBDB	16	±2	±1	–40°C to +85°C	SSOP-28	SSOP-28	LTC1597BIG
DAC8820ICDB	16	±1	±1	–40°C to +85°C	SSOP-28	SSOP-28	LTC1597AIG

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8820IBDB	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820IBDB.A	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820IBDB.B	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820IBDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820IBDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820IBDBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDB	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDB.A	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDB.B	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDBG4	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDBRG4.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820
DAC8820ICDBRG4.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8820

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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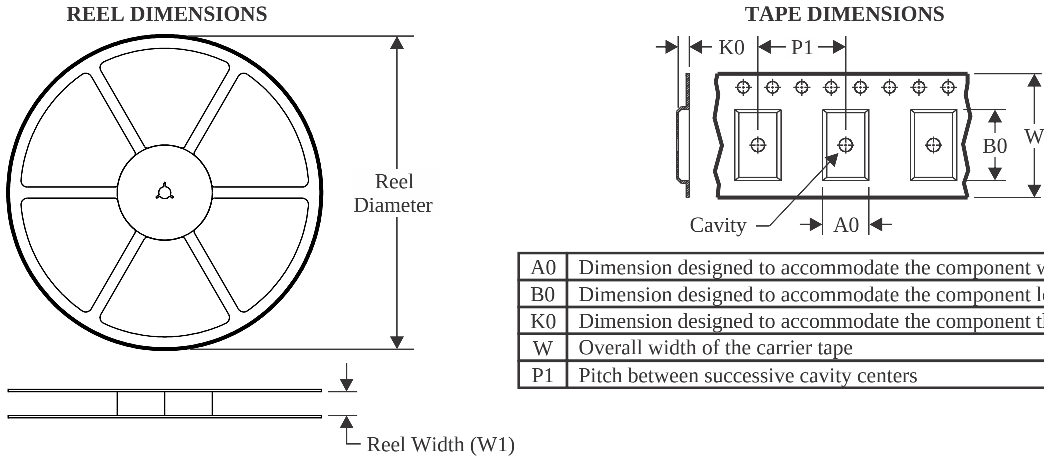
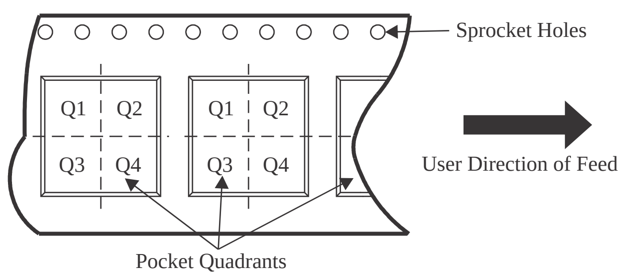
TAPE AND REEL INFORMATION



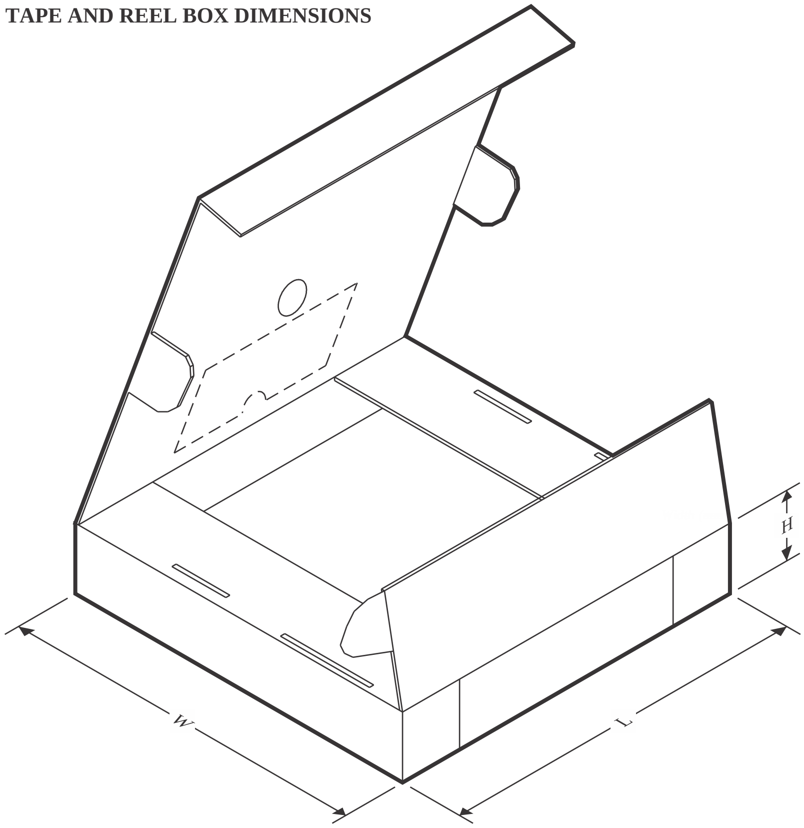
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8820IBDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
DAC8820ICDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
DAC8820ICDBRG4	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

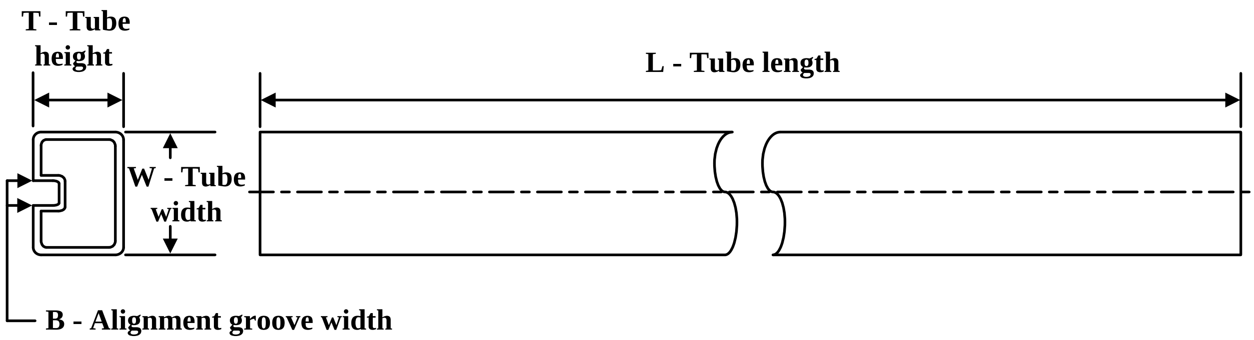
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

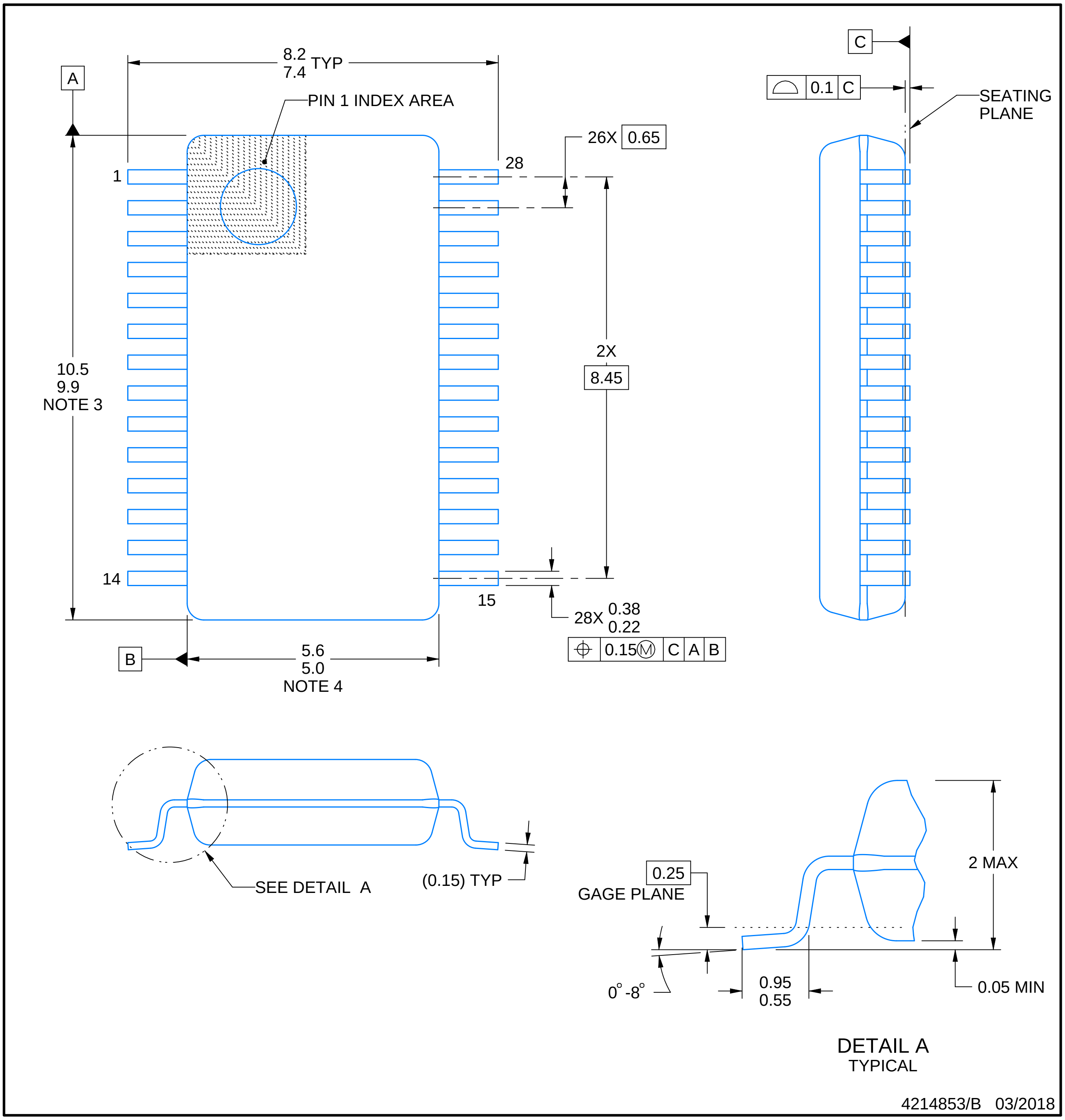
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8820IBDBR	SSOP	DB	28	2000	350.0	350.0	43.0
DAC8820ICDBR	SSOP	DB	28	2000	350.0	350.0	43.0
DAC8820ICDBRG4	SSOP	DB	28	2000	350.0	350.0	43.0

TUBE



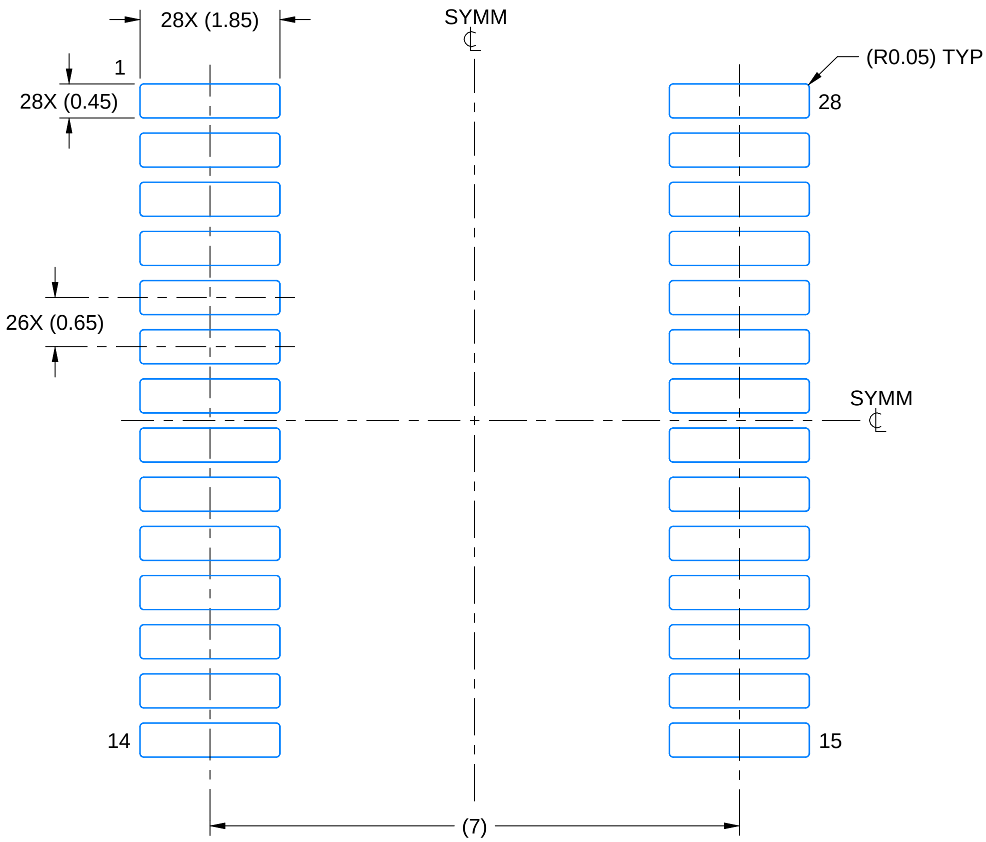
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC8820IBDB	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8820IBDB.A	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8820IBDB.B	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8820ICDB	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8820ICDB.A	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8820ICDB.B	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8820ICDBG4	DB	SSOP	28	50	530	10.5	4000	4.1

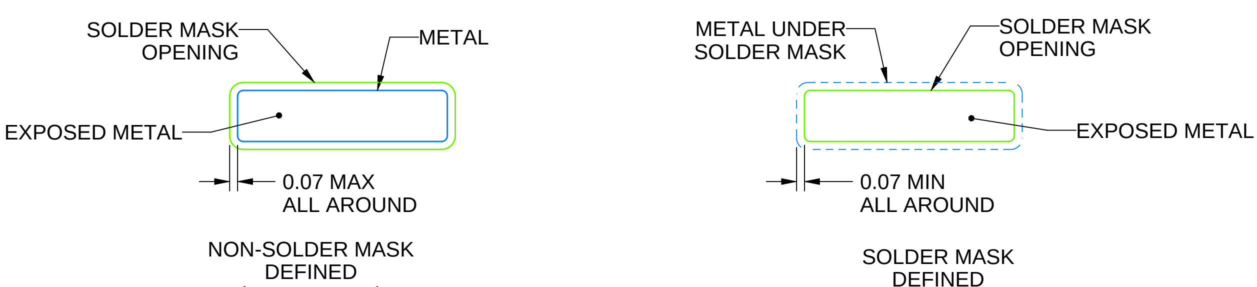


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

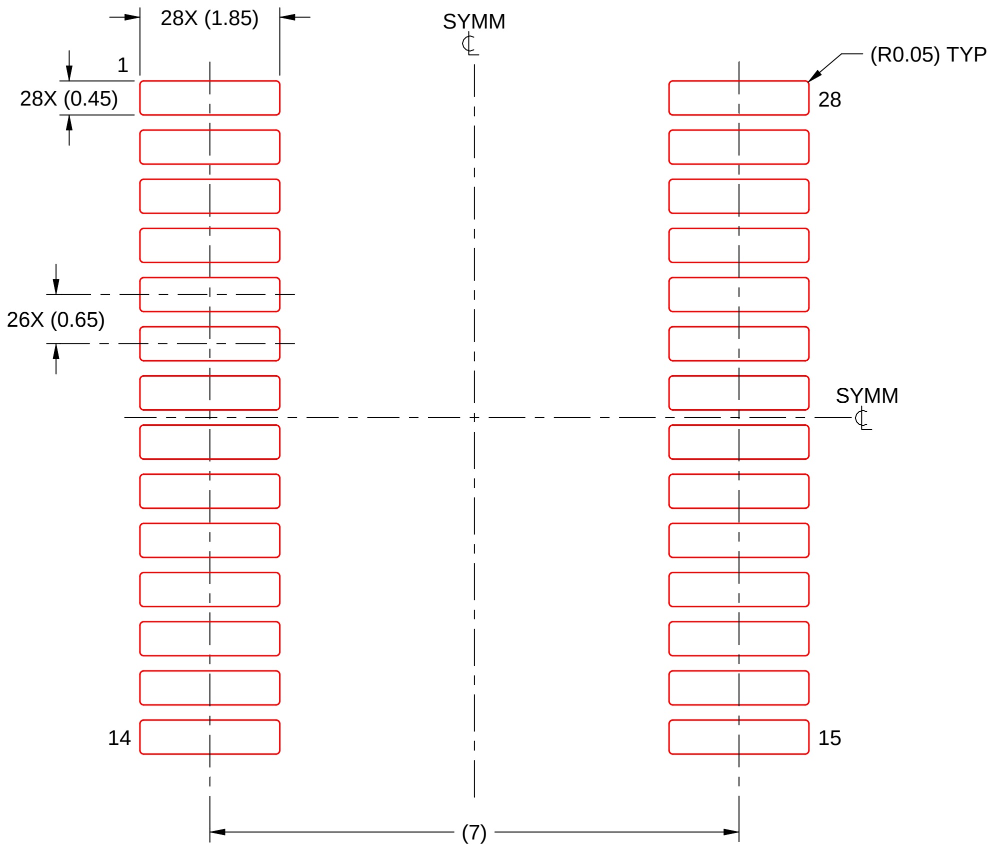


SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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