



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	PACKAGE ORDERING MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8581	TSSOP-16	PW	–40°C to +85°C	D8581I	DAC8581IPW	Tube, 90-Piece
					DAC8581IPWR	Tape and Reel, 2000-Piece

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		UNIT
AV _{DD} or DV _{DD} to AV _{SS}		–0.3 V to 12 V
Digital input voltage to AV _{SS}		–0.3 V to 12 V
V _{OUT} or V _{REF} to AV _{SS}		–0.3 V to 12 V
DGND and AGND to AV _{SS}		–0.3 V to 6 V
Operating temperature range		–40°C to +85°C
Storage temperature range		–65°C to +150°C
Junction temperature range (T _J max)		+150°C
Power dissipation	Thermal impedance (θ _{JA})	118°C/W
	Thermal impedance (θ _{JC})	29°C/W

- (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $+AV_{DD} = +5\text{ V}$, $-AV_{DD} = -5\text{ V}$, $DV_{DD} = +5\text{ V}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	DAC8581			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE					
Resolution		16			Bits
Linearity error	V _{REF} = 4.096 V	±0.03			±0.1 %FS
Differential linearity error		±0.25			±0.5 LSB
Gain error		1	2	3	%FS
Gain drift		±5			ppm/°C
Bipolar zero error		−5			±25 mV
Bipolar zero drift		±20			μV/°C
Total drift		±10			ppm/°C
OUTPUT CHARACTERISTICS					
Voltage output	V _{REF} up to 5.5 V, when AV _{DD} = 6 V, AV _{SS} = −6 V	−V _{REF}	V _{REF}		V
Output impedance		1			Ω
Maximum output current		±25			mA
Settling time	C _L < 200 pF, R _L = 2 kΩ, to 0.1% FS, 8-V step	0.65			μs
	To 0.003% FS	1			
Slew rate ⁽¹⁾		35			V/μs
Code change glitch	1 LSB change around major carry	0.5			nV-S
Overshoot	Full-scale change	50			mV
Digital feedthrough ⁽²⁾		0.5			nV-S
SNR	Digital sine wave input, f _{OUT} = 1 kHz, BW = 10 kHz, 2-MSPS update rate	108			dB
THD	Digital sine wave input, f _{OUT} = 20 kHz, 8-V _{PP} output, 2-MSPS update rate	−72			dB
Output voltage noise	0.1 Hz to 10 Hz	25			μV _{PP}
	At 10-kHz offset frequency	25			nV/√Hz
	At 100-kHz offset frequency	20			nV/√Hz
Power supply rejection	VDD varies ±10%	0.75			mV/V
REFERENCE					
Reference input bandwidth	Large signal: 2-V _{PP} sine wave on 4 V DC	3			MHz
	Small signal: 100-mV _{PP} sine wave on 4 V DC	10			MHz
Reference input voltage range		3	AV _{DD}		V
Reference input impedance		5			kΩ
Reference input capacitance		5			pF
DIGITAL INPUTS					
V _{IH}		0.7 x DV _{DD}			V
V _{IL}		GND	0.3 x DV _{DD}		
Input current		±1			μA
Input capacitance		10			pF
Power-on delay	From V _{DD} high to $\overline{\text{CS}}$ low	20			μs

(1) Slew rate is measured from 10% to 90% of transition when the output changes from 0 to full-scale.

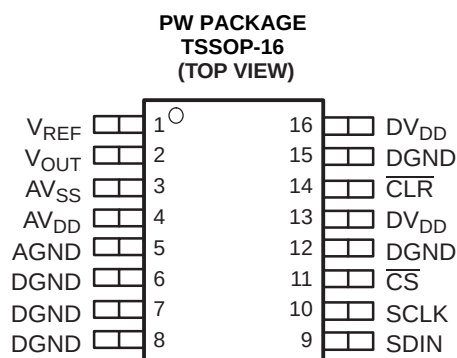
(2) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change, $\overline{CS}$ is held high, and while SCLK and SDIN signals are toggled.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $+AV_{DD} = +5\text{ V}$, $-AV_{DD} = -5\text{ V}$, $DV_{DD} = +5\text{ V}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	DAC8581			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
+AV _{DD}		4.0	5	6.0	V
−AV _{DD}		−4.0	−5	−6.0	V
DV _{DD}		1.8		AV _{DD}	V
I _{DVDD}			10	20	μA
I _{DD}	I _{REF} and IDV _{DD} included		17	24	mA
I _{SS}			−23	−32	mA
TEMPERATURE RANGE					
Specified performance		−40		+85	°C

PIN CONFIGURATION



TERMINAL FUNCTIONS

TERMINAL		
NAME	NO.	
V_{REF}	1	Reference input voltage.
V_{OUT}	2	DAC output voltage. Output swing is $\pm V_{REF}$.
AV_{SS}	3	Negative analog supply voltage, tie to -5 V.
AV_{DD}	4	Positive analog supply voltage, tie to +5 V.
AGND	5	The ground reference point of all analog circuitry of the device. Tie to 0 V.
DGND	6, 7, 8, 15	Tie to DGND to ensure correct operation.
SDIN	9	Digital input, serial data. Ignored when $\overline{CS}$ is high.
SCLK	10	Digital input, serial bit clock. Ignored when $\overline{CS}$ is high.
$\overline{CS}$	11	Digital input. Chip Select ($\overline{CS}$) signal. Active low. When $\overline{CS}$ is high, SCLK and SDI are ignored. When $\overline{CS}$ is low, data can be transferred into the device.
DGND	12	Ground reference for digital circuitry. Tie to 0 V.
DV_{DD}	13	Positive digital supply, 1.8 V–5.5 V compatible.
$\overline{CLR}$	14	Digital input for forcing the output to midscale. Active low. When pin $\overline{CLR}$ is low during 16 th SCLK following the falling edge of $\overline{CS}$, the falling edge of 16 th SCLK sets DAC Latch to midcode, and the DAC output to 0 V. When pin $\overline{CLR}$ is High, the falling edge of 16 th SCLK updates DAC latch with the value of input shift register, and changes DAC output to corresponding level.
DV_{DD}	16	Tie to DV_{DD} to ensure correct operation.

TIMING REQUIREMENTS⁽¹⁾

PARAMETER		MIN	MAX	UNIT
t_{SCK}	SCLK period	20		ns
t_{WSCK}	SCLK high or low time	10		ns
t_{Lead}	Delay from falling $\overline{CS}$ to first rising SCLK	20		ns
t_{TD}	$\overline{CS}$ High between two active Periods	20		ns
t_{SU}	Data setup time (Input)	5		ns
t_{HI}	Data hold time (input)	5		ns
t_R	Rise time		30	ns
t_F	Fall time		30	ns
t_{WAIT}	Delay from 16th falling edge of SCLK to $\overline{CS}$ low	100		ns
t_{UPDAC}	Delay from 16th falling edge of SCLK to DAC output	1		μ s
	V_{DD} High to $\overline{CS}$ Low (power-up delay)	100		μ s

(1) Assured by design. Not production tested.

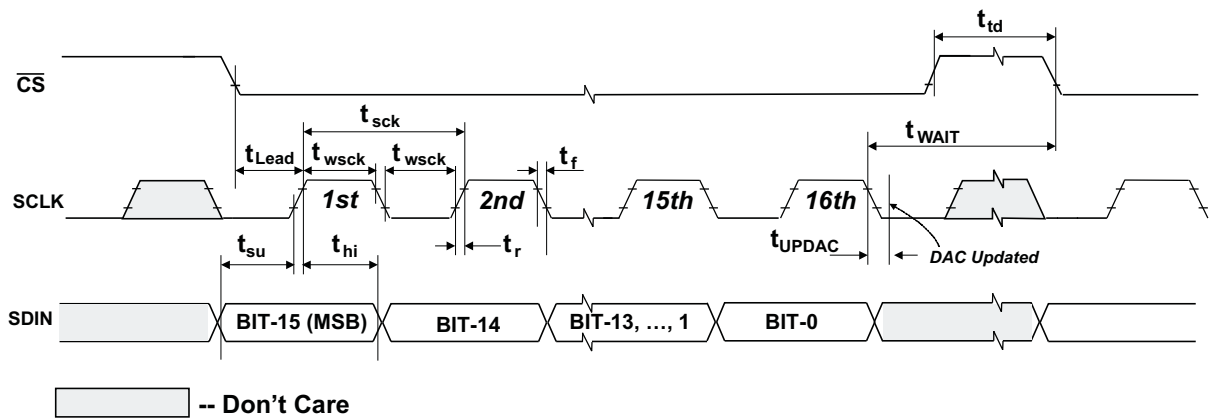


Figure 1. DAC8581 Timing Diagram

TYPICAL CHARACTERISTICS

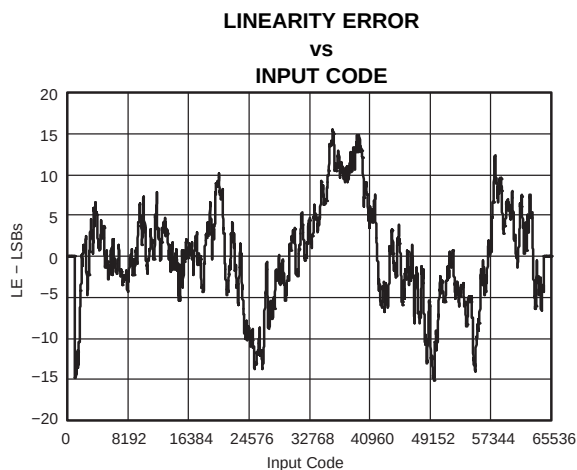


Figure 2.

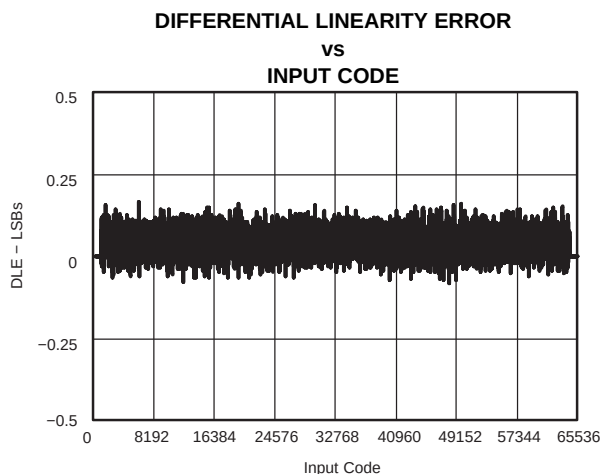


Figure 3.

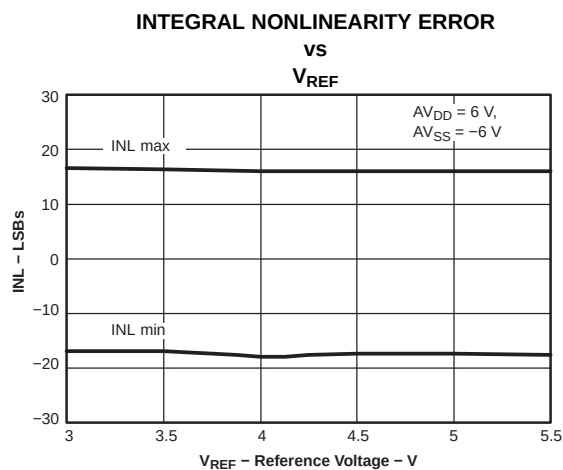


Figure 4.

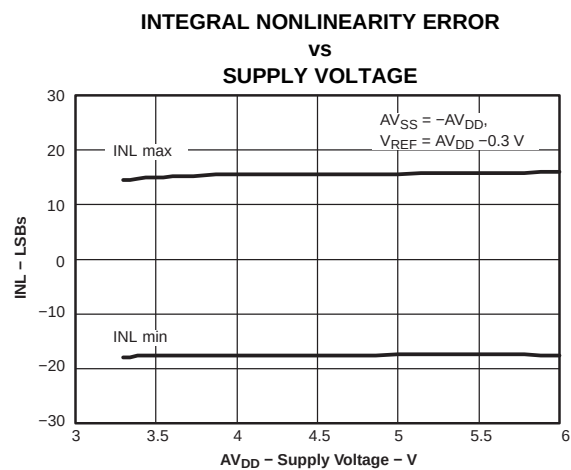


Figure 5.

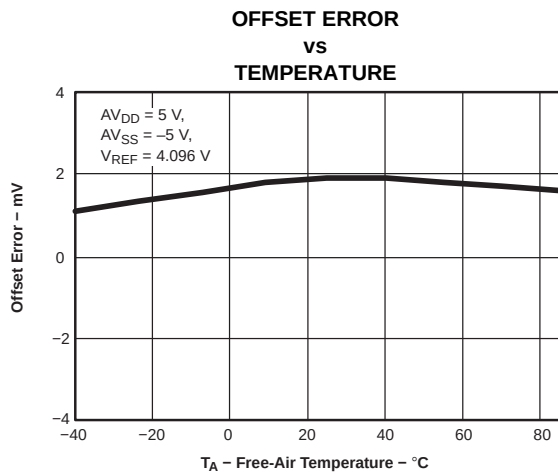


Figure 6.

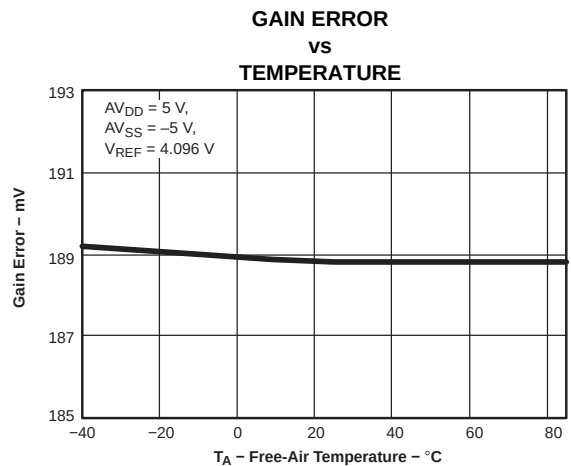


Figure 7.

TYPICAL CHARACTERISTICS (continued)

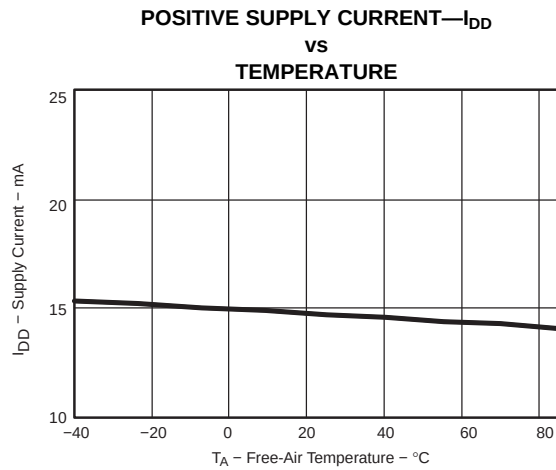


Figure 8.

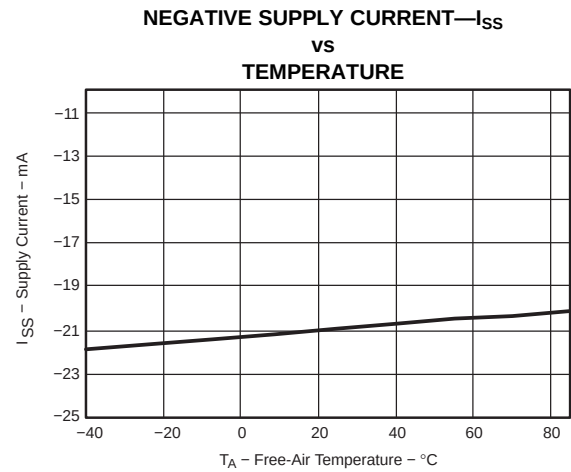


Figure 9.

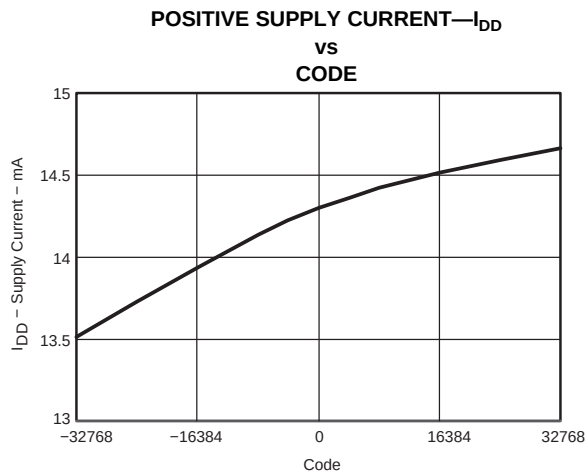


Figure 10.

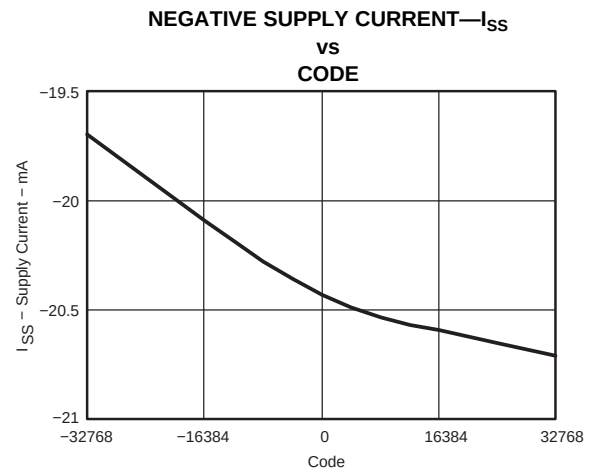


Figure 11.

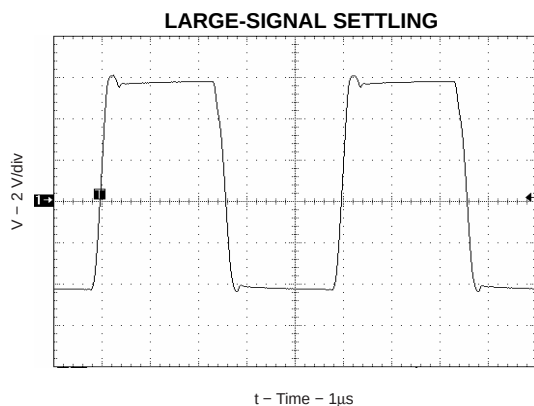


Figure 12.

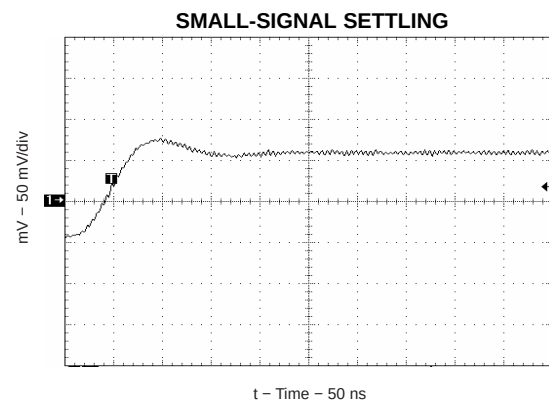


Figure 13.

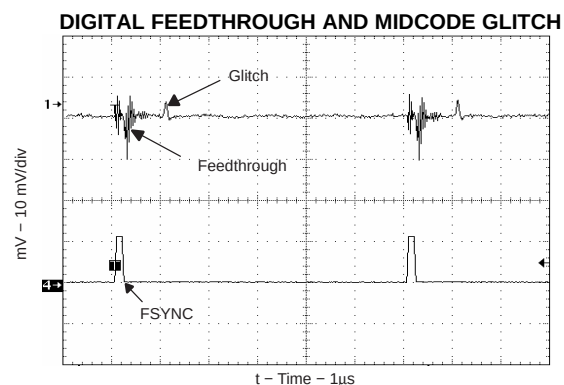
TYPICAL CHARACTERISTICS (continued)

Figure 14.

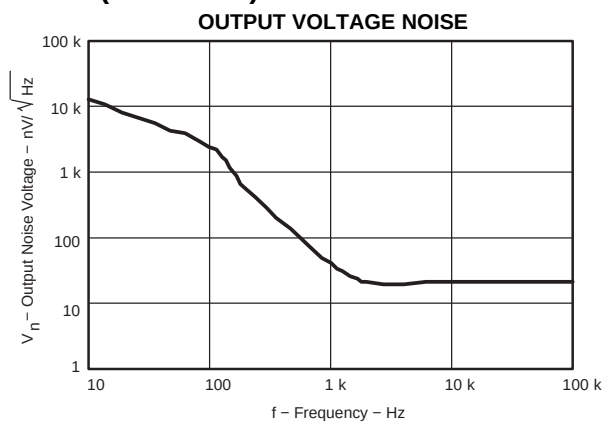


Figure 15.

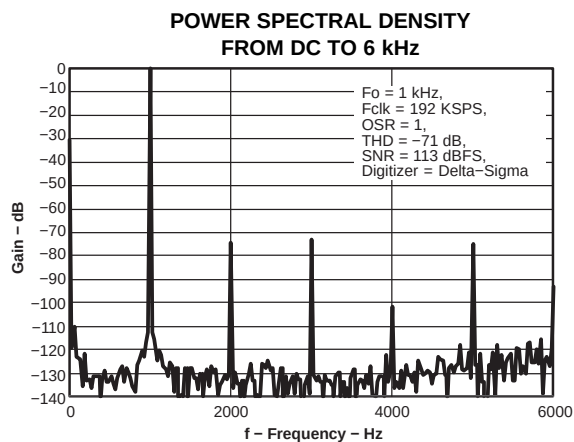


Figure 16.

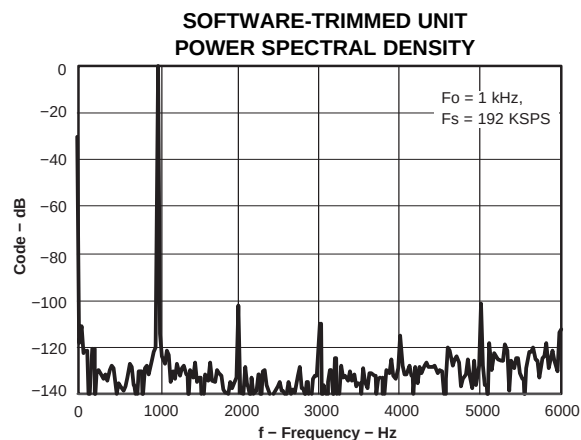


Figure 17.

**SOFTWARE-TRIMMED UNIT
LINEARITY ERROR
vs
INPUT CODE**

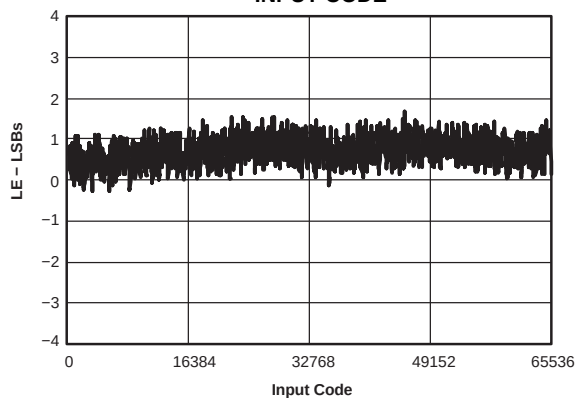


Figure 18.

THEORY OF OPERATION

The DAC8581 uses a proprietary, monotonic, high-speed resistor string architecture. The 16-bit input data are coded in twos complement, MSB-first format and transmitted using a 3-wire serial interface. The serial interface sends the input data to the DAC latch. The digital data are then decoded to select a tap voltage of the resistor string. The resistor string output is sent to a high-performance output amplifier. The output buffer has bipolar (± 5 V) swing capability on a 600- Ω , 200-pF load. The resistor string DAC architecture provides exceptional differential linearity and temperature stability whereas the output buffer provides fast-settling, low-glitch, and exceptionally low idle-channel noise. The DAC8581 settles within 1 μ s for large input signals. Exceptionally low glitch (0.5 nV-s) is attainable for small-signal, code-to-code output changes. The resistor string architecture also provides code-independent power consumption and code-independent settling time. The DAC8581 resistor string needs an external reference voltage to set the output voltage range of the DAC. To aid fast settling, V_{REF} input is internally buffered.

Supply Pins

The DAC8581 uses ± 5 -V analog power supplies (AV_{DD} , AV_{SS}) and a 1.8-V to 5.5-V digital supply (DV_{DD}). Analog and digital ground pins (AGND and DGND) are also provided. For low-noise operation, analog and digital power and ground pins should be separated. Sufficient bypass capacitors, at least 1 μ F, should be placed between AV_{DD} and AV_{SS} , AV_{SS} and DGND, and DV_{DD} and DGND pins. Series inductors are *not* recommended on the supply paths. The digital input pins should not exceed the ground potential during power up. During power up, AGND and DGND are first applied with all digital inputs and the reference input kept at 0 V. Then, AV_{DD} , DV_{DD} , AV_{SS} , and V_{REF} should be applied together. Care should be taken to avoid applying V_{REF} before AV_{DD} and AV_{SS} . All digital pins must be kept at ground potential before power up.

Reference Input Voltage

The reference input pin V_{REF} is typically tied to a +3.3-V, +4.096-V, or +5.0-V external reference. A bypass capacitor (0.1 μ F or less) is recommended, depending on the load-driving capability of the voltage reference. To reduce crosstalk and improve settling time, the V_{REF} pin is internally buffered by a high-performance amplifier. The V_{REF} pin has constant 5-k Ω impedance to AGND. The output range of the DAC8581 is equal to $\pm V_{REF}$ voltage. The V_{REF} pin should be powered at the same time, or after the supply pins. [REF3133](#) and [REF3140](#) are recommended to set the DAC8581 output range to ± 3.3 V and ± 4.096 V, respectively.

Output Voltage

The input data format is in twos-complement format as shown in [Table 1](#). The DAC8581 uses a high-performance, bipolar output buffer capable of driving a 600- Ω , 200-pF load with fast 0.65- μ s settling. The buffer has exceptional noise performance (20 nV/ $\sqrt{\text{Hz}}$) and fast slew rate (35 V/ μ s). The small-signal settling time is under 300 ns, allowing update rates up to 3 MSPS. Loads of 50 Ω or 75 Ω could be driven as long as output current does not exceed ± 25 mA continuously. Long cables, up to 1 nF in capacitance, can be driven without the use of external buffers. To aid stability under large capacitive loads (>1 nF), a small series resistor can be used at the output.

Table 1. Data Format

DAC OUTPUT	DIGITAL CODE	
	BINARY	HEX
$+V_{REF}$	0111111111111111	7FFF
$+V_{REF}/2$	0100000000000000	4000
0	0000000000000000	0000
$-V_{REF}/2$	1011111111111111	BFFF
$-V_{REF}$	1000000000000000	8000

Glitch area is low at 0.5 nV-s, with peak glitch amplitude under 10 mV, and the glitch duration under 100 ns. Low glitch is obtained for code-to-code (small signal) changes across the entire transfer function of the device. For large signals, settling characteristics of the reference and output amplifiers are observed in terms of overshoot and undershoot.

Combined with ± 5 -V output range, and extremely good noise performance, the outstanding differential linearity performance of this device becomes significant. That is, each DAC step can be clearly observed at the DAC output, without being corrupted by wideband noise.

SERIAL INTERFACE

The DAC8581 serial interface consists of the serial data input pin SDIN, bit clock pin SCLK, and chip-select pin, CS. The serial interface is designed to support the industry standard SPI interface up to 50 MHz. The serial inputs are 1.8-V to 5.5-V logic compatible.

$\overline{\text{CS}}$ operates as an active-low, chip-select signal. The falling edge of $\overline{\text{CS}}$ initiates the data transfer. Each rising edge of SCLK following the falling edge of $\overline{\text{CS}}$ shifts the SDIN data into a 16-bit shift register, MSB-first. At the 16th rising edge of SCLK, the shift register becomes full and the DAC data updates on the falling edge that follows the 16th rising edge. After the data update, further clocking gets ignored. The sequence restarts at the next falling edge of CS. If the CS is brought high before the DAC data are updated, the data are ignored. See the timing diagram (Figure 1) for details.

Pin $\overline{\text{CLR}}$

Pin $\overline{\text{CLR}}$ is implemented to set the DAC output to 0 V. When the $\overline{\text{CS}}$ pin is low during the 16th SCLK cycle following the falling edge of $\overline{\text{CS}}$, the falling edge of the 16th SCLK sets the DAC latch to midcode, and the DAC output to 0 V. If the CLR pin is high during the 16th clock, the falling edge of the 16th clock updates the DAC latch with the input data. Therefore, if the CLR pin is brought back to High from Low during serial communication, the DAC output stays at 0 V until the falling edge of the next 16th clock is received. The CLR pin is active low. CLR low does not affect the serial data transfer. The serial data input does not get interrupted or lost while the output is set at midscale.

SCLK

This digital input pin is the serial bit-clock. Data are clocked into the device at the rising edge of SCLK.

$\overline{\text{CS}}$

This digital input pin is the chip-select signal. When $\overline{\text{CS}}$ is low, the serial port is enabled and data can be transferred into the device. When CS is high, all SCLK and SDIN signals are ignored.

SDIN

This digital input is the serial data input. Serial data are shifted on the rising edge of the SCLK when $\overline{\text{CS}}$ is low.

APPLICATION INFORMATION

IMPROVING DAC8581 LINEARITY USING EXTERNAL CALIBRATION

At output frequencies up to 50 kHz, DAC8581 linearity error and total harmonic distortion are dominated by resistor mismatches in the string. These resistor mismatches are fairly insensitive to temperature and aging effects and also to reference voltage changes. Therefore, it is possible to use a piece-wise linear (PWL) approximation to cancel linearity errors, and the calibration remains effective for different supply and V_{REF} voltages, etc. The cancellation of linearity errors also improves the total harmonic distortion (THD) performance. It is possible to improve the integral linearity errors from ± 25 LSB to ± 1 LSB and the THD from -70 dB to almost -98 dB (see [Figure 17](#) and [Figure 18](#)). The improvements are at the expense of $\sim 2\times$ DNL deterioration, which is not critical for the generation of large-signal waveforms.

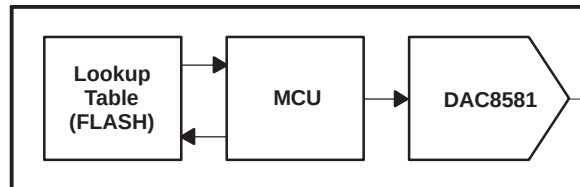


Figure 19. A Simple Printed-Circuit Board Scheme for Calibrated Use of DAC8581

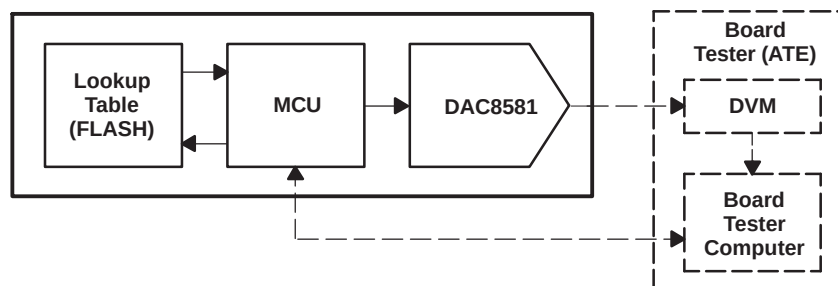


Figure 20. Production Test Setup for a DAC8581 Board With Calibration

The PWL calibration scheme uses a DAC8581 and a microcontroller unit (MCU) with flash memory, on a printed-circuit board as seen in [Figure 19](#). Calibration is done during board test, and the calibration coefficients are stored permanently in flash memory as seen in [Figure 20](#). An automated board tester is assumed to have a precision digital voltmeter (DVM) and a tester computer. The test flow for a 1024-segment, piece-wise linear calibration is as follows:

1. Use the tester computer to load software into the MCU to ramp the DAC8581 and:
 - Take a reading at each step after a short wait time
 - Store 65,536 readings in the tester computer volatile memory
2. Use the tester computer to:
 - Search the 65,536-point capture data and find the actual DAC8581 codes which would generate ideal DAC outputs for DAC input codes 0, 64, 128, 192, ...
 - Store these actual codes in the onboard microcontroller's flash memory in a 1025-point array called COEFF[].
3. Use the tester computer to program the MCU such that, when the end-user provides new 16-bit input data D0 to the MCU:
 - The 10 MSBs of D0 directly index the array COEFF[].
 - The content of indexed memory of COEFF[] and the content of the next higher memory location are placed in variables I1 and I2.
 - The six LSBs of the user data D0 with two variables I1 and I2 are used for computing [Equation 1](#) (see [Figure 21](#)).
 - Instead of D0, I0 is loaded to DAC8581

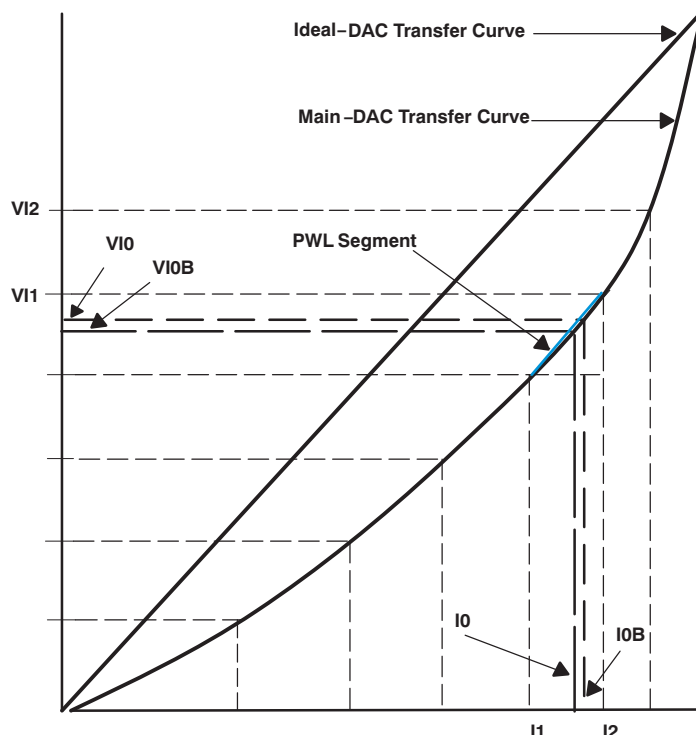


Figure 21. The Geometry Behind the PWL Calibration

$$I_0 = \frac{I_1 + (I_2 - I_1)(D_0 - VI_1)}{VI_2 - VI_1} \quad (1)$$

Where both x-axis and y-axis are normalized from 0 to 65535, and:

VI0: Desired ideal DAC voltage corresponding to input code D0.

VI0B: DAC8581 output voltage, which approximates VI0 after PWL calibration. This is the actual DAC8581 output for input code D0 after PWL calibration.

I0: DAC8581 code generating VI0B, an approximation to the desired voltage VI0. This is actual code loaded into DAC latch for input code D0, after PWL calibration.

I0B: DAC8581 code, which generates output VI0. This code is approximated by the N-segment PWL calibration.

I1: Contents of memory COEFF[], addressed by the 10 MSBs of user input code D0.

I2: Contents of the next memory location in COEFF[].

VI1: DAC8581 output voltage corresponding to code I1. Notice that (D0–VI1) is nothing but the six LSBs of the input code D0, given that the y-axis is normalized from 0 to 65,536.

VI2: DAC8581 output voltage corresponding to code I2. Notice that (VI2–VI1) is always equal to number 64, given that the y-axis is normalized from 0 to 65,536. Division becomes a 6-bit arithmetic right shift.

Other similar PWL calibration implementations exist. This particular algorithm does not need digital division, and it does not accumulate measurement errors at each segment.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August, 2005) to Revision B	Page
• Updated document format to current stylistic standards	1
• Deleted lead temperature specifications from <i>Absolute Maximum Ratings</i> table	2
• Deleted footnote 1 from <i>Electrical Characteristics</i> table	3
• Revised test conditions for voltage output specification	3
Changes from Revision B (December 2009) to Revision C	Page
• Changed "rail-to-rail" to "bipolar"	1
• Changed "rail-to-rail" to "bipolar"	9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8581IPW	NRND	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	D8581I
DAC8581IPW.B	NRND	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	D8581I
DAC8581IPWR	NRND	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	D8581I
DAC8581IPWR.B	NRND	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	D8581I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

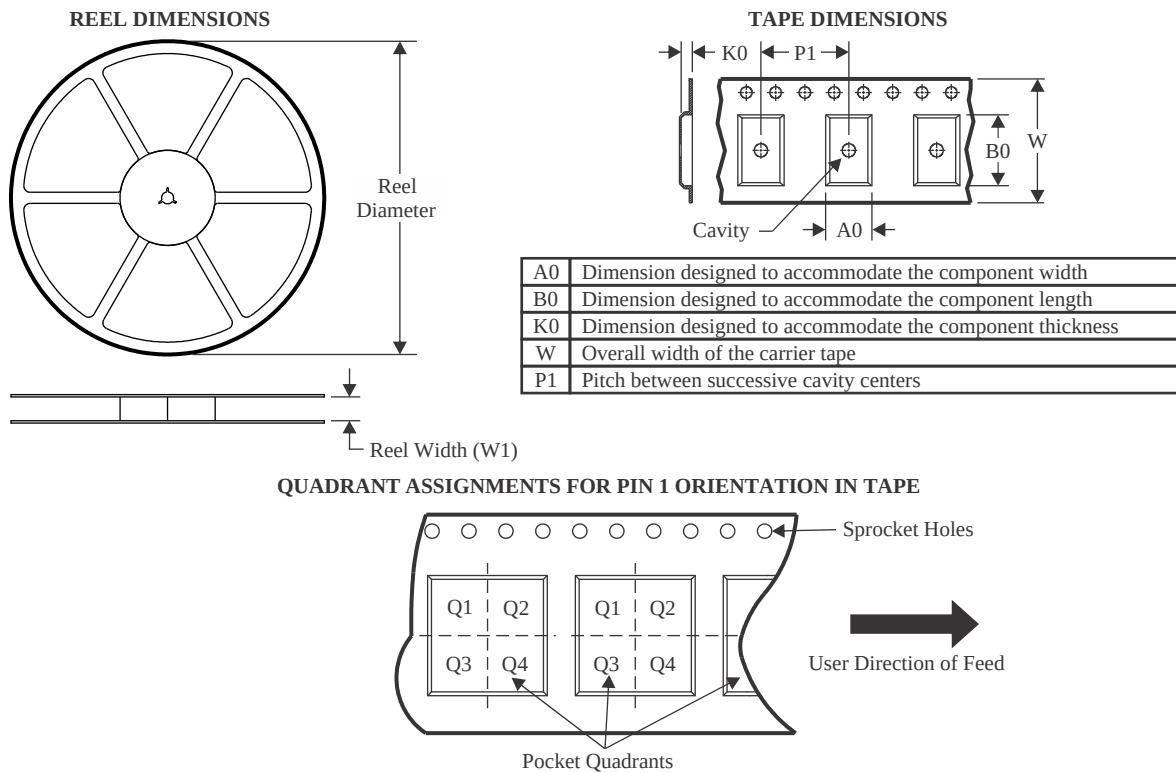
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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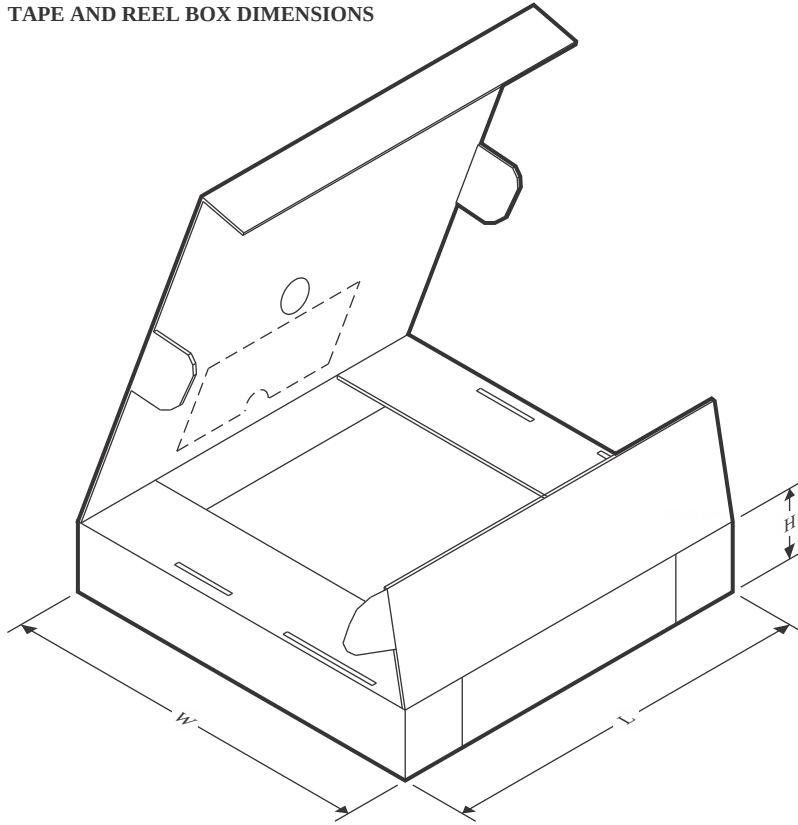
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8581IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

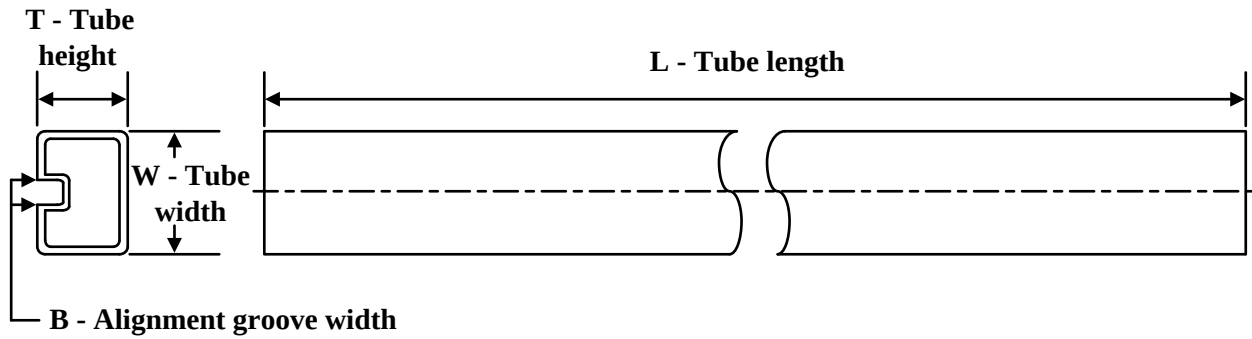
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

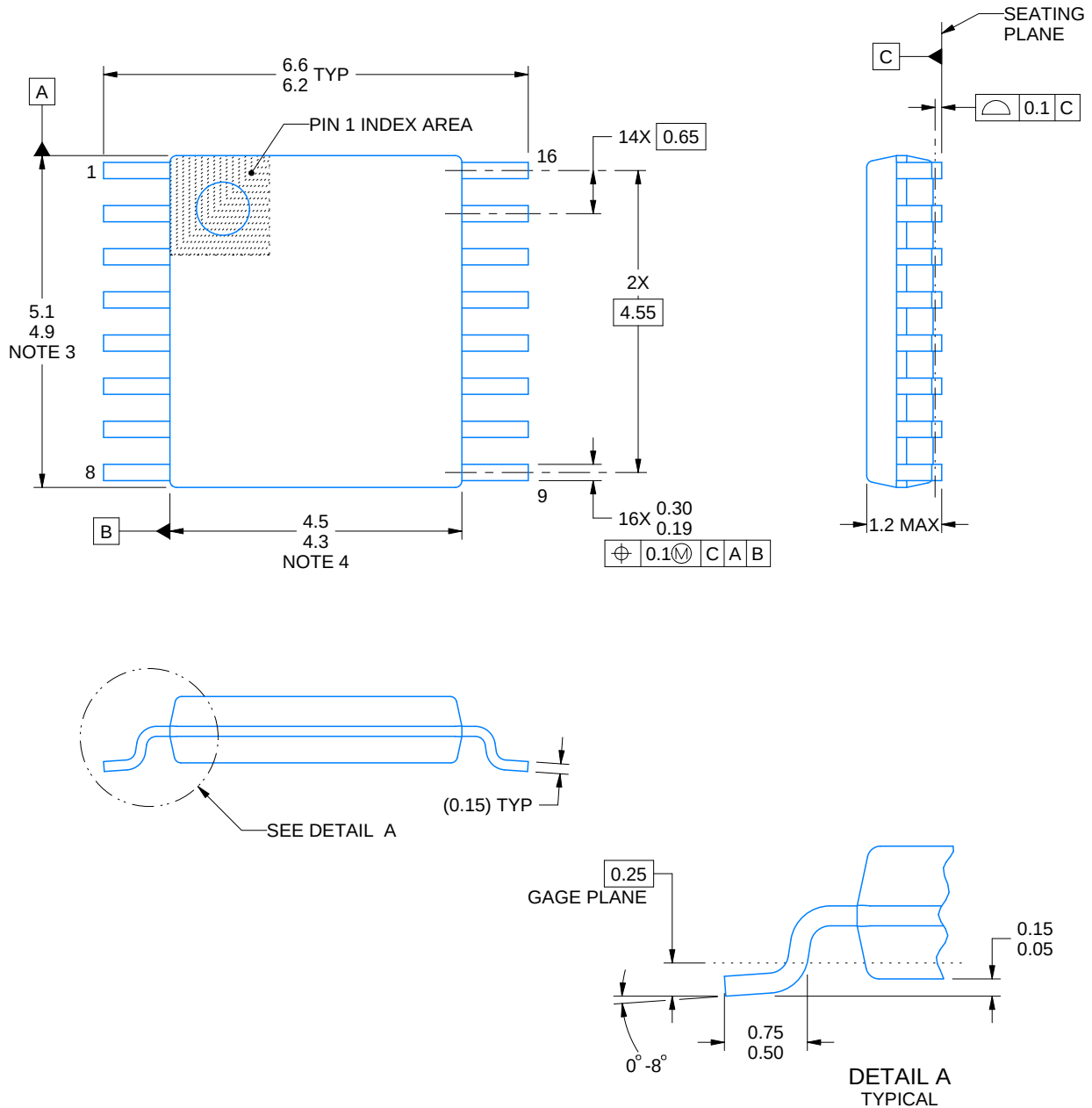
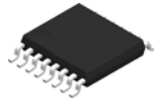
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8581IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC8581IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC8581IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5



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NOTES:

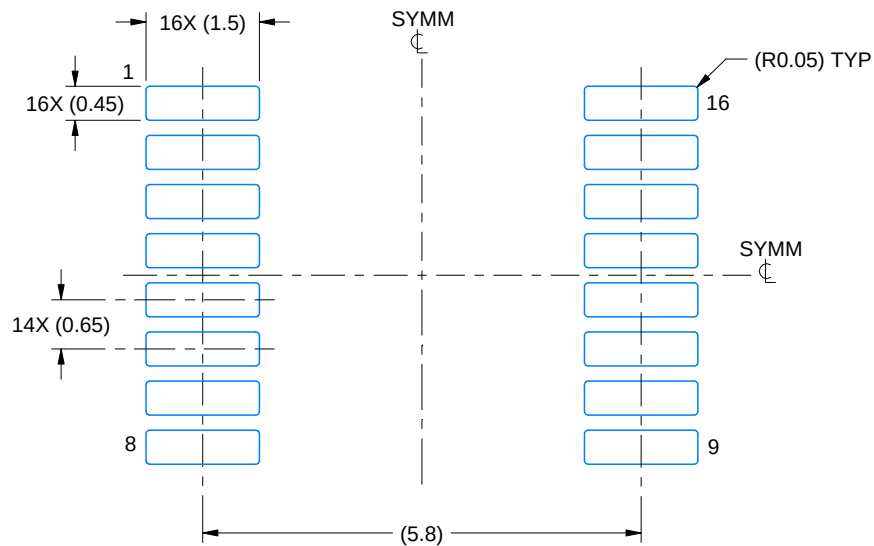
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

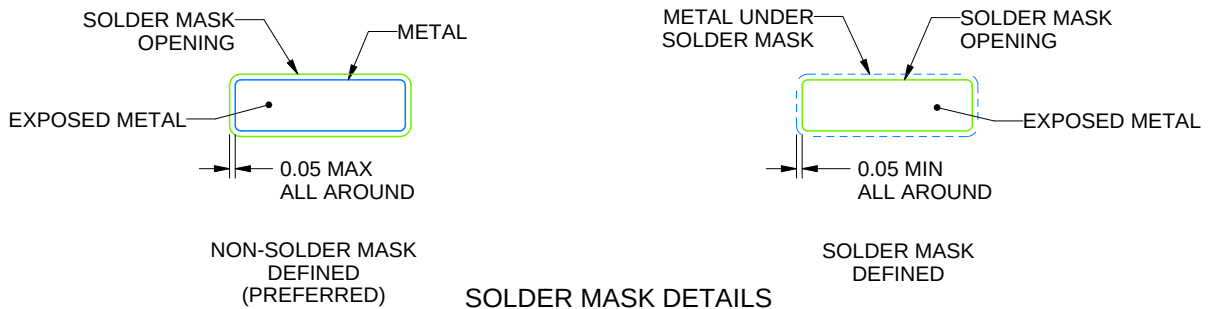
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

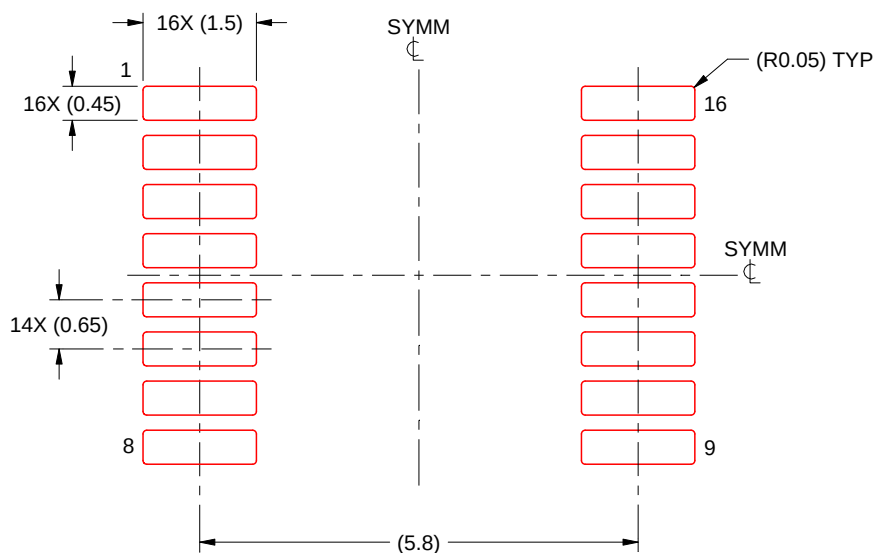
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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