TEXAS INSTRUMENTS
DAC5311, DAC6311, DAC7311
JAJS498D – AUGUST 2008 – REVISED AUGUST 2023

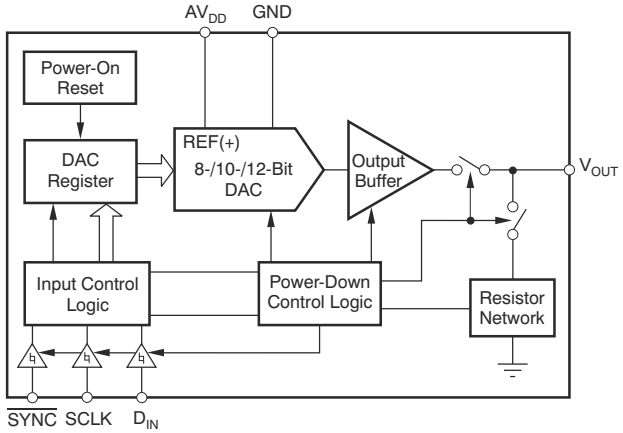
DACx311 2V~5.5V、80µA、8 ビット、10 ビット、12 ビット、低消費電力、シングルチャネル、D/A コンバータ、SC70 パッケージ封止

1 特長

- 相対精度:
  - 0.25LSB INL (DAC5311:8 ビット)
  - 0.5LSB INL (DAC6311:10 ビット)
  - 1LSB INL (DAC7311:12 ビット)
- マイクロパワー動作:80µA (2.0V 時)
- パワーダウン:5V で 0.5µA、2.0V で 0.1µA
- 広い電源電圧範囲:2.0V～5.5V
- ゼロ・スケールへのパワーオン・リセット
- ストレート・バイナリ・データ・フォーマット
- シュミット・トリガ入力を持つ低消費電力シリアル・インターフェイス:最高 50MHz
- レール・ツー・レール動作のオンチップ出力バッファ・アンプ
- $\overline{\text{SYNC}}$ 割り込み機能
- 拡張温度範囲:–40℃～+125℃
- 小型の 6 ピン SC70 パッケージで供給されるピン互換のファミリ

2 アプリケーション

- 携帯型のバッテリ駆動計測機器
- 4mA～20mA のループ電源アプリケーション
- プロセス制御および産業用オートメーション
- プログラム可能な電圧源および電流源



概略回路図

3 概要

8 ビット DAC5311、10 ビット DAC6311、12 ビット DAC7311 (DACx311) は、低消費電力、シングル・チャネルの電圧出力 D/A コンバータ (DAC) です。通常動作時の消費電力が低いため (5V で 0.55mW、パワーダウン・モードでは 2.5µW に低下)、DACx311 は携帯型のバッテリ駆動アプリケーションに最適です。

これらのデバイスは設計上単調で、優れた直線性を備えており、不要なコード間過渡電圧が最小限に抑えられているうえに、ピン互換のファミリ内で簡単にアップグレードできます。すべてのデバイスは、最高 50MHz のクロック・レートで動作する汎用 3 ワイヤ・シリアル・インターフェイスにより、SPI、QSPI、Microwire の規格、およびデジタル・シグナル・プロセッサ (DSP) との接続に対応しています。

すべてのデバイスは、出力範囲を設定するための基準電圧として外部電源を使用しています。このデバイスにはパワーオン・リセット (POR) 回路が組み込まれており、DAC 出力が 0V で起動され、デバイスへの有効な書き込みが発生するまで 0V に維持されます。DACx311 には、シリアル・インターフェイスでアクセス可能なパワーダウン機能が含まれており、パワーダウン・モードではデバイスの消費電流を 2.0V で 0.1µA にまで低減できます。

これらのデバイスは DAC8311 および DAC8411 とピン互換であり、8 ビット、10 ビット、12 ビットの分解能から 14 ビット、16 ビットの分解能に簡単にアップグレードできます。すべてのデバイスは小型の 6 ピン SC70 (SOT) パッケージで供給されます。このパッケージは、ファミリ内でピン互換および機能互換の柔軟なドロップイン DAC を提供し、拡張温度範囲 -40℃～+125℃で動作します

製品情報(1)

部品番号(2)	分解能	パッケージ・サイズ (3)
DAC7311	12 ビット	DCK (SC70、6) 2mm × 1.5mm
DAC6311	10 ビット	
DAC5311	8 ビット	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
(2) 製品比較表を参照してください。
(3) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (July 2015) to Revision D (August 2023) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....1
- 本体サイズではなくパッケージ・サイズを示すように「製品情報」表を変更し、デバイス間の違いを示す項目を追加.....1
- Changed power dissipation max value for normal mode at AV_{DD} = 3.6 V to 5.5 V from 0.88 mW to 0.99 mW in *Electrical Characteristics*.....5
- Changed I_{DD} max value for normal mode at AV_{DD} = 3.6 V to 5.5 V from 160 µA to 180 µA in *Electrical Characteristics*.....5

Changes from Revision B (May 2013) to Revision C (July 2015) **Page**

- 「ESD 定格」表、および「機能説明」、「デバイスの機能モード」、「アプリケーションと実装」、「電源に関する推奨事項」、「レイアウト」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」の各セクションを追加.....1
- Added *Device Comparison* section and moved existing tables to this new section.....3
- Moved *Operating Temperature* parameter from *Electrical Characteristics* table to *Recommended Operating Conditions* table.....4
- Deleted *Parameter Definitions* section; definitions moved to new *Glossary* section.....33

Changes from Revision A (August 2011) to Revision B (May 2013) **Page**

- データシート全体にわたってすべての 1.8V を 2.0V に変更.....1
- Deleted the 1.8-V Typical Characteristics section.....8
- Changed X-axis for Figure 7-36, Power-Supply Current vs Power-Supply Voltage.....8
- Changed X-axis for Figure 7-37, Power-Down Current vs Power-Supply Voltage.....8

Changes from Revision * (August, 2008) to Revision A (August, 2011) **Page**

- Changed specifications and test conditions for input low voltage parameter.....5
- Changed specifications and test conditions for input high voltage parameter.....5

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5 Device Comparison

表 5-1. Related Devices

RELATED DEVICES	16-BIT	14-BIT	12-BIT	10-BIT	8-BIT
Pin and Function Compatible	DAC8411	DAC8311	DAC7311	DAC6311	DAC5311

表 5-2. Relative Accuracy and Differential Nonlinearity

DEVICE	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)
DAC5311	±0.25	±0.25
DAC6311	±0.5	±0.5
DAC7311	±1	±1

6 Pin Configuration and Functions

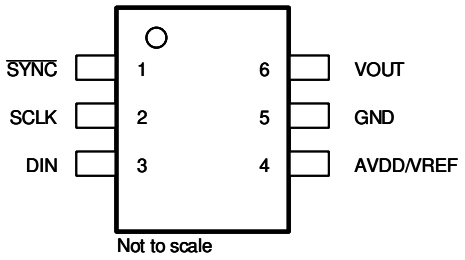

図 6-1. DCK Package, 6-Pin SC70 (Top View)

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AV_{DD}/V_{REF}	4	Input	Power supply input, 2.0 V to 5.5 V.
D_{IN}	3	Input	Serial Data Input. Data are clocked into the 16-bit input shift register on the falling edge of the serial clock input.
GND	5	—	Ground reference point for all circuitry on the part.
SCLK	2	Input	Serial clock input. Data are transferred at rates up to 50 MHz.
$\overline{SYNC}$	1	Input	Level-triggered control input (active low). This pin is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, the input shift register is enabled and data are transferred in on the falling edges of the following clocks. The DAC is updated following 16th clock cycle, unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DACx311. See the *SYNC Interrupt* section for more details.
V_{OUT}	6	Output	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Voltage	AV_{DD} to GND	–0.3	+6	V
		Digital input voltage to GND	–0.3	$+AV_{DD}$ + 0.3	V
		V_{OUT} to GND	–0.3	$+AV_{DD}$ + 0.3	V
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating temperature	–40		125	°C
AV_{DD}	Supply voltage	2		5.5	V

7.4 Thermal Information

THERMAL METRIC(1)		DACx311 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics* application note.

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7.5 Electrical Characteristics

at AV_{DD} = 2.0 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, and T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC5311	Resolution		8			Bits
DAC6311			10			Bits
DAC7311			12			Bits
DAC5311	Relative accuracy	Measured by the line passing through codes 3 and 252		±0.01	±0.25	LSB
DAC6311		Measured by the line passing through codes 12 and 1012		±0.06	±0.5	LSB
DAC7311		Measured by the line passing through codes 30 and 4050		±0.3	±1	LSB
DAC5311	Differential nonlinearity			±0.01	±0.25	LSB
DAC6311				±0.03	±0.5	LSB
DAC7311				±0.2	±1	LSB
Offset error		Measured by the line passing through two codes(2)		±0.05	±4	mV
Offset error drift				3		µV/°C
Zero code error		All zeros loaded to the DAC register		0.2		mV
Full-scale error		All ones loaded to DAC register		0.04	0.2	% of FSR
Gain error				0.05	±0.15	% of FSR
Gain temperature coefficient		AV_{DD} = 5 V		±0.5		ppm of FSR/°C
		AV_{DD} = 2.0 V		±1.5		
OUTPUT CHARACTERISTICS						
Output voltage range			0		AV_{DD}	V
Output voltage settling time(3)		R_L = 2 kΩ, C_L = 200 pF, AV_{DD} = 5 V, 1/4 scale to 3/4 scale		6	10	µs
		R_L = 2 MΩ, C_L = 470 pF		12		µs
Slew rate				0.7		V/µs
Capacitive load stability		R_L = ∞		470		pF
		R_L = 2 kΩ		1000		pF
Code change glitch impulse		1 LSB change around major carry		0.5		nV-s
Digital feedthrough				0.5		nV-s
Power-on glitch impulse		R_L = 2 kΩ, C_L = 200 pF, AV_{DD} = 5 V		17		mV
DC output impedance				0.5		Ω
Short circuit current		AV_{DD} = 5 V		50		mA
		AV_{DD} = 3 V		20		mA
Power-up time		Coming out of power-down mode		50		µs
AC PERFORMANCE						
SNR		T_A = 25°C, BW = 20 kHz, 12-bit level, AV_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation		81		dB
THD				–65		dB
SFDR				65		dB
SINAD				65		dB

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7.5 Electrical Characteristics (continued)

at AV_{DD} = 2.0 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, and T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC output noise density(4)		T_A = 25°C, at zero-scale input, f_{OUT} = 1 kHz, AV_{DD} = 5 V			17		nV/√Hz
		T_A = 25°C, at mid-code input, f_{OUT} = 1 kHz, AV_{DD} = 5 V			110		nV/√Hz
DAC output noise(5)		T_A= +25°C, at mid-code input, 0.1 Hz to 10 Hz, AV_{DD} = 5 V			3		μV_{PP}
LOGIC INPUTS(3)							
Input current						±1	µA
$V_{IN}L$, Input low voltage		AV_{DD} = 2.7 V to 5.5 V				0.3 × AV_{DD}	V
		AV_{DD} = 2.0 V to 2.7 V				0.1 × AV_{DD}	V
$V_{IN}H$, Input high voltage		AV_{DD} = 2.7 V to 5.5 V		0.7 × AV_{DD}			V
		AV_{DD} = 2.0 V to 2.7 V		0.9 × AV_{DD}			V
Pin capacitance					1.5	3	pF
POWER REQUIREMENTS							
AV_{DD}				2.0		5.5	V
I_{DD}	Normal mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(6)	AV_{DD} = 3.6 V to 5.5 V		110	180	µA
			AV_{DD} = 2.7 V to 3.6 V		95	150	µA
			AV_{DD} = 2.0 V to 2.7 V		80	140	µA
	All power-down mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(6)	AV_{DD} = 3.6 V to 5.5 V		0.5	3.5	µA
			AV_{DD} = 2.7 V to 3.6 V		0.4	3	µA
			AV_{DD} = 2.0 V to 2.7 V		0.1	2	µA
Power dissipation	Normal mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(6)	AV_{DD} = 3.6 V to 5.5 V		0.55	0.99	mW
			AV_{DD} = 2.7 V to 3.6 V		0.25	0.54	mW
			AV_{DD} = 2.0 V to 2.7 V		0.14	0.38	mW
	All power-down mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(6)	AV_{DD} = 3.6 V to 5.5 V		2.50	19.2	µW
			AV_{DD} = 2.7 V to 3.6 V		1.08	10.8	µW
			AV_{DD} = 2.0 V to 2.7 V		0.72	8.1	µW

(1) Linearity calculated using a reduced code range of 3 to 252 for 8-bit, 12 to 1012 for 10bit, and 30 to 4050 for 12-bit, output unloaded.
(2) Straight line passing through codes 3 and 252 for 8-bit, 12 and 1012 for 10-bit, and 30 and 4050 for 12-bit, output unloaded.
(3) Specified by design and characterization, not production tested.
(4) For more details, see 図 7-23.
(5) For more details, see 図 7-24.
(6) For more details, see 図 7-16 and 図 7-58.

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7.6 Timing Requirements

at –40°C to 125°C, and AV_{DD} = 2 V to 5.5 V (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency	AV_{DD} = 2.0 V to 3.6 V			20	MHz
		AV_{DD} = 3.6 V to 5.5 V			50	
t_1	SCLK cycle time	AV_{DD} = 2.0 V to 3.6 V	50			ns
		AV_{DD} = 3.6 V to 5.5 V	20			
t_2	SCLK high time	AV_{DD} = 2.0 V to 3.6 V	25			ns
		AV_{DD} = 3.6 V to 5.5 V	10			
t_3	SCLK low time	AV_{DD} = 2.0 V to 3.6 V	25			ns
		AV_{DD} = 3.6 V to 5.5 V	10			
t_4	$\overline{SYNC}$ to SCLK rising edge setup time	AV_{DD} = 2.0 V to 3.6 V	0			ns
		AV_{DD} = 3.6 V to 5.5 V	0			
t_5	Data setup time	AV_{DD} = 2.0 V to 3.6 V	5			ns
		AV_{DD} = 3.6 V to 5.5 V	5			
t_6	Data hold time	AV_{DD} = 2.0 V to 3.6 V	4.5			ns
		AV_{DD} = 3.6 V to 5.5 V	4.5			
t_7	SCLK falling edge to $\overline{SYNC}$ rising edge	AV_{DD} = 2.0 V to 3.6 V	0			ns
		AV_{DD} = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{SYNC}$ high time	AV_{DD} = 2.0 V to 3.6 V	50			ns
		AV_{DD} = 3.6 V to 5.5 V	20			
t_9	16th SCLK falling edge to $\overline{SYNC}$ falling edge	AV_{DD} = 2.0 V to 3.6 V	100			ns
		AV_{DD} = 3.6 V to 5.5 V	100			
t_{10}	$\overline{SYNC}$ rising edge to 16th SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	AV_{DD} = 2.0 V to 3.6 V	15			ns
		AV_{DD} = 3.6 V to 5.5 V	15			

(1) All input signals are specified with $t_R = t_F$ = 3 ns (10% to 90% of AV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.

7.7 Timing Diagrams

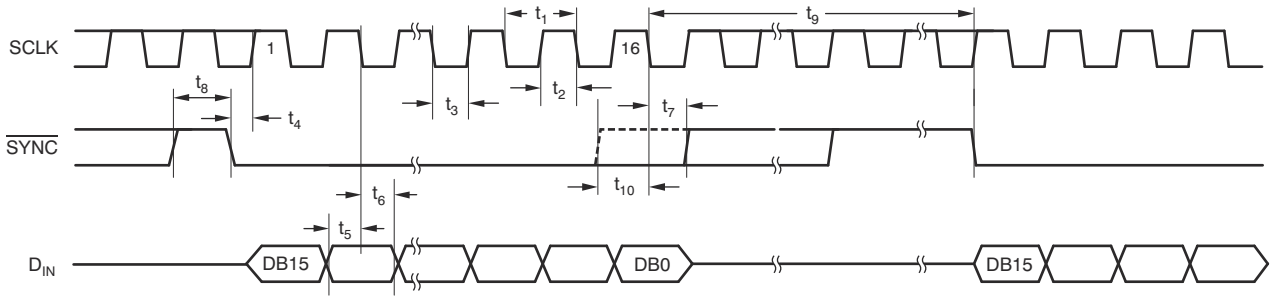

図 7-1. Serial Write Operation

7.8 Typical Characteristics: AV_{DD} = 5 V

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

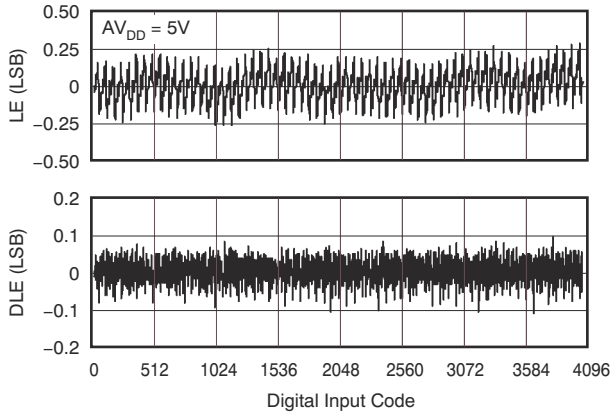

図 7-2. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

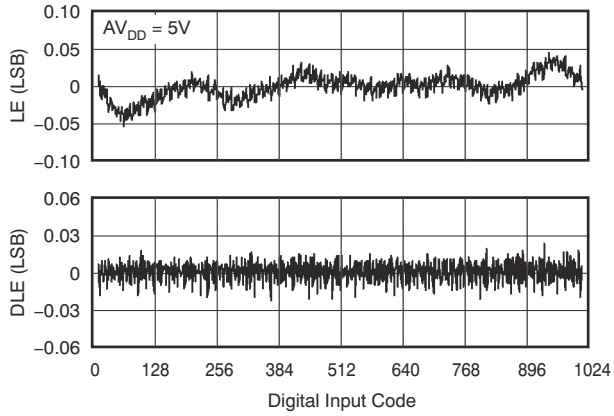

図 7-3. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

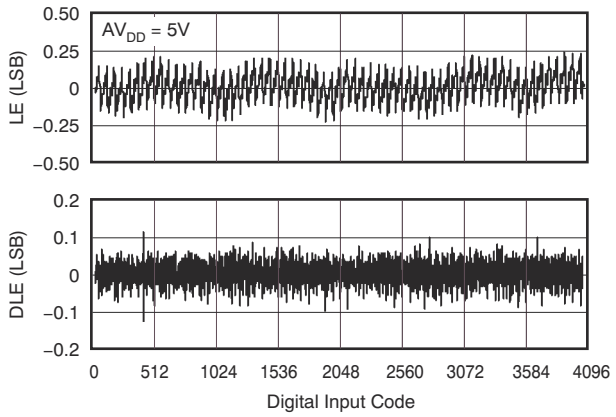

図 7-4. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

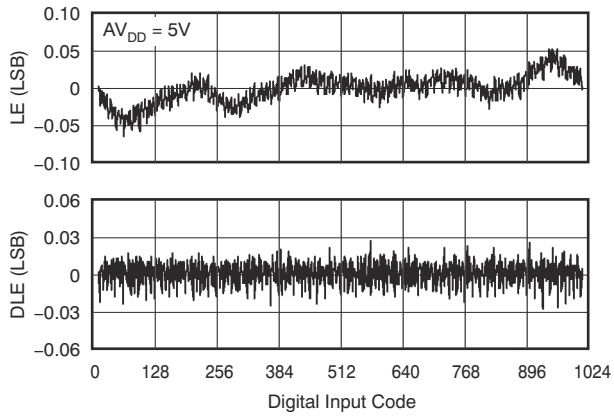

図 7-5. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

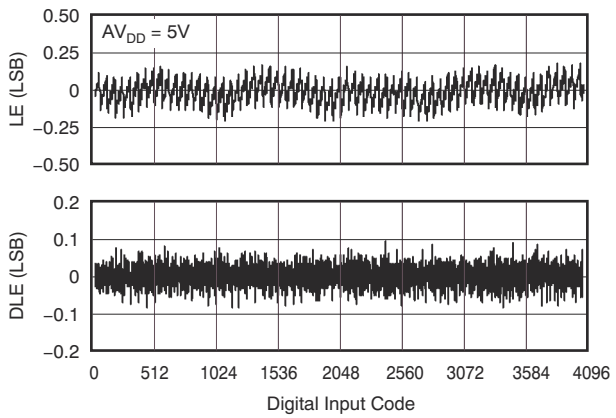

図 7-6. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

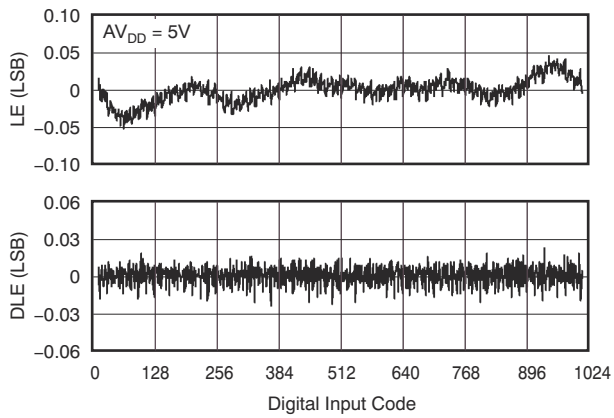

図 7-7. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

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7.8 Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

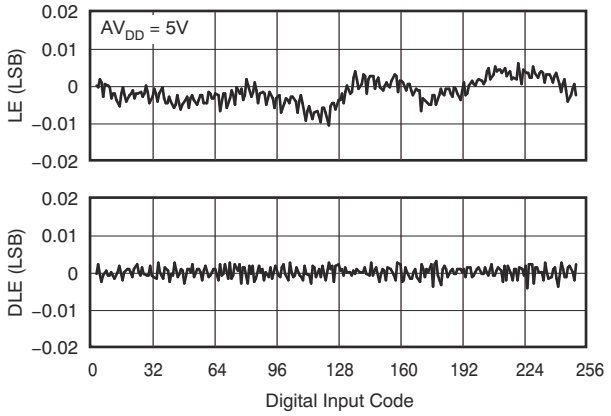

図 7-8. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

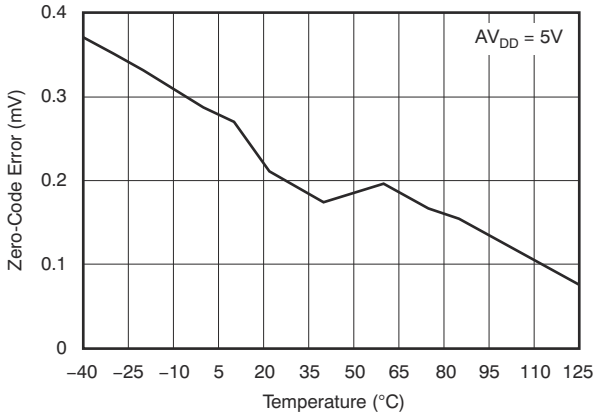

図 7-9. Zero-Code Error vs Temperature

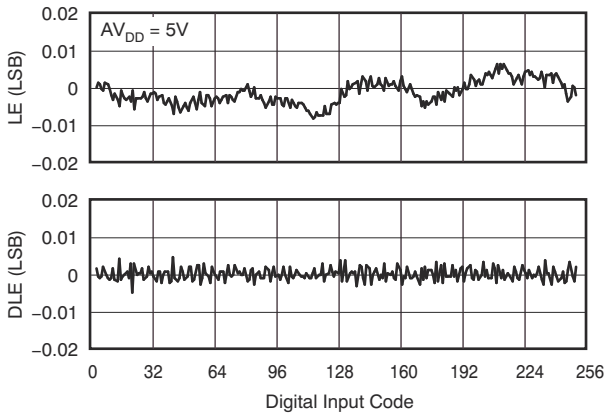

図 7-10. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

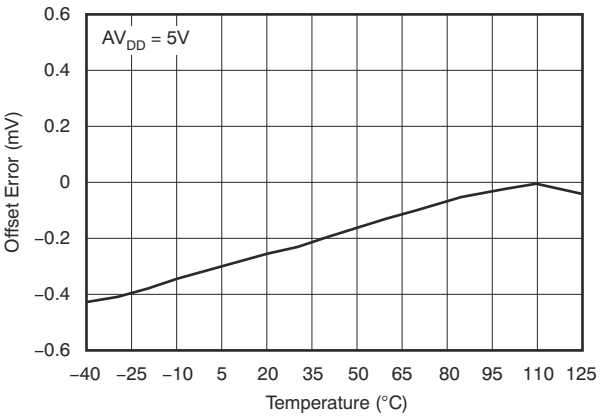

図 7-11. Offset Error vs Temperature

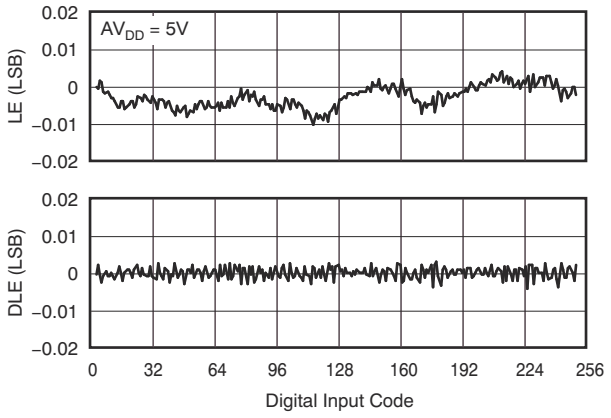

図 7-12. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

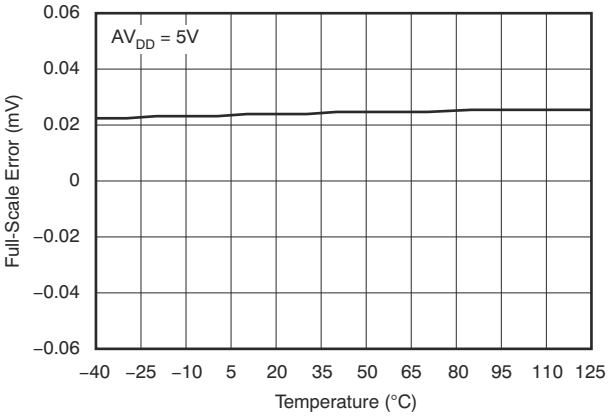

図 7-13. Full-Scale Error vs Temperature

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7.8 Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

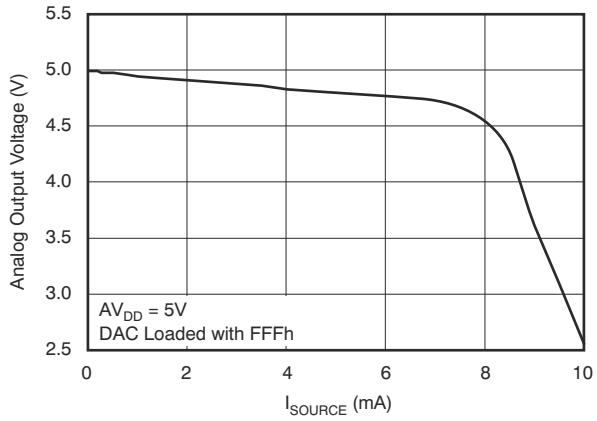

図 7-14. Source Current at Positive Rail

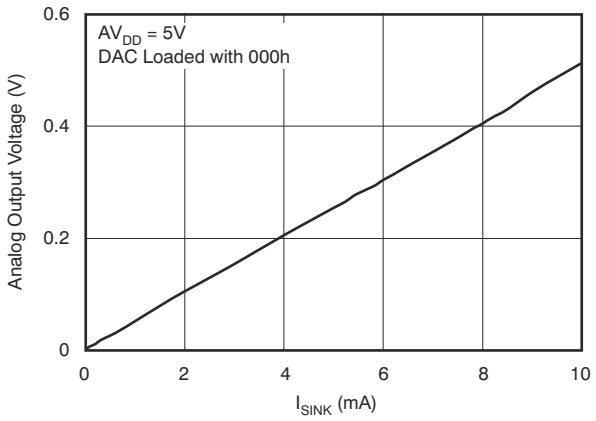

図 7-15. Sink Current at Negative Rail

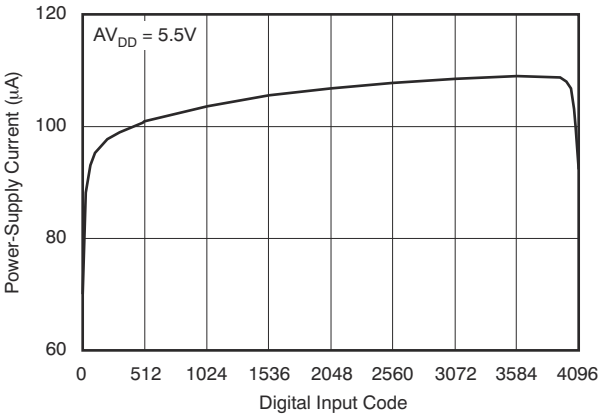

図 7-16. Power-Supply Current vs Digital Input Code

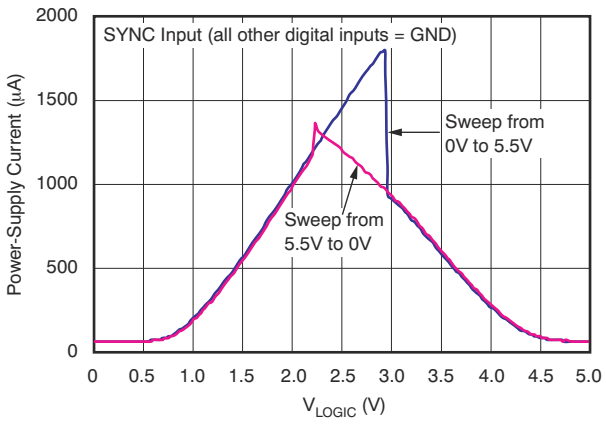

図 7-17. Power-Supply Current vs Logic Input Voltage

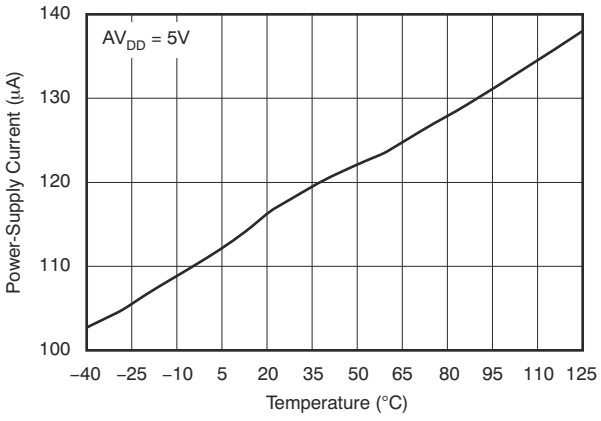

図 7-18. Power-Supply Current vs Temperature

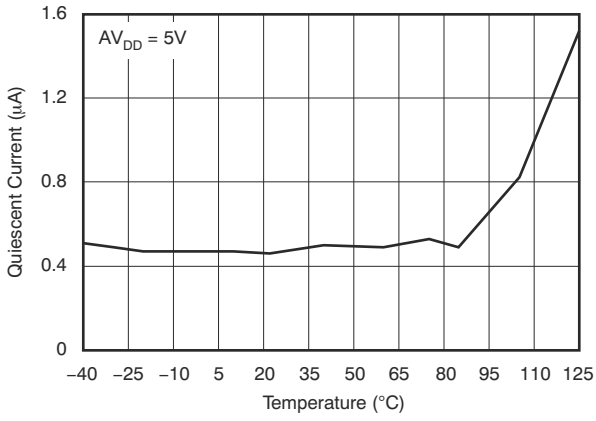

図 7-19. Power-Down Current vs Temperature

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7.8 Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

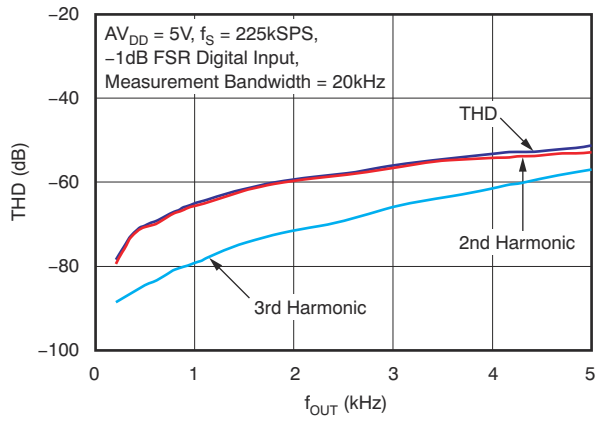

図 7-20. Total Harmonic Distortion vs Output Frequency

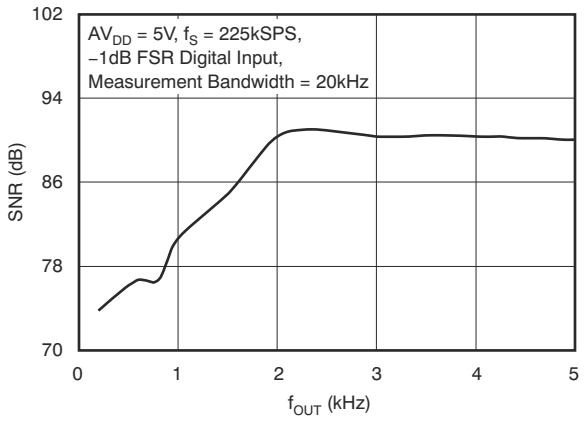

図 7-21. Signal-to-Noise Ratio vs Output Frequency

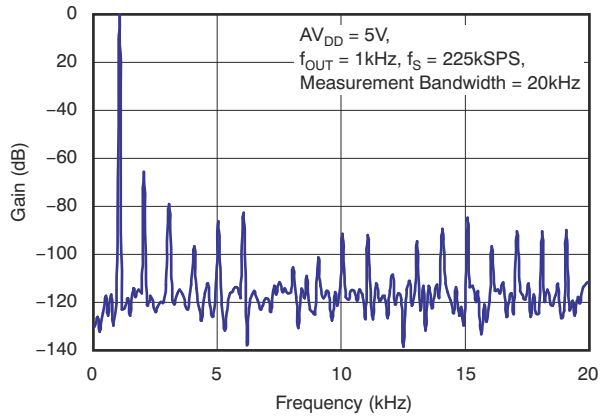

図 7-22. Power Spectral Density

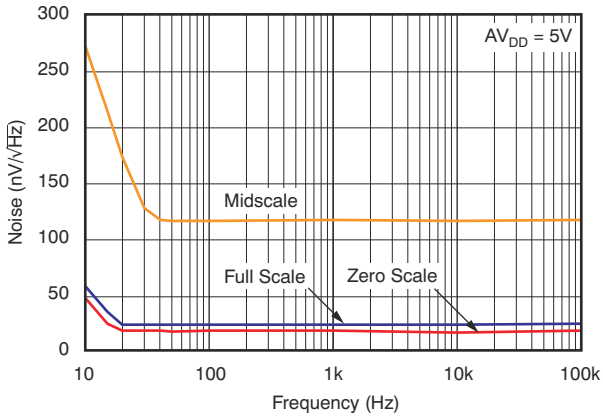

図 7-23. DAC Output Noise Density vs Frequency

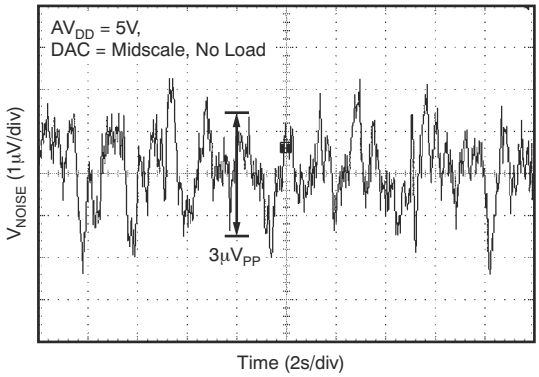

図 7-24. DAC Output Noise, 0.1-Hz to 10-Hz Bandwidth

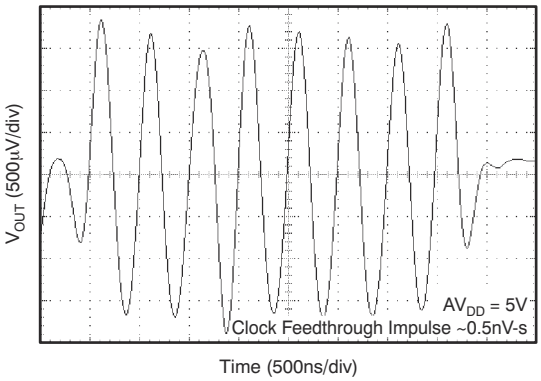

図 7-25. Clock Feedthrough, 5-V, 2-MHz, Midscale

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7.8 Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

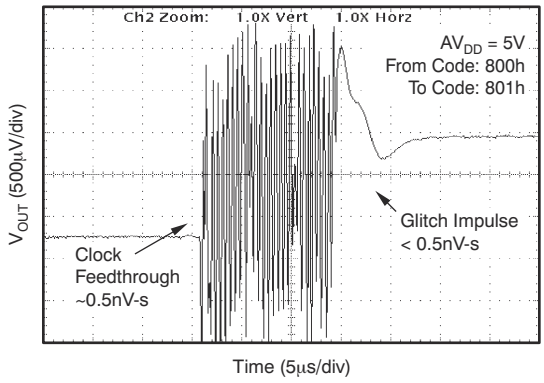

図 7-26. Glitch Energy, 5-V, 12-Bit, 1-LSB Step, Rising Edge

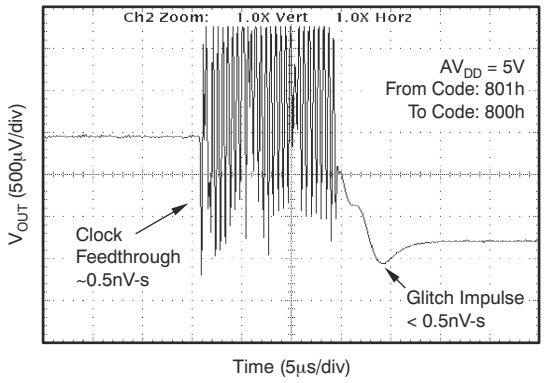

図 7-27. Glitch Energy, 5-V, 12-Bit, 1-LSB Step, Falling Edge

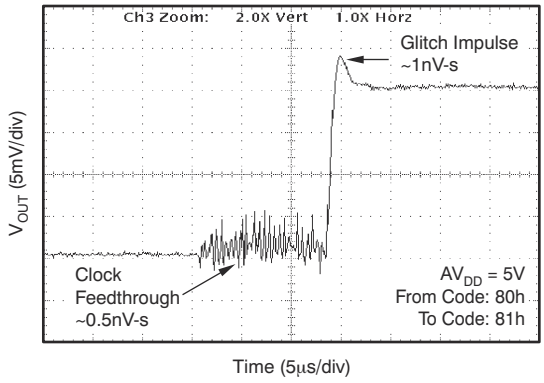

図 7-28. Glitch Energy, 5-V, 8-Bit, 1-LSB Step, Rising Edge

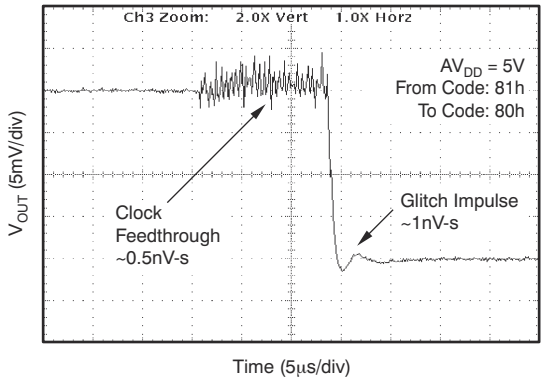

図 7-29. Glitch Energy, 5-V, 8-Bit, 1-LSB Step, Falling Edge

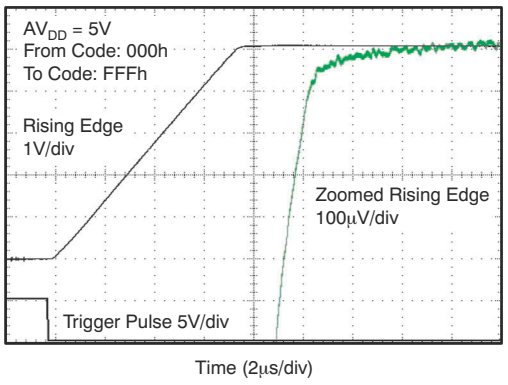

図 7-30. Full-Scale Settling Time, 5-V Rising Edge

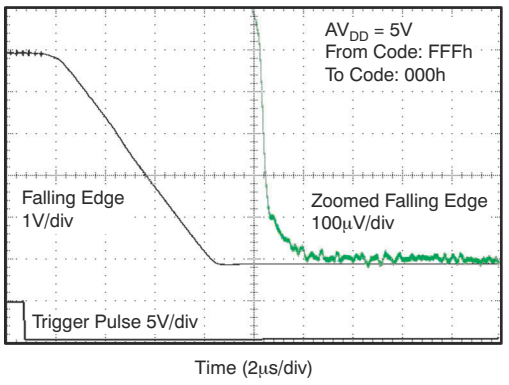

図 7-31. Full-Scale Settling Time, 5-V Falling Edge

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7.8 Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

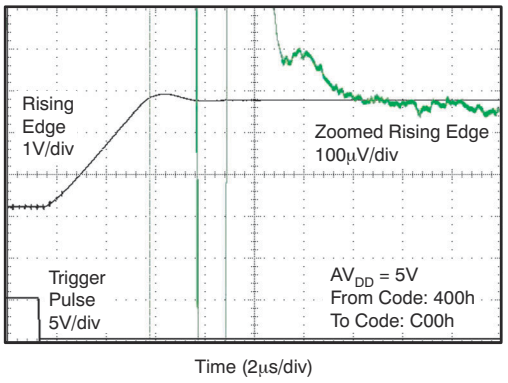

図 7-32. Half-Scale Settling Time, 5-V Rising Edge

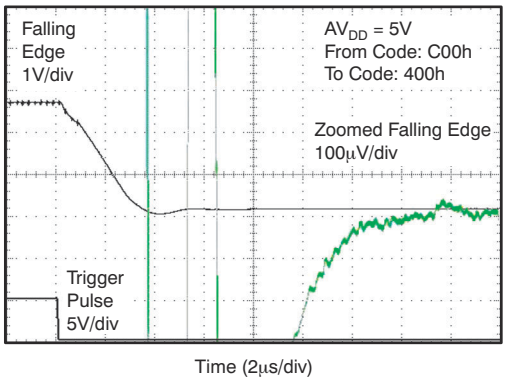

図 7-33. Half-Scale Settling Time 5-V Falling Edge

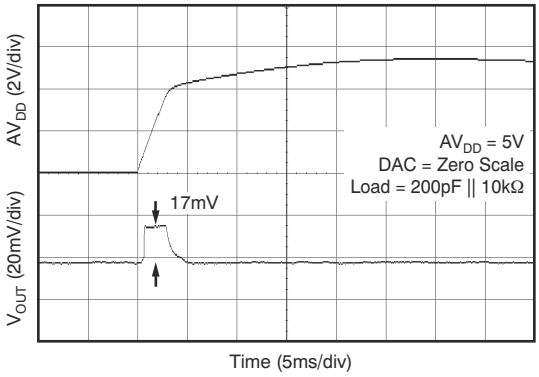

図 7-34. Power-On Reset to 0-V Power-On Glitch

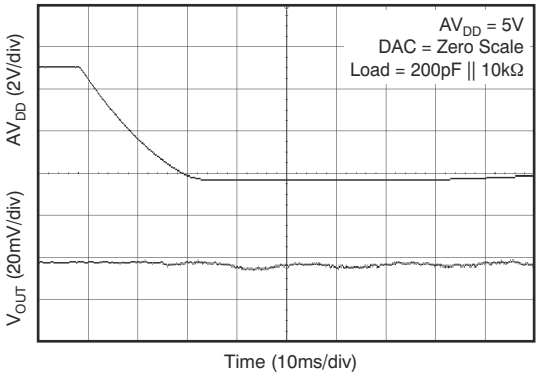

図 7-35. Power-Off Glitch

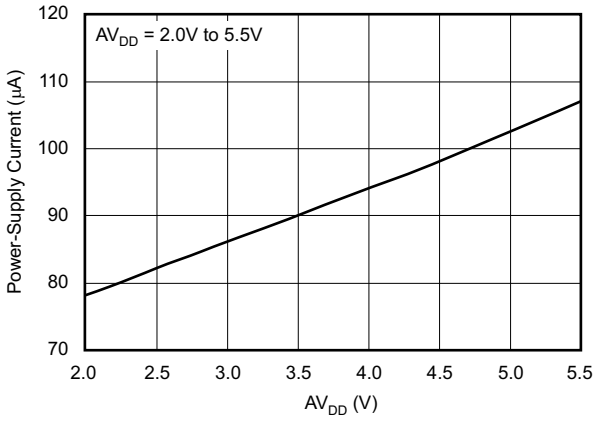

図 7-36. Power-Supply Current vs Power-Supply Voltage

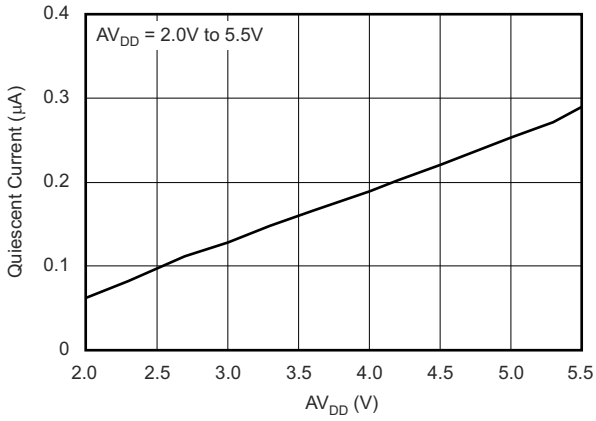

図 7-37. Power-Down Current vs Power-Supply Voltage

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7.8 Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

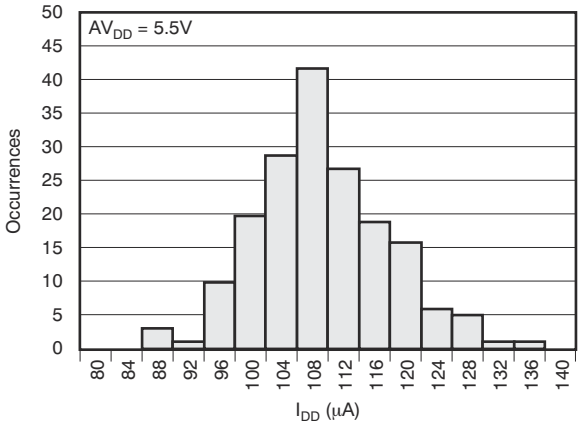

図 7-38. Power-Supply Current Histogram

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7.9 Typical Characteristics: AV_{DD} = 3.6 V

at T_A = 25°C, AV_{DD} = 3.6 V, and DAC loaded with midscale code (unless otherwise noted)

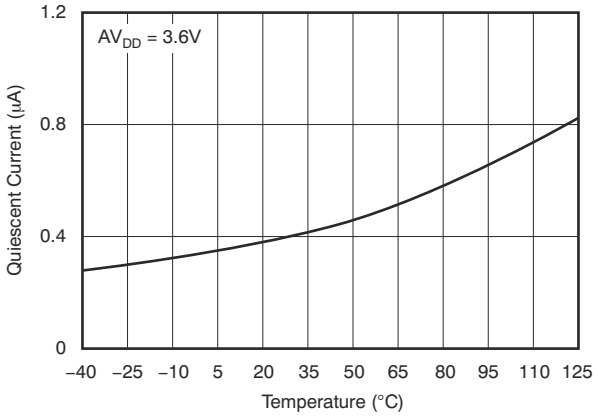

図 7-39. Power-Down Current vs Temperature

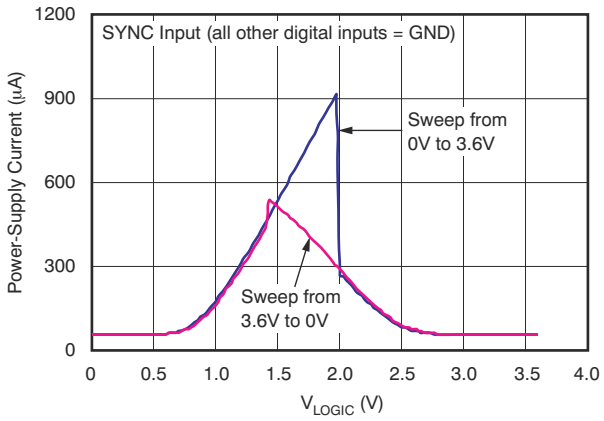

図 7-40. Power-Supply Current vs Logic Input Voltage

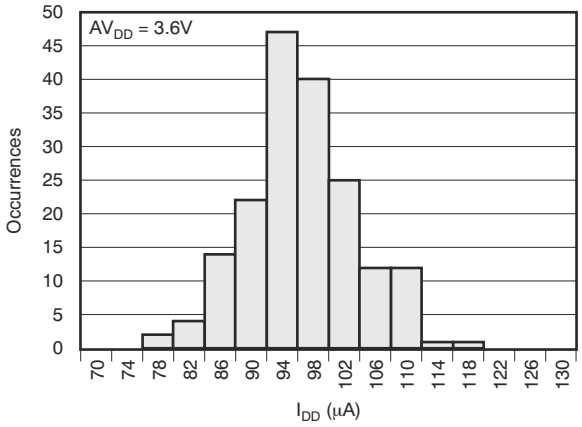

図 7-41. Power-Supply Current Histogram

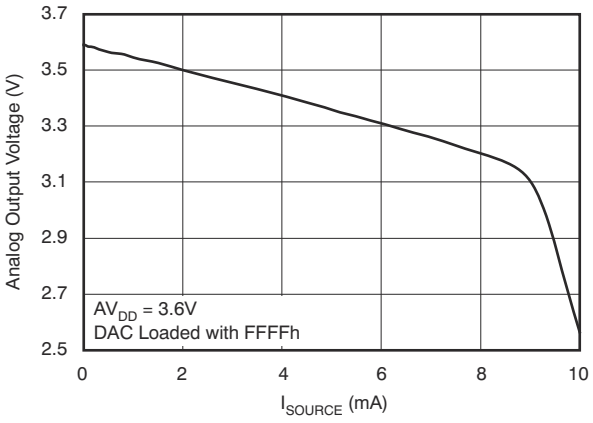

図 7-42. Source Current at Positive Rail

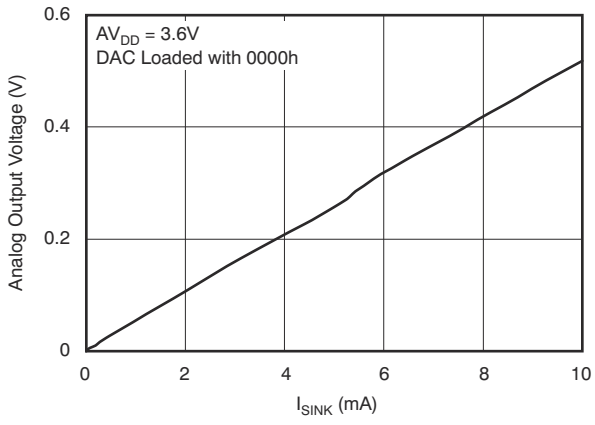

図 7-43. Sink Current at Negative Rail

7.10 Typical Characteristics: AV_{DD} = 2.7 V

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

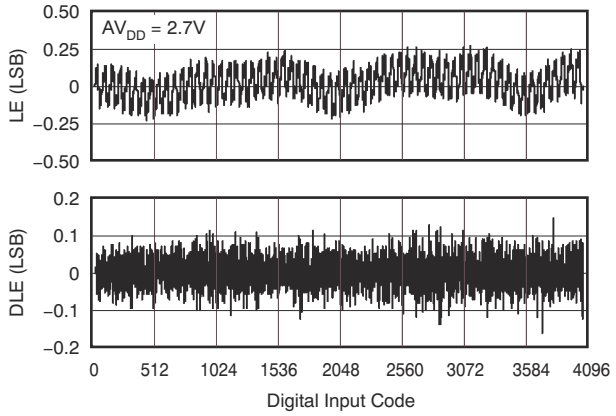

図 7-44. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

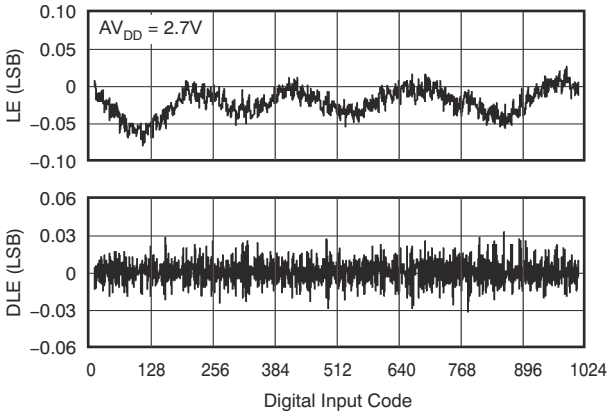

図 7-45. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

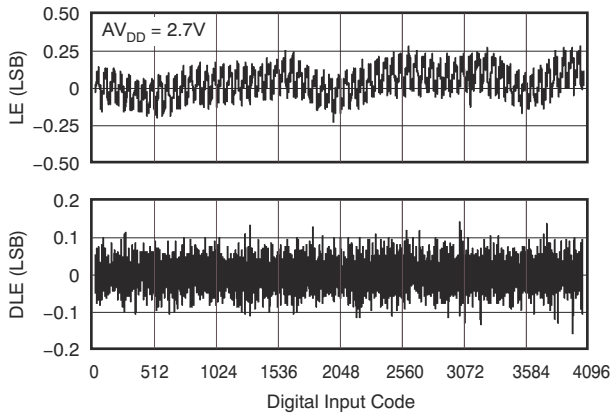

図 7-46. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

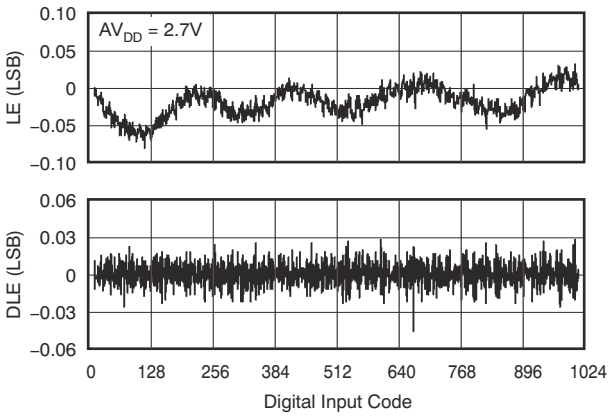

図 7-47. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

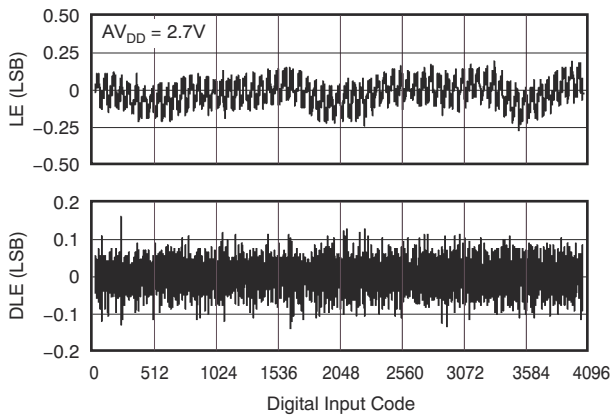

図 7-48. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

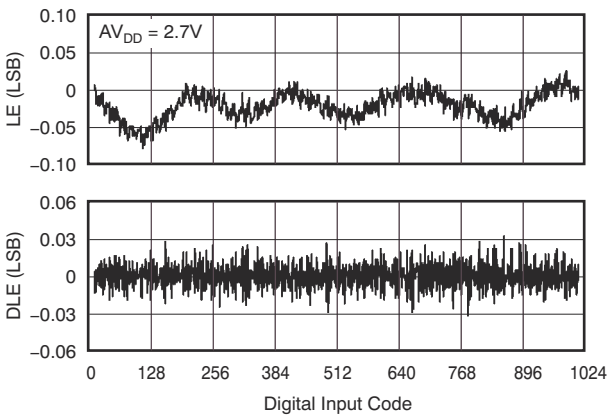

図 7-49. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

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7.10 Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

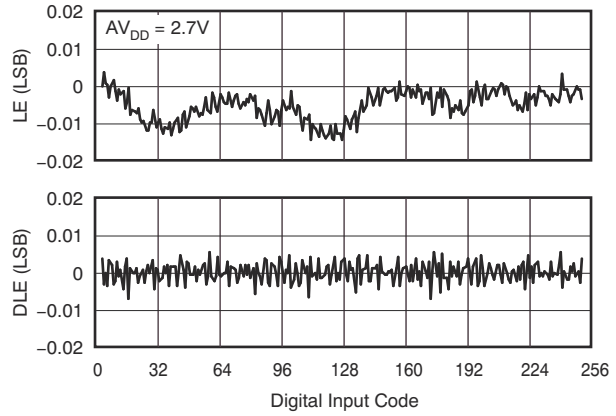

図 7-50. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

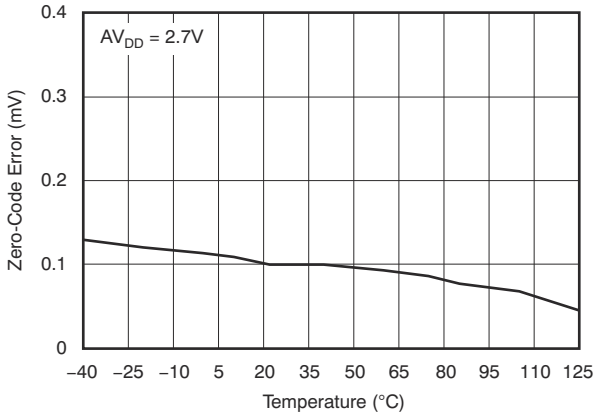

図 7-51. Zero-Code Error vs Temperature

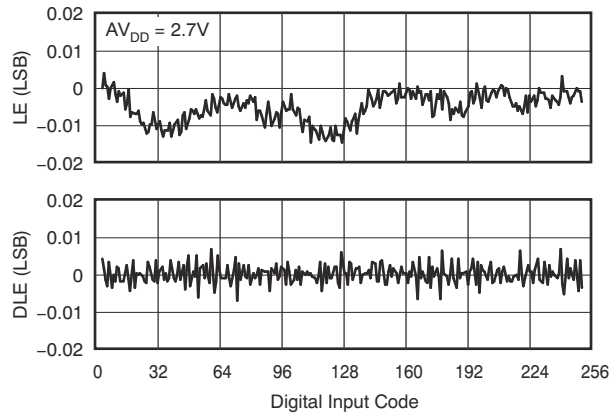

図 7-52. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

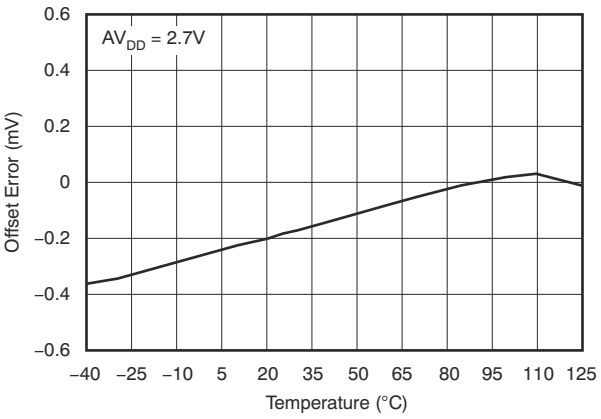

図 7-53. Offset Error vs Temperature

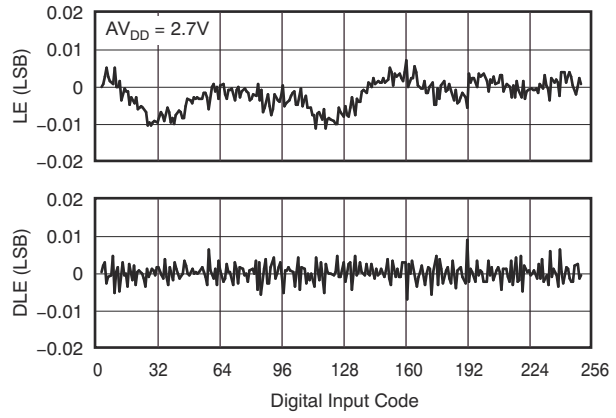

図 7-54. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

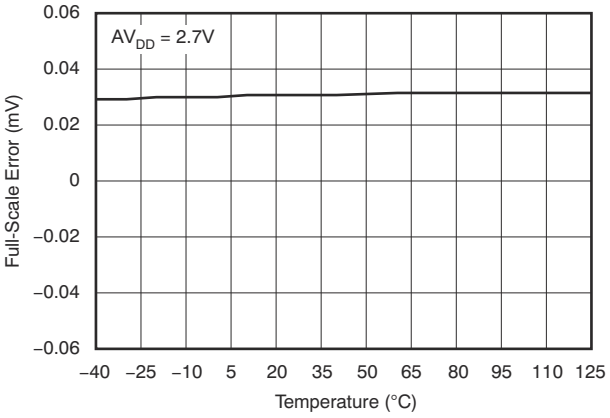

図 7-55. Full-Scale Error vs Temperature

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7.10 Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

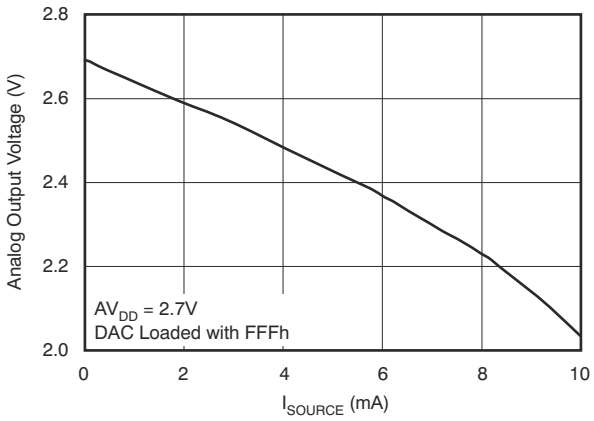

図 7-56. Source Current at Positive Rail

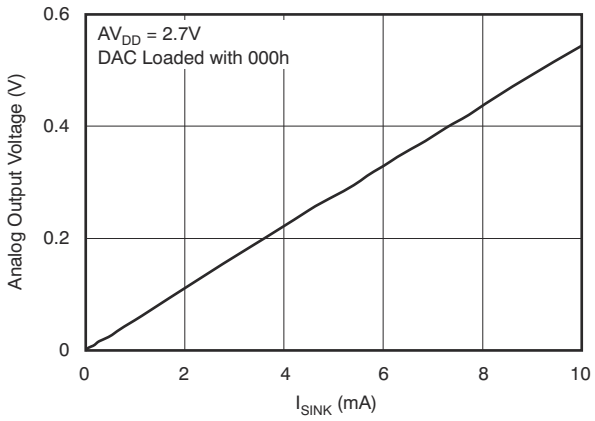

図 7-57. Sink Current at Negative Rail

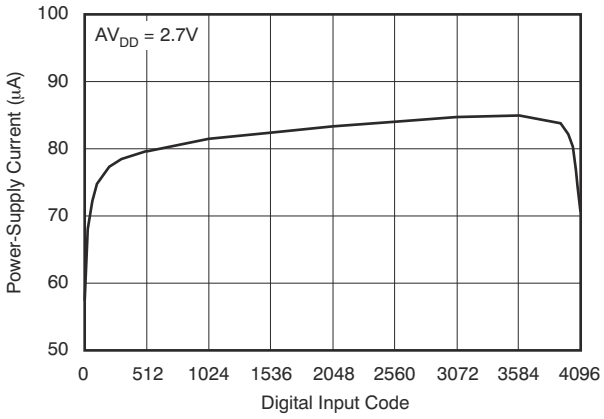

図 7-58. Power-Supply Current vs Digital Input Code

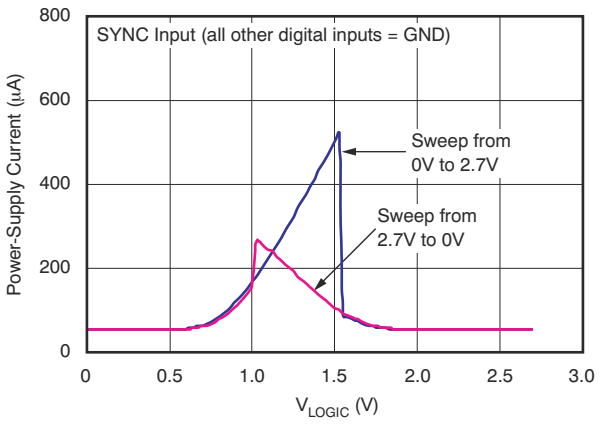

図 7-59. Power-Supply Current vs Logic Input Voltage

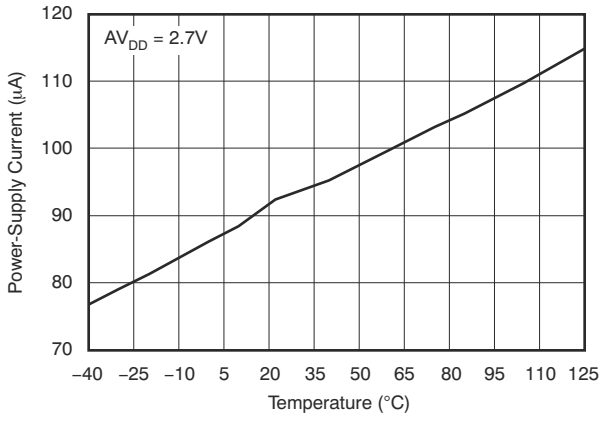

図 7-60. Power-Supply Current vs Temperature

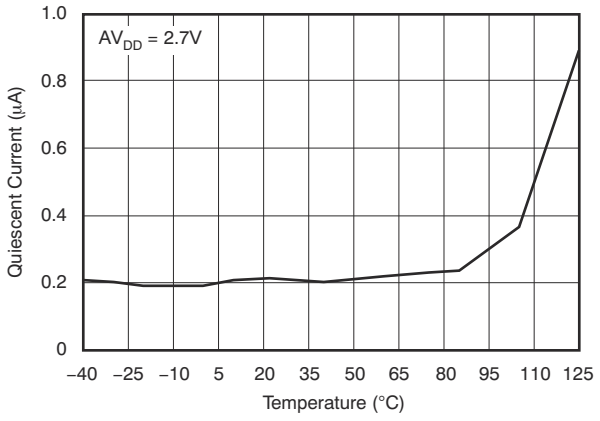

図 7-61. Power-Down Current vs Temperature

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7.10 Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

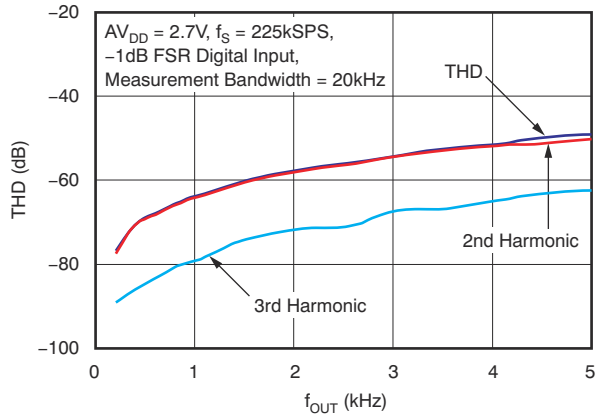

図 7-62. Total Harmonic Distortion vs Output Frequency

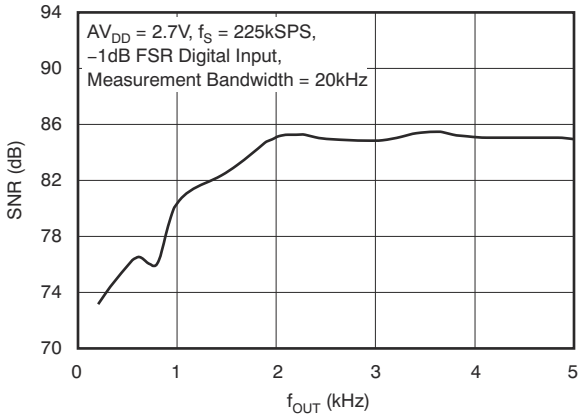

図 7-63. Signal-to-Noise Ratio vs Output Frequency

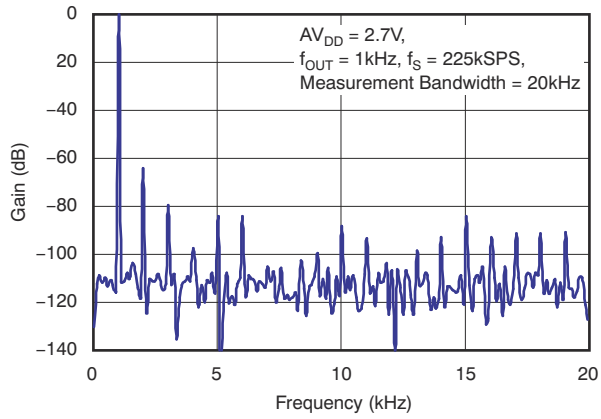

図 7-64. Power Spectral Density

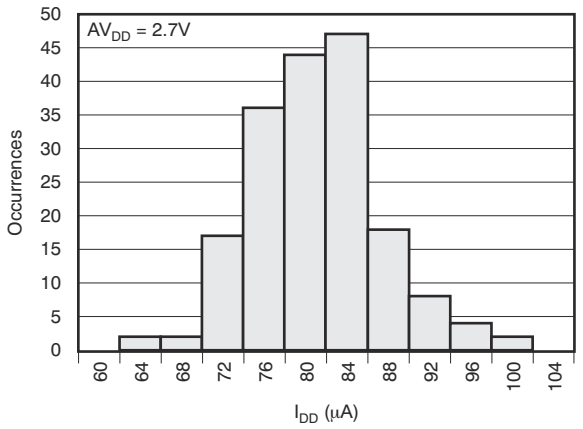

図 7-65. Power-Supply Current Histogram

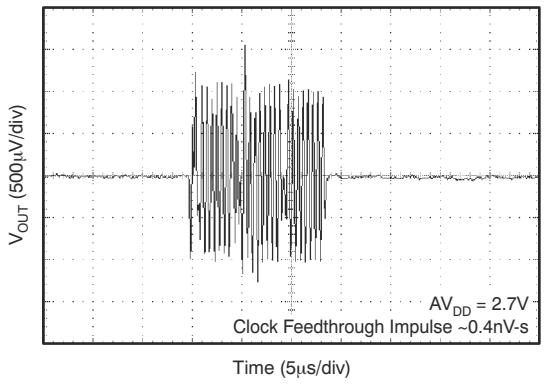

図 7-66. Clock Feedthrough 2.7-V, 20-MHz, Midscale

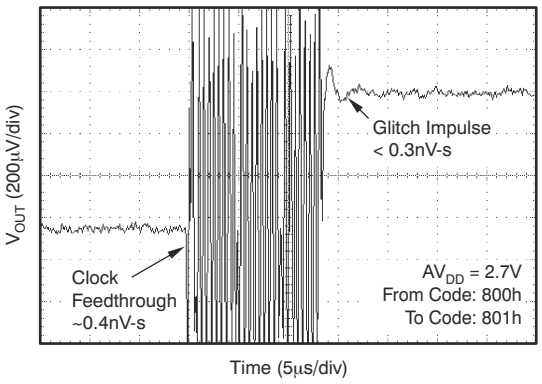

図 7-67. Glitch Energy, 2.7-V, 12-Bit, 1-LSB Step, Rising Edge

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7.10 Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

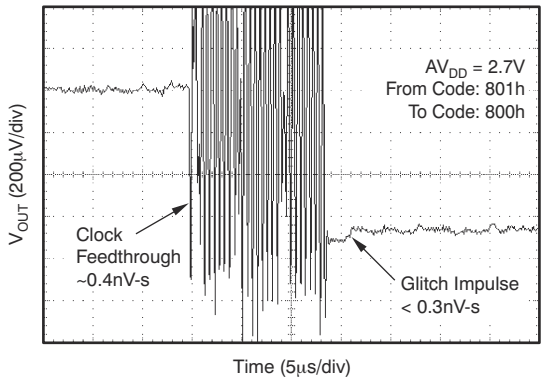

図 7-68. Glitch Energy, 2.7-V, 12-Bit, 1-LSB Step, Falling Edge

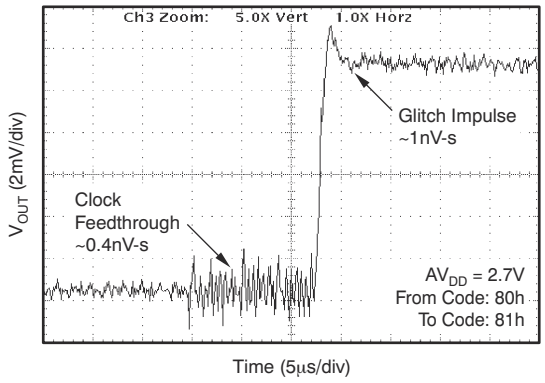

図 7-69. Glitch Energy, 2.7-V, 8-Bit, 1-LSB Step, Rising Edge

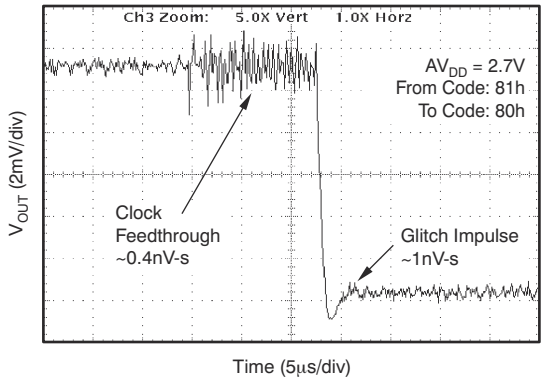

図 7-70. Glitch Energy, 2.7-V, 8-Bit, 1-LSB Step, Falling Edge

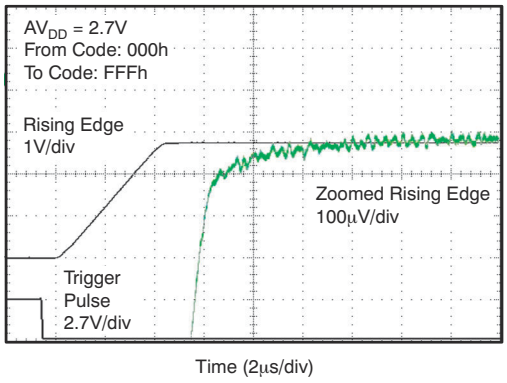

図 7-71. Full-Scale Settling Time, 2.7-V Rising Edge

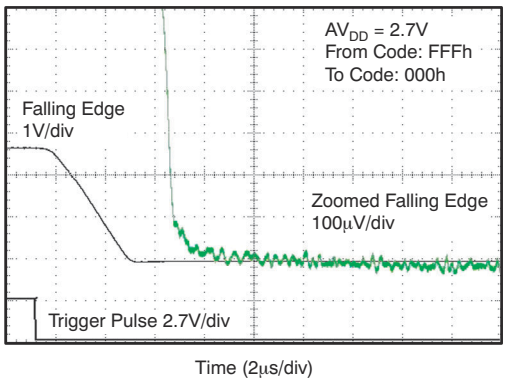

図 7-72. Full-Scale Settling Time, 2.7-V Falling Edge

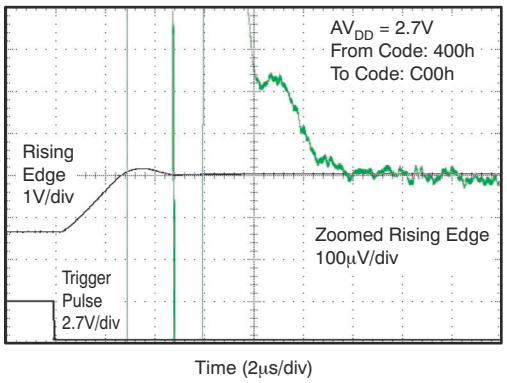

図 7-73. Half-Scale Settling Time, 2.7-V Rising Edge

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7.10 Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

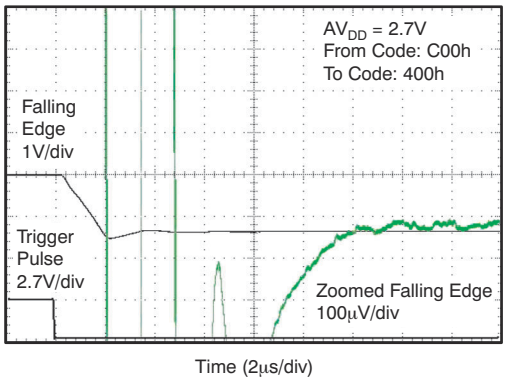


図 7-74. Half-Scale Settling Time, 2.7-V Falling Edge

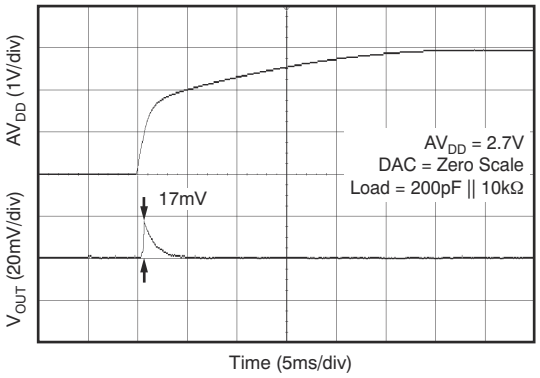


図 7-75. Power-On Reset to 0-V Power-On Glitch

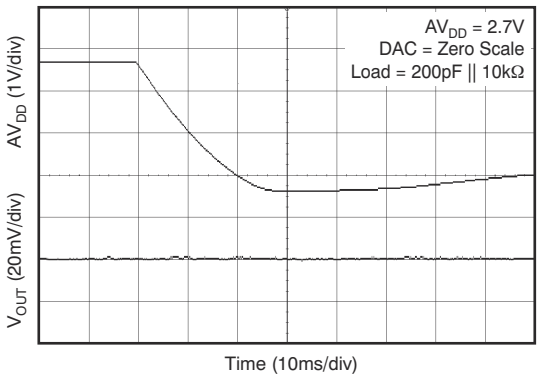


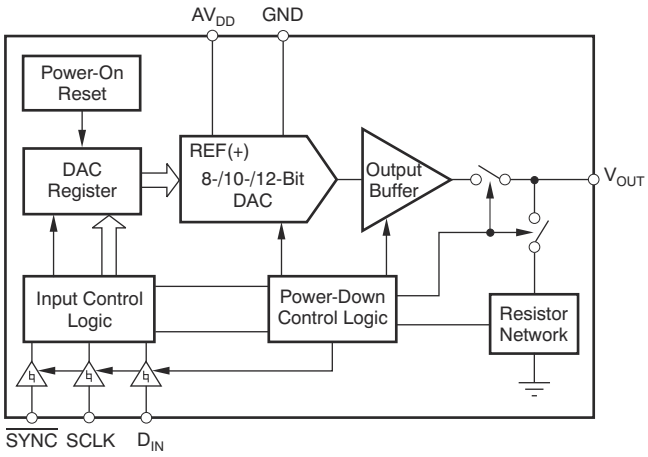
図 7-76. Power-Off Glitch

8 Detailed Description

8.1 Overview

The 8-bit DAC5311, 10-bit DAC6311, and 12-bit DAC7311 devices (DACx311) are low-power, single-channel, voltage output DACs. These devices are monotonic by design, provide excellent linearity, and minimize undesired code-to-code transient voltages while offering an easy upgrade path within a pin-compatible family. All devices use a versatile, three-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI, Microwire, and digital signal processor (DSP) interfaces.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Section

The DACx311 are fabricated using Texas Instruments' proprietary HPA07 process technology. The architecture consists of a string DAC followed by an output buffer amplifier. Because there is no reference input pin, the power supply (AV_{DD}) acts as the reference. 図 8-1 shows a block diagram of the DAC architecture.

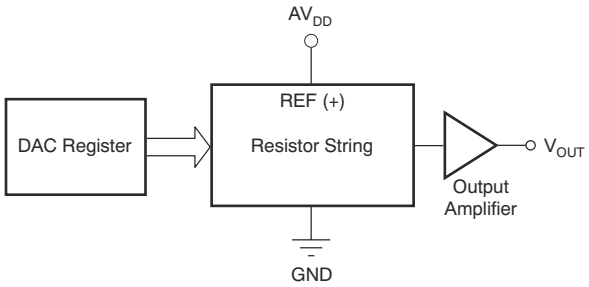


図 8-1. DACx311 Architecture

The input coding to the DACx311 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = AV_{DD} \times \frac{D}{2^n} \quad (1)$$

where

- n = resolution in bits; either 8 (DAC5311), 10 (DAC6311), or 12 (DAC7311).
- D = decimal equivalent of the binary code that is loaded to the DAC register. D ranges from 0 to 255 for 8-bit DAC5311, 0 to 1023 for the 10-bit DAC6311, and 0 to 4095 for the 12-bit DAC7311.

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8.3.2 Resistor String

図 8-2 shows the resistor string section, which is a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. The resistor string architecture is inherently monotonic.

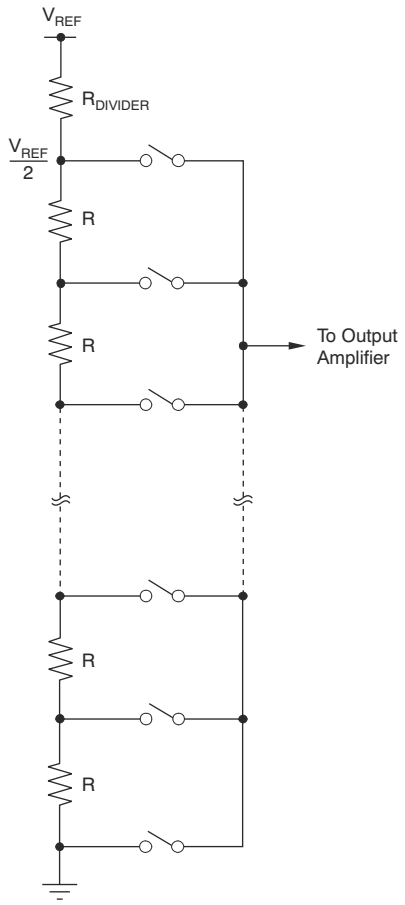

図 8-2. Resistor String

8.3.3 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on the output, which gives an output range of 0 V to AV_{DD}. The output amplifier is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the *Typical Characteristics* section for the given voltage input. The slew rate is 0.7 V/µs with a half-scale settling time of typically 6 µs with the output unloaded.

8.3.4 Power-On Reset

The DACx311 contain a power-on reset circuit that controls the output voltage during power up. On power up, the DAC register is filled with zeros and the output voltage is 0 V. The DAC register remains that way until a valid write sequence is made to the DAC. This design is useful in applications where knowing the state of the DAC output while powering up is important.

The occurring power-on glitch impulse is only a few millivolts (typically, 17 mV; see 図 7-34).

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8.4 Device Functional Modes

8.4.1 Power-Down Modes

The DACx311 contain four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. 表 8-1 shows how the state of the bits corresponds to the mode of operation of the device.

表 8-1. Modes of Operation for the DACx311

PD1	PD0	OPERATING MODE
NORMAL MODE		
0	0	Normal Operation
POWER-DOWN MODES		
0	1	Output 1 kΩ to GND
1	0	Output 100 kΩ to GND
1	1	High-Z

When both bits are set to 0, the device works normally with a standard power consumption of typically 80 µA at 2 V. However, for the three power-down modes, the typical supply current falls to 0.5 µA at 5 V, 0.4 µA at 3 V, and 0.1 µA at 2 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. The advantage of this architecture is that the output impedance of the part is known while the part is in power-down mode. There are three different options: the output is connected internally to GND either through a 1-kΩ resistor or a 100-kΩ resistor, or is left open-circuited (High-Z). 図 8-3 illustrates the output stage.

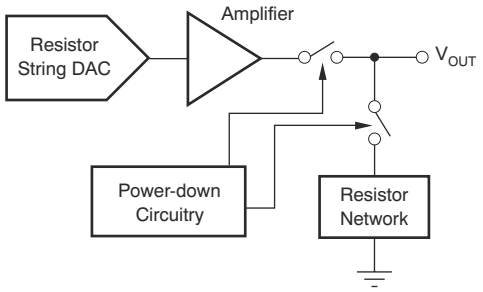

図 8-3. Output Stage During Power-Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 50 µs for AV_{DD} = 5 V and AV_{DD} = 3 V.

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8.5 Programming

8.5.1 Serial Interface

The DACx311 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. For an example of a typical write sequence, see 図 7-1.

8.5.1.1 Input Shift Register

The input shift register is 16 bits wide, as shown in 表 8-2. The first two bits (PD0 and PD1) are reserved control bits that set the desired mode of operation (normal mode or any one of three power-down modes) as indicated in 表 8-1.

The remaining data bits are either 12 (DAC7311), 10 (DAC6311), or 8 (DAC5311) data bits, followed by *don't care* bits, as shown in 表 8-2, 表 8-3, and 表 8-4, respectively.

表 8-2. DAC5311 8-Bit Data Input Register

DB15	DB14								DB6	DB5					DB0
PD1	PD0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-3. DAC6311 10-Bit Data Input Register

DB15	DB14										DB4	DB3			DB0
PD1	PD0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-4. DAC7311 12-Bit Data Input Register

DB15	DB14												DB2	DB1	DB0
PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line are clocked into the 16-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making

the DACx311 compatible with high-speed DSPs. On the 16th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed.

At this point, the $\overline{\text{SYNC}}$ line can be kept low or brought high. In either case, $\overline{\text{SYNC}}$ must be brought high for a minimum of 20 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence.

8.5.1.2 $\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, bringing $\overline{\text{SYNC}}$ high before the 16th falling edge acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in 図 8-4.

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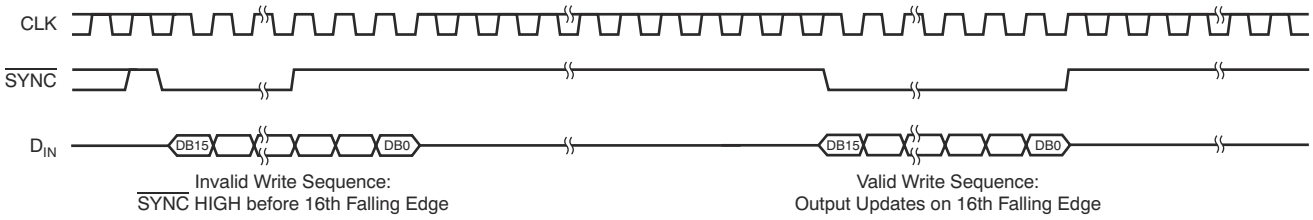

図 8-4. DACx311 SYNC Interrupt Facility

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9 Application and Implementation

注

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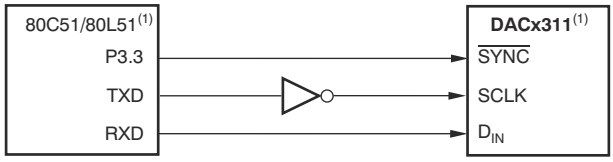
9.1 Application Information

9.1.1 Microprocessor Interfacing

9.1.1.1 DACx311 to 8051 Interface

図 9-1 shows a serial interface between the DACx311 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DACx311, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data are to be transmitted to the DACx311, P3.3 is taken low. The 8051 transmits data only in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 remains low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 8051 outputs the serial data in a format that has the LSB first. The DACx311 requires data with the MSB as the first bit received. Therefore, the 8051 transmit routine must take this requirement into account, and *mirror* the data as needed.

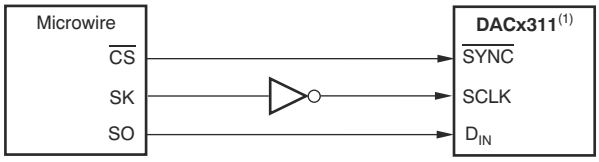


NOTE: (1) Additional pins omitted for clarity.

図 9-1. DACx311 to 80C51/80I51 Interfaces

9.1.1.2 DACx311 to Microwire Interface

図 9-2 shows an interface between the DACx311 and any Microwire-compatible device. Serial data (SO) are shifted out on the falling edge of the serial clock (SK) and are clocked into the DACx311 on the rising edge of the SK signal.

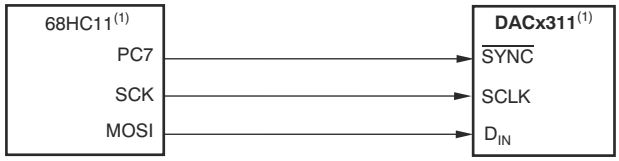


NOTE: (1) Additional pins omitted for clarity.

図 9-2. DACx311 to Microwire Interface

9.1.1.3 DACx311 to 68HC11 Interface

図 9-3 shows a serial interface between the DACx311 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DACx311, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7), similar to what was done for the 8051.



NOTE: (1) Additional pins omitted for clarity.

図 9-3. DACx311 to 68HC11 Interface

Configure the 68HC11 so that the CPOL bit is 0 and the CPHA bit is 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the $\overline{SYNC}$ line is taken low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data are transmitted MSB first. To load data to the DACx311, PC7 is held low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

9.2 Typical Applications

9.2.1 Loop Powered Transmitter

The described loop powered transmitter can accurately source currents from 4 mA to 20 mA.

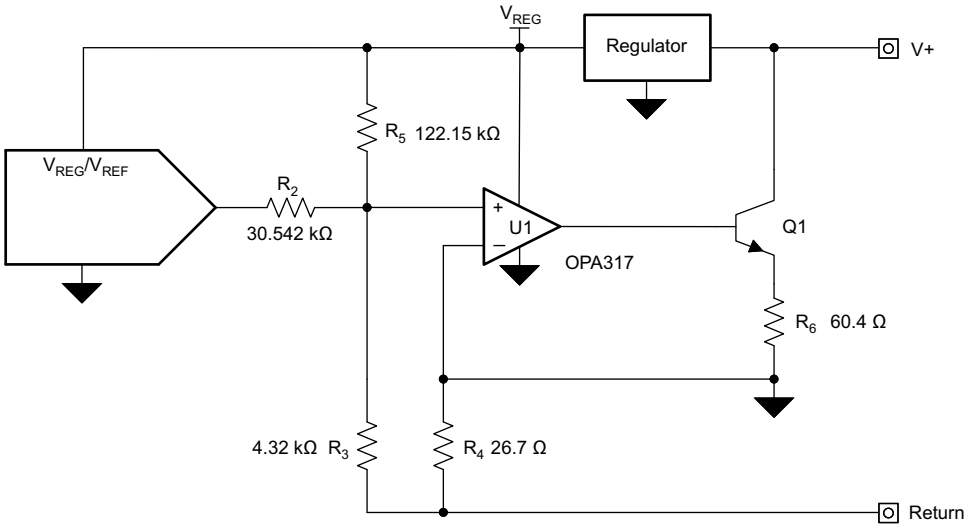


図 9-4. Loop Powered Transmitter Schematic

9.2.1.1 Design Requirements

The transmitter has only two external input pins; a supply connection and a ground (or return) connection. The transmitter communicates back to the host, typically a PLC analog input module, by precisely controlling the magnitude of the return current. To conform to the 4-mA to 20-mA communication standards, the complete transmitter must consume less than 4 mA of current.

The complete design of this circuit is outlined in TIPD158, *Low Cost Loop-Powered 4-20mA Transmitter EMC/EMI Tested Reference Design*. The design is expected to be low-cost and deliver immunity to the IEC61000-4 suite of tests with minimum impact on the accuracy of the system. Reference design TIPD158 includes the design goals, simulated results, and measured performance.

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9.2.1.2 Detailed Design Procedure

Amplifier U1 uses negative feedback to make sure that the potentials at the inverting (V–) and noninverting (V+) input terminals are equal. In this configuration, V– is directly tied to the local GND; therefore, the potential at the noninverting input terminal is driven to local ground. Thus, the voltage difference across R_2 is the DAC output voltage (VOUT), and the voltage difference across R_5 is the regulator voltage (VREG). These voltage differences cause currents to flow through R_2 and R_5, as illustrated in 図 9-5.

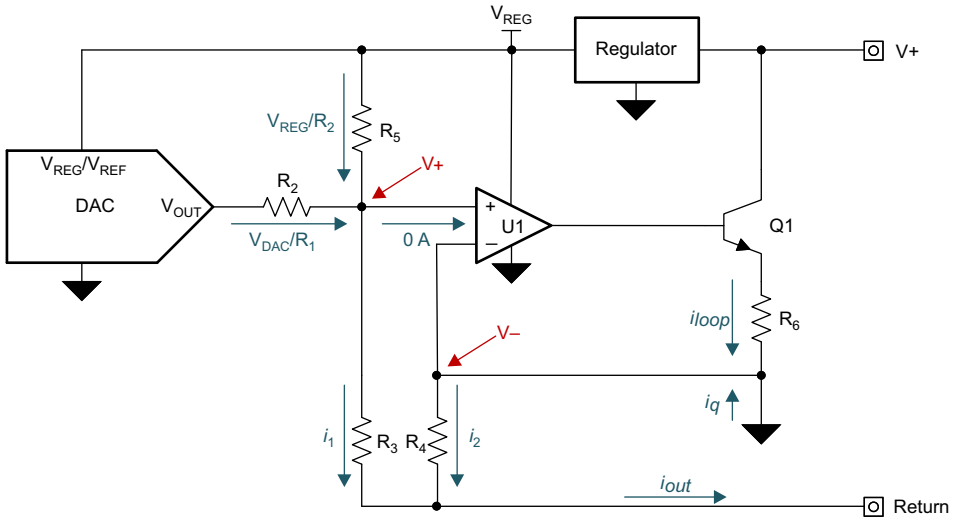

図 9-5. Voltage to Current Conversion

The currents from R_2 and R_5 sum into i_1 (defined in 式 2), and i_1 flows through R_3.

$$i_1 = \frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} \tag{2}$$

Amplifier U2 drives the base of Q1, the NPN bipolar junction transistor (BJT), to allow current to flow through R_4 so that the voltage drops across R_3 and R_4 remain equal. This design keeps the inverting and noninverting terminals at the same potential. A small part of the current through R_4 is sourced by the quiescent current of all of the components used in the transmitter design (regulator, amplifier, and DAC). The voltage drops across R_3 and R_4 are equal; therefore, different-sized resistors cause different current flow through each resistor. Use these different-sized resistors to apply gain to the current flow through R_4 by controlling the ratio of resistor R_3 to R_4, as shown in 式 3:

$$\begin{aligned} V+ &= i_1 \cdot R_3 \\ V- &= i_2 \cdot R_4 \Rightarrow i_2 = \frac{i_1 \cdot R_3}{R_4} \\ V+ &= V- \end{aligned} \tag{3}$$

The current gain in the circuit helps allow a majority of the output current to come directly from the loop through Q1 instead of from the voltage-to-current converter. This current gain, in addition to the low-power components, keeps the current consumption of the voltage-to-current converter low. Currents i_1 and i_2 sum to form output current i_{out}, as shown in 式 4:

$$i_{out} = i_1 + i_2 = \frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} + \frac{R_3}{R_4} \cdot \left(\frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} \right) = \left(\frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} \right) \cdot \left(1 + \frac{R_3}{R_4} \right) \tag{4}$$

The complete transfer function, arranged as a function of input code, is shown in 式 5. The remaining sections divide this circuit into blocks for simplified discussion.

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$$i_{out}(Code) = \left(\frac{V_{REG} \cdot Code}{2^{Resolution} \cdot R_2} + \frac{V_{REG}}{R_5} \right) \cdot \left(1 + \frac{R_3}{R_4} \right) \quad (5)$$

Resistor R_6 is included to reduce the gain of transistor Q1, and therefore, reduce the closed-loop gain of the voltage-to-current converter for a stable design. Size resistors R_2, R_3, R_4, and R_5 based on the full-scale range of the DAC, regulator voltage, and the desired current output range of the design.

9.2.1.3 Application Curves

図 9-6 shows the measured transfer function of the circuit. 図 9-7 shows the total unadjusted error (TUE) of the circuit, staying below 0.15 %FSR.

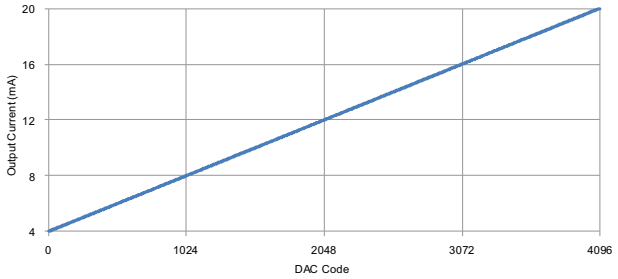

図 9-6. Output Current vs Code

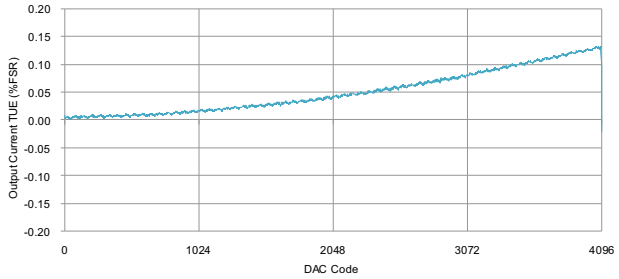

図 9-7. Current Total Unadjusted Error vs Code

9.2.2 Using the REF5050 as a Power Supply for the DACx311

As a result of the extremely low supply current required by the DACx311, an alternative option is to use a REF5050 5-V precision voltage reference to supply the required voltage to the part, as shown in 図 9-8. This option is especially useful if the power supply is too noisy or if the system supply voltages are at some value other than 5 V. The REF5050 outputs a steady supply voltage for the DACx311. If the REF5050 is used, the current needed to supply DACx311 is typically 110 µA at 5 V, with no load on the output of the DAC. When the DAC output is loaded, the REF5050 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is:

110 µA + (5 V / 5 kΩ) = 1.11 mA (6)

The load regulation of the REF5050 is typically 0.002%/mA, which results in an error of 90 µV for the 1.1 mA current drawn from the device. This value corresponds to a 0.07 LSB error at 12 bits (DAC7311).

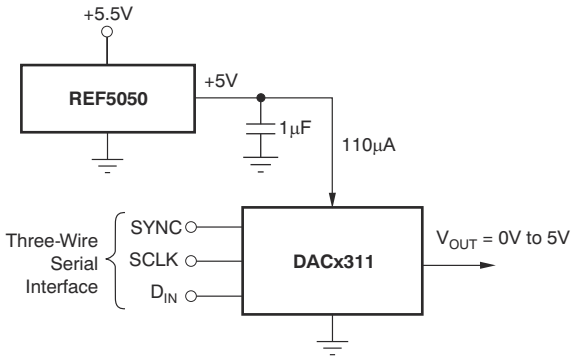

図 9-8. REF5050 as Power Supply to DACx311

For other power-supply voltages, alternative references such as the REF3030 (3 V), REF3033 (3.3 V), or REF3220 (2.048 V) are recommended. For a full list of available voltage references from TI, see the TI web site at www.ti.com.

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9.2.3 Bipolar Operation Using the DACx311

The DACx311 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in 図 9-9. The circuit shown gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an OPA211, OPA340, or OPA703 as the output amplifier. For a full list of available operational amplifiers from TI, see the TI web site at www.ti.com

The output voltage for any input code can be calculated as follows:

$$V_O = \left[AV_{DD} \times \left(\frac{D}{2^n} \right) \times \left(\frac{R_1 + R_2}{R_1} \right) - AV_{DD} \times \left(\frac{R_2}{R_1} \right) \right] \quad (7)$$

where

- n = resolution in bits; either 8 (DAC5311), 10 (DAC6311), or 12 (DAC7311).
- D = decimal equivalent of the binary code that is loaded to the DAC register. D ranges from 0 to 255 for 8-bit DAC5311, 0 to 1023 for the 10-bit DAC6311 and 0 to 4095 for the 12-bit DAC7311.

With AV_{DD} = 5 V, R_1 = R_2 = 10 kΩ:

$$V_O = \left(\frac{10 \times D}{2^n} \right) - 5V \quad (8)$$

The resulting output voltage range is ±5 V. Code 000h corresponds to a –5-V output and FFFh (12-bit level) corresponding to a +5-V output.

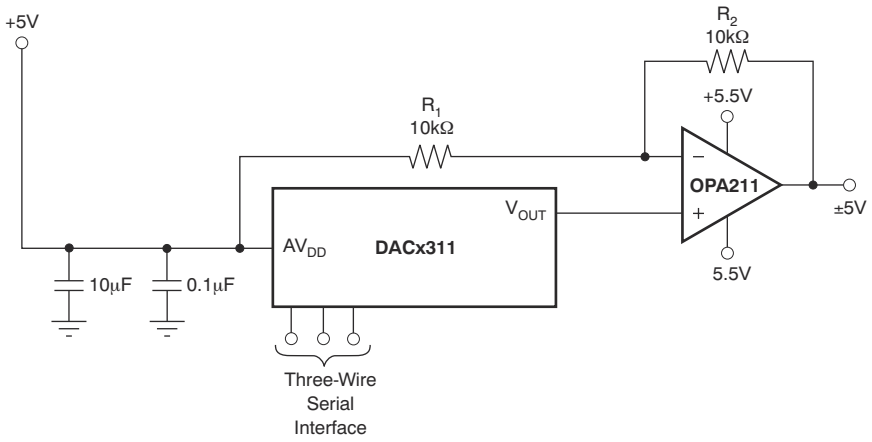

図 9-9. Bipolar Operation With the DACx311

9.3 Power Supply Recommendations

The DACx311 is designed to operate with a unipolar analog power supply ranging from 2.0 V to 5.5 V on the AV_{DD} pin. The AV_{DD} pin supplies power to the digital and analog circuits (including the resistor string) inside the DAC. The current consumption of this pin is specified in the *Electrical Characteristics* table. Use a 1 µF to 10 µF capacitor in parallel with a 0.1 µF bypass capacitor on this pin to remove high-frequency noise.

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9.4 Layout

9.4.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DACx311 offers single-supply operation, and is often used in close proximity to digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult the task is to achieve good performance from the converter.

As a result of the single ground pin of the DACx311, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND is connected directly to an analog ground plane. Separate this plane from the ground connection for the digital components until connected at the power entry point of the system.

The power applied to AV_{DD} must be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as the internal logic switches state. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. This condition is particularly true for the DACx311, as the power supply is also the reference voltage for the DAC.

As with the GND connection, connect AV_{DD} to a 5-V power supply plane or trace that is separate from the connection for digital logic until connected at the power entry point. In addition, 1-µF to 10-µF and 0.1-µF bypass capacitors are strongly recommended. In some situations, additional bypassing can be required, such as a 100 µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply and remove high-frequency noise.

9.4.2 Layout Example

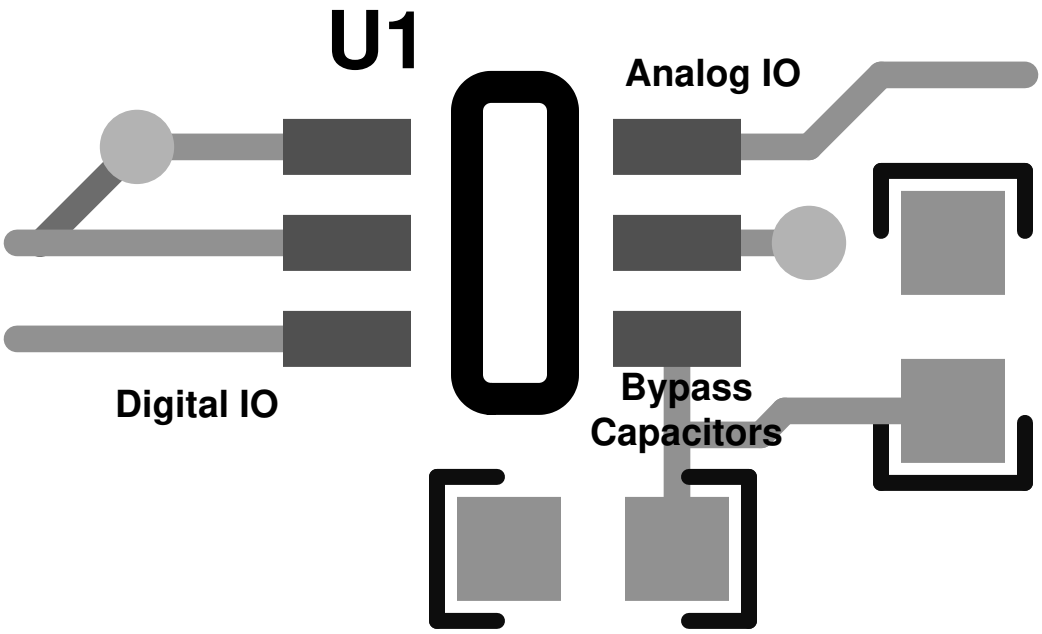

図 9-10. Recommended Layout

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10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC5311IDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53
DAC5311IDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53
DAC5311IDCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53
DAC5311IDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53
DAC5311IDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53
DAC5311IDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53
DAC6311IDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63
DAC6311IDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63
DAC6311IDCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63
DAC6311IDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63
DAC6311IDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63
DAC6311IDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63
DAC6311IDCKTG4	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63
DAC7311IDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73
DAC7311IDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73
DAC7311IDCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73
DAC7311IDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73
DAC7311IDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73
DAC7311IDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73
DAC7311IDCKTG4	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DAC5311 :

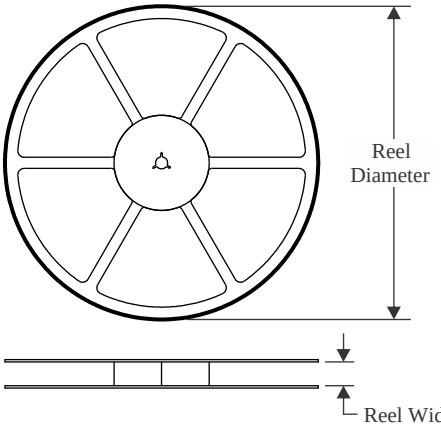
- Automotive : DAC5311-Q1

NOTE: Qualified Version Definitions:

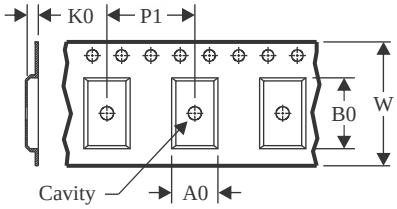
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

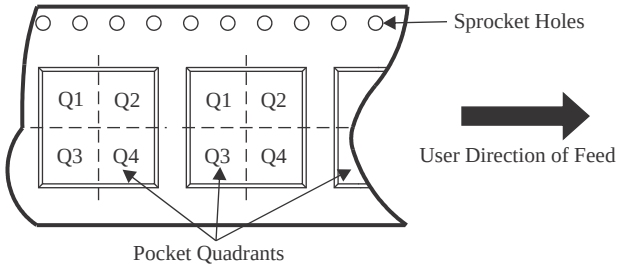


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

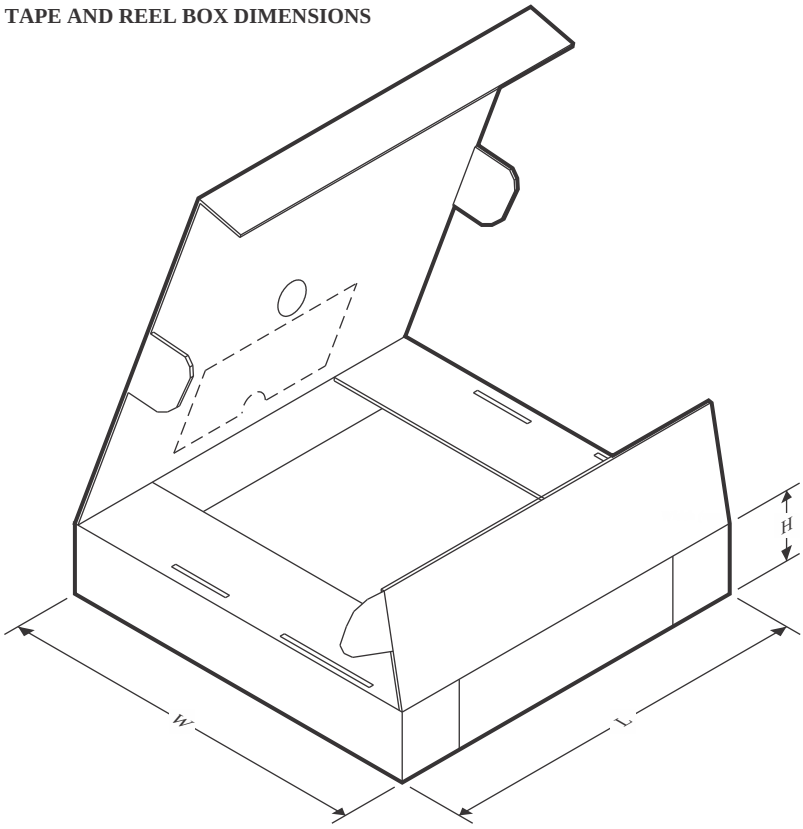
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC5311IDCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC5311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC6311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC6311IDCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC6311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC7311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC7311IDCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC7311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

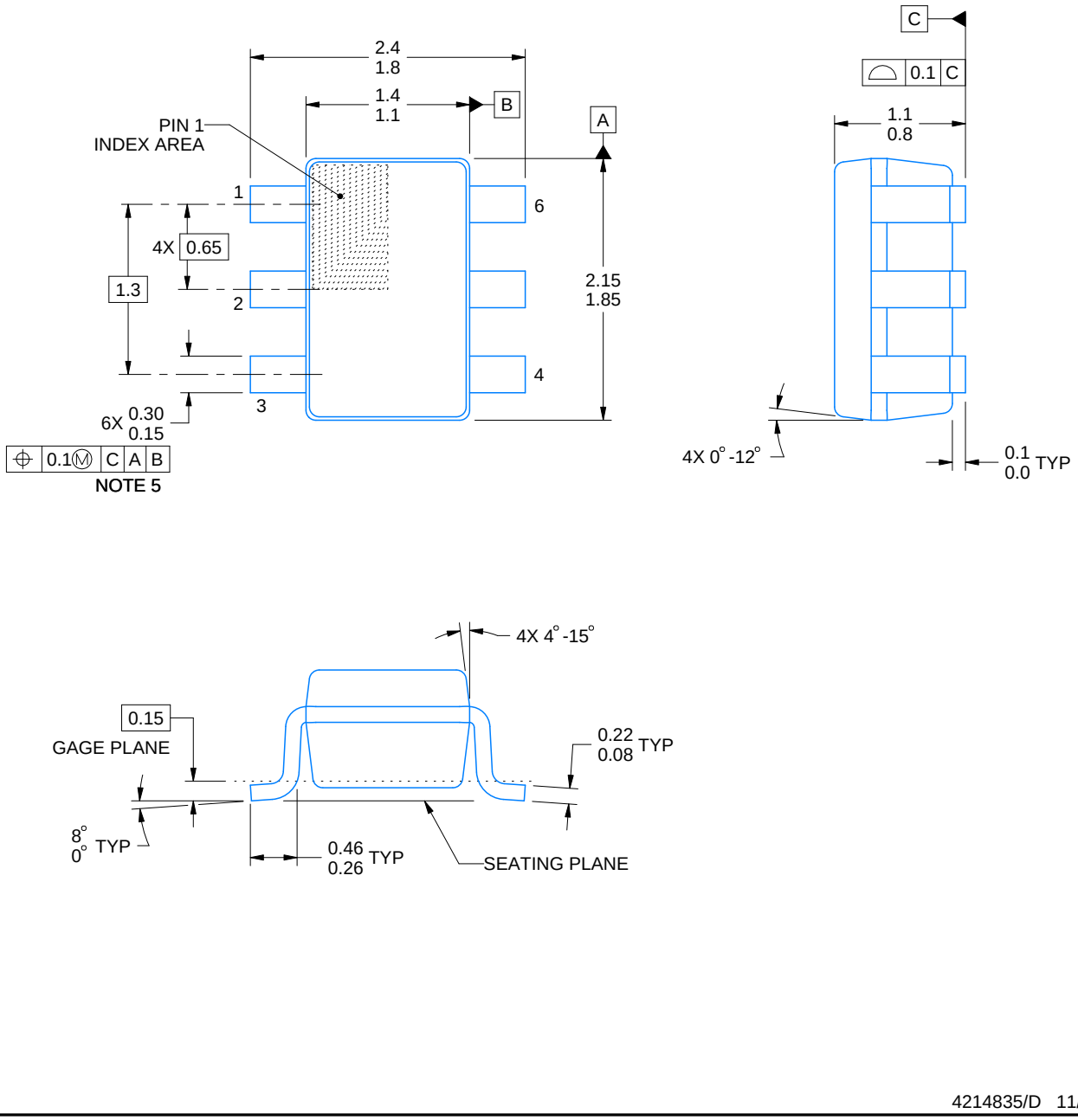
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC5311IDCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
DAC5311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
DAC6311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC6311IDCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
DAC6311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
DAC7311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC7311IDCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
DAC7311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

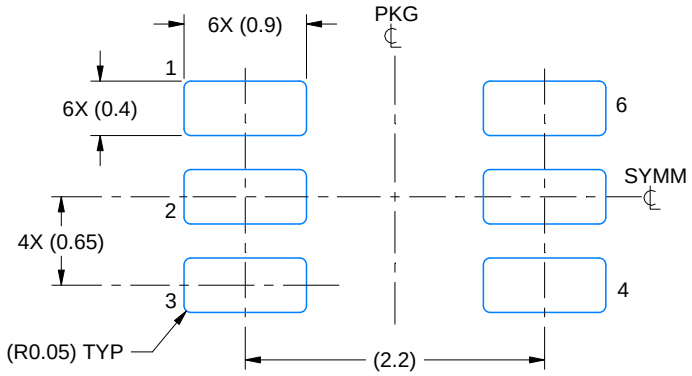
SMALL OUTLINE TRANSISTOR



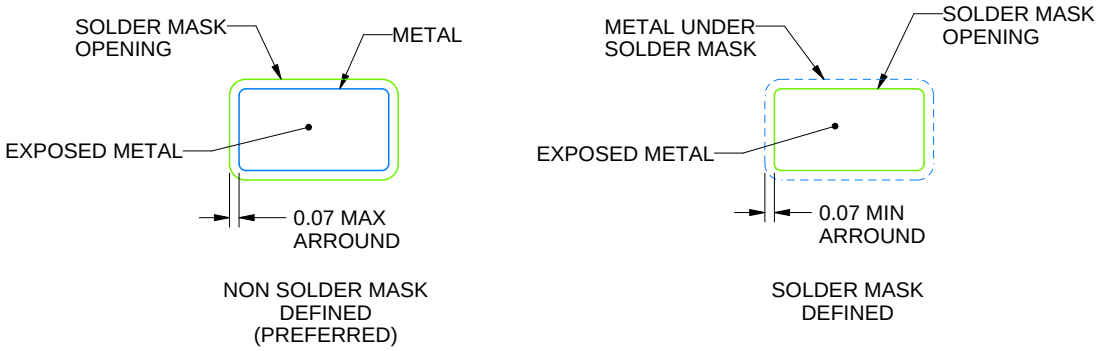
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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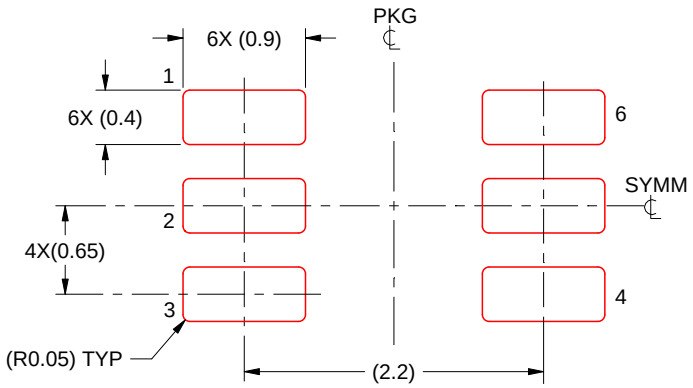
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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