16-BIT, 500 MSPS 2×–8× INTERPOLATING DUAL-CHANNEL DIGITAL-TO-ANALOG CONVERTER (DAC)

FEATURES

- **500 MSPS**
- **Selectable 2×–8× Interpolation**
- **On-Chip PLL/VCO Clock Multiplier**
- **Full IQ Compensation Including Offset, Gain, and Phase**
- **Flexible Input Options:**
  - **FIFO With Latch on External or Internal Clock**
  - **Even/Odd Multiplexed Input**
  - **Single Port Demultiplexed Input**
- **Complex Mixer With 32-Bit NCO**
- **Fixed Frequency Mixer With $f_S/4$ and $f_S/2$**
- **1.8-V or 3.3-V I/O Voltage**
- **On-Chip 1.2-V Reference**
- **Differential Scalable Output: 2 mA to 20 mA**
- **Pin Compatible to DAC5686**
- **High Performance**
  - **81-dBc ACLR WCDMA TM1 at 30.72 MHz**
  - **72-dBc ACLR WCDMA TM1 at 153.6 MHz**
- **Package: 100-Pin HTQFP**

APPLICATIONS

- **Cellular Base Transceiver Station Transmit Channel**
  - **CDMA: W-CDMA, CDMA2000, TD-SCDMA**
  - **TDMA: GSM, IS-136, EDGE/UWC-136**
  - **OFDM: 802.16**
- **Cable Modem Termination System**

DESCRIPTION

The DAC5687 is a dual-channel 16-bit high-speed digital-to-analog converter (DAC) with integrated 2×, 4×, and 8× interpolation filters, a complex numerically controlled oscillator (NCO), onboard clock multiplier, IQ compensation, and on-chip voltage reference. The DAC5687 is pin-compatible to the DAC5686, requiring only changes in register settings for most applications, and offers additional features and superior linearity, noise, crosstalk, and PLL phase noise performance.

The DAC5687 has six signal processing blocks: two interpolate-by-two digital filters, a fine frequency mixer with 32-bit NCO, a quadrature modulation compensation block, another interpolate-by-two digital filter, and a coarse frequency mixer with $f_S/2$ or $f_S/4$. The different modes of operation enable or bypass the signal processing blocks.

The coarse and fine mixers can be combined to span a wider range of frequencies with fine resolution. The DAC5687 allows both complex or real output. Combining the frequency upconversion and complex output produces a Hilbert transform pair that is output from the two DACs. An external RF quadrature modulator then performs the final single-sideband upconversion.

The IQ compensation feature allows optimization of phase, gain, and offset to maximize sideband rejection and minimize LO feedthrough for an analog quadrature modulator.

The DAC5687 includes several input options: single-port interleaved data, even and odd multiplexing at half-rate, and an input FIFO with either external or internal clock to ease the input timing ambiguity when the DAC5687 is clocked at the DAC output sample rate.

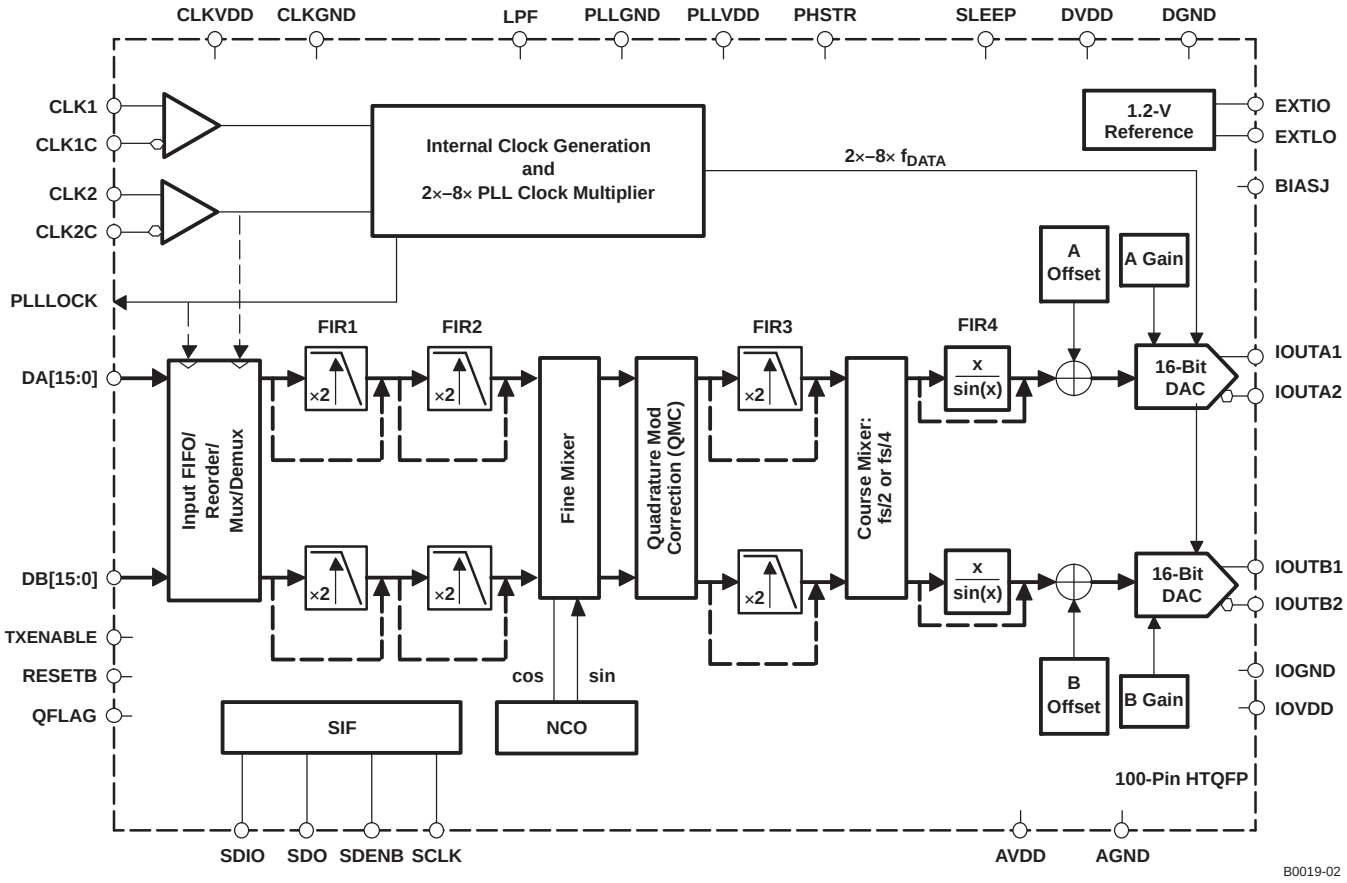
ORDERING INFORMATION

T_A	Package Device
–40°C to 85°C	100 HTQFP(1) (PZP) PowerPAD™ package, plastic quad flatpack
	DAC5687IPZP

(1) Thermal pad size: 6 mm × 6 mm.

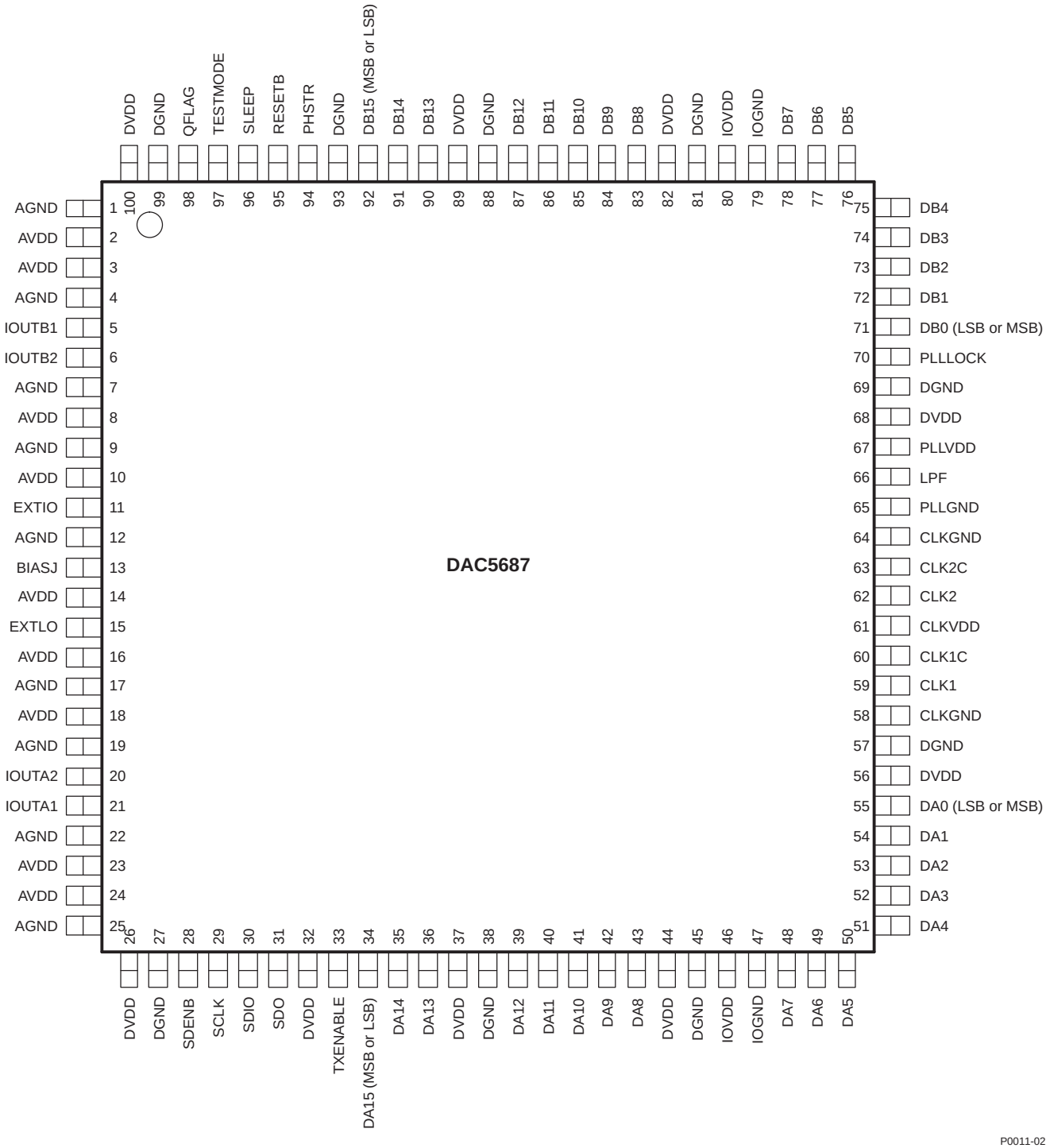
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



PINOUT

PZP PACKAGE
(TOP VIEW)



P0011-02

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	1, 4, 7, 9, 12, 17, 19, 22, 25	I	Analog ground return
AVDD	2, 3, 8, 10, 14, 16, 18, 23, 24	I	Analog supply voltage
BIASJ	13	O	Full-scale output current bias
CLK1	59	I	In PLL clock mode and dual clock modes, provides data input rate clock. In external clock mode, provides optional input data rate clock to FIFO latch. When the FIFO is disabled, CLK1 is not used and can be left unconnected.
CLK1C	60	I	Complementary input of CLK1.
CLK2	62	I	External and dual clock mode clock input. In PLL mode, CLK2 is unused and can be left unconnected.
CLK2C	63	I	Complementary input of CLK2. In PLL mode, CLK2C is unused and can be left unconnected.
CLKGND	58, 64	I	Ground return for internal clock buffer
CLKVDD	61	I	Internal clock buffer supply voltage
DA[15:0]	34–36, 39–43, 48–55	I	A-channel data bits 0 through 15. DA15 is most significant data bit (MSB). DA0 is least significant data bit (LSB). Order can be reversed by register change.
DB[15:0]	71–78, 83–87, 90–92	I	B-channel data bits 0 through 15. DB15 is most significant data bit (MSB). DB0 is least significant data bit (LSB). Order can be reversed by register change.
DGND	27, 38, 45, 57, 69, 81, 88, 93, 99	I	Digital ground return
DVDD	26, 32, 37, 44, 56, 68, 82, 89, 100	I	Digital supply voltage
EXTIO	11	I/O	Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as internal reference output when EXTLO = AGND, requires a 0.1-μF decoupling capacitor to AGND when used as reference output
EXTLO	15	I/O	Internal/external reference select. Internal reference selected when tied to AGND, external reference selected when tied to AVDD. Output only when atest is not zero (register 0x1B bits 7 to 3).
IOUTA1	21	O	A-channel DAC current output. Full scale when all input bits are set 1
IOUTA2	20	O	A-channel DAC complementary current output. Full scale when all input bits are 0
IOUTB1	5	O	B-channel DAC current output. Full scale when all input bits are set 1
IOUTB2	6	O	B-channel DAC complementary current output. Full scale when all input bits are 0
IOGND	47, 79	I	Digital I/O ground return
IOVDD	46, 80	I	Digital I/O supply voltage
LPF	66	I	PLL loop filter connection
PHSTR	94	I	Synchronization input signal that can be used to initialize the NCO, coarse mixer, internal clock divider, and/or FIFO circuits.
PLLGND	65	I	Ground return for internal PLL
PLLVDD	67	I	PLL supply voltage. When PLLVDD is 0 V, the PLL is disabled.
PLLLOCK	70	O	In PLL mode, provides PLL lock status bit or internal clock signal. PLL is locked to input clock when high. In external clock mode, provides input rate clock.
QFLAG	98	I	When qflag register is 1, the QFLAG pin is used by the user during interleaved data input mode to identify the B sample. High QFLAG indicates B sample. Must be repeated every B sample.
RESETB	95	I	Resets the chip when low. Internal pullup
SCLK	29	I	Serial interface clock
SDENB	28	I	Active-low serial data enable, always an input to the DAC5687
SDIO	30	I/O	Bidirectional serial data in three-pin interface mode, input-only in four-pin interface mode. Three-pin mode is the default after chip reset.
SDO	31	O	Serial interface data, unidirectional data output, if SDIO is an input. SDO is in the high-impedance state when the three-pin interface mode is selected (register 0x04 bit 7).

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SLEEP	96	I	Asynchronous hardware power-down input. Active-High. Internal pulldown.
TXENABLE	33	I	TXENABLE has two purposes. In all modes, TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data presented to DA[15:0] and DB[15:0] is ignored. In interleaved data mode, when the qflag register bit is cleared, TXENABLE is used to synchronizes the data to channels A and B. The first data after the rising edge of TXENABLE is treated as A data, while the next data is treated as B data, and so on.
TESTMODE	97	I	TESTMODE is DGND for the user

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
	Supply voltage range	AVDD(2)	–0.5 V to 4 V
		DVDD(3)	–0.5 V to 2.3 V
		CLKVDD(2)	–0.5 V to 4 V
		IOVDD(2)	–0.5 V to 4 V
		PLLVDD(2)	–0.5 V to 4 V
	Voltage between AGND, DGND, CLKGND, PLLGND, and IOGND		–0.5 V to 0.5 V
	Supply voltage range	AVDD to DVDD	–0.5 V to 2.6 V
		DA[15:0](4)	–0.5 V to IOVDD + 0.5 V
		DB[15:0](4)	–0.5 V to IOVDD + 0.5 V
		SLEEP(4)	–0.5 V to IOVDD + 0.5 V
		CLK1/2, CLK1/2C(3)	–0.5 V to CLKVDD + 0.5 V
		RESETB(4)	–0.5 V to IOVDD + 0.5 V
		LPF(4)	–0.5 V to PLLVDD + 0.5 V
		IOUT1, IOUT2(2)	–1 V to AVDD + 0.5 V
		EXTIO, BIASJ(2)	–0.5 V to AVDD + 0.5 V
		EXTLO(2)	–0.5 V to IAVDD + 0.5 V
	Peak input current (any input)		20 mA
	Peak total input current (all inputs)		30 mA
T_A	Operating free-air temperature range (DAC5687I)		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND.
(3) Measured with respect to DGND.
(4) Measured with respect to IOGND.

THERMAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

Thermal Conductivity		100 HTQFP	UNIT
T_J	Junction temperature(2)	105	°C
θ_{JA}	Theta junction-to-ambient (still air)	19.88	°C/W
	Theta junction-to-ambient (150 lfm) (0.762 m/s)	14.37	°C/W

(1) Air flow or heat sinking reduces θ_{JA} and is highly recommended.
(2) Air flow or heat sinking required for sustained operation at 85°C and maximum operating conditions to maintain junction temperature.

THERMAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

Thermal Conductivity		100 HTQFP	UNIT
θ_{JC}	Theta junction-to-case	0.12	°C/W

ELECTRICAL CHARACTERISTICS (DC SPECIFICATIONS)

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 19.2 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION			16			Bits
DC ACCURACY(1)						
INL	Integral nonlinearity	1 LSB = $IOUT_{FS}/2^{16}$ T_{MIN} to T_{MAX}		±4		LSB
DNL	Differential nonlinearity			±4		LSB
ANALOG OUTPUT						
	Coarse gain linearity	Worst-case error from ideal linearity		±0.04		LSB
	Fine gain linearity			±3		LSB
	Offset error	Mid code offset		0.01		%FSR
	Gain error	Without internal reference		1		%FSR
		With internal reference		0.7		%FSR
	Gain mismatch	With internal reference, dual DAC, and SSB mode	–2		2	%FSR
	Minimum full-scale output current(2)			2		mA
	Maximum full-scale output current(2)			20		mA
	Output compliance range(3)	$IOUT_{FS}$ = 20 mA	AVDD – 0.5 V		AVDD + 0.5 V	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
REFERENCE OUTPUT						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
REFERENCE INPUT						
V_{EXTIO}	Input voltage range		0.1		1.25	V
	Input resistance			1		MΩ
	Small signal bandwidth			1.4		MHz
	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift			±1		ppm of FSR/°C
	Gain drift	Without internal reference		±15		ppm of FSR/°C
		With internal reference		±30		
	Reference voltage drift			±8		ppm of FSR/°C

(1) Measured differential across IOUTA1 and IOUTA2 or IOUTB1 and IOUTB2 with 25 Ω each to AVDD.
(2) Nominal full-scale current, $IOUT_{FS}$, equals 32× the IBIAS current.
(3) The upper limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5687 device. The lower limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the limits adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high impedance input to drive any external load.

ELECTRICAL CHARACTERISTICS (DC SPECIFICATIONS) (continued)

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 19.2 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		3	3.3	3.6	V
DVDD	Digital supply voltage		1.71	1.8	2.15	V
CLKVDD	Clock supply voltage		3	3.3	3.6	V
IOVDD	I/O supply voltage		1.71		3.6	V
PLLVDD	PLL supply voltage		3	3.3	3.6	V
I_{AVDD}	Analog supply current	Mode 5(5)		41		mA
		Mode 6(5)		80		
I_{DVDD}	Digital supply current(5)	Mode 6(5)		587		mA
I_{CLKVDD}	Clock supply current(5)	Mode 6(5)		5		mA
I_{PLLVDD}	PLL supply current(5)	Mode 6(5)		20		mA
I_{IOVDD}	IO supply current(5)	Mode 6(5)		2		mA
I_{AVDD}	Sleep mode AVDD supply current	Sleep mode (SLEEP pin high), CLK2 = 500 MHz		1		mA
I_{DVDD}	Sleep mode DVDD supply current	Sleep mode (SLEEP pin high), CLK2 = 500 MHz		2		mA
I_{CLKVDD}	Sleep mode CLKVDD supply current	Sleep mode (SLEEP pin high), CLK2 = 500 MHz		0.25		mA
I_{PLLVDD}	Sleep mode PLLVDD supply current	Sleep mode (SLEEP pin high), CLK2 = 500 MHz		0.6		mA
I_{IOVDD}	Sleep mode IOVDD supply current	Sleep mode (SLEEP pin high), CLK2 = 500 MHz		0.6		mA
P_D	Power dissipation	Mode 1(5) AVDD = 3.3 V, DVDD = 1.8 V		750		mW
		Mode 2(5) AVDD = 3.3 V, DVDD = 1.8 V		910		
		Mode 3(5) AVDD = 3.3 V, DVDD = 1.8 V		760		
		Mode 4(5) AVDD = 3.3 V, DVDD = 1.8 V		1250		
		Mode 5(5) AVDD = 3.3 V, DVDD = 1.8 V		1250		
		Mode 6(5) AVDD = 3.3 V, DVDD = 1.8 V		1410		
		Mode 7(5) AVDD = 3.3 V, DVDD = 1.8 V		1400	1750	
		Sleep mode (SLEEP pin high), CLK2 = 500 MHz		11	20	
APSRR	Power supply rejection ratio		–0.2		0.2	%FSR/V
DPSRR			–0.2		0.2	%FSR/V

(5) MODE 1 – MODE 7:
a. Mode 1: X2, PLL off, CLK2 = 320 MHz, DACA and DACB on, IF = 5 MHz
b. Mode 2: X4 QMC, PLL on, CLK1 = 125 MHz, DACA and DACB on, IF = 5 MHz
c. Mode 3: X4 CMIX, PLL off, CLK2 = 500 MHz, DACA off and DACB on, IF = 150 MHz
d. Mode 4: X4L FMIX CMIX, PLL off, CLK2 = 500 MHz, DACA off and DACB on, IF = 150 MHz
e. Mode 5: X4L FMIX CMIX, PLL on, CLK1 = 125 MHz, DACA off and DACB on, IF = 150 MHz
f. Mode 6: X4L FMIX CMIX, PLL on, CLK1 = 125 MHz, DACA on and DACB on, IF = 150 MHz
g. Mode 7: X8 FMIX CMIX, PLL on, CLK1 = 62.5 MHz, DACA and DACB on, IF = 150 MHz

ELECTRICAL CHARACTERISTICS (AC SPECIFICATIONS)[1]

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V (= 3.3 V for PLL clock mode), IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 19.2 mA, external clock mode, 4:1 transformer output termination, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
f_{CLK}	Maximum output update rate		500			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10.4		ns
t_{pd}	Output propagation delay			3		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%			2		ns
$t_{f(IOUT)}$	Output fall time 90% to 10%			2		ns
AC PERFORMANCE						
SFDR	Spurious free dynamic range[2]	X2, PLL off, CLK2 = 250 MHz, DAC A and DAC B on, IF = 5.1 MHz, first Nyquist zone < $f_{DATA}/2$		78		dBc
		X4, PLL off, CLK2 = 500 MHz, DAC A and DAC B on, IF = 5.1 MHz, first Nyquist zone < $f_{DATA}/2$		77		
		X4, CLK2 = 500 MHz, DAC A and DAC B on, IF = 20.1 MHz, PLL on for MIN, PLL off for TYP, first Nyquist zone < $f_{DATA}/2$	68[3]	76		
SNR	Signal-to-noise ratio	X4, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, single tone, 0 dBFS, IF = 20.1 MHz		73		dBc
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 70.1 MHz		65		
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, single tone, 0 dBFS, IF = 150.1 MHz		57		
		X4 FMIX CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, single tone, 0 dBFS, IF = 180.1 MHz		54		
		X4, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, four tones, each –12 dBFS, IF = 24.7, 24.9, 25.1, 25.3 MHz		73		
IMD3	Third-order two-tone intermodulation (each tone at –6 dBFS)	X4, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 20.1 and 21.1 MHz		79		dBc
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 70.1 and 71.1 MHz		73		
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF= 150.1 and 151.1 MHz		68		
		X4 FMIX CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 180.1 and 181.1 MHz		67		
IMD	Four-tone intermodulation to Nyquist (each tone at –12 dBFS)	X4 CMIX, CLK2 = 500 MHz, f_{OUT} = 149.2, 149.6, 150.4, and 150.8 MHz		66		dBc

(1) Measured single ended into 50-Ω load.
(2) See the *Non-Harmonic Clock Related Spurious Signals* section for information on spurious products out of band (< $f_{DATA}/2$).
(3) 1:1 transformer output termination.

ELECTRICAL CHARACTERISTICS (AC SPECIFICATIONS) (continued)

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V (= 3.3 V for PLL clock mode), IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 19.2 mA, external clock mode, 4:1 transformer output termination, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACLR[4]	Adjacent channel leakage ratio	Single carrier, baseband, X4, PLL clock mode, CLK1 = 122.88 MHz		78.4		dBc
		Single carrier, baseband, X4, PLL clock mode, CLK2 = 491.52 MHz		78.5		
		Single carrier, IF = 153.6 MHz, X4 CMIX, external clock mode, CLK2 = 491.52 MHz		70.9		
		Two carrier, IF = 153.6 MHz, X4 CMIX, external clock mode, CLK2 = 491.52 MHz		67.8		
		Four carrier, baseband, X4, external clock mode, CLK2 = 491.52 MHz		76.1		
		Four carrier, IF = 92.16 MHz, X4L, external clock mode, CLK2 = 491.52 MHz		66.8		
		Single carrier, IF = 153.6 MHz, X4 CMIX, external clock mode, CLK2 = 491.52 MHz, DVDD = 2.1 V		72.2		
		Two carrier, IF = 153.6 MHz, X4 CMIX, external clock mode, CLK2 = 491.52 MHz, DVDD = 2.1 V		69.3		
		Four carrier, baseband, X4, external clock mode, CLK2 = 491.52 MHz, DVDD = 2.1 V		68.5		
		Four carrier, IF = 92.16 MHz, X4L, external clock mode, CLK2 = 491.52 MHz, DVDD = 2.1 V		66.3		
	Noise floor	50-MHz offset, 1-MHz BW, single carrier, baseband, X4, external clock mode, CLK2 = 491.52 MHz		92		dBc
		50-MHz offset, 1-MHz BW, four carrier, baseband, X4, external clock mode, CLK2 = 491.52 MHz		81		
		50-MHz offset, 1-MHz BW, single carrier, baseband, X4, PLL clock mode, CLK1 = 122.88 MHz		88		
		50-MHz offset, 1-MHz BW, four carrier, baseband, X4, PLL clock mode, CLK1 = 122.88 MHz		81		

(4) W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF. TESTMODEL 1, 10 ms

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS)

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 19.2 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE						
V_{IH}	High-level input voltage		2	3		V
V_{IL}	Low-level input voltage		0	0	0.8	V
V_{IH}	High-level input voltage	IOVDD = 1.8 V	1.26			V
V_{IL}	Low-level input voltage	IOVDD = 1.8 V			0.54	V
I_{IH}	High-level input current		–40		40	µA
I_{IL}	Low-level input current		–40		40	µA
	Input capacitance			5		pF
V_{OH}	PLLLOCK, SDO, SDIO	I_{load} = –100 µA	IOVDD – 0.2			V
		I_{load} = –8 mA	0.8 IOVDD			
V_{OL}	PLLLOCK, SDO, SDIO	I_{load} = 100 µA			0.2	V
		I_{load} = 8 mA			0.22 IOVDD	
	Input data rate	External or dual-clock modes	0		250	MSPS
		PLL clock mode	2.5		160	

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS) (continued)

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 19.2 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL						
	Phase noise	At 600-kHz offset, measured at DAC output, 25-MHz, 0-dBFS tone, f_{DATA} = 125 MSPS, 4× interpolation, pll_freq = 1, pll_kv = 0		133		dBc/Hz
		At 6-MHz offset, measured at DAC output, 25 MHz 0-dBFS tone, 125 MSPS, 4× interpolation, pll_freq = 1, pll_kv = 0		148.5		
	VCO maximum frequency	pll_freq = 0, pll_kv = 1	370			MHz
		pll_freq = 0, pll_kv = 0	480			
		pll_freq = 1, pll_kv = 1	495			
		pll_freq = 1, pll_kv = 0	520			
	VCO minimum frequency	pll_freq = 0, pll_kv = 1			225	MHz
		pll_freq = 0, pll_kv = 0			200	
		pll_freq = 1, pll_kv = 1			480	
		pll_freq = 1, pll_kv = 0			480	
NCO and QMC BLOCKS						
	QMC clock rate				320	MHz
	NCO clock rate				320	MHz
SERIAL PORT TIMING						
$t_{s(SDENB)}$	Setup time, SDENB to rising edge of SCLK		20			ns
$t_{s(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK		10			ns
$t_{h(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK		5			ns
t_{SCLK}	Period of SCLK		100			ns
t_{SCLKH}	High time of SCLK		40			ns
t_{SCLK}	Low time of SCLK		40			ns
$t_{d(Data)}$	Data output delay after falling edge of SCLK			10		ns
CLOCK INPUT (CLK1/CLK1C, CLK2/CLK2C)						
	Duty cycle		40%		60%	
	Differential voltage		0.4	1		V
TIMING PARALLEL DATA INPUT: CLK1 LATCHING MODES (PLL Mode – See Figure 45, Dual Clock Mode FIFO Disabled – See Figure 47, Dual Clock Mode With FIFO Enabled – See Figure 48)						
$t_{s(DATA)}$	Setup time, DATA valid to rising edge of CLK1		0.5			ns
$t_{h(DATA)}$	Hold time, DATA valid after rising edge of CLK1		1.5			ns
t_align	Maximum offset between CLK1 and CLK2 rising edges – dual clock mode with FIFO disabled				$\frac{1}{2f_{CLK2}} - 0.5$	ns
Timing Parallel Data Input (External Clock Mode, Latch on PLLLOCK Rising Edge, CLK2 Clock Input, See Figure 43)						
$t_{s(DATA)}$	Setup time, DATA valid to rising edge of PLLLOCK	72-Ω load on PLLLOCK	0.5			ns
$t_{h(DATA)}$	Hold time, DATA valid after rising edge of PLLLOCK	72-Ω load on PLLLOCK	1.5			ns
$t_{delay(Pllock)}$	Delay from CLK2 rising edge to PLLLOCK rising edge	72-Ω load on PLLLOCK. Note that PLLLOCK delay increases with a lower-impedance load.		4.5		ns
Timing Parallel Data Input (External Clock Mode, Latch on PLLLOCK Falling Edge, CLK2 Clock Input, See Figure 44)						
$t_{s(DATA)}$	Setup time, DATA valid to falling edge of PLLLOCK	High-impedance load on PLLLOCK	0.5			ns
$t_{h(DATA)}$	Hold time, DATA valid after falling edge of PLLLOCK	High-impedance load on PLLLOCK	1.5			ns
$t_{delay(Pllock)}$	Delay from CLK2 rising edge to PLLLOCK *rising* edge	High-impedance load on PLLLOCK. Note that PLLLOCK delay increases with a lower-impedance load.		4.5		ns

Typical Characteristics

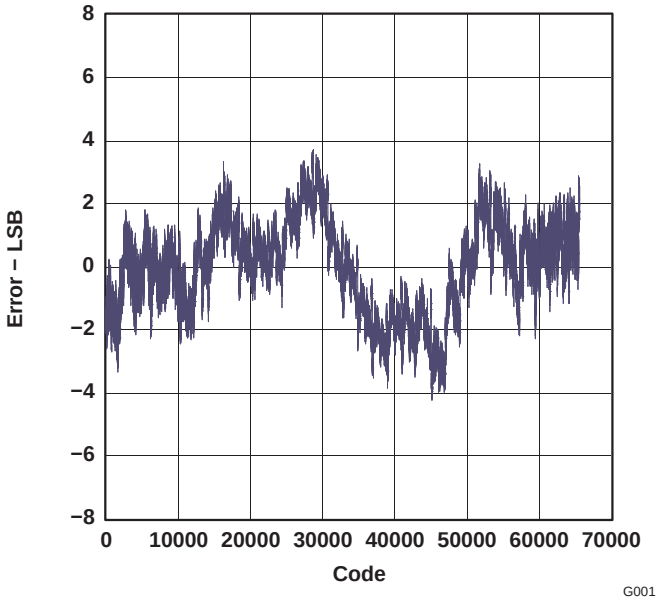


Figure 1. Integral Nonlinearity

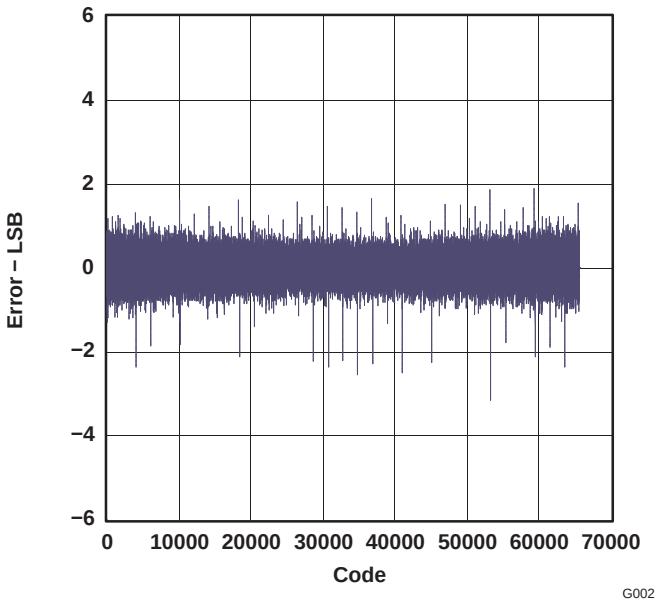


Figure 2. Differential Nonlinearity

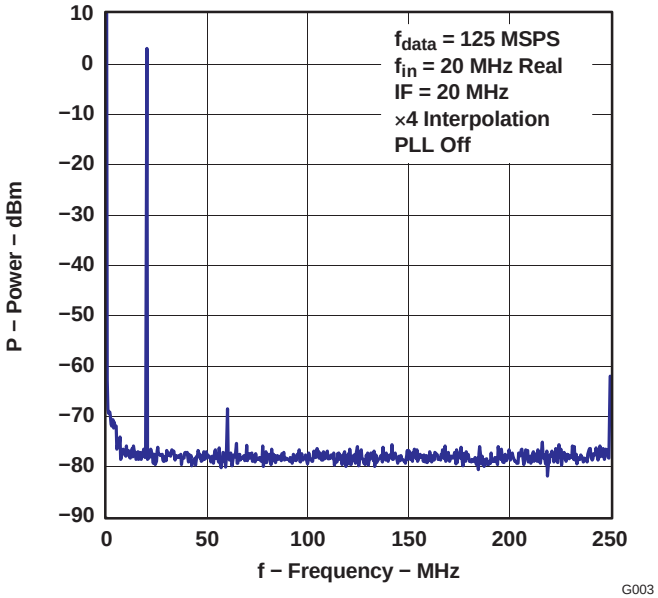


Figure 3. Single-Tone Spectral Plot

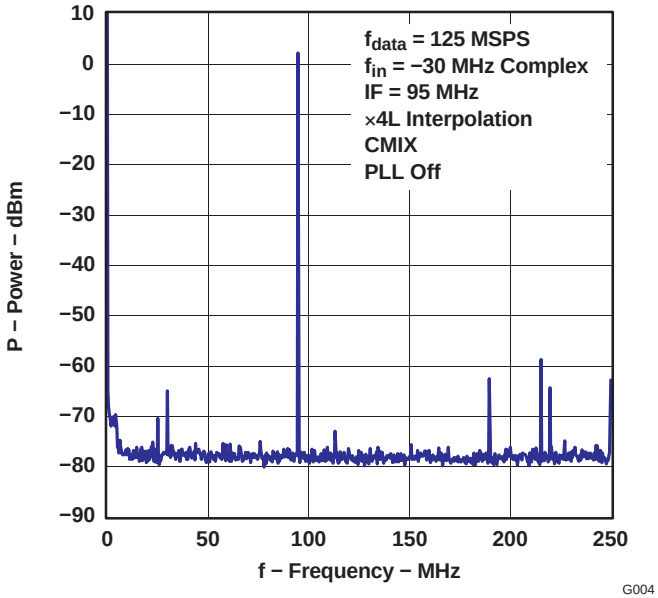


Figure 4. Single-Tone Spectral Plot

Typical Characteristics (continued)

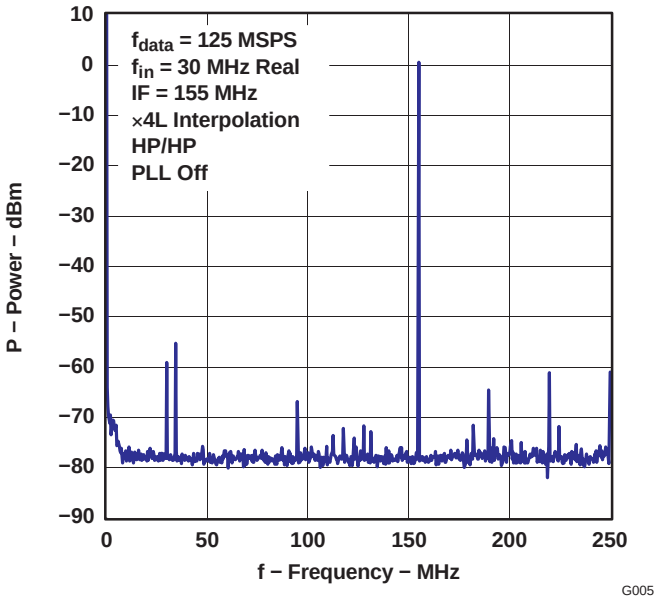


Figure 5. Single-Tone Spectral Plot

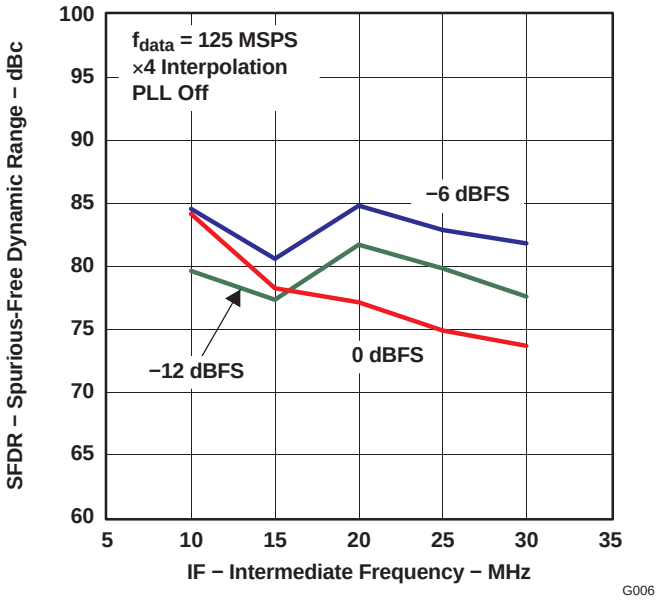


Figure 6. In-Band SFDR vs Intermediate Frequency

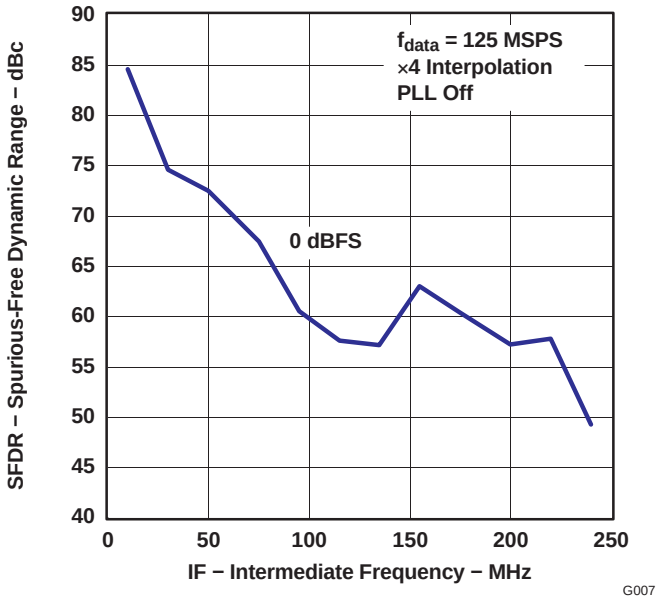


Figure 7. Out-of-Band SFDR vs Intermediate Frequency

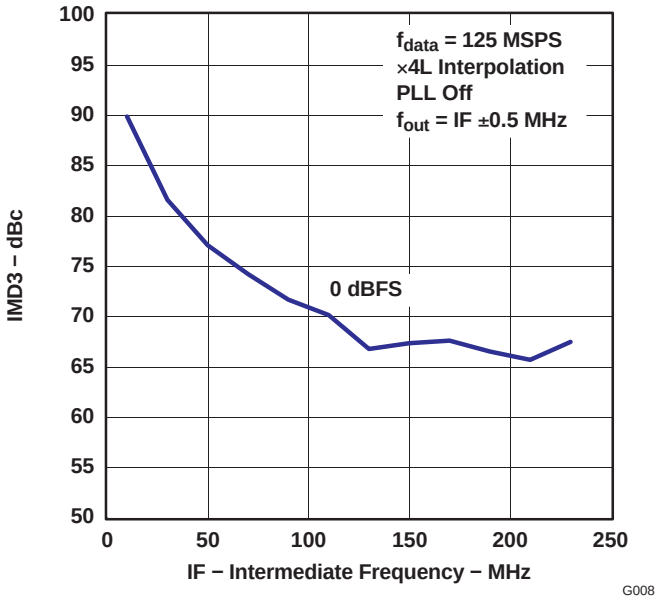


Figure 8. Two-Tone IMD vs Intermediate Frequency

Typical Characteristics (continued)

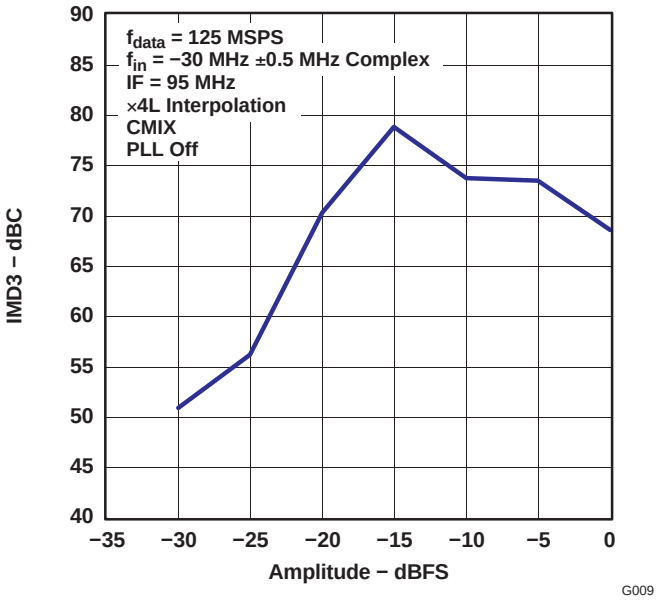


Figure 9. Two-Tone IMD vs Amplitude

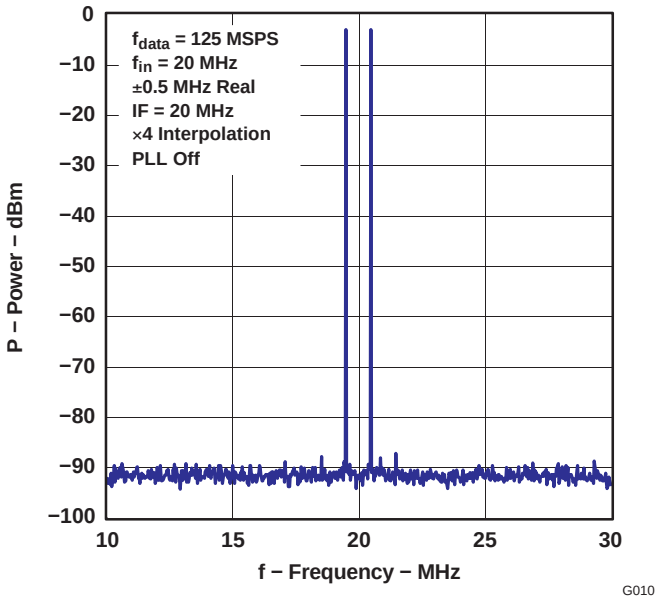


Figure 10. Two-Tone IMD Spectral Plot

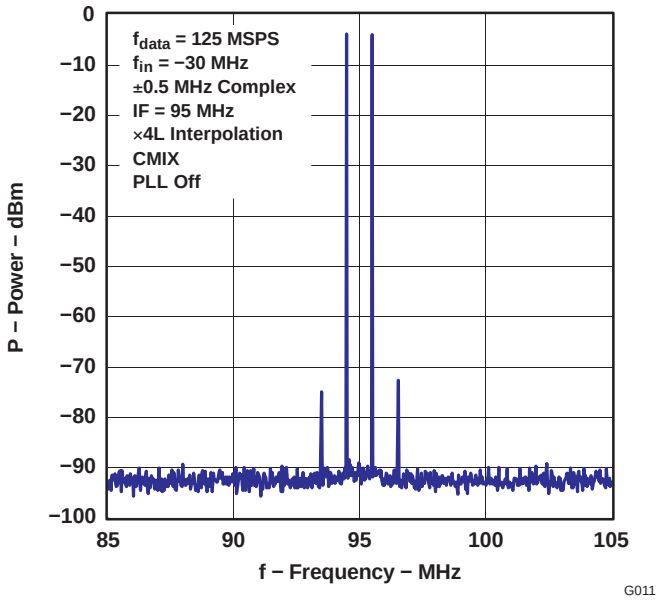


Figure 11. Two-Tone IMD Spectral Plot

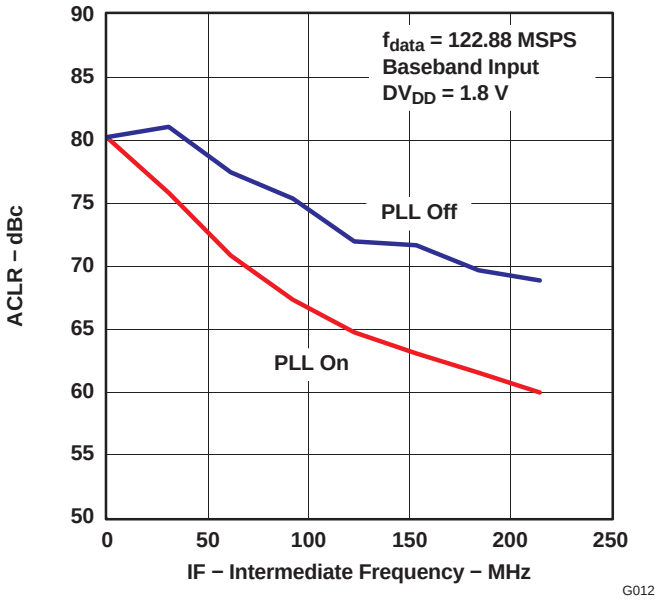


Figure 12. WCDMA ACLR vs Intermediate Frequency

Typical Characteristics (continued)

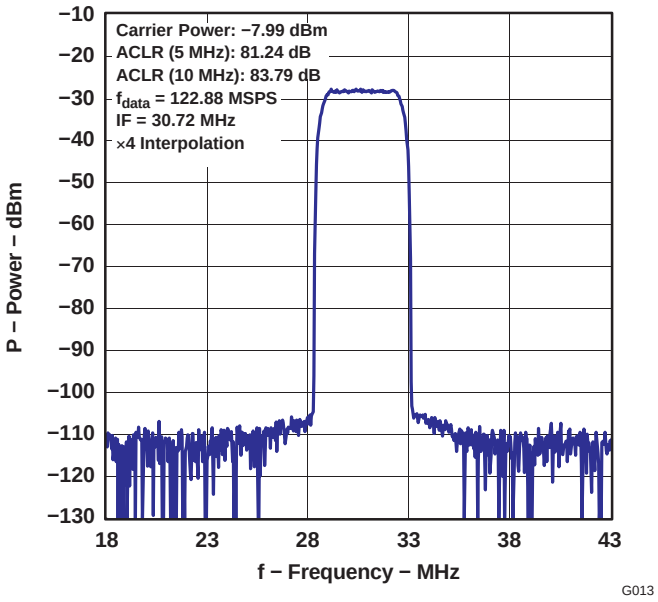


Figure 13. WCDMA TM1: Single Carrier, PLL Off, DVDD = 1.8 V

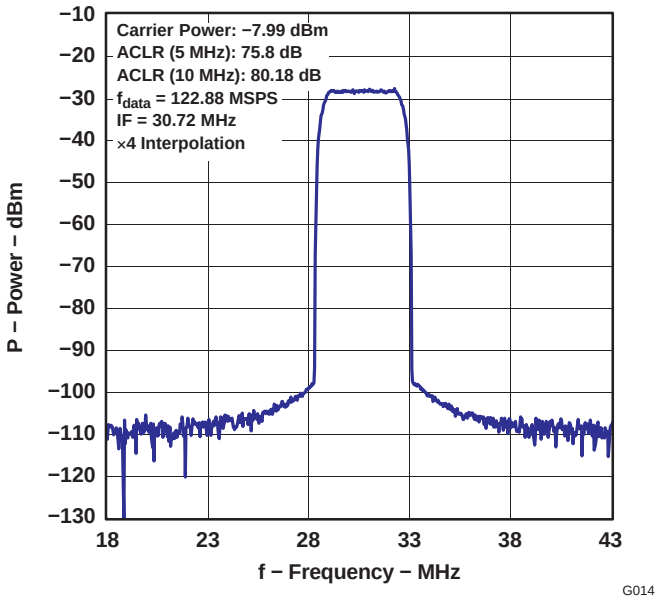


Figure 14. WCDMA TM1: Single Carrier, PLL On, DVDD = 1.8 V

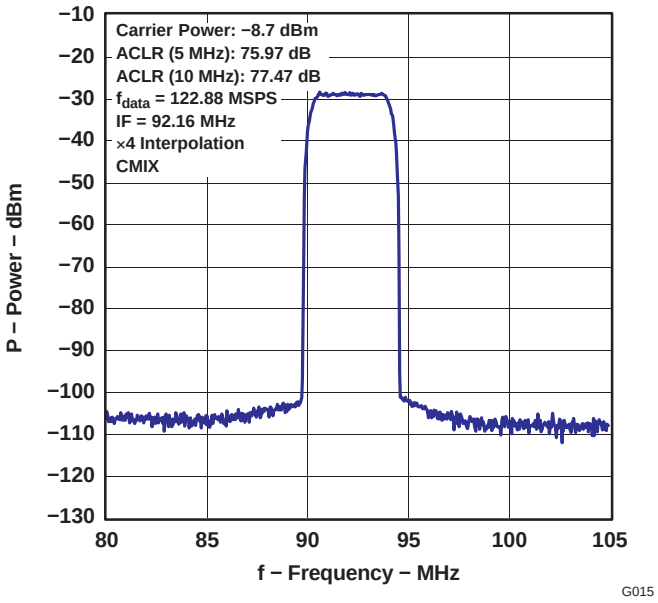


Figure 15. WCDMA TM1: Single Carrier, PLL Off, DVDD = 1.8 V

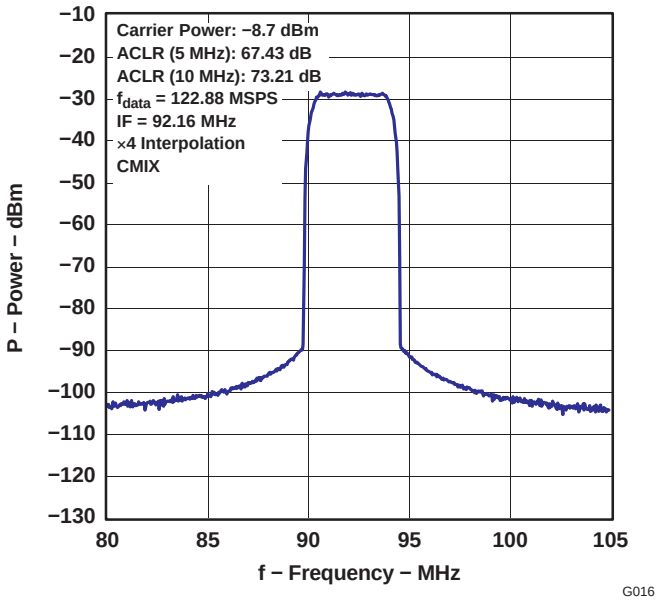


Figure 16. WCDMA TM1: Single Carrier, PLL On, DVDD = 1.8 V

Typical Characteristics (continued)

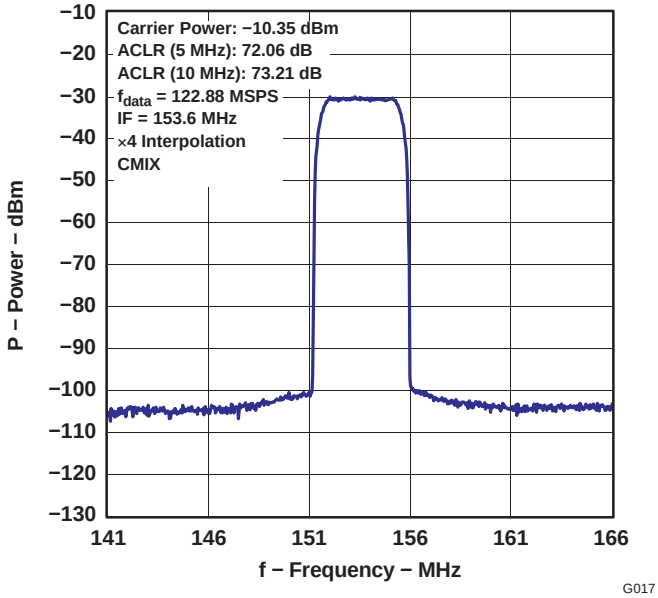


Figure 17. WCDMA TM1: Single Carrier, PLL Off, DVDD = 1.8 V

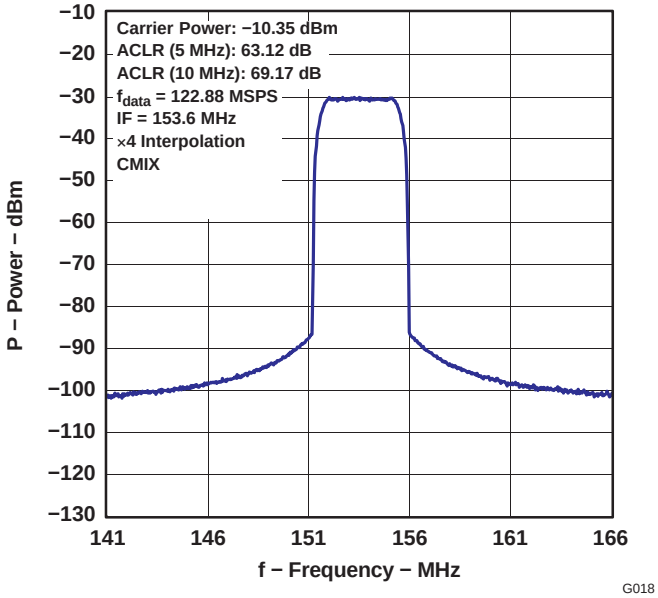


Figure 18. WCDMA TM1: Single Carrier, PLL On, DVDD = 1.8 V

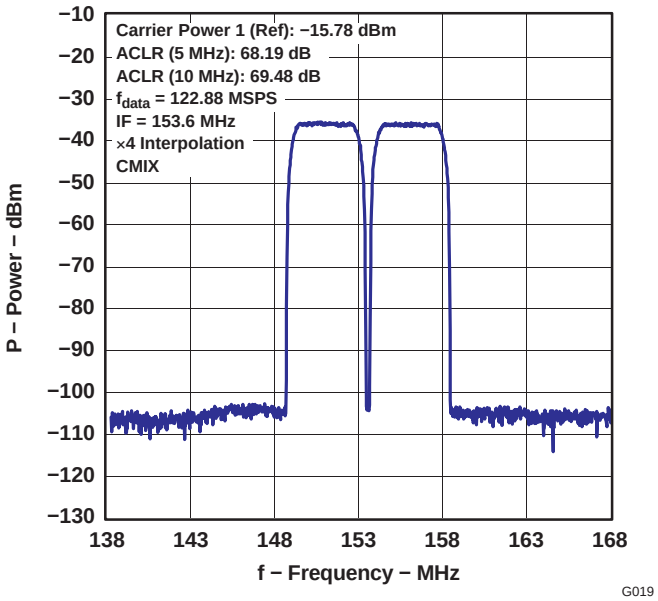


Figure 19. WCDMA TM1: Two Carriers, PLL Off, DVDD = 1.8 V

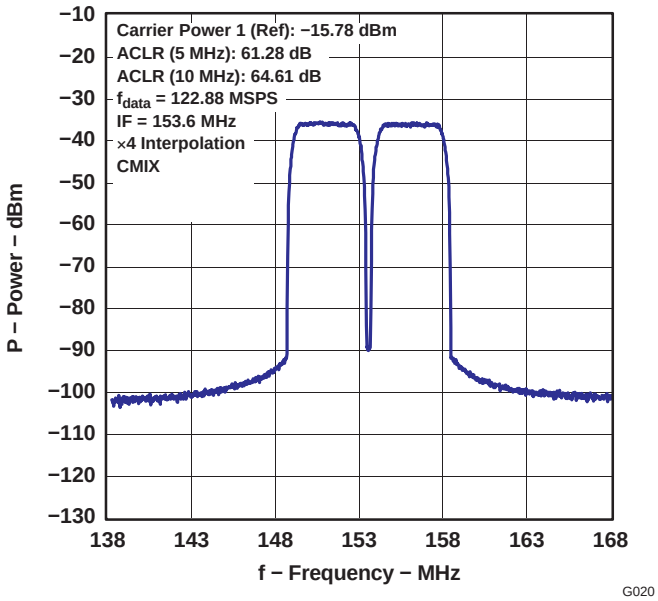


Figure 20. WCDMA TM1: Two Carriers, PLL On, DVDD = 1.8 V

Typical Characteristics (continued)

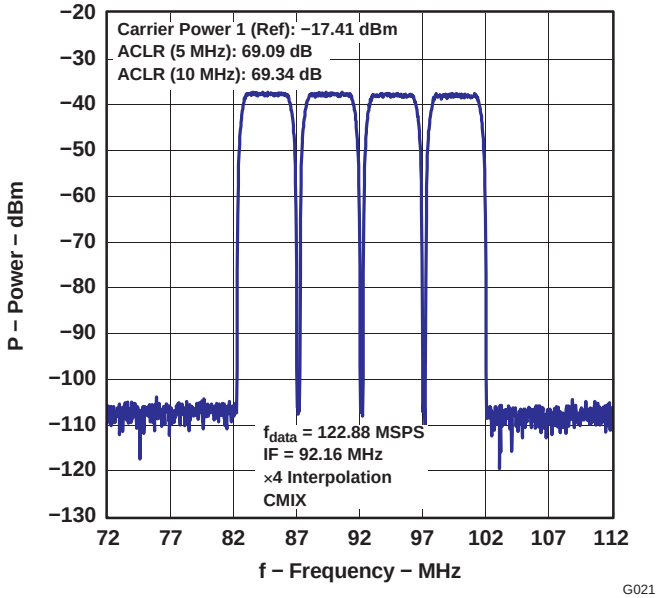


Figure 21. WCDMA TM1: Four Carriers, PLL Off, DVDD = 1.8 V

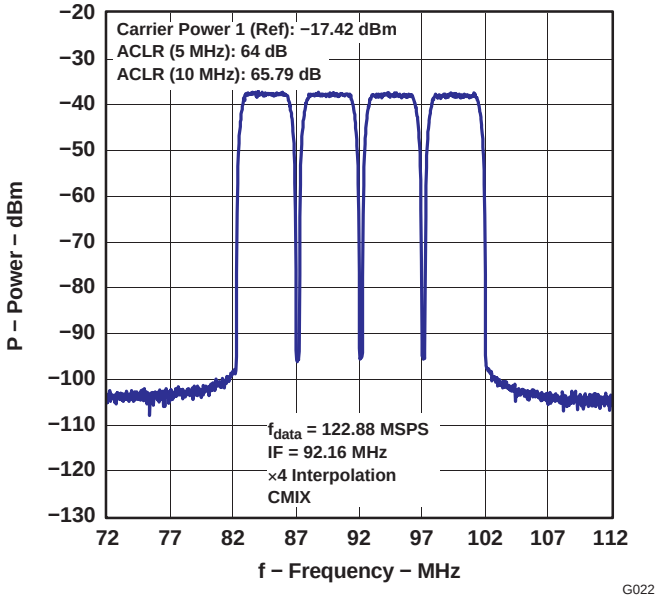


Figure 22. WCDMA TM1: Four Carriers, PLL On, DVDD = 1.8 V

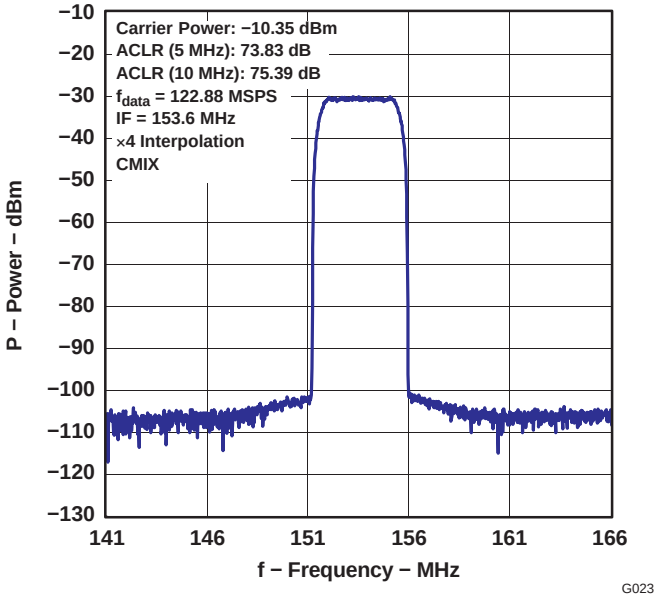


Figure 23. WCDMA TM1: Single Carrier, PLL Off, DVDD = 2.1 V

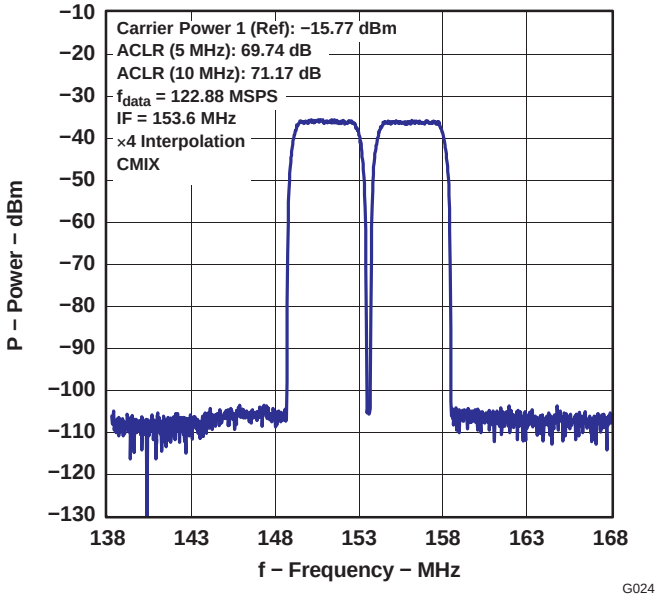


Figure 24. WCDMA TM1: Two Carriers, PLL Off, DVDD = 2.1 V

Typical Characteristics (continued)

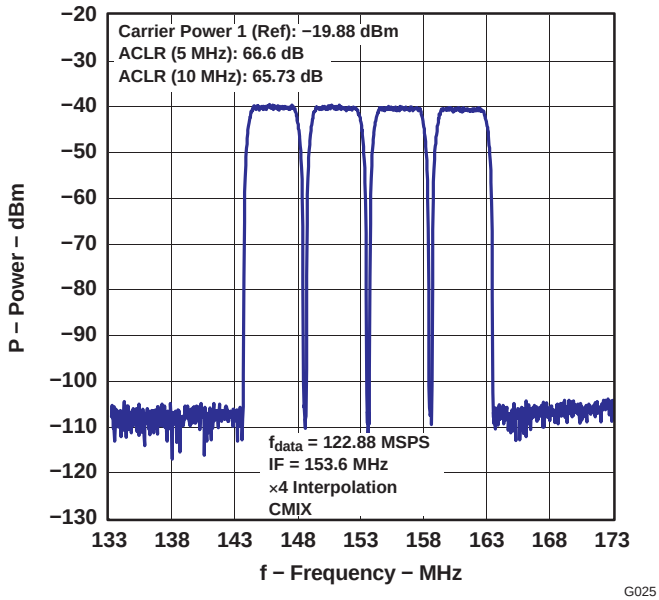


Figure 25. WCDMA TM1: Four Carriers, PLL Off, DVDD = 2.1 V

Test Methodology

Typical ac specifications in external clock mode were characterized with the DAC5687EVM using the test configuration shown in Figure 26. The DAC sample-rate clock f_{DAC} is generated by an HP8665B signal generator. An Agilent 8133A pulse generator is used to divide f_{DAC} for the data-rate clock f_{DATA} for the Agilent 16702A pattern-generator clock and provide adjustable skew to the DAC input clock. The 8133A f_{DAC} output is set to 1 V_{PP}, equivalent to 2-V_{PP} differential at CLK2/CLK2C pins. Alternatively, the DAC5687 PLLLOCK output can be used for the pattern generator clock.

The DAC5687 output is characterized with a Rohde & Schwarz FSQ8 spectrum analyzer. For WCDMA signal characterization, it is important to use a spectrum analyzer with high IP3 and noise subtraction capability so that the spectrum analyzer does not limit the ACPR measurement. For all specifications, both DACA and DACB are measured and the lowest value used as the specification.

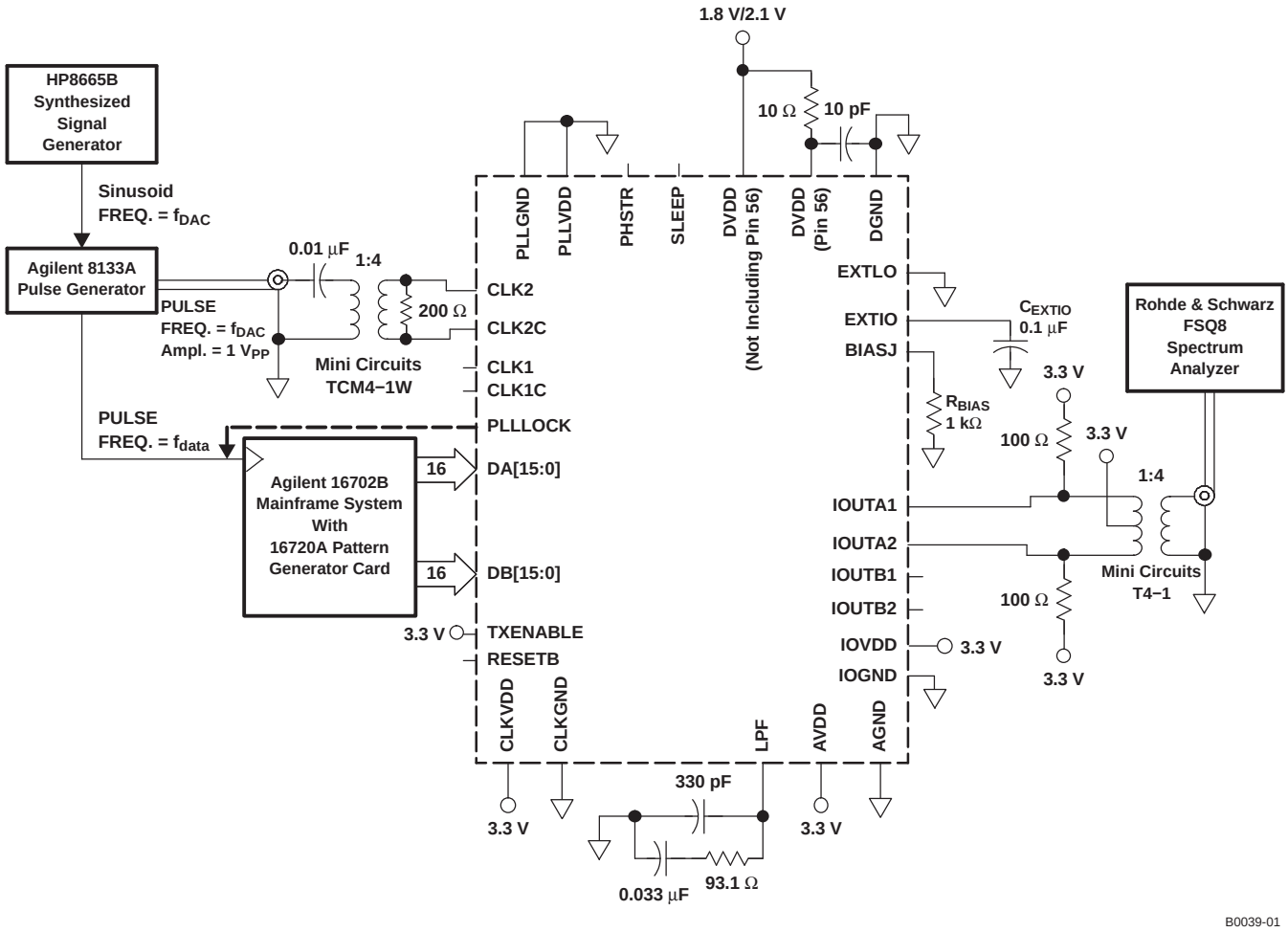


Figure 26. DAC5687 Test Configuration for External Clock Mode

PLL clock mode was characterized using the test configuration shown in Figure 27. The DAC data rate clock f_{DATA} is generated by an HP8665B signal generator. An Agilent 8133A pulse generator is used to generate a clock f_{DATA} for the Agilent 16702A pattern-generator clock and provide adjustable skew to the DAC input clock. The 8133A f_{DAC} output is set to 1 V_{PP}, equivalent to 2-V_{PP} differential at CLK1/CLK1C pins. Alternatively, the DAC5687 PLLLOCK output can be used for the pattern-generator clock.

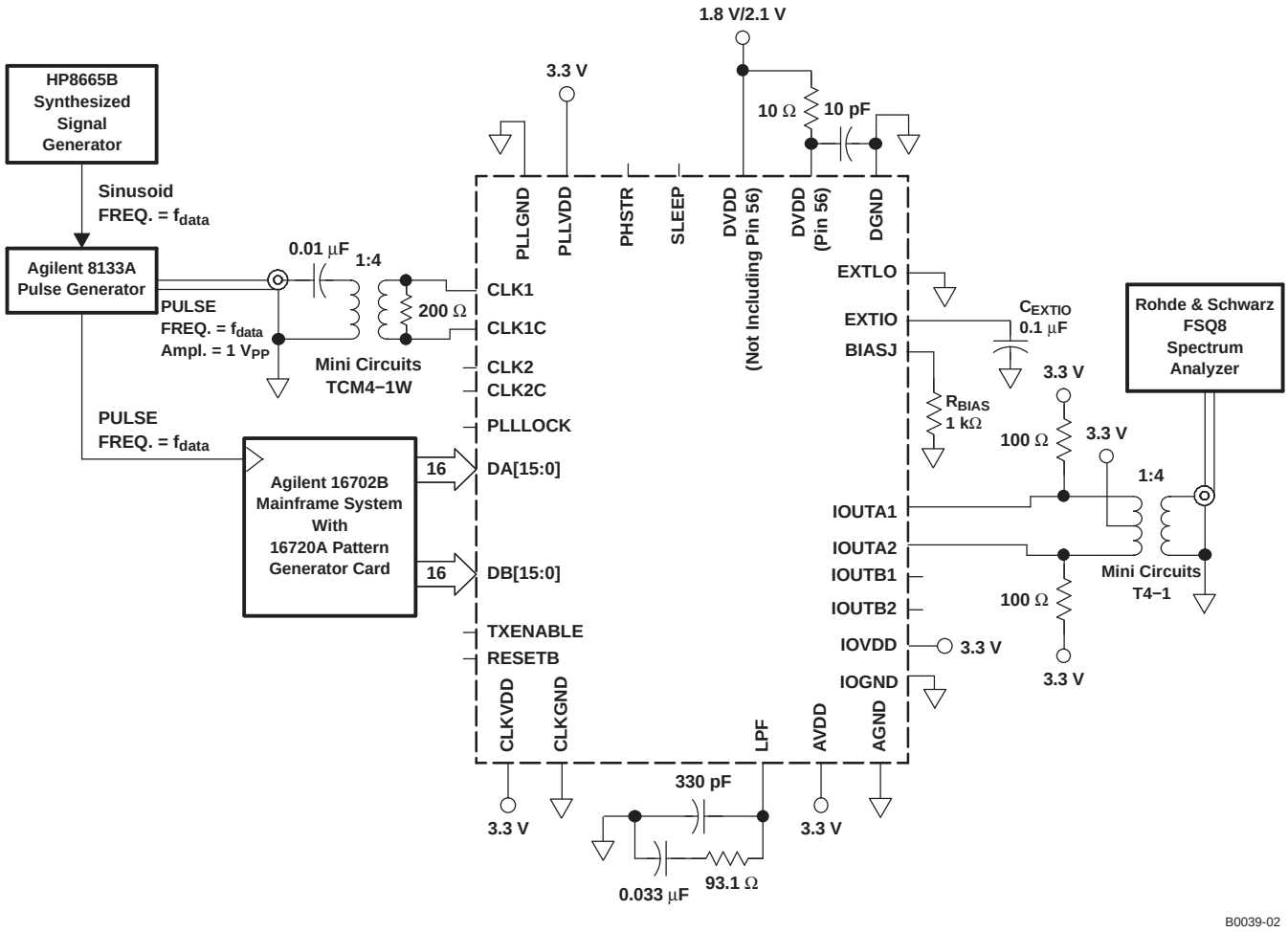


Figure 27. DAC5687 Test Configuration for PLL Clock Mode

WCDMA test-model-1 test vectors for the DAC5687 characterization were generated in accordance with the 3GPP Technical Specification. Chip-rate data was generated using the test-model-1 block in the Agilent ADS. For multicarrier signals, different random seeds and PN offsets were used for each carrier. A Matlab™ script performed pulse shaping, interpolation to the DAC input data rate, frequency offsets, rounding, and scaling. Each test vector is 10 ms long, representing one frame. Special care is taken to assure that the end of the file wraps smoothly to the beginning of the file.

The cumulative complementary distribution function (CCDF) for the 1-, 2-, and 4-carrier test vectors is shown in Figure 28. The test vectors are scaled such that the absolute maximum data point is 0.95 (–0.45 dB) of full scale. No peak reduction is used.

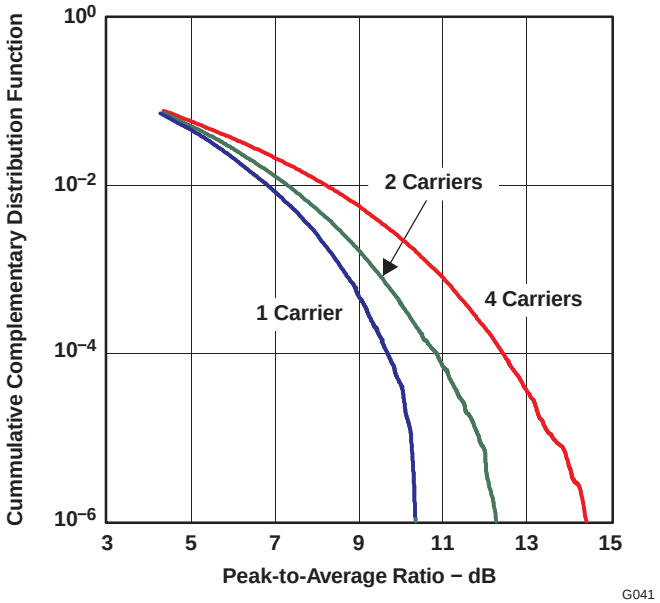


Figure 28. WCDMA TM1 Cumulative Complementary Distribution Function for 1, 2, and 4 Carriers

DETAILED DESCRIPTION

Modes of Operation

The DAC5687 has six digital signal processing blocks: FIR1 and FIR2 (interpolate-by-two digital filters), FMIX (fine frequency mixer), QMC (quadrature modulation phase correction), FIR3 (interpolate-by-two digital filter) and CMIX (coarse frequency mixer). The modes of operation, listed in Table 1, enable or bypass the blocks to produce different results. The modes are selected by registers CONFIG1, CONFIG2, and CONFIG3 (0x02, 0x03, and 0x04). Block diagrams for each mode (X2, X4, X4L, and X8) are shown in Figure 29 through Figure 32.

Table 1. DAC5687 Modes of Operation

MODE	FIR1	FIR2	FMIX	QMC	FIR3	CMIX
FULL BYPASS	–	–	–	–	–	–
X2	–	–	–	–	ON	–
X2 FMIX	–	–	ON	–	ON	–
X2 QMC	–	–	–	ON	ON	–
X2 FMIX QMC	–	–	ON	ON	ON	–
X2 CMIX	–	–	–	–	ON	ON
X2 FMIX CMIX	–	–	ON	–	ON	ON
X2 QMC CMIX	–	–	–	ON(1)	ON	ON
X2 FMIX QMC CMIX	–	–	ON	ON(1)	ON	ON
X4	ON	ON	–	–	–	–
X4 FMIX(2)	ON	ON	ON	–	–	–
X4 QMC(2)	ON	ON	–	ON	–	–
X4 FMIX QMC	ON	ON	ON	ON	–	–
X4 CMIX	ON	ON	–	–	–	ON
X4L	ON	–	–	–	ON	–

(1) The QMC phase correction is eliminated by the CMIX, so the QMC phase should be set to zero. The QMC gain settings can still be used to adjust the signal path gain as needed.
(2) f_{DAC} limited to maximum clock rate for the NCO and QMC (see Electrical Characteristics (AC Specifications)).

Table 1. DAC5687 Modes of Operation (continued)

MODE	FIR1	FIR2	FMIX	QMC	FIR3	CMIX
X4L FMIX	ON	–	ON	–	ON	–
X4L QMC	ON	–	–	ON	ON	–
X4L FMIX QMC	ON	–	ON	ON	ON	–
X4L CMIX	ON	–	–	–	ON	ON
X4L FMIX CMIX	ON	–	ON		ON	ON
X4L QMC CMIX	ON	–	–	ON(2)	ON	ON
X4L FMIX QMC CMIX	ON	–	ON	ON(2)	ON	ON
X8	ON	ON	–	–	ON	–
X8 FMIX	ON	ON	ON	–	ON	–
X8 QMC	ON	ON	–	ON	ON	–
X8 FMIX QMC	ON	ON	ON	ON	ON	–
X8 CMIX	ON	ON	–	–	ON	ON
X8 FMIX CMIX	ON	ON	ON	–	ON	ON
X8 QMC CMIX	ON	ON	–	ON(1)	ON	ON
X8 FMIX QMC CMIX	ON	ON	ON	ON(1)	ON	ON

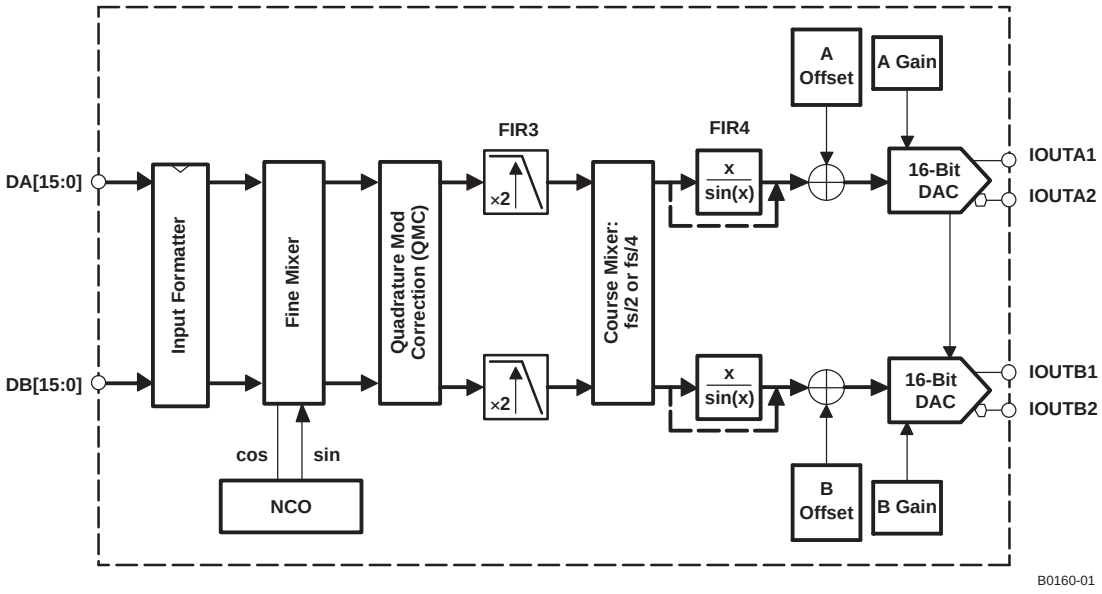
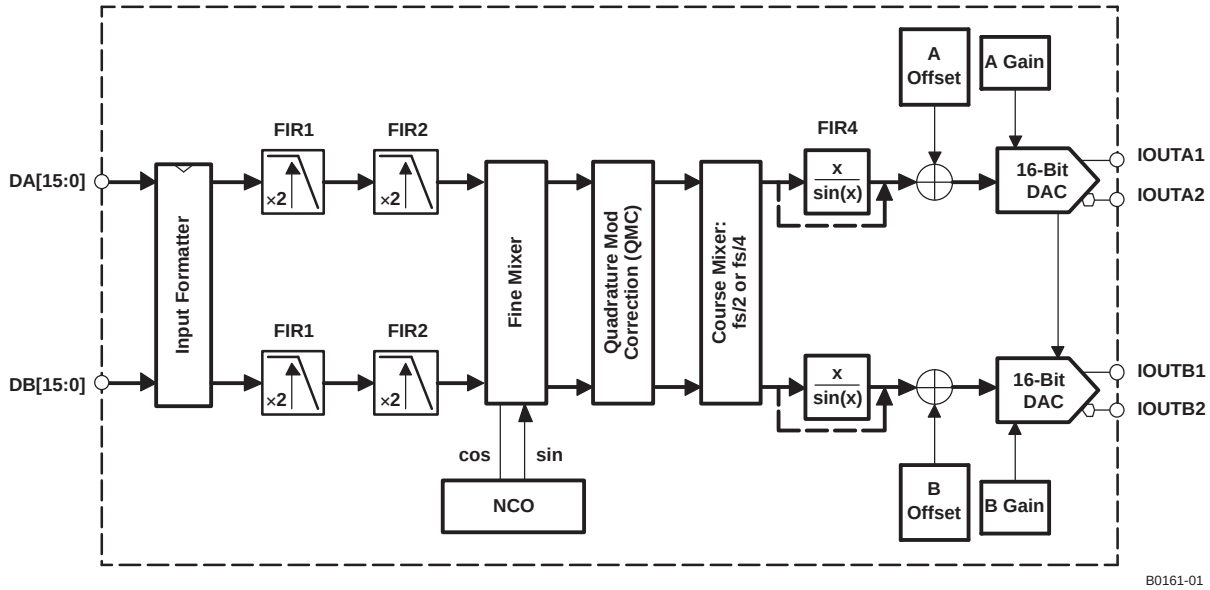


Figure 29. Block Diagram for X2 Mode



A. FMIX or QMC block cannot be enabled with CMIX block.

Figure 30. Block Diagram for X4 Mode (A)

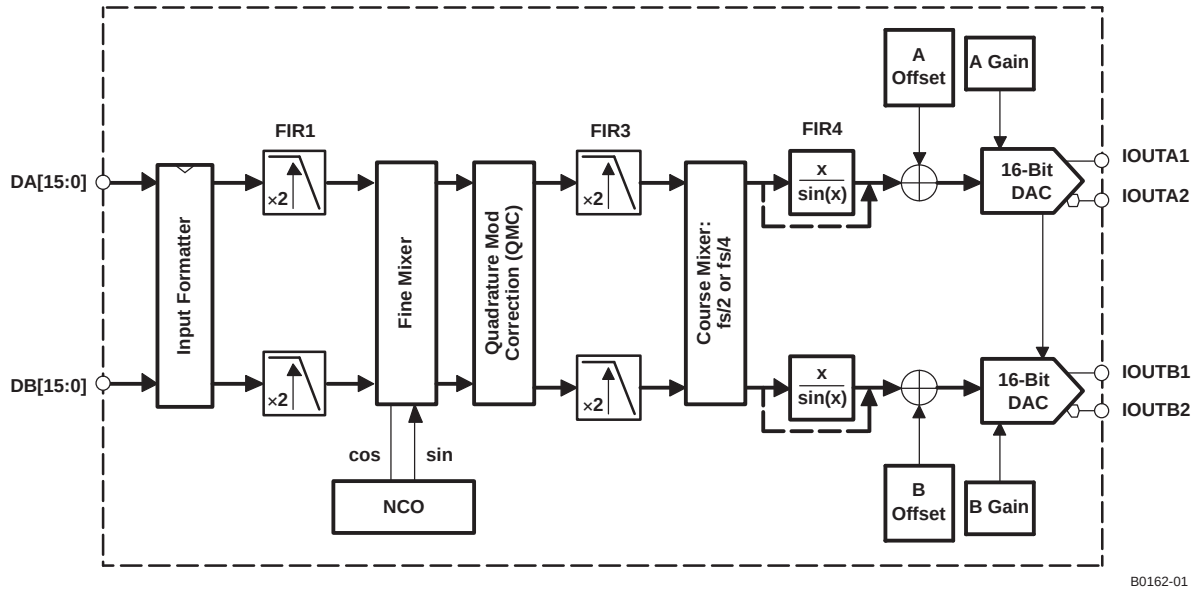


Figure 31. Block Diagram for X4L Mode

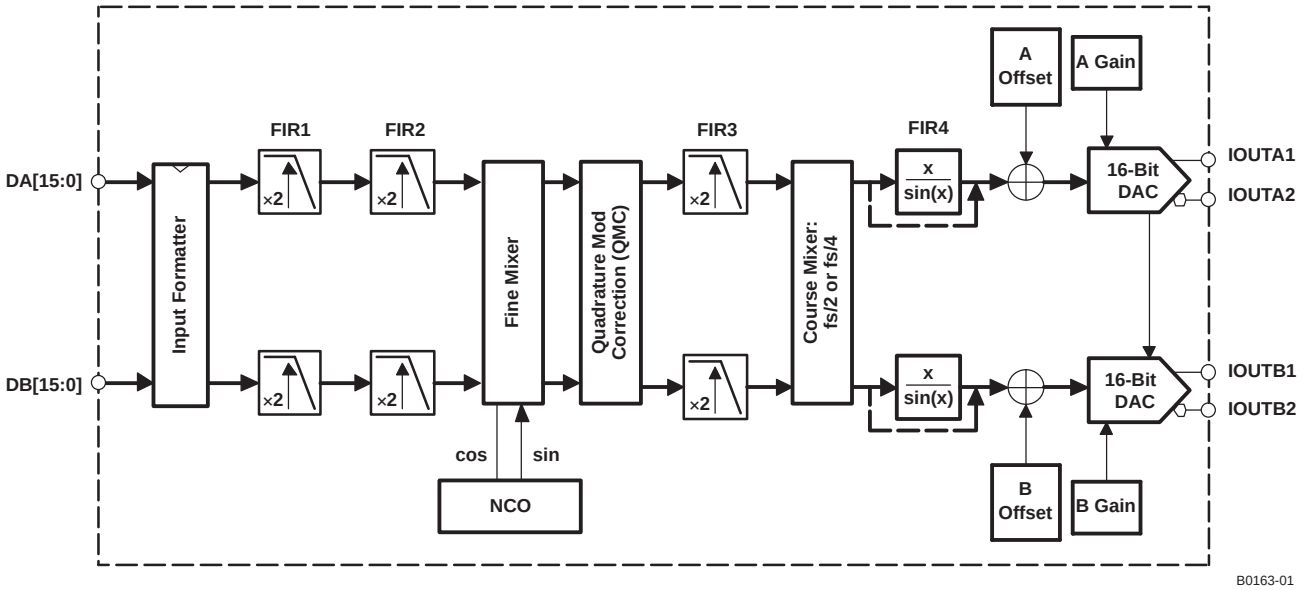


Figure 32. Block Diagram for X8 Mode

Programming Registers

REGISTER MAP

Name	Address	Default	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
VERSION	0x00	0x03	sleep_daca	sleep_dacb	hpla	hplb	unused	version(2:0)		
CONFIG0	0x01	0x00	pll_div(1:0)		pll_freq	pll_kv	interp(1:0)		inv_plllock	fifo_bypass
CONFIG1	0x02	0x00	qflag	interl	dual_clk	twos	rev_abus	rev_bbus	fir_bypass	full_bypass
CONFIG2	0x03	0x80	nco	nco_gain	qmc	cm_mode(3:0)				invsinc
CONFIG3	0x04	0x00	sif_4pin	dac_ser_data	half_rate	unused	usb	counter_mode(2:0)		
SYNC_CNTL	0x05	0x00	sync_phstr	sync_nco	sync_cm	sync_fifo(2:0)			unused	unused
SER_DATA_0	0x06	0x00	dac_data(7:0)							
SER_DATA_1	0x07	0x00	dac_data(15:8)							
Factory use only	0x08	0x00								
NCO_FREQ_0	0x09	0x00	freq(7:0)							
NCO_FREQ_1	0x0A	0x00	freq(15:8)							
NCO_FREQ_2	0x0B	0x00	freq(23:16)							
NCO_FREQ_3	0x0C	0x40	freq(31:24)							
NCO_PHASE_0	0x0D	0x00	phase(7:0)							
NCO_PHASE_1	0x0E	0x00	phase(15:8)							
DACA_OFFSET_0	0x0F	0x00	daca_offset(7:0)							
DACB_OFFSET_0	0x10	0x00	dacb_offset(7:0)							
DACA_OFFSET_1	0x11	0x00	daca_offset(12:8)					unused	unused	unused
DACB_OFFSET_1	0x12	0x00	dacb_offset(12:8)					unused	unused	unused
QMCA_GAIN_0	0x13	0x00	qmc_gain_a(7:0)							
QMCB_GAIN_0	0x14	0x00	qmc_gain_b(7:0)							
QMC_PHASE_0	0x15	0x00	qmc_phase(7:0)							
QMC_PHASE_GAIN_1	0x16	0x00	qmc_phase(9:8)		qmc_gain_a(10:8)			qmc_gain_b(10:8)		
DACA_GAIN_0	0x17	0x00	daca_gain(7:0)							
DACB_GAIN_0	0x18	0x00	dacb_gain(7:0)							
DACA_DACB_GAIN_1	0x19	0xFF	daca_gain(11:8)				dacb_gain(11:8)			
Factory use only	0x1A	0x00								
ATEST	0x1B	0x00	atest(4:0)					phstr_del(1:0)		unused
DAC_TEST	0x1C	0x00	factory use only							phstr_clkdiv_sel
Factory use only	0x1D	0x00								
Factory use only	0x1E	0x00								
Factory use only	0x1F	0x00								

Register Name: VERSION—Address: 0x00, Default = 0x03

BIT 7 BIT 0

sleep_daca	sleep_dacb	hpla	hplb	unused	version(2:0)		
0	0	0	0	0	0	1	1

sleep_daca: DAC A sleeps when set, operational when cleared.

sleep_dacb: DAC B sleeps when set, operational when cleared.

hpla: A-side first FIR filter in high-pass mode when set, low-pass mode when cleared.

hplb: B-side first FIR filter in high-pass mode when set, low-pass mode when cleared.

version(2:0): A hardwired register that contains the version of the chip. Read-only.

Register Name: CONFIG0—Address: 0x01, Default = 0x00

BIT 7 BIT 0

pll_div(1:0)		pll_freq	pll_kv	interp(1:0)		inv_plllock	fifo_bypass
0	0	0	0	0	0	0	0

pll_div(1:0): PLL VCO divider; {00 = 1, 01 = 2, 10 = 4, 11 = 8}.

pll_freq: PLL VCO center frequency; {0 = low center frequency, 1 = high center frequency}.

pll_kv: PLL VCO gain; {0 = high gain, 1 = low gain}.

interp(1:0): FIR interpolation; {00 = X2, 01 = X4, 10 = X4L, 11 = X8}. X4 uses lower power than X4L, but f_{DAC} = 320 MHz maximum when NCO or QMC is used.

inv_plllock: Multifunction bit, depending on clock mode

fifo_bypass: When set, the internal four-sample FIFO is disabled. When cleared, the FIFO is enabled.

Table 2. inv_plllock Bit Modes

PLLVDD	dual_clk	inv_plllock	fifo_bypass	DESCRIPTION
0 V	0	0	1	Input data latched on PLLLOCK pin rising edges, FIFO disabled
0 V	0	1	1	Input data latched on PLLLOCK pin falling edges, FIFO disabled
0 V	0	0	0	Input data latched on PLLLOCK pin rising edges, FIFO enabled and must be synchronized
0 V	0	1	0	Input data latched on PLLLOCK pin falling edges, FIFO enabled and must be synchronized
0 V	1	0	1	Input data latched on CLK1/CLK1C differential input. Timing between CLK1 and CLK2 rising edges must be tightly controlled (500 ps maximum at 500-MHz CLK2). PLLLOCK output signal is always low. The FIFO is always disabled in this mode.
0 V	1	1	0	Input data latched on CLK1/CLK1C differential input. No phase relationship required between CLK1 and CLK2. The FIFO is employed to manage the internal handoff between the CLK1 input clock and the CLK2 derived output clock; the FIFO must be synchronized. The PLLLOCK output signal reflects the internally generated FIFO output clock.
0 V	1	0	0	Not a valid setting. Do not use.
0 V	1	1	1	Not a valid setting. Do not use.
3.3 V	X	X	1	Internal PLL enabled, CLK1/CLK1C input differential clock is used to latch the input data. The FIFO is always disabled in this mode.
3.3 V	X	X	0	Not a valid setting. Do not use.

Register Name: CONFIG1—Address: 0x02, Default = 0x00

BIT 7 BIT 0

qflag	interl	dual_clk	twos	rev_abus	rev_bbus	fir_bypass	full_bypass
0	0	0	0	0	0	0	0

qflag: When set, the QFLAG input pin operates as a B sample indicator when interleaved data is enabled. When cleared, the TXENABLE rising determines the A/B timing relationship.

interl: When set, interleaved input data mode is enabled; both A and B data streams are input at the DA[15:0] input pins.

dual_clk: Only used when the PLL is disabled. When set, two differential clocks are used to input the data to the chip; CLK1/CLK1C is used to latch the input data into the chip and CLK2/CLK2C is used as the DAC sample clock.

twos: When set, input data is interpreted as 2s complement. When cleared, input data is interpreted as offset binary.

rev_abus: When cleared, DA input data MSB to LSB order is DA[15] = MSB and DA[0] = LSB. When set, DA

input data MSB to LSB order is reversed, DA[15] = LSB and DA[0] = MSB.

rev_bbus: When cleared, DB input data MSB to LSB order is DB[15] = MSB and DB[0] = LSB. When set, DB input data MSB to LSB order is reversed, DB[15] = LSB and DB[0]= MSB.

fir_bypass: When set, all interpolation filters are bypassed (interp(1:0) setting has no effect). QMC and NCO blocks are functional in this mode up to f_{DAC} = 250 MHz, limited by the input data rate.

full_bypass: When set, all filtering, QMC and NCO functions are bypassed.

Register Name: CONFIG2—Address: 0x03, Default = 0x80

BIT 7 BIT 0

nco	nco_gain	qmc	cm_mode(3:0)				invsinc
1	0	0	0	0	0	0	0

nco: When set, the NCO is enabled.

nco_gain: When set, the data output of the NCO is increased by 2×.

qmc: Quadrature modulator gain and phase correction is enabled when set.

cm_mode(3:0): Controls $f_{DAC}/2$ or $f_{DAC}/4$ mixer modes for the coarse mixer block.

Table 3. Coarse Mixer Sequences

cm_mode(3:0)	Mixing Mode	Sequence
00XX	No mixing	
0100	$f_{DAC}/2$	DAC A = {–A +A –A +A …} DAC B = {–B +B –B +B …}
0101	$f_{DAC}/2$	DAC A = {–A +A –A +A …} DAC B = {+B –B +B –B …}
0110	$f_{DAC}/2$	DAC A = {+A –A +A –A …} DAC B = {–B +B –B +B …}
0111	$f_{DAC}/2$	DAC A = {+A –A +A –A …} DAC B = {+B –B +B –B …}
1000	$f_{DAC}/4$	DAC A = {+A –B –A +B …} DAC B = {+B +A –B –A …}
1001	$f_{DAC}/4$	DAC A = {+A –B –A +B …} DAC B = {–B –A +B +A …}
1010	$f_{DAC}/4$	DAC A = {–A +B +A –B …} DAC B = {+B +A –B –A …}
1011	$f_{DAC}/4$	DAC A = {–A +B +A –B …} DAC B = {–B –A +B +A …}
1100	$-f_{DAC}/4$	DAC A = {+A +B –A –B …} DAC B = {+B –A –B +A …}
1101	$-f_{DAC}/4$	DAC A = {+A +B –A –B …} DAC B = {–B +A +B –A …}
1110	$-f_{DAC}/4$	DAC A = {–A –B +A +B …} DAC B = {+B –A –B +A …}
1111	$-f_{DAC}/4$	DAC A = {–A –B +A +B …} DAC B = {–B +A +B –A …}

invsinc: Enables the invsinc compensation filter when set.

Register Name: CONFIG3—Address: 0x04, Default = 0x00

BIT 7 BIT 0

sif_4pin	dac_ser_data	half_rate	unused	usb	counter_mode(2:0)		
0	0	0	0	0	0	0	0

sif_4pin: Four-pin serial interface mode is enabled when set, three-pin mode when cleared.

dac_ser_data: When set, both DAC A and DAC B input data is replaced with fixed data loaded into the 16-bit serial interface ser_data register.

half_rate: Enables half-rate input mode. Input data for the DAC A data path is input to the chip at half speed using both the DA[15:0] and DB[15:0] input pins.

usb: When set, the data to DACB is inverted to generate upper-sideband output.

counter_mode(2:0): Controls the internal counter that can be used as the DAC data source. Replaces digital values at DACs with a cyclic counter.
{0XX = off; 100 = all 16b; 101 = 7b LSBs; 110 = 5b MIDs; 111 = 5b MSBs}

Register Name: SYNC_CNTL—Address: 0x05, Default = 0x00

BIT 7 BIT 0

sync_phstr	sync_nco	sync_cm	sync_fifo(2:0)			unused	unused
0	0	0	0	0	0	0	0

sync_phstr: When set, the internal clock divider logic is initialized with a PHSTR pin low-to-high transition.

sync_nco: When set, the NCO phase accumulator is cleared with a PHSTR low-to-high transition.

sync_cm: When set, the coarse mixer is initialized with a PHSTR low-to-high transition.

sync_fifo(2:0): Sync source selection mode for the FIFO. When a low-to-high transition is detected on the selected sync source, the FIFO input and output pointers are initialized.

Table 4. Synchronization Source

sync_fifo(2:0)	Synchronization Source
000	TXENABLE pin
001	PHSTR pin
010	QFLAG pin
011	DB[15]
100	DA[15] first transition (one shot)
101	Software sync using SIF write
110	Sync source disabled (always off)
111	Always on

Register Name: SER_DATA_0—Address: 0x06, Default = 0x00

BIT 7 BIT 0

dac_data(7:0)							
0	0	0	0	0	0	0	0

dac_data(7:0): Lower 8 bits of DAC data input to the DACs when dac_ser_data is set.

Register Name: SER_DATA_1—Address: 0x07, Default = 0x00

BIT 7 BIT 0

dac_data(15:8)							
0	0	0	0	0	0	0	0

dac_data(15:8): Upper 8 bits of DAC data input to the DACs when dac_ser_data is set.

Register Name: BYPASS_MASK_CNTL—Address: 0x08, Default = 0x00

BIT 7 BIT 0

fast_latch	bp_ invsinc	bp_fir3	bp_qmc	bp_fmix	bp_fir2	bp_fir1	nco_only
0	0	0	0	0	0	0	0

These modes are for factory use only – leave as default.

Register Name: NCO_FREQ_0—Address: 0x09, Default = 0x00

BIT 7 BIT 0

freq(7:0)							
0	0	0	0	0	0	0	0

freq(7:0): Bits 7:0 of the NCO frequency word.

Register Name: NCO_FREQ_1—Address: 0x0A, Default = 0x00

BIT 7 BIT 0

freq(15:8)							
0	0	0	0	0	0	0	0

freq(15:8): Bits 15:8 of the NCO frequency word.

Register Name: NCO_FREQ_2—Address: 0x0B, Default = 0x00

BIT 7 BIT 0

freq(23:16)							
0	0	0	0	0	0	0	0

freq(23:16): Bits 23:16 of the NCO frequency word.

Register Name: NCO_FREQ_3—Address: 0x0C, Default = 0x40

BIT 7 BIT 0

freq(31:24)							
0	1	0	0	0	0	0	0

freq(31:24): Bits 31:24 of the NCO frequency word.

Register Name: NCO_PHASE_0—Address: 0x0D, Default = 0x00

BIT 7 BIT 0

phase(7:0)							
0	0	0	0	0	0	0	0

phase(7:0): Bits 7:0 of the NCO phase offset word.

Register Name: NCO_PHASE_1—Address: 0x0E, Default = 0x00

BIT 7 BIT 0

phase(15:8)							
0	0	0	0	0	0	0	0

phase(15:8): Bits 15:8 of the NCO phase offset word.

Register Name: DACA_OFFSET_0—Address: 0x0F, Default = 0x00

BIT 7 BIT 0

daca_offset(7:0)							
0	0	0	0	0	0	0	0

daca_offset(7:0): Bits 7:0 of the DAC A offset word.

Register Name: DACB_OFFSET_0—Address: 0x10, Default = 0x00

BIT 7 BIT 0

dacb_offset(7:0)							
0	0	0	0	0	0	0	0

dacb_offset(7:0): Bits 7:0 of the DAC B offset word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

Register Name: DACA_OFFSET_1—Address: 0x11, Default = 0x00

BIT 7 BIT 0

daca_offset(12:8)					unused	unused	unused
0	0	0	0	0	0	0	0

daca_offset(12:8): Bits 12:8 of the DAC A offset word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

Register Name: DACB_OFFSET_1—Address: 0x12, Default = 0x00

BIT 7 BIT 0

dacb_offset(12:8)					unused	unused	unused
0	0	0	0	0	0	0	0

dacb_offset(12:8): Bits 12:8 of the DAC B offset word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

Register Name: QMCA_GAIN_0—Address: 0x13, Default = 0x00

BIT 7 BIT 0

qmc_gain_a(7:0)							
0	0	0	0	0	0	0	0

qmc_gain_a(7:0): Bits 7:0 of the QMC A path gain word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

Register Name: QMCB_GAIN_0—Address: 0x14, Default = 0x00

BIT 7 BIT 0

qmc_gain_b(7:0)							
0	0	0	0	0	0	0	0

qmc_gain_b(7:0): Bits 7:0 of the QMC B path gain word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

Register Name: QMC_PHASE_0—Address: 0x15, Default = 0x00

BIT 7 BIT 0

qmc_phase(7:0)							
0	0	0	0	0	0	0	0

qmc_phase(7:0): Bits 7:0 of the QMC phase word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

Register Name: QMC_PHASE_GAIN_1—Address: 0x16, Default = 0x00

BIT 7 BIT 0

qmc_phase(9:8)		qmc_gain_a(10:8)			qmc_gain_b(10:8)		
0	0	0	0	0	0	0	0

qmc_phase(9:8): Bits 9:8 of the QMC phase word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

qmc_gain_a(10:8): Bits 10:8 of the QMC A path gain word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

qmc_gain_b(10:8): Bits 10:8 of the QMC B path gain word. Updates to this register do not take effect until DACA_OFFSET_0 has been written.

Register Name: DACA_GAIN_0—Address: 0x17, Default = 0x00

BIT 7 BIT 0

daca_gain(7:0)							
0	0	0	0	0	0	0	0

daca_gain(7:0): Bits 7:0 of the DAC A gain adjustment word.

Register Name: DACB_GAIN_0—Address: 0x18, Default = 0x00

BIT 7 BIT 0

dacb_gain(7:0)							
0	0	0	0	0	0	0	0

dacb_gain(7:0): Bits 7:0 of the DAC B gain adjustment word.

Register Name: DACA_DACB_GAIN_1—Address: 0x19, Default = 0xFF

BIT 7 BIT 0

daca_gain(11:8)				dacb_gain(11:8)			
1	1	1	1	1	1	1	1

daca_gain(11:8): Bits 11:8 of the DAC A gain word. Four MSBs of gain control for DAC A.

dacb_gain(11:8): Bits 11:8 of the DAC B gain word. Four MSBs of gain control for DAC B.

Register Name: DAC_CLK_CNTL—Address: 0x1A, Default = 0x00

BIT 7 BIT 0

Factory use only							
0	0	0	0	0	0	0	0

Reserved for factory use only.

Register Name: ATEST—Address: 0x1B, Default = 0x00

BIT 7 BIT 0

atest(4:0)					phstr_del(1:0)		unused
0	0	0	0	0	0	0	0

atest(4:0): Can be used to enable clock output at the PLLLOCK pin according to Table 5. Pin EXTLO must be open when atest(4:0) is not equal to 00000.

Table 5. PLLLOCK Output

atest(4:0)	PLLLOCK Output Signal	
	PLL Enabled (PLLVDD = 3.3 V)	PLL Disabled (PLLVDD = 0 V)
11101	f_{DAC}	Normal operation
11110	f_{DAC} divided by 2	Normal operation
11111	f_{DAC} divided by 4	Normal operation
All others	Normal operation	

phstr_del: Adjusts the initial phase of the $f_S/2$ and $f_S/4$ blocks cmix block after PHSTR.

Register Name: DAC_TEST—Address: 0x1C, Default = 0x00

BIT 7 BIT 0

Factory use only							phstr_clkdiv_sel
0	0	0	0	0	0	0	0

phstr_clkdiv_sel: Selects the clock used to latch the PHSTR input when restarting the internal dividers. When set, the full DAC sample rate CLK2 signal latches PHSTR, and when cleared, the divided down input clock signal latches PHSTR.

Address: 0x1D, 0x1E, and 0x1F – Reserved

Writes have no effect and reads are 0x00.

Serial Interface

The serial port of the DAC5687 is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of the DAC5687. It is compatible with most synchronous transfer formats and can be configured as a three- or four-pin interface by **sif_4pin** in register **CONFIG3**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For three-pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For four-pin configuration, **SDIO** is data in only and **SDO** is data out only.

Each read/write operation is framed by signal **SDENB** (serial data enable bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle, which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data. Table 6 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 to 5 comprise the data transfer cycle.

Table 6. Instruction Byte of the Serial Interface

MSB LSB

Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from the DAC5687, and a low indicates a write operation to the DAC5687.

[N1:N0] Identifies the number of data bytes to be transferred, per Table 7. Data is transferred MSB first. With multibyte transfers, [A4:A0] is the address of the first data byte, and the address is decremented for each subsequent byte.

Table 7. Number of Transferred Bytes Within One Communication Frame

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

[A4:A0] Identifies the address of the register to be accessed during the read or write operation. For multibyte transfers, this address is the starting address. Note that the address is written to the DAC5687 MSB first.

Figure 33 shows the serial interface timing diagram for a DAC5687 write operation. **SCLK** is the serial interface clock input to the DAC5687. Serial data enable **SDENB** is an active-low input to the DAC5687. **SDIO** is serial data in. Input data to the DAC5687 is clocked on the rising edges of **SCLK**.

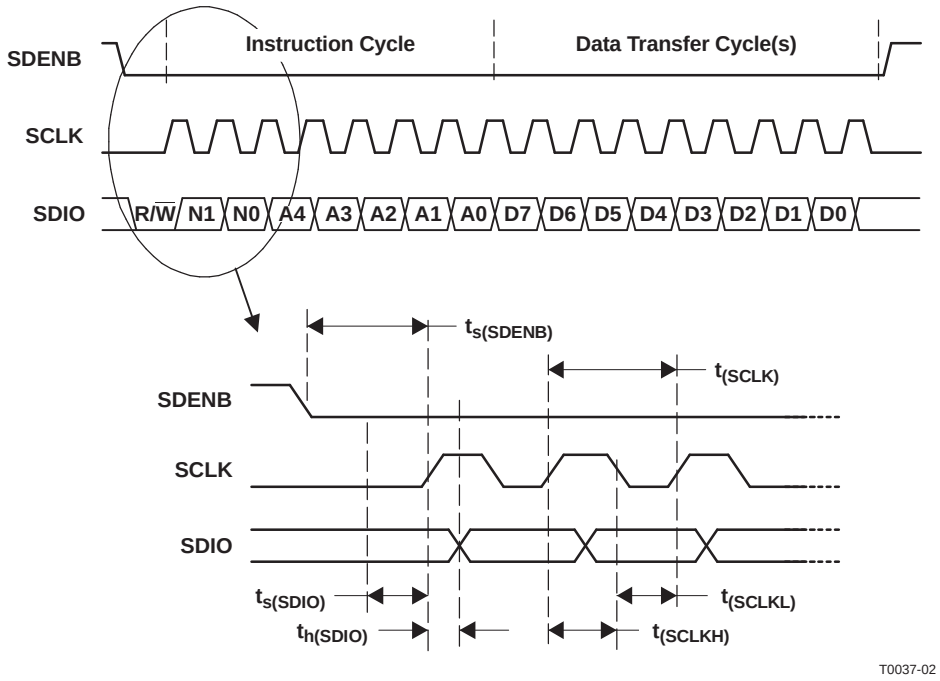


Figure 33. Serial-Interface Write Timing Diagram

Figure 34 shows the serial interface timing diagram for a DAC5687 read operation. **SCLK** is the serial interface clock input to the DAC5687. Serial data enable **SDENB** is an active-low input to the DAC5687. **SDIO** is serial data in during the instruction cycle. In three-pin configuration, **SDIO** is data out from the DAC5687 during the data transfer cycle(s), while **SDO** is in a high-impedance state. In four-pin configuration, **SDO** is data out from the DAC5687 during the data transfer cycle(s). At the end of the data transfer, **SDO** outputs low on the final falling edge of SCLK until the rising edge of SDENB, when it goes into the high-impedance state.

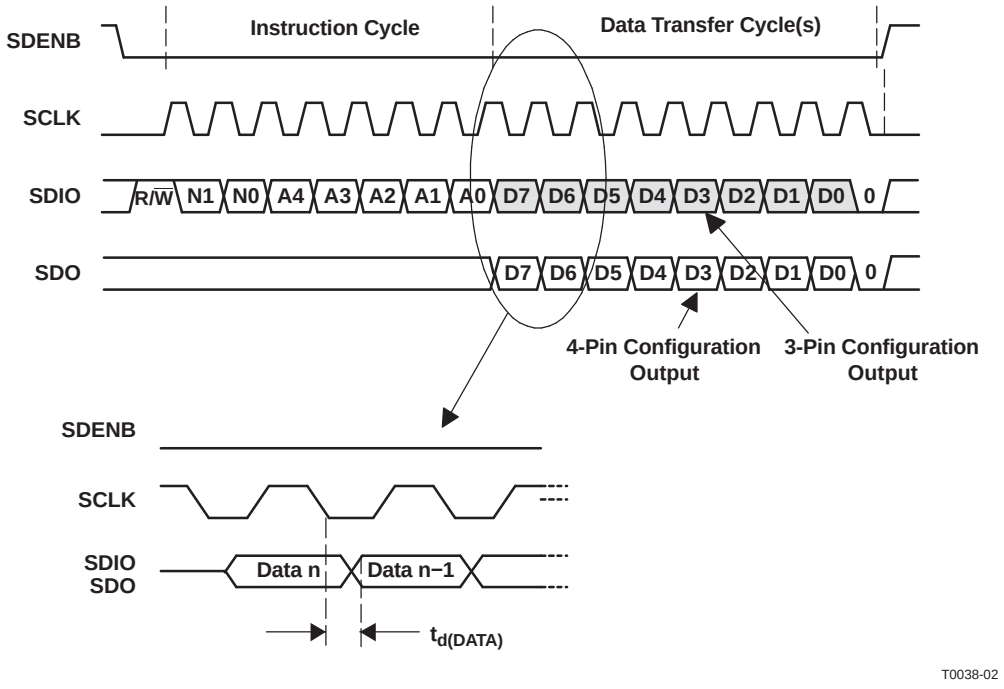


Figure 34. Serial-Interface Read Timing Diagram

FIR Filters

Figure 35 shows the magnitude spectrum response for the identical 51-tap FIR1 and FIR3 filters. The transition band is from 0.4 to 0.6 × f_{IN} (the input data rate for the FIR filter) with < 0.002-dB pass-band ripple and > 80-dB stop-band attenuation. Figure 36 shows the region from 0.35 to 0.45 × f_{IN}. Up to 0.44 × f_{IN}, there is less than 0.5 dB of attenuation.

Figure 37 shows the magnitude spectrum response for the 19-tap FIR2 filter. The transition band is from 0.25 to 0.75 × f_{IN} (the input data rate for the FIR filter) with < 0.002-dB pass-band ripple and > 80-dB stop-band attenuation.

The DAC5687 also has an inverse sinc filter (FIR4) that runs at the DAC update rate (f_{DAC}) that can be used to flatten the frequency response of the sample-and-hold output. The DAC sample-and-hold output sets the output current and holds it constant for one DAC clock cycle until the next sample, resulting in the well-known sin(x)/x or sinc(x) frequency response shown in Figure 38 (red dash-dotted line). The inverse sinc filter response (Figure 38, blue solid line) has the opposite frequency response between 0 to 0.4 × f_{DAC}, resulting in the combined response (Figure 38, green dotted line). Between 0 to 0.4 × f_{DAC}, the inverse sinc filter compensates the sample-and-hold rolloff with less than 0.03-dB error.

The inverse sinc filter has a gain > 1 at all frequencies. Therefore, the signal input to FIR4 must be reduced from full scale to prevent saturation in the filter. The amount of backoff required depends on the signal frequency, and is set such that at the signal frequencies, the combination of the input signal and filter response is less than 1 (0 dB). For example, if the signal input to FIR4 is at 0.25 × f_{DAC}, the response of FIR4 is 0.9 dB, and the signal must be backed off from full scale by 0.9 dB. The gain function in the QMC block can be used to set reduce amplitude of the input signal. The advantage of FIR4 having a positive gain at all frequencies is that the user is then able to optimize backoff of the signal based on the signal frequency.

The filter taps for all digital filters are listed in Table 8.

Note that the loss of signal amplitude may result in lower SNR due to decrease in signal amplitude.

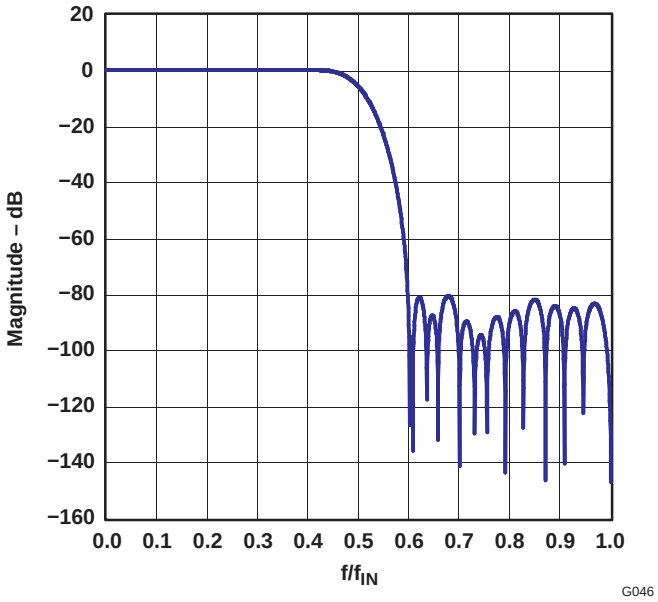


Figure 35. Magnitude Spectrum for FIR1 and FIR3

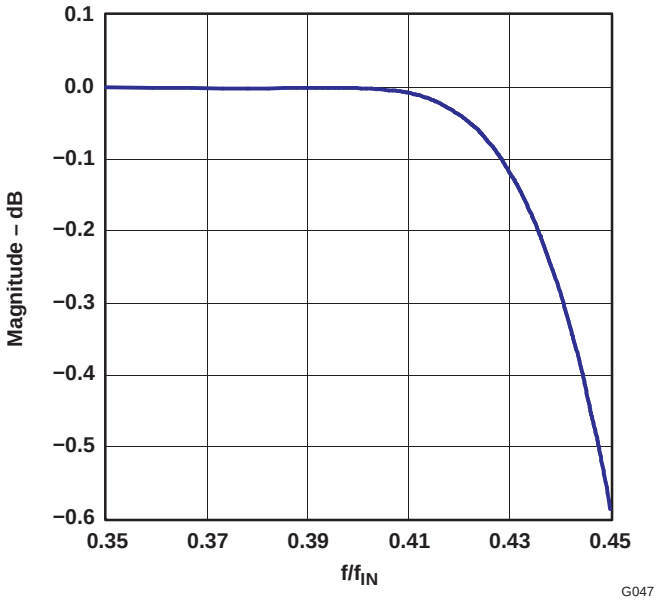


Figure 36. FIR1 and FIR3 Transition Band

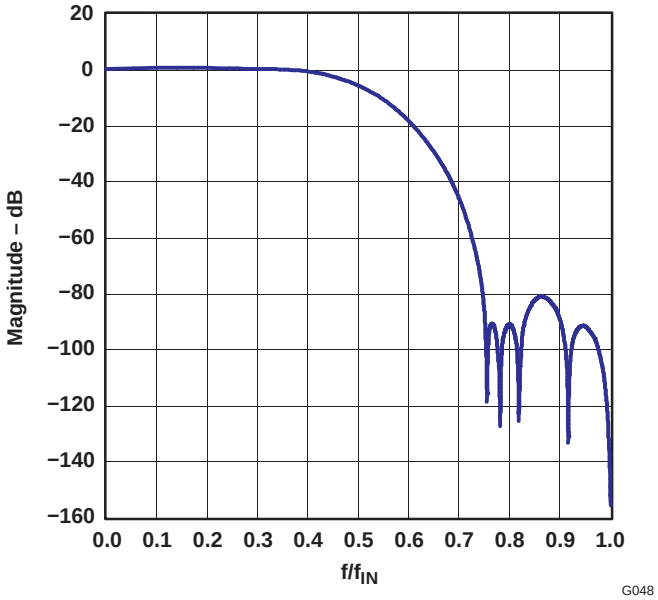


Figure 37. Magnitude Spectrum for FIR2

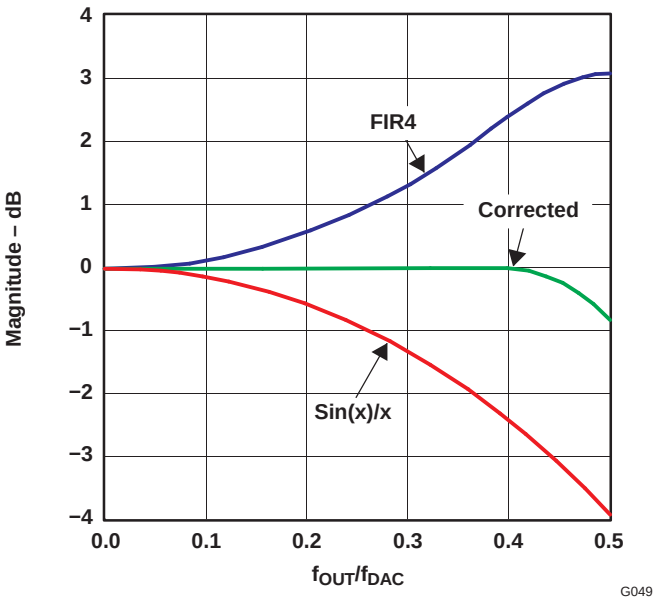


Figure 38. Magnitude Spectrum for Inverse Sinc Filter FIR4 (Versions 1 and 2)

Table 8. Digital Filter Taps

FIR1 and FIR3		FIR2		FIR4 (Invsinc)	
Tap	Coeff	Tap	Coeff	Tap	Coeff
1, 51	8	1, 19	9	1, 9	1
2, 50	0	2, 18	0	2, 8	–4
3, 49	–24	3, 17	–58	3, 7	13
4, 48	0	4, 16	0	4, 6	–50
5, 47	58	5, 15	214	5	592
6, 46	0	6, 14	0		
7, 45	–120	7, 13	–638		
8, 44	0	8, 12	0		
9, 43	221	9, 11	2521		
10, 42	0	10	4096		
11, 41	–380				
12, 40	0				
13, 39	619				
14, 38	0				
15, 37	–971				
16, 36	0				
17, 35	1490				
18, 34	0				
19, 33	–2288				
20, 32	0				
21, 31	3649				
22, 30	0				
23, 29	–6628				
24, 28	0				
25, 27	20,750				
26	32,768				

Dual-Channel Real Upconversion

The DAC5687 can be used in a dual-channel mode with real upconversion by mixing with a 1, –1, … sequence in the signal chain to invert the spectrum. This mixing mode maintains isolation of the A and B channels. There are two points of mixing: in X4L mode, the FIR1 output is inverted (high-pass mode) by setting registers **hpla** and **hplb** to 1, and the FIR3 output is inverted by setting CMIX to $f_{DAC}/2$. In X8 mode, the output of FIR1 is inverted by setting **hpla** and **hplb** to 1, and the FIR3 output is inverted by setting CMIX to $f_{DAC}/2$. In X2 and X4 modes, the output of FIR3 is inverted by setting CMIX to $f_{DAC}/2$.

The wide bandwidth of FIR3 (40% passband) in X4L mode provides options for setting four different frequency ranges, listed in Table 9. For example, with f_{DATA} = 125 MSPS (f_{DAC} = 500 MSPS), setting FIR1/FIR3 to High Pass/High Pass, respectively, upconverts a signal between 25 MHz and 50 MHz to a signal between 150 MHz and 175 MHz. With the High Pass/Low Pass and Low Pass/High Pass settings, the upconvertered signal is spectrally inverted.

Table 9. X4L Mode High-Pass/Low-Pass Options

FIR1	FIR3	Input Frequency	Output Frequency	Bandwidth	Inverted?
Low pass	Low pass	0–0.4 × f_{DATA}	0–0.4 × f_{DATA}	0.4 × f_{DATA}	No
High pass	Low pass	0.2 to 0.4 × f_{DATA}	0.6–0.8 × f_{DATA}	0.2 × f_{DATA}	Yes
High pass	High pass	0.2 to 0.4 × f_{DATA}	1.2–1.4 × f_{DATA}	0.2 × f_{DATA}	No
Low pass	High pass	0–0.4 × f_{DATA}	1.6–2 × f_{DATA}	0.4 × f_{DATA}	Yes

Limitations on Signal BW and Final Output Frequency in X4L and X8 Modes

For very wide-bandwidth signals, the FIR3 pass band (0–0.4 × $f_{DAC}/2$) can limit the range of the final output frequency. For example, in X4L FMIX CMIX mode (4× interpolation with FMIX after FIR1), at the maximum input data rate of f_{IN} = 125 MSPS, the input signal can be ±50 MHz before running into the transition band of FIR1. After 2× interpolation, FIR3 limits the signal to ±100 MHz (0.4 × 250 MHz). Therefore, at the maximum signal bandwidth, FMIX can mix up to 50 MHz and still fall within the pass band of FIR3. This results in gaps in the final output frequency between FMIX alone (0 MHz to 50 MHz) and FMIX + CMIX with $f_{DAC}/4$ (75 MHz to 175 MHz) and FMIX + CMIX with $f_{DAC}/2$ (200 MHz to 250 MHz).

In practice, it may be possible to extend the signal into the FIR3 transition band. Referring to Figure 36 in the preceding *FIR Filters* section, if 0.5 dB of attenuation at the edge of the signal can be tolerated, then the signal can be extended up to 0.44 × f_{IN}. This would extend the range of FMIX in the example to 60 MHz.

Fine Mixer (FMIX)

The fine mixer block FMIX uses a numerically controlled oscillator (NCO) with a 32-bit frequency register **freq(31:0)** and a 16-bit phase register **phase(15:0)** to provide sin and cos for mixing. The NCO tuning frequency is programmed in registers 0x09 through 0x0C. Phase offset is programmed in registers 0x0D and 0x0E. A block diagram of the NCO is shown in Figure 39.

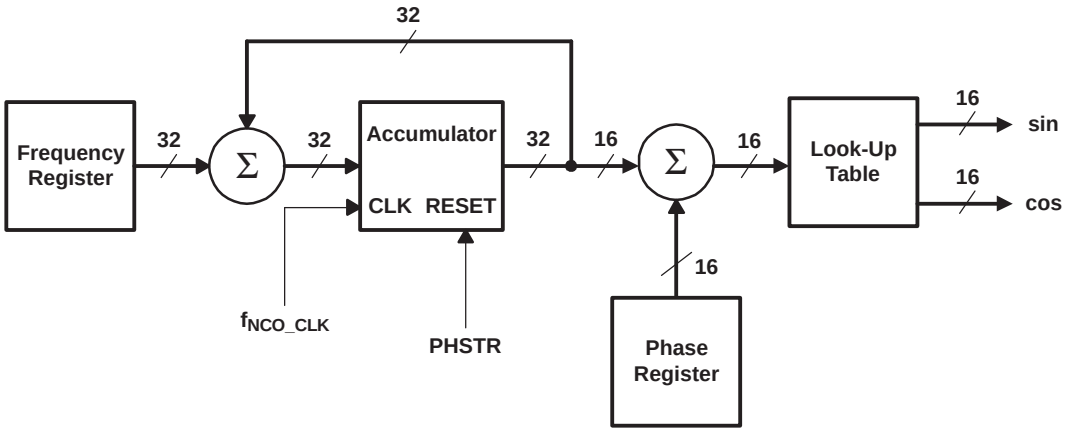


Figure 39. Block Diagram of the NCO

Synchronization of the NCO occurs by resetting the NCO accumulator to zero with assertion of **PHSTR**. See the following *NCO Synchronization* section. Frequency word **freq** in the frequency register is added to the accumulator every clock cycle. The output frequency of the NCO is

$$f_{NCO} = \frac{freq \times f_{NCO\_CLK}}{2^{32}} \text{ for } freq \leq 2^{31} \Big/ f_{NCO} = \frac{(freq - 2^{32}) \times f_{NCO\_CLK}}{2^{32}} \text{ for } freq > 2^{31}$$

where f_{NCO_CLK} is the clock frequency of the NCO circuit. In X4 mode, the NCO clock frequency is the same as the DAC sample rate, f_{DAC}. The maximum clock frequency the NCO can operate at is 320 MHz – in X4 FMIX mode, where FMIX operates at the DAC update rate, the DAC updated rate is limited to 320 MSPS. In X2, X4L and X8 modes, the NCO circuit is followed by a further 2× interpolation and so $f_{NCO\_CLK} = f_{DAC}/2$ and operates at f_{DAC} = 500 MHz.

Treating channels A and B as a complex vector I + I × Q where I(t) = A(t) and Q(t) = B(t), the output of FMIX $I_{OUT}(t)$ and $Q_{OUT}(t)$ is

$$I_{OUT}(t) = (I_{IN}(t)\cos(2\pi f_{NCO}t + \delta) - Q_{IN}(t)\sin(2\pi f_{NCO}t + \delta)) \times 2^{(NCO\_GAIN - 1)}$$

$$Q_{OUT}(t) = (I_{IN}(t)\sin(2\pi f_{NCO}t + \delta) + Q_{IN}(t)\cos(2\pi f_{NCO}t + \delta)) \times 2^{(NCO\_GAIN - 1)}$$

where t is the time since the last resetting of the NCO accumulator, δ is the initial accumulator value, and NCO_GAIN, bit 6 in register CONFIG2, is either 0 or 1. δ is given by

$$\delta = 2\pi \times \textbf{phase(15:0)}/2^{16}.$$

The maximum output amplitude of FMIX occurs if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously full-scale amplitude and the sine and cosine arguments $2\pi f_{NCO}t + \delta = (2N - 1) \times \pi/4$ (N = 1, 2, ...). With NCO_GAIN = 0, the gain through FMIX is sqrt(2)/2 or –3 dB. This loss in signal power is in most cases undesirable, and it is recommended that the gain function of the QMC block be used to increase the signal by 3 dB to 0 dBFS by setting qmca_gain and qmcb_gain each to 1446 (decimal).

With NCO_GAIN = 1, the gain through FMIX is sqrt(2) or 3 dB, which can cause clipping of the signal if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously near full-scale amplitude, and should therefore be used with caution.

Coarse Mixer (CMIX)

The coarse mixer block provides mixing capability at the DAC output rate with fixed frequencies of $f_S/2$ or $f_S/4$. The coarse mixer output phase sequence is selected by the cm_mode(3:0) bits in register CONFIG2 and is shown in Table 10.

Table 10. Coarse Mixer Sequences

cm_mode(3:0)	Mixing Mode	Sequence
00XX	No mixing	
0100	$f_{DAC}/2$	DAC A = {–A +A –A +A …} DAC B = {–B +B –B +B …}
0101	$f_{DAC}/2$	DAC A = {–A +A –A +A …} DAC B = {+B –B +B –B …}
0110	$f_{DAC}/2$	DAC A = {+A –A +A –A …} DAC B = {–B +B –B +B …}
0111	$f_{DAC}/2$	DAC A = {+A –A +A –A …} DAC B = {+B –B +B –B …}
1000	$f_{DAC}/4$	DAC A = {+A –B –A +B …} DAC B = {+B +A –B –A …}
1001	$f_{DAC}/4$	DAC A = {+A –B –A +B …} DAC B = {–B –A +B +A …}
1010	$f_{DAC}/4$	DAC A = {–A +B +A –B …} DAC B = {+B +A –B –A …}
1011	$f_{DAC}/4$	DAC A = {–A +B +A –B …} DAC B = {–B –A +B +A …}
1100	$-f_{DAC}/4$	DAC A = {+A +B –A –B …} DAC B = {+B –A –B +A …}
1101	$-f_{DAC}/4$	DAC A = {+A +B –A –B …} DAC B = {–B +A +B –A …}
1110	$-f_{DAC}/4$	DAC A = {–A –B +A +B …} DAC B = {+B –A –B +A …}
1111	$-f_{DAC}/4$	DAC A = {–A –B +A +B …} DAC B = {–B +A +B –A …}

The output of CMIX is complex. For a real output, either DACA or DACB can be used and the other DAC slept, the difference being the phase sequence.

Quadrature Modulator Correction (QMC)

The quadrature modulator correction (QMC) block provides a means for changing the phase balance of the complex signal to compensate for I and Q imbalance present in an analog quadrature modulator. The QMC block is limited in operation to a clock rate of 320 MSPS.

The block diagram for the QMC block is shown in Figure 40. The QMC block contains three programmable parameters. Registers **qmc_gain_a** and **qmc_gain_b** control the I and Q path gains and are 11-bit values with a range of 0 to approximately 2. Note that the I and Q gain can also be controlled by setting the DAC full-scale output current (see following). Register **qmc_phase** controls the phase imbalance between I and Q and is a 10-bit value with a range of –1/2 to approximately 1/2.

LO feedthrough can be minimized by adjusting the DAC offset feature described as follows.

An example of sideband optimization using the QMC block and gain adjustment is shown in Figure 41. The QMC phase adjustment in combination with the DAC gain adjustment can reduce the unwanted sideband signal from ~40 dBc to > 65 dBc.

Note that mixing in the CMIX block after the QMC correction destroys the I and Q phase compensation information from the QMC block.

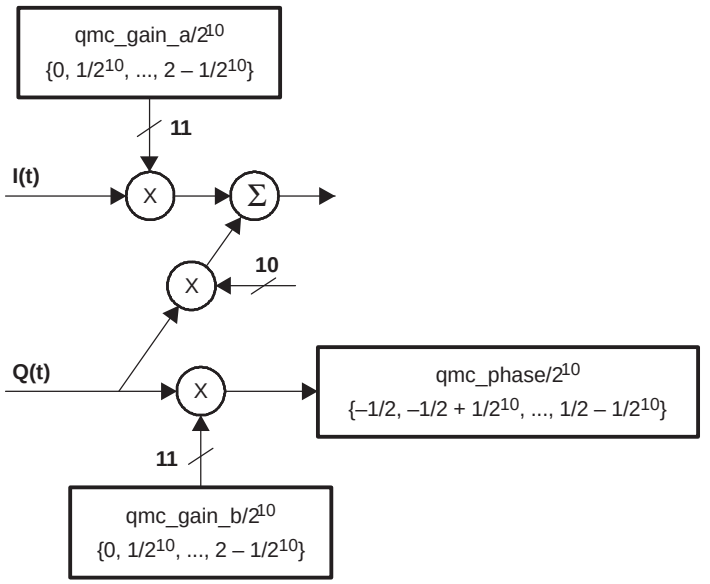


Figure 40. QMC Block Diagram

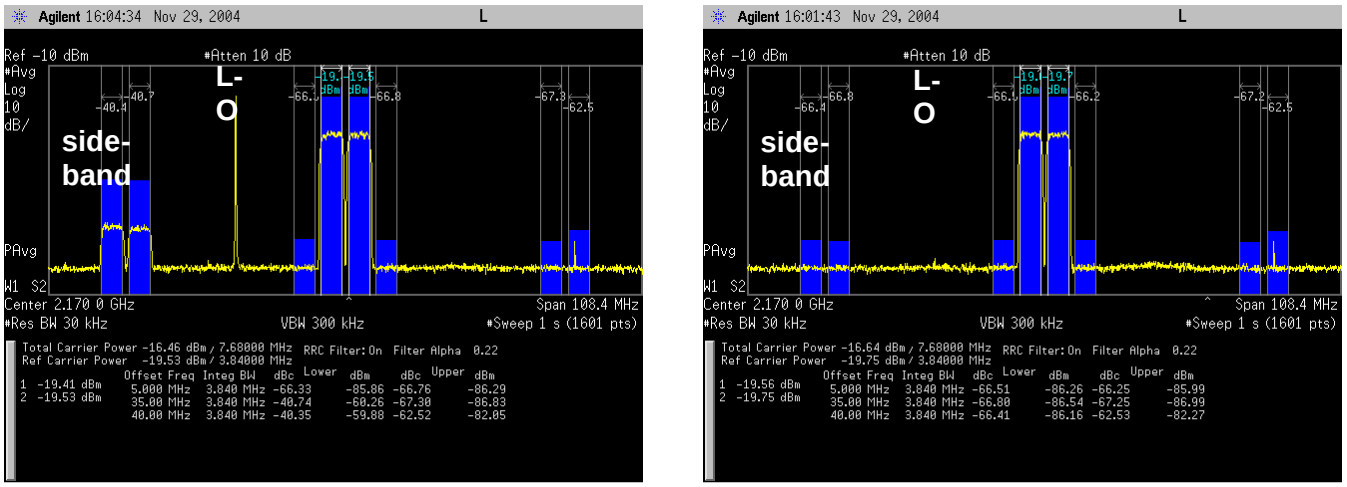


Figure 41. Example of Sideband Optimization Using QMC Phase and Gain Adjustments

DAC Offset Control

Registers **daca_offset** and **dacb_offset** control the I and Q path offsets and are 13-bit values with a range of –4096 to 4095. The DAC offset value adds a digital offset to the digital data before digital-to-analog conversion. The **qmc_gain_a** and **qmc_gain_b** registers can be used to back off the signal before the offset to prevent saturation when the offset value is added to the digital signal. The offset values are in 2s-complement format.

It takes four DAC clock cycles to update the 14-bit DAC5687 offset registers. During the first clock cycle, the two MSBs, daca_offset(13:12) and dacb_offset(13:12), are updated, followed by daca_offset(11:8) and dacb_offset(11:8) on the second clock cycle, daca_offset(7:4) and dacb_offset(7:4) on the third clock cycle, and daca_offset(3:0) and dacb_offset(3:0) on the fourth clock cycle.

During the four DAC clock cycles, the partially updated offset register values are summed to the DAC signal. This can result in offset values during the first three DAC clock cycles that are significantly different from the starting and ending offset values. For example, Table 11 shows the transition from offset value 1023 to 1025. The bit changes in each clock cycle are in bold. As can be seen, the transition between 1023 and 1025 results in offset values of 1023, 1279, and 1039 during the transition.

Table 11. Offset Values During Transition

DAC Clock Cycle	Signed Integer Value	Binary Format	Hexadecimal Format
0	1023 starting value	00 0011 1111 1111	0x03FF
1	1023	**00** 0011 1111 1111	0x03FF
2	1279	00 **0100** 1111 1111	0x04FF
3	1039	00 0100 **0000** 1111	0x040F
4	1025 ending value	00 0100 0000 **0001**	0x0401

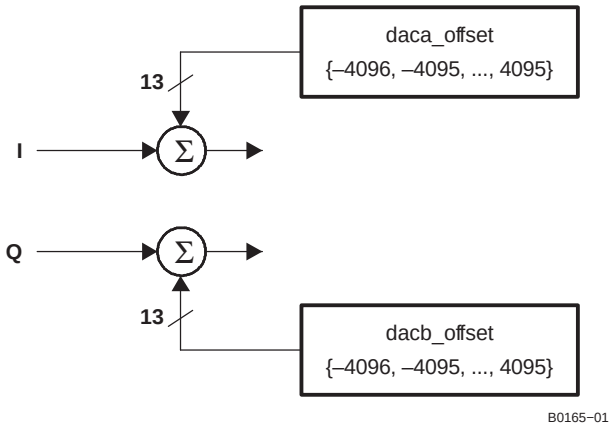


Figure 42. DAC Offset Block

Analog DAC Gain

The full-scale DAC output current can be set by programming the **daca_gain** and **dacb_gain** registers. The DAC gain value controls the full-scale output current.

$$I_{fullscale} = \left[\frac{16(V_{extio})}{R_{BIAS}} \times \frac{GAINCODE + 1}{16} \div \left(1 - \frac{FINEGAIN}{3072}\right) \right]$$

where GAINCODE = daca_gain(11:8) or dacb_gain(11:8) is the coarse gain setting (0 to 15) and FINEGAIN = daca_gain(7:0) or dacb_gain(7:0) (–128 to 127) is the fine gain setting.

Clock Modes

In the DAC5687, the internal clocks (1×, 2×, 4×, and 8× as needed) for the logic, FIR interpolation filters, and DAC are derived from a clock at either the input data rate using an internal PLL (PLL clock mode) or DAC output sample rate (external clock mode). Power for the internal PLL blocks (PLLVDD and PLLGND) are separate from the other clock generation blocks power (CLKVDD and CLKGND), thus minimizing phase noise within the PLL.

The DAC5687 has three clock modes for generating the internal clocks (1×, 2×, 4×, and 8× as needed) for the logic, FIR interpolation filters, and DACs. The clock mode is set using the PLLVDD pin and **dual_clk** in register **CONFIG1**.

1. PLLVDD = 0 V and **dual_clk** = 0: EXTERNAL CLOCK MODE

In EXTERNAL CLOCK MODE, the user provides a clock signal at the DAC output sample rate through CLK2/CLK2C. CLK1/CLK1C and the internal PLL are not used. The LPF and CLK1/CLK1C pins can be left unconnected. The input data-rate clock and interpolation rate are selected by the bits **interp(1:0)** in register **CONFIG0** and is output through the PLLLOCK pin. The PLLLOCK clock can be used to drive the input data source (such as digital upconverter) that sends the data to the DAC. Note that the PLLLOCK delay relative to the input CLK2 rising edge ($t_{d(PLLLOCK)}$ in Figure 43 and Figure 44) increases with increasing loads. The PLLLOCK output driver is not capable of reaching full speed at lower IOVDD voltages. For example, at IOVDD = 1.8 V, PLLLOCK output frequencies > 100 MHz are not recommended. The input data is latched on either the rising (**inv_plllock** = 0) or falling edge (**inv_plllock** = 1) of PLLLOCK, which is sensed internally at the output pin.

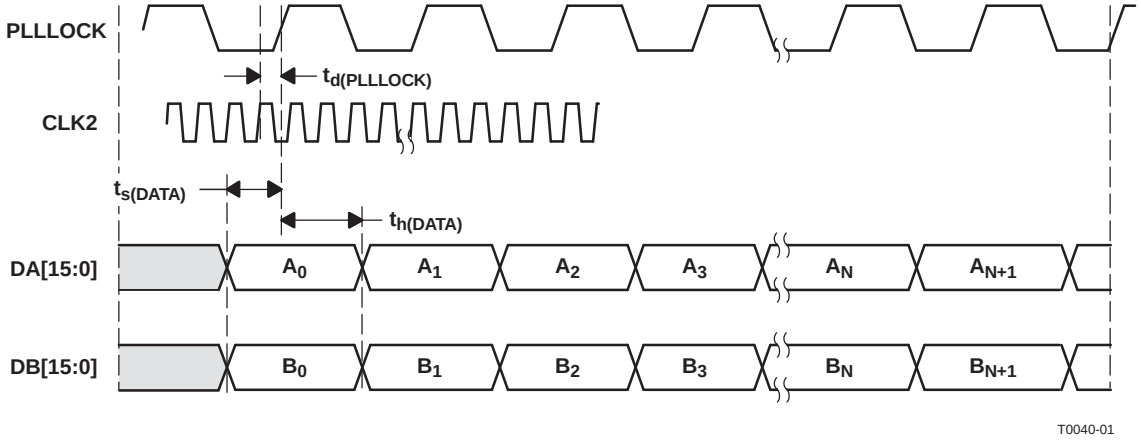


Figure 43. Dual-Bus Mode Timing Diagram for External Clock Mode (PLLLOCK Rising Edge)

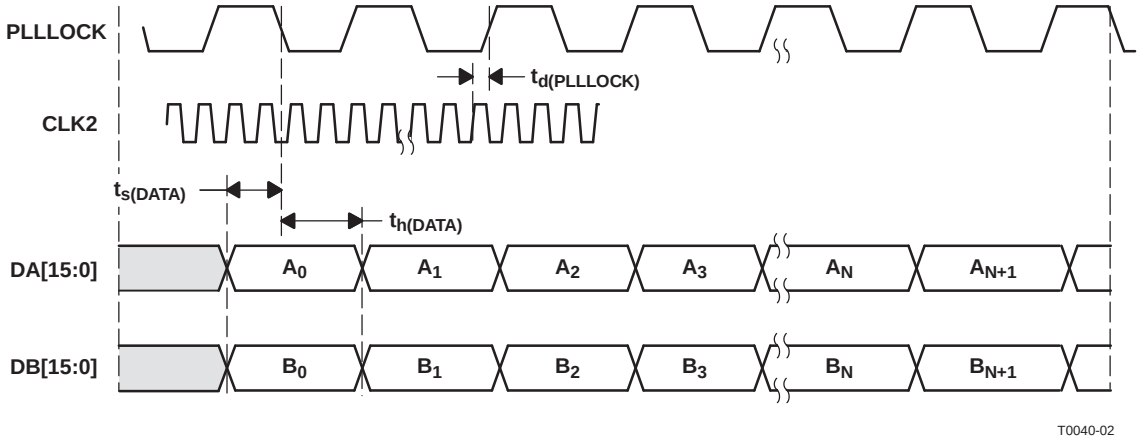


Figure 44. Dual-Bus Mode Timing Diagram for External Clock Mode (PLLLOCK Falling Edge)

2. PLLVDD = 3.3 V (**dual_clk** can be 0 or 1 and is ignored): PLL CLOCK MODE

In PLL CLOCK MODE, drive the DAC at the input sample rate (unless the data is multiplexed) through CLK1/CLK1C. CLK2/CLK2C is not used. In this case, there is no phase ambiguity on the clock. The DAC generates the higher-speed DAC sample-rate clock using an internal PLL/VCO. In PLL clock mode, the user provides a differential external reference clock on CLK1/CLK1C.

A type-four phase-frequency detector (PFD) in the internal PLL compares this reference clock to a feedback clock and drives the PLL to maintain synchronization between the two clocks. The feedback clock is generated by dividing the VCO output by 1×, 2×, 4×, or 8× as selected by the prescaler **div(1:0)**. The output of the prescaler is the DAC sample rate clock and is divided down to generate clocks at ÷2, ÷4, and ÷8. The feedback clock is selected by the registers **sel(1:0)**, which is fed back to the PFD for synchronization to the input clock. The feedback clock is also used for the data input rate, so the ratio of DAC output clock to feedback clock sets the interpolation rate of the DAC5687. The PLLLOCK pin is an output indicating when the PLL has achieved lock. An external RC low-pass PLL filter is provided by the user at pin LPF. See the *Low-Pass Filter* section for filter-setting calculations. This is the only mode where the LPF filter applies.

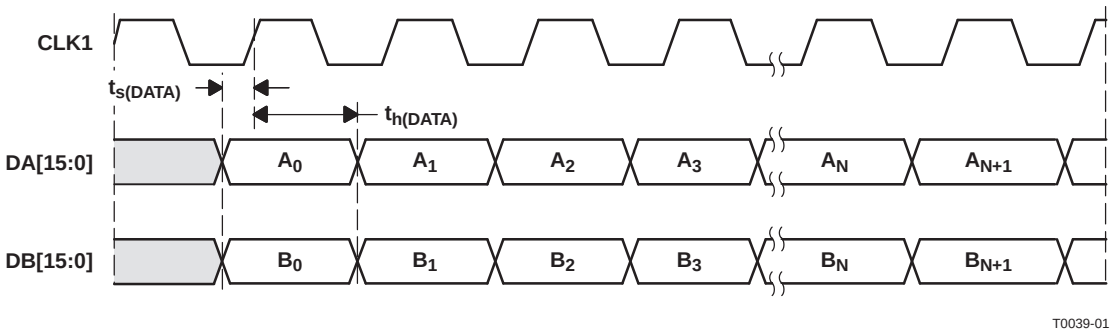


Figure 45. Dual-Bus Mode Timing Diagram (PLL Mode)

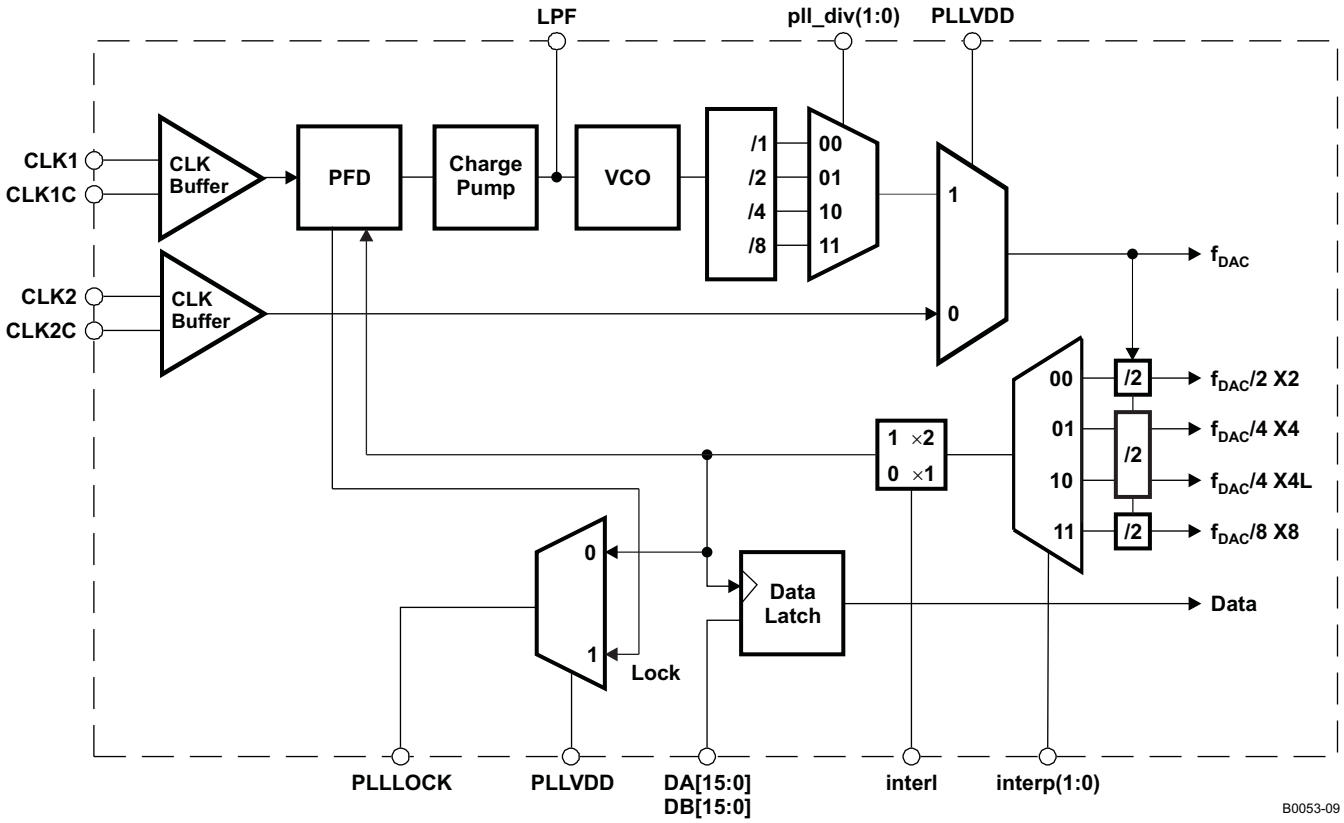


Figure 46. Clock Generation Architecture in PLL Mode

3. PLLVDD = 0 V and **dual_clk** = 1: DUAL CLOCK MODE

In DUAL CLOCK MODE, the DAC is driven at the DAC sample rate through CLK2/CLK2C and the input data rate through CLK1/CLK1C. There are two options in dual clock mode: with FIFO (**inv_plllock** set) and without FIFO (**inv_plllock** clear). If the FIFO is not used, the CLK1/CLK1C input is used to set the phase of the internal clock divider. In this case, the edges of CLK1 and CLK2 must be aligned to within $\pm t_{align}$ (Figure 47), defined as

$$t_{align} = \frac{1}{2f_{CLK2}} - 0.5 \text{ ns}$$

where f_{CLK2} is the clock frequency at CLK2. For example, t_{align} = 0.5 ns at f_{CLK2} = 500 MHz and 1.5 ns at f_{CLK2} = 250 MHz.

If the FIFO is enabled (**inv_plllock** set) in dual clock mode, then CLK1 is only used as an input latch (Figure 48), is independent from the internal divided clock generated from CLK2/CLK2C, and there is no alignment specification. However, the FIFO must be synchronized by one of the methods listed in the **SYNC_CNTL** register, and the latency of the DAC can be up to one clock cycle different, depending on the phase relationship between CLK1 and the internally divided clock.

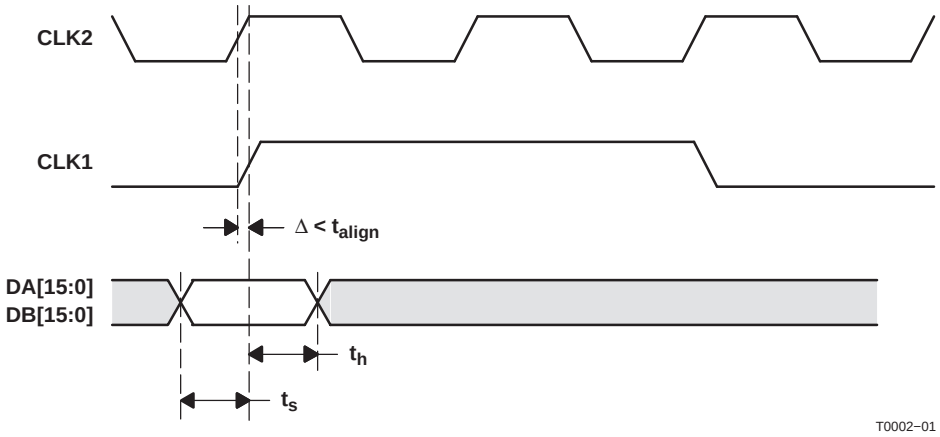


Figure 47. Dual Clock Mode Without FIFO

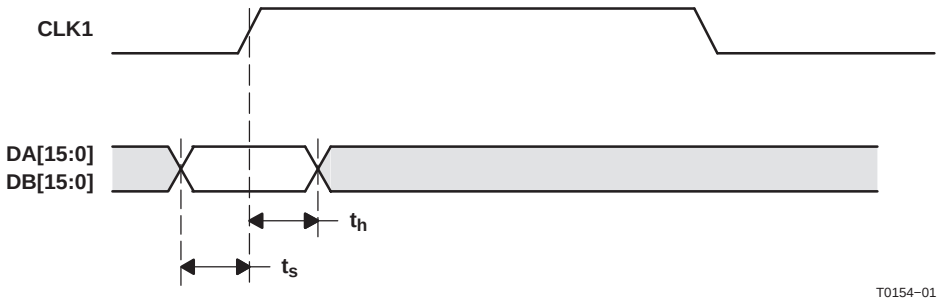


Figure 48. Dual Clock Mode With FIFO

The CDC7005 from Texas Instruments is recommended for providing phase-aligned clocks at different frequencies for this application.

Interleave Bus Mode

In interleave bus mode, one parallel data stream with interleaved data (I and Q) is input to the DAC5687 on data bus **DA**. Interleave bus mode is selected by setting **INTERL** to 1 in the **config_msb** register. Figure 49 shows the DAC5687 data path in interleave bus mode. The interleave bus mode timing diagram is shown in Figure 50.

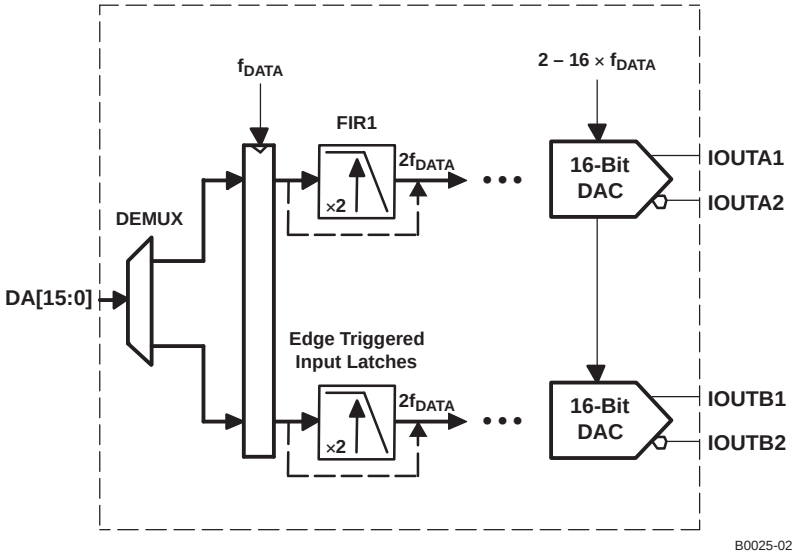


Figure 49. Interleave Bus Mode Data Path

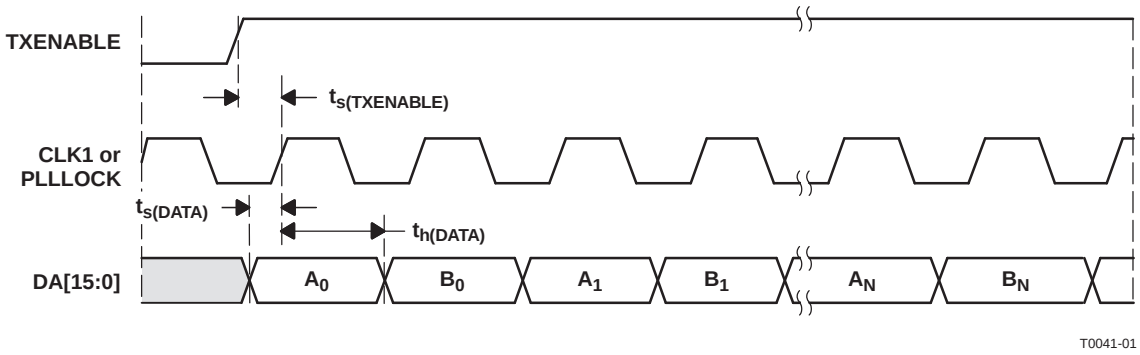


Figure 50. Interleave Bus Mode Timing Diagram Using TXENABLE

Interleaved user data on data bus **DA** is alternately multiplexed to internal data channels A and B. Data channels A and B can be synchronized using either the **QFLAG** pin or the **TXENABLE** pin. When **qflag** in register **config_usb** is 0, transitions on **TXENABLE** identify the interleaved data sequence. The first data after the rising edge of **TXENABLE** is latched with the rising edge of **CLK** as channel-A data. Data is then alternately distributed to B and A channels with successive rising edges of **CLK**. When **qflag** is 1, the **QFLAG** pin is used as an output to identify the interleaved data sequence. **QFLAG** high identifies data as channel B (see Figure 51).

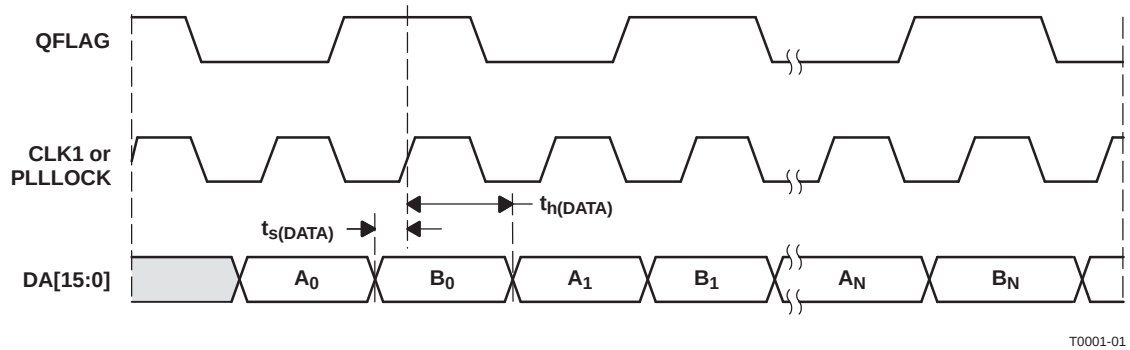


Figure 51. Interleave Bus Mode Timing Diagram Using QFLAG

When using interleaved input mode with the PLL enabled, input clock CLK1 is at 2× the frequency of the input to FIR1. If the dividers for multiple DAC5687s are not synchronized, there can be a one-CLK1-period output time difference between devices that have synchronized input data. However, the divider that generates the clock for the FIR1 input is not connected to the DAC5687 synchronization circuitry. In general, dual-clock mode is recommended in applications where multiple DAC5687s must be synchronized in interleaved input mode. If PLL mode is required, the following workaround using the asynchronous RESET pin synchronizes the clock dividers. With the CLK1 input off and the chip powered, set RESET low for >50 ns and then high for all devices, simultaneously restarting CLK1. Note that the devices must be reprogrammed after the reset sequence. If CLK1 is kept active during the reset sequence, then multiple devices are typically reset to the same clock phase, but because the RESET pin is asynchronous, the clock divider on two devices can come out of reset at slightly different times.

Input FIFO

In external clock mode, where the DAC5687 is clocked at the DAC update rate, the DAC5687 has an optional input FIFO that allows latching of DA[15:0], DB[15:0] and PHSTR based on a user-provided CLK1/CLK1C input or the input data rate clock provided to the PLLLOCK pin. The FIFO can be bypassed by setting register **fifo_bypass** in **CONFIG0** to 1.

The input interface FIFO incorporates a four-sample register file, an input pointer, and an output pointer. Initialization of the FIFO pointers can be programmed to one of seven different sources.

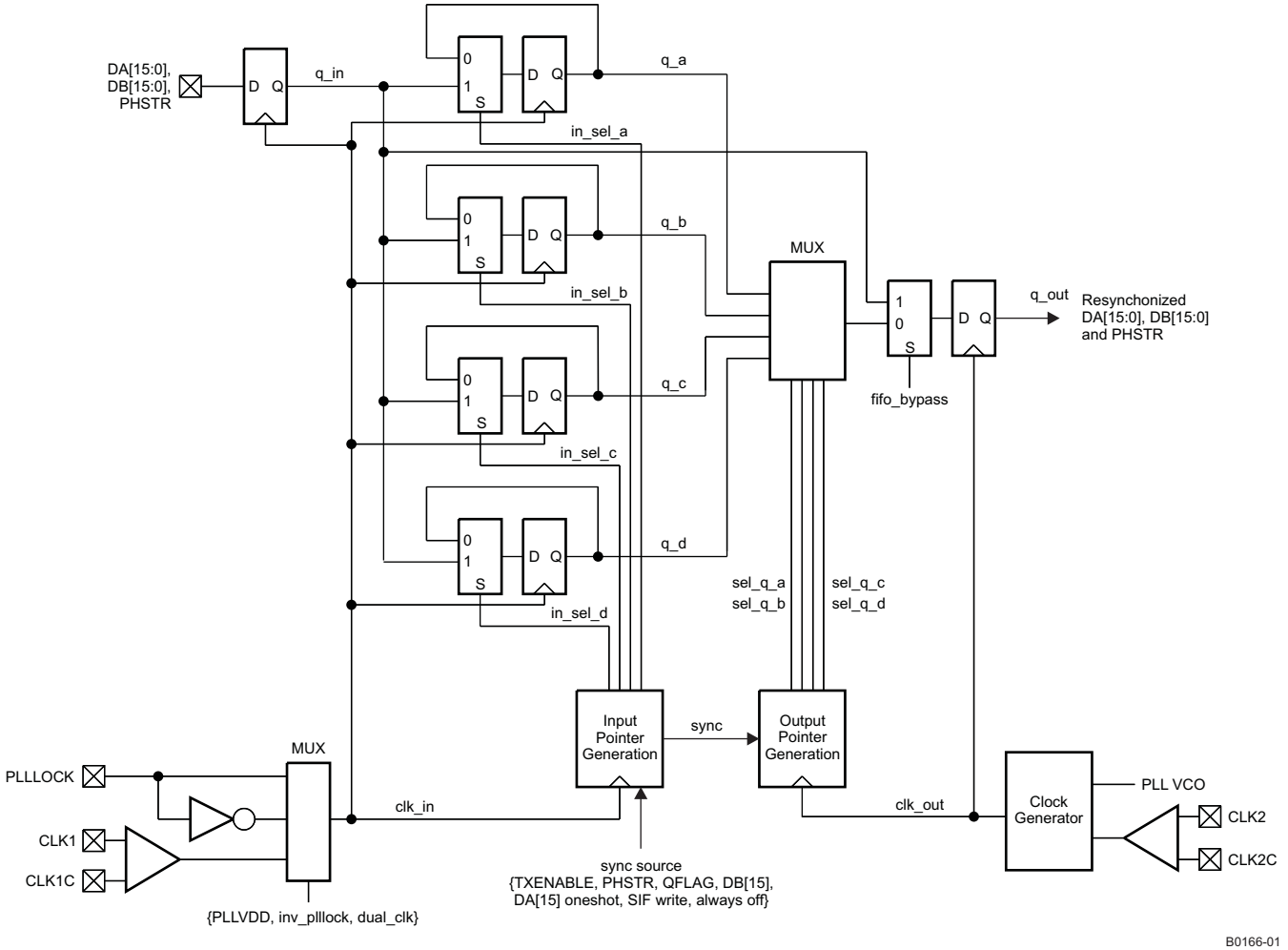


Figure 52. DAC5687 Input FIFO Logic

Initialization of the FIFO block involves selecting and asserting a synchronization source. Initialization causes the input and output pointers to be forced to an offset of 2; the input pointer is forced to the in_sel_a state, while the output pointer is forced to the sel_q_c state. This initialization of the input and output pointers can cause discontinuities in a data stream and should therefore be handled at startup.

Table 12. Synchronization Source Selection

sync_fifo(2:0)	Synchronization Source
000	TXENABLE pin
001	PHSTR pin
010	QFLAG pin
011	DB[15]
100	DA[15] first transition (one shot)
101	Sync now with SIF write (always on)
110	Sync source disabled (always off)
111	Sync now with SIF write (always on)

All possible sync sources are registered with clk_in and then passed through a synchronous rising edge detector.

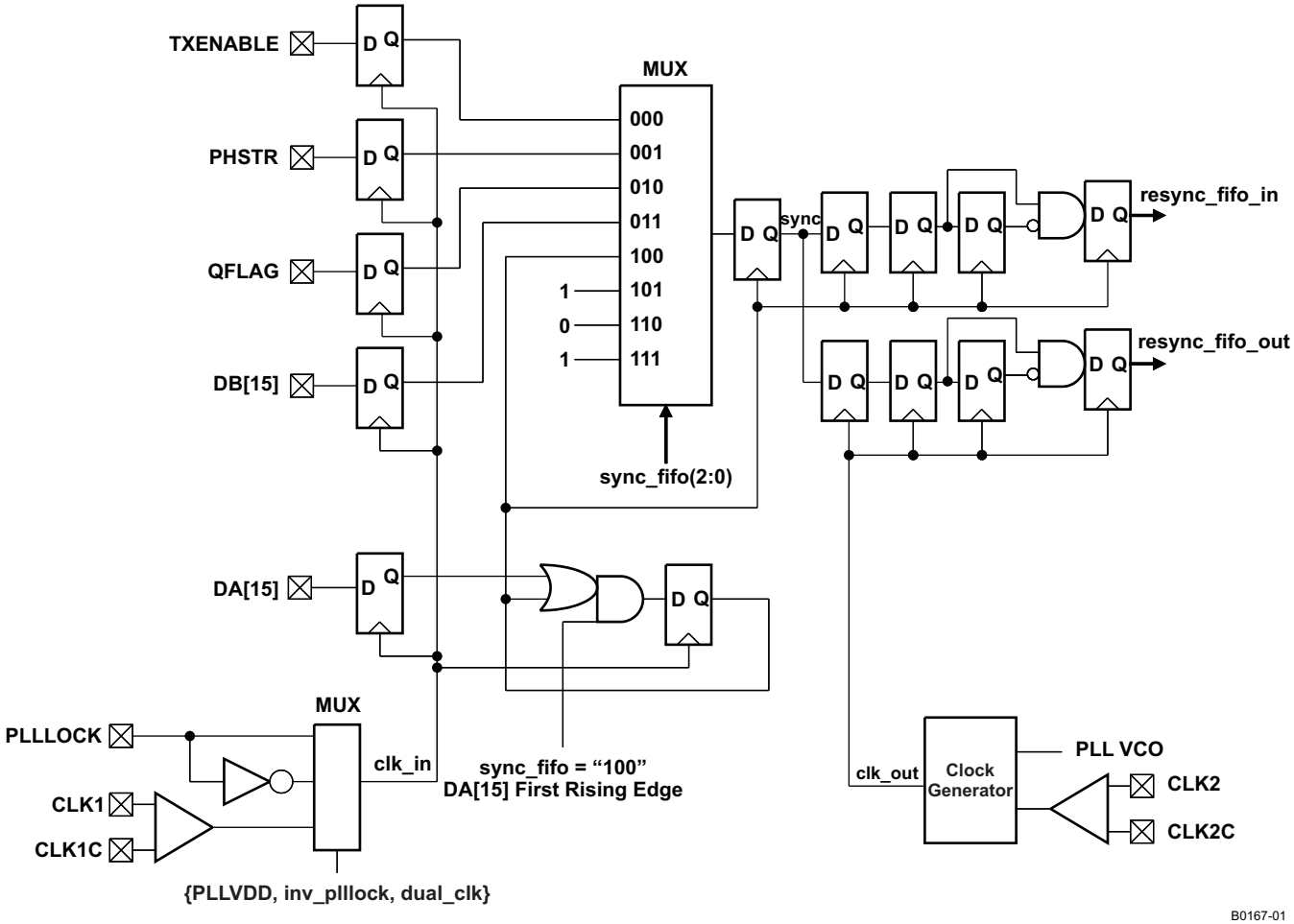


Figure 53. DAC5687 FIFO Synchronization Source Logic

For example, if TXENABLE is selected as the sync source, a low-to-high transition on the TXENABLE pin causes the pointers to be initialized.

Once initialized, the FIFO input pointer advances using clk_in and the output pointer advances using clk_out, providing an *elastic* buffering effect. The phase relationship between clk_in and clk_out can wander or drift until the output pointer overruns the input pointer or vice versa.

Even/Odd Input Mode

The DAC5687 has a double data rate input mode that allows both input ports to be used to multiplex data onto one DAC channel (A). In the even/odd mode, the FIR3 filter can be used to interpolate the data by 2×. The even/odd input mode is enabled by setting **half_rate** in **CONFIG3**. The maximum input rate for each port is 250 MSPS, for a combined rate of 500 MSPS.

Synchronization

The DAC5687 has several digital circuits that can be synchronized to a known state. The circuits that can be synchronized are the fine mixer (NCO), coarse mixer (fixed $f_S/2$ or $f_S/4$ mixer), the FIFO input and output pointers, and the internal clock divider.

Table 13. Synchronization in Different Clock Modes

Clock Mode	PLLVDD Pin	Serial Interface Register Bits			DA, DB, PHSTR, and TXENABLE Latch	Description
		fifo_bypass	dual_clk	inv_plllock		
Single external clock without FIFO	0 V	1	0	0	PLLLOCK rising edge	Signal at the PLLLOCK output pin is used to clock the PHSTR signal into the chip. The PLLLOCK output clock is generated by dividing the CLK2/CLK2C input signal by the programmed interpolation and interface settings.
				1	PLLLOCK falling edge	
Single external clock with FIFO	0 V	0	0	0	PLLLOCK rising edge	Signal at the PLLLOCK output pin is used to clock the PHSTR signal into the chip. The PLLLOCK output clock is generated by dividing the CLK2/CLK2C input signal by the programmed interpolation and interface settings. Enabling the FIFO allows the chip to function with large loads on the PLLLOCK output pin at high input rates. *The FIFO must be initialized first in this mode*.
				1	PLLLOCK falling edge	
Dual external clock without FIFO	0 V	1	1	0	CLK1/CLK1C	The CLK1/CLK1C input signal is used to clock in the PHSTR signal. CLK1/CLK1C and CLK2/CLK2C are both input to the chip, and the phase relationship must be tightly controlled.
Dual external clock with FIFO	0 V	0	1	1	CLK1/CLK1C	The CLK1/CLK1C input signal is used to clock in the PHSTR signal. CLK1/CLK1C and CLK2/CLK2C are both input to the chip, but no phase relationship is required. The FIFO input circuits are used to manage the clock domain transfers. *The FIFO must be initialized in this mode.*
PLL enabled	3.3 V	1	0	0	CLK1/CLK1C	The CLK1/CLK1C input signal is used to clock in the PHSTR signal. *The FIFO must be bypassed when the PLL is enabled*.

NCO Synchronization

The phase accumulator in the NCO block (see the *Fine Mixer (FMIX)* section and Figure 39 for a description of the NCO) can be synchronously reset when PHSTR is asserted. The PHSTR signal passes through the input FIFO block, using the input clock associated with the clocking mode. If the FIFO is enabled, there can be some uncertainty in the exact instant the PHSTR synchronization signal arrives at the NCO accumulator due to the *elastic* capabilities of the FIFO. For example, in dual-clock mode with the FIFO enabled, the internal clock generator divides down the CLK2/CLK2C input signal to generate the FIFO output clock. The phase of this generated clock is unknown externally, resulting in an uncertainty of the exact PHSTR instant of as much as a few input clock cycles.

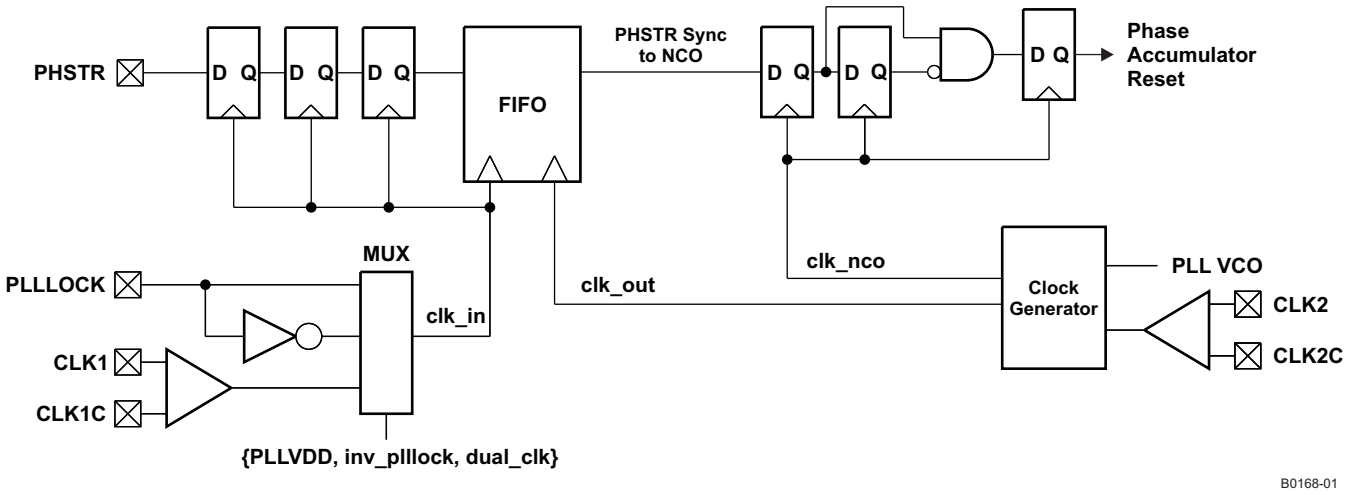


Figure 54. Logic Path for PHSTR Synchronization Signal to NCO

The serial interface includes a **sync_nco** bit in register **SYNC_CNTL**, which must be set for the PHSTR input signal to initialize the phase accumulator.

The NCO uses a rising edge detector to perform the synchronous reset of the phase accumulator. Due to the pipelined nature of the NCO, the latency from the phstr sync signal at the FIFO output to the instant the phase accumulator is cleared is 13 f_{NCO} clock cycles (f_{NCO} = f_{DAC} in X4 mode, f_{NCO} = f_{DAC}/2 in X2, X4L, and X8 modes). In 2× interpolation mode with the inverse sinc filter disabled, overall latency from PHSTR input to DAC output is ~100 input clock cycles.

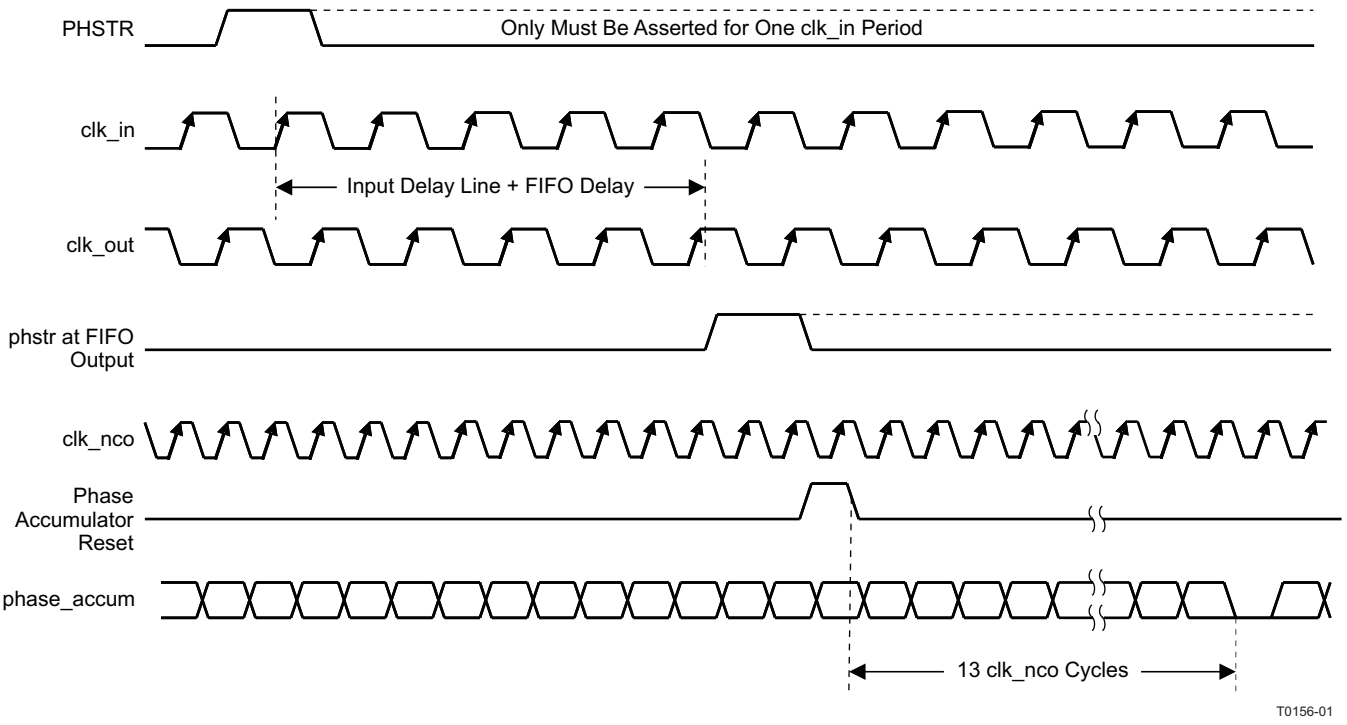


Figure 55. NCO Phase Accumulator Reset Synchronization Timing

Coarse Mixer (CMIX) Synchronization

The coarse mixer implements the $f_{DAC}/2$ and $f_{DAC}/4$ (and $-f_{DAC}/4$) fixed complex mixing operation using simple complements of the data-path signals to create the proper sequences. The sequences are controlled using a simple counter, and this counter can be synchronously reset using the PHSTR signal.

Similar to the NCO, the PHSTR signal used by the coarse mixer is from the FIFO output. This introduces the same uncertainty effect due to the FIFO input-to-output pointer relationship. Bypassing the FIFO and using the dual external clock mode without FIFO eliminates this uncertainty for systems using multiple DAC5687 devices when this cannot be tolerated. Using the internal PLL, as with the NCO, allows the complete control and synchronization of the coarse mixer.

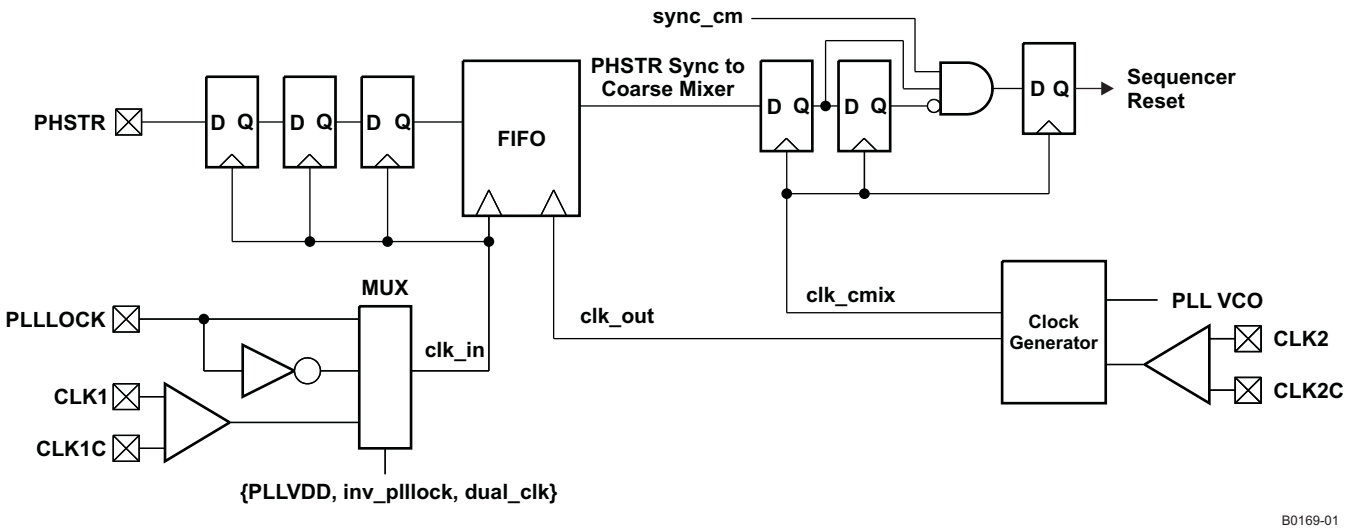


Figure 56. Logic Path for PHSTR Synchronization Signal to CMIX Reset

To enable the PHSTR synchronous reset, the serial interface bit **sync_cm** in register **SYNC_CNTL** must be set. The coarse mixer sequence counter is held in reset when PHSTR is low and operates when PHSTR is high.

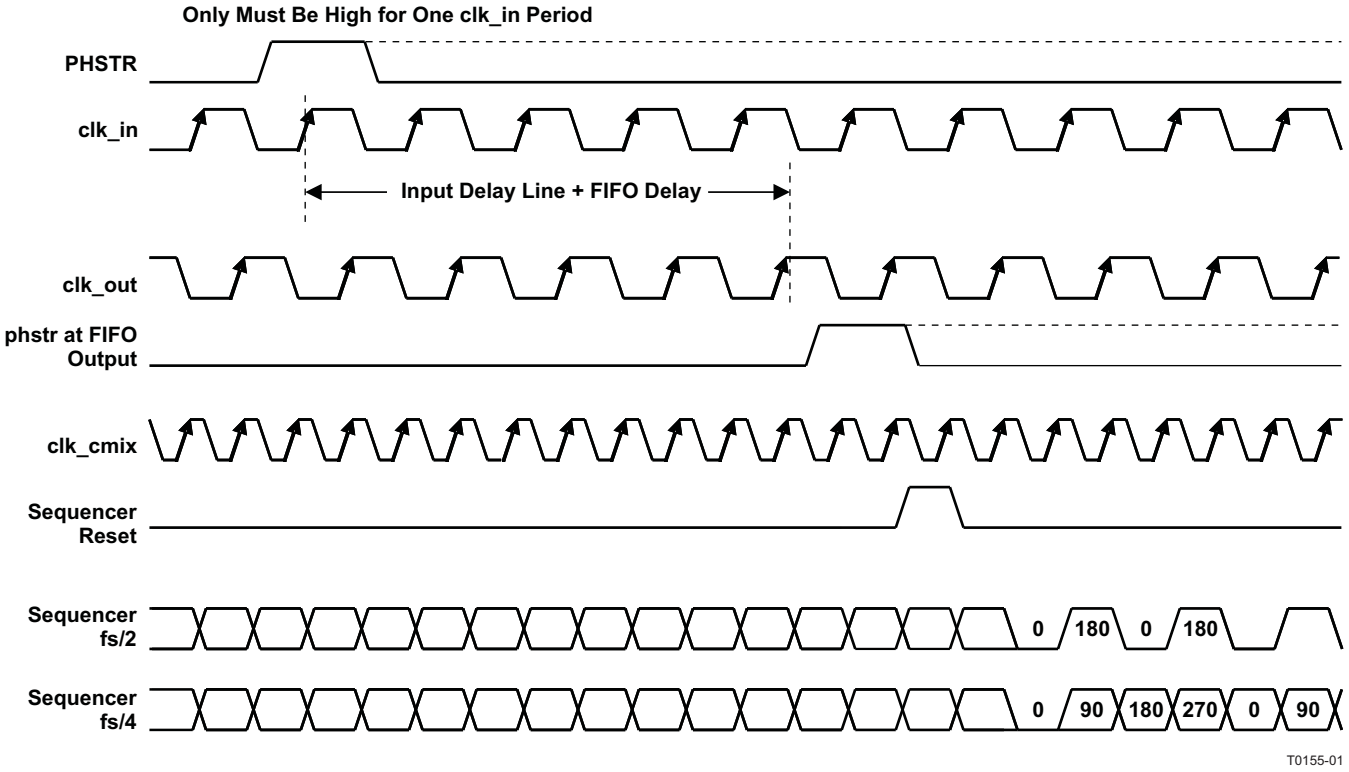


Figure 57. CMIX Reset Synchronization Timing

In addition to the reset function provided by the PHSTR signal, the **phstr_del(1:0)** bits in register **ATEST** allow the user to select the initial (reset) state. Changing the cm_mode lower 2 bits produces the same phase shift results.

Table 14. Initial State of CMIX After Reset

Fix Mix Selection	phstr_del(1:0)	Initial State at PHSTR
$f_S/2$	00 and 10	Normal
$f_S/2$	01 and 11	180-degree shift
$f_S/4$	00	Normal
$f_S/4$	01	90-degree shift
$f_S/4$	10	180-degree shift
$f_S/4$	11	270-degree shift

Input Clock Synchronization of Multiple DAC5687s

For applications where multiple DAC5687 chips are used, clock synchronization is best achieved by using dual-clock mode with the FIFO disabled or the PLL-clock mode. In the dual-clock mode with FIFO disabled, an appropriate clock PLL such as the CDC7005 is required to provide the DAC and input rate clocks that meet the skew requirement $\mathbf{t_{align}}$ (see Figure 47). An example for synchronizing multiple DAC5687 devices in dual clock mode with two CDC7005s is shown in Figure 58. When using the internal PLL-clock mode, synchronization of multiple using PHSTR is completely deterministic due to the phase/frequency detector in the PLL feedback loop. All chips using the same CLK1/CLK1C input clock have identical internal clocking phases.

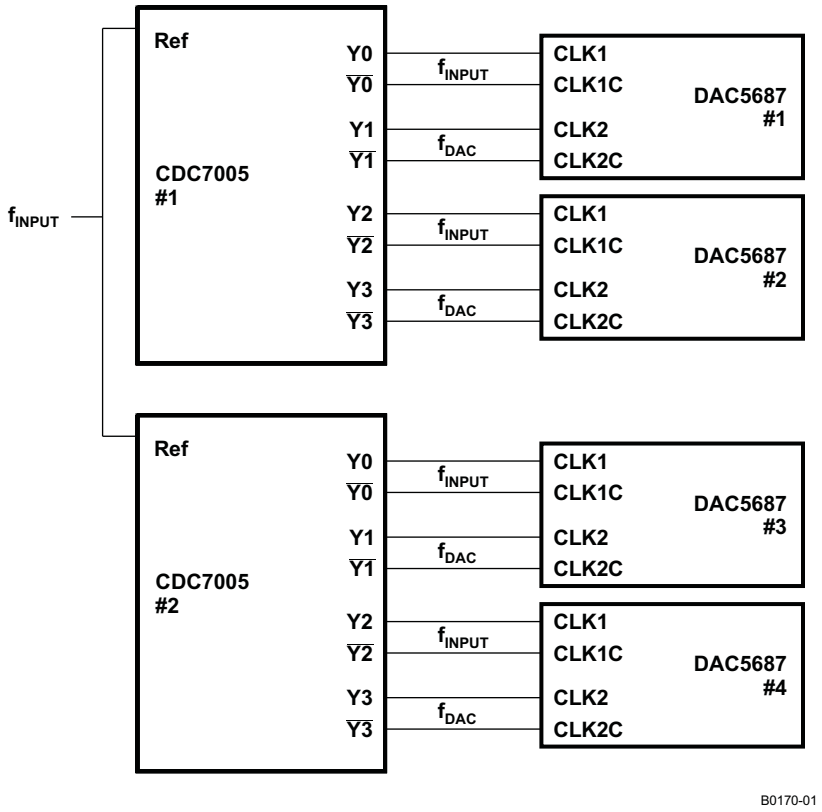


Figure 58. Block Diagram for Clock Synchronization of Multiple DAC5687 Devices in Dual-Clock Mode

Reference Operation

The DAC5687 comprises a band-gap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current IBIAS through resistor R_{BIAS} is defined by the on-chip band-gap reference voltage and control amplifier. The full-scale output current equals 16 times this bias current. The full-scale output current $IOUT_{FS}$ can thus be expressed as:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{EXTIO} / R_{BIAS}$$

where V_{EXTIO} is the voltage at terminal EXTIO. The band-gap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor C_{EXT} of 0.1 μF should be connected externally to terminal EXTIO for compensation. The band-gap reference can additionally be used for external reference operation. In that case, an external buffer with high-impedance input should be applied in order to limit the band-gap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor C_{EXT} may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 mA.

DAC Transfer Function

The CMOS DACs consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current of each current source through either one of the complementary output nodes IOUT1 or IOUT2. Complementary output currents enable differential operation, thus canceling out common-mode noise sources (digital feedthrough, on-chip and PCB noise), dc offsets, even-order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip band-gap voltage reference source (1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 16 times IBIAS. The full-scale current $IOUT_{FS}$ can be adjusted from 20 mA down to 2 mA.

The relation between IOUT1 and IOUT2 can be expressed as:

$$IOUT1 = –IOUT_{FS} – IOUT2$$

Current flowing into a node is denoted as – current, and current flowing out of a node as + current. Because the output stage is a current sink, the current can only flow from AVDD into the IOUT1 and IOUT2 pins. If IOUT2 = –5 mA and $IOUT_{FS}$ = 20 mA then:

$$IOUT1 = –20 – (–5) = –15 \text{ mA}$$

The output current flow in each pin driving a resistive load can be expressed as:

$$IOUT1 = IOUT_{FS} \times CODE / 65{,}536$$

$$IOUT2 = IOUT_{FS} \times (65{,}535 – CODE) / 65{,}536$$

where CODE is the decimal representation of the DAC data input word.

For the case where IOUT1 and IOUT2 drive resistor loads R_L directly, this translates into single-ended voltages at IOUT1 and IOUT2:

$$VOUT1 = AVDD – | IOUT1 | \times R_L$$

$$VOUT2 = AVDD – | IOUT2 | \times R_L$$

Assuming that the data is full scale (65,535 in offset binary notation) and R_L is 25 Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as:

$$VOUT1 = AVDD – | –20 \text{ mA} | \times 25 \Omega = 2.8 \text{ V}$$

$$VOUT2 = AVDD – | –0 \text{ mA} | \times 25 \Omega = 3.3 \text{ V}$$

$$VDIFF = VOUT1 – VOUT2 – 0.5 \text{ V}$$

Note that care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

Analog Current Outputs

Figure 59 shows a simplified schematic of the current source array output with corresponding switches. Differential switches direct the current of each individual NMOS current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referred to AVDD. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to AVDD – 0.5 V. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals AVDD + 0.5 V. Beyond this value, transistor breakdown may occur, resulting in reduced reliability of the DAC5687 device. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral nonlinearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 is in the range of AVDD ±0.5 V.

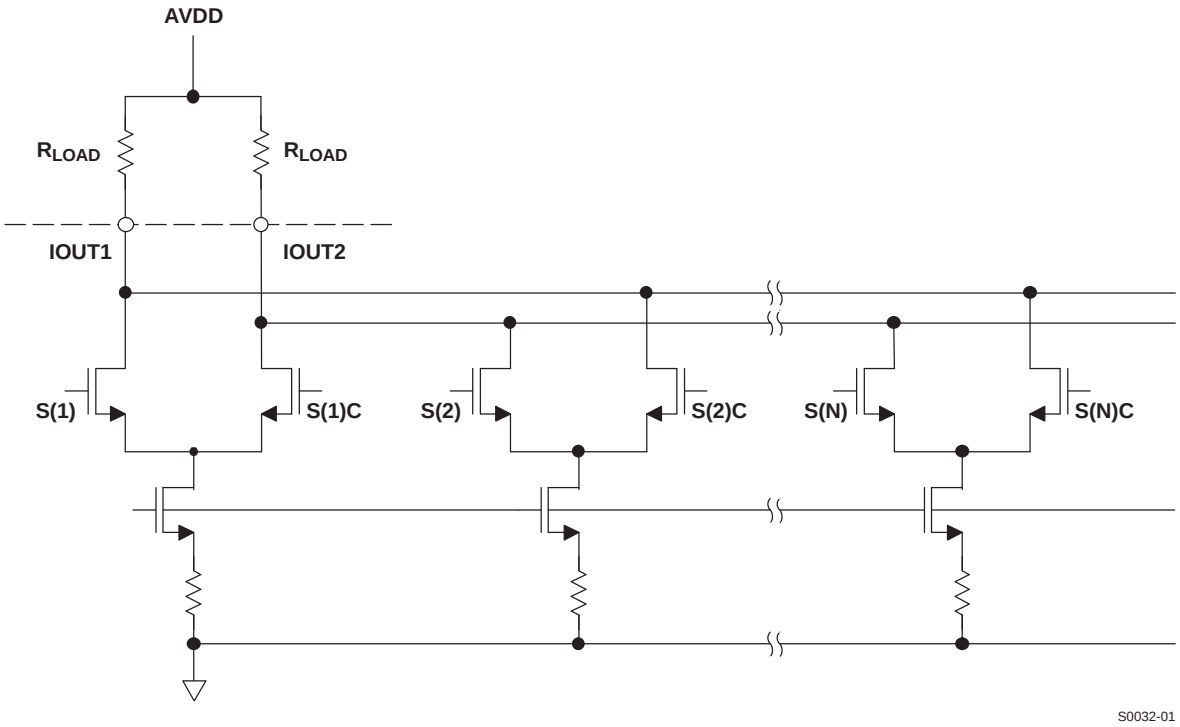


Figure 59. Equivalent Analog Current Output

The DAC5687 can be easily configured to drive a doubly terminated 50-Ω cable using a properly selected RF transformer. Figure 60 and Figure 61 show the 50-Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. Note that the center tap of the primary input of the transformer must be connected to AVDD to enable a dc current flow. Applying a 20-mA full-scale output current would lead to a 0.5-V_{PP} output for a 1:1 transformer and a 1-V_{PP} output for a 4:1 transformer. The low dc impedance between the IOUT1 or IOUT2 and the transformer center tap sets the center of the ac signal at AVDD, so the 1-V_{PP} output for the 4:1 transformer results in an output between AVDD + 0.5 V and AVDD – 0.5 V.

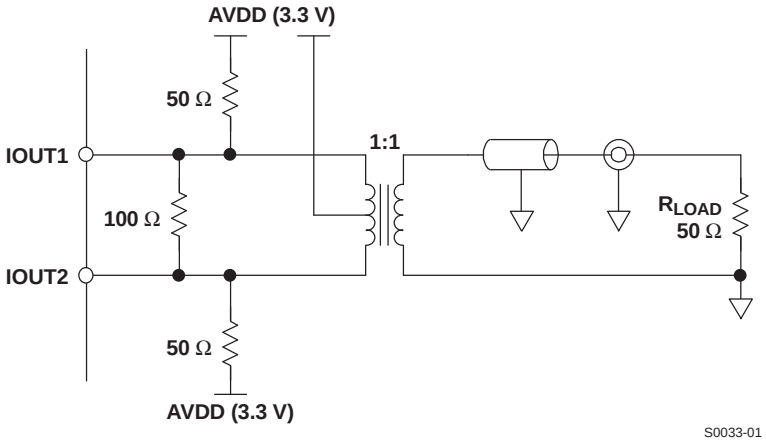


Figure 60. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

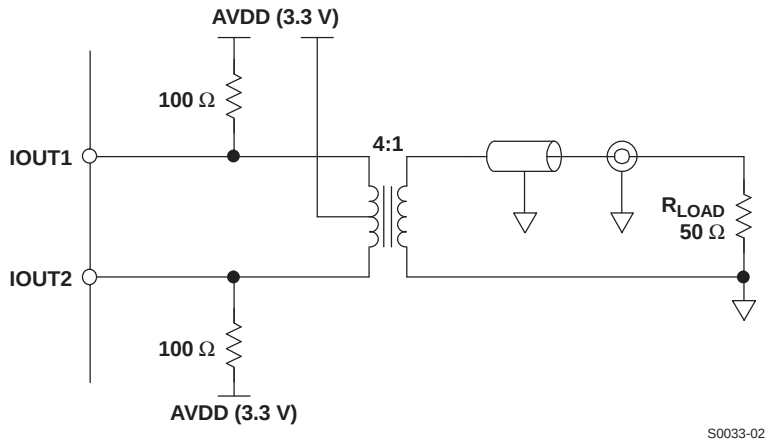


Figure 61. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

Combined Output Termination

The DAC5687 DAC A and DAC B outputs can be summed together as shown in Figure 62 to provide a 40-mA full-scale output for increased output power.

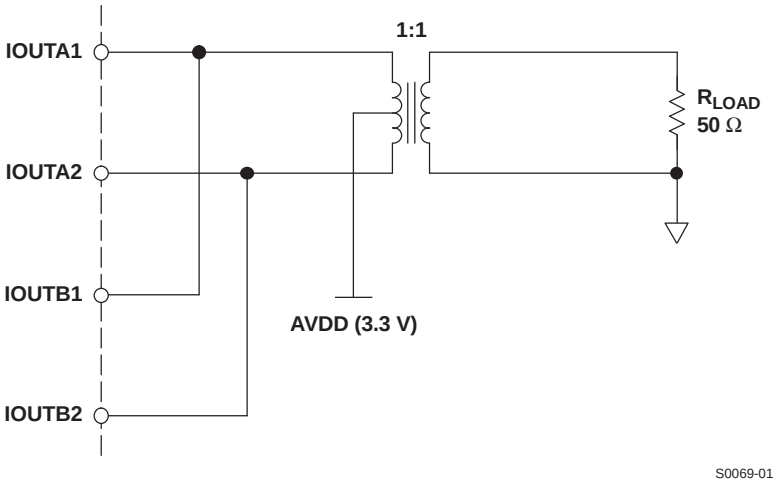


Figure 62. Combined Output Termination Using a 1:1 Impedance Ratio Transformer Into 50-Ω Load

For the case where the digital codes for the two DACs are identical, the termination results in a full-scale swing of 2 V_{PP} into the 50-Ω load, or 10 dBm. This is 6 dB higher than the 4:1 output termination recommended for a single DAC output.

There are two methods to produce identical DAC codes. In modes where there is mixing between digital channels A and B, i.e., when channels A and B are isolated, the identical data can be sent to both input ports to produce identical DAC codes. Channels A and B are isolated when FMIX is disabled, the QMC is disabled or enabled with QMC phase register set to 0, and CMIX is disabled or set to $f_{DAC}/2$. Note that frequency upconversion is still possible using the high-pass filter setting and CMIX $f_{DAC}/2$.

Alternatively, by applying the input data on one input port only and setting the other input port to midscale (zero), the NCO can be used to duplicate the output of the active input channel in the other channel by setting the frequency to zero, phase to 8192 and NCO_GAIN = 1 and QMC gain = 1446. Assuming I(t) is the wanted signal and Q(t) = 0, this is demonstrated by the simplification of the NCO equations in the *Fine Mixer (FMIX)* section:

$$I_{OUT}(t) = (I_{IN}(t)\cos(2\pi \times 0 \times t + \pi/4) - 0 \times \sin(2\pi \times 0 \times t + \pi/4) \times 2^{(1\ -\ 1)} = I_{IN}(t)\cos(\pi/4) = I_{IN}(t)/2^{½}$$

$$Q_{OUT}(t) = (I_{IN}(t)\sin(2\pi \times 0 \times t + \pi/4) + 0 \times \cos(2\pi \times 0 \times t + \pi/4)) \times 2^{(1-1)} = I_{IN}(t)\sin(\pi/4) = I_{IN}(t)/2^{½}$$

Applying the QMC gain of 1446, equivalent to $2^{½}$, increases the signal back to unity gain through the FMIX and the QMC blocks.

Note that with this termination, the DAC side of the transformer is not 50-Ω terminated and therefore may result in reflections when used with a cable output.

Digital Inputs

Figure 63 shows a schematic of the equivalent CMOS digital inputs of the DAC5687. DA[15:0], DB[15:0], SLEEP, PHSTR, TXENABLE, QFLAG, SDIO, SCLK, and SDENB have pulldown resistors and RESETB has a pullup resistor internal to the DAC5687. See the specification table for logic thresholds. The pullup and pulldown circuitry is approximately equivalent to 100 kΩ.

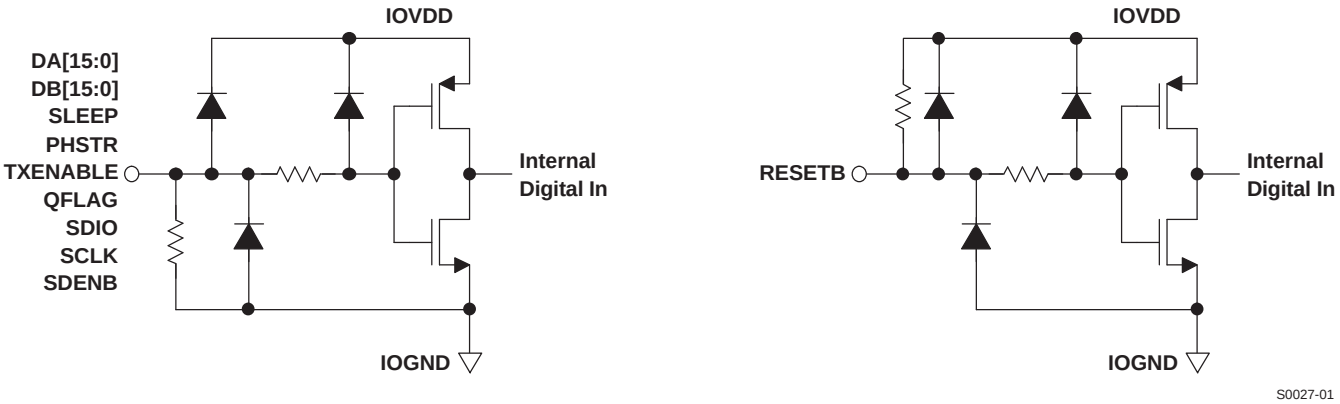


Figure 63. CMOS/TTL Digital Equivalent Input

Clock Inputs

Figure 64 shows an equivalent circuit for the clock input.

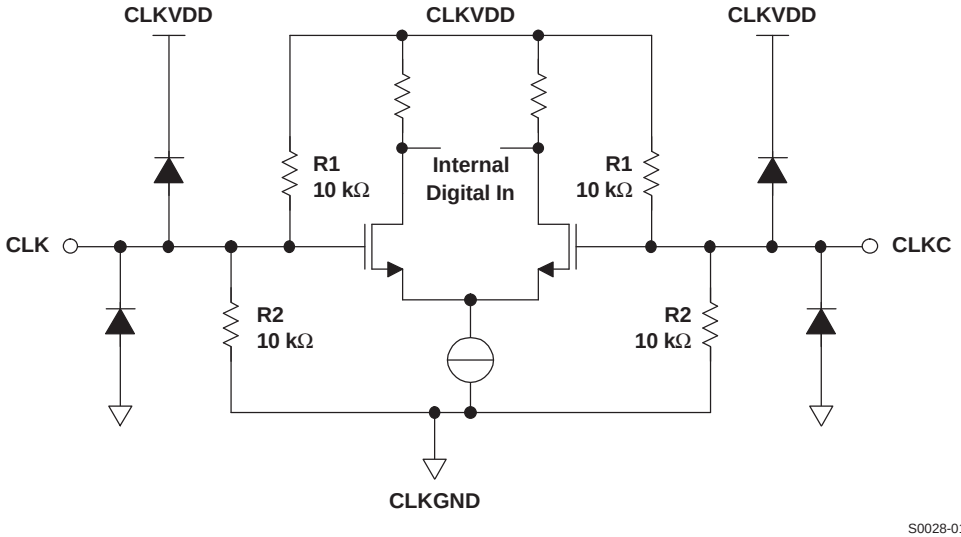


Figure 64. Clock Input Equivalent Circuit

Figure 65, Figure 66, and Figure 67 show various input configurations for driving the differential clock input (CLK/CLKC).

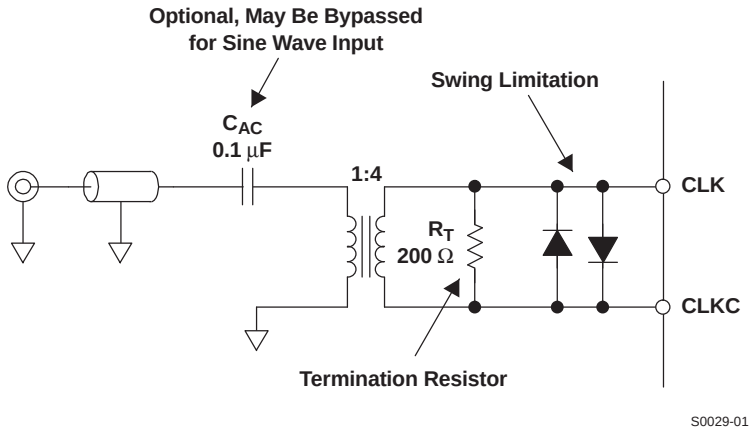


Figure 65. Clock Input Configuration Using 50-Ω Cable Input

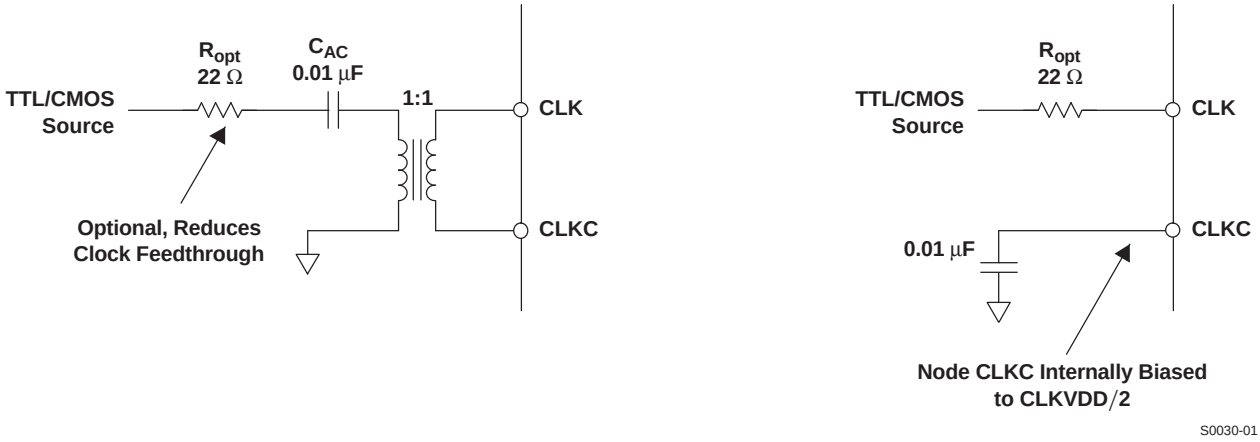


Figure 66. Driving the DAC5687 With a Single-Ended TTL/CMOS Clock Source

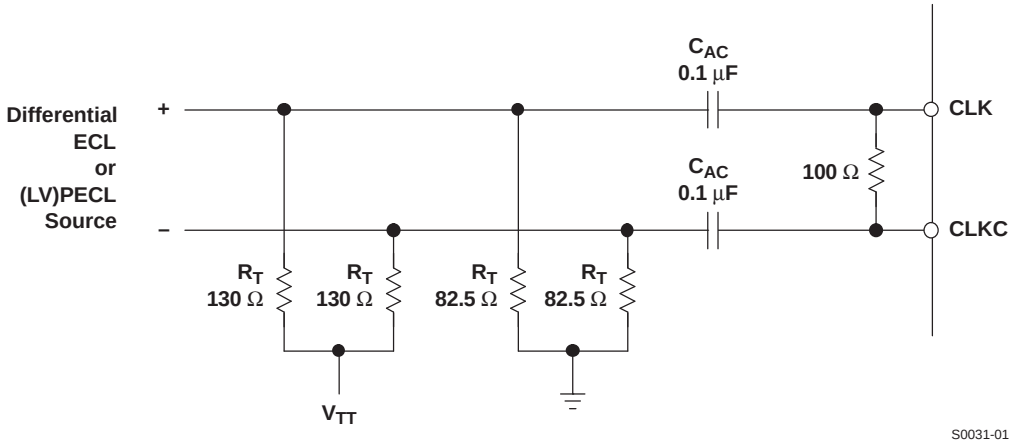


Figure 67. Driving the DAC5687 With Differential ECL/PECL Clock Source

Power-Up Sequence

In all conditions, bring up DVDD first. If PLLVDD is powered (PLL on), CLKVDD should be powered before or simultaneously with PLLVDD. AVDD, CLKVDD, and IOVDD can be powered simultaneously or in any order. Within AVDD, the multiple AVDD pins should be powered simultaneously.

There are no specific requirements on the ramp rate for the supplies.

Sleep Mode

The DAC5687 features a power-down mode that turns off the output current and reduces the supply current to less than 5 mA over the supply range of 3 V to 3.6 V and temperature range. The power-down mode is activated by applying a logic level 1 to the SLEEP pin (e.g., by connecting pin SLEEP to AVDD). An internal pulldown circuit at node SLEEP ensures that the DAC5687 is enabled if the input is left disconnected. Power-up and power-down activation times depend on the value of external capacitor at node EXTIO. For a nominal capacitor value of 0.1 μF, power down takes less than 5 μs and approximately 3 ms to power back up.

APPLICATION INFORMATION

Designing the PLL Loop Filter

Table 15. Optimum DAC5687 PLL Settings

f_{DAC} (MHz)	pll_freq	pll_kv	pll_div(1:0)	f_{VCO}/f_{DAC}	Estimated G_{VCO} (MHz/V)
25 to 28.125	0	0	11	8	380
28.125 to 46.25	0	1	11	8	250
46.25 to 60	0	0	11	8	300
60 to 61.875	1	1	11	8	130
61.875 to 65	1	0	11	8	225
65 to 92.5	0	1	10	4	250
92.5 to 120	0	0	10	4	300
120 to 123.75	1	1	10	4	130
123.75 to 130	1	0	10	4	225
130 to 185	0	1	01	2	250
185 to 240	0	0	01	2	300
240 to 247.5	1	1	01	2	130
247.5 to 260	1	0	01	2	225
260 to 370	0	1	00	1	250
370 to 480	0	0	00	1	300
480 to 495	1	1	00	1	130
495 to 520	1	0	00	1	225

The optimized DAC5687 PLL settings based on the VCO frequency MIN and MAX values (see the digital specifications) as a function of f_{DAC} are listed in Table 15. To minimize phase noise at a given f_{DAC}, **pll_freq**, **pll_kv**, and **pll_div** have been chosen so G_{VCO} is minimized and within the MIN and MAX frequency for a given setting.

For example, if f_{DAC} = 245.76 MHz, **pll_freq** is set to 1, **pll_kv** is set to 0 and **pll_div(1:0)** is set to 01 (divide by 2) to lock the VCO at 491.52 MHz.

The external loop filter components C1, C2, and R1 are set by the G_{VCO}, $N = f_{VCO}/f_{DATA} = f_{VCO} \times \text{Interpolation}/f_{DAC}$, the loop phase margin ϕ_d and the loop bandwidth ω_d. Except for applications where abrupt clock frequency changes require a fast PLL lock time, it is suggested that ϕ_d be set to at least 80 degrees for stable locking and suppression of the phase-noise side lobes. Phase margins of 60 degrees or less can be sensitive to board layout and decoupling details.

C1, C2, and R1 are then calculated by the following equations

$$C1 = \tau1\left(1 - \frac{\tau2}{\tau3}\right) \qquad C2 = \frac{\tau1 - \tau2}{\tau3} \qquad R1 = \frac{\tau3^2}{\tau1\,(\tau3 - \tau2)}$$

where,

$$\tau1 = \frac{K_d K_{vco}}{\omega_d^2}\left(\tan\phi_d + \sec\phi_d\right) \qquad \tau2 = \frac{1}{\omega_d\left(\tan\phi_d + \sec\phi_d\right)} \qquad \tau3 = \frac{\tan\phi_d + \sec\phi_d}{\omega_d}$$

and

charge pump current: iqp = 1 mA

vco gain: $K_{VCO} = 2\pi \times G_{VCO}$ rad/V

FVCO/FDATA: N = {2, 4, 8, 16, 32}

phase detector gain: $K_d = iqp \times (2 \times N) - 1$ A/rad

An Excel™ spreadsheet is provided by Texas Instruments for automatically calculating the values for C1, C2, and R.

Completing the example given previously with:

Parameter	Value	Units
G_{VCO}	1.30E+02	MHz/V
ωd	0.50E+00	MHz
N	4	
ϕd	80	Degrees

The component values are:

C1 (F)	C2 (F)	R (Ω)
3.74E–08	2.88E–10	9.74E+01

As the PLL characteristics are not sensitive to these components, the closest 20% tolerance capacitor and 1% tolerance resistor values can be used. If the calculation results in a negative value for C2 or an unrealistically large value for C1, then the phase margin may need to be reduced slightly.

DAC5687 Passive Interface to Analog Quadrature Modulators

The DAC5687 has a maximum 20-mA full-scale output and a compliance range of AVDD ±0.5 V. The TRF3701 or TRF3702 analog quadrature modulators (AQM) require a common mode of approximately 3.7 V and 1.5 V to 2-V_{PP} differential swing. A resistive network as shown in Figure 68 can be used to translate the common-mode voltage between the DAC5687 and TRF3701 or TRF3702. The voltage at the DAC output pins for a full-scale sine wave is centered at approximately AVDD with a 1-V_{PP} single-ended (2-V_{PP} differential) swing. The voltage at the TRF3701/2 input pins is centered at 3.7 V and swings 0.76-V_{PP} single-ended (1.52-V_{PP} differential), or 2.4 dB of insertion loss.

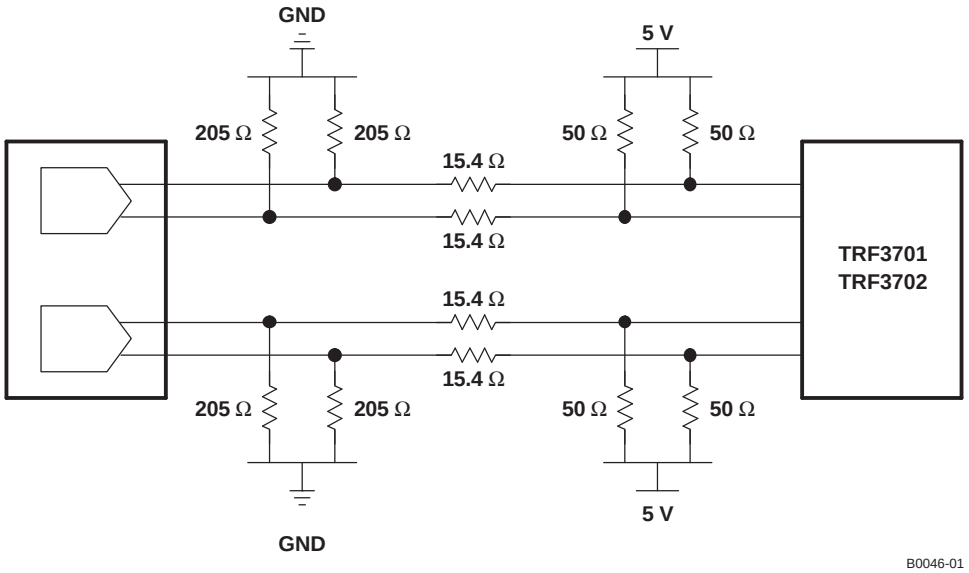


Figure 68. DAC5687 Passive Interface to TRF3701/2 Analog Quadrature Modulator

Changing the voltage levels and resistor values enables other common-mode voltages at the analog quadrature modulator input. For example, the network shown in Figure 69 can produce a 3.3-V common mode for the TRF3703-33, with a 0.96-V_{PP} single-ended swing (1.56-V_{PP} differential swing).

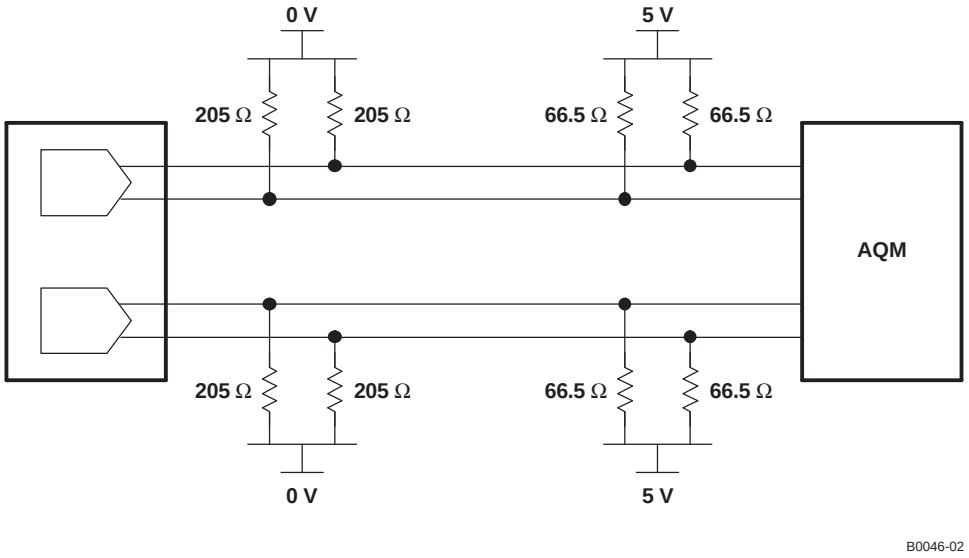


Figure 69. DAC5687 Passive Interface to TRF3703-33 Analog Quadrature Modulator

Nonharmonic Clock-Related Spurious Signals

In interpolating DACs, imperfect isolation between the digital and DAC clock circuits generates spurious signals at frequencies related to the DAC clock rate. The digital interpolation filters in these DACs run at subharmonic frequencies of the output rate clock, where these frequencies are $f_{DAC}/2^N$, N = 1 – 3. For example, for X2 mode there is only one interpolation filter running at $f_{DAC}/2$; for X4 and X4L modes, on the other hand, there are two interpolation filters running at $f_{DAC}/2$ and $f_{DAC}/4$. In X8 mode, there are three interpolation filters running at $f_{DAC}/2$, $f_{DAC}/4$, and $f_{DAC}/8$. These lower-speed clocks for the interpolation filter mix with the DAC clock circuit and create spurious images of the wanted signal and second Nyquist-zone image at offsets of $f_{DAC}/2^N$.

To calculate the nonharmonic clock-related spurious signals for a particular condition, we first determine the location of the spurious signals and then the amplitude.

Location of the Spurious Signals

The location of the spurious signals is determined by the DAC5687 output frequency (f_{SIG}) and whether the output is used as a dual-output complex signal to be fed to an analog quadrature modulator (AQM) or as a real IF signal from a single DAC output.

Figure 70 shows the location of spurious signals for X2 mode as a function of f_{SIG}/f_{DAC}. For complex outputs, the spurious frequencies cover a range of $-0.5 \times f_{DAC}$ to $0.5 \times f_{DAC}$, with the negative complex frequency indicating that the spurious signal falls in the opposite sideband from the wanted signal at the output of the AQM. For the real output, the phase information for the spurious signal is lost, and therefore what was a negative frequency for the complex output is a positive frequency for a real output.

For the X2 mode, there is one spurious frequency with an absolute frequency less than $0.5 \times f_{DAC}$. For a complex output in X2 mode, the spurious signal always is offset $f_{DAC}/2$ from the wanted signal at $f_{SIG} - f_{DAC}/2$. For a real output, as f_{SIG} approaches $f_{DAC}/4$, the spurious signal frequency falls at $f_{DAC}/2 - f_{SIG}$, which also approaches $f_{DAC}/4$.

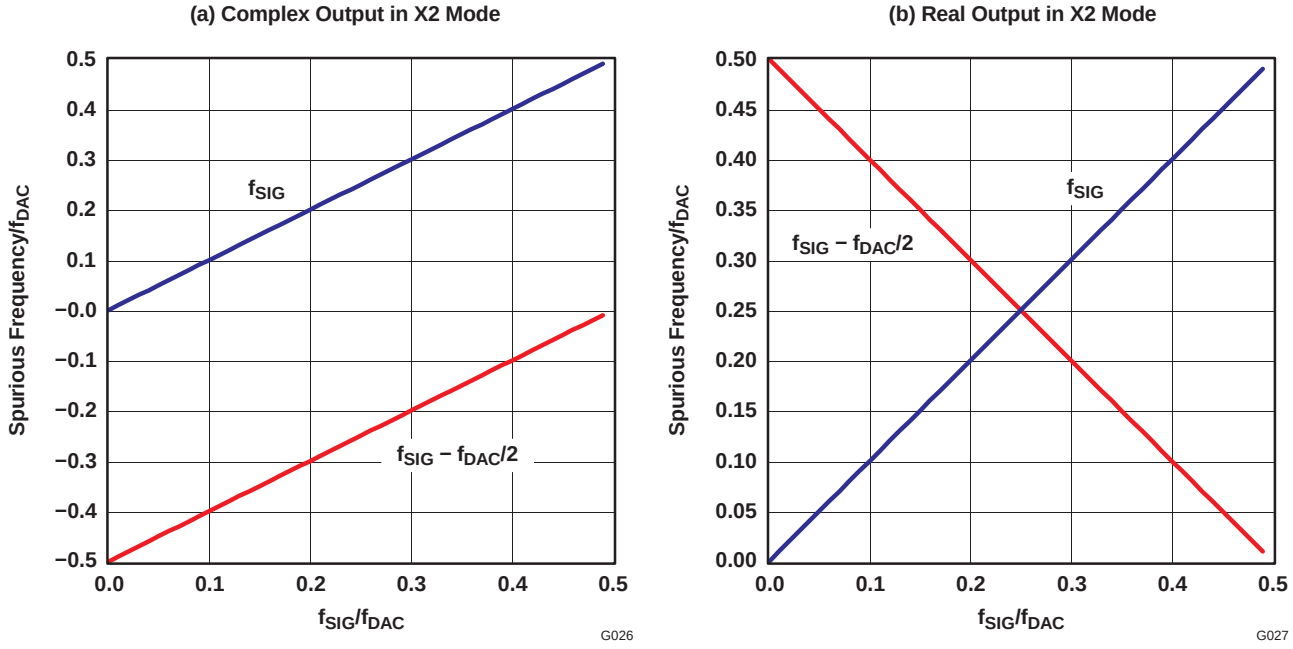


Figure 70. Frequency of Clock Mixing Spurious Images in X2 Mode

Figure 71 shows the location of spurious signals for X4 and X4L mode as a function of f_{SIG}/f_{DAC}. The addition of the $f_{DAC}/4$ clock frequency for the first interpolation filter creates three new spurious signals. For a complex output, the nearest spurious signals are $f_{DAC}/4$ offset from f_{SIG}. For a real output, the signal due to $f_{SIG} - f_{DAC}/4$ and $f_{SIG} - f_{DAC} \times 3/4$ falls in band as f_{SIG} approaches $f_{DAC}/8$ and $f_{DAC} \times 3/8$. This creates optimum real output frequencies $f_{SIG} = f_{DAC} \times N/16$ (N = 1, 3, 5, and 7), where the minimum spurious product offset from f_{SIG} is $f_{DAC}/8$.

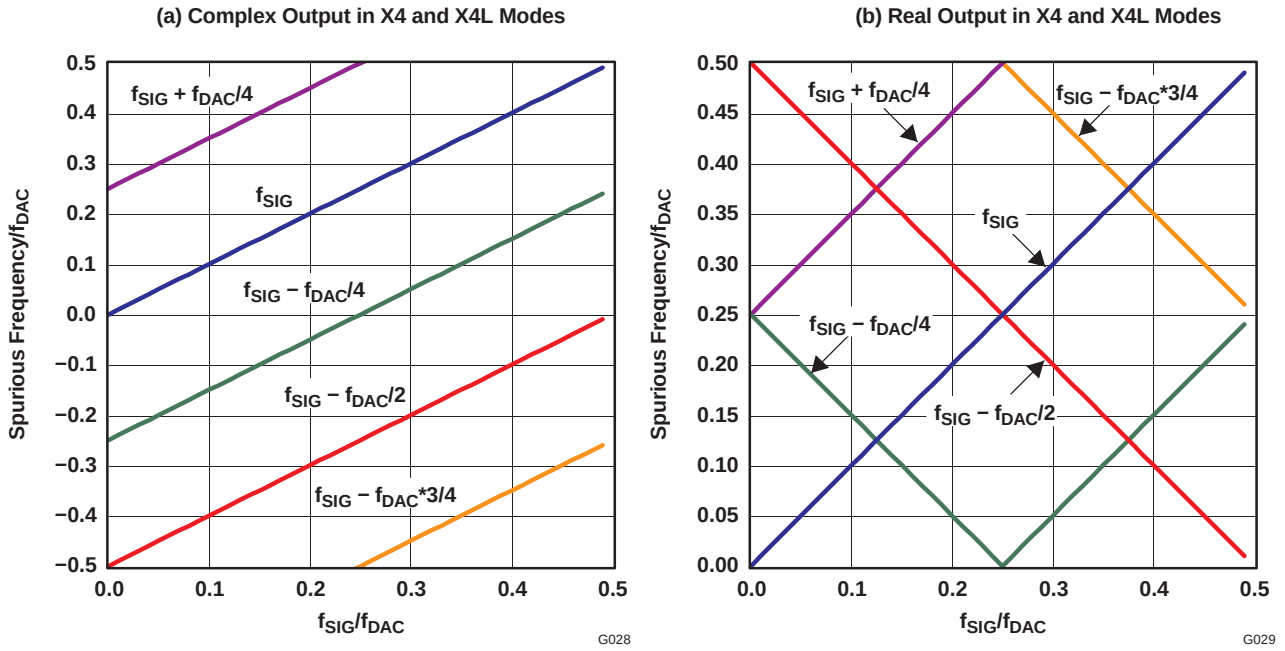


Figure 71. Frequency of Clock Mixing Spurious Images in X4 and X4L Modes

Figure 72 shows the location of spurious signals for X8 mode as a function of f_{SIG}/f_{DAC}. The addition of the $f_{DAC}/8$ clock frequency for the first interpolation filter creates four new spurious signals. For a complex output, the nearest spurious signals are $f_{DAC}/8$ offset from f_{SIG}. For a real output, the optimum real output frequencies $f_{SIG} = f_{DAC} \times N/16$ (N = 3 and 5), where the minimum spurious product offset from f_{SIG} is $f_{DAC}/8$.

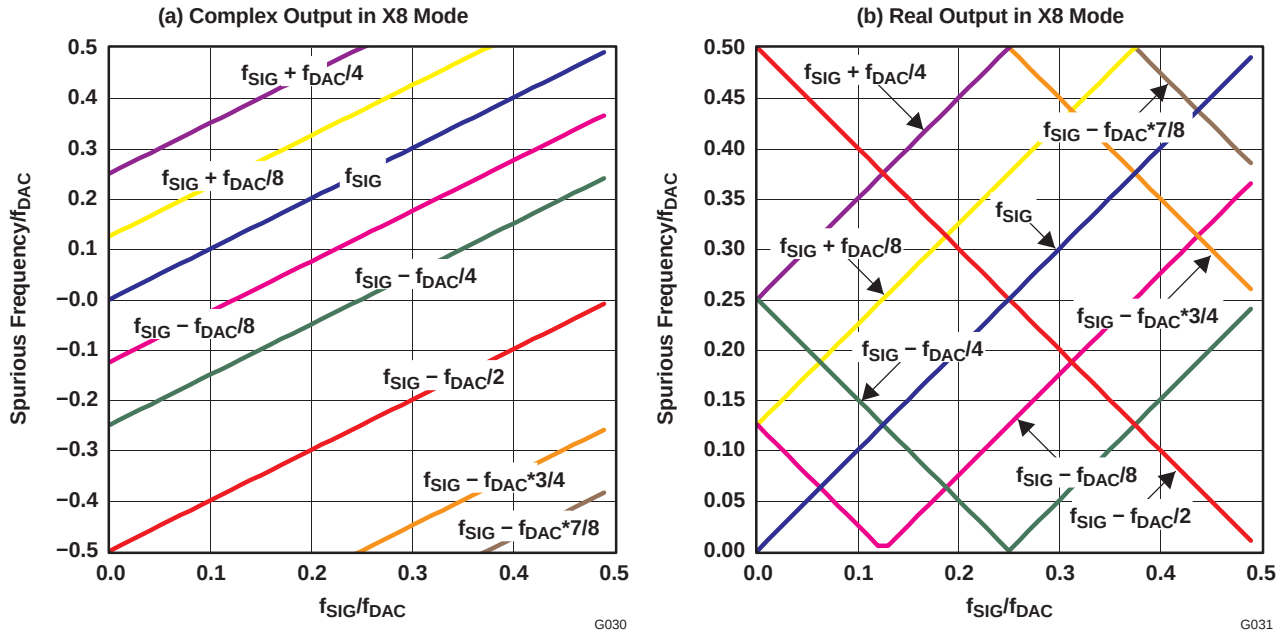


Figure 72. Frequency of Clock Mixing Spurious Images in X8 Mode

Amplitude of the Spurious Signals

The spurious signal amplitude is sensitive to factors such as temperature, voltage, and process. The following typical worst-case estimates to account for the variation over these factors are provided as design guidelines.

Figure 73 and Figure 74 show the typical worst-case spurious signal amplitudes vs f_{DAC} for a signal frequency $f_{SIG} = 11 \times f_{DAC}/32$ in each mode for PLL on (PLL clock mode) and PLL off (external and dual-clock modes). Each spurious signal ($f_{DAC}/2$, $f_{DAC}/4$ and $f_{DAC}/8$) has its own curve. The spurious signal amplitudes can then be adjusted for the exact signal frequency f_{SIG} by applying the amplitude adjustment factor shown in Figure 75. The amplitude adjustment factor is the same for each spurious signal ($f_{DAC}/2$, $f_{DAC}/4$, and $f_{DAC}/8$) and is normalized for $f_{SIG} = 11 \times f_{DAC}/32$.

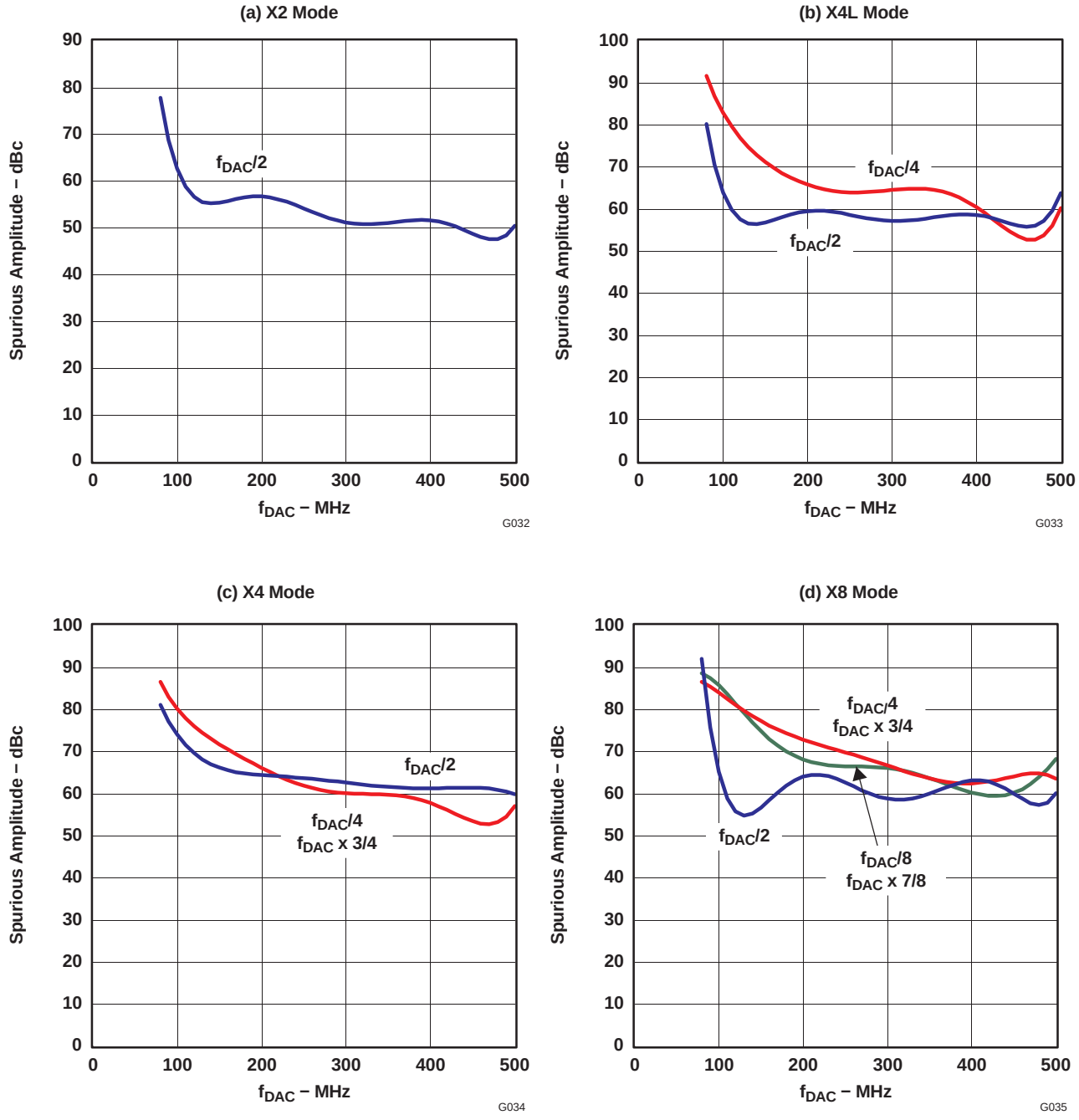


Figure 73. Clock-Related Spurious Signal Amplitude With PLL Off for $f_{SIG} = 11 \times f_{DAC} / 32$

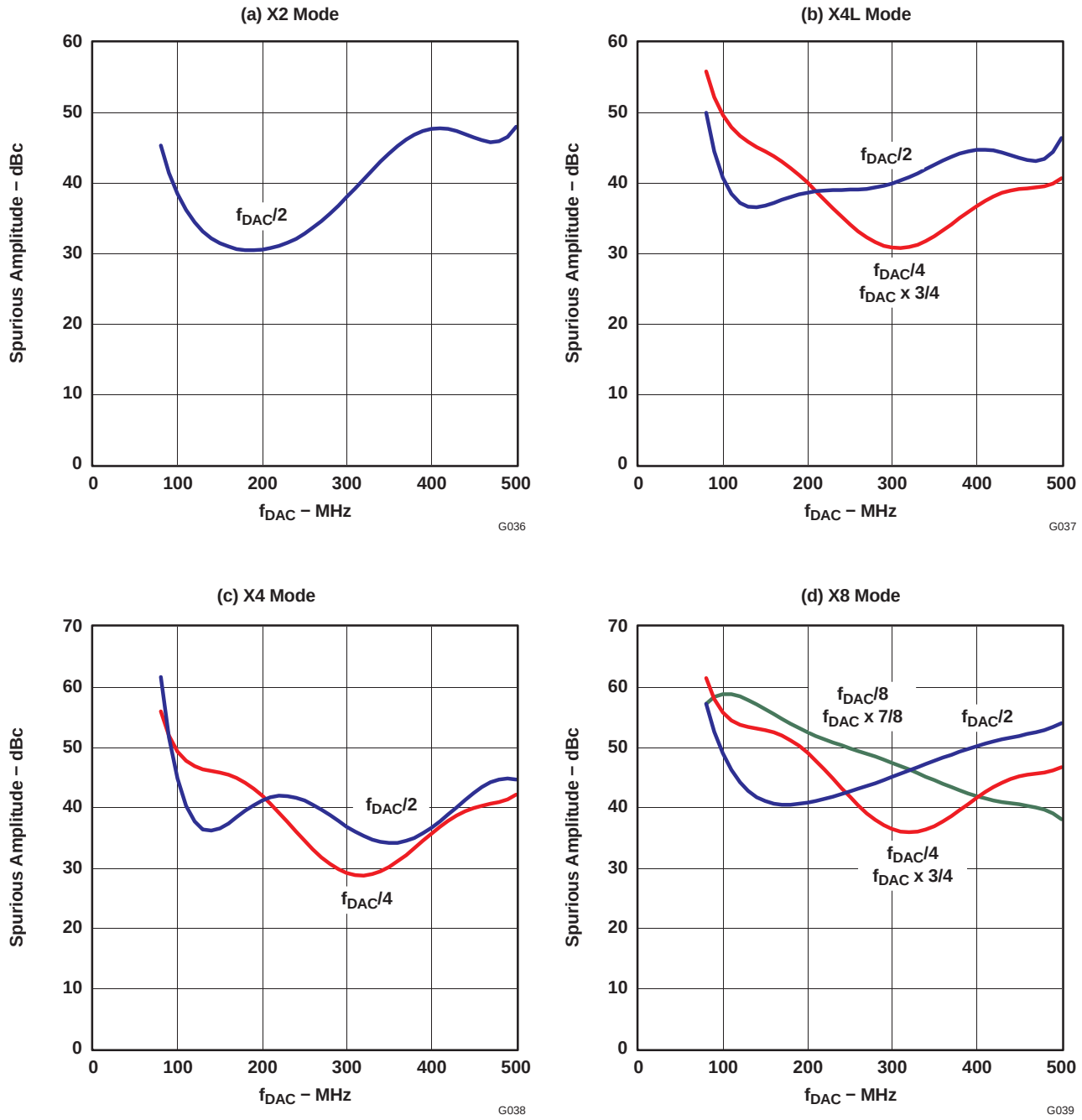


Figure 74. Clock-Related Spurious Signal Amplitude With PLL On for $f_{SIG} = 11 \times f_{DAC} / 32$

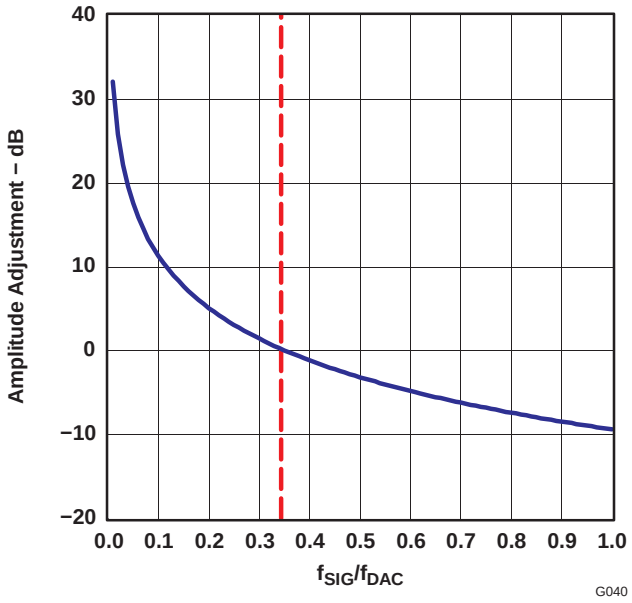


Figure 75. Amplitude Adjustment Factor for f_{SIG}

The steps for calculating the nonharmonic spurious signals are:

1. Find the spurious signal frequencies for the appropriate mode from Figure 70, Figure 71, or Figure 72.
2. Find the amplitude for each spurious frequency for the appropriate mode from Figure 73 or Figure 74.
3. Adjust the amplitude of the spurious signals for f_{SIG} using the adjustment factor in Figure 75.

Consider Example 1 with the following conditions:

1. X4 Mode
2. PLL off
3. Complex output
4. f_{DAC} = 500 MHz
5. f_{SIG} = 160 MHz = 0.32 × f_{DAC}

First, the location of the spurious signals is found for the X4 complex output in Figure 71(a). Three spurious signals are present in the range –0.5 × f_{DAC} to 0.5 × f_{DAC}: two from f_{DAC}/4 (35 MHz and –215 MHz) and one from f_{DAC}/2 (–90 MHz). Consulting Figure 73(c), the raw amplitudes for f_{DAC}/2 and f_{DAC}/4 are 60 and 58 dBc, respectively. From Figure 75, the amplitude adjustment factor for f_{SIG} = 0.32 × f_{DAC} is estimated at ~1 dB, and so the f_{DAC}/2 and f_{DAC}/4 are adjusted to 61 and 59 dBc.

Table 16. Example # 1 for Calculating Spurious Signals

Spurious Signal	Frequency/f_{DAC}	Frequency (MHz)	Raw Amplitude (dBc)	Adjusted Amplitude (dBc)
f_{DAC}/4	0.07	35	58	59
f_{DAC}/2	–0.18	–90	60	61
f_{DAC}/4	–0.43	–215	58	59

Now consider Example 2 with the following conditions:

1. X2 Mode
2. PLL on
3. Real output
4. f_{DAC} = 400 MHz
5. f_{SIG} = 70 MHz = 0.175 × f_{DAC}

First, the location of the spurious signal is found for the X2 real output in Figure 70(b). One spurious signal is present in the range 0 to 0.5 × f_{DAC} at 0.325 × f_{DAC} (see Table 17). Consulting Figure 74(a), the raw amplitude for f_{DAC}/2 is 47 dBc. From Figure 75, the amplitude adjustment factor for f_{SIG} = 0.175 × f_{DAC} is estimated at ~6 dB, and so the f_{DAC}/2 spurious signal is adjusted to 53 dBc.

Table 17. Example # 2 for Calculating Spurious Signals

Spurious Signal	Frequency/f_{DAC}	Frequency (MHz)	Raw Amplitude (dBc)	Adjusted Amplitude (dBc)
f_{DAC}/2	0.325	130	47	53

Schematic and Layout Recommendations

The DAC5687 clock is sensitive to fast transitions of input data on pins DA0, DA1, and DA2 (55, 54, and 53) due to coupling to DVDD pin 56. The noise-like spectral energy of the DA[2:0] couples into the DAC clock resulting in increased jitter. This significantly improves by using a 10-Ω resistor between DVDD and pin 56 in addition to 10-pF capacitor to DGND, as implemented on the DAC5687EVM (see the DAC5687 EVM user's guide, SLWU017). Pin 56 draws only approximately 2 mA of current and the 0.02-V voltage drop across the resistor is acceptable for DVDD voltages within the MINIMUM and MAXIMUM specifications. It is also recommended that the transition rate of the input lines be slowed by inserting series resistors near the data source. The optimized value of the series resistor depends on the capacitance of the trace between the series resistor and DAC5687 input pin. For a 2–3-inch trace, a 22-Ω to 47-Ω resistor is recommended.

The effect of DAC clock jitter on the DAC output signal is worse for signals at higher signal frequencies. For low IF (< 75 MHz) or baseband signals, there is little degradation of the output signal. However, for high IF (> 75 MHz) the DAC clock jitter may result in an elevated noise floor, which often appears as broad humps in the DAC output spectrum. It is recommended for signals above 75 MHz that the inputs to DA0 and DA1, which are the two LSBs if input DA[15:0] is not reversed, not be connected to input data to prevent coupling to the DAC rate clock. The decrease in resolution to 14 bits and increase in quantization noise does not significantly affect the DAC5687 SNR for signals > 75 MHz.

Application Examples

Application Example: Real IF Radio

An system example of the DAC5687 used for a flexible real IF radio is shown in Figure 76. A complex baseband input to the DAC would be generated by a digital upconverter such as Texas Instruments GC4116, GC5016, or GC5316. The DAC5687 would be used to increase the data rate through interpolation and flexibly place the output signal using the FMIX and/or CMIX blocks. Although the DAC5687 X4 mode is shown, any of the modes (X2, X4L, or X8) would be appropriate.

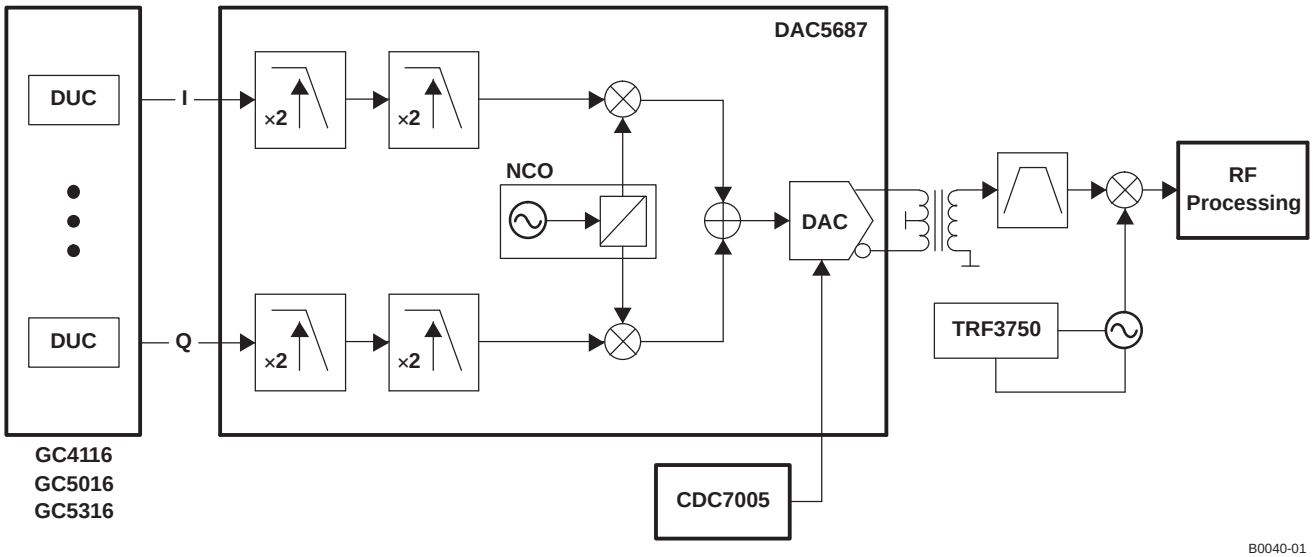


Figure 76. System Diagram of a Real IF System Using the DAC5687

With the DAC5687 in external clock mode, a low-phase-noise clock for the DAC5687 at the DAC sample rate would be generated by a VCXO and PLL such as Texas Instruments CDC7005, which can also provide other system clocks at the VCXO frequency divided by 2^{-n} (n = 0 to 4). In this mode, the DAC5687 PLLLOCK pin output would typically be used to clock the digital upconverter. With the DAC in PLL clock mode, the same input rate clock would be used for the DAC clock and digital upconverter and the DAC internal PLL/VCO would generate the DAC sample rate clock. Note that the internal PLL/VCO phase noise may degrade the quality of the DAC output signal, and also has higher nonharmonic clock-related spurious signals (see the *Nonharmonic Clock-Related Spurious Signals* section).

Either DACA or DACB outputs can be used (with the other DAC put into sleep mode) and would typically be terminated with a transformer (see the *Analog Current Outputs* section). An IF filter, either LC or SAW, is used to suppress the DAC Nyquist zone images and other spurious signals before being mixed to RF with a mixer.

An alternative architecture uses the DAC5687 in a dual-channel mode to create a dual-channel system with real IF input and output. This would be used for narrower signal bandwidth and at the expense of less output frequency placement flexibility (see Figure 77). Frequency upconversion can be accomplished by using the high-pass filter and CMIX $f_{DAC}/2$ mixing features.

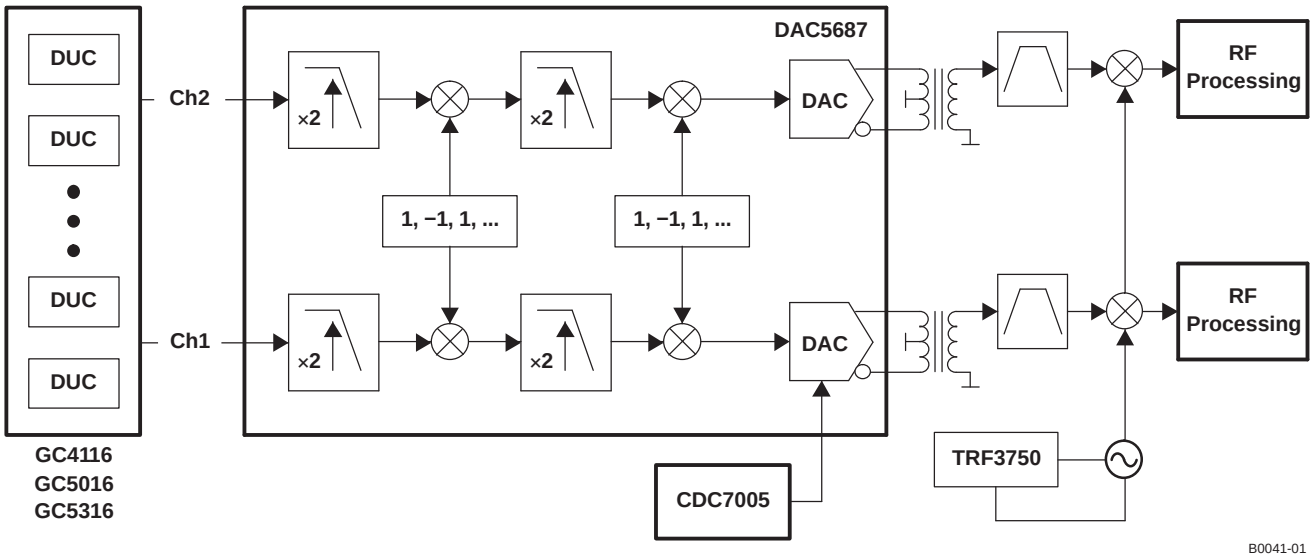


Figure 77. System Diagram of a Dual-Channel Real IF Radio

The outputs of multiple DAC5687s can be phase synchronized for multiple antenna/beamforming applications.

Application Example: Complex IF to RF Conversion Radio

An alternative to a real IF system is to use a complex IF DAC output with analog quadrature modulator, as shown in Figure 78. The same complex baseband input as the real IF system in Figure 76 is used. The DAC5687 would be used to increase the data rate through interpolation and flexibly place the output signal using the FMIX and/or CMIX blocks. Although the DAC5687 X4 mode is shown, any of the modes (X2, X4L, or X8) would be appropriate.

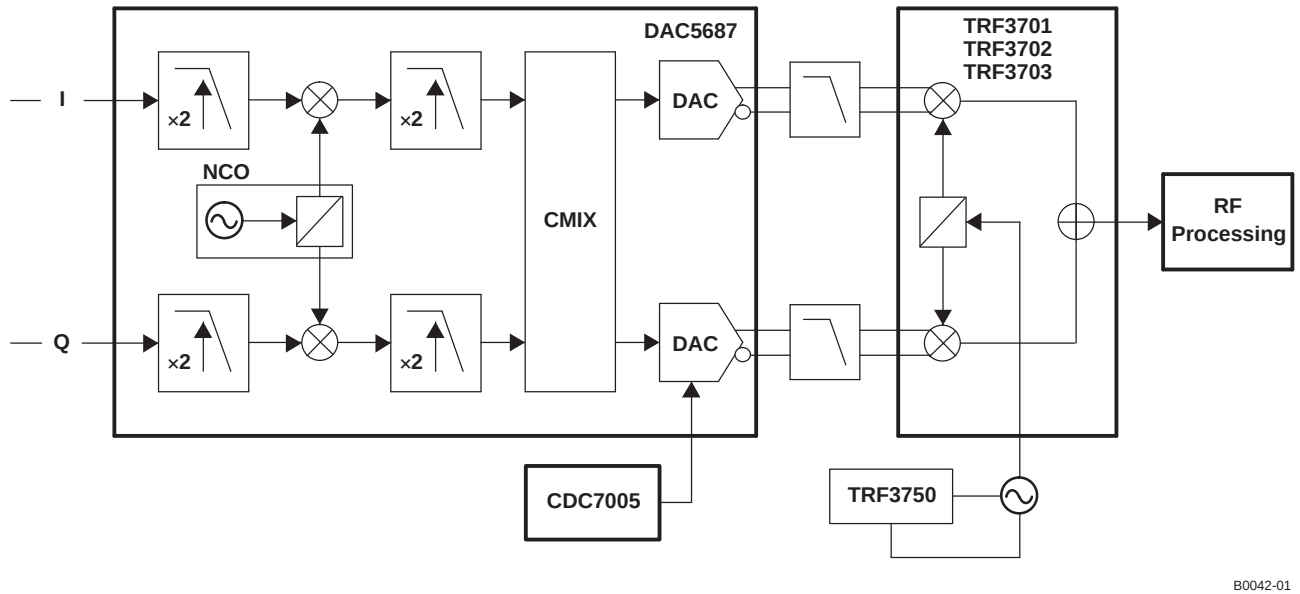


Figure 78. Complex IF System Using the DAC5687 in X4L Mode

Instead of only using one DAC5687 output as for the real IF output, both DAC5687 outputs are used for a complex IF Hilbert transform pair.

The DAC5687 outputs can be expressed as:

$$A(t) = I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t) = m(t)$$

$$B(t) = I(t)\sin(\omega_c t) + Q(t)\cos(\omega_c t) = m_h(t)$$

where m(t) and $m_h(t)$ connote a Hilbert transform pair and ωc is the sum of the NCO and CMIX frequencies.

The complex DAC5687 output is input to an analog quadrature modulator (AQM) such as the TRF3701 or TRF3702. A passive (resistor-only) interface is recommended between the DAC5687 and TRF3701/2 (See the Passive Interface to TRF3701/2 section). Upper single-sideband upconversion is achieved at the output of the analog quadrature modulator, whose output is expressed as:

$$RF(t) = I(t)\cos(\omega_c + \omega_{LO})t - Q(t)\sin(\omega_c + \omega_{LO})t$$

Flexibility is provided to the user by allowing for the selection of –B(t) out, which results in lower-sideband upconversion. This option is selected by usb in the CONFIG3 register.

Note that the process of complex mixing in FMIX and CMIX to translate the signal frequency from 0 Hz means that the analog quadrature modulator IQ imbalance produces a sideband and LO feedthrough that falls outside the signal.

This is shown in Figure 79, which is the RF analog quadrature modulator (AQM) output of an asymmetric three-carrier WCDMA signal with the properties in Table 18. The wanted signal is offset from the LO frequency by the DAC5687 complex IF, in this case 122.88 MHz. The nearest spurious signals are ~100 MHz away from the wanted signal (due to nonharmonic clock-related spurious signals generated by the $f_{DAC}/4$ digital clock), providing 200 MHz of spurious-free bandwidth. The AQM phase and gain imbalance produce a lower-sideband product, which does not affect the quality of the wanted signal. Unlike the real IF architecture, the nonharmonic clock-related spurious signals generated by the $f_{DAC}/2$ digital clock fall ±245.76-MHz offset from the wanted, rather than falling in-band.

As a consequence, in the complex IF system it may be possible that no AQM phase, gain and offset correction is needed, instead relying on RF filtering to remove the LO feedthrough, sideband, and other spurious products.

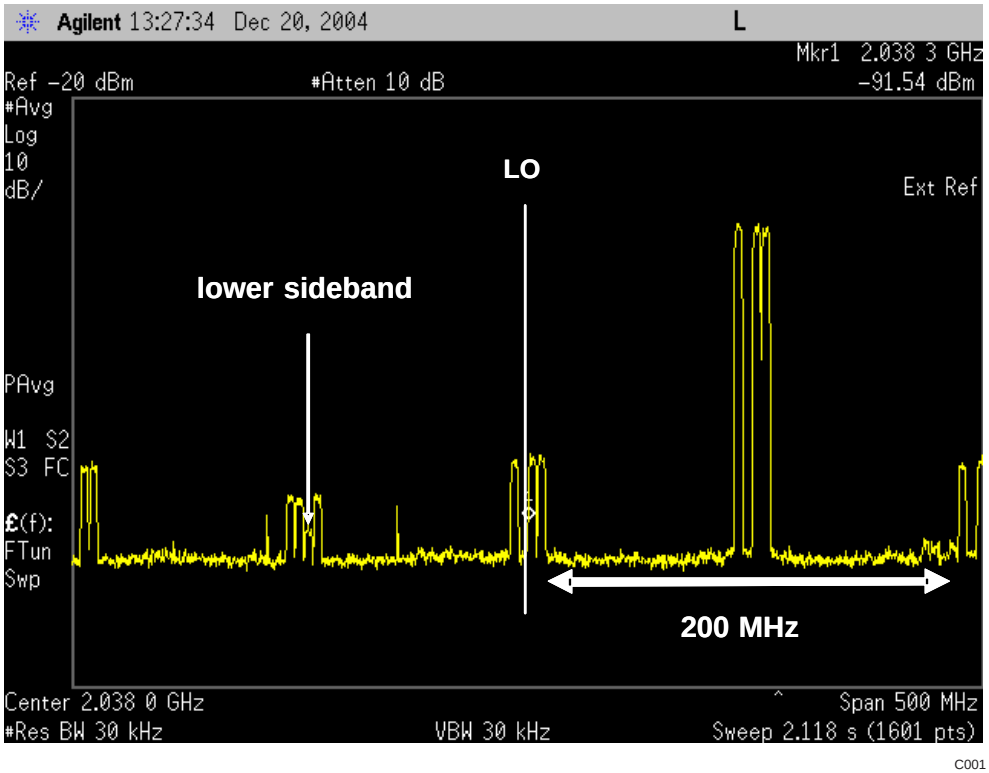


Figure 79. Analog Quadrature Modulator Output for a Complex IF System

Table 18. Signal and System Properties for Complex IF System Example in Figure 79

Signal	Three WCDMA carriers, test model 1
Baseband carrier offsets	–7.5 MHz, 2.5 MHz, 7.5 MHz
DAC5687 input rate	122.88 MSPS
DAC5687 output rate	491.52 MSPS (4× interpolation)
DAC5687 mode	X4 CMIX
DAC5687 complex IF	122.88 MHz (f_{DAC}/4)
LO frequency	2140 MHz

The complex IF has several advantages over the real IF architecture such as:

- Uncalibrated sideband suppression, ~35 dBc compared to 0 dBc for real IF architecture.
- Direct DAC–complex-mixer connection—no amplifiers
- Nonharmonic clock-related spurious signals fall out-of-band
- DAC second Nyquist zone image is offset f_{DAC} compared with $f_{DAC} – 2 \times$ IF for a real IF architecture, reducing the need for filtering at the DAC output.
- Uncalibrated LO feedthrough for AQM is ~35 dBc and calibration can reduce or completely remove the LO feedthrough.

Application Example: Wide-Bandwidth Direct Baseband-to-RF Conversion

A system example of the DAC5687 used in a wide-bandwidth direct baseband-to-RF conversion is shown in Figure 80. The DAC input would typically be generated by a crest factor reduction processor such as Texas Instruments GC1115 and digital predistortion processor. With a complex baseband input, the DAC5687 would be used to increase the data rate through interpolation. In addition, phase, gain, and offset correction of the IQ imbalance is possible using the QMC block, DAC gain, and DAC offset features. The correction could be done one time during manufacturing (see the TRF3701 data sheet (SLWS145) and the TRF3702 data sheet (SLWS149) for the variation with temperature, supply, LO frequency, etc., after calibration at nominal conditions) or during operation with a separate feedback loop measuring imbalance in the RF signal.

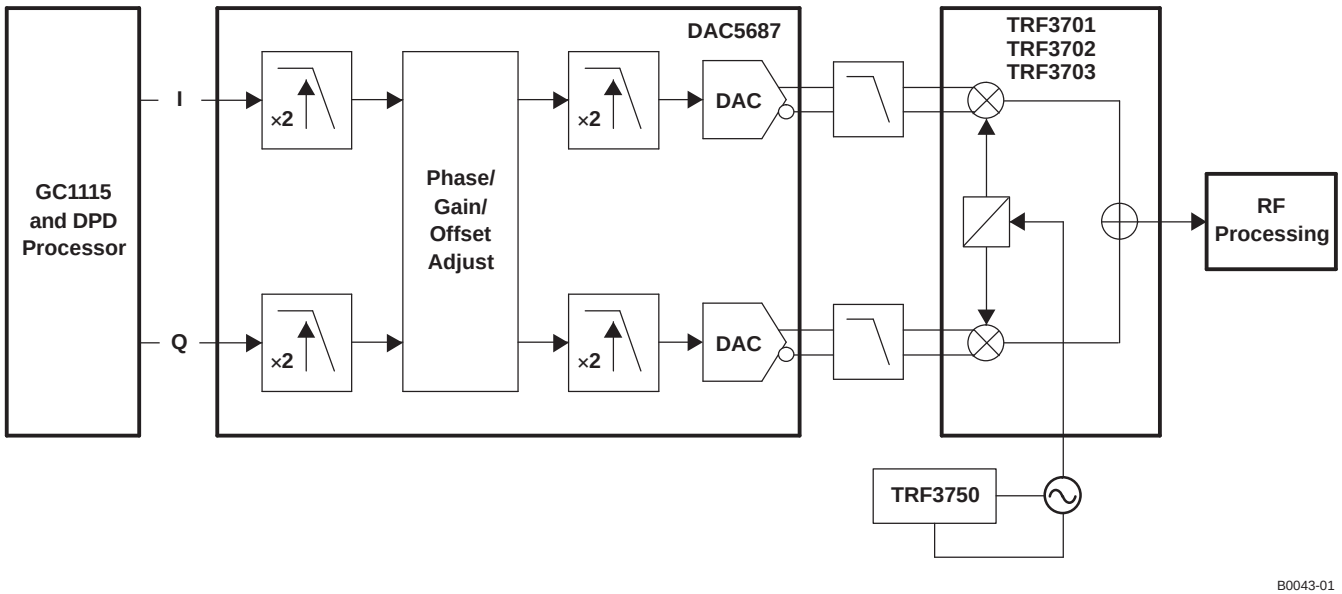


Figure 80. Direct Conversion System Using DAC5687 in X4L Mode

Operating at baseband has the advantage that the DAC5687 output is insensitive to DAC sample clock phase noise, so using the DAC PLL clock mode has similar spectral performance to the external clock mode. In addition, the nonharmonic clock-related spurious signals are small due to the low DAC output frequency.

With a complex input rate specified up to 250 MSPS, the DAC5687 is capable of producing signals with up to 200-MHz bandwidth for systems such as digital predistortion (DPD).

Application Example: CMTS/VOD Transmitter

The exceptional SNR of the DAC5687 enables a dual-cable modem termination system (CMTS) or video on demand (VOD) QAM transmitter in excess of the stringent DOCSIS specification, with > 74 dBc and 75 dBc in the adjacent and alternate channels.

A typical system using the DAC5687 for a cost-optimized dual-channel two-QAM transmitter is shown in Figure 81. A GC5016 would take four separate symbol rate inputs and provide pulse shaping and interpolation to ~128 MSPS. The four QAM carriers would be combined into two groups of two QAM carriers with intermediate frequencies of approximately 30 MHz to 40 MHz. The GC5016 would output two real data streams to one DAC5687. The DAC5687 would function as a dual-channel device and provide 2× interpolation to increase the frequency of the second Nyquist zone image. The two signals are then output through the two DAC outputs, through a transformer and to an RF upconverter.

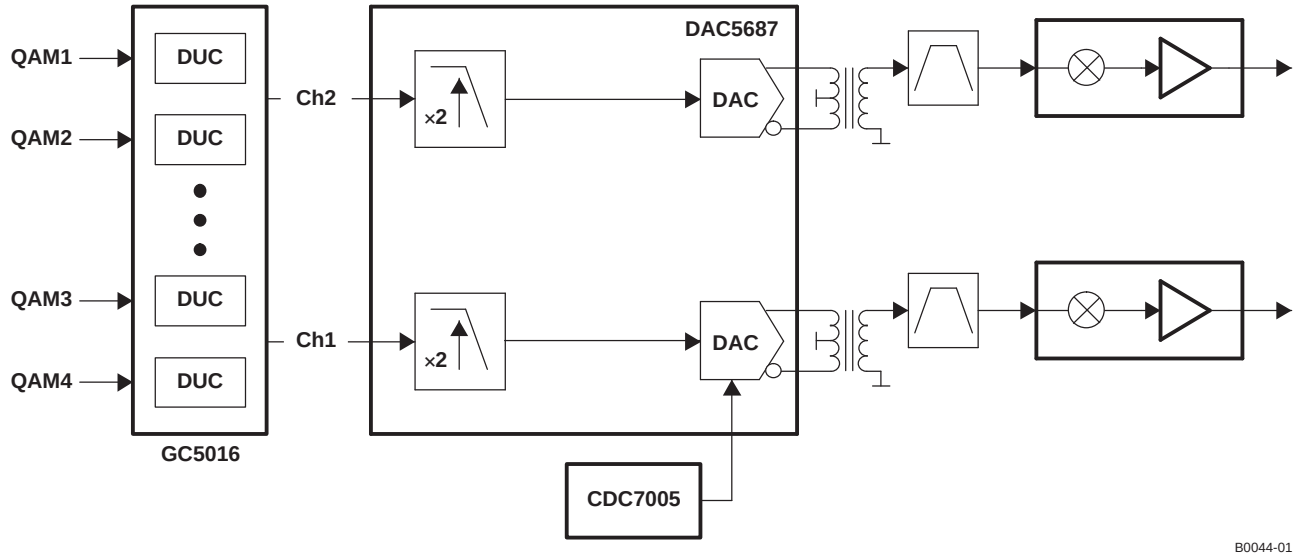


Figure 81. Dual-Channel Two-QAM CMTS Transmitter System Using DAC5687

The DAC5687 output for a two-QAM256 carrier signal at 33-MHz and 39-MHz IF with the signal and system properties listed in Table 19 is shown in Figure 82. The low DAC5687 noise floor provides better than 75 dBc (equal bandwidth normalized to one QAM256 power) at > 6-MHz offset.

Table 19. Signal and System Properties for Complex IF System Example in Figure 82

Signal	QAM256, 5.36 MSPS, α = 0.12
IF frequencies	33 MHz and 39 MHz
DAC5687 input rate	5.36 MSPS × 24 = 128.64 MSPS
DAC5687 output rate	257.28 MSPS (2× interpolation)
DAC5687 mode	X2

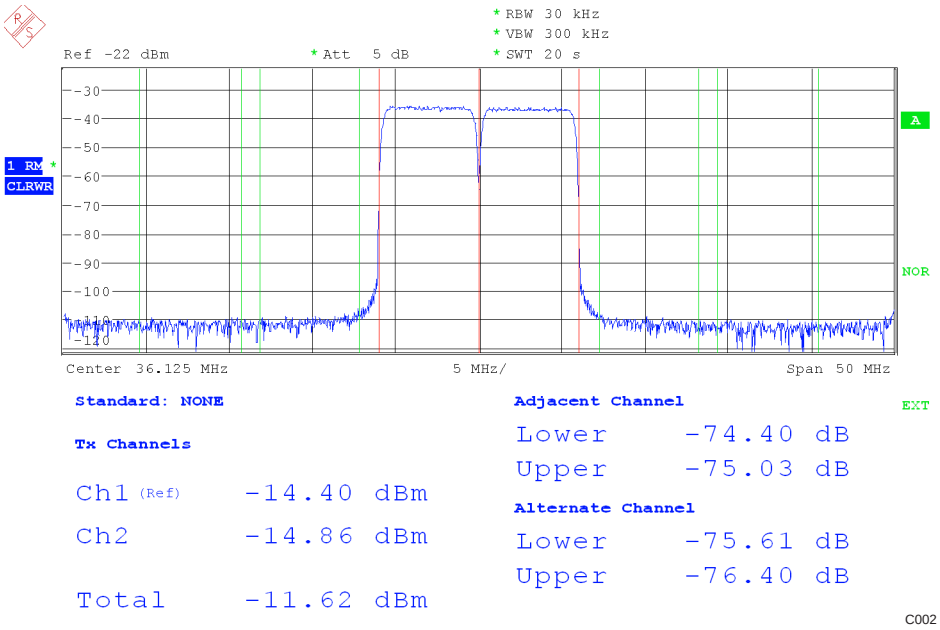


Figure 82. Two QAM256 Carriers With 36-MHz IF

Application Example: High-Speed Arbitrary Waveform Generator

The DAC5687 flexible input allows use of the dual input ports with demultiplexed odd/even samples at a combined rate of up to 500 MSPS. Combined with the DAC 16-bit resolution, the DAC5687 allows wideband signal generation for test and measurement applications.

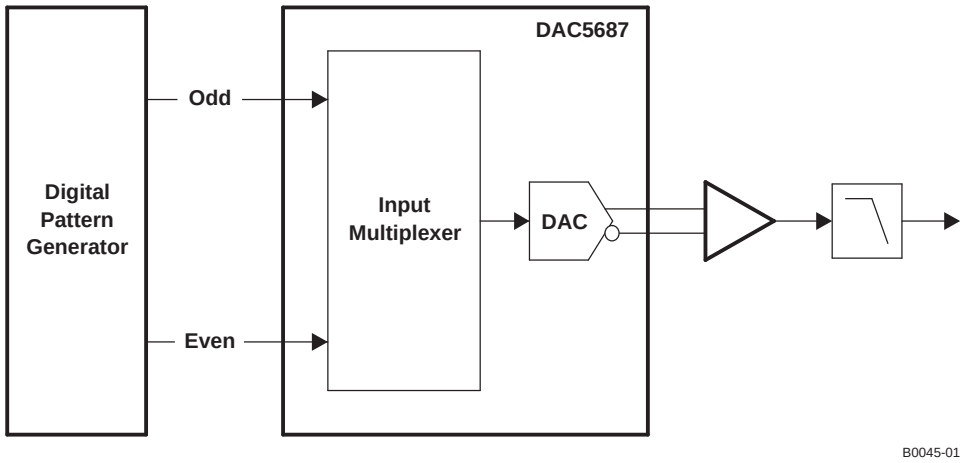


Figure 83. DAC5687 in Odd/Even Input Mode

Changes from Revision D (July 2006) to Revision E

Page

- Inverted CLK2 waveform in Figure 50 timing diagram 44
- Deleted $\Delta < t_{align}$ from Figure 51 timing diagram..... 44

Changes from Revision C (April 2006) to Revision D

Page

- For pins 34 and 92 in pinout diagram, changed "MSB" to "MSB or LSB," and for pins 55 and 71 changed "LSB" to "LSB or MSB," to reflect option of bus reversal. 3
- Added V_{IH} and V_{IL} specifications for IOVDD = 1.8 V 9
- In register CONFIG3, added sentence to counter_mode(2:0) description indicating that counter mode replaces digital signal with a counter signal 27
- In register NCO_FREQ_2, changed address to 0x0B..... 28
- In register NCO_FREQ_3, changed address to 0x0C..... 28
- In register DACA_DACB_GAIN_1, added daca_gain(11:8) to description 30
- In the description of instruction bytes N1 and N0, added description of multibyte transfers..... 32
- For FIR filters, corrected description (color and type) of lines in Figure 38..... 34
- Changed "... FMIX + f_{DAC}/2" to "FMIX + CMIX with f_{DAC}/2" 36
- Changed f_{DAC} to f_{NCO} in Figure 39..... 36
- To DAC Offset Control section, appended description of the transition between offset values during four DAC clock cycles (two paragraphs and Table 11)..... 39
- Added sentence in external clock mode description explaining that the PLLLOCK output should not be used above 100 MHz for IOVDD = 1.8 V 41
- In dual clock mode equation, changed "f_{align}" to "t_{align}"..... 43
- Appended paragraph to Interleave Bus Mode section describing issues with synchronization in PLL mode with interleaved data 45
- First sentence of Input FIFO section, changed "DAC clock mode" to "external clock mode" 45
- Changed second "=" in equation to a "–"..... 52
- Changed "The external output resistors are referred to an external ground." to "The external output resistors are referred to AVDD." 52
- Changed "Exceeding the output compliance voltage..." to "Exceeding the minimum output compliance voltage..."..... 52
- Changed "does not exceed 0.5 V" to "is in the range of AVDD ±0.5 V."..... 52
- Appended sentence, "The pullup and pulldown circuitry is approximately equivalent to 100 kΩ." 55
- Changed caption of Figure 65 56
- Changed "...it is suggested that ω_d be set... to "...it is suggested that ϕ_d be set..."..... 57
- In last sentence of paragraph, changed "1.56-V_{PP} differential" to "1.52-V_{PP} differential" 58
- Changed example of an interface to a 1.5-V common-mode device to an interface to a 3.3-V common mode for TRF3703-33..... 59
- In Table 16, changed value in top row of Frequency/f_{DAC} column from 0.7 to 0.07 64
- In text for example #2, changed "...f_{DAC}/2 and f_{DAC}/4 signal is adjusted..." to "...f_{DAC}/2 spurious signal is adjusted..." 65
- Changed referenced figure number to Figure 82 70

Changes from Revision B (June 2005) to Revision C **Page**

- First sentence: Changed "The lower limit" to "upper limit". 3rd sentence: "upper limit" to "lower limit". Last sentence: "Exceeding the upper limit" to "Exceeding the limits". 6
- Noise Floor Test Conditions: Swapped "CLK1 = 122.88 MHz" and "CLK2 = 491.52 MHz" for all four lines 9
- Input data rate, External or dual-clock modes, minimum changed to 0 Hz 9
- Input data rate, PLL clock mode, minimum changed to 2.5 MHz 9
- VCO maximum frequency test condition, "pll_kv = 0" changed to "pll_kv = 1" and vice versa 10
- VCO minimum frequency test condition, "pll_kv = 0" changed to "pll_kv = 1" and vice versa 10
- Figure 26 – "16702A Pattern Generator Card" changed to "16720A Pattern Generator Card" 18
- Figure 27 – "16702A Pattern Generator Card" changed to "16720A Pattern Generator Card" 19
- Figure 45: changed "CLK2" to "CLK1" 42
- Second paragraph of *Analog Current Outputs* reworded 52
- Table 15: "pll_kv = 0" changed to "pll_kv = 1" and vice versa 57
- Figure 72 caption – changed "X4 and X4L" to "X8" 61
- Figure 81 – removed one stage of interpolation from DAC block diagram 70

Changes from Revision A (April 2005) to Revision B **Page**

- Added thermal pad dimensions 1
- Reversed "External Clock Mode" and "PLL Clock Mode" in noise floor test 9
- Changed PLLLOCK Output Signal for PLLVDD = 0 to "Normal Operation" in Table 5 31
- Reversed $t_{s(DATA)}$ and $t_{h(DATA)}$ in Figure 43 41
- Reversed $t_{s(DATA)}$ and $t_{h(DATA)}$ in Figure 44 41
- Reversed $t_{s(DATA)}$ and $t_{h(DATA)}$ in Figure 45 42
- Updated Figure 46 42

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC5687IPZP	Active	Production	HTQFP (PZP) | 100	90 | EIAJ TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5687IPZP
DAC5687IPZP.A	Active	Production	HTQFP (PZP) | 100	90 | EIAJ TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5687IPZP
DAC5687IPZPG4	Active	Production	HTQFP (PZP) | 100	90 | EIAJ TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5687IPZP
DAC5687IPZPR	Active	Production	HTQFP (PZP) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5687IPZP
DAC5687IPZPR.A	Active	Production	HTQFP (PZP) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5687IPZP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DAC5687 :

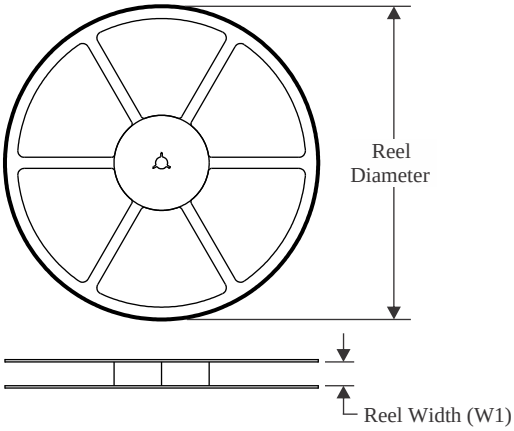
- Enhanced Product : DAC5687-EP

NOTE: Qualified Version Definitions:

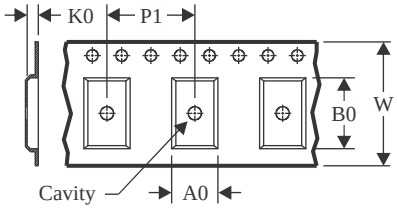
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

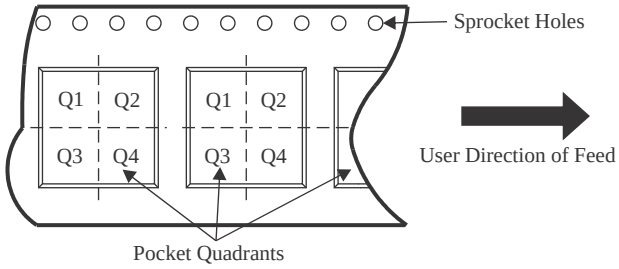


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

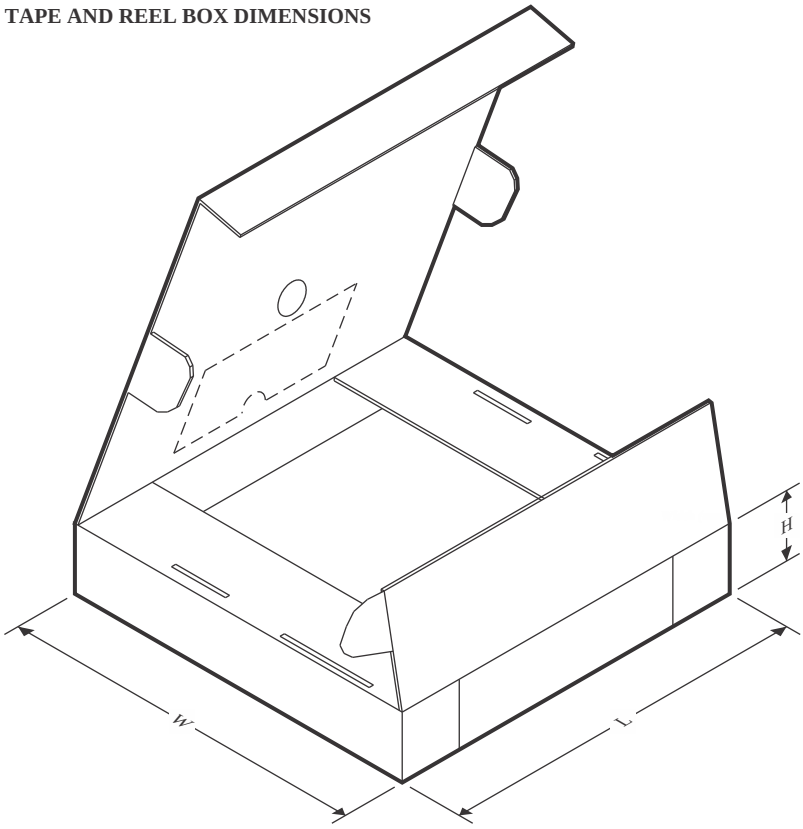
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5687IPZPR	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

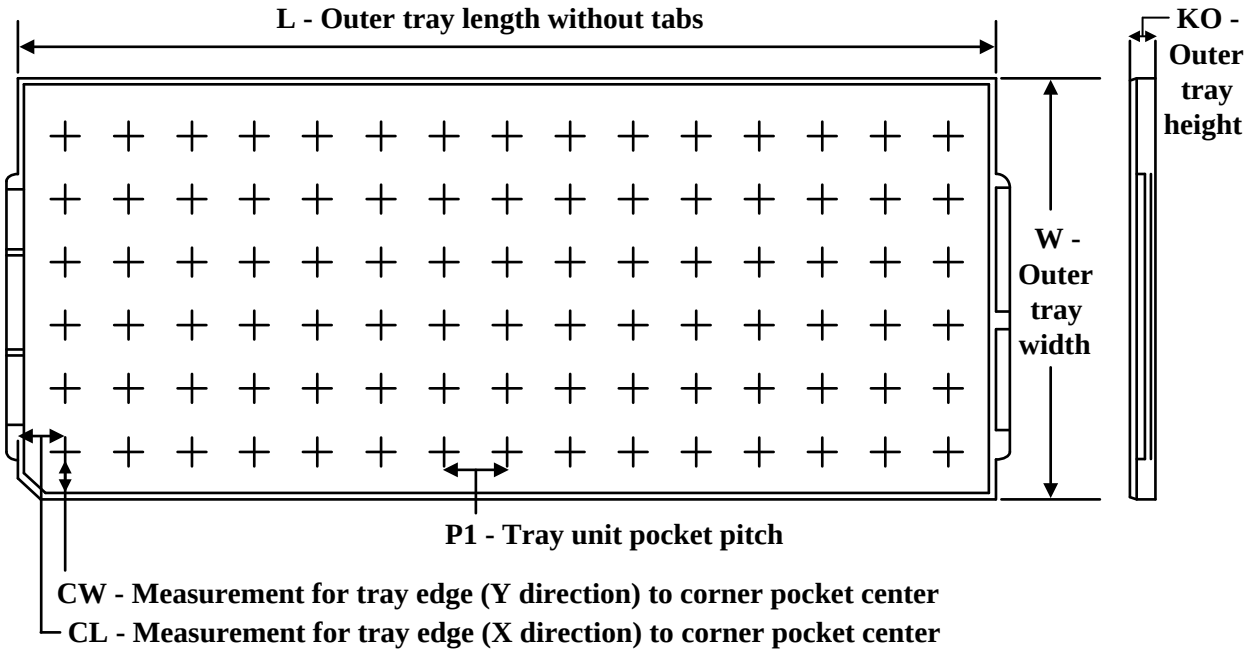
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5687IPZPR	HTQFP	PZP	100	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC5687IPZP	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45
DAC5687IPZP.A	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45
DAC5687IPZPG4	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45

GENERIC PACKAGE VIEW

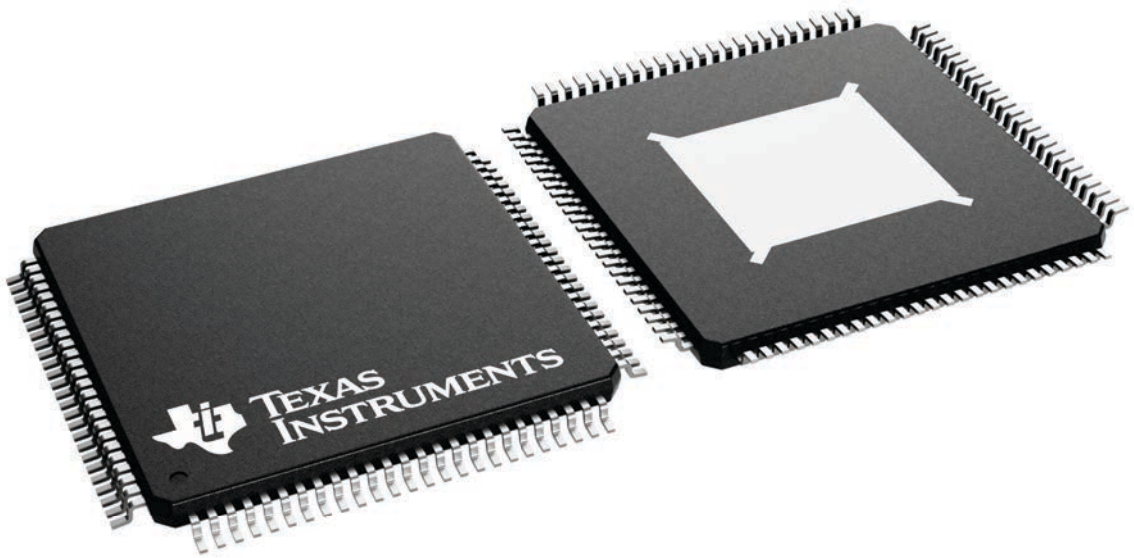
PZP 100

PowerPAD ™ TQFP - 1.2 mm max height

14 x 14 mm Pkg Body, 0.5 mm pitch
16 x 16 mm Pkg Area

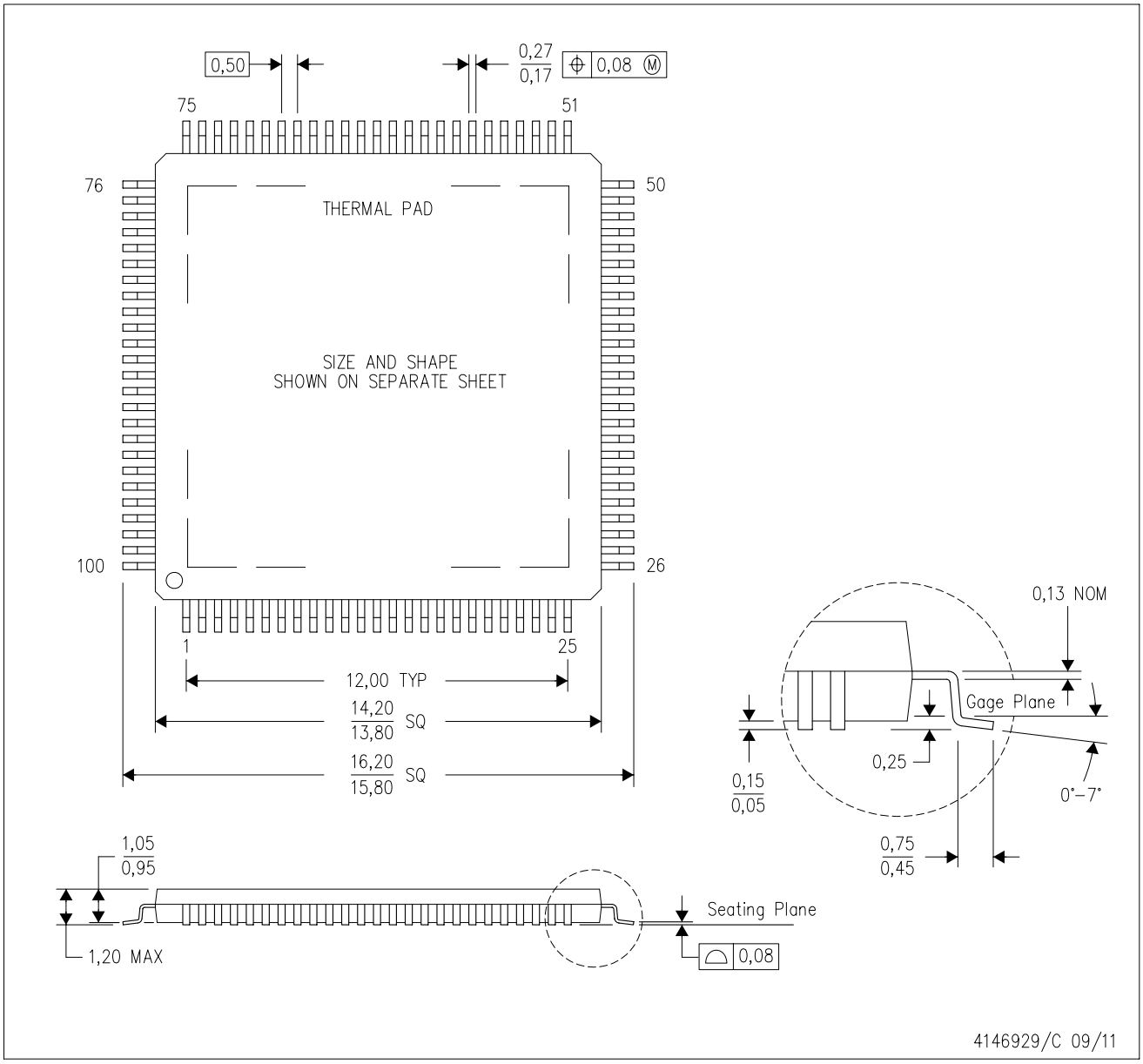
PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224739/B

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

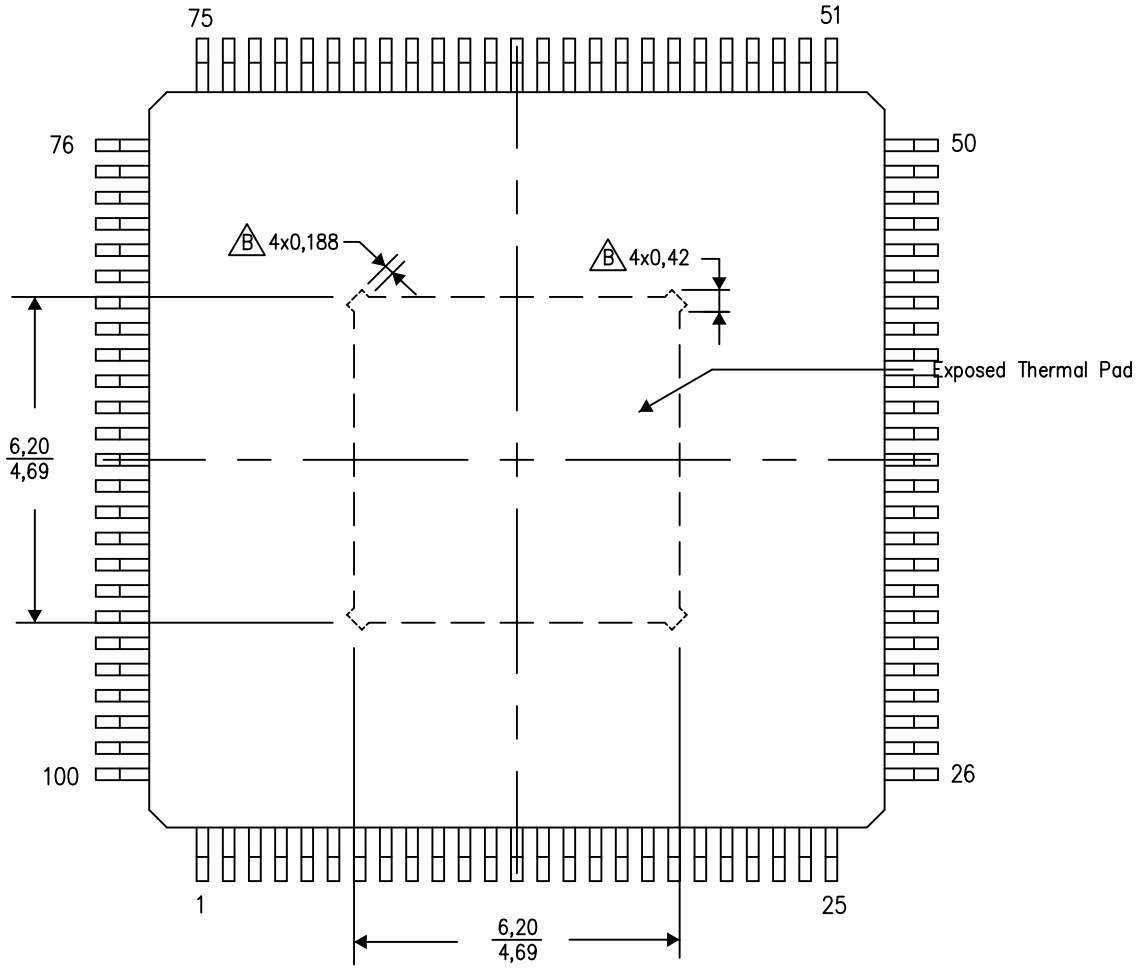
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206333–3/L 05/14

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

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