TEXAS INSTRUMENTS
DAC43508, DAC53508, DAC63508
JAJSLP4A – DECEMBER 2021 – REVISED MAY 2024

DACx3508 オクタル、8 ビット、10 ビット、および 12 ビット、SPI、バッファ付き電圧出力 DAC、 超小型 3 × 3 WQFN パッケージ

1 特長

- ±1LSB DNL
- 広い動作範囲:
  - 電源:1.8V～5.5V
  - 温度範囲:-40℃～+125℃
- 3 線式シリアル ペリフェラル インターフェイス (SPI)
  - 2.7V ≤ V_{DD} ≤ 5.5V の場合、VIH = 2.4V
  - 1.8V ≤ V_{DD} ≤ 2.7V の場合、VIH = (V_{DD} - 0.3V)
- $\overline{LDAC}$ ピンによる出力の同時更新
- 超低消費電力:チャネルあたり 0.1mA (1.8V の場合)
- 低消費電力スタートアップ モード:出力は A_{GND} に接続した 10kΩ でパワーダウンします
- 超小型パッケージ:3mm × 3mm、16 ピン WQFN

2 アプリケーション

- マルチファンクション・プリンタ (プリンタ複合機)
- TV 向けディスプレイ・パネル
- OLED (有機 EL) TV
- バーチャル・リアリティ・ヘッドセット
- 貨幣計数機
- 現金自動預け払い機 (ATM)

3 概要

8 ビット DAC43508、10 ビット DAC53508、12 ビット DAC63508 (DACx3508) は、低消費電力、8 チャネルの電圧出力 D/A コンバータ (DAC) です。DACx3508 は、1.8V～5.5V の広い電源電圧範囲にわたって単調性を維持するように設計されています。DACx3508 は外部基準電圧を使用することで、各チャネルごとに 0.1mA 静止電流を消費する、フルスケール 1.8V～5.5V の出力電圧範囲を提供します。また、DACx3508 には、チャネルごとにユーザーがプログラム可能なパワーダウン レジスタも内蔵しています。これらのレジスタにより、DAC 出力バッファは起動時は 10KΩ-AGND パワーダウン状態にされ、これらの出力バッファにパワーアップ コマンドが発行されるまで、この状態を維持します。

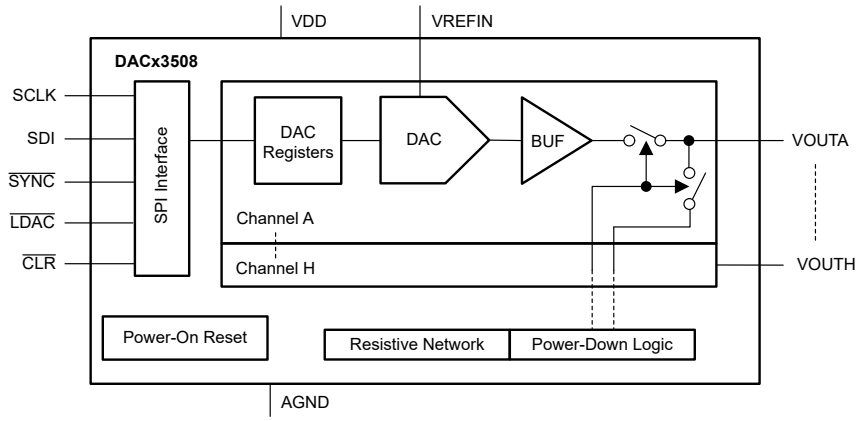
低静止電流、広い電源電圧範囲、8 チャネル、チャネルあたりのパワーダウン オプションから、DACx3508 は高密度、低消費電力のバッテリ駆動システムに最適です。

これらのデバイスは、3 線式 (書き込み専用) シリアル ペリフェラル インターフェイス (SPI) 経由で通信します。これらのデバイスは、ロード DAC ($\overline{LDAC}$) とクリア ($\overline{CLR}$) 入力も備えています。

製品情報

部品番号	分解能	パッケージ (1)
DAC43508	8 ビット	RTE (WQFN、16)
DAC53508	10 ビット	
DAC63508	12 ビット	

(1) 詳細については、セクション 11 を参照してください。



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4 Pin Configurations and Functions

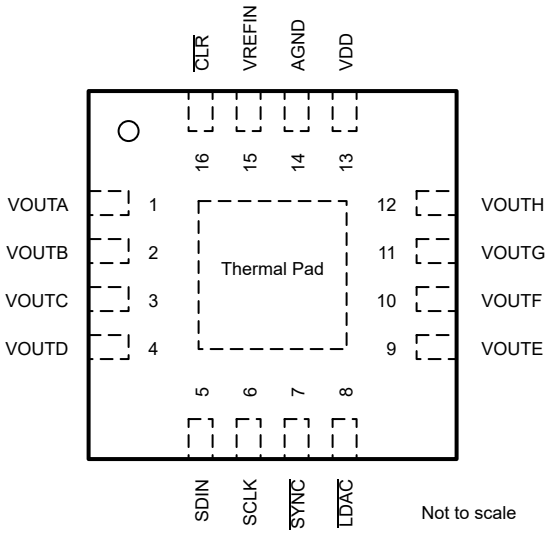


図 4-1. RTE Package, 16-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VOUTA	Output	Analog voltage output from DAC channel A.
2	VOUTB	Output	Analog voltage output from DAC channel B.
3	VOUTC	Output	Analog voltage output from DAC channel C.
4	VOUTD	Output	Analog voltage output from DAC channel D.
5	SDIN	Input	SPI data input.
6	SCLK	Input	SPI clock input.
7	$\overline{\text{SYNC}}$	Input	SPI chip select input (active low).
8	$\overline{\text{LDAC}}$	Input	Load DAC (active low) input for synchronous output update, simultaneous output update, or both.
9	VOUTE	Output	Analog voltage output from DAC channel E.
10	VOUTF	Output	Analog voltage output from DAC channel F.
11	VOUTG	Output	Analog voltage output from DAC channel G.
12	VOUTH	Output	Analog voltage output from DAC channel H.
13	VDD	Power	Power supply input (1.8 V to 5.5 V).
14	AGND	Ground	Ground reference for all circuitry on the device.
15	VREFIN	Power	External reference input. To use VDD as the reference, connect this pin to VDD.
16	$\overline{\text{CLR}}$	Input	Asynchronous output clear input (active low).
—	Thermal Pad	Ground	Connect thermal pad to AGND.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Power-supply voltage to A_{GND}	–0.3	6	V
V_{REFIN}	External reference voltage to A_{GND}	–0.3	V_{DD} + 0.3	V
	Digital inputs to A_{GND}	–0.3	V_{DD} + 0.3	V
V_{OUT}	Voltage output to A_{GND}	–0.3	V_{DD} + 0.3	V
	Current into any pin except the VOUTx, VDD, and AGND pins	–10	10	mA
T_J	Junction temperature,T_J	–40	150	°C
T_{stg}	Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD} to A_{GND}	Positive supply voltage to ground		1.8		5.5	V
V_{REFIN} to A_{GND}	Reference input supply voltage to ground		1.8		V_{DD}	V
V_{IH}	Digital input high voltage	1.8 V ≤ V_{DD} ≤ 2.7 V	V_{DD} – 0.3			V
		2.7 V < V_{DD} ≤ 5.5 V	2.4			
V_{IL}	Digital input low voltage				0.5	V
T_A	Ambient temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		DACx3508 RTE (WQFN) 16 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

5.5 Electrical Characteristics

all minimum and maximum values at T_A = –40°C to +125°C and all typical values at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{REFIN} = 2.5 V for V_{DD} ≥ 2.7 V, V_{REFIN} = 1.8 V for V_{DD} ≤ 2.7 V, R_L= 5 kΩ to A_{GND}, C_L = 200 pF to A_{GND}, and digital inputs at V_{DD} or A_{GND} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC63508	12			Bits
		DAC53508	10			
		DAC43508	8			
INL	Integral nonlinearity(1)	DAC53508, DAC43508	–1		1	LSB
		DAC63508	–4		4	
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error	Code 0d into DAC		6	12	mV
	Zero-code-error temperature coefficient	Code 0d into DAC		±5		µV/°C
	Offset error(1)		–0.5	0.25	0.5	%FSR
	Offset-error temperature coefficient(1)			±0.0003		%FSR/°C
	Gain error(1)		–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(1)			±0.0004		%FSR/°C
	Full-scale error(4)	2.7 V ≤ V_{DD} ≤ 5.5 V	–0.5	0.25	0.5	%FSR
		1.8 V ≤ V_{DD} ≤ 2.7 V	–1	0.5	1	
	Full-scale-error temperature coefficient(4)			±0.0004		%FSR/°C
OUTPUT						
V_{OUTX}	Output voltage		0		V_{DD}	V
C_L	Capacitive load(2)	R_L = Infinite			1	nF
					2	
	Load regulation	DAC at midscale, –10 mA ≤ I_{OUT} ≤ +10 mA, V_{DD} = 5.5 V		0.1		mV/mA
	Short-circuit current(3)	V_{DD} = 1.8 V		10		mA
		V_{DD} = 2.7 V		25		
		V_{DD} = 5.5 V		50		
	Output voltage headroom	To V_{DD}, DAC output unloaded		0.05		V
	Output voltage headroom(2)	To V_{DD}, load current = 10 mA at V_{DD} = 5.5 V, load current = 3 mA at V_{DD} = 2.7 V, load current = 1 mA at V_{DD} = 1.8 V, DAC code at full-scale	10			%FSR
Z_O	DC output impedance	DAC at midscale		0.25		Ω
		DAC at code 32d		0.25		
		DAC at code 4064d		0.26		
DC PSRR	Power supply rejection ratio (dc)	DAC at midscale, V_{DD} = 5 V ±10%		0.25		mV/V

5.5 Electrical Characteristics (続き)

all minimum and maximum values at T_A = –40°C to +125°C and all typical values at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{REFIN} = 2.5 V for V_{DD} ≥ 2.7 V, V_{REFIN} = 1.8 V for V_{DD} ≤ 2.7 V, R_L= 5 kΩ to A_{GND}, C_L = 200 pF to A_{GND}, and digital inputs at V_{DD} or A_{GND} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		10		µs
SR	Slew rate	V_{DD} = 5.5 V		0.6		V/µs
	Power-on glitch magnitude			110		mV
V_n	Output noise	f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		40		μV_{pp}
V_n	Output noise	f = 0.1 Hz to 100 kHz, DAC at midscale, V_{DD} = 5.5 V		0.05		mV_{rms}
V_n	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.2		µV/√Hz
		f = 10 kHz, DAC at midscale, V_{DD} = 5.5 V		0.2		
AC PSRR	Power-supply rejection ratio (ac)	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage, DAC at midscale		–71		dB
	Channel-to-channel ac crosstalk	Full-scale swing on adjacent channel		1.5		nV-s
	Channel-to-channel dc crosstalk	Full-scale swing on all channels, measured channel at zero-scale or full-scale		0.2		LSB
	Code change glitch impulse	±1-LSB change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1-LSB change around midscale (including feedthrough)		25		mV
VOLTAGE REFERENCE INPUT						
	Reference input impedance	All channels powered on		24		kΩ
	Reference input capacitance			50		pF
DIGITAL INPUTS						
	Digital feedthrough	SCLK = 1 MHz, DAC output static at midscale		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Current flowing into V_{DD}	Normal mode, all DACs at full-scale, digital interface static		3	5	mA
		All DAC channels powered down		50		µA

(1) End point fit between codes: code 32d to 4064d for 12 bit, code 8d to code 1016d for 10 bit, code 2d to code 252d for 8 bit.
(2) Characterized by design. Not production tested.
(3) Full-scale output shorted per channel to A_{GND} or zero-scale output shorted to V_{DD}.
(4) Code 4095d into DAC, no headroom.

5.6 Timing Requirements: SPI

all inputs signals are specified with $t_R = t_F$ = 1 V/ns (10% to 90% of V_{DD}) and timed from a voltage level of $V_{DD}/2$, 1.8 V ≤ V_{DD} ≤ 5.5 V and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency, 1.7 V ≤ V_{DD} < 2.7 V			25	MHz
	Serial clock frequency, 2.7 V ≤ V_{DD} ≤ 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ V_{DD} < 2.7 V	20			ns
	SCLK high time, 2.7 V ≤ V_{DD} ≤ 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ V_{DD} < 2.7 V	20			ns
	SCLK low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	10			
t_{SDIS}	SDI setup time, 1.7 V ≤ V_{DD} < 2.7 V	16			ns
	SDI setup time, 2.7 V ≤ V_{DD} ≤ 5.5 V	8			
t_{SDIH}	SDI hold time, 1.7 V ≤ V_{DD} < 2.7 V	10			ns
	SDI hold time, 2.7 V ≤ V_{DD} ≤ 5.5 V	5			
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time, 1.7 V ≤ V_{DD} < 2.7 V	36			ns
	$\overline{SYNC}$ to SCLK falling edge setup time, 2.7 V ≤ V_{DD} ≤ 5.5 V	18			
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge, 1.7 V ≤ V_{DD} < 2.7 V	10			ns
	SCLK falling edge to $\overline{SYNC}$ rising edge, 2.7 V ≤ V_{DD} ≤ 5.5 V	5			
t_{CSHIGH}	$\overline{SYNC}$ high time, 1.7 V ≤ V_{DD} < 2.7 V	50			ns
	$\overline{SYNC}$ high time, 2.7 V ≤ V_{DD} ≤ 5.5 V	25			

5.7 Timing Requirements: Logic

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, 1.8 V ≤ V_{REFIN} ≤ V_{DD}, –40°C ≤ T_A ≤ +125°C, V_{pullup} = V_{DD} for 1.8 V ≤ V_{DD} ≤ 2.7 V, V_{pullup} = 2.7 V or V_{DD} for 2.7 V ≤ V_{DD} ≤ 5.5 V

		MIN	NOM	MAX	UNIT
$t_{CS2LDAC}$	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ V_{DD} < 2.7 V	100			ns
	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 2.7 V ≤ V_{DD} ≤ 5.5 V	50			
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ V_{DD} < 2.7 V	60			ns
	$\overline{LDAC}$ low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	30			
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ V_{DD} < 2.7 V	60			ns
	$\overline{CLR}$ low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	30			

5.8 Timing Diagrams

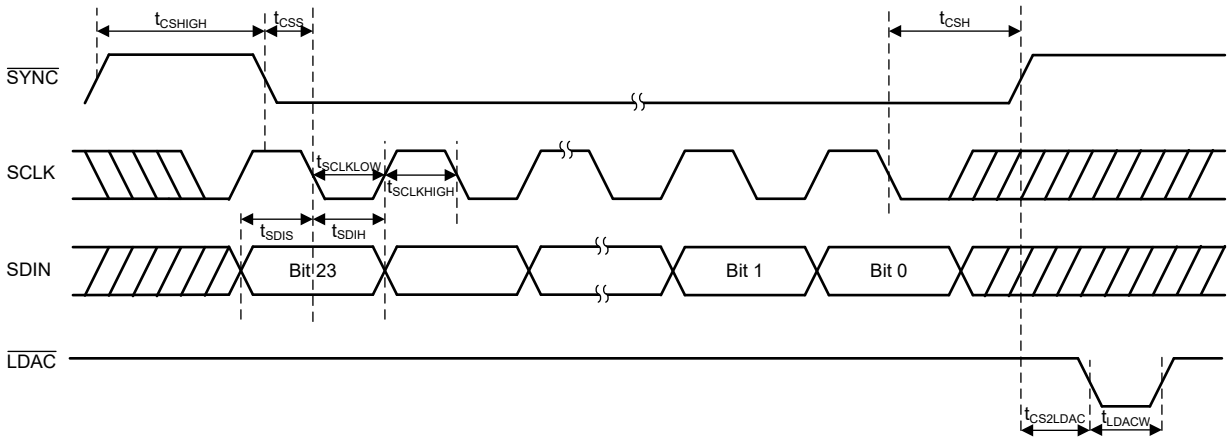
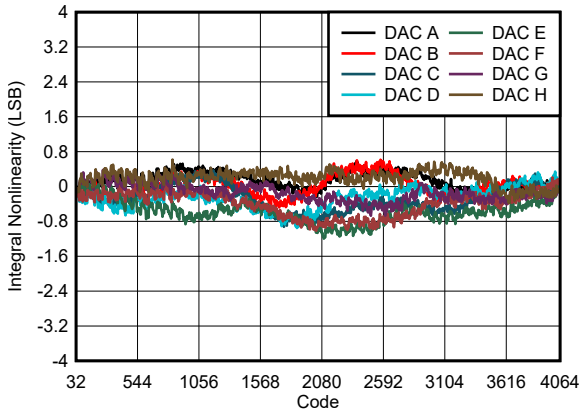


図 5-1. Serial Interface Timing Diagram

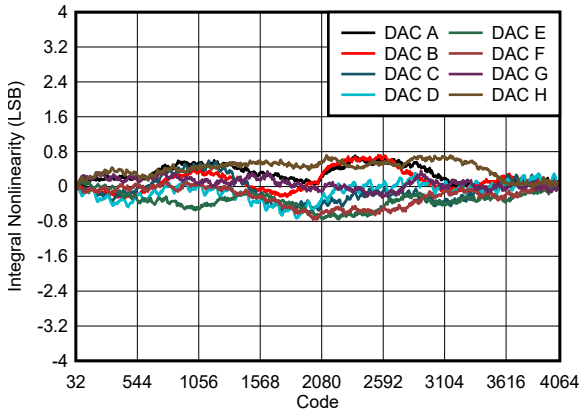
5.9 Typical Characteristics: Static Performance

at T_A = 25°C, reference = 1.8 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



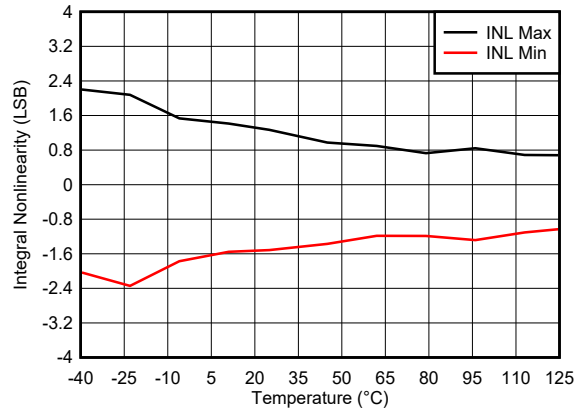
V_{DD} = 1.8 V

図 5-2. Integral Nonlinearity vs Digital Input Code



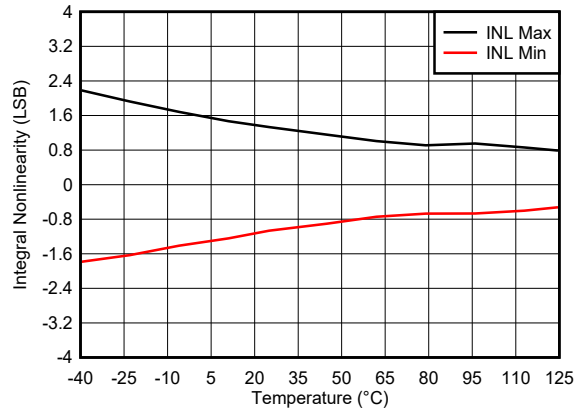
V_{DD} = 5.5 V

図 5-3. Integral Nonlinearity vs Digital Input Code



V_{DD} = 1.8 V

図 5-4. Integral Nonlinearity vs Temperature



V_{DD} = 5.5 V

図 5-5. Integral Nonlinearity vs Temperature

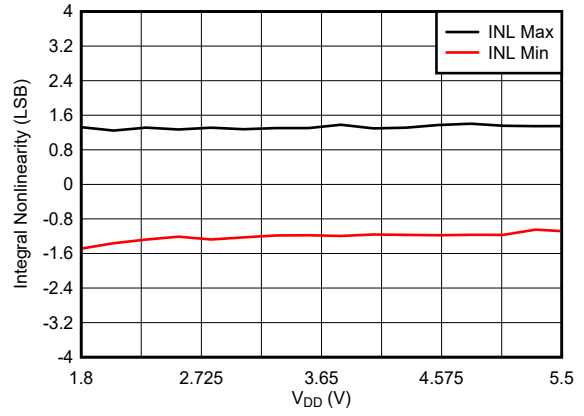
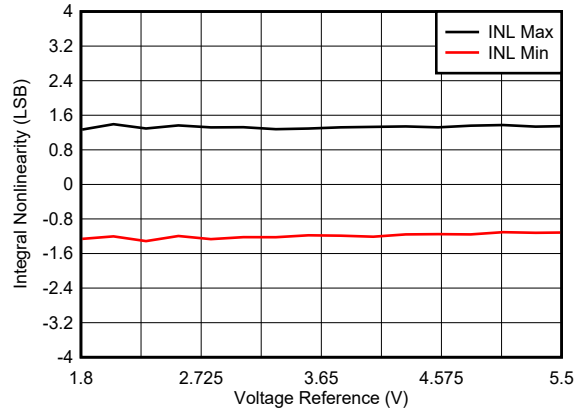


図 5-6. Integral Nonlinearity vs Supply Voltage

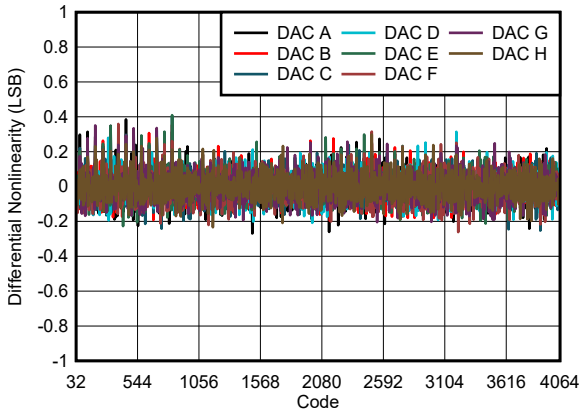


V_{DD} = 5.5 V

図 5-7. Integral Nonlinearity vs Voltage Reference

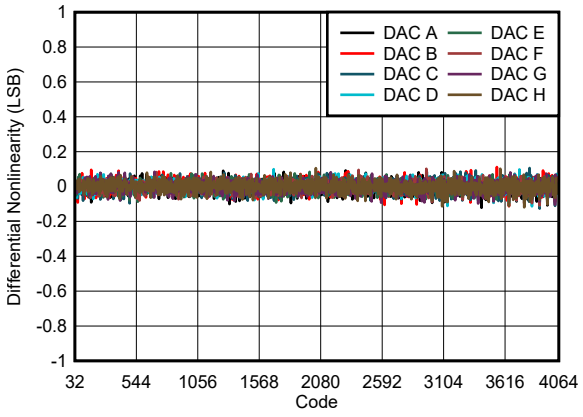
5.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



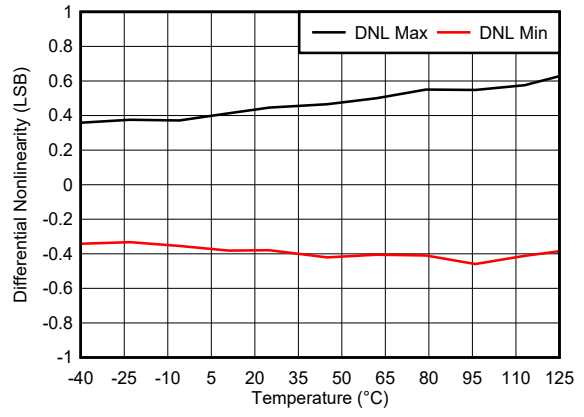
V_{DD} = 1.8 V

図 5-8. Differential Nonlinearity vs Digital Input Code



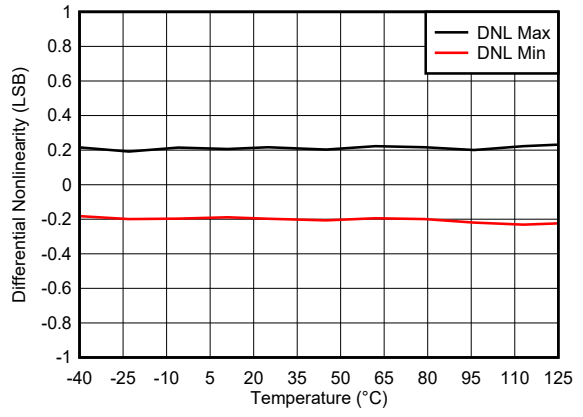
V_{DD} = 5.5 V

図 5-9. Differential Nonlinearity vs Digital Input Code



V_{DD} = 1.8 V

図 5-10. Differential Nonlinearity vs Temperature



V_{DD} = 5.5 V

図 5-11. Differential Nonlinearity vs Temperature

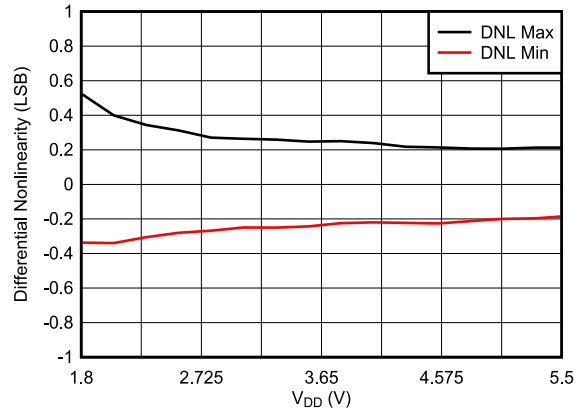


図 5-12. Differential Nonlinearity vs Supply Voltage

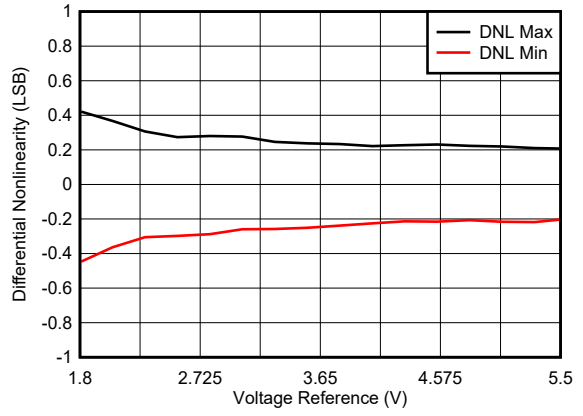
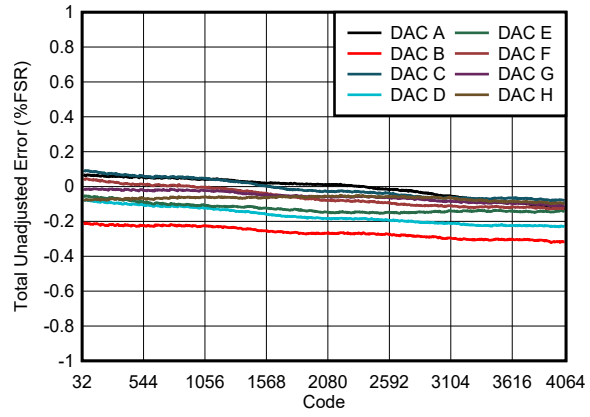


図 5-13. Differential Nonlinearity vs Voltage Reference

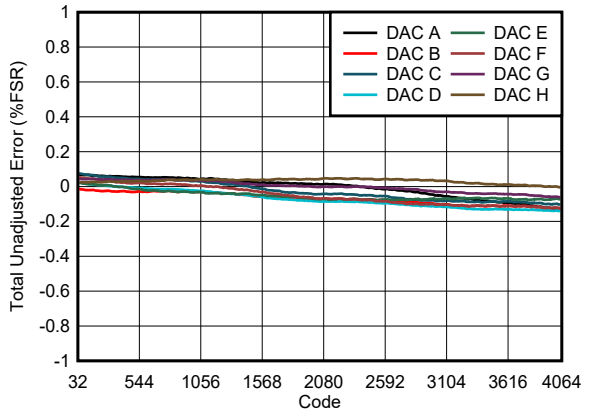
5.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



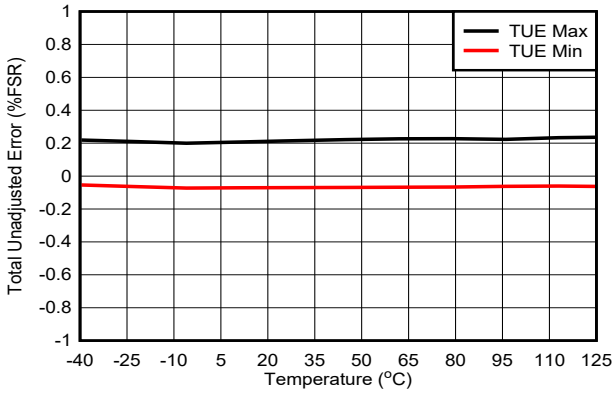
V_{DD} = 1.8 V

図 5-14. Total Unadjusted Error vs Digital Input Code



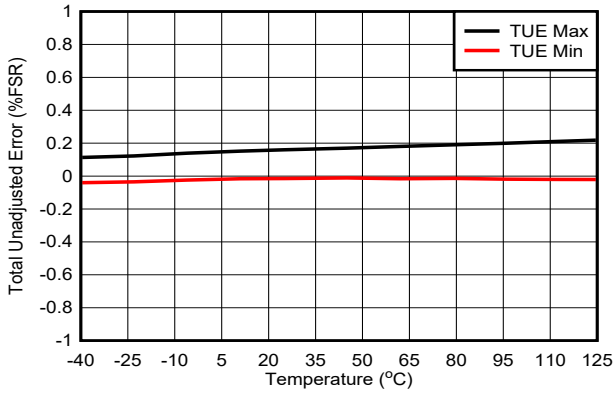
V_{DD} = 5.5 V

図 5-15. Total Unadjusted Error vs Digital Input Code



V_{DD} = 1.8 V

図 5-16. Total Unadjusted Error vs Temperature



V_{DD} = 5.5 V

図 5-17. Total Unadjusted Error vs Temperature

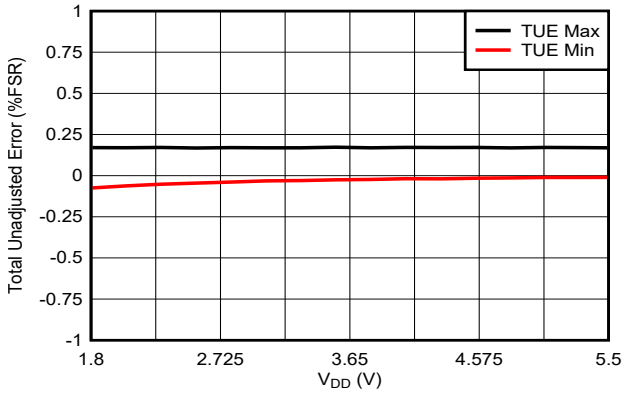
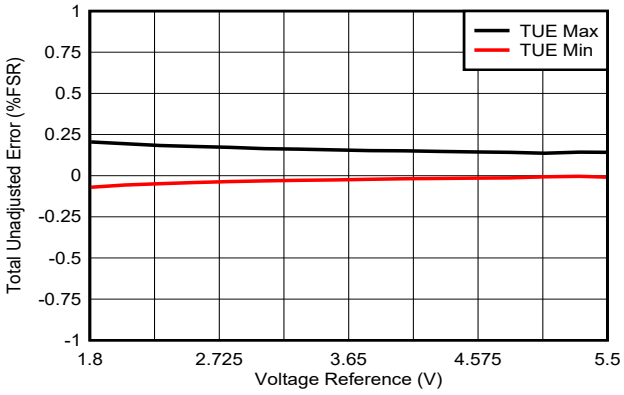


図 5-18. Total Unadjusted Error vs Supply Voltage



V_{DD} = 5.5 V

図 5-19. Total Unadjusted Error vs Voltage Reference

5.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

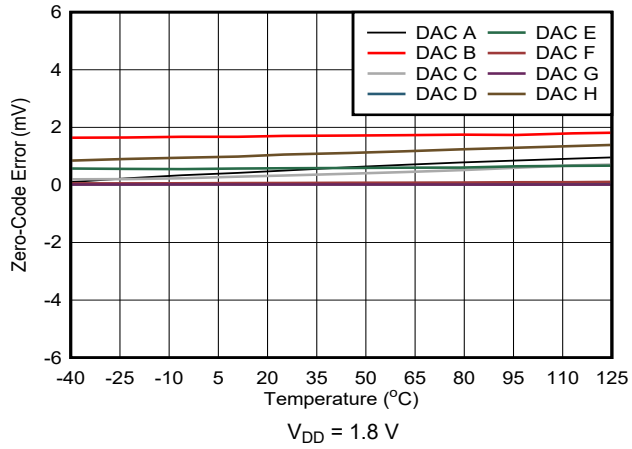


図 5-20. Zero-Code Error vs Temperature

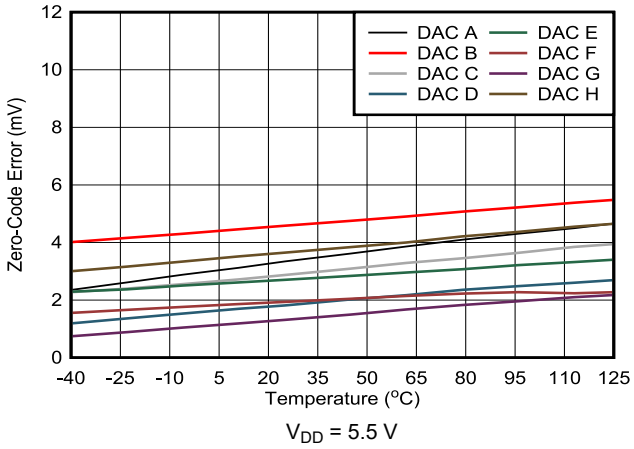


図 5-21. Zero-Code Error vs Temperature

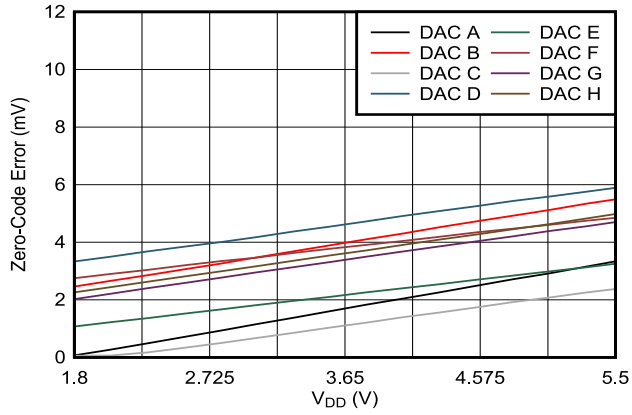


図 5-22. Zero-Code Error vs Supply Voltage

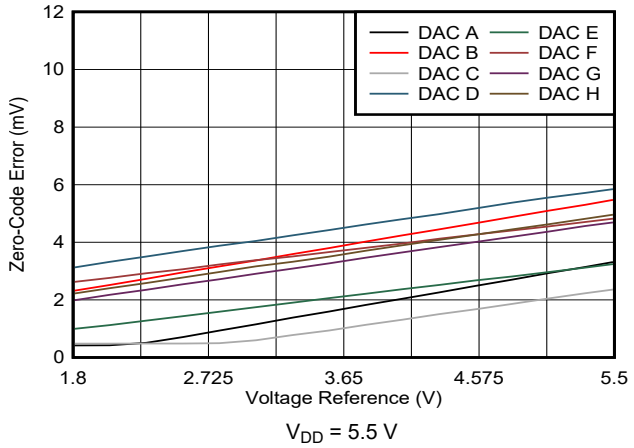


図 5-23. Zero-Code Error vs Voltage Reference

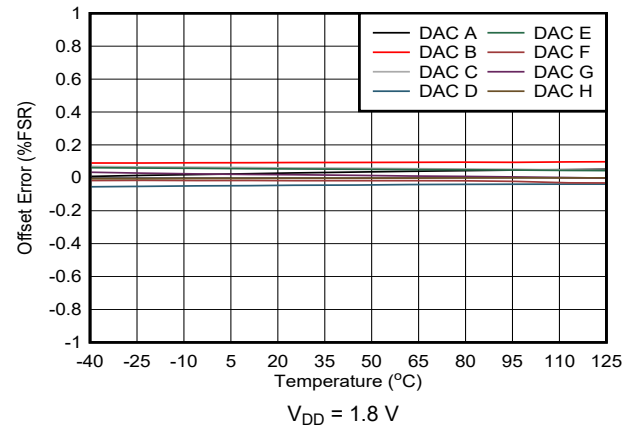


図 5-24. Offset Error vs Temperature

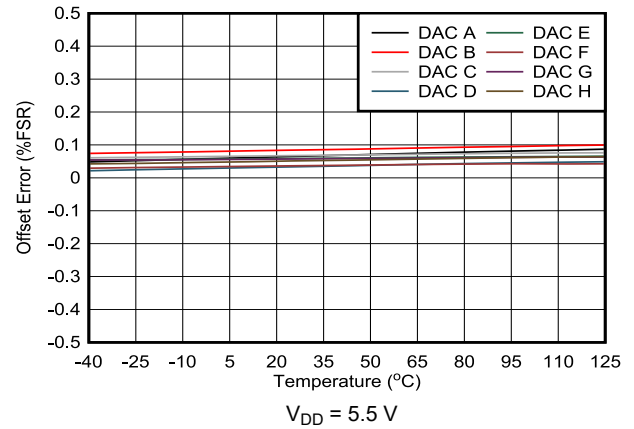


図 5-25. Offset Error vs Temperature

5.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

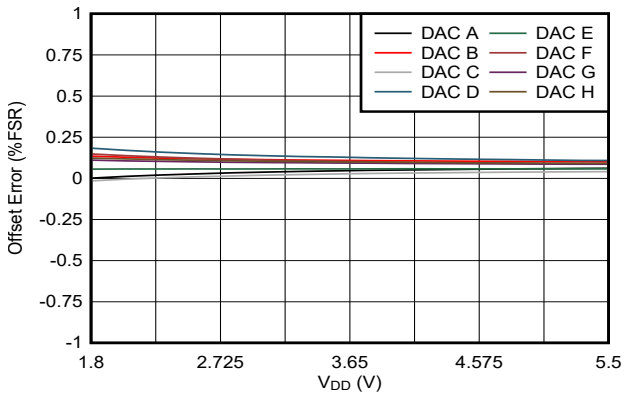


図 5-26. Offset Error vs Supply Voltage

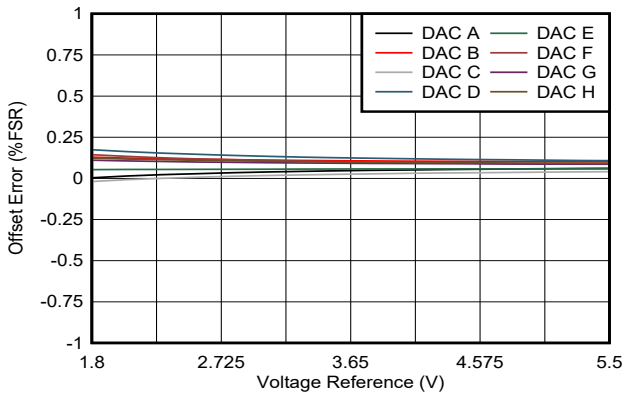


図 5-27. Offset Error vs Voltage Reference

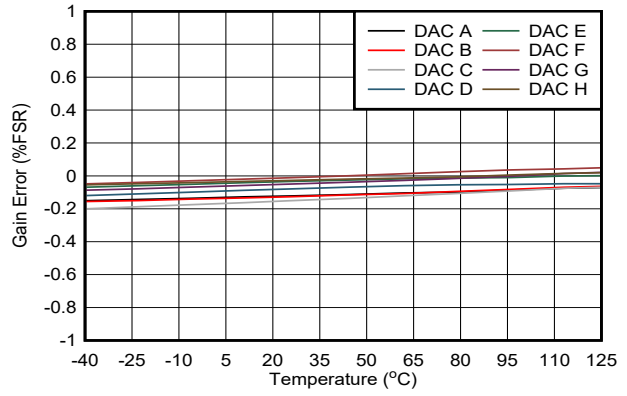


図 5-28. Gain Error vs Temperature

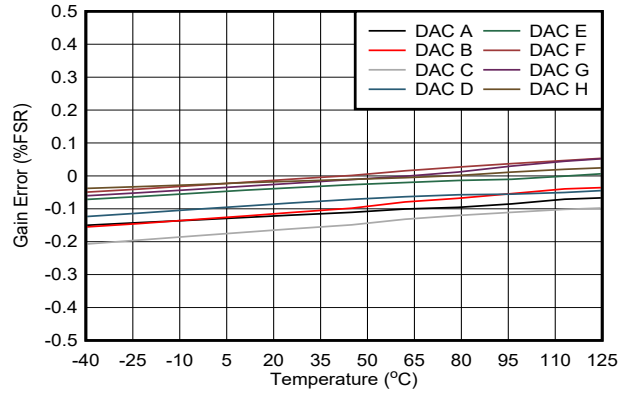


図 5-29. Gain Error vs Temperature

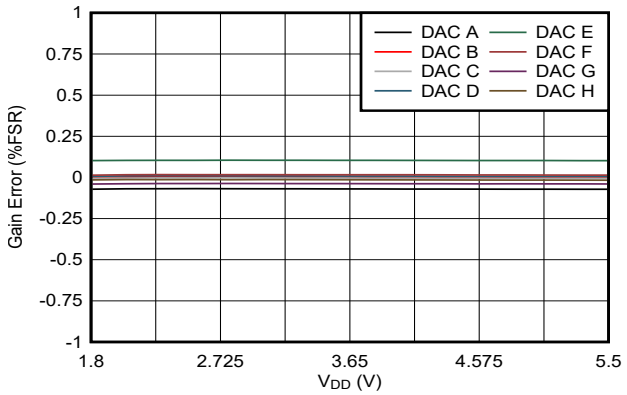


図 5-30. Gain Error vs Supply Voltage

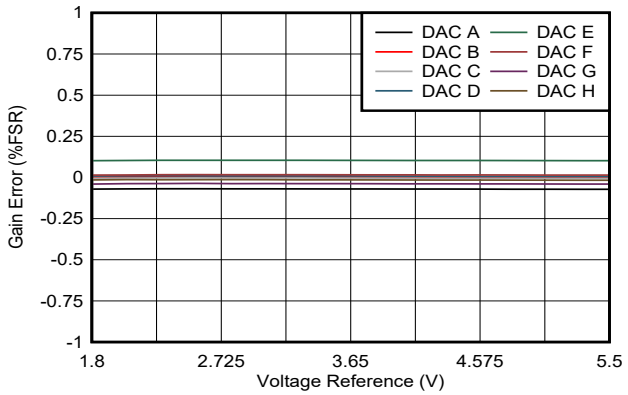
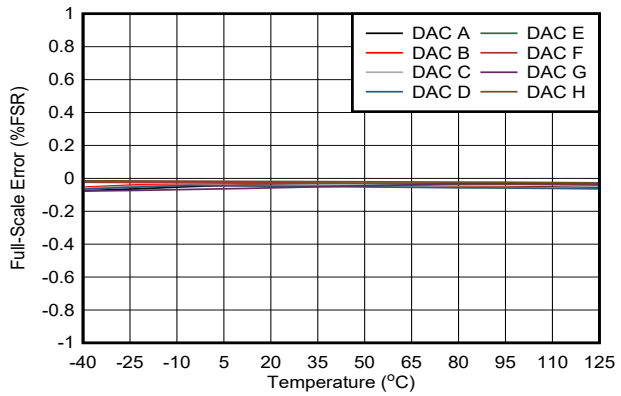


図 5-31. Gain Error vs Voltage Reference

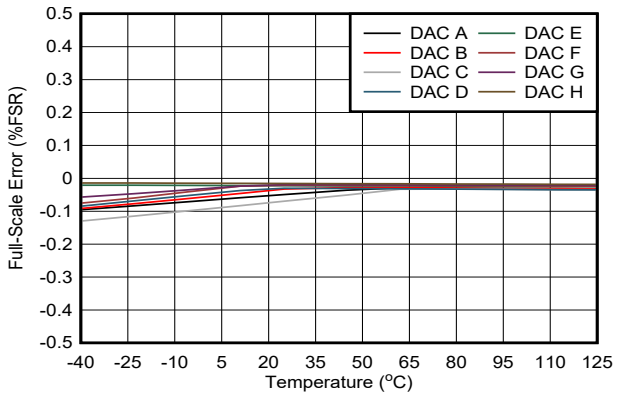
5.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



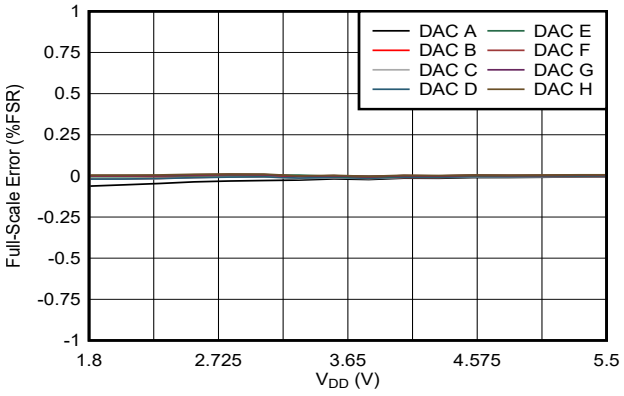
V_{DD} = 1.8 V

図 5-32. Full-Scale Error vs Temperature



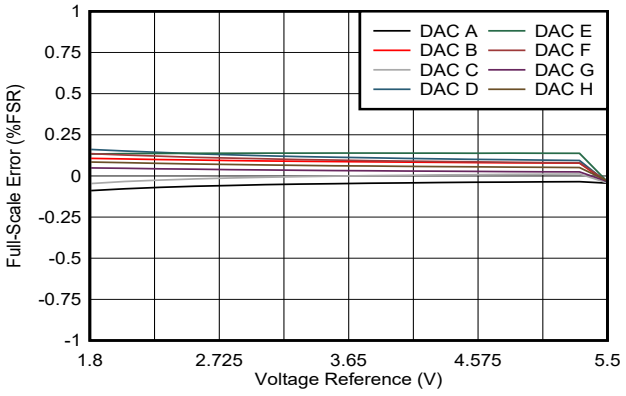
V_{DD} = 5.5 V

図 5-33. Full-Scale Error vs Temperature



V_{DD} = 5.5 V

図 5-34. Full-Scale Error vs Supply Voltage

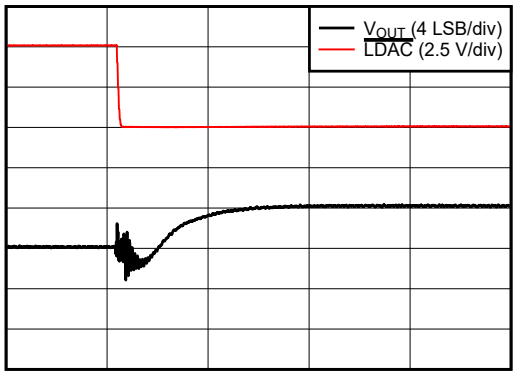


V_{DD} = 5.5 V

図 5-35. Full-Scale Error vs Voltage Reference

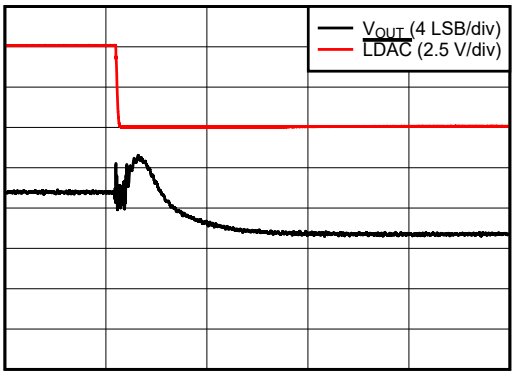
5.10 Typical Characteristics: Dynamic Performance

at T_A = 25°C, V_{DD} = 5.5 V, reference = 5.5 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



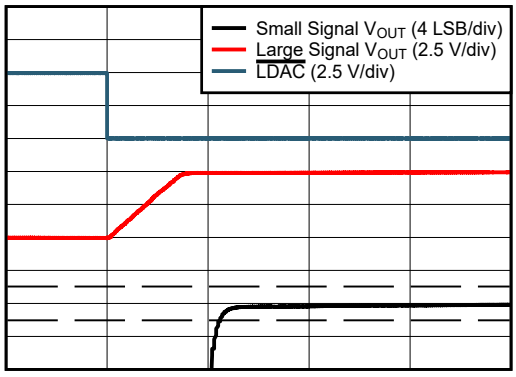
DAC code transition from midscale – 4 LSB to midscale, output load: 5 kΩ || 200 pF

図 5-36. Glitch Impulse, Rising Edge, 4-LSB Step



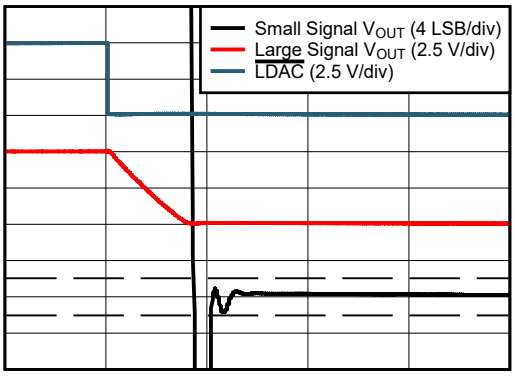
DAC code transition from midscale to midscale – 4 LSB, output load: 5 kΩ || 200 pF

図 5-37. Glitch Impulse, Falling Edge, 4-LSB Step



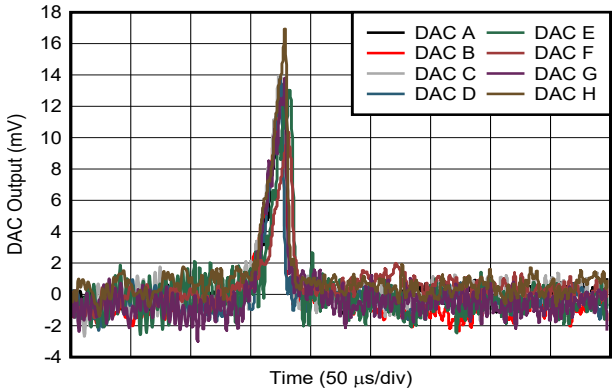
DAC code transition from 408d to 3688d, typical channel shown, output load: 5 kΩ || 200 pF

図 5-38. Full-Scale Settling Time, Rising Edge



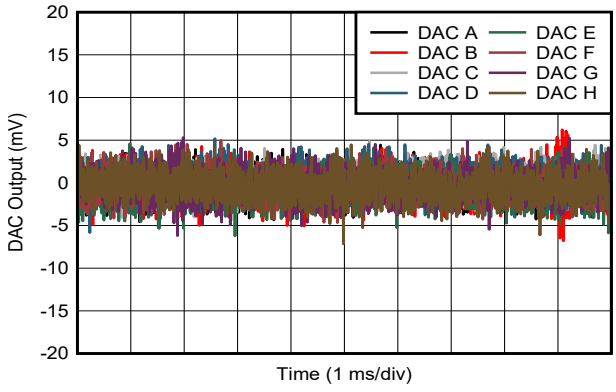
DAC code transition from 3688d to 408d, typical channel shown, output load: 5 kΩ || 200 pF

図 5-39. Full-Scale Settling Time, Falling Edge



Output load: 5 kΩ || 200 pF

図 5-40. Power-On Glitch

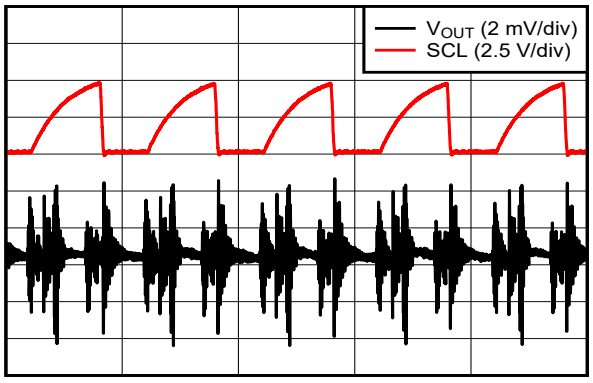


Output load: 5 kΩ || 200 pF

図 5-41. Power-Off Glitch

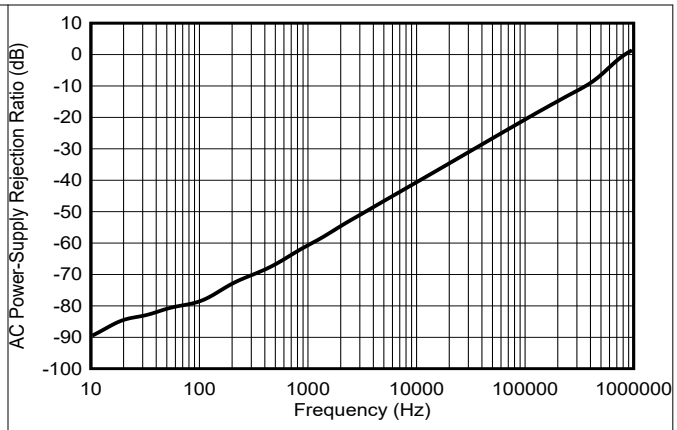
5.10 Typical Characteristics: Dynamic Performance (continued)

at T_A = 25°C, V_{DD} = 5.5 V, reference = 5.5 V, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



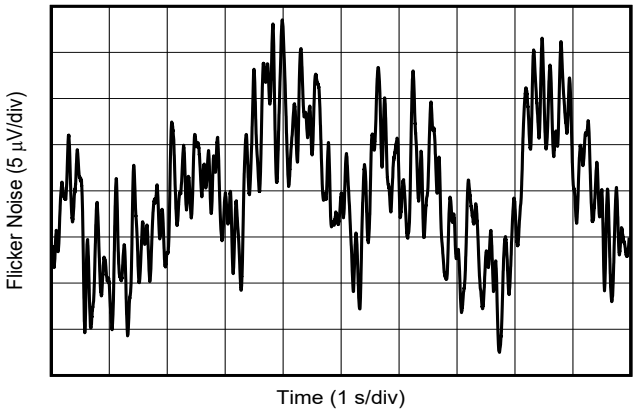
DAC at midscale, reference tied to V_{DD}, output load: 5 kΩ || 200 pF, SCLK = 1 MHz

図 5-42. Clock Feedthrough



DAC at full-scale, output load: 5 kΩ || 200 pF, V_{DD} = 5.25 V + 0.2 V_{PP}, V_{REFIN} = 4.5 V

図 5-43. AC Power-Supply Rejection Ratio vs Frequency



DAC at midscale, f = 0.1 Hz to 10 Hz

図 5-44. Flicker Noise

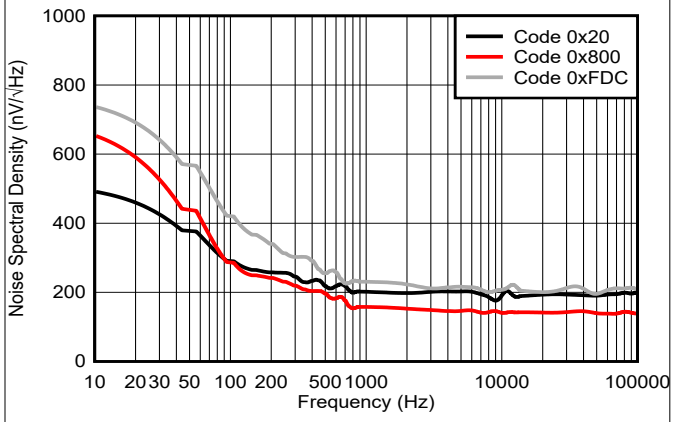
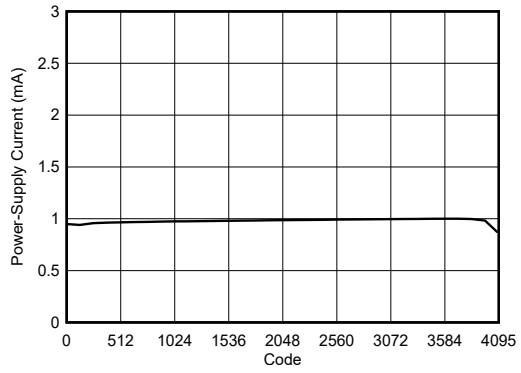


図 5-45. Noise Spectral Density

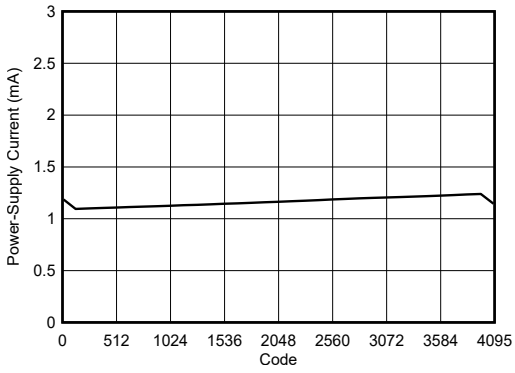
5.11 Typical Characteristics: General

at T_A = 25°C, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



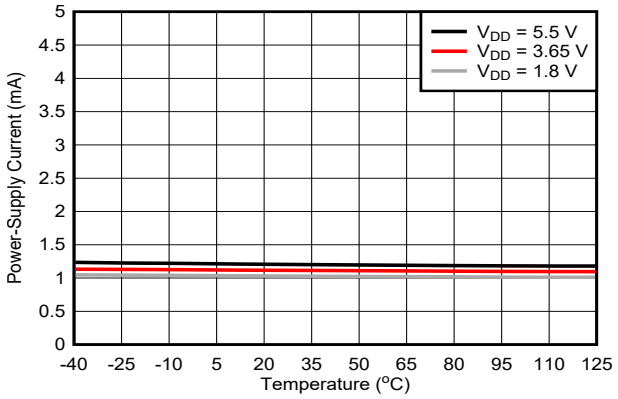
V_{DD} = 1.8 V, reference = 1.8 V

図 5-46. Power-Supply Current vs Digital Input Code



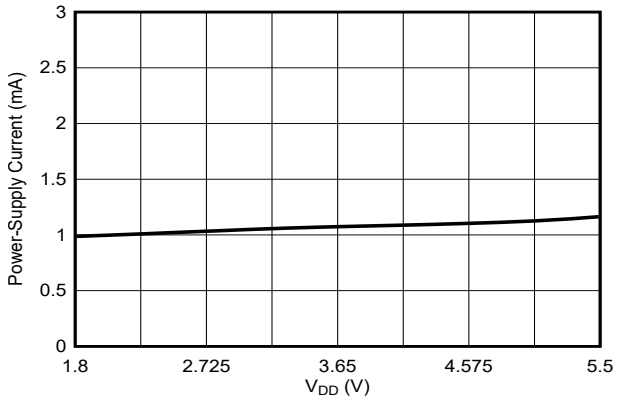
V_{DD} = 5.5 V, reference = 5.5 V

図 5-47. Power-Supply Current vs Digital Input Code



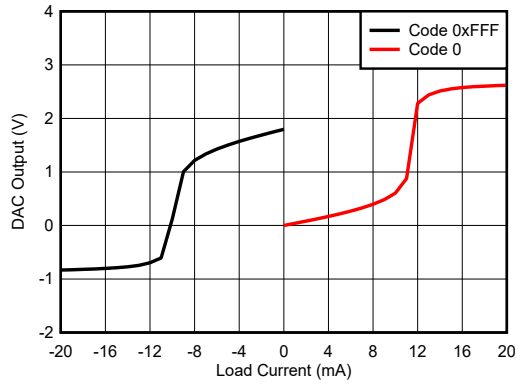
DAC at midscale

図 5-48. Power-Supply Current vs Temperature



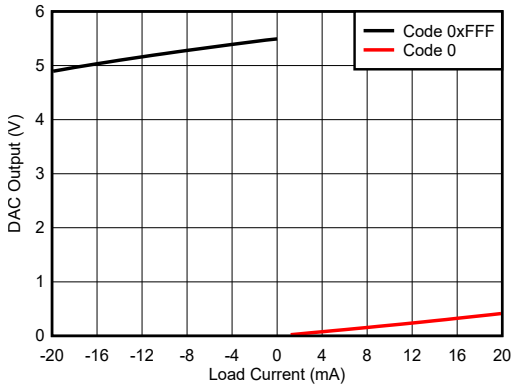
DAC at midscale, reference tied to V_{DD}

図 5-49. Power-Supply Current vs Supply Voltage



V_{DD} = 1.8 V, reference = 1.8 V

図 5-50. Output Source and Sink Capability

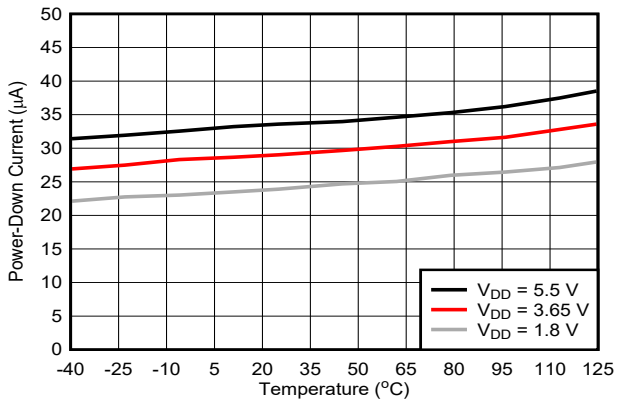


V_{DD} = 5.5 V, reference = 5.5 V

図 5-51. Output Source and Sink Capability

5.11 Typical Characteristics: General (continued)

at T_A = 25°C, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



V_{DD} = 5.5 V

図 5-52. Power-Down Current vs Temperature

6 Detailed Description

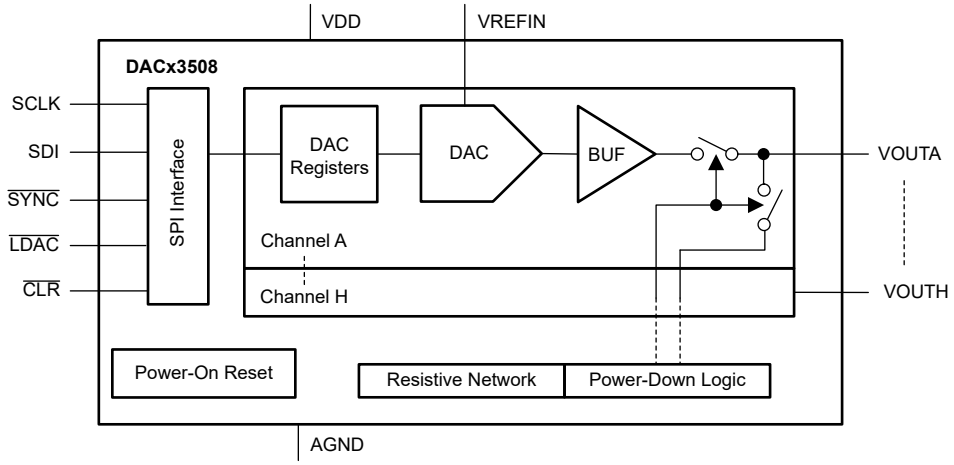
6.1 Overview

The 8-bit DAC43508, 10-bit DAC53508, and 12-bit DAC63508 (DACx3508) are a pin-compatible family of eight-channel, buffered voltage-output digital-to-analog converters (DACs). With an external reference ranging from 1.8 V to 5.5 V, a full-scale output voltage of 1.8 V to 5.5 V is achievable. These devices are specified monotonic across the power-supply range.

Communication to the devices is established through a three-wire SPI-compatible interface. These devices do not support readback operation. These devices include a load DAC ($\overline{\text{LDAC}}$) pin for simultaneous DAC updates and a clear ($\overline{\text{CLR}}$) pin for setting the outputs to zero scale.

The DACx3508 devices are characterized for operation over the temperature range of –40°C to +125°C and are available in tiny QFN packages.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Digital-to-Analog Converter (DAC) Architecture

Each output channel in the DACx3508 family of devices consists of string architecture with an output buffer amplifier. 図 6-1 shows a block diagram of the DAC architecture.

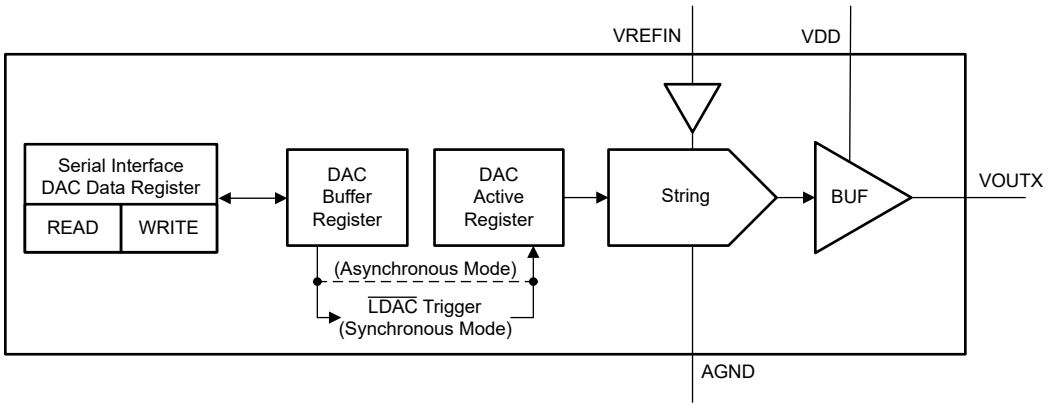


図 6-1. DACx3508 DAC Architecture

6.3.1.1 DAC Transfer Function

The device writes the input data to the individual DAC Data registers in straight binary format. After a power-on or a reset event, the device sets all DAC registers to zero-code. 式 1 shows DAC transfer function.

$$V_{OUTX} = \frac{DACn\_DATA}{2^N} \times V_{REFIN} \quad (1)$$

where:

- N = resolution in bits: 8 (DAC43508), 10 (DAC53508), or 12 (DAC63508)
- DACn_DATA is the decimal equivalent of the binary code that is loaded to the DAC register
- DACn_DATA ranges from 0 to $2^N - 1$
- V_{REFIN} is the DAC reference voltage

6.3.1.2 DAC Register Update and $\overline{\text{LDAC}}$ Functionality

The device stores the data written to the DAC data registers in the DAC buffer registers. Transfer of data from the DAC buffer registers to the DAC active registers can be set to happen immediately (asynchronous mode) or initiated by an $\overline{\text{LDAC}}$ trigger (synchronous mode). After the DAC active registers are updated, the DAC outputs change to the new values.

The update mode for each DAC channel is determined by the status of $\overline{\text{LDAC}}$ pin.

In asynchronous mode ($\overline{\text{LDAC}}$ = low before the DAC write command), a write to the DAC data register results in an immediate update of the DAC active register and DAC output at the 24th rising-edge of the clock.

In synchronous mode ($\overline{\text{LDAC}}$ = high before the DAC write command), writing to the DAC data register does not automatically update the DAC output. Instead, the update occurs only after $\overline{\text{LDAC}}$ is pulled low. The synchronous update mode enables simultaneous update of all DAC outputs.

6.3.1.3 $\overline{\text{CLR}}$ Functionality

The $\overline{\text{CLR}}$ pin is an asynchronous input pin to the DAC. When this pin is pulled low, the DAC buffers and the DAC active registers are set to zero code.

6.3.1.4 Output Amplifier

The output buffer amplifier generates rail-to-rail voltages on the output, giving a maximum output range of 0 V to V_{DD}. 式 1 shows that the full-scale output range of the DAC output is determined by the voltage on the VREFIN pin

6.3.2 Reference

The DACx3508 require an external reference to operate. However, the reference pin, VREFIN, and the supply pin, VDD, can be tied together. The reference input pin voltage ranges from 1.8 V to V_{DD}. The typical input impedance of this pin when all the channels are powered on is 24 kΩ.

6.3.3 Power-On Reset (POR)

The DACx3508 family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a 5-ms delay, when V_{DD} reaches DAC operating range. The default value for the DAC data registers is zero code. The DAC output remains at the power-up voltage until a valid command is written to a channel.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in 図 6-2, to discharge the internal capacitors and reset the device on power up. To trigger a POR, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.7 V but remains greater than 0.7 V (shown as the undefined region), the device does not reset successfully under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.7 V, a POR does not occur.

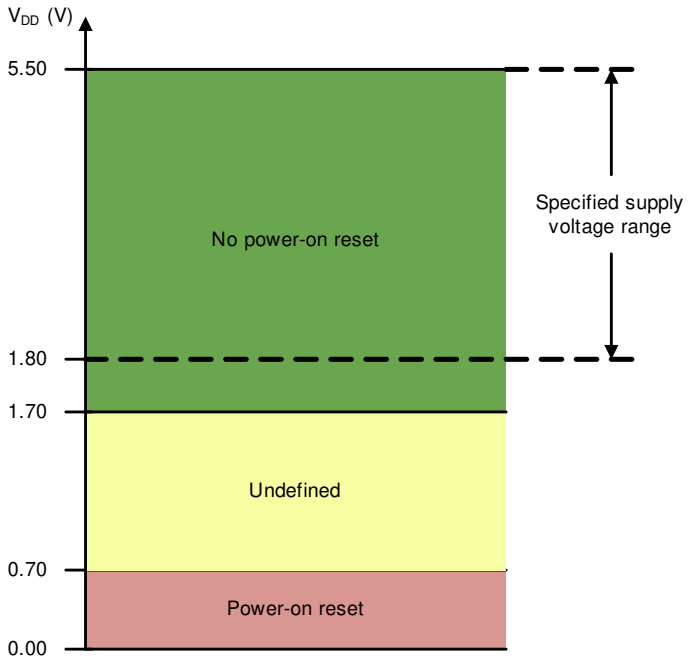


図 6-2. Threshold Levels for V_{DD} POR Circuit

6.3.4 Software Reset

A device software reset event is initiated by writing the reserved code 1010b to the SW_RST bit in the STATUS_TRIGGER register.

6.4 Device Functional Modes

The DACx3508 has two modes of operation: normal and power-down.

6.4.1 Power-Down Mode

The DACx3508 DAC output amplifiers can be independently or globally powered down (10 kΩ to A_{GND}) through the DEVICE_CONFIG register. In global power down mode, the device consumes 50 µA (V_{DD} = 1.8 V). At power-up, all output channels buffer amplifiers start in power-down (10 kΩ-AGND) mode until a power-up command is issued by writing 0 to the per-channel power-down register bits.

6.5 Programming

6.5.1 Serial Peripheral Interface (SPI)

The DACx3508 supports a three-wire SPI with write-only functionality. An SPI write cycle for DACx3508 is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for DACx3508 is 24 bits long; therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 SCLK falling edges. The write cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the write cycle contains less than the minimum clock edges, the communication is ignored. If the write cycle contains more than the minimum clock edges, only the first 24 bits are used by the device.

表 6-1 describes the format for the 24-bit SPI write access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as the 8-bit address to be written. The last 16 bits in the cycle form the data cycle.

表 6-1. SPI Write Access Cycle

BIT	FIELD	DESCRIPTION
23-16	A[7:0]	Register address: specifies the register to be accessed during the write operation.
15-0	DI[15:0]	Data cycle bits: The data cycle bits are the values written to the register with address A[7:0].

7 Register Map

表 7-1. Register Map

REGISTER NAME	REGISTER ADDRESS	DATA BITS												
		MSDB				LSDB								
	B23-B16	B15-B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DEVICE_CONFIG (セクション 7.1)	01h	X	RESERVED			PDN-All	PDNH	PDNG	PDNF	PDNE	PDND	PDNC	PDNB	PDNA
STATUS_TRIGGER (セクション 7.2)	02h	X	X								SW_RST			
BRDCAST (セクション 7.3)	03h	X	BRDCAST_DATA[11:0] / BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0]											
DACA_DATA (セクション 7.4)	08h	X	DACA_DATA[11:0] / DACA_DATA[9:0] / DACA_DATA[7:0]											
DACB_DATA (セクション 7.4)	09h	X	DACB_DATA[11:0] / DACB_DATA[9:0] / DACB_DATA[7:0]											
DACC_DATA (セクション 7.4)	0Ah	X	DACC_DATA[11:0] / DACC_DATA[9:0] / DACC_DATA[7:0]											
DACD_DATA (セクション 7.4)	0Bh	X	DACD_DATA[11:0] / DACD_DATA[9:0] / DACD_DATA[7:0]											
DACE_DATA (セクション 7.4)	0Ch	X	DACE_DATA[11:0] / DACE_DATA[9:0] / DACE_DATA[7:0]											
DACF_DATA (セクション 7.4)	0Dh	X	DACF_DATA[11:0] / DACF_DATA[9:0] / DACF_DATA[7:0]											
DACG_DATA (セクション 7.4)	0Eh	X	DACG_DATA[11:0] / DACG_DATA[9:0] / DACG_DATA[7:0]											
DACH_DATA (セクション 7.4)	0Fh	X	DACH_DATA[11:0] / DACH_DATA[9:0] / DACAH_DATA[7:0]											

表 7-2. Register Section/Block Access Type Codes

Access Type	Code	Description
W	W	Write only
W	X	Don't care
-n		Value after reset or the default value

7.1 DEVICE_CONFIG Register (address = 01h) [reset = 00FFh]

図 7-1. DEVICE_CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				RESERVED			PDN-All	PDNH	PDNG	PDNF	PDNE	PDND	PDNC	PDNB	PDNA
W-0h				W-0h			W-0h	W-FFh							

表 7-3. DEVICE_CONFIG Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	X	W	0h	Don't care
11-9	RESERVED	W	0h	Reserved
8	PDN-All	W	0h	Global power down bit: 0: Normal operation 1: All DAC channels and internal biasing blocks are powered down.
7-0	PDNx	W	FFh	Channel-specific power down bits: 0: DACx powered up 1: DACx powered down with 10 kΩ pulldown resistor to A_{GND}.

7.2 STATUS_TRIGGER Register (address = 02h) [reset = 0000h]

図 7-2. STATUS_TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X												SW_RST			
W-000h												W-0h			

表 7-4. STATUS_TRIGGER Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	X	W	000h	Don't care
3-0	SW_RST	W	0h	Device resets to default value when this bit field is set to 1010b. Other values do not have any impact.

7.3 BRDCAST Register (address = 03h) [reset = 0000h]

図 7-3. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				BRDCAST_DATA[11:0], BRDCAST_DATA[9:0], BRDCAST_DATA[7:0]											
W-0h				W-000h											

表 7-5. BRDCAST Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	X	W	0h	Don't care
11-0	BRDCAST_DATA[11:0], BRDCAST_DATA[9:0], BRDCAST_DATA[7:0]	W	000h	Writing to the BRDCAST register forces the DAC channel to update the active register data to BRDCAST_DATA. Data are MSB-aligned in straight-binary format and follow the format below: DAC43508: { DATA[7:0], X, X, X, X } DAC53508: { DATA[9:0], X, X } DAC63508: { DATA[11:0] } X – Don’t care bits

7.4 DACn_DATA Register (address = 08h to 0Fh) [reset = 0000h]

図 7-4. DACn_DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				DACn_DATA[11:0], DACn_DATA[9:0], DACn_DATA[7:0]											
W-0h				W-000h											

表 7-6. DACn_DATA Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	X	W	0h	Don't care
11-0	DACn_DATA[11:0], DACn_DATA[9:0], DACn_DATA[7:0]	W	000h	Writing to the DACn_DATA register forces the respective DAC channel to update the active register data to the DACn_DATA. Data are MSB-aligned in straight-binary format and follow the format below: DAC43508: { DATA[7:0], X, X, X, X } DAC53508: { DATA[9:0], X, X } DAC63508: { DATA[11:0] } X – Don’t care bits

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DACx3508 is a buffered output, eight-channel, low-power DAC available in a tiny 3-mm x 3-mm package. The multichannel, low power, and small package makes this DAC an excellent choice for general-purpose applications in wide range of end equipment. Some of the most-common applications for these devices are LED biasing-in multifunction printers, power-supply supervision with programmable comparators, offset and gain trimming in precision circuits, and power-supply margining.

8.2 Typical Applications

8.2.1 Programmable LED Biasing

End equipments such as multifunction printers, projectors and electronic point-of-sale (EPOS) require a steady luminous intensity from the LED. 図 8-1 shows a simplified circuit diagram for biasing an LED using the DAC53508.

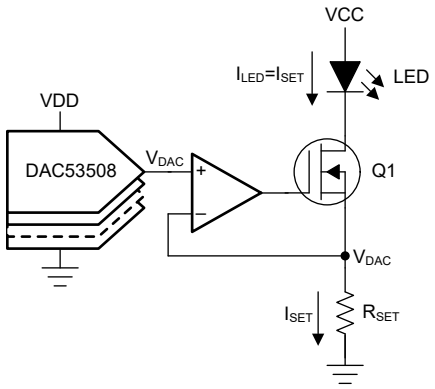


図 8-1. Programmable LED Biasing

8.2.1.1 Design Requirements

- Programmable constant current through an LED tied to a power supply on one end
- DAC output range: 0 V to 5 V
- LED current range: 0 mA to 20 mA

8.2.1.2 Detailed Design Procedure

The DAC is used to set the source current of a MOSFET using a unity-gain buffer, as shown in 図 8-1. Connect the LED between the power supply and the drain of the MOSFET. This configuration allows the DAC to control or set the amount of current through the LED. The buffer following the DAC controls the gate-source voltage of the MOSFET inside the feedback loop, thus compensating this drop and corresponding drift due to temperature, current, and ageing of the MOSFET. The current set by the DAC that flows through the LED is calculated with 式 2. To generate 0 mA to 20 mA from a 0 V to 5 V DAC output range, a 250-Ω R_{SET} is required.

$$I_{SET} = \frac{V_{DAC}}{R_{SET}} \tag{2}$$

The following pseudocode is provided to help get started with the LED biasing application:

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <DATA>
//Power-up the device and channels
WRITE DEVICE_CONFIG(0x01), 0x0000
//Program mid code (or the desired voltage) on all channels
WRITE DACA_DATA(0x08), 0x07FC //10-bit MSB aligned
WRITE DACB_DATA(0x09), 0x07FC //10-bit MSB aligned
WRITE DACC_DATA(0x0A), 0x07FC //10-bit MSB aligned
WRITE DACD_DATA(0x0B), 0x07FC //10-bit MSB aligned
WRITE DACE_DATA(0x0C), 0x07FC //10-bit MSB aligned
WRITE DACF_DATA(0x0D), 0x07FC //10-bit MSB aligned
WRITE DACG_DATA(0x0E), 0x07FC //10-bit MSB aligned
WRITE DACH_DATA(0x0F), 0x07FC //10-bit MSB aligned
```

8.2.1.3 Application Curve

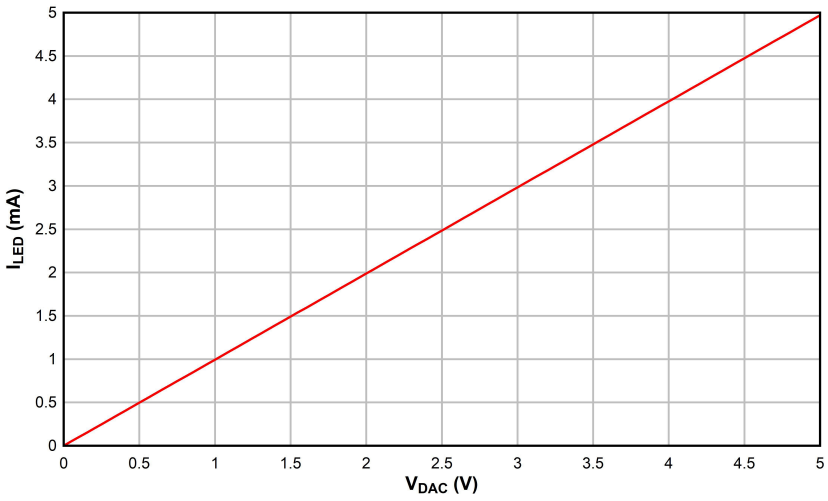


図 8-2. DC Transfer Characteristics of LED Biasing Circuit

8.2.2 Programmable Window Comparator

End equipment that use a centralized power supply (such as network servers, optical modules, and others) require the monitoring of power buses to protect the components. This monitoring or supervision is accomplished using a window comparator. A window comparator monitors a signal input for upper- and lower-threshold violations. A trigger signal is generated when the threshold violations occur. Multichannel monitoring is required to supervise all power supplies available in a module. The DACx3508 provides an easy-to-use, low-footprint method to address this requirement. 図 8-3 shows how the DAC53508 is used to create a programmable window comparator.

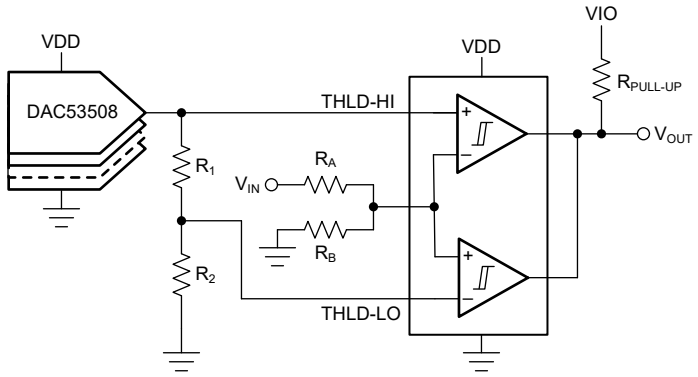


図 8-3. Programmable Window Comparator

8.2.2.1 Design Requirements

- Voltage to be monitored: 5 V
- High threshold: 5 V + 10%
- Low threshold: 5 V – 10%
- Trigger output: 3.3-V open-drain single output

8.2.2.2 Detailed Design Procedure

図 8-3 provides an example in which a single DAC channel is used to compare both high and low thresholds. A dual comparator is used per DAC channel, as shown. A voltage divider formed by resistors R_A and R_B are used to bring the signal level within the DAC range. Another pair of resistors, R_1 and R_2, are used to settle the low threshold as a factor of the high threshold. This configuration allows the use of a single DAC channel to monitor both the high- and low-threshold levels. Use open-drain comparators to provide the following advantages.

- Generate a logic output level appropriate for the monitoring processor
- Allow shorting of the two outputs to generate a single trigger

In the circuit depicted in 図 8-3, the output of the circuit remains high as long as the signal input remains within the high- and low-threshold levels. Upon violation of any one threshold, the output goes low. 式 3 provides the derivation of the low threshold voltage from the high threshold set by the DAC.

$$V_{THLD-LO} = V_{DAC} \times \left(\frac{R_2}{R_1 + R_2}\right) \quad (3)$$

To monitor a power supply of 5 V within ±10%, place the nominal value at the DAC midcode. The output range of the DACx3508 is 0 V to 5 V, thus the midcode voltage output is 2.5 V. Therefore, R_A and R_B are chosen so that the voltage to be compared is 2.5 V. For this example, R_A equals R_B; use 10-kΩ resistors for both. One channel of the DACx3508 must be programmed to $V_{THLD-HI}$ (for example, 2.5 V + 5% = 2.625 V). This result corresponds to a 10-bit DAC code of (2^{10} / 5 V) × 2.625 V = 537.6 (0x21Ah). To generate $V_{THLD-LO}$ (for example, 2.5 V – 5% = 2.405 V) from 2.625 V, the values of R_1 and R_2 are calculated as 7.5 kΩ and 82 kΩ, respectively, using 式 3.

The following pseudocode is provided to help get started with the programmable window comparator application at the desired DAC value.

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <DATA>
//Power-up the device and channels
WRITE DEVICE_CONFIG(0x01), 0x0000
//Program 2.625V on channel A
WRITE DACA_DATA(0x08), 0x0868 //10-bit MSB aligned
```

8.2.2.3 Application Curve

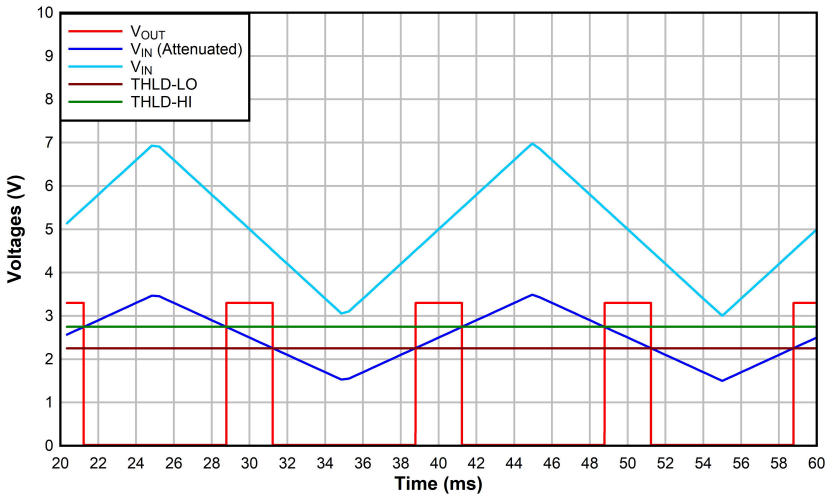


図 8-4. Programmable Comparator Output Waveform

8.3 Power Supply Recommendations

The DACx3508 family of devices does not require specific supply sequencing. These devices require a single power supply, V_{DD}. A 0.1-µF decoupling capacitor is recommended for the V_{DD} pin.

8.4 Layout

8.4.1 Layout Guidelines

The DACx3508 pinout separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate digital and analog traces and place decoupling capacitors close to the device pins.

8.4.2 Layout Example

図 8-5 shows an example layout drawing with decoupling capacitors and pullup resistors.

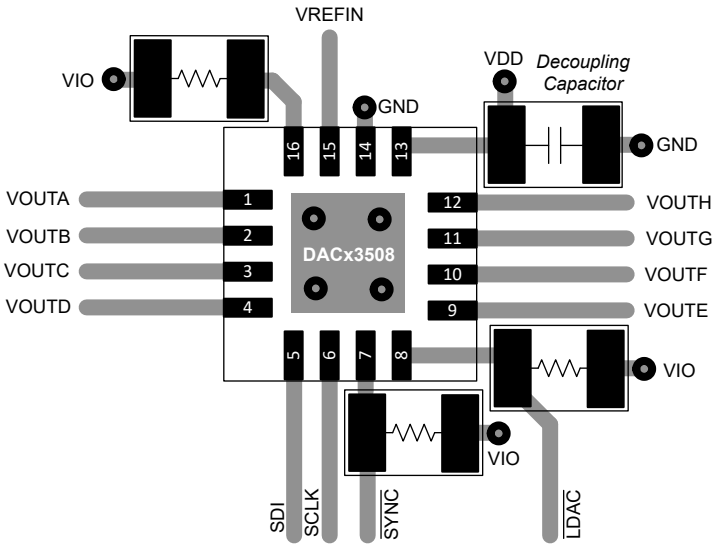


図 8-5. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *DAC53608EVM* user's guide

9.2 ドキュメントの更新通知を受け取る方法

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2023) to Revision A (May 2024)	Page
• DAC63508 とそれに関連する内容を追加	1
• 「特長」の最初の項目から INL を削除	1
• Added exceptions for "current into any pin" in the *Absolute Maximum Ratings*	4
• Updated footnotes in the *Electrical characteristics*	5
• Added 12-bit resolution in *Electrical Characteristics*	5
• Added INL data for 12-bit resolution in *Electrical Characteristics*	5
• Updated DAC codes in the test conditions for DC output impedance in the *Electrical Characteristics*	5
• Updated the reference input impedance value in the *Electrical Characteristics*	5
• Moved plots and updated section titles to better organize all *Typical Characteristics*	8
• Changed all plots to accommodate data for 12-bit resolution in all *Typical Characteristics*	8
• Added the resolution information to the header test conditions for all *Typical Characteristics*	8
• Updated plot test conditions for Figure 5-36, *Glitch Impulse, Rising Edge, 4-LSB Step*; Figure 5-37, *Glitch Impulse, Falling Edge, 4-LSB Step*; Figure 5-38, *Full-Scale Settling Time, Rising Edge*; Figure 5-39, *Full-Scale Settling Time, Falling Edge* in *Typical Characteristics: Dynamic Performance*	14

- Changed "end of SPI frame" to "24th rising-edge of the clock" in *DAC Register Update and $\overline{LDAC}$ Functionality* 19
- Changed from 12.5 kΩ to 24 kΩ in *Reference* 20
- Changed 0x1010 to 1010b in *Software Reset* 20
- Updated sentence to specify global power down current more accurately in *Power-Down Mode* 21
- Updated BRDCAST_DATA and DACn_DATA bits from B11 till B0 in the *Register Map* 22
- Changed Command Bits to Register Address in the *Register Map* table header 22
- Changed 1010 to 1010b in the *STATUS_TRIGGER Register* 23
- Updated B11:B0 to accommodate 12-bit resolution in the *DACn_DATA Register* 24

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC43508RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D43508
DAC43508RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D43508
DAC43508RTERG4.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D43508
DAC53508RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53508
DAC53508RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53508
DAC53508RTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53508
DAC53508RTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53508
DAC63508RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63508
DAC63508RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63508

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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TAPE AND REEL INFORMATION

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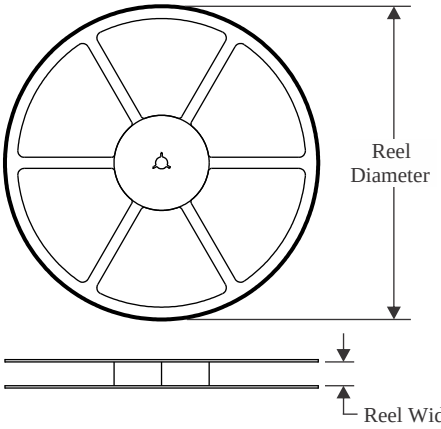
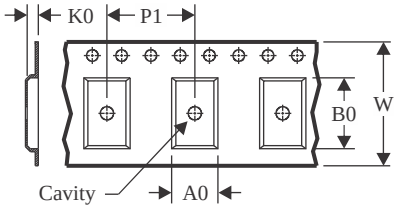
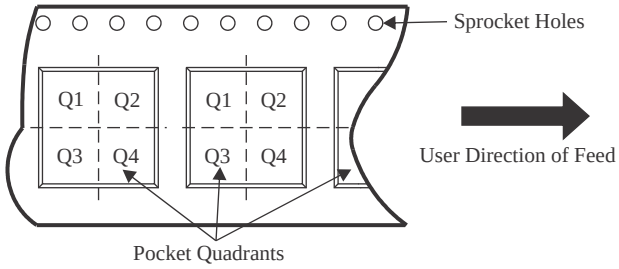


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

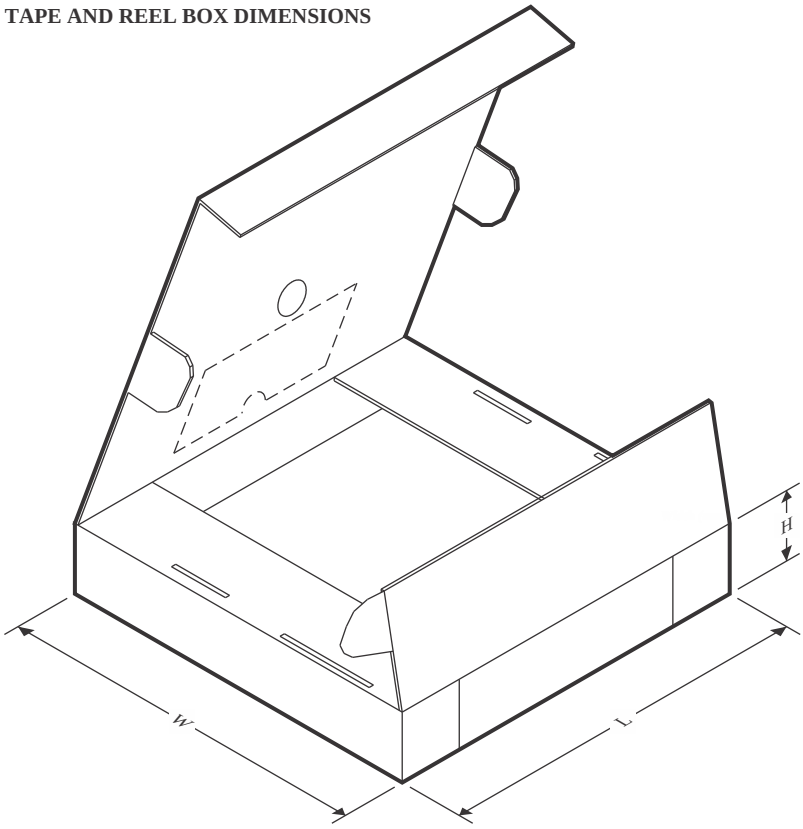
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC43508RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC53508RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC53508RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC63508RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC43508RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
DAC53508RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
DAC53508RTET	WQFN	RTE	16	250	210.0	185.0	35.0
DAC63508RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

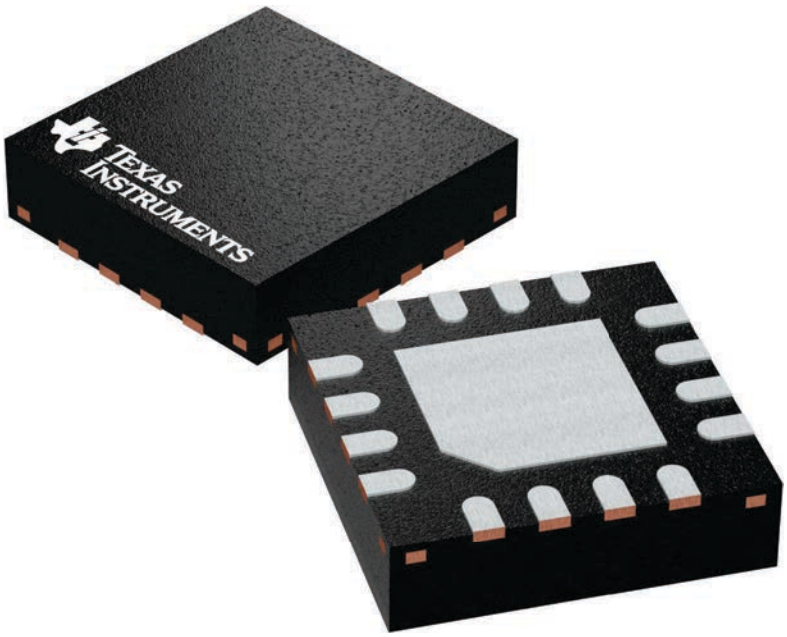
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

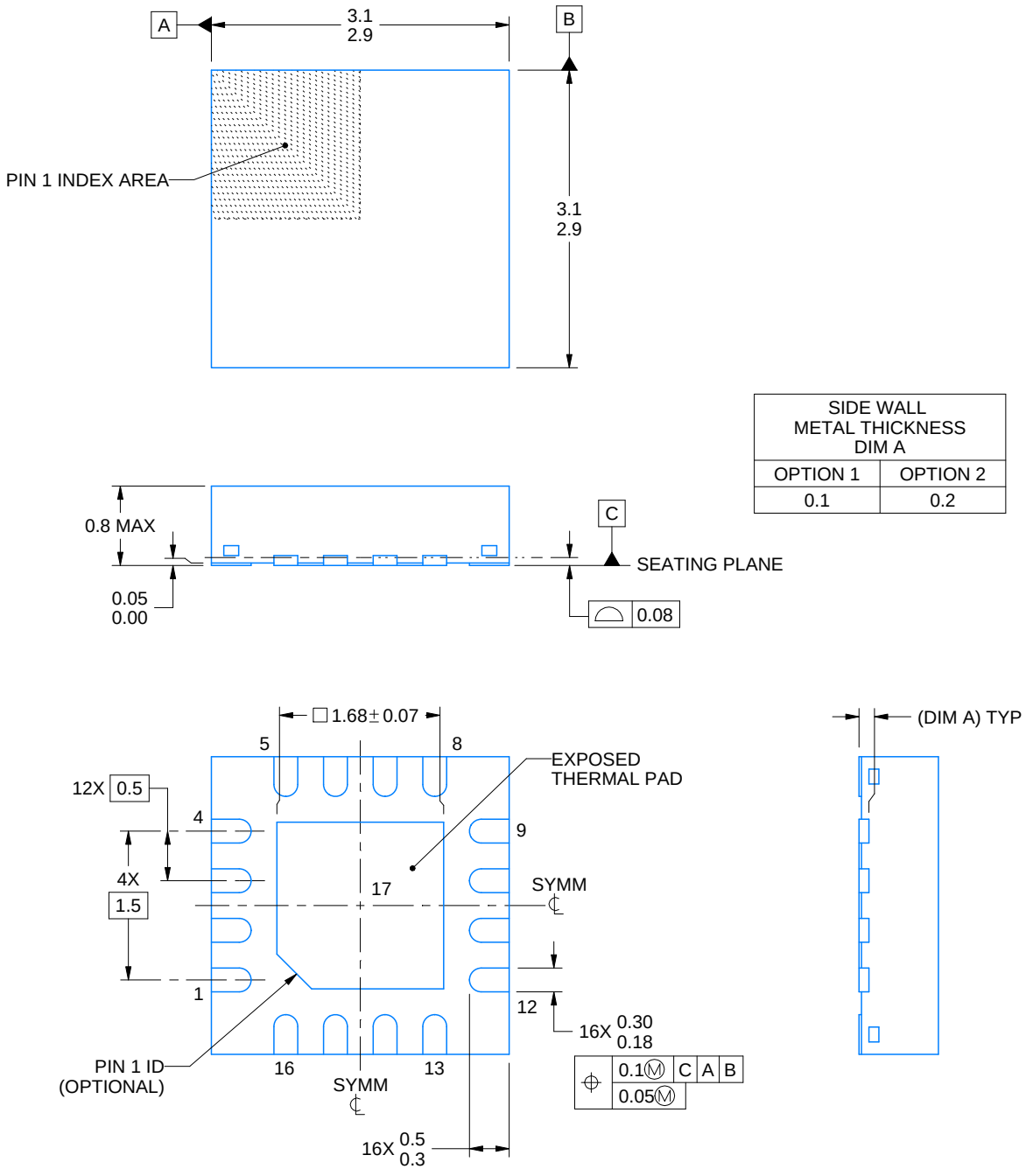


RTE0016C

PACKAGE OUTLINE

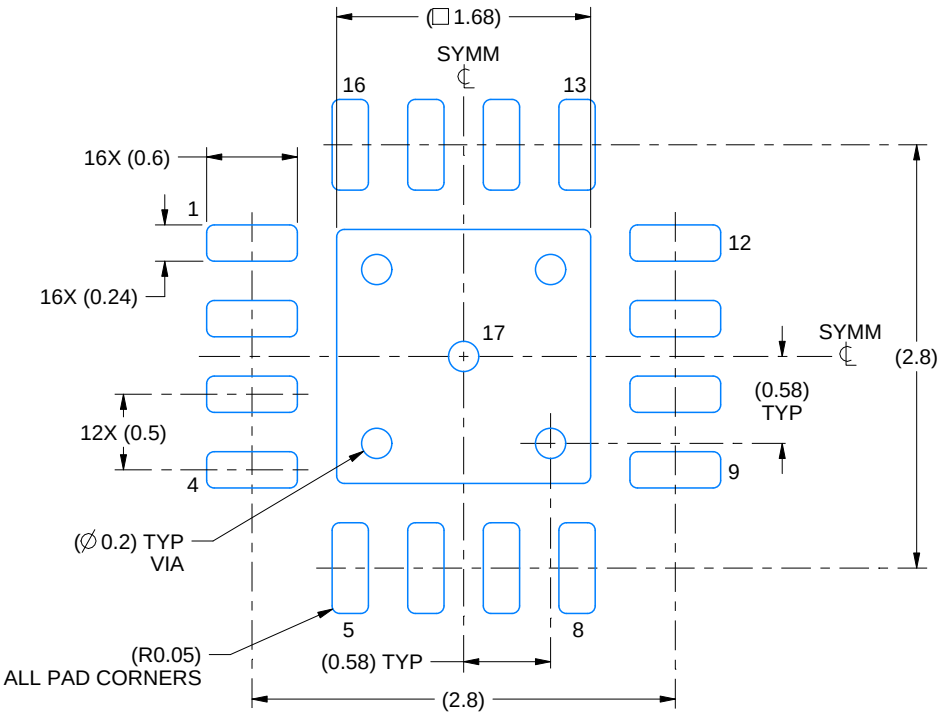
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

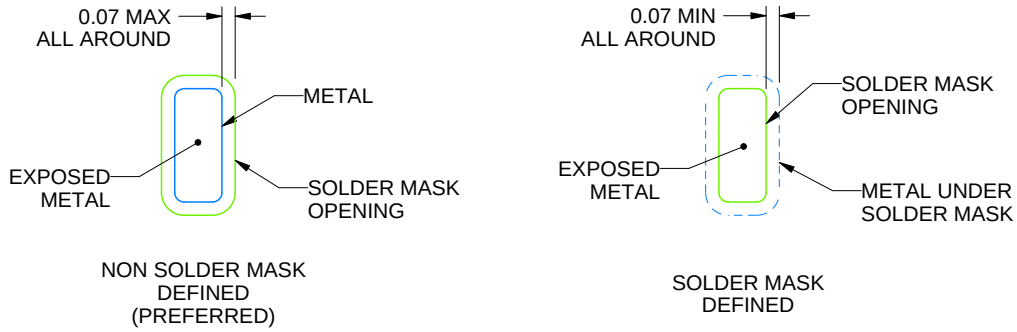


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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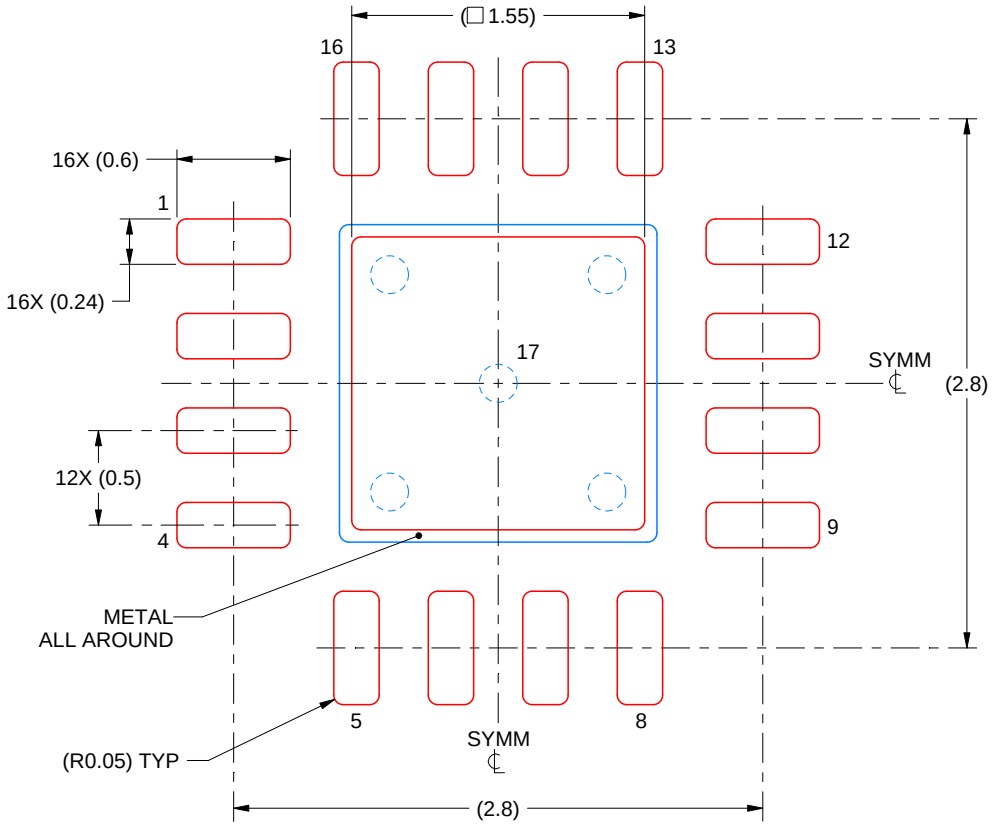
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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