DACx3701-Q1 不揮発性メモリと GPI 制御との PMBus™ 互換 I²C インターフェイスを搭載した車載用 10 ビットおよび 8 ビット、電圧出力スマート D/A コンバータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:–40℃~+125℃、T_A
- 1 LSB の INL と DNL (10 ビットおよび 8 ビット)
- 幅広い動作範囲
  - 電源:1.8V~5.5V
- 汎用入力 (GPI) ベースの機能トリガ
- PMBus™ 互換 I²C インターフェイス
  - Standard、Fast、Fast mode plus
  - ブロードキャスト・アドレスを使用して構成された 4 つのターゲット・アドレス・オプション
  - V_{IH}:1.62V (V_{DD} = 5.5V の場合)
- ユーザーがプログラム可能な不揮発性メモリ (NVM/EEPROM)
  - すべてのレジスタ設定の保存と復元
- プログラム可能な波形生成:方形波、三角波、のこぎり波
- 三角波と FB ピンを使用するパルス幅変調 (PWM) 出力
- デジタル・スルーレート制御
- 内部リファレンス
- 超低消費電力:1.8V で 0.2mA
- 柔軟な起動:ハイ・インピーダンスまたは 10K-GND
- 超小型パッケージ:8 ピン WSON (2mm × 2mm)

2 アプリケーション

- リア・ライト
- ヘッドライト
- 室内灯

3 概要

車載用 10 ビットの DAC53701-Q1 および 8 ビットの DAC43701-Q1 (DACx3701-Q1) は、バッファ付き、電圧出力のスマート D/A コンバータ (DAC) のピン互換ファミリです。これらのデバイスは消費電力が非常に小さく、超小型の 8 ピン WSON パッケージで供給されます。機能セットが小型パッケージや低消費電力と組み合わされている DACx3701-Q1 は、車載用テール・ライト + ブレーキ・ライト、ナンバー・プレート・ライトのフェードイン・フェードアウト、車内照明用の PWM 拡張などのアプリケーションに最適です。

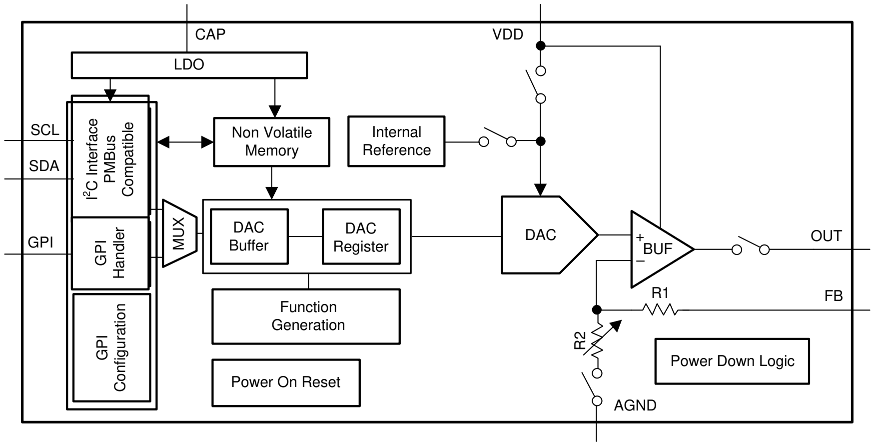
これらのデバイスは不揮発性メモリ (NVM)、内部リファレンス、PMBus 互換の I²C インターフェイス、および汎用入力を備えています。DACx3701-Q1 は、内部リファレンスまたは電源をリファレンスとして使用して動作し、1.8 V~5.5 V のフルスケール出力を実現します。

DACx3701-Q1 は、高度な統合機能を備えたスマート DAC デバイスです。フォース・センス出力、GPI ベースの機能トリガ、PWM 出力、NVM 機能を備えたスマート DAC は、ソフトウェアを使用せずにシステム性能と制御を実現します。

製品情報

部品番号	分解能	パッケージ (1) (2)
DAC53701-Q1	10 ビット	DSG (WSON、8) 2mm × 2mm
DAC43701-Q1	8 ビット	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。


CAP
VDD
LDO
SCL
SDA
GPI
I2C Interface PMBus Compatible
GPI Handler
GPI Configuration
MUX
Non Volatile Memory
Internal Reference
DAC Buffer
DAC Register
Function Generation
Power On Reset
DAC
BUF
OUT
R1
FB
R2
Power Down Logic
AGND

機能ブロック図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2020) to Revision A (September 2023)	Page
• DACx3701-Q1 デバイスを事前情報 (プレビュー) から量産データ (アクティブ) に変更	1
• I^2C および PMBus に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更	1

5 Pin Configuration and Functions

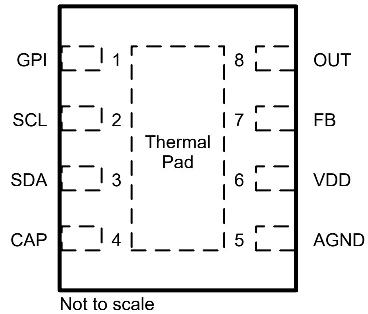


図 5-1. DSG Package, 8-Pin WSON (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GPI	Input	General-purpose input.
2	SCL	Input	Serial interface clock. This pin must be connected to the supply voltage with an external pullup resistor.
3	SDA	Input/Output	Data are clocked into or out of the input register. This pin is a bidirectional, and must be connected to the supply voltage with an external pullup resistor.
4	CAP	Input	External capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
5	AGND	Ground	Ground reference point for all circuitry on the device.
6	VDD	Power	Analog supply voltage: 1.8 V to 5.5 V
7	FB	Input	Voltage-feedback pin.
8	OUT	Output	Analog output voltage from DAC.
—	Thermal Pad	Ground	Connect the thermal pad to AGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to AGND	–0.3	6	V
	Digital inputs to AGND	–0.3	V_{DD} + 0.3	V
	V_{FB} to AGND	–0.3	V_{DD} + 0.3	V
	V_{OUT} to AGND	–0.3	V_{DD} + 0.3	V
	Current into any pin except the OUT, VDD, and AGND pins	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)] HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (AGND)	1.71		5.5	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		DACx3701-Q1	UNIT
		DSG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report*.

6.5 Electrical Characteristics

all minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C; typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC53701-Q1	10			Bits
		DAC43701-Q1	8			
INL	Relative accuracy(1)		–1		1	LSB
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error	Code 0d into DAC, external reference, V_{DD} = 5.5 V		6	12	mV
		Code 0d into DAC, internal reference, gain = 4 ×, V_{DD} = 5.5 V		6	15	
	Zero-code-error temperature coefficient			±10		µV/°C
	Offset error(2)		–0.6	0.25	0.6	%FSR
	Offset-error temperature coefficient(2)			±0.0003		%FSR/°C
	Gain error(2)		–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(2)			±0.0008		%FSR/°C
	Full-scale error	1.8 V ≤ V_{DD} < 2.7 V, code 1023d into DAC for 10-bit resolution, code 255d into DAC for 8-bit resolution, no headroom	–1	0.5	1	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, code 1023d into DAC for 10-bit resolution, code 255d into DAC for 8-bit resolution, no headroom	–0.5	0.25	0.5	
	Full-scale-error temperature coefficient			±0.0008		%FSR/°C
OUTPUT CHARACTERISTICS						
	Output voltage	Reference tied to V_{DD}	0		5.5	V
C_L	Capacitive load(3)	R_L = Infinite, phase margin = 30°			1	nF
		R_L = 5 kΩ, phase margin = 30°			2	
	Load regulation	DAC at midscale, –10 mA ≤ I_{OUT} ≤ 10 mA, V_{DD} = 5.5 V		0.4		mV/mA
	Short circuit current	V_{DD} = 1.8 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		10		mA
		V_{DD} = 2.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		25		
		V_{DD} = 5.5 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		50		
	Output voltage headroom(1)	To V_{DD}, DAC output unloaded, internal reference = 1.21 V, V_{DD} ≥ 1.21 × gain + 0.2 V	0.2			V
		To V_{DD}, DAC output unloaded, reference tied to V_{DD}	0.8			%FSR
		To V_{DD}, I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V, DAC code = full scale	10			
	V_{OUT} dc output impedance	DAC output enabled and DAC code = midscale		0.25		Ω
		DAC output enabled and DAC code = 8d for 10-bit resolution and code = 2d for 8-bit resolution		0.25		
		DAC output enabled and DAC code = 1016d for 10-bit resolution and code = 254d for 8-bit resolution		0.26		

6.5 Electrical Characteristics (続き)

all minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C; typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_O	V_{FB} dc output impedance(4)	DAC output enabled, DAC reference tied to VDD (gain = 1 ×) or internal reference (gain = 1.5 × or 2 ×)	160	200	240	kΩ
		DAC output enabled, internal V_{REF}, gain = 3 × or 4 ×	192	240	288	
	V_{OUT} + V_{FB} dc output leakage(3)	At start up, measured when DAC output is disabled and held at V_{DD} / 2 for V_{DD} = 5.5 V			7	nA
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2 ×, DAC at midscale; V_{DD} = 5 V ±10%		0.25		mV/V
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		8		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4 ×		12		
	Slew rate	V_{DD} = 5.5 V		1		V/µs
	Power-on glitch magnitude	At start-up, DAC output disabled, R_L = 5 kΩ, C_L = 200 pF		75		mV
		At start-up, DAC output disabled, R_L = 100 kΩ		200		
	Output enable glitch magnitude	DAC output disabled to enabled, DAC registers at zero scale, R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		34		μV_{PP}
		Internal V_{REF}, gain = 4 ×, 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		70		
	Output noise density	Measured at 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.2		µV/√Hz
		Internal V_{REF}, gain = 4 ×, measured at 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.7		
	Power supply rejection ratio (ac)(4)	Internal V_{REF}, gain = 4 ×, 200-mV 50-Hz or 60-Hz sine wave superimposed on power supply voltage, DAC at midscale		–71		dB
	Code change glitch impulse	±1-LSB change around midcode (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1-LSB change around midcode (including feedthrough)		15		mV
	Function generator TIME-STEP accuracy			±6.25		%
VOLTAGE REFERENCE						
	Initial accuracy			1.212		V
	Reference output temperature coefficient(3)				65	ppm/°C
EEPROM						
	Endurance(3)	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A > 85°C		1000		
	Data retention(3)			50		Years
		T_A = 125°C		20		
	EEPROM programming write cycle time(3)		10		20	ms
DIGITAL INPUTS						
	Digital feedthrough	DAC output static at midscale, fast-mode plus, SCL toggling		20		nV-s

6.5 Electrical Characteristics (続き)

all minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C; typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Pin capacitance	Per pin		10		pF

6.5 Electrical Characteristics (続き)

all minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C; typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
	Load capacitor - CAP pin[3]		0.5		15	µF
I_{DD}	Current flowing into VDD	Normal mode, DACs at full scale, digital pins static		0.225	0.55	mA
		DAC power down, internal reference power down		80		µA

(1) Measured with DAC output unloaded. For external reference between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution. For internal reference V_{DD} ≥ 1.21 × gain + 0.2 V, between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution.
(2) Measured with DAC output unloaded. For 10-bit resolution, between end-point codes: 8d to 1016d and for 8-bit resolution, between end-point codes: 2d to 254d.
(3) Specified by design and characterization, not production tested.
(4) Specified with 200-mV headroom with respect to reference value when internal reference is used.

6.6 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			0.1	MHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns

6.7 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			0.4	MHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns

6.8 Timing Requirements: I²C Fast-Mode Plus

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull\text{-}up}$ ≤ V_{DD} V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns

6.9 Timing Requirements: GPI

all input signals are timed from VIL to 70% of V_{DD}. 1.8 V ≤ V_{DD} ≤ 5.5 V and –40°C ≤ T_A ≤ +125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{GPIDELAY}$	GPI edge to start of operation delay, 1.7 V ≤ V_{DD} ≤ 5.5 V[(1)]		2		µs

(1) The maximum value specified for $t_{GPIDELAY}$ in the timing table is in addition to 2x SLEW_RATE for margin-high, low and function generation operations. The maximum value for the total delay is (2xSLEW_RATE + $t_{GPIDELAY}$).

6.10 Timing Diagram

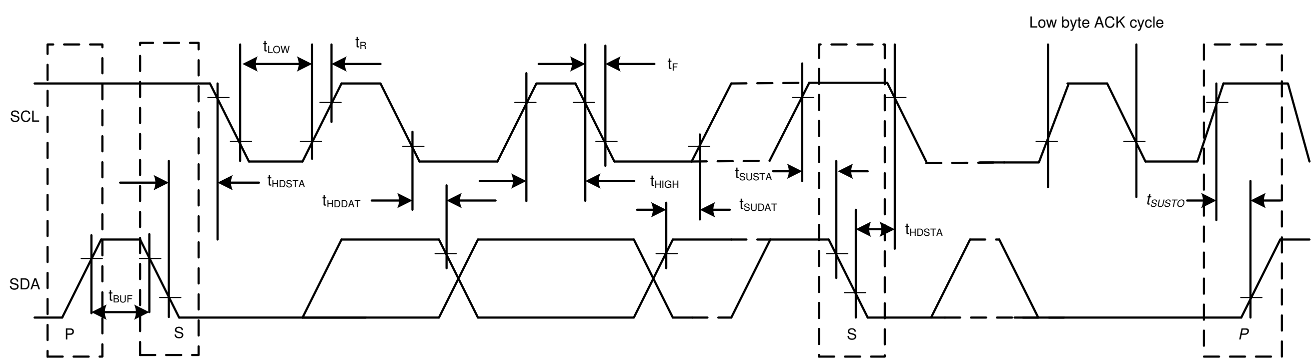


図 6-1. I²C Timing Diagram

6.11 Typical Characteristics: V_{DD} = 5.5 V (Reference = V_{DD}) or V_{DD} = 5 V (Internal Reference)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)

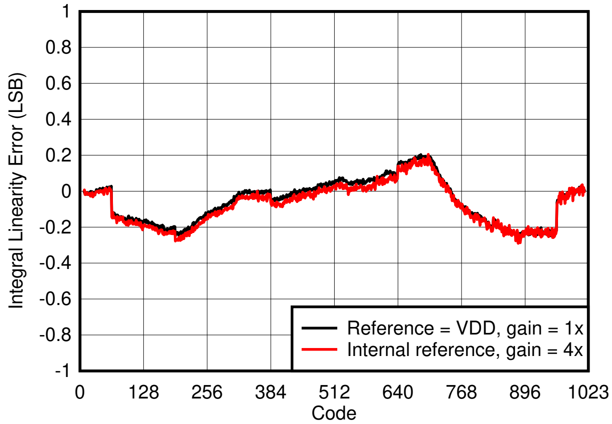


図 6-2. Integral Linearity Error vs Digital Input Code

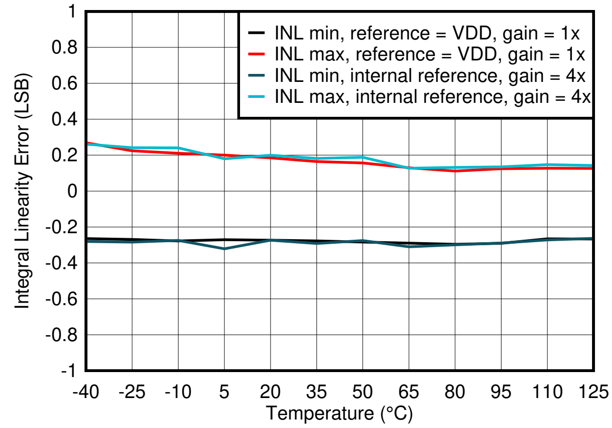


図 6-3. Integral Linearity Error vs Temperature

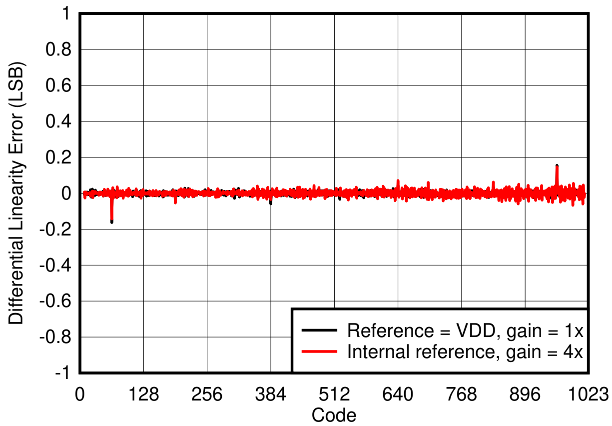


図 6-4. Differential Linearity Error vs Digital Input Code

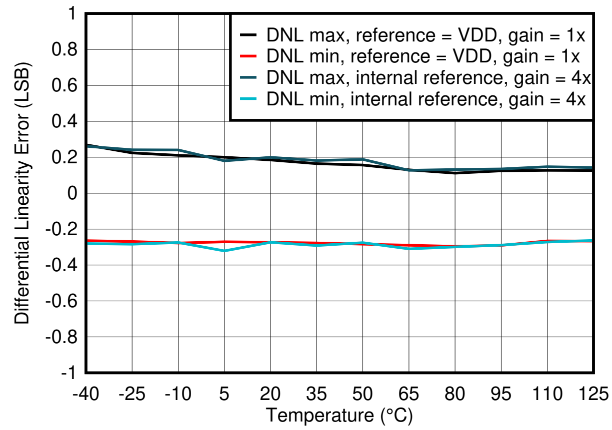


図 6-5. Differential Linearity Error vs Temperature

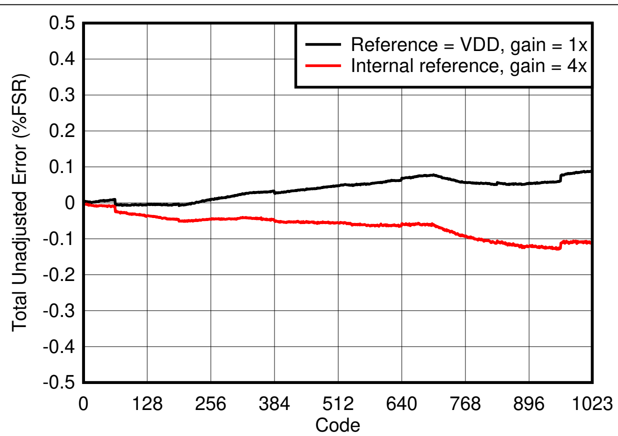


図 6-6. Total Unadjusted Error vs Digital Input Code

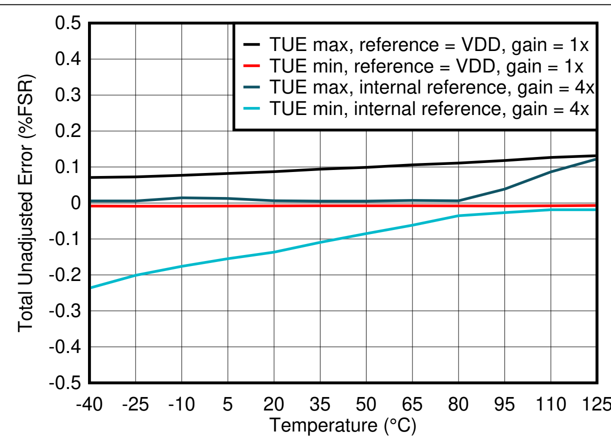
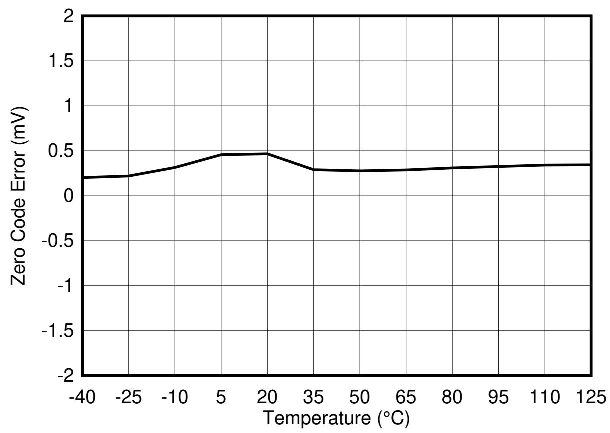


図 6-7. Total Unadjusted Error vs Temperature

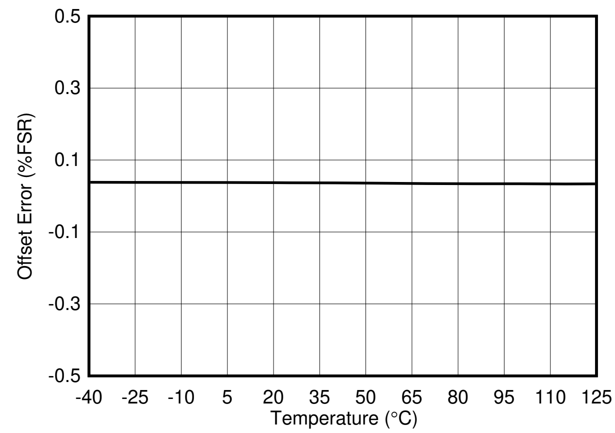
6.11 Typical Characteristics: V_{DD} = 5.5 V (Reference = V_{DD}) or V_{DD} = 5 V (Internal Reference) (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD}

図 6-8. Zero Code Error vs Temperature



Reference = V_{DD}

図 6-9. Offset Error vs Temperature

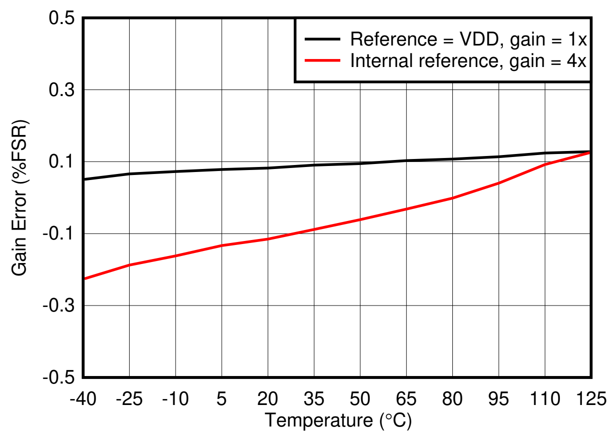


図 6-10. Gain Error vs Temperature

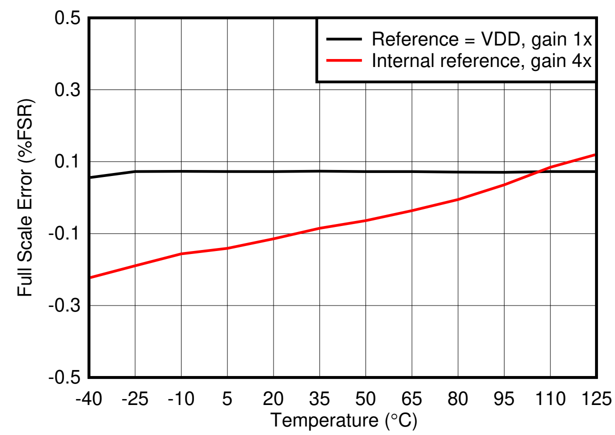


図 6-11. Full-Scale Error vs Temperature

6.12 Typical Characteristics: V_{DD} = 1.8 V (Reference = V_{DD}) or V_{DD} = 2 V (Internal Reference)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)

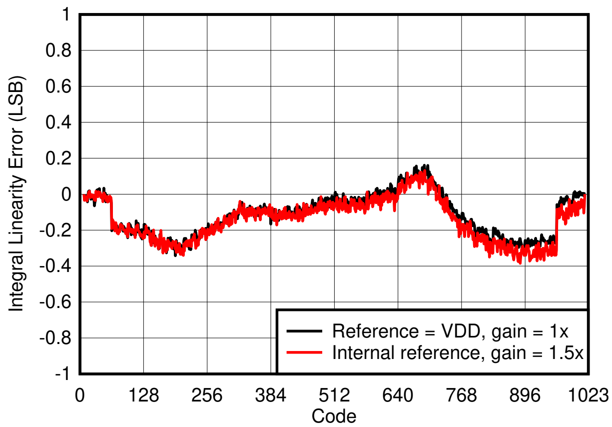


図 6-12. Integral Linearity Error vs Digital Input Code

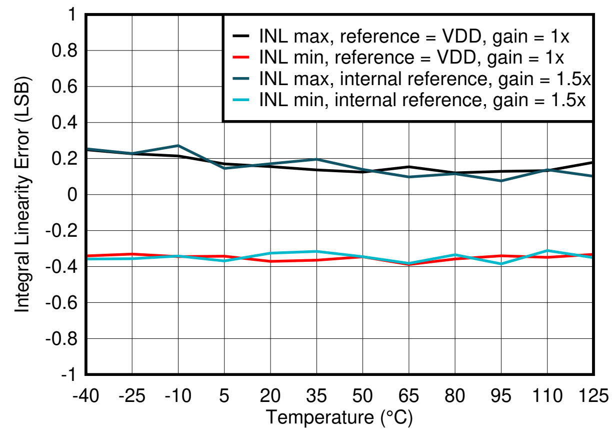


図 6-13. Integral Linearity Error vs Temperature

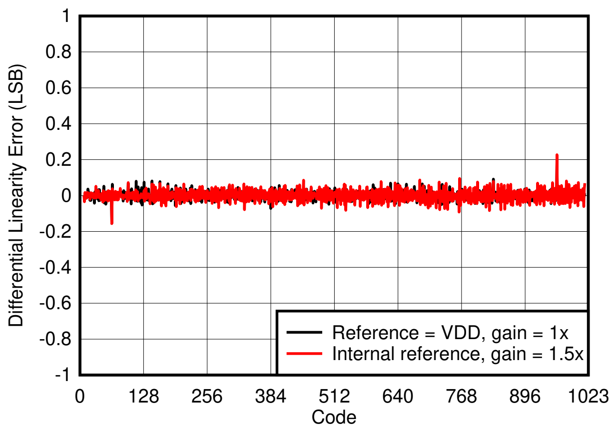


図 6-14. Differential Linearity Error vs Digital Input Code

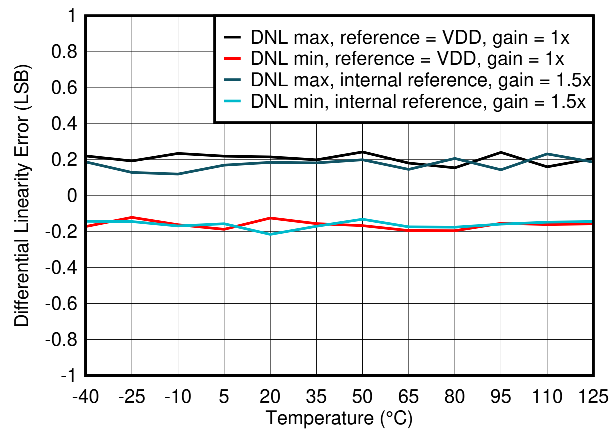


図 6-15. Differential Linearity Error vs Temperature

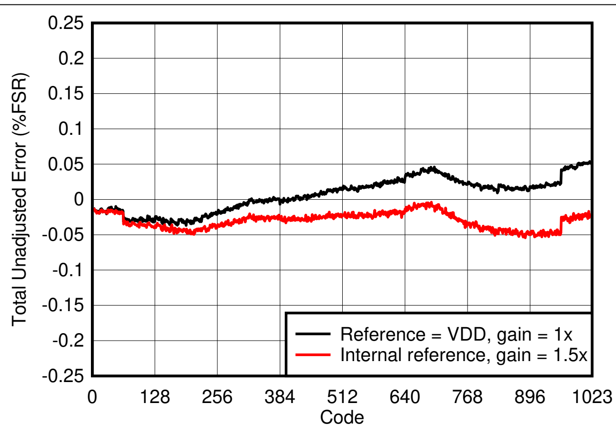


図 6-16. Total Unadjusted Error vs Digital Input Code

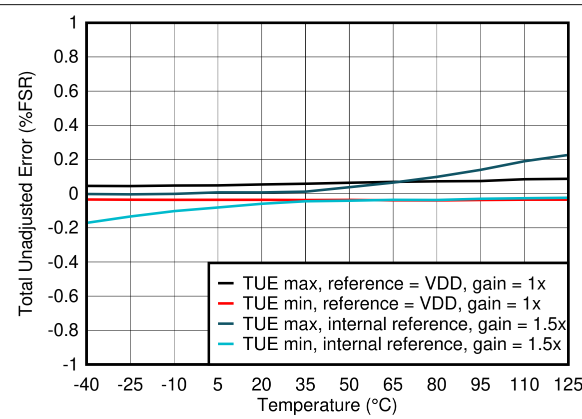
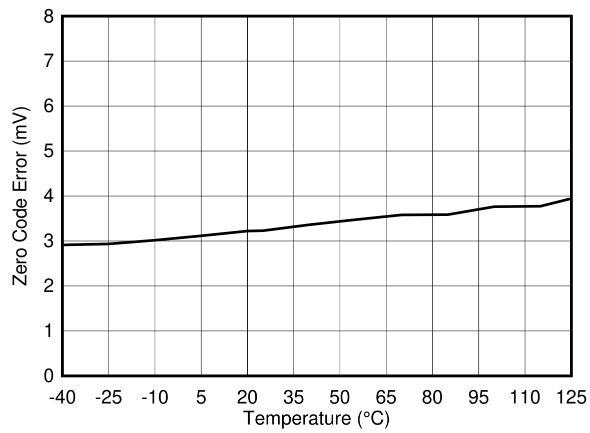


図 6-17. Total Unadjusted Error vs Temperature

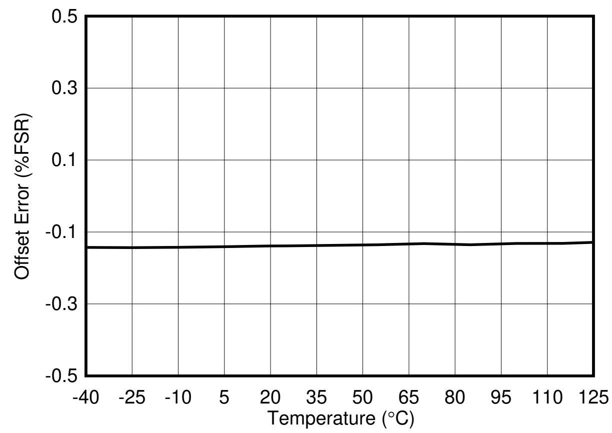
6.12 Typical Characteristics: V_{DD} = 1.8 V (Reference = V_{DD}) or V_{DD} = 2 V (Internal Reference) (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD}

図 6-18. Zero Code Error vs Temperature



Reference = V_{DD}

図 6-19. Offset Error vs Temperature

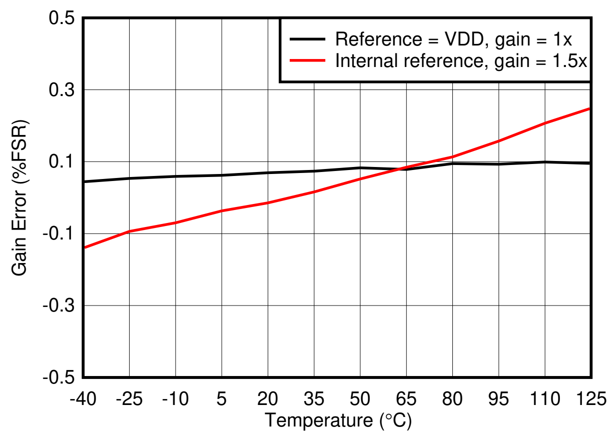


図 6-20. Gain Error vs Temperature

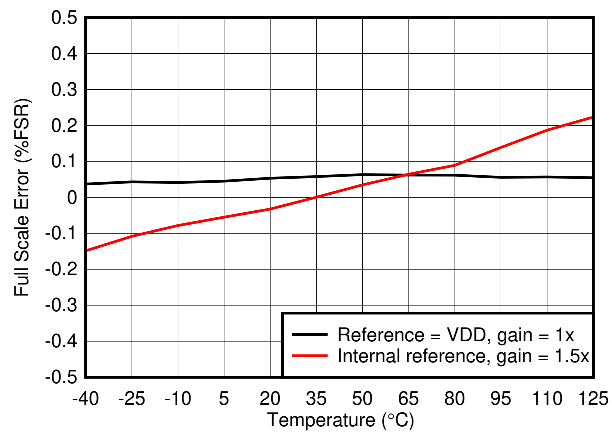
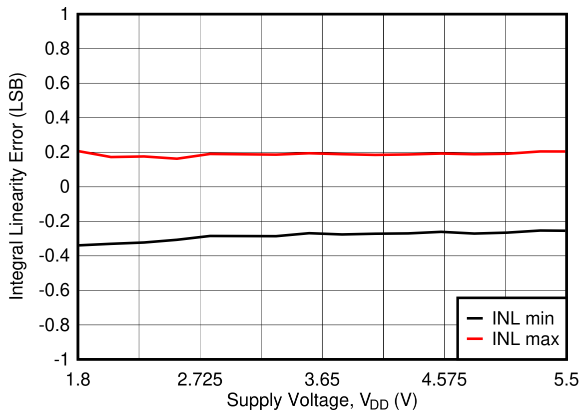


図 6-21. Full-Scale Error vs Temperature

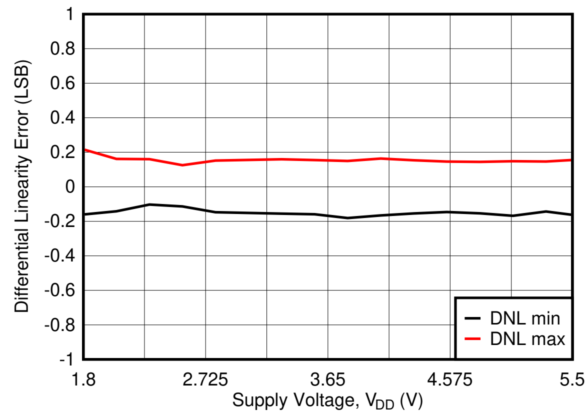
6.13 Typical Characteristics

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



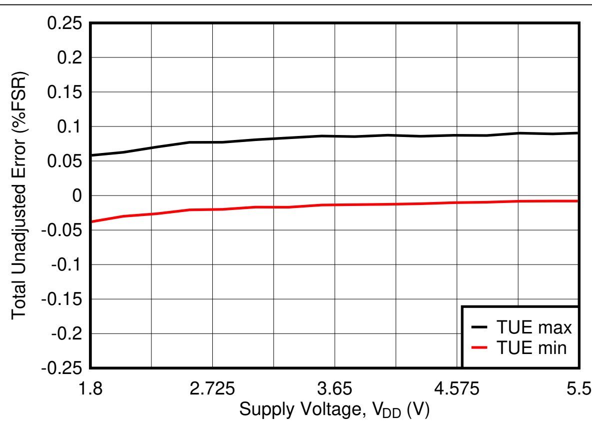
Reference = V_{DD}

図 6-22. Integral Linearity Error vs Supply Voltage



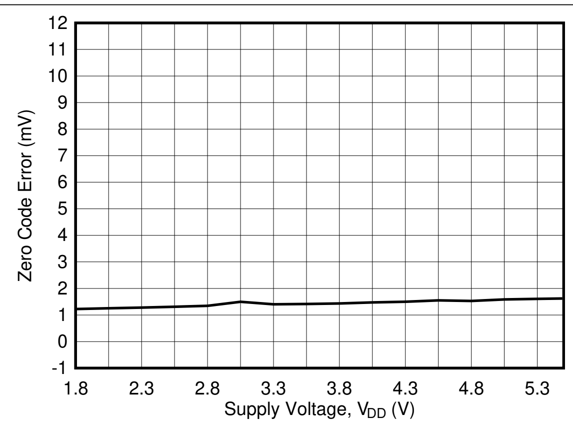
Reference = V_{DD}

図 6-23. Differential Linearity Error vs Supply Voltage



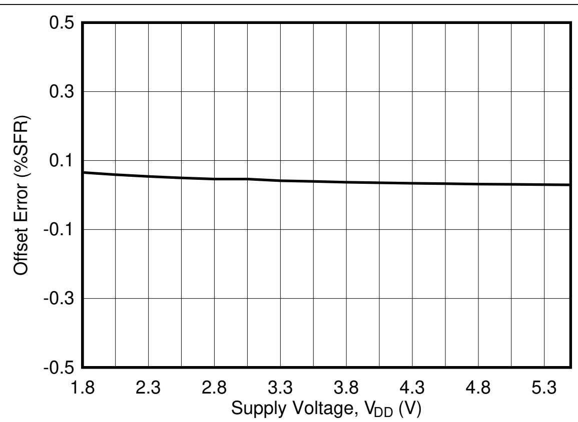
Reference = V_{DD}

図 6-24. Total Unadjusted Error vs Supply Voltage



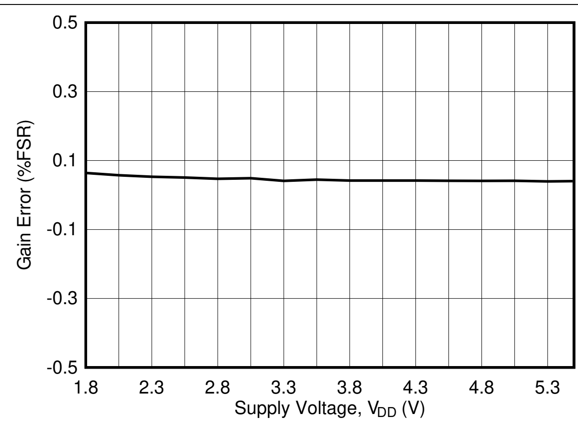
Reference = V_{DD}

図 6-25. Zero-Code Error vs Supply Voltage



Reference = V_{DD}

図 6-26. Offset Error vs Supply Voltage

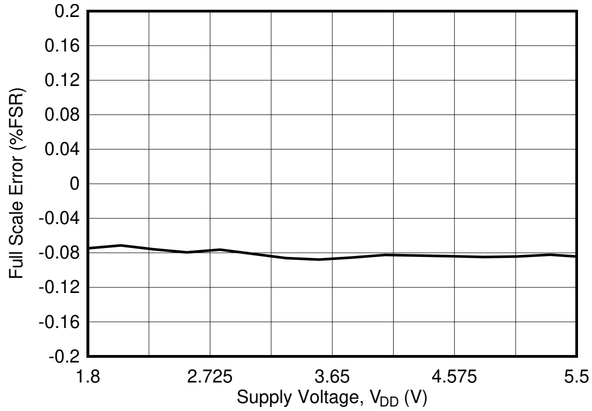


Reference = V_{DD}

図 6-27. Gain Error vs Supply Voltage

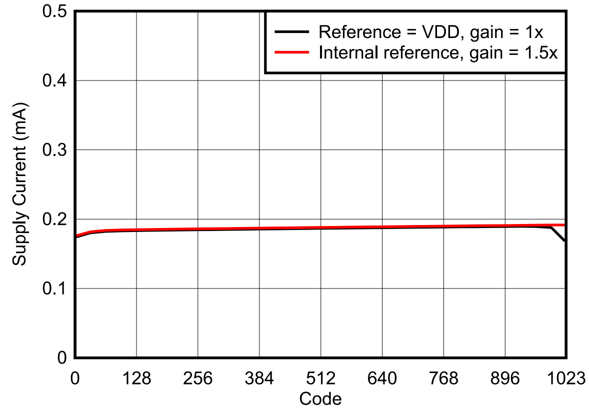
6.13 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



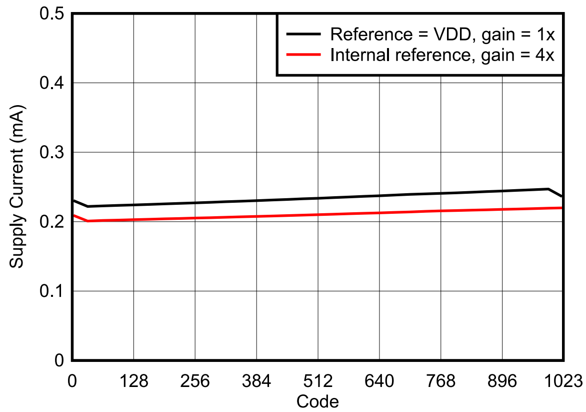
Reference = V_{DD}

図 6-28. Full-Scale Error vs Supply Voltage



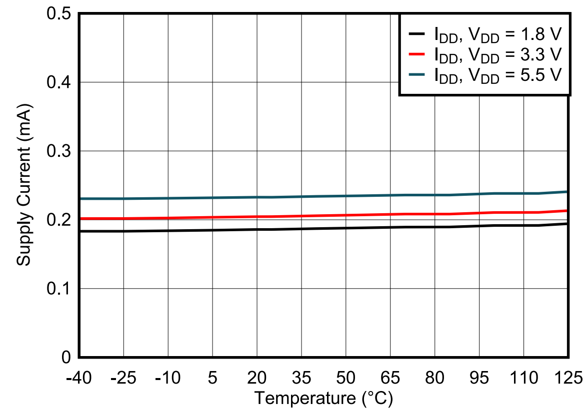
V_{DD} = 1.8 V

図 6-29. Supply Current vs Digital Input Code



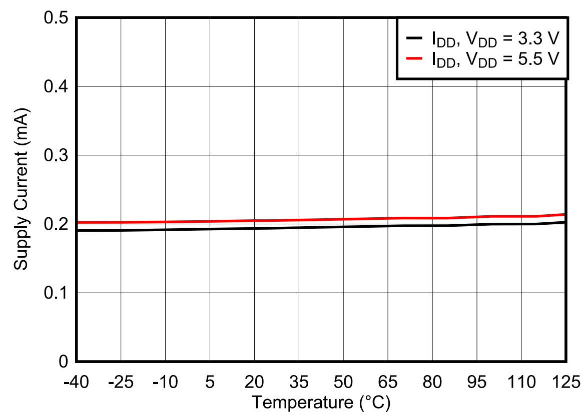
V_{DD} = 5.5 V

図 6-30. Supply Current vs Digital Input Code



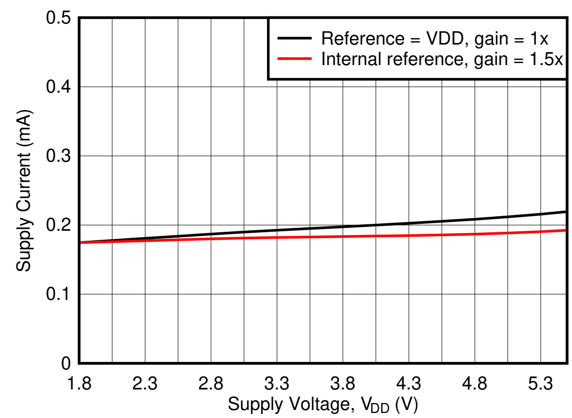
Reference = V_{DD}, DAC at midscale

図 6-31. Supply Current vs Temperature



Internal reference (gain = 4 ×), DAC at midscale

図 6-32. Supply Current vs Temperature

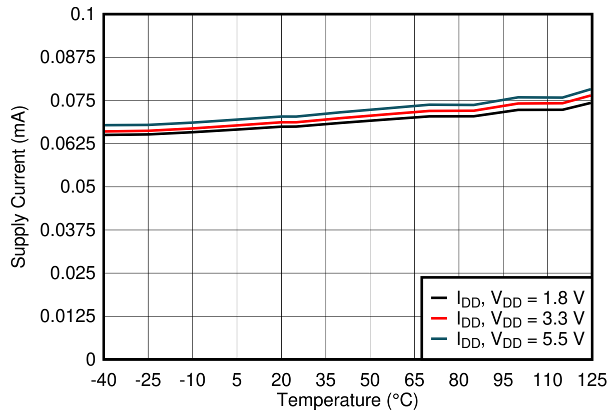


DAC at midscale

図 6-33. Supply Current vs Supply Voltage

6.13 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD}, DAC powered down

図 6-34. Power-Down Current vs Temperature

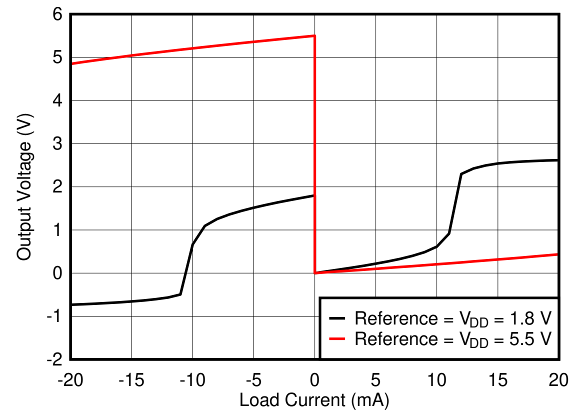
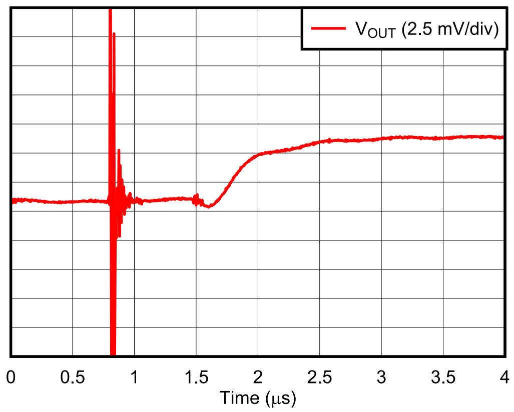
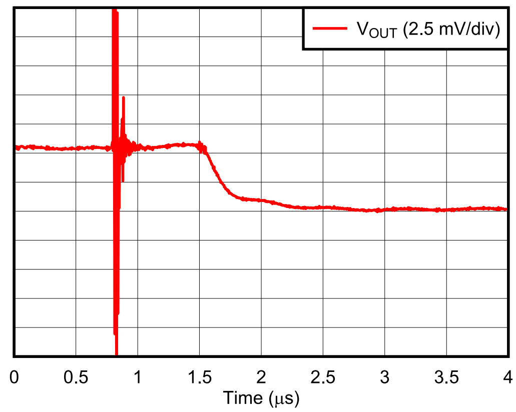


図 6-35. Source and Sink Capability



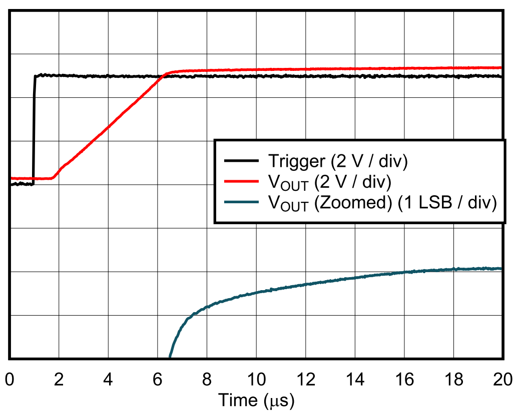
Reference = V_{DD} = 5.5 V, DAC code transition from midscale to midscale + 1 LSB, DAC load = 5 kΩ || 200 pF

図 6-36. Glitch Impulse, Rising Edge, 1-LSB Step



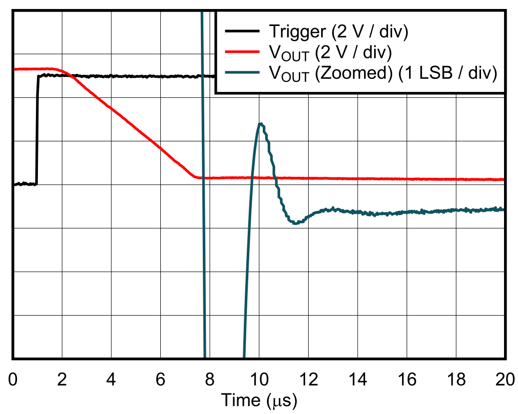
Reference = V_{DD} = 5.5 V, DAC code transition from midscale to midscale – 1 LSB, DAC load = 5 kΩ || 200 pF

図 6-37. Glitch Impulse, Falling Edge, 1-LSB Step



Reference = V_{DD} = 5.5 V, DAC load = 5 kΩ || 200 pF

図 6-38. Full-Scale Settling Time, Rising Edge

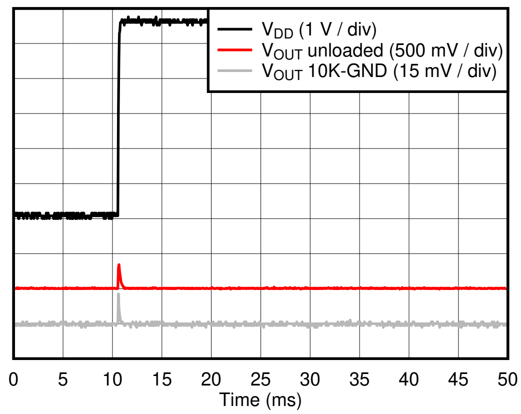


Reference = V_{DD} = 5.5 V, DAC load = 5 kΩ || 200 pF

図 6-39. Full-Scale Settling Time, Falling Edge

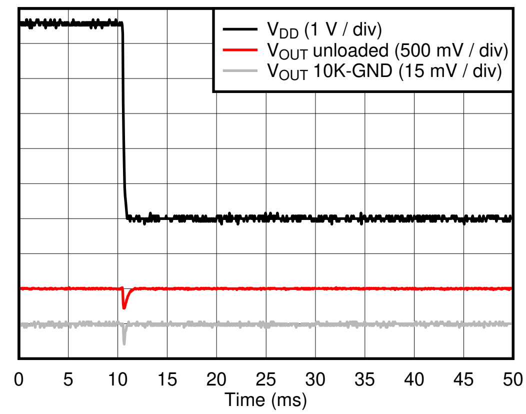
6.13 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



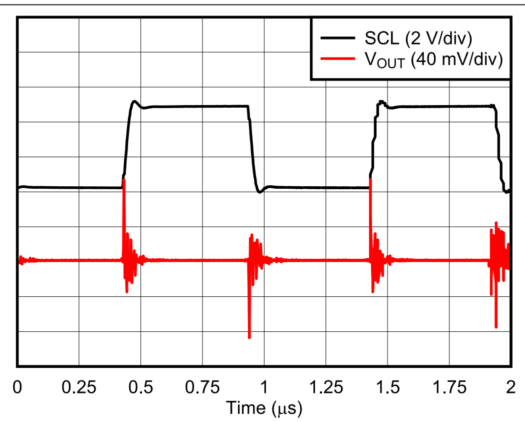
Reference = V_{DD} = 5.5 V

図 6-40. Power-on Glitch



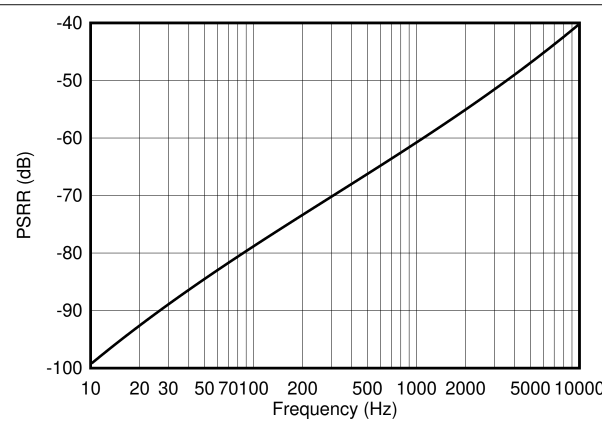
Reference = V_{DD} = 5.5 V

図 6-41. Power-off Glitch



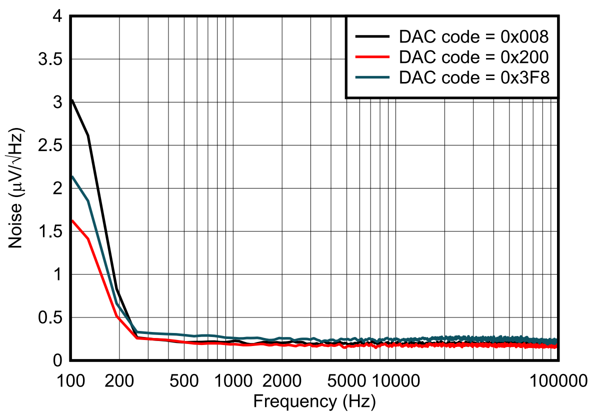
Reference = V_{DD} = 5.5 V, fast-mode plus, DAC at midscale, DAC load = 5 kΩ || 200 pF

図 6-42. Clock Feedthrough



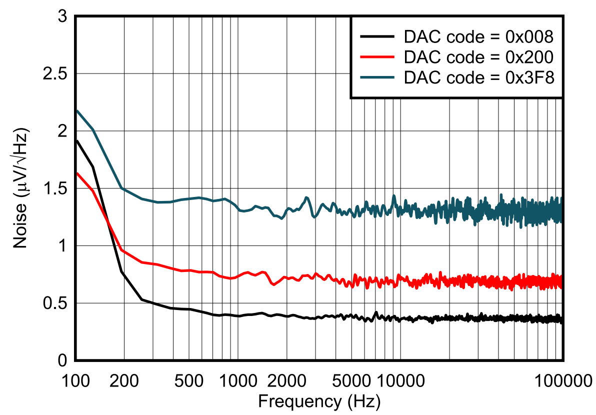
Internal reference (gain = 4 ×), V_{DD} = 5.25 V + 0.25 V_{PP}, DAC at midscale, DAC load = 5 kΩ || 200 pF

図 6-43. DAC Output AC PSRR vs Frequency



Reference = V_{DD} = 5.5 V

図 6-44. DAC Output Noise Spectral Density

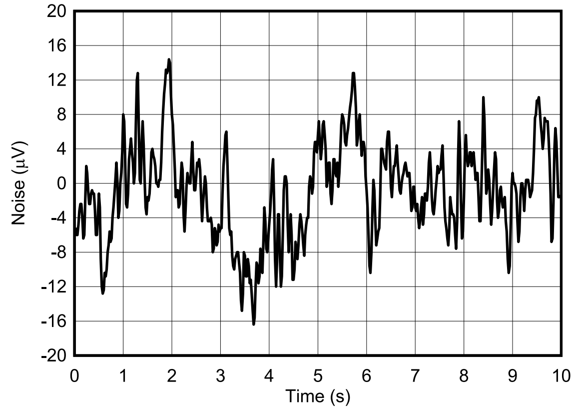


Internal reference (gain = 4 ×), V_{DD} = 5.5 V

図 6-45. DAC Output Noise Spectral Density

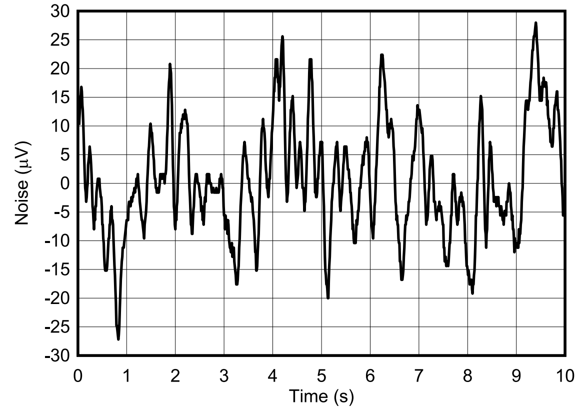
6.13 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD} = 5.5 V, DAC at midscale

図 6-46. DAC Output Noise: 0.1 Hz to 10 Hz



Internal reference (gain = 4 ×), V_{DD} = 5.5 V, DAC at midscale

図 6-47. DAC Output Noise: 0.1 Hz to 10 Hz

7 Detailed Description

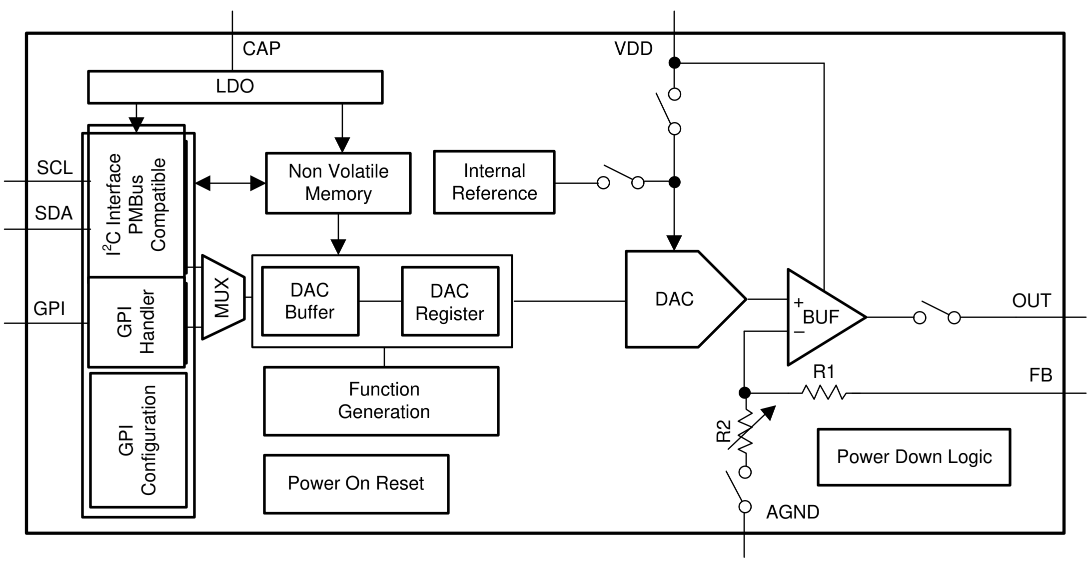
7.1 Overview

The 10-bit DAC53701-Q1 and 8-bit DAC43701-Q1 (DACx3701-Q1) are a pin-compatible family of automotive, buffered voltage-output, smart digital-to-analog converters (DACs). These smart DACs contain nonvolatile memory (NVM), an internal reference, a PMBus-compatible I^2C interface, force-sense output, and a general-purpose input. The DACx3701-Q1 operate with either an internal reference or with a power supply as the reference, and provide a full-scale output of 1.8 V to 5.5 V.

These devices communicate through an I^2C interface, and support I^2C standard mode (100Kbps), fast mode (400Kbps), and fast-mode plus (1Mbps). These devices also support specific PMBus commands such as *turn on/off*, *margin high or low*, and more. The GPI input can be configured as a power-down trigger, margin-high-low, and function trigger. The DACx3701-Q1 also include digital slew rate control, and support basic signal generation such as *square*, *ramp*, and *sawtooth* waveforms. These devices can generate pulse-width modulation (PWM) output with the combination of the triangular or sawtooth waveform and the FB pin. These features enable the DACx3701-Q1 to go beyond the limitations of a conventional DAC that depends on a processor to function. Because of processor-less operation and the *smart* feature set, the DACx3701-Q1 are called smart DACs.

The DACx3701-Q1 have a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The DAC output powers on in high-impedance mode (default); this setting can be programmed to 10kΩ-GND using NVM.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital-to-Analog Converter (DAC) Architecture

The DACx3701-Q1 family of devices consists of string architecture with an output buffer amplifier. セクション 7.2 shows the DAC architecture within the block diagram. This DAC architecture operates from a 1.8-V to 5.5-V power supply. These devices consume only 0.2 mA of current when using a 1.8-V power supply. The DAC output pin starts up in high-impedance mode, making these devices an excellent choice for power-supply control applications. To change the power-up mode to 10kΩ-GND, program the DAC_PDN bit (address: D1h), and load these bits in the device NVM. The DACx3701-Q1 devices include a *smart* feature set to enable processor-less operation and high-integration. The NVM enables a predictable start up. The GPI triggers the DAC output without the I^2C interface in the absence of a processor or when the processor or software fails. The integrated functions and the FB pin enable PWM output for control applications. The FB pin enables this device to be used as a programmable comparator. The digital slew rate control and the Hi-Z power-down modes enable a hassle-free voltage margining and function.

7.3.1.1 Reference Selection and DAC Transfer Function

The device writes the input data to the DAC data registers in straight-binary format. After a power-on or a reset event, the device sets all DAC registers to the values set in the NVM.

7.3.1.1.1 Power Supply as Reference

By default, the DACx3701-Q1 operate with the power-supply pin (VDD) as a reference. 式 1 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1x.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \tag{1}$$

where:

- N is the resolution in bits, either 8 (DAC43701-Q1) or 10 (DAC53701-Q1).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{DD} is used as the DAC reference voltage.

7.3.1.1.2 Internal Reference

The DACx3701-Q1 also contain an internal reference that is disabled by default. Enable the internal reference by writing 1 to REF_EN (address D1h). The internal reference generates a fixed 1.21-V voltage (typical). Using DAC_SPAN (address D1h) bits, gain of 1.5 ×, 2 ×, 3 ×, 4 × can be achieved for the DAC output voltage (V_{OUT}) 式 2 shows DAC transfer function when the internal reference is used.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \tag{2}$$

where:

- N is the resolution in bits, either 8 (DAC43701-Q1) or 10 (DAC53701-Q1).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 × based on DAC_SPAN (address D1h) bits.

7.3.2 General-Purpose Input (GPI)

The GPI pin of DACx3701-Q1 enables *processorless* operation. 表 7-1 shows that the GPI pin can be configured to trigger various functions. The GPI_EN bit in the TRIGGER (セクション 7.6.4) register enables or disables the GPI input. The GPI_CONFIG field in the CONFIG2 (セクション 7.6.3) register maps the GPI pin to various functions. The GPI operations are edge-triggered after the device boots up. After the power supply ramps up, the device registers the GPI level and executes the associated command. Use this feature configure the initial output state at power on. By default, the GPI pin is not mapped to any operation. Pull the GPI pin to high or low when not used. When the GPI pin is mapped to a specific function, the corresponding software bit functionality is disabled to avoid a race condition. When the GPI is mapped to margin-high or low trigger function, the output changes dynamically, unlike the behavior with I²C-based programming. All other constraints of the functions are applied to the GPI-based trigger.

表 7-1. GPI Configuration

REGISTER NAME	GPI_EN	GPI_CONFIG	PIN FUNCTION	PIN EDGE	COMMAND
D2h, CONFIG2 and D3h, TRIGGER	0	X	None	X	No Operation (Default)
	1	000	Power-Up, Down (Hi-Z)	Rising	Power-Up
				Falling	Hi-Z Power-Down
	1	001	Power-Up, Down (10-kΩ)	Rising	Power-Up
				Falling	10-kΩ Power-Down
	1	010	Margin-High, Low	Rising	Margin High Trigger
				Falling	Margin Low Trigger
	1	011	Function Generation	Rising	Start Function Generation
				Falling	Stop Function Generation
	1	100	High-Priority Medical Alarm	Rising	Start High-Priority Medical Alarm
				Falling	Stop High-Priority Medical Alarm
	1	101	Medium-Priority Medical Alarm	Rising	Start Medium-Priority Medical Alarm
				Falling	Stop Medium-Priority Medical Alarm
	1	110	Low-Priority Medical Alarm	Rising	Start Low-Priority Medical Alarm
				Falling	Stop Low-Priority Medical Alarm
	1	111	I²C Target Address	Rising	Enable I²C Target Address Update
				Falling	Disable I²C Target Address Update

7.3.3 DAC Update

The DAC output pin (OUT) is updated at the end of I^2C DAC write frame.

7.3.3.1 DAC Update Busy

The DAC_UPDATE_BUSY bit (address D0h) is set to 1 by the device when certain DAC update operations, such as *function generation*, *transition to margin high or low*, or any of the medical alarms are in progress. When the DAC_UPDATE_BUSY bit is set to 1, do not write to any of the DAC registers. After the DAC update operation is completed (DAC_UPDATE_BUSY = 0), any of the DAC registers can be written.

7.3.4 Nonvolatile Memory (EEPROM or NVM)

The DACx3701-Q1 contain nonvolatile memory (NVM) bits. These memory bits are user-programmable and erasable, and retain the set values in the absence of a power supply. All the register bits shown in 表 7-2 can be stored in the device NVM by setting NVM_PROG = 1 (address D3h). The NVM_BUSY bit (address D0h) is set to 1 by device when a NVM write or reload operation is ongoing. During this time, the device blocks all write operations to the device. The NVM_BUSY bit is set to 0 after the write or reload operation is complete; at this point, all write operations to the device are allowed. The default value for all the registers in the DACx3701-Q1 is loaded from NVM as soon as a POR event is issued. Do not perform a read operation from the DAC register while NVM_BUSY = 1.

The DACx3701-Q1 also implement NVM_RELOAD bit (address D3h). Set this bit to 1 for the device to start an NVM reload operation. After the operation is complete, the device autoresets this bit to 0. During the NVM_RELOAD operation, the NVM_BUSY bit is set to 1.

表 7-2. NVM Programmable Registers

REGISTER ADDRESS	REGISTER NAME	BIT ADDRESS	BIT NAME
D1h	GENERAL_CONFIG	13	DEVICE_LOCK
		11:9	CODE_STEP
		8:5	SLEW_RATE
		4:3	DAC_PDN
		2	REF_EN
		1:0	DAC_SPAN
D2h	CONFIG2	15:14	TARGET_ADDRESS
		13:11	GPI_CONFIG
		5:4	INTERBURST_TIME
		3:2	PULSE_OFF_TIME
		1:0	PULSE_ON_TIME
D3h	TRIGGER	10	GPI_EN
21h	DAC_DATA	11:2	DAC_DATA
25h	DAC_MARGIN_HIGH	11:4	MARGIN_HIGH (8 most significant bits)
26h	DAC_MARGIN_LOW	11:4	MARGIN_LOW (8 most significant bits)

7.3.4.1 NVM Cyclic Redundancy Check

The DACx3701-Q1 implement a cyclic redundancy check (CRC) feature for the device NVM to make sure that the data stored in the device NVM is uncorrupted. There are two types of CRC alarm bits implemented in DACx3701-Q1:

- NVM_CRC_ALARM_USER
- NVM_CRC_ALARM_INTERNAL

The NVM_CRC_ALARM_USER bit indicates the status of user-programmable NVM bits, and the NVM_CRC_ALARM_INTERNAL bit indicates the status of internal NVM bits The CRC feature is implemented by storing a 10-Bit CRC (CRC-10-ATM) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM_CRC_ALARM_USER and NVM_CRC_ALARM_INTERNAL address D0h) report any errors after the data are read from the device NVM.

7.3.4.2 NVM_CRC_ALARM_USER Bit

A logic 1 on NVM_CRC_ALARM_USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see *セクション 7.3.7*) command, or cycle power to the DAC. A power cycle also reloads the user-programmable NVM bits. In case of NVM data corruption, program the NVM again.

7.3.4.3 NVM_CRC_ALARM_INTERNAL Bit

A logic 1 on NVM_CRC_ALARM_INTERNAL bit indicates that the internal NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see *セクション 7.3.7*) command or cycle power to the DAC.

7.3.5 Programmable Slew Rate

When the DAC data registers are written, the voltage on DAC output (V_{OUT}) immediately transitions to the new code following the slew rate and settling time specified in the *Electrical Characteristics*. The slew rate control feature controls the rate at which the output voltage (V_{OUT}) changes. When this feature is enabled (using SLEW_RATE[3:0] bits), the DAC output changes from the current code to the code in MARGIN_HIGH (address 25h) or MARGIN_LOW (address 26h) registers (when margin high or low commands are issued to the DAC) using the step and rate set in CODE_STEP and SLEW_RATE bits. With the default slew rate control setting (CODE_STEP and SLEW_RATE bits, address D1h), the output changes smoothly at a rate limited by the output drive circuitry and the attached load. Using this feature, the output steps digitally at a rate defined by bits CODE_STEP and SLEW_RATE on address D1h. SLEW_RATE defines the rate at which the digital slew updates; CODE_STEP defines the amount by which the output value changes at each update. 表 7-3 and 表 7-4 show different settings for CODE_STEP and SLEW_RATE.

表 7-3. Code Step

REGISTER ADDRESS AND NAME	CODE_STEP[2]	CODE_STEP[1]	CODE_STEP[0]	COMMENT
D1h, GENERAL_CONFIG	0	0	0	Code step size = 1 LSB (default)
	0	0	1	Code step size = 2 LSB
	0	1	0	Code step size = 3 LSB
	0	1	1	Code step size = 4 LSB
	1	0	0	Code step size = 6 LSB
	1	0	1	Code step size = 8 LSB
	1	1	0	Code step size = 16 LSB
	1	1	1	Code step size = 32 LSB

表 7-4. Slew Rate

REGISTER ADDRESS AND NAME	SLEW_RATE[3]	SLEW_RATE[2]	SLEW_RATE[1]	SLEW_RATE[0]	TIME PERIOD (PER STEP)
D1h, GENERAL_CONFIG	0	0	0	0	25.6 µs
	0	0	0	1	32 µs
	0	0	1	0	38.4 µs
	0	0	1	1	44.8 µs
	0	1	0	0	204.8 µs
	0	1	0	1	256 µs
	0	1	1	0	307.2 µs
	0	1	1	1	819.2 µs
	1	0	0	0	1638.4 µs
	1	0	0	1	2457.6 µs
	1	0	1	0	3276.8 µs
	1	0	1	1	4915.2 µs
	1	1	0	0	12 µs
	1	1	0	1	8 µs
	1	1	1	0	4 µs
	1	1	1	1	0 µs, no slew (default)

When the slew rate control feature is used, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. Do not write to CODE_STEP, SLEW_RATE, or DAC_DATA during the output slew.

7.3.6 Power-On Reset (POR)

The DACx3701-Q1 family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a 30-ms, POR delay. The default value for all the registers in the DACx3701-Q1 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in 図 7-1, to make sure that the internal capacitors discharge and reset the device on power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

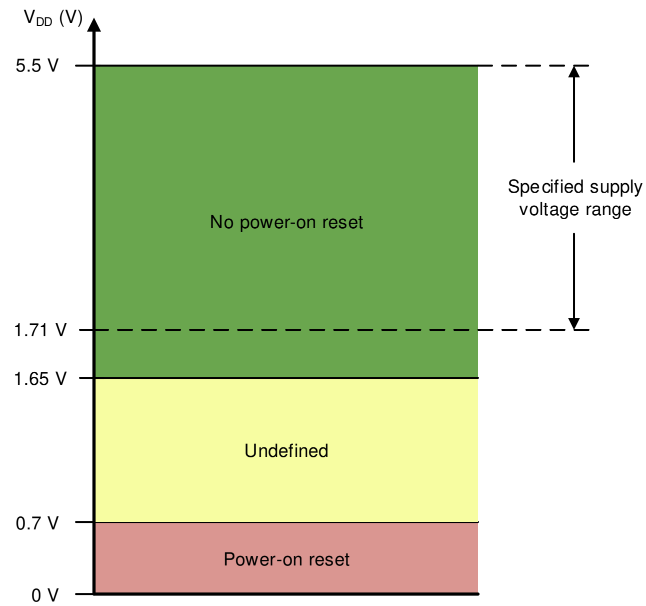


図 7-1. Threshold Levels for the V_{DD} POR Circuit

7.3.7 Software Reset

To initiate a device software reset event, write the reserved code 1010 to the SW_RESET (address D3h). A software reset initiates a POR event.

7.3.8 Device Lock Feature

The DACx3701-Q1 implement a device lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEVICE_LOCK bit (address D1h) is set to 1. To bypass the DEVICE_LOCK setting, write 0101 to the DEVICE_UNLOCK_CODE bits (address D3h).

7.3.9 PMBus Compatibility

The PMBus protocol is an I^2C-based communication standard for power-supply management. PMBus contains standard command codes tailored to power-supply applications. The DACx3701-Q1 implement some PMBus commands such as *Turn Off*, *Turn On*, *Margin Low*, *Margin High*, *Communication Failure Alert Bit (CML)*, as well as *PMBUS revision*. 図 7-2 shows typical PMBus connections. The EN_PMBUS bit (Bit 12, address D1h) must be set to 1 to enable the PMBus protocol.

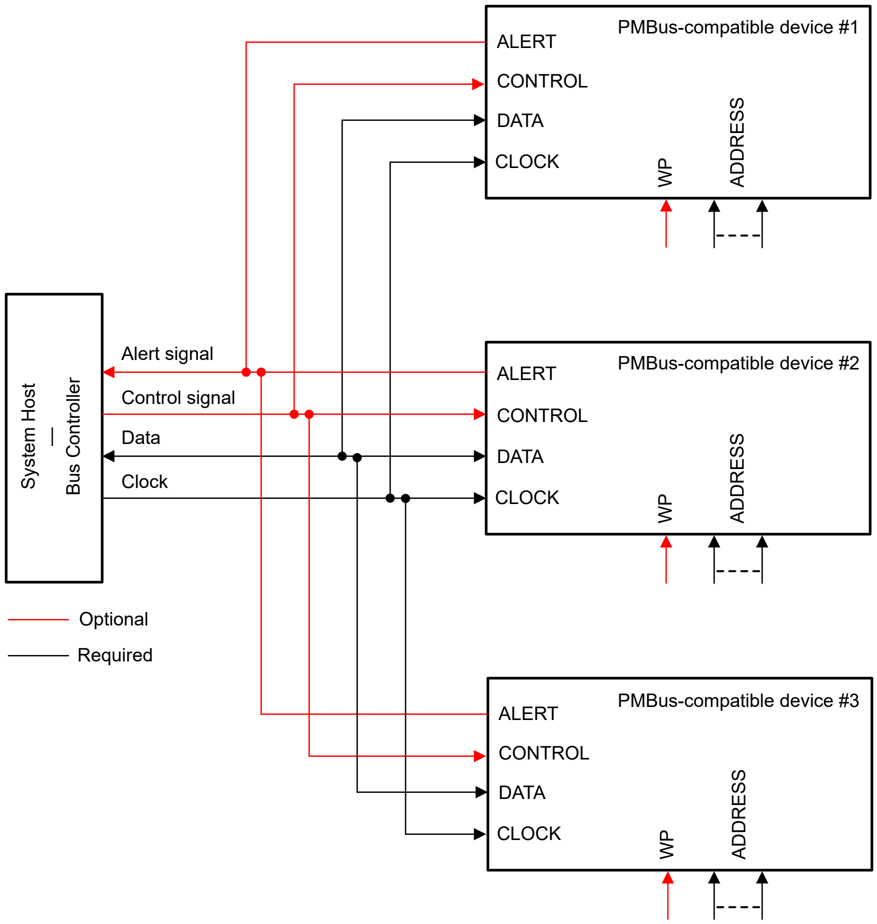


図 7-2. PMBus Connections

Similar to I^2C, PMBus is a variable length packet of 8-bit data bytes, each with a receiver acknowledge, wrapped between a start bit and a stop bit. The first byte is always a 7-bit *target address* followed by a *write* bit, sometimes called the *even address* that identifies the intended receiver of the packet. The second byte is an 8-bit *command* byte, identifying the PMBus command being transmitted using the respective command code. After the command byte, the transmitter either sends data associated with the command to write to the receiver command register (from most significant byte to least significant byte), or sends a new start bit indicating the desire to read the data associated with the command register from the receiver. Then the receiver transmits the data following the same most significant byte first format (see 表 7-8).

7.4 Device Functional Modes

7.4.1 Power Down Mode

The DACx3701-Q1 output amplifier and internal reference can be independently powered down through the DAC_PDN bits (address D1h). At power up, the DAC output and the internal reference are disabled by default. In power-down mode, the DAC output (OUT pin) is in a high-impedance state. To change this state to 10kΩ-A_{GND} (at power up), use the DAC_PDN bits (address D1h).

The DAC power-up state can be programmed to any state (power-down or normal mode) using the NVM. 表 7-5 shows the DAC power-down bits.

表 7-5. DAC Power-Down Bits

REGISTER ADDRESS AND NAME	DAC_PDN[1]	DAC_PDN[0]	DESCRIPTION
D1h, GENERAL_CONFIG	0	0	Power up
	0	1	Power down to 10 kΩ
	1	0	Power down to high impedance (HiZ) (default)
	1	1	Power down to 10 kΩ

7.4.2 Continuous Waveform Generation (CWG) Mode

The DACx3701-Q1 implement a continuous waveform generation feature. To set the device to this mode, set the START_FUNC_GEN (address D3h) to 1. In this mode, the DAC output pin (OUT) generates a continuous waveform based on the FUNC_CONFIG bits (address D1h). 表 7-6 shows the continuous waveforms that can be generated in this mode. The following equations show the frequency of the waveform depends on the resistive and capacitive load on the OUT pin, high and low codes, and slew rate settings.

$$f_{SQUARE} = \frac{1}{2 \times SLEW\_RATE} \tag{3}$$

$$f_{SAWTOOTH} = \frac{1}{SLEW\_RATE \times CEILING\left(\frac{MARGIN\_HIGH - MARGIN\_LOW}{CODE\_STEP} + 1\right)} \tag{4}$$

$$f_{TRIANGLE} = \frac{1}{2 \times SLEW\_RATE \times CEILING\left(\frac{MARGIN\_HIGH - MARGIN\_LOW}{CODE\_STEP}\right)} \tag{5}$$

where:

- SLEW_RATE is the programmable DAC slew rate specified in 表 7-4.
- MARGIN_HIGH and MARGIN_LOW are the programmable DAC codes.
- CODE_STEP is the programmable DAC step code in 表 7-3.
- CEILING is a function that returns the smallest integer value which is greater than or equal to the specified number.

The accuracy of the waveform frequencies depend on the accuracy of the internal oscillator. The DACx3701-Q1 support a calibration option to get the best oscillator frequency accuracy. The DAC-MARGIN-HIGH[11:4] register bits store the oscillator accuracy in the NVM in 2's compliment format. Any overwrite to these NVM bits clears this information permanently. The stored error resolution is 0.15% per LSB. 式 6 calculates the percentage frequency error.

$$f_{ERROR}(\%) = DAC\_MARGIN\_HIGH[11:4] \times 0.15 \tag{6}$$

表 7-6. FUNC_CONFIG bits

REGISTER ADDRESS AND NAME	FUNC_CONFIG[1]	FUNC_CONFIG[0]	DESCRIPTION
D1h, GENERAL_CONFIG	0	0	Generates a triangle wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with the slope defined by the SLEW_RATE and CODE_STEP (address D1h) bits.
	0	1	Generates a sawtooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with the rising slope defined by the SLEW_RATE and CODE_STEP (address D1h) bits and immediate falling edge.
	1	0	Generates a sawtooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with the falling slope defined by the SLEW_RATE and CODE_STEP (address D1h) bits and immediate rising edge.
	1	1	Generates a square wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with the pulse high and low period defined by the SLEW_RATE (address D1h) bits.

7.4.3 PMBus Compatibility Mode

The DACx3701-Q1 I^2C interface implements some of the PMBus commands. 表 7-7 shows the supported PMBus commands that are implemented in DACx3701-Q1.The DAC uses MARGIN_LOW (address 26h), MARGIN_HIGH (address 25h) bits, SLEW_RATE, and CODE_STEP bits (address D1h) for PMBUS_OPERATION_CMD. The EN_PMBUS bit (Bit 12, address D1h) must be set to 1 to enable the PMBus protocol.

表 7-7. PMBus Operation Commands

REGISTER ADDRESS AND NAME	PMBUS_OPERATION_CMD[15:8]	DESCRIPTION
01h, PMBUS_OPERATION	00h	Turn off
	80h	Turn on
	94h	Margin low
	A4h	Margin high

The DACx3701-Q1 also implement PMBus features such as group command protocol and communication time-out failure. The CML bit (address 78h) indicates a communication fault in the PMBus. This bit is reset by writing 1.

To get the PMBus version, read the PMBUS_VERSION bits (address 98h).

7.5 Programming

The DACx3701-Q1 devices have a 2-wire serial interface, SCL and SDA (see the pin diagram in *セクション 5*). The I^{2}C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^{2}C-compatible devices connect to the I^{2}C bus through the open drain I/O pins, SDA and SCL.

The I^{2}C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller device generates the SCL signal. The controller device also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller device on an I^{2}C bus is typically a microcontroller or digital signal processor (DSP). The DACx3701-Q1 family operates as a target device on the I^{2}C bus. A target device acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, theDACx3701-Q1 family operates as a target receiver. A controller device writes to the DACx3701-Q1, a target receiver. However, if a controller device requires the DACx3701-Q1 internal register data, the DACx3701-Q1 operate as a target transmitter. In this case, the controller device reads from the DACx3701-Q1. According to I^{2}C terminology, read and write refer to the controller device.

The DACx3701-Q1 family is a target and supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast-mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast-mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The DACx3701-Q1 family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I^{2}C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. 図 7-3 shows that a not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle.

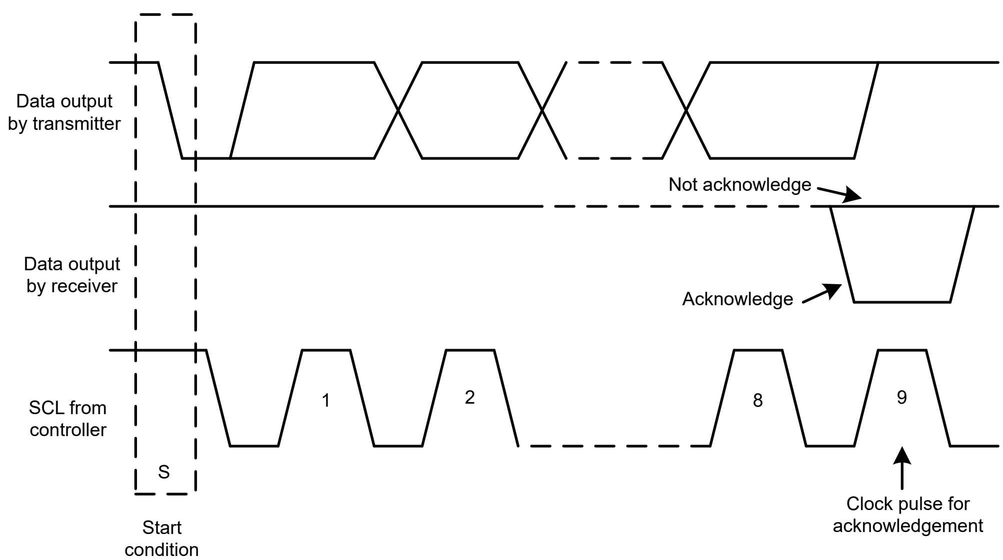


図 7-3. Acknowledge and Not Acknowledge on the I^{2}C Bus

7.5.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. 図 7-4 shows that he start condition is when a high-to-low transition occurs on the SDA line while SCL is high. All I^{2}C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the controller makes sure that data are valid. 図 7-5 shows that a valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle (see 図 7-3). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of 8-data bits and 1 acknowledge-bit, and can continue as long as necessary.
4. 図 7-4 shows that to signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high. This action releases the bus and stops the communication link with the addressed target. All I^{2}C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

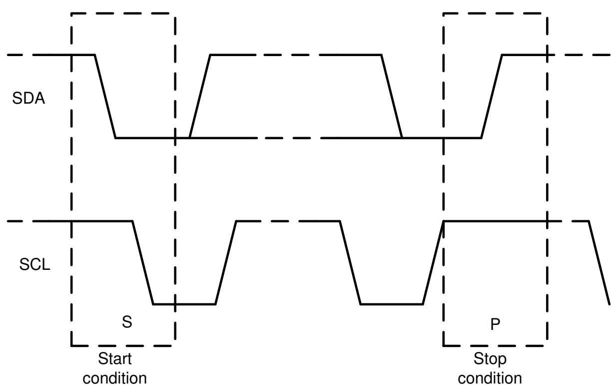


図 7-4. Start and Stop Conditions

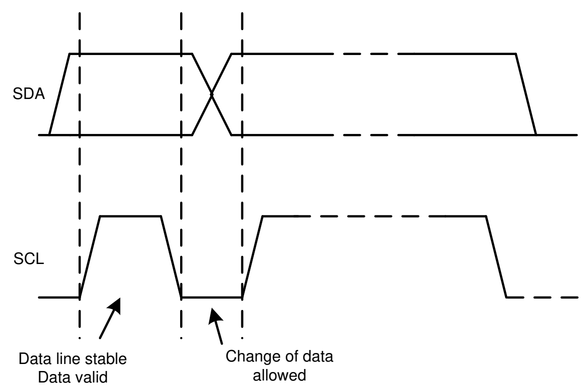


図 7-5. Bit Transfer on the I^{2}C Bus

7.5.2 I²C Update Sequence

For a single update, the DACx3701-Q1 require a start condition, a valid I²C address byte, a command byte, and two data bytes. 表 7-8 lists the update sequence.

表 7-8. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte セクション 7.5.2.1				Command byte セクション 7.5.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the DACx3701-Q1 family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. 図 7-6 shows the I²C bus protocol. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the DACx3701-Q1 devices.

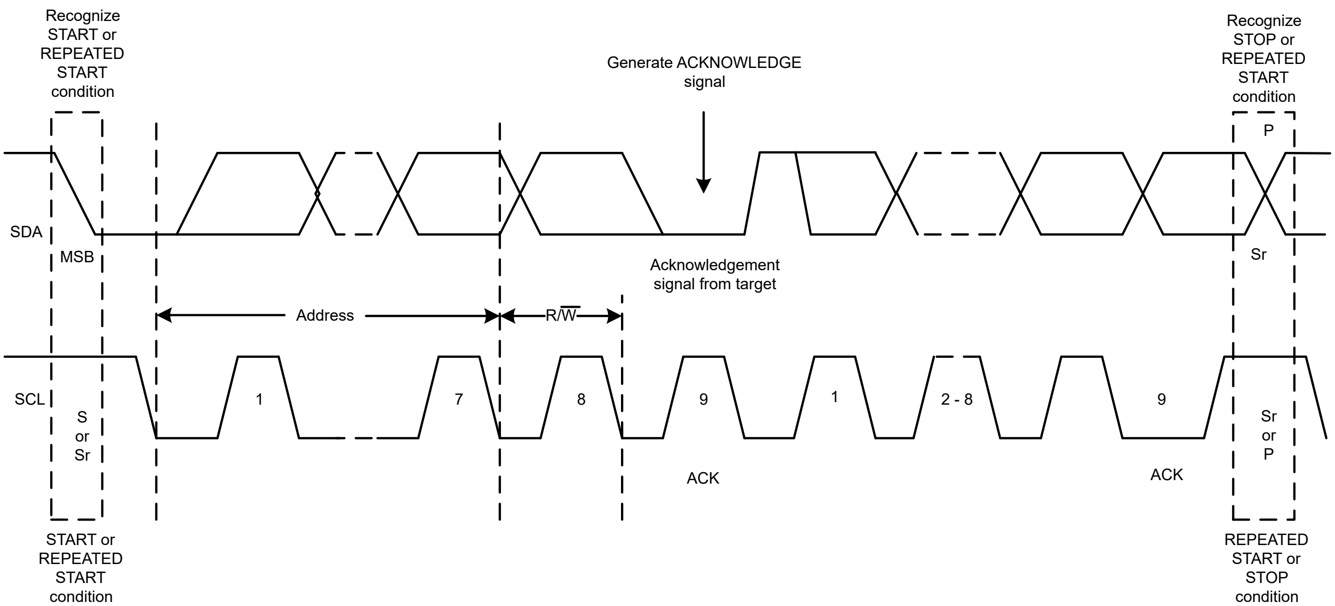


図 7-6. I²C Bus Protocol

The command byte sets the operating mode of the selected DACx3701-Q1 device. For a data update to occur when the operating mode is selected by this byte, the DACx3701-Q1 device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The DACx3701-Q1 device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using the fast-mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the DACx3701-Q1 device releases the I²C bus and awaits a new start condition.

7.5.2.1 Address Byte

The following tables shows the address byte, which is the first byte received following the start condition from the controller device. The first five bits (MSBs) of the address are factory preset to 10010. The next two bits of the address are controlled by the TARGET_ADDRESS field in the CONFIG2 register. Follow the procedure described in the next section to configure the target address. The possible target addresses using these bits are also shown in the next section.

表 7-9. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/ $\overline{W}$
General address	1	0	0	1	0	See 表 7-10 (target address column)		0 or 1
Broadcast address	1	0	0	0	1	1	1	0

The DACx3701-Q1 family supports broadcast addressing, which can be used for synchronously updating or powering down multiple DACx3701-Q1 devices. The DACx3701-Q1 family is designed to work with other members of the family to support multichip synchronous updates. Using the broadcast address, the DACx3701-Q1 devices respond regardless of the states of the TARGET_ADDRESS bits. Broadcast is only supported in write mode.

7.5.2.1.1 Target Address Configuration

This section provides the step by step procedure to configure the I^2C target addresses for up to four DACs. Use the broadcast address for all the steps.

1. Set GPI pin to 0b for all devices.
2. Set GPI_CONFIG in the CONFIG2 register to 111b.
3. Set GPI_EN in the TRIGGER register to 1b.
4. Set the GPI pin to logic high for the device to be configured.
5. Write data to TARGET_ADDRESS bit field in the CONFIG2 register. Only the device with GPI pin logic high updates the TARGET_ADDRESS setting passed in the command. Make sure that the rest of the devices on the same I^2C bus have the respective GPI pins set to logic low during this process.
6. Toggle the GPI pin of the device bring programmed to logic low.
7. Repeat steps (1) through (6) above to program the I2C target addresses to all the devices on the bus.
8. Set GPI_EN to 0b.
9. Change GPI_CONFIG to 000b.
10. Trigger NVM write operation.

The devices are now ready for use.

表 7-10. Address Format

TARGET ADDRESS	TARGET_ADDRESS FIELD IN CONFIG2 REGISTER
1001000	00 (default)
1001001	01
1001010	10
1001011	11

7.5.2.2 Command Byte

表 7-11 lists the command byte addresses.

表 7-11. Command Byte (Register Names)

ADDRESS	REGISTER NAME
D0h	STATUS
D1h	GENERAL_CONFIG
D2h	CONFIG2
D3h	TRIGGER
21h	DAC_DATA
25h	DAC_MARGIN_HIGH
26h	DAC_MARGIN_LOW
01h	PMBUS_OPERATION
78h	PMBUS_STATUS_BYTE
98h	PMBUS_VERSION

7.5.3 I^{2}C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/ $\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/ $\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

An alternative reading method allows for reading back the value of the last register written. The sequence is a start or repeated start with the target address and the R/ $\overline{W}$ bit set to 1, and the two bytes of the last register are read out.

The broadcast address cannot be used for reading.

表 7-12. Read Sequence

S	MSB	…	R/ $\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/ $\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	Address Byte セクション 7.5.2.1				Command Byte セクション 7.5.2.2				Sr	Address Byte セクション 7.5.2.1				MSDB				LSDB			
From controller				Target	From controller			Target	From controller				Target	From target			Controller	From target			Controller

7.6 Register Map

表 7-13. Register Map

<table>
<tr><th rowspan="2">ADDRESS</th><th colspan="8">MOST SIGNIFICANT DATA BYTE (MSDB)</th><th colspan="8">LEAST SIGNIFICANT DATA BYTE (LSDB)</th></tr>
<tr><th>BIT15</th><th>BIT14</th><th>BIT13</th><th>BIT12</th><th>BIT11</th><th>BIT10</th><th>BIT9</th><th>BIT8</th><th>BIT7</th><th>BIT6</th><th>BIT5</th><th>BIT4</th><th>BIT3</th><th>BIT2</th><th>BIT1</th><th>BIT0</th></tr>
<tr><td>D0h</td><td>NVM_CRC_ALARM_USER</td><td>NVM_CRC_ALARM_INTERNAL</td><td>NVM_BUSY</td><td>DAC_UPDATE_BUSY</td><td colspan="6">X[(1)]</td><td colspan="4">DEVICE_ID</td><td colspan="2">VERSION_ID</td></tr>
<tr><td>D1h</td><td colspan="2">FUNC_CONFIG</td><td>DEVICE_LOCK</td><td>EN_PMBUS</td><td colspan="3">CODE_STEP</td><td colspan="4">SLEW_RATE</td><td colspan="2">DAC_PDN</td><td>REF_EN</td><td colspan="2">DAC_SPAN</td></tr>
<tr><td>D2h</td><td colspan="2">TARGET_ADDRESS</td><td colspan="3">GPI_CONFIG</td><td colspan="5">RESERVED</td><td colspan="6">FB_IMP</td></tr>
<tr><td>D3h</td><td colspan="4">DEVICE_UNLOCK_CODE</td><td>X</td><td>GPI_EN</td><td>DEVICE_CONFIG_RESET</td><td>START_FUNC_GEN</td><td>PMBUS_MARGIN_HIGH</td><td>PMBUS_MARGIN_LOW</td><td>NVM_RELOAD</td><td>NVM_PROG</td><td colspan="4">SW_RESET</td></tr>
<tr><td>21h</td><td colspan="4">X</td><td colspan="10">DAC_DATA[9:0] (10-Bit) or DAC_DATA[7:0] (8-Bit)</td><td colspan="2">X</td></tr>
<tr><td>25h</td><td colspan="4">X</td><td colspan="10">MARGIN_HIGH[9:0] (10-Bit) or MARGIN_HIGH[7:0] (8-Bit)</td><td colspan="2">X</td></tr>
<tr><td>26h</td><td colspan="4">X</td><td colspan="10">MARGIN_LOW[9:0] (10-Bit) or MARGIN_LOW[7:0] (8-Bit)</td><td colspan="2">X</td></tr>
<tr><td>01h</td><td colspan="8">PMBUS_OPERATION_CMD</td><td colspan="8">Not available</td></tr>
<tr><td>78h</td><td colspan="6">X</td><td>CML</td><td>X</td><td colspan="8">Not available</td></tr>
<tr><td>98h</td><td colspan="8">PMBUS_VERSION</td><td colspan="8">Not available</td></tr>
</table>

(1) X = Don't care.

表 7-14. Register Names

ADDRESS	REGISTER NAME	SECTION
D0h	STATUS	セクション 7.6.1
D1h	GENERAL_CONFIG	セクション 7.6.2
D2h	CONFIG2	セクション 7.6.3
D3h	TRIGGER	セクション 7.6.4
21h	DAC_DATA	セクション 7.6.5
25h	DAC_MARGIN_HIGH	セクション 7.6.6
26h	DAC_MARGIN_LOW	セクション 7.6.7
01h	PMBUS_OPERATION	セクション 7.6.8
78h	PMBUS_STATUS_BYTE	セクション 7.6.9
98h	PMBUS_VERSION	セクション 7.6.10

表 7-15. Access Type Codes

Access Type	Code	Description
X	X	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

7.6.1 STATUS Register (address = D0h) [reset = 000Ch or 0014h]

図 7-7. STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM_CRC_ALARM_USER	NVM_CRC_ALARM_INTERNAL	NVM_BUSY	DAC_UPDATE_BUSY	X						DEVICE_ID				VERSION_ID	
R-0	R-0	R-0	R-0	X-00h						10-bit: R-3h 8-bit: R-5h				R-00	

表 7-16. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM_CRC_ALARM_USER	R	0	0: No CRC error in user NVM bits 1: CRC error in user NVM bits
14	NVM_CRC_ALARM_INTERNAL	R	0	0: No CRC error in internal NVM 1: CRC error in internal NVM bits
13	NVM_BUSY	R	0	0: NVM write or load completed, Write to DAC registers allowed 1: NVM write or load in progress, Write to DAC register map not allowed
12	DAC_UPDATE_BUSY	R	0	0: DAC outputs updated, Write to DAC registers allowed 1: DAC outputs update in progress, Write to DAC register map not allowed
11:6	X	X	00h	Don't care
5:2	DEVICE_ID	R	DAC53701-Q1: 3h DAC43701-Q1: 5h	Device identifier: DAC53701-Q1: 3h DAC43701-Q1: 5h
1:0	VERSION_ID	R	00	Silicon version identifier. This field can have a different value based on the silicon revision.

7.6.2 GENERAL_CONFIG Register (address = D1h) [reset = 01F0h]

図 7-8. GENERAL_CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC_CONFIG		DEVICE_LOCK	EN_PMBUS	CODE_STEP			SLEW_RATE				DAC_PDN		REF_EN	DAC_SPAN	
R/ $\overline{W}$-00		R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-000			R/$\overline{W}$-Fh				R/$\overline{W}$-10h		R/$\overline{W}$-0	R/$\overline{W}$-00	

表 7-17. GENERAL_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FUNC_CONFIG	R/$\overline{W}$	00	00: Generates a triangle wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with slope defined by SLEW_RATE and CODE_STEP bits. 01: Generates Saw-Tooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with rising slope defined by SLEW_RATE and CODE_STEP bits and immediate falling edge. 10: Generates Saw-Tooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with falling slope defined by SLEW_RATE and CODE_STEP bits and immediate rising edge. 11: Generates a square wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with pulse high and low period defined by SLEW_RATE bits.
13	DEVICE_LOCK	R/$\overline{W}$	0	0: Device not locked 1: Device locked, the device locks all the registers. This bit can be overwritten (unlock device) by writing 0101 to the DEVICE_UNLOCK_CODE bits (address D3h)

表 7-17. GENERAL_CONFIG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
12	EN_PMBUS	R/$\overline{W}$	0	0: PMBus mode disabled 1: PMBus mode enabled
11:9	CODE_STEP	R/$\overline{W}$	000	Code step for programmable slew rate control. 000: Code step size = 1 LSB (default) 001: Code step size = 2 LSB 010: Code step size = 3 LSB 011: Code step size = 4 LSB 100: Code step size = 6 LSB 101: Code step size = 8 LSB 110: Code step size = 16 LSB 111: Code step size = 32 LSB
8:5	SLEW_RATE	R/$\overline{W}$	Fh	Slew rate for programmable slew rate control. 0000: 25.6 µs (per step) 0001: 32 µs (per step) 0010: 38.4 µs (per step) 0011: 44.8 µs (per step) 0100: 204.8 µs (per step) 0101:256 µs (per step) 0110: 307.2 µs (per step) 0111: 819.2 µs (per step) 1000: 1.6384 ms (per step) 1001: 2.4576 ms (per step) 1010: 3.2768 ms (per step) 1011: 4.9152 ms (per step) 1100: 12 µs (per step) 1101: 8 µs (per step) 1110: 4 µs (per step) 1111: No slew (default)
4:3	DAC_PDN	R/$\overline{W}$	10	00: Power up 01: Power down to 10 kΩ 10: Power down to high impedance (default) 11: Power down to 10 kΩ
2	REF_EN	R/$\overline{W}$	0	0: Internal reference disabled, V_{DD} is DAC reference voltage, DAC output range from 0 V to V_{DD}. 1: Internal reference enabled, DAC reference = 1.21 V, DAC output range is a function of DAC_SPAN.
1:0	DAC_SPAN	R/$\overline{W}$	00	Only applicable when internal reference is enabled. 00: Reference to V_{OUT} gain = 1.5 × 01: Reference to V_{OUT} gain = 2 × 10: Reference to V_{OUT} gain = 3 × 11: Reference to V_{OUT} gain = 4 ×

7.6.3 CONFIG2 Register (address = D2h) [reset = device-specific]

図 7-9. CONFIG2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TARGET_ADDRESS		GPI_CONFIG			RESERVED					FB_IMP					
R/$\overline{W}$-00		R/$\overline{W}$-000			R/$\overline{W}$-00h					R/$\overline{W}$-device-specific					

表 7-18. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	TARGET_ADDRESS	R/$\overline{W}$	00	AD1-AD0 of target address as per 表 7-10
13:11	GPI_CONFIG	R/$\overline{W}$	000	Refer to 表 7-1 for the GPI configuration
10:6	RESERVED	R/$\overline{W}$	00h	Reserved.
5:0	FB_IMP	R/$\overline{W}$	Device-specific	These register bits store the measured error of the dc impedance from the FB pin to ground with respect to the typical value, for internal reference with gains 3 × and 4 ×. This value is stored in the NVM. An overwrite to these NVM bits clears this information permanently. The error resolution is 1% and the measurement accuracy is ±2%.

7.6.4 TRIGGER Register (address = D3h) [reset = 0008h]

図 7-10. TRIGGER Register

15 14 13 12	11	10	9	8	7	6	5	4	3 2 1 0
DEVICE_UNLOCK_CODE	X	GPI_ EN	DEVICE_ CONFIG_ RESET	START_ FUNC_ GEN	PMBUS_ MARGIN_ HIGH	PMBUS_ MARGIN_ LOW	NVM_ RELOAD	NVM_ PROG	SW_RESET
W-0h	X-0	R/W-0	W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	W-8h

表 7-19. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	DEVICE_UNLOCK_CODE	W	0h	Write 0101 to unlock the device to bypass DEVICE_LOCK bit.
11	X	X	0	Don't care
10	GPI_EN	R/W	0	0: GPI disabled 1: GPI enabled
9	DEVICE_CONFIG_RESET	W	0	0: Device configuration reset not initiated 1: Device configuration reset initiated. All registers loaded with factory reset values.
8	START_FUNC_GEN	R/W	0	0: Continuous waveform generation mode disabled 1: Continuous waveform generation mode enabled, device generates continuous waveform based on FUNC_CONFIG (address D1h), MARGIN_LOW (address 26h), MARGIN_HIGH (address 25h), and SLEW_RATE and CODE_STEP (address D1h) bits.
7	PMBUS_MARGIN_HIGH	R/W	0	0: PMBus margin high command not initiated 1: PMBus margin high command initiated, DAC output margins high to MARGIN_HIGH code (address 25h). This bit automatically resets to 0 after the DAC code reaches MARGIN_HIGH value.
6	PMBUS_MARGIN_LOW	R/W	0	0: PMBus margin low command not initiated 1: PMBus margin low command initiated, DAC output margins low to MARGIN_LOW code (address 26h). This bit automatically resets to 0 after the DAC code reaches MARGIN_LOW value.
5	NVM_RELOAD	R/W	0	0: NVM reload not initiated 1: NVM reload initiated, applicable DAC registers loaded with corresponding NVM. NVM_BUSY bit set to 1 which this operation is in progress.. This bit self-resets.
4	NVM_PROG	R/W	0	0: NVM write not initiated 1: NVM write initiated, NVM corresponding to applicable DAC registers loaded with existing register settings. NVM_BUSY bit set to 1 which this operation is in progress. This bit self-resets.
3:0	SW_RESET	W	8h	1000: Software reset not initiated 1010: Software reset initiated, DAC registers loaded with corresponding NVMs, all other registers loaded with default settings.

7.6.5 DAC_DATA Register (address = 21h) [reset = 0000h]

図 7-11. DAC_DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				DAC_DATA[9:0] / DAC_DATA[7:0] – MSB Left aligned										X	
X-0h				R/$\overline{W}$-000h										X-00	

表 7-20. DAC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	X	X	0h	Don't care
11:2	DAC_DATA[9:0] / DAC_DATA[7:0]	R/$\overline{W}$	000h	Writing to the DAC_DATA register forces the respective DAC channel to update the active register data to the DAC_DATA. Data are in straight binary format and use the following format: DACx3701-Q1: {DATA[9:0]} DACx3701-Q1: {DATA[7:0], X, X} X = Don't care bits
1:0	X	X	00	Don't care

7.6.6 DAC_MARGIN_HIGH Register (address = 25h) [reset = device-specific]

図 7-12. DAC_MARGIN_HIGH Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				MARGIN_HIGH[9:0] / MARGIN_HIGH[7:0] – MSB Left aligned										X	
X-0h				R/W-device-specific										X-00	

表 7-21. DAC_MARGIN_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	X	X	0h	Don't care
11:2	MARGIN_HIGH[9:0] / MARGIN_HIGH[7:0] – MSB Left aligned	R/W	Device-specific	Margin high code for DAC output. Data are in straight binary format and use the following format: DACx3701-Q1: {MARGIN_HIGH[[9:0]} DACx3701-Q1: {MARGIN_HIGH[[7:0], X, X} X = Don't care bits The MARGIN_HIGH[7:0] bits store the oscillator frequency error for every device with 0.15%/LSB resolution in the NVM. An overwrite to this NVM field clears the error information permanently. See セクション 7.4.2 for the error calculation.
1:0	X	X	00	Don't care

7.6.7 DAC_MARGIN_LOW Register (address = 26h) [reset =device-specific]

図 7-13. DAC_MARGIN_LOW Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				MARGIN_LOW[9:0] / MARGIN_LOW[7:0] – MSB Left aligned										X	
X-0h				R/W-device-specific										X-00	

表 7-22. DAC_MARGIN_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	X	X	0h	Don't care
11:2	MARGIN_LOW[9:0] / MARGIN_LOW[7:0] – MSB Left aligned	R/W	Device-specific	Margin low code for DAC output. Data are in straight binary format and follows the format below: DACx3701-Q1: {MARGIN_LOW[[9:0]} DACx3701-Q1: {MARGIN_LOW[[7:0], X, X} X = Don't care bits Register bits 7:2 store the measured error of the dc impedance from the FB pin to ground with respect to the typical value, for external reference or internal reference with gains 1 × and 2 ×. This value is stored in the NVM. An overwrite to these NVM bits clears this information permanently. The error resolution is 1% and the measurement accuracy is ±2%.
1:0	X	X	00	Don't care

7.6.8 PMBUS_OPERATION Register (address = 01h) [reset = 0000h]

図 7-14. PMBUS_OPERATION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS_OPERATION_CMD								X							
R/$\overline{W}$-00h								X-00h							

表 7-23. PMBUS_OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PMBUS_OPERATION_CMD	R/$\overline{W}$	00h	PMBus operation commands 00h: Turn off 80h: Turn on A4h: Margin high, DAC output margins high to MARGIN_HIGH code (address 25h) 94h: Margin low, DAC output margins low to MARGIN_LOW code (address 26h)
7:0	X	X	00h	Not applicable

7.6.9 PMBUS_STATUS_BYTE Register (address = 78h) [reset = 0000h]

図 7-15. PMBUS_STATUS_BYTE Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X						CML	X	N/A							
X-00h						R/$\overline{W}$-0	X-0	X-00h							

表 7-24. PMBUS_STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	X	X	00h	Don't care
9	CML	R/$\overline{W}$	0	0: No communication Fault 1: PMBus communication fault for write with incorrect number of clocks, read before write command, invalid command address, and invalid or unsupported data value; reset this bit by writing 1.
8	X	X	0	Don't care
7:0	X	X	00h	Not applicable

7.6.10 PMBUS_VERSION Register (address = 98h) [reset = 2200h]

図 7-16. PMBUS_VERSION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS_VERSION								X							
R-22h								X-00h							

表 7-25. PMBUS_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PMBUS_VERSION	R	22h	PMBus version
7:0	X	X	00h	Not applicable

8 Application and Implementation

注

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8.1 Application Information

The DACx3701 are buffered, force-sense output, single-channel, DACs that include an NVM and internal reference and are available in a tiny 3-mm × 3-mm package . These DACs are designed for general-purpose applications in a wide range of end equipment. Some of the most common applications for these devices are power-supply margining and control, adaptive voltage scaling (AVS), *set-and-forget* LED biasing in automotive applications and mobile projectors, general-purpose function generation, medical alarm generation, and programmable comparator applications (such as smoke detectors, standalone PWM control loops, and offset and gain trimming in precision circuits).

8.2 Typical Applications

This section explains the design details of two primary applications of DACx3701-Q1: power-supply margining and LED thermal foldback.

8.2.1 Power-Supply Margining

A power-supply margining or scaling circuit is used to test and trim the output of a power converter. This example circuit is used to test a system by margining the power supplies, for adaptive voltage scaling, or to program a desired value at the output. Adjustable power supplies, such as LDOs and DC/DC converters provide a feedback or adjust input that is used to set the desired output. A precision voltage-output DAC is the best choice for controlling the power-supply output linearly. 図 8-1 shows a control circuit for a switch-mode power supply (SMPS) using the DACx3701-Q1. Typical applications of power-supply margining are communications equipment, enterprise servers, test and measurement, automotive processor modules, and general-purpose power-supply modules.

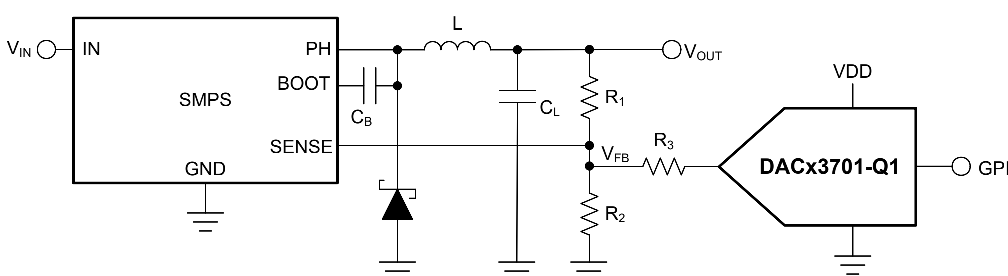

図 8-1. Power-Supply Margining

8.2.1.1 Design Requirements

- Power-supply nominal output: 3.3 V
- Reference voltage of the converter (V_{FB}): 0.6 V
- Margin: ±10% (that is, 2.97 V to 3.63 V)
- DAC output range: 1.8 V
- Nominal current through R_1 and R_2: 100 μA

8.2.1.2 Detailed Design Procedure

The DACx3701-Q1 features a Hi-Z power-down mode that is set by default at power up, unless the device is programmed otherwise using the NVM. When the DAC output is at Hi-Z, the current through R_3 is zero and the SMPS is set at the nominal output voltage of 3.3 V. To have the same nominal condition when the DAC powers up, bring up the device at the same output as V_{FB} (that is 0.6 V). This configuration makes sure there is no current through R_3 even at power-up. Calculate R_1 as (V_{OUT} – V_{FB}) / 100 μA = 27 kΩ.

To achieve ±10% margin-high and margin-low conditions, the DAC must sink or source additional current through R_1. Calculate the current from the DAC (I_{MARGIN}) using 式 7 as 12 μA.

$$I_{MARGIN} = \left(\frac{V_{OUT} \times (1 + MARGIN) - V_{FB}}{R_1} \right) - I_{NOMINAL} \quad (7)$$

where

- I_{MARGIN} is the margin current sourced or sunk from the DAC.
- MARGIN is the percentage margin value divided by 100.
- $I_{NOMINAL}$ is the nominal current through R_1 and R_2.

To calculate the value of R_3, first decide the DAC output range, and make sure to avoid the codes near zero-scale and full-scale for safe operation in the linear region. A DAC output of 20 mV is a safe consideration as the minimum output, and (1.8 V – 0.6 V – 20 mV = 1.18 V) as the maximum output. When the DAC output is at 20 mV, the power supply goes to margin high, and when the DAC output is at 1.18 V, the power supply goes to margin low. Calculate the value of R_3 using 式 8 as 48.3 kΩ. Choose a standard resistor value and adjust the DAC outputs. Choosing R_3 = 47 kΩ makes the DAC margin high code as 1.164 V and the DAC margin low code as 36 mV.

$$R_3 = \frac{|V_{DAC} - V_{FB}|}{I_{MARGIN}} \quad (8)$$

The DACx3701-Q1 have a slew rate feature that is used to toggle between margin high, margin low, and nominal outputs with a defined slew rate. See the 表 7-17 for the slew rate setting details.

注

The MARGIN HIGH register value in DACx3701-Q1 results in the MARGIN LOW value at the power supply output. Similarly, the MARGIN LOW register value in DACx3701-Q1 results in the MARGIN HIGH value at the power-supply output.

The pseudocode for getting started with a power-supply control application is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Write DAC code (12-bit aligned) for nominal output
//For a 1.8-V output range, the 10-bit hex code for 0.6 V is 0x0155.
//With 12-bit alignment, the hex code is 0x0554
WRITE DAC_DATA(0x21), 0x05, 0x54
//Write DAC code (12-bit aligned) for margin-low output at the power supply
//For a 1.8-V output range, the 10-bit hex code for 1.164 V is 0x0296.
//With 12-bit alignment, the hex code is 0x0A58
WRITE DAC_MARGIN_HIGH(0x25), 0x0A, 0x58
//Write DAC code (12-bit aligned) for margin-high output at the power supply
//For a 1.8-V output range, the 10-bit hex code for 36 mV is 0x14.
//With 12-bit alignment, the hex code is 0x50
WRITE DAC_MARGIN_LOW(0x26), 0x00, 0x50
//Power-up the device with enable internal reference with 1.5x output span.
//This configuration outputs the nominal voltage (0.6 V)
//CODE_STEP: 2 LSB, SLEW_RATE: 25.6 µs
WRITE GENERAL_CONFIG(0xD1), 0x12, 0x14
//Trigger margin-low output at the power supply
WRITE TRIGGER(0xD3), 0x00, 0x80
//Trigger margin-high output at the power supply
WRITE TRIGGER(0xD3), 0x00, 0x40
//Write back DAC code (12-bit aligned) for nominal output
WRITE DAC_DATA(0x21), 0x05, 0x54
```

8.2.1.3 Application Curves

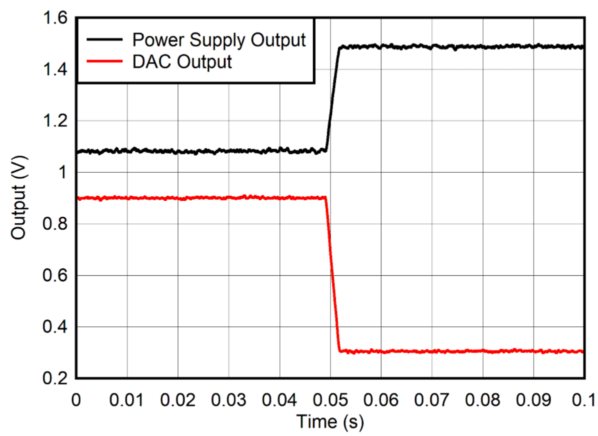

図 8-2. Power-Supply Margin High

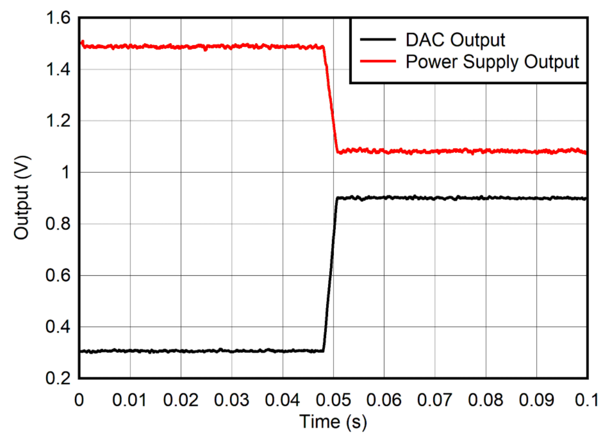

図 8-3. Power Supply Margin Low

8.2.2 LED Thermal Foldback

The reliability of LED lights is inversely proportional to the operating temperature. Most LED lighting designs implement a heat sink for thermal management. However, to improve the life of the LEDs, an active thermal-foldback loop is needed to avoid over-design of the thermal management components. The daytime running light (DRL) in automotive lighting remains always on and is exposed to sunlight during daytime. Thermal foldback is a necessity in DRLs to maximize the LED life. DACx3701-Q1 provides a thermal-foldback loop using the force-sense output of the DAC. 図 8-4 shows a simplified circuit diagram of the LED thermal foldback.

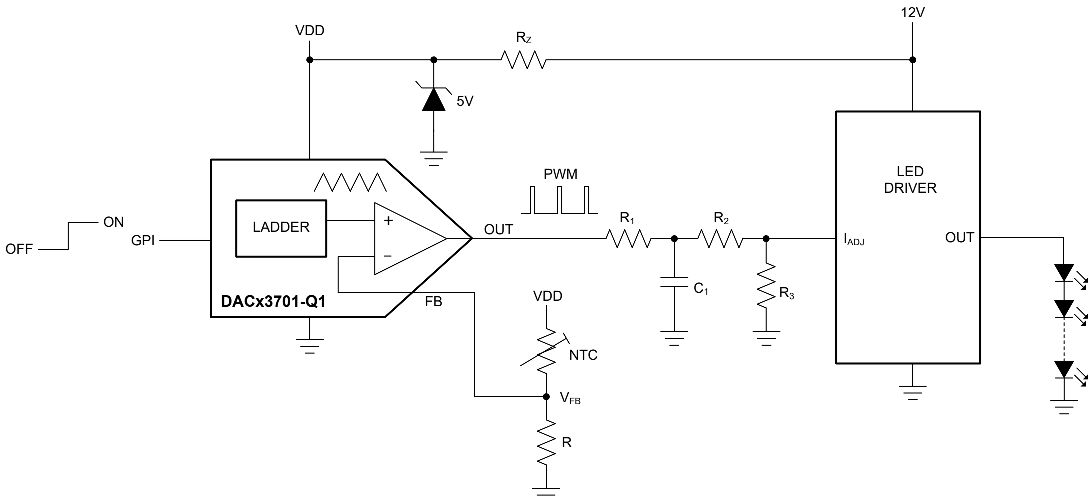

図 8-4. LED Thermal Foldback

8.2.2.1 Design Requirements

- LED supply voltage: 12 V
- DAC supply voltage: 5 V
- Temperature range: –20°C to +105°C
- Foldback point: 30°C
- Cut-off temperature: 105°C
- Output type: PWM
- PWM frequency: approximately 200 Hz

8.2.2.2 Detailed Design Procedure

Choose a 5-V Zener diode of less than 50 µA of reverse current. The DACx3701-Q1consumes a quiescent current of around 200 µA. Assume the load current of the DAC to be maximum 500 µA. Thus, the total current needed for the DAC and the Zener diode is 750 µA. Considering a 2 × derating factor, design the circuit for 1.5 mA. Hence, the value of the current limiting resistor R_Z is (12 V – 5 V) / 1.5 mA = 4.7 kΩ. The worst-case power dissipation across the Zener diode is (5 V × 1.5 mA) = 7.5 mW. Any standard Zener diode can be used with this power rating.

Choose a negative temperature coefficient (NTC) thermistor with nominal resistance of 10 kΩ at 25°C. At the foldback point of 30°C, the resistance of the NTC, R_{NTC} is approximately 7 kΩ. At 105°C, the resistance of the NTC is approximately 800 Ω. Choose the value of R after simulating the linearity plot along with the correct NTC part number. For the sake of calculation, take R as 5 kΩ. In this case, V_{FB} is 2.08 V at 25°C (R_{NTC} = 7 kΩ). For 10-bit resolution and a full-scale output of 5 V, 2.08 V corresponds to the DAC code (2.08 × 1024 / 5) = 426. Similarly, the LED must be cut off at 105°C, which refers to an R_{NTC} of 800 Ω and a corresponding V_{FB} of 4.31 V, or the DAC code 883. Thus, the margin-high value is 883, or 0x373, and the margin-low value is 426, or 0x1AA.

Configure the FUNC_CONFIG bits to 00b in the GENERAL_CONFIG register to select triangular waveform. Use 式 5 for calculating the frequency of the triangular waveform. By choosing a CODE_STEP of 6 LSB and SLEW_RATE of (25.6 µs × 1.25), the frequency of the triangular waveform is 205 Hz.

For voltage output, use an RC filter as shown in 図 8-4. The resistor divider comprised of R1, R2, and R3 define the voltage below the foldback temperature. This voltage divider is useful in case the maximum LED current is set below the 100% value.

8.2.2.3 Application Curves

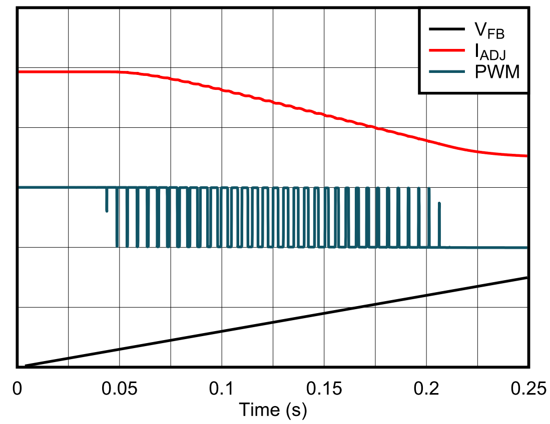

図 8-5. LED Thermal Foldback

8.3 Power Supply Recommendations

The DACx3701-Q1 family of devices does not require specific supply sequencing. These devices require a single power supply, V_{DD}. Use a 0.1-μF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 μF for the CAP pin.

8.4 Layout

8.4.1 Layout Guidelines

The DACx3701-Q1 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

8.4.2 Layout Example

図 8-6 shows an example layout drawing with decoupling capacitors and pullup resistors.

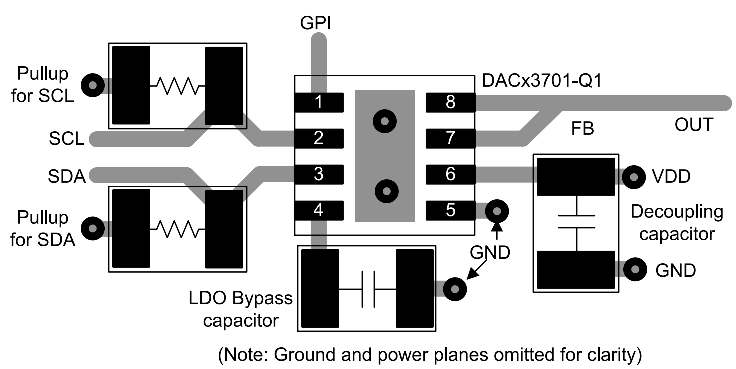

図 8-6. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

Texas, Instruments *DAC53701EVM* user's guide

9.2 ドキュメントの更新通知を受け取る方法

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC43701DSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	47Q1
DAC43701DSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	47Q1
DAC53701DSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	57Q1
DAC53701DSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	57Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DAC43701-Q1, DAC53701-Q1 :

- Catalog : DAC43701, DAC53701

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

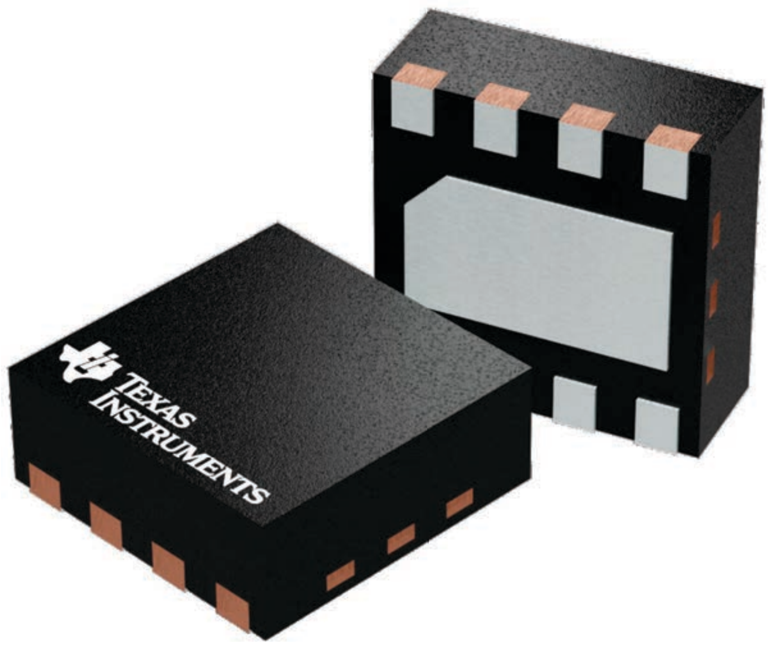
DSG 8

WSON - 0.8 mm max height

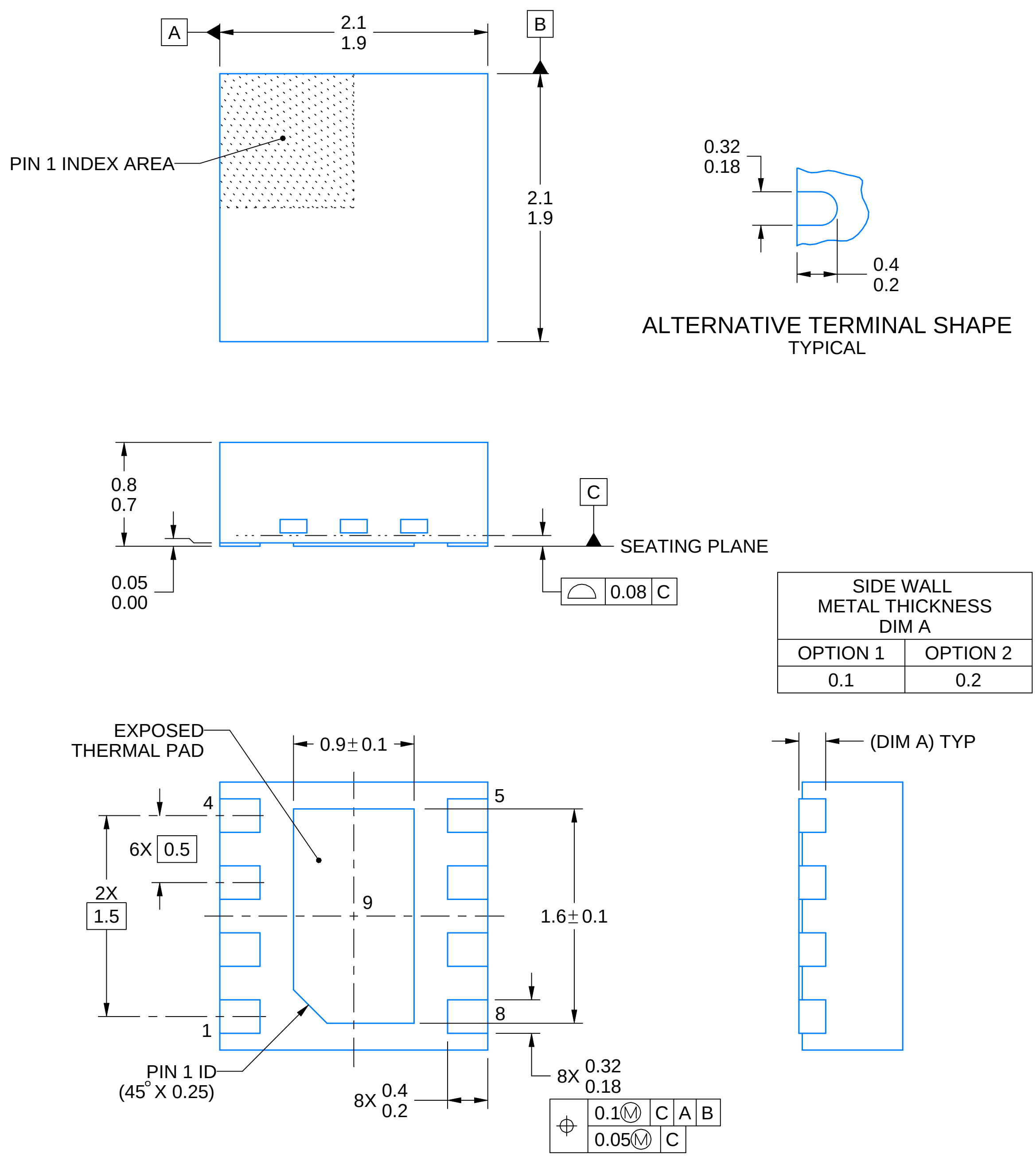
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

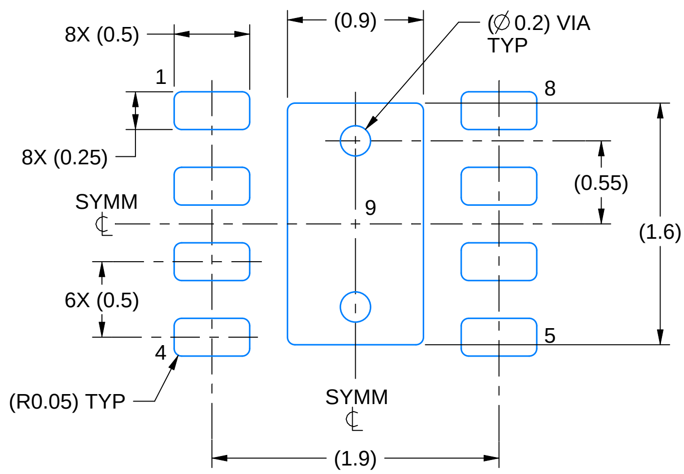


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

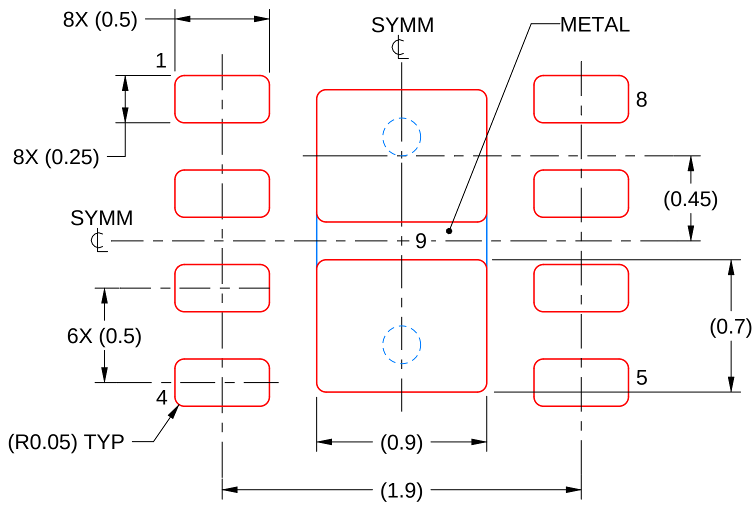
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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