DAC12DL3200 低レイテンシ LVDS インターフェイス搭載、最大 6.4GSPS のシングルチャネル / 3.2GSPS デュアルチャネル 12 ビット D/A コンバータ (DAC)

1 特長

- 12 ビット分解能
- 最大入力および出力サンプル・レート:
  - シングル・チャネルで最大 6.4GSPS
  - デュアル・チャネルで最大 3.2GSPS
- マルチナイキスト動作モード:
  - シングル・チャネル・モード:NRZ、RTZ、RF
  - デュアル・チャネル・モード:NRZ、RTZ、RF、2xRF
- デバイス全体で低レイテンシ:6～8ns
- 送信機能を低レイテンシ レシーバ ADC12DL3200 にマッチングさせる機能
  - DAC と ADC の合計レイテンシ < 15ns (FPGA を含まない)
- パラレル DDR LVDS インターフェイス
  - タイミングを簡素化するソース同期インターフェイス:
  - 24 または 48 本の LVDS ペアで最大 1.6Gbps に対応
  - 12 ビット・バスごとに 1 つの LVDS DDR クロック
- 出力周波数範囲:> 8GHz
- フルスケール電流:21mA
- クロックと同期の簡素化
  - SYSREF のウィンドウ処理により、セットアップ時間とホールド時間を簡素化
- オンチップのダイレクト・デジタル・シンセサイザ(DDS)
  - シングルトーンと 2 トーンの正弦波生成
  - 32 x 32 ビット数値制御オシレータ
  - 高速周波数ホッピング機能 (500ns 未満)
  - 同期 CMOS 周波数 / 位相入力
- f_{OUT} = 4.703 GHz、6.4GSPS、RF モードで高性能を発揮
  - 出力電力:-3dBm
  - ノイズ・フロア (70MHz オフセット):-147dBc/Hz
  - SFDR:60dBc
- 電源:1.0V、1.8V、-1.8V
- 消費電力:1.49W (2 チャネル、RF モード、3.2GSPS)
- パッケージ:256 ボール FCBGA (17 x 17mm、1mm ピッチ)

2 アプリケーション

- 電子兵器
- ジェネレータ:パルス、パターン、任意波形ジェネレータ (AWG)

3 概要

DAC12DL3200 は、超低レイテンシのデュアル・チャネル RF サンプリング D/A コンバータ (DAC) であり、デュアル・チャネル・モードで最大 3.2GSPS 、シングル・チャネル・モードで 6.4GSPS の入力 / 出力レートに対応します。この DAC は、2GHz を上回る信号帯域幅を送信することができ、マルチナイキスト出力モードを使用する場合はキャリア周波数が 8GHz に迫ります。高い出力周波数範囲により、C バンド (8GHz) 以上での直接サンプリングが可能です。

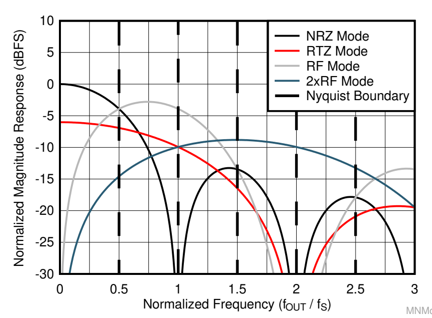
DAC12DL3200 は、デュアル・チャネル・モードで I/Q ベースバンド DAC として使用できます。また、サンプリング・レートが高く出力周波数範囲が広い DAC12DL3200 は、任意波形生成 (AWG) と直接デジタル合成 (DDS) に対応しています。統合された DDS ブロックにより、シングルトーンと 2 トーン生成がチップ上で可能になります。

DAC12DL3200 は、最大 48 個の LVDS ペアと 4 個の DDR LVDS クロックで構成されるパラレル LVDS インターフェイスを採用しています。インターフェイスの同期にはストローブ信号を使用します。この信号は、最下位ビット (LSB) で送信することも、オプションとして専用のストローブ LVDS レーン上で送信することもできます。各 LVDS ペアは、最大 1.6Gbps に対応します。同期信号 (SYSREF) を使用したマルチデバイス同期をサポートしており、JESD204B/C クロック供給デバイスとの互換性を確保しています。SYSREF ウィンドウ処理により、マルチデバイス・システムでの同期が簡単になります。

パッケージ情報

部品番号	パッケージ[(1)]	本体サイズ (公称)
DAC12DL3200	FCBGA (256)	17mm × 17mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



デュアル・チャネル・モードの周波数応答

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2021) to Revision B (June 2022) — **Page**

- Added the *Trigger Clock* section........ 72
- Deleted text *Streaming mode can be disabled by setting the ADDR_HOLD bit* from the *Streaming Mode* section........ 74
- Changed the description of Bit 2 in SYS_ALM Register Field Descriptions........ 74
- Changed the description of Bit 1 in FIFO_ALIGN Register Field Descriptions........ 74

Changes from Revision * (June 2021) to Revision A (October 2021) — **Page**

- ドキュメントのステータスを「事前情報」から「量産データ」に変更........ 1

5 Pin Configuration and Functions

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	
16	VSSCLK	VSSCLK	VSSCLK	AGND	VOUTB+	VOUTB-	AGND	VDDA18B	VDDA18A	AGND	VOUTA-	VOUTA+	AGND	AGND	RBIAS	AGND	16
15	CLK+	VDDCLK18	VDDHAF	AGND	AGND	AGND	AGND	VDDA	VDDA	AGND	AGND	AGND	AGND	AGND	ATEST	EXTIO	15
14	CLK-	VDDCLK18	VDDHAF	AGND	VEEBM18	VEEBM18	VSSCLK	VDDL2B	VDDL2A	VSSCLK	VEEAM18	VEEAM18	AGND	ALARM	SDI	$\overline{\text{SCS}}$	14
13	VSSCLK	VSSCLK	VSSCLK	VDDCLK10	VSSCLK	VDDCLK10	VSSCLK	VDDCLK10	VDDCLK10	VSSCLK	VDDCLK10	VSSCLK	AGND	SCAN_EN	SDO	SCLK	13
12	SYSREF-	VSSCLK	VDDSYS18	VSSCLK	VSSCLK	VSSL2B	VSSL2B	VDDL2B	VDDL2A	VSSL2A	VSSL2A	VSSCLK	VSSCLK	TRIGCLK	SLEEP	RESETB	12
11	SYSREF+	VSSCLK	VDDSYS18	VDDEB	VDDEB	VDDEB	VDDEB	VDDEB	VDDEA	VDDEA	VDDEA	VDDEA	VDDEA	NCOBANKSEL	SYNCB	TXENABLE	11
10	VSSCLK	VSSCLK	VQPS18	DGND	VDDDIG	DGND	VDDDIG	DGND	VDDDIG	DGND	VDDDIG	DGND	VDDDIG	VDDIO	NCOSEL3	NCOSEL2	10
9	DGND	DGND	VQPS18	VDDDIG	DGND	VDDDIG	DGND	VDDDIG	DGND	VDDDIG	DGND	VDDDIG	DGND	VDDIO	NCOSEL1	NCOSEL0	9
8	DC11-	DC11+	DC7-	DC7+	DC3-	DC3+	DCCLK+	DGND	VDDDIG	DACLK+	DA3+	DA3-	DA7+	DA7-	DA11+	DA11-	8
7	DC10-	DC10+	DC6-	DC6+	DC2-	DC2+	DCCLK-	DGND	VDDDIG	DACLK-	DA2+	DA2-	DA6+	DA6-	DA10+	DA10-	7
6	DC9-	DC9+	DC5-	DC5+	DC1-	DC1+	DCSTR+	DGND	VDDDIG	DASTR+	DA1+	DA1-	DA5+	DA5-	DA9+	DA9-	6
5	DC8-	DC8+	DC4-	DC4+	DC0-	DC0+	DCSTR-	DGND	VDDDIG	DASTR-	DA0+	DA0-	DA4+	DA4-	DA8+	DA8-	5
4	DD11-	DD11+	DD7-	DD7+	DD3-	DD3+	DDCLK+	VDDDIG	DGND	DBCLK+	DB3+	DB3-	DB7+	DB7-	DB11+	DB11-	4
3	DD10-	DD10+	DD6-	DD6+	DD2-	DD2+	DDCLK-	VDDDIG	DGND	DBCLK-	DB2+	DB2-	DB6+	DB6-	DB10+	DB10-	3
2	DD9-	DD9+	DD5-	DD5+	DD1-	DD1+	DGND	DDSTR+	DBSTR+	DGND	DB1+	DB1-	DB5+	DB5-	DB9+	DB9-	2
1	DGND	DD8-	DD8+	DD4-	DD4+	DD0-	DD0+	DDSTR-	DBSTR-	DB0+	DB0-	DB4+	DB4-	DB8+	DB8-	DGND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	

1.8V Supply
1.0V Supply
-1.8V Supply
Grounds

ACF, 256 Ball FCBGA, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	D14, D15, D16, E15, F15, G15, G16, K15, K16, L15, M15, N13, N14, N15, N16, P15, P16, T16	—	Analog supply ground, must be directly connected to DGND and VSSCLK
ALARM	P14	O	ALARM pin is asserted when an internal unmasked alarm is detected. Alarm mask is set by ALM_MASK register.
ATEST	R15	O	Analog test pin. Can be left disconnected if not used.
CLK+	A15	I	Device clock input positive terminal. There is an internal 100-Ω differential termination between CLK+ and CLK–. This input is self-biased and should be AC coupled to the clock source.
CLK–	A14	I	Device clock input negative terminal. See CLK+ description.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA0+	L5	I	LVDS bus A bit 0 data input positive terminal. There is an internal 100-Ω differential termination between DA0+ and DA0–.
DA0–	M5	I	LVDS bus A bit 0 data input negative terminal. There is an internal 100-Ω differential termination between DA0+ and DA0–.
DA1+	L6	I	LVDS bus A bit 1 data input positive terminal. There is an internal 100-Ω differential termination between DA1+ and DA1–.
DA1–	M6	I	LVDS bus A bit 1 data input negative terminal. There is an internal 100-Ω differential termination between DA1+ and DA1–.
DA10+	R7	I	LVDS bus A bit 10 data input positive terminal. There is an internal 100-Ω differential termination between DA10+ and DA10–.
DA10–	T7	I	LVDS bus A bit 10 data input negative terminal. There is an internal 100-Ω differential termination between DA10+ and DA10–.
DA11+	R8	I	LVDS bus A bit 11 data input positive terminal. There is an internal 100-Ω differential termination between DA11+ and DA11–.
DA11–	T8	I	LVDS bus A bit 11 data input negative terminal. There is an internal 100-Ω differential termination between DA11+ and DA11–.
DA2+	L7	I	LVDS bus A bit 2 data input positive terminal. There is an internal 100-Ω differential termination between DA2+ and DA2–.
DA2–	M7	I	LVDS bus A bit 2 data input negative terminal. There is an internal 100-Ω differential termination between DA2+ and DA2–.
DA3+	L8	I	LVDS bus A bit 3 data input positive terminal. There is an internal 100-Ω differential termination between DA3+ and DA3–.
DA3–	M8	I	LVDS bus A bit 3 data input negative terminal. There is an internal 100-Ω differential termination between DA3+ and DA3–.
DA4+	N5	I	LVDS bus A bit 4 data input positive terminal. There is an internal 100-Ω differential termination between DA4+ and DA4–.
DA4–	P5	I	LVDS bus A bit 4 data input negative terminal. There is an internal 100-Ω differential termination between DA4+ and DA4–.
DA5+	N6	I	LVDS bus A bit 5 data input positive terminal. There is an internal 100-Ω differential termination between DA5+ and DA5–.
DA5–	P6	I	LVDS bus A bit 5 data input negative terminal. There is an internal 100-Ω differential termination between DA5+ and DA5–.
DA6+	N7	I	LVDS bus A bit 6 data input positive terminal. There is an internal 100-Ω differential termination between DA6+ and DA6–.
DA6–	P7	I	LVDS bus A bit 6 data input negative terminal. There is an internal 100-Ω differential termination between DA6+ and DA6–.
DA7+	N8	I	LVDS bus A bit 7 data input positive terminal. There is an internal 100-Ω differential termination between DA7+ and DA7–.
DA7–	P8	I	LVDS bus A bit 7 data input negative terminal. There is an internal 100-Ω differential termination between DA7+ and DA7–.
DA8+	R5	I	LVDS bus A bit 8 data input positive terminal. There is an internal 100-Ω differential termination between DA8+ and DA8–.
DA8–	T5	I	LVDS bus A bit 8 data input negative terminal. There is an internal 100-Ω differential termination between DA8+ and DA8–.
DA9+	R6	I	LVDS bus A bit 9 data input positive terminal. There is an internal 100-Ω differential termination between DA9+ and DA9–.
DA9–	T6	I	LVDS bus A bit 9 data input negative terminal. There is an internal 100-Ω differential termination between DA9+ and DA9–.
DACLK+	K8	I	LVDS bus A data clock positive terminal. A DDR data clock is applied to DACLK+/– to capture the DA[11:0]+/– and DASTR+/– inputs. There is an internal 100-Ω differential termination between DACLK+ and DACLK–.
DACLK–	K7	I	LVDS bus A data clock negative terminal. See DACLK+ description.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DASTR+	K6	I	LVDS bus A strobe positive terminal. DASTR+/– is used to synchronize the input pointer of the interface FIFO by marking a specific sample on each LVDS bus. DAx+/– can optionally be used for this purpose instead to reduce the number of LVDS pairs, where x = (12 - LVDS_RESOLUTION). There is an internal 100-Ω differential termination between DASTR+ and DASTR–.
DASTR–	K5	I	LVDS bus A strobe negative terminal. See DASTR+ description.
DB0+	K1	I	LVDS bus B bit 0 data input positive terminal. There is an internal 100-Ω differential termination between DB0+ and DB0–.
DB0–	L1	I	LVDS bus B bit 0 data input negative terminal. There is an internal 100-Ω differential termination between DB0+ and DB0–.
DB1+	L2	I	LVDS bus B bit 1 data input positive terminal. There is an internal 100-Ω differential termination between DB1+ and DB1–.
DB1–	M2	I	LVDS bus B bit 1 data input negative terminal. There is an internal 100-Ω differential termination between DB1+ and DB1–.
DB10+	R3	I	LVDS bus B bit 10 data input positive terminal. There is an internal 100-Ω differential termination between DB10+ and DB10–.
DB10–	T3	I	LVDS bus B bit 10 data input negative terminal. There is an internal 100-Ω differential termination between DB10+ and DB10–.
DB11+	R4	I	LVDS bus B bit 11 data input positive terminal. There is an internal 100-Ω differential termination between DB11+ and DB11–.
DB11–	T4	I	LVDS bus B bit 11 data input negative terminal. There is an internal 100-Ω differential termination between DB11+ and DB11–.
DB2+	L3	I	LVDS bus B bit 2 data input positive terminal. There is an internal 100-Ω differential termination between DB2+ and DB2–.
DB2–	M3	I	LVDS bus B bit 2 data input negative terminal. There is an internal 100-Ω differential termination between DB2+ and DB2–.
DB3+	L4	I	LVDS bus B bit 3 data input positive terminal. There is an internal 100-Ω differential termination between DB3+ and DB3–.
DB3–	M4	I	LVDS bus B bit 3 data input negative terminal. There is an internal 100-Ω differential termination between DB3+ and DB3–.
DB4+	M1	I	LVDS bus B bit 4 data input positive terminal. There is an internal 100-Ω differential termination between DB4+ and DB4–.
DB4–	N1	I	LVDS bus B bit 4 data input negative terminal. There is an internal 100-Ω differential termination between DB4+ and DB4–.
DB5+	N2	I	LVDS bus B bit 5 data input positive terminal. There is an internal 100-Ω differential termination between DB5+ and DB5–.
DB5–	P2	I	LVDS bus B bit 5 data input negative terminal. There is an internal 100-Ω differential termination between DB5+ and DB5–.
DB6+	N3	I	LVDS bus B bit 6 data input positive terminal. There is an internal 100-Ω differential termination between DB6+ and DB6–.
DB6–	P3	I	LVDS bus B bit 6 data input negative terminal. There is an internal 100-Ω differential termination between DB6+ and DB6–.
DB7+	N4	I	LVDS bus B bit 7 data input positive terminal. There is an internal 100-Ω differential termination between DB7+ and DB7–.
DB7–	P4	I	LVDS bus B bit 7 data input negative terminal. There is an internal 100-Ω differential termination between DB7+ and DB7–.
DB8+	P1	I	LVDS bus B bit 8 data input positive terminal. There is an internal 100-Ω differential termination between DB8+ and DB8–.
DB8–	R1	I	LVDS bus B bit 8 data input negative terminal. There is an internal 100-Ω differential termination between DB8+ and DB8–.
DB9+	R2	I	LVDS bus B bit 9 data input positive terminal. There is an internal 100-Ω differential termination between DB9+ and DB9–.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DB9–	T2	I	LVDS bus B bit 9 data input negative terminal. There is an internal 100-Ω differential termination between DB9+ and DB9–.
DBCLK+	K4	I	LVDS bus B data clock positive terminal. A DDR data clock is applied to DBCLK+/– to capture the DB[11:0]+/– and DBSTR+/– inputs. There is an internal 100-Ω differential termination between DBCLK+ and DBCLK–.
DBCLK–	K3	I	LVDS bus B data clock negative terminal. See DBCLK+ description.
DBSTR+	J2	I	LVDS bus B strobe positive terminal. DBSTR+/– is used to synchronize the input pointer of the interface FIFO by marking a specific sample on each LVDS bus. DBx+/– can optionally be used for this purpose instead to reduce the number of LVDS pairs, where x = (12 - LVDS_RESOLUTION). There is an internal 100-Ω differential termination between DBSTR+ and DBSTR–.
DBSTR–	J1	I	LVDS bus B strobe negative terminal. See DBSTR+ description.
DC0+	F5	I	LVDS bus C bit 0 data input positive terminal. There is an internal 100-Ω differential termination between DC0+ and DC0–.
DC0–	E5	I	LVDS bus C bit 0 data input negative terminal. There is an internal 100-Ω differential termination between DC0+ and DC0–.
DC1+	F6	I	LVDS bus C bit 1 data input positive terminal. There is an internal 100-Ω differential termination between DC1+ and DC1–.
DC1–	E6	I	LVDS bus C bit 1 data input negative terminal. There is an internal 100-Ω differential termination between DC1+ and DC1–.
DC10+	B7	I	LVDS bus C bit 10 data input positive terminal. There is an internal 100-Ω differential termination between DC10+ and DC10–.
DC10–	A7	I	LVDS bus C bit 10 data input negative terminal. There is an internal 100-Ω differential termination between DC10+ and DC10–.
DC11+	B8	I	LVDS bus C bit 11 data input positive terminal. There is an internal 100-Ω differential termination between DC11+ and DC11–.
DC11–	A8	I	LVDS bus C bit 11 data input negative terminal. There is an internal 100-Ω differential termination between DC11+ and DC11–.
DC2+	F7	I	LVDS bus C bit 2 data input positive terminal. There is an internal 100-Ω differential termination between DC2+ and DC2–.
DC2–	E7	I	LVDS bus C bit 2 data input negative terminal. There is an internal 100-Ω differential termination between DC2+ and DC2–.
DC3+	F8	I	LVDS bus C bit 3 data input positive terminal. There is an internal 100-Ω differential termination between DC3+ and DC3–.
DC3–	E8	I	LVDS bus C bit 3 data input negative terminal. There is an internal 100-Ω differential termination between DC3+ and DC3–.
DC4+	D5	I	LVDS bus C bit 4 data input positive terminal. There is an internal 100-Ω differential termination between DC4+ and DC4–.
DC4–	C5	I	LVDS bus C bit 4 data input negative terminal. There is an internal 100-Ω differential termination between DC4+ and DC4–.
DC5+	D6	I	LVDS bus C bit 5 data input positive terminal. There is an internal 100-Ω differential termination between DC5+ and DC5–.
DC5–	C6	I	LVDS bus C bit 5 data input negative terminal. There is an internal 100-Ω differential termination between DC5+ and DC5–.
DC6+	D7	I	LVDS bus C bit 6 data input positive terminal. There is an internal 100-Ω differential termination between DC6+ and DC6–.
DC6–	C7	I	LVDS bus C bit 6 data input negative terminal. There is an internal 100-Ω differential termination between DC6+ and DC6–.
DC7+	D8	I	LVDS bus C bit 7 data input positive terminal. There is an internal 100-Ω differential termination between DC7+ and DC7–.
DC7–	C8	I	LVDS bus C bit 7 data input negative terminal. There is an internal 100-Ω differential termination between DC7+ and DC7–.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DC8+	B5	I	LVDS bus C bit 8 data input positive terminal. There is an internal 100-Ω differential termination between DC8+ and DC8–.
DC8–	A5	I	LVDS bus C bit 8 data input negative terminal. There is an internal 100-Ω differential termination between DC8+ and DC8–.
DC9+	B6	I	LVDS bus C bit 9 data input positive terminal. There is an internal 100-Ω differential termination between DC9+ and DC9–.
DC9–	A6	I	LVDS bus C bit 9 data input negative terminal. There is an internal 100-Ω differential termination between DC9+ and DC9–.
DCCLK+	G8	I	LVDS bus C data clock positive terminal. A DDR data clock is applied to DCCLK+/– to capture the DC[11:0]+/– and DCSTR+/– inputs. There is an internal 100-Ω differential termination between DCCLK+ and DCCLK–.
DCCLK–	G7	I	LVDS bus C data clock negative terminal. See DCCLK+ description.
DCSTR+	G6	I	LVDS bus C strobe positive terminal. DCSTR+/– is used to synchronize the input pointer of the interface FIFO by marking a specific sample on each LVDS bus. DCx+/– can optionally be used for this purpose instead to reduce the number of LVDS pairs, where x = (12 - LVDS_RESOLUTION). There is an internal 100-Ω differential termination between DCSTR+ and DCSTR–.
DCSTR–	G5	I	LVDS bus C strobe negative terminal. See DCSTR+ description.
DD0+	G1	I	LVDS bus D bit 0 data input positive terminal. There is an internal 100-Ω differential termination between DD0+ and DD0–.
DD0–	F1	I	LVDS bus D bit 0 data input negative terminal. There is an internal 100-Ω differential termination between DD0+ and DD0–.
DD1+	F2	I	LVDS bus D bit 1 data input positive terminal. There is an internal 100-Ω differential termination between DD1+ and DD1–.
DD1–	E2	I	LVDS bus D bit 1 data input negative terminal. There is an internal 100-Ω differential termination between DD1+ and DD1–.
DD10+	B3	I	LVDS bus D bit 10 data input positive terminal. There is an internal 100-Ω differential termination between DD10+ and DD10–.
DD10–	A3	I	LVDS bus D bit 10 data input negative terminal. There is an internal 100-Ω differential termination between DD10+ and DD10–.
DD11+	B4	I	LVDS bus D bit 11 data input positive terminal. There is an internal 100-Ω differential termination between DD11+ and DD11–.
DD11–	A4	I	LVDS bus D bit 11 data input negative terminal. There is an internal 100-Ω differential termination between DD11+ and DD11–.
DD2+	F3	I	LVDS bus D bit 2 data input positive terminal. There is an internal 100-Ω differential termination between DD2+ and DD2–.
DD2–	E3	I	LVDS bus D bit 2 data input negative terminal. There is an internal 100-Ω differential termination between DD2+ and DD2–.
DD3+	F4	I	LVDS bus D bit 3 data input positive terminal. There is an internal 100-Ω differential termination between DD3+ and DD3–.
DD3–	E4	I	LVDS bus D bit 3 data input negative terminal. There is an internal 100-Ω differential termination between DD3+ and DD3–.
DD4+	E1	I	LVDS bus D bit 4 data input positive terminal. There is an internal 100-Ω differential termination between DD4+ and DD4–.
DD4–	D1	I	LVDS bus D bit 4 data input negative terminal. There is an internal 100-Ω differential termination between DD4+ and DD4–.
DD5+	D2	I	LVDS bus D bit 5 data input positive terminal. There is an internal 100-Ω differential termination between DD5+ and DD5–.
DD5–	C2	I	LVDS bus D bit 5 data input negative terminal. There is an internal 100-Ω differential termination between DD5+ and DD5–.
DD6+	D3	I	LVDS bus D bit 6 data input positive terminal. There is an internal 100-Ω differential termination between DD6+ and DD6–.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DD6–	C3	I	LVDS bus D bit 6 data input negative terminal. There is an internal 100-Ω differential termination between DD6+ and DD6–.
DD7+	D4	I	LVDS bus D bit 7 data input positive terminal. There is an internal 100-Ω differential termination between DD7+ and DD7–.
DD7–	C4	I	LVDS bus D bit 7 data input negative terminal. There is an internal 100-Ω differential termination between DD7+ and DD7–.
DD8+	C1	I	LVDS bus D bit 8 data input positive terminal. There is an internal 100-Ω differential termination between DD8+ and DD8–.
DD8–	B1	I	LVDS bus D bit 8 data input negative terminal. There is an internal 100-Ω differential termination between DD8+ and DD8–.
DD9+	B2	I	LVDS bus D bit 9 data input positive terminal. There is an internal 100-Ω differential termination between DD9+ and DD9–.
DD9–	A2	I	LVDS bus D bit 9 data input negative terminal. There is an internal 100-Ω differential termination between DD9+ and DD9–.
DDCLK+	G4	I	LVDS bus D data clock positive terminal. A DDR data clock is applied to DDCLK+/– to capture the DD[11:0]+/– and DDSTR+/– inputs. There is an internal 100-Ω differential termination between DDCLK+ and DDCLK–.
DDCLK–	G3	I	LVDS bus D data clock negative terminal. See DDCLK+ description.
DDSTR+	H2	I	LVDS bus D strobe positive terminal. DDSTR+/– is used to synchronize the input pointer of the interface FIFO by marking a specific sample on each LVDS bus. DDx+/– can optionally be used for this purpose instead to reduce the number of LVDS pairs, where x = (12 - LVDS_RESOLUTION). There is an internal 100-Ω differential termination between DDSTR+ and DDSTR–.
DDSTR–	H1	I	LVDS bus D strobe negative terminal. See DDSTR+ description.
DGND	A1, A9, B9, D10, E9, F10, G2, G9, H10, H5, H6, H7, H8, J3, J4, J9, K10, K2, L9, M10, N9, T1	—	Digital supply ground, must be directly connected to AGND and VSSCLK
EXTIO	T15	O	Reference voltage output. Requires a 0.1 µF decoupling capacitor to AGND.
NCOBANKSEL	P11	I	Used to select the NCO bank updated by NCOSEL[0:3] inputs (0=A, 1=B). It is also possible to update both banks at once, in which case NCOBANKSEL can be used as a 5th bit to effectively have 32 different NCO accumulators. Latched by TRIGCLK. Internal pulldown.
NCOSEL0	T9	I	Bit 0 of NCOSEL. Internal pulldown.
NCOSEL1	R9	I	Bit 1 of NCOSEL. Internal pulldown.
NCOSEL2	T10	I	Bit 2 of NCOSEL. Internal pulldown.
NCOSEL3	R10	I	Bit 3 of NCOSEL. Internal pulldown.
RBIAS	R16	O	Full-scale output current bias is set by the resistor tied from this terminal to AGND. A 3.6-kΩ resistor is expected for 20.5 mA full scale output with default settings. The full-scale output current can be adjusted using the SPI interface by programming the COARSE_CUR_A/B and FINE_CUR_A/B register settings.
$\overline{\text{RESET}}$	T12	I	Device reset input, active low. Must be toggled after power up and application of a stable clock. Internal pullup.
SCLK	T13	I	Serial programming interface (SPI) clock input. Internal pulldown.
$\overline{\text{SCS}}$	T14	I	Serial programming interface (SPI) device select input, active low. Internal pullup.
SDI	R14	I	Serial programming interface (SPI) data input. Internal pulldown.
SDO	R13	O	Serial programming interface (SPI) data output. High-Z when not outputting SPI data.
SLEEP	R12	I	Device sleep control. The device changes to the mode specified by the SLEEP_CFG register when high. Internal pulldown.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{SYNC}}$	R11	I	Allows data LSB to be used as the LVDS sync input. Internal pullup. Has SPI register override: LSB_SYNC.
SYSREF+	A11	I	System timing reference (SYSREF) input positive terminal. This input is used to synchronize internal clock dividers and the LVDS interface FIFO output pointer. SYSREF+/– and data interface strobes must be used to achieve deterministic latency through the device. There is an internal 100-Ω differential termination between SYSREF+ and SYSREF–. This input is self-biased when AC coupled.
SYSREF–	A12	I	System timing reference (SYSREF) input negative terminal. See SYSREF+ description.
SCAN_EN	P13	I	This pin is used for factory testing. Connect to ground for normal operation. Internal pulldown.
TRIGCLK	P12	O	Trigger clock output. Rising edge latches NCOBANKSEL and NCOSEL[3:0].
TXENABLE	T11	I	Transmit enable active high input. This pin must be enabled using register TXEN_SEL. The DAC output is forced to midcode (0x0000 in 2's complement) when transmission is disabled. Internal pullup.
VDDA	H15, J15	I	1.0-V supply voltage for internal reference. Must be separate from VDDDIG for best performance.
VDDA18A	J16	I	1.8-V supply voltage for DAC channel A. Can be combined with VDDA18B, but may degrade channel-to-channel crosstalk (XTALK).
VDDA18B	H16	I	1.8-V supply voltage for DAC channel B. Can be combined with VDDA18A, but may degrade channel-to-channel crosstalk (XTALK).
VDDCLK10	D13, F13, H13, J13, L13	I	1.0-V supply voltage for internal sampling clock distribution path. Noise or spurs on this supply may degrade phase noise performance. Recommended to separate from VDDDIG and VDDA for best performance.
VDDCLK18	B14, B15	I	1.8-V supply voltage for clock (CLK+/–) input buffer. Noise or spurs on this supply may degrade phase noise performance.
VDDDIG	D9, E10, F9, G10, H3, H4, H9, J10, J5, J6, J7, J8, K9, L10, M9, N10	I	1.0-V supply voltage for digital block and LVDS input receivers. Recommended to separate from VDDA and VDDCLK for best performance.
VDDEA	J11, K11, L11, M11, N11	I	1.0-V supply voltage for channel A DAC encoder. Can be combined with VDDEB.
VDDEB	D11, E11, F11, G11, H11	I	1.0-V supply voltage for channel B DAC encoder. Can be combined with VDDEA.
VDDHAF	C14, C15	I	1.0-V supply voltage. Can be combined with VDDCLK10. Noise or spurs on this supply may degrade phase noise performance.
VDDIO	P9, P10	I	1.8-V supply for CMOS input and output terminals.
VDDL2A	J12, J14	I	1.0-V supply for DAC analog latch for channel A. Separate from VDDL2B for best channel-to-channel crosstalk (XTALK). Must be separated from VDDDIG for best performance.
VDDL2B	H12, H14	I	1.0-V supply for DAC analog latch for channel B. Separate from VDDL2A for best channel-to-channel crosstalk (XTALK). Must be separated from VDDDIG for best performance.
VDDSYS18	C11, C12	I	1.8-V supply voltage for SYSREF (SYSREF+/–) input buffer. Can be combined with VDDCLK18 when SYSREF is disabled during normal operation. This supply should be separate from VDDCLK18 when SYSREF is run continuously during operation to avoid noise and spur coupling and reduced phase noise performance.
VEEAM18	L14, M14	I	–1.8-V supply voltage for DAC current source bias for channel A. Can be combined with VEEBM18, but may degrade channel-to-channel crosstalk (XTALK).
VEEBM18	E14, F14	I	–1.8-V supply voltage for DAC current source bias for channel B. Can be combined with VEEAM18, but may degrade channel-to-channel crosstalk (XTALK).
VOUTA+	M16	O	DAC channel A analog output positive terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.
VOUTA–	L16	O	DAC channel A analog output negative terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUTB+	E16	O	DAC channel B analog output positive terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.
VOUTB–	F16	O	DAC channel B analog output negative terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.
VQPS	C9, C10	I	These pins are used for factory testing. Connect to DGND.
VSSCLK	A10, A13, A16, B10, B11, B12, B13, B16, C13, C16, D12, E12, E13, G13, G14, K13, K14, M12, M13, N12	—	Clock supply ground, must be directly connected to AGND and DGND
VSSL2A	K12, L12	—	DAC latch supply ground, must be directly connected to AGND, DGND, VSSCLK and VSSL2B through a common low-impedance ground plane.
VSSL2B	F12, G12	—	DAC latch supply ground, must be directly connected to AGND, DGND, VSSCLK and VSSL2A through a common low-impedance ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	VDDA18A, VDDA18B[2]	-0.3	2.45	V
	VEEAM18, VEEBM18[2]	-2.0	0.3	V
	VDDA[2]	-0.3	1.3	V
	VDDCLK18, VDDSYS18[3]	-0.3	2.45	V
	VDDHAF, VDDL2B, VDDL2A, VDDCLK10[3]	-0.3	1.3	V
	Supply voltage range, VDDIO18, VQPS[4]	-0.3	2.45	V
	VDDDIG, VDDEB, VDDEA[4]	-0.3	1.3	V
	Voltage between any combination of AGND, DGND and VSSCLK	-0.1	0.1	V
Input voltage	DA[11:0]+, DA[11:0]–, DACLK+, DACLK–, DASTR+, DASTR–, DB[11:0]+, DB[11:0]–, DBCLK+, DBCLK–, DBSTR+, DBSTR–, DC[11:0]+, DC[11:0]–, DCCLK+, DCCLK–, DCSTR+, DCSTR–, DD[11:0]+, DD[11:0]–, DDCLK+, DDCLK–, DDSTR+, DDSTR–[4]	-0.3	VDDIO18+0.3	V
	CLK+, CLK–[3]	-0.3	VDDCLK18+0.3	
	SYSREF+, SYSREF–[3]	-0.3	VDDSYS18+0.3	
	SCLK, $\overline{\text{SCS}}$, SDI, $\overline{\text{RESET}}$, NCOBANKSEL, NCOSEL[0:3], SLEEP, $\overline{\text{SYNC}}$, TESTMODE, TXENABLE[4]	-0.3	VDDIO18+0.3	
Output voltage	VOUTA+, VOUTA–[2]	-0.3	VDDA18A + 0.5	V
	VOUTB+, VOUTB–[2]	-0.3	VDDA18B + 0.5	
	ATEST, EXTIO, RBIAS[2]	-0.3	VDDA18A + 0.3	
	SDI, SDO, ALARM, TRIGCLK[4]	-0.3	VDDIO18 + 0.3	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured to AGND.
(3) Measured to VSSCLK.
(4) Measured to DGND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage range		VDDA18A, VDDA18B[1]	1.71	1.8	1.89	V
		VEEAM18, VEEBM18[1]	-1.89	-1.8	-1.71	V
		VDDA[1]	0.95	1	1.05	V
		VDDCLK18, VDDSYS18[2]	1.71	1.8	1.89	V
		VDDHAF, VDDL2B, VDDL2A, VDDCLK10[2]	0.95	1	1.05	V
		VDDIO18[3]	1.71	1.8	1.89	V
		VQPS[3]	0	0	1.89	V
		VDDDIG, VDDEB, VDDEA[3]	0.95	1	1.05	V
V_{CMI}	Input common mode voltage	DA[11:0]+, DA[11:0]–, DACLK+, DACLK–, DASTR+, DASTR–, DB[11:0]+, DB[11:0]–, DBCLK+, DBCLK–, DBSTR+, DBSTR–, DC[11:0]+, DC[11:0]–, DCCLK+, DCCLK–, DCSTR+, DCSTR–, DD[11:0]+, DD[11:0]–, DDCLK+, DDCLK–, DDSTR+, DDSTR–[3]	1.0	1.2	1.5	V
		CLK+, CLK–[2] [4]		0.5		
		SYSREF+, SYSREF–[2] [4] [6]	0.3	0.5	0.7	
V_{ID}	Input differential peak-to-peak voltage	DA[11:0]+ to DA[11:0]–, DACLK+ to DACLK–, DASTR+ to DASTR–, DB[11:0]+ to DB[11:0]–, DBCLK+ to DBCLK–, DBSTR+ to DBSTR–, DC[11:0]+ to DC[11:0]–, DCCLK+ to DCCLK–, DCSTR+ to DCSTR–, DD[11:0]+ to DD[11:0]–, DDCLK+ to DDCLK–, DDSTR+ to DDSTR–	350	700	1000	$mV_{PP-DIFF}$
		CLK+ to CLK–	800	1000	2000	
		SYSREF+ to SYSREF–, AC coupled with self bias	200	1000	2000	
		SYSREF+ to SYSREF–, DC coupled with Vcm between 0.3 and 0.7V, 125ps rise/fall time	200	1000	1000	
T_{DCLKH}	Data Clock input pulse high time	DACLK±, DBCLK±, DCCLK±, DDCLK ±	540			ps
T_{DCLKL}	Data Clock input pulse low time	DACLK±, DBCLK±, DCCLK±, DDCLK ±	540			ps
DC	CLK+/– duty cycle		45	50	55	%
T_A	Operating free-air temperature		-40		85	°C
T_J	Recommended operating junction temperature				105[5]	°C
T_{J-MAX}	Maximum rated operating junction temperature		125			°C

(1) Measured to AGND.
(2) Measured to VSSCLK.
(3) Measured to DGND.
(4) CLK+/- and SYSREF+/- are weakly self-biased to the optimal common mode voltage. CLK+/- should always be AC coupled to the clock source. SYSREF+/- is recommended to be AC coupled to the clock source when possible.
(5) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.
(6) Max V_{ID} for the larger Vcm range can be as large as $2V_{PP-DIFF}$ without any reliability concerns. However, it may degrade the accuracy of the SYSREF windowing by 1 bit.

6.4 Thermal Information

THERMAL METRIC(1)		DAC12DL3200 ACF or ALJ (FCBGA) 256 BALLS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	16.7	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	5.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics - DC Specifications

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, RF mode, I_{OUTFS} = 20.5mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
BITS	DAC core resolution[1]		16			bits
DNL	Differential nonlinearity	LVDS input with 12-bit resolution (1 LSB = Fullscale/4096)		±0.6		LSB
INL	Integral nonlinearity	LVDS input with 12-bit resolution (1 LSB = Fullscale/4096)		±0.9		LSB
DAC ANALOG OUTPUT (IOUTA+, IOUTA–, IOUTB+, IOUTB–)						
P_{OUTFS}	Output power	DACFS = 0xF, NRZ mode, 6.4 Gsps, f_{OUT} = 397 MHz, measured into 100-Ω load[5] [4]		1.4		dBm
I_{FS}	Switched full scale output current[2]	3.6-kΩ resistor from RBIAS to AGND, COARSE_CUR_A/B = 0xF and FINE_CUR_A/FINE_CUR_B = 0x1F		20.5		mA
		3.6-kΩ resistor from RBIAS to AGND, COARSE_CUR_A/B = 0x0 and FINE_CUR_A/FINE_CUR_B = 0x00		5.2		
$I_{FSDRIFT}$	Full scale output current temperature drift	3.6-kΩ resistor from RBIAS to AGND, COARSE_CUR_A/B = 0xF and FINE_CUR_A/FINE_CUR_B = 0x1F		0.6		uA/°C
				23		PPM/°C
V_{COMP}	Output compliance voltage range	Meaured from VOUTA+, VOUTA–, VOUTB+ or VOUTB– to AGND	1.3		2.3	V
C_{OUT}	Output capacitance	Single-ended capacitance to ground		0.04		pF
R_{TERM}	Output differential termination resistance			109		Ω
$R_{TERMDRIFT}$	Output differential termination resistance temperature coeff			-0.13		mΩ/°C
				-133		PPM/°C
CLOCK AND SYSREF INPUTS (CLKIN+, CLKIN-, SYSREF+, SYSREF-)						
R_T	Internal differential termination resistance			107		Ω
V_{CM}	Input common mode voltage			0.5		V
C_{IN}	Internal differential input capacitance			0.5		pF
REFERENCE OUTPUT (EXTIO)						
V_{REF}	Reference output voltage			0.9		V
$V_{REF-DRIFT}$	Reference output voltage drift over temperature			±34		ppm/°C
I_{REF}	Maximum reference output current sourcing capability			100		nA
LVDS INTERFACE (DAx±, DBx±, DCx±, DDx±, DxSTR±, DCLKx±)						
R_T	Internal differential termination resistance			115		Ω
CMOS INTERFACE (SCLK, $\overline{SCS}$, SDI, SDO, $\overline{RESET}$, NCOBANKSEL, NCOSEL[0:3], SLEEP, $\overline{SYNC}$)						
I_{IH}	High level input current	High level input current[6]			200	uA
I_{IL}	Low level input current	Low level input current[6]	-200			uA
V_{IH}	High level input voltage	SCLK, $\overline{SCS}$, SDI, $\overline{RESET}$, NCOBANKSEL, NCOSEL[0:3], SLEEP, SYNC, TESTMODE, TXENABLE[3]	0.7 x VDDIO18			V
V_{IL}	Low level input voltage	SCLK, $\overline{SCS}$, SDI, $\overline{RESET}$, NCOBANKSEL, NCOSEL[0:3], SLEEP, SYNC, TESTMODE, TXENABLE[3]			0.3 x VDDIO18	V
C_I	Input capacitance	Input capacitance		2		pF
V_{OH}	High level output voltage	I_{LOAD} = –400 uA	1.55			V

6.5 Electrical Characteristics - DC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, RF mode, I_{OUTFS} = 20.5mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	I_{LOAD} = 400 uA			0.25	V
TEMPERATURE SENSOR						
Res	Resolution			8		bits
Range	Digital Range		-64		127	℃
T_{ERROR}	Temperature Error	TA = 25℃, device powered down except for temperature sensor and SPI interface		±5		℃

(1) When using LVDS input, the resolution is limited by the LVDS interface to 12-bits. 16-bits only applies when using the NCO.
(2) In addition to the switched full scale output current, each output (VOUTA+, VOUTA-, VOUTB+, VOUTB-) has a fixed output current of ~ 3mA at a coarse DAC setting of 15.
(3) Measured to DGND.
(4) See DAC Output Modes for information on the frequency response of different DAC output modes. Output power vs frequency for different modes relative to NRZ mode at low frequency is shown in Single Channel: Output Power vs Output Frequency and Mode through Single Channel RTZ Mode: Output Power vs Output Frequency
(5) A 100Ω load is equivalent to a 2:1 with 50Ω single ended load
(6) With no IO supply voltage offset in connecting device.

6.6 Electrical Characteristics - Power Consumption

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDDA18}	1.8-V combined supply current for VDDA18A and VDDA18B	Dual channel, NRZ mode, f_{CLK} = 3.2 GHz, f_{DATA} = 3.2 Gsps, LVDS_MODE = 1		38	40	mA
I_{VEE}	–1.8-V combined supply current for VEEAM18 and VEEBM18		-90	-84		
I_{VDDA}	1.0-V supply current for VDDA			0.15	0.4	
$I_{VDDCLK18}$	1.8-V combined supply current for VDDCLK18 and VDDSYS18			8.0	10	
I_{VDDCLK}	1.0-V combined supply current for VDDHAF, VDDL2B, VDDL2A and VDDCLK10			597	800	
I_{VDDIO}	1.8-V supply current for VDDIO			7	10	
I_{VDDE}	1.0-V combined supply current for VDDEB and VDDEA			242	350	
I_{VDDDIG}	1.0-V supply current for VDDDIG			319	800	
P_{DIS}	Total power dissipation			1.49	1.95	W
I_{VDDA18}	1.8-V combined supply current for VDDA18A and VDDA18B	Dual channel, RF mode, f_{CLK} = 3.2 GHz, f_{DATA} = 3.2 Gsps, LVDS_MODE = 1		38	40	mA
I_{VEE}	–1.8-V combined supply current for VEEAM18 and VEEBM18		-90	-84		
I_{VDDA}	1.0-V supply current for VDDA			0.15	0.4	
$I_{VDDCLK18}$	1.8-V combined supply current for VDDCLK18 and VDDSYS18			8.0	10	
I_{VDDCLK}	1.0-V combined supply current for VDDHAF, VDDL2B, VDDL2A and VDDCLK10			597	800	
I_{VDDIO}	1.8-V supply current for VDDIO			7	10	
I_{VDDE}	1.0-V combined supply current for VDDEB and VDDEA			242	350	
I_{VDDDIG}	1.0-V supply current for VDDDIG			320	800	
P_{DIS}	Total power dissipation			1.49	1.95	W
I_{VDDA18}	1.8-V combined supply current for VDDA18A and VDDA18B	Dual channel, 2xRF mode, f_{CLK} = 6.4 GHz (double rate DAC), f_{DATA} = 3.2 Gsps, LVDS_MODE = 1		38	40	mA
I_{VEE}	–1.8-V combined supply current for VEEAM18 and VEEBM18		-90	-84		
I_{VDDA}	1.0-V supply current for VDDA			0.15	0.4	
$I_{VDDCLK18}$	1.8-V combined supply current for VDDCLK18 and VDDSYS18			7.8	10	
I_{VDDCLK}	1.0-V combined supply current for VDDHAF, VDDL2B, VDDL2A and VDDCLK10			945	1200	
I_{VDDIO}	1.8-V supply current for VDDIO			6.5	10	
I_{VDDE}	1.0-V combined supply current for VDDEB and VDDEA			400	500	
I_{VDDDIG}	1.0-V supply current for VDDDIG			400	800	
P_{DIS}	Total power dissipation			2.1	2.95	W

6.6 Electrical Characteristics - Power Consumption (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDDA18}	1.8-V combined supply current for VDDA18A and VDDA18B	Single channel, RF mode, f_{CLK} = 6.4 GHz, f_{DATA} = 6.4 Gsps, LVDS_MODE = 2		24	30	mA
I_{VEE}	–1.8-V combined supply current for VEEA– and VEEB–		-52	-48		
I_{VDDA}	1.0-V supply current for VDDA			0.15	0.4	
$I_{VDDCLK18}$	1.8-V combined supply current for VDDCLK18 and VDDSYS18			7.8	10	
I_{VDDCLK}	1.0-V combined supply current for VDDHAF, VDDL2B, VDDL2A and VDDCLK10			935	1200	
I_{VDDIO}	1.8-V supply current for VDDIO			6.5	10	
I_{VDDE}	1.0-V combined supply current for VDDEB and VDDEA			365	500	
I_{VDDDIG}	1.0-V supply current for VDDDIG			420	800	
P_{DIS}	Total power dissipation			2.05	2.75	W
I_{VDDA18}	1.8-V combined supply current for VDDA18A and VDDA18B	Dual channel, RF mode, f_{CLK} = 6.4 GHz, f_{DATA} = 6.4 Gsps, LVDS_MODE = 2, DAC A outputting data from LVDS interface and DAC B operating as DDS		38	40	mA
I_{VEE}	–1.8-V combined supply current for VEEAM18 and VEEBM18		-90	-84		
I_{VDDA}	1.0-V supply current for VDDA			0.15	0.4	
$I_{VDDCLK18}$	1.8-V combined supply current for VDDCLK18 and VDDSYS18			7.8	10	
I_{VDDCLK}	1.0-V combined supply current for VDDHAF, VDDL2B, VDDL2A and VDDCLK10			950	1200	
I_{VDDIO}	1.8-V supply current for VDDIO			6.5	10	
I_{VDDE}	1.0-V combined supply current for VDDEB and VDDEA			400	525	
I_{VDDDIG}	1.0-V supply current for VDDDIG			697	1050	
P_{DIS}	Total power dissipation			2.27	3.3	W
P_{DIS}	Total power dissipation	MODE = 0b11, SHUNTREG_EN Register (Offset = 1A0h-1A1h) = 0x0000		148		mW

6.7 Electrical Characteristics - AC Specifications

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Analog output bandwidth (-3 dB)	Excluding sinx/x response. Useable bandwidth may exceed the -3 dB point.		8		GHz
Crosstalk	Isolation between channel A (VOUTA+/–) and channel B (VOUTB+/-), dual channel (MODE0)	$f_{OUT}A$ = 97 MHz, $f_{OUT}B$ = 127 MHz, NRZ mode		-96		dBc
		$f_{OUT}A$ = 897 MHz, $f_{OUT}B$ = 927 MHz, NRZ mode		-90		dBc
		$f_{OUT}A$ = 1703 MHz, $f_{OUT}B$ = 1927 MHz, RF mode		-84		dBc
		$f_{OUT}A$ = 4097 MHz, $f_{OUT}B$ = 3927 MHz, 2xRF mode		-75		dBc
		$f_{OUT}A$ = 5803 MHz, $f_{OUT}B$ = 5927 MHz, 2xRF mode		-77		dBc
		$f_{OUT}A$ = 7897 MHz, $f_{OUT}B$ = 7927 MHz, 2xRF mode		-66		dBc
Φ_{NOISE}	Residual DAC phase noise, NRZ mode	f_{OUT} = 1597 MHz, 100-Hz offset		-104		dBc/Hz
		f_{OUT} = 1597 MHz, 1-KHz offset		-122		
		f_{OUT} = 1597 MHz, 10-kHz offset		-134		
		f_{OUT} = 1597 MHz, 100-kHz offset		-144		
		f_{OUT} = 1597 MHz, 1-MHz offset		-153		
		f_{OUT} = 1597 MHz, 10-MHz offset		-159		
	Integrated Phase Noise, SSB, 100Hz - 100MHz	f_{OUT} = 1597 MHz		-74.3		dBc
		f_{OUT} = 4597 MHz, RF Mode		-67.1		dBc
3.2 GSPS, DUAL CHANNEL, NRZ MODE						
SFDR	Spurious free dynamic range, across full Nyquist zone	f_{OUT} = 97 MHz		79		dBc
		f_{OUT} = 597 MHz		67		
		f_{OUT} = 897 MHz	60[1]	70		
		f_{OUT} = 1497 MHz		67		
IMD3	Third-order two tone intermodulation distortion	f_1 = 92 MHz, f_1 = 102 MHz, –6 dBFS/tone		-94		dBc
		f_1 = 592 MHz, f_1 = 602 MHz, –6 dBFS/tone		-77		
		f_1 = 892 MHz, f_1 = 902 MHz, –6 dBFS/tone		-73		
		f_1 = 847 MHz, f_1 = 947 MHz, –6 dBFS/tone		-72	-70	
		f_1 = 1492 MHz, f_1 = 1502 MHz, –6 dBFS/tone		-75		
NSD	Noise spectral density, sinusoidal output	f_{OUT} = 97 MHz, 70-MHz offset from f_{OUT}		-163		dBc/Hz
		f_{OUT} = 597 MHz, 70-MHz offset from f_{OUT}		-163		
		f_{OUT} = 897 MHz, 70-MHz offset from f_{OUT}		-161		
		f_{OUT} = 1497 MHz, 70-MHz offset from f_{OUT}		-157		
SPUR	Signal independent spurs	f_S / 2		-96		dBm

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NPR	Noise power ratio, peak	Signal spanning 90% of 1st Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		51		dBc
ENOB	Effective number of bits	Calculated from peak NPR, 1st Nyquist zone		10.3		bits
3.2 GSPS, DUAL CHANNEL, RTZ MODE						
SFDR	Spurious free dynamic range, across full Nyquist zone	f_{OUT} = 97 MHz		73		dBc
		f_{OUT} = 597 MHz		68		
		f_{OUT} = 897 MHz		70		
		f_{OUT} = 1497 MHz		73		
		f_{OUT} = 1703 MHz		70		
		f_{OUT} = 2303 MHz		64		
		f_{OUT} = 2603 MHz		65		
		f_{OUT} = 3103 MHz		66		
IMD3	Third-order two tone intermodulation distortion	f_1 = 92 MHz, f_1 = 102 MHz, –6 dBFS/tone		-87		dBc
		f_1 = 592 MHz, f_1 = 602 MHz, –6 dBFS/tone		-79		
		f_1 = 892 MHz, f_1 = 902 MHz, –6 dBFS/tone		-76		
		f_1 = 847 MHz, f_1 = 947 MHz, –6 dBFS/tone		-77		
		f_1 = 1492 MHz, f_1 = 1502 MHz, –6 dBFS/tone		-80		
		f_1 = 1698 MHz, f_1 = 1708 MHz, –6 dBFS/tone		-80		
		f_1 = 2298 MHz, f_1 = 2308 MHz, –6 dBFS/tone		-73		
		f_1 = 2598 MHz, f_1 = 2608 MHz, –6 dBFS/tone		-71		
		f_1 = 2253 MHz, f_1 = 2353 MHz, –6 dBFS/tone		-73		
		f_1 = 3098 MHz, f_1 = 3108 MHz, –6 dBFS/tone		-73		
NSD	Noise spectral density, sinusoidal output	f_{OUT} = 97 MHz, 70-MHz offset from f_{OUT}		-153		dBc/Hz
		f_{OUT} = 597 MHz, 70-MHz offset from f_{OUT}		-158		
		f_{OUT} = 897 MHz, 70-MHz offset from f_{OUT}		-157		
		f_{OUT} = 1497 MHz, 70-MHz offset from f_{OUT}		-154		
		f_{OUT} = 1703 MHz, 70-MHz offset from f_{OUT}		-153		
		f_{OUT} = 2303 MHz, 70-MHz offset from f_{OUT}		-151		
		f_{OUT} = 2603 MHz, 70-MHz offset from f_{OUT}		-150		
		f_{OUT} = 3103 MHz, 70-MHz offset from f_{OUT}		-147		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPUR	Signal independent spurs	f_S / 2		-100		dBm
		f_S		-65		
NPR	Noise power ratio, peak	Signal spanning 90% of 1st Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		48		dBc
		Signal spanning 90% of 2nd Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		42		
ENOB	Effective number of bits	Calculated from peak NPR, 1st Nyquist zone		9.7		bits
ENOB	Effective number of bits	Calculated from peak NPR, 2nd Nyquist zone		8.7		
3.2 GSPS, DUAL CHANNEL, RF MODE						
SFDR	Spurious free dynamic range, across full Nyquist zone	f_{OUT} = 1703 MHz		67		dBc
		f_{OUT} = 2303 MHz		66		
		f_{OUT} = 2603 MHz		65		
		f_{OUT} = 3103 MHz		57		
		f_{OUT} = 3297 MHz		58		
		f_{OUT} = 3797 MHz		59		
		f_{OUT} = 4097 MHz		61		
		f_{OUT} = 4697 MHz		63		
IMD3	Third-order two tone intermodulation distortion	f_1 = 1698 MHz, f_1 = 1708 MHz, –6 dBFS/tone		-73		dBc
		f_1 = 2298 MHz, f_1 = 2308 MHz, –6 dBFS/tone		-76		
		f_1 = 2598 MHz, f_1 = 2608 MHz, –6 dBFS/tone		-75		
		f_1 = 2253 MHz, f_1 = 2353 MHz, –6 dBFS/tone		-80		
		f_1 = 3098 MHz, f_1 = 3108 MHz, –6 dBFS/tone		-64		
		f_1 = 3292 MHz, f_1 = 3302 MHz, –6 dBFS/tone		-63		
		f_1 = 3792 MHz, f_1 = 3802 MHz, –6 dBFS/tone		-68		
		f_1 = 4092 MHz, f_1 = 4102 MHz, –6 dBFS/tone		-69		
		f_1 = 4047 MHz, f_1 = 4147 MHz, –6 dBFS/tone		-72		
		f_1 = 4692 MHz, f_1 = 4702 MHz, –6 dBFS/tone		-62		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise spectral density, sinusoidal output	f_{OUT} = 1703 MHz, 70-MHz offset from f_{OUT}		-156		dBc/Hz
		f_{OUT} = 2303 MHz, 70-MHz offset from f_{OUT}		-155		
		f_{OUT} = 2603 MHz, 70-MHz offset from f_{OUT}		-154		
		f_{OUT} = 3103 MHz, 70-MHz offset from f_{OUT}		-152		
		f_{OUT} = 3297 MHz, 70-MHz offset from f_{OUT}		-151		
		f_{OUT} = 3797 MHz, 70-MHz offset from f_{OUT}		-151		
		f_{OUT} = 4097 MHz, 70-MHz offset from f_{OUT}		-150		
		f_{OUT} = 4697 MHz, 70-MHz offset from f_{OUT}		-147		
SPUR	Signal independent spurs	f_S / 2		-96		dBm
		f_S		-63		
		3 * f_S / 2		-102		
NPR	Noise power ratio, peak	Signal spanning 90% of 2nd Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		47		dBc
		Signal spanning 90% of 3rd Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		44		
ENOB	Effective number of bits	Calculated from peak NPR, 2nd Nyquist zone		9.5		bits
		Calculated from peak NPR, 3rd Nyquist zone		9.1		
3.2 GSPS, DUAL CHANNEL, 2xRF MODE						
SFDR	Spurious free dynamic range, across full Nyquist zone	f_{OUT} = 3297 MHz		60		dBc
		f_{OUT} = 3797 MHz		57		
		f_{OUT} = 4097 MHz		59		
		f_{OUT} = 4697 MHz		61		
		f_{OUT} = 4903 MHz		59		
		f_{OUT} = 5503 MHz		56		
		f_{OUT} = 5803 MHz		54		
		f_{OUT} = 6303 MHz		59		
		f_{OUT} = 6497 MHz		59		
		f_{OUT} = 6997 MHz		62		
		f_{OUT} = 7297 MHz		58		
		f_{OUT} = 7897 MHz		54		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	Third-order two tone intermodulation distortion	f_1 = 3292 MHz, f_1 = 3302 MHz, –6 dBFS/tone		-62		dBc
		f_1 = 3792 MHz, f_1 = 3802 MHz, –6 dBFS/tone		-63		
		f_1 = 4092 MHz, f_1 = 4102 MHz, –6 dBFS/tone		-63		
		f_1 = 4047 MHz, f_1 = 4147 MHz, –6 dBFS/tone		-63		
		f_1 = 4692 MHz, f_1 = 4702 MHz, –6 dBFS/tone		-62		
		f_1 = 4898 MHz, f_1 = 4908 MHz, –6 dBFS/tone		-61		
		f_1 = 5498 MHz, f_1 = 5508 MHz, –6 dBFS/tone		-58		
		f_1 = 5798 MHz, f_1 = 5808 MHz, –6 dBFS/tone		-60		
		f_1 = 5453 MHz, f_1 = 5553 MHz, –6 dBFS/tone		-62		
		f_1 = 6298 MHz, f_1 = 6308 MHz, –6 dBFS/tone		-61		
		f_1 = 6492 MHz, f_1 = 6502 MHz, –6 dBFS/tone		-61		
		f_1 = 6992 MHz, f_1 = 7002 MHz, –6 dBFS/tone		-60		
		f_1 = 7292 MHz, f_1 = 7302 MHz, –6 dBFS/tone		-57		
		f_1 = 7892 MHz, f_1 = 7902 MHz, –6 dBFS/tone		-48		
NSD	Noise spectral density, sinusoidal output	f_{OUT} = 3297 MHz, 70-MHz offset from f_{OUT}		-146		dBc/Hz
		f_{OUT} = 3797 MHz, 70-MHz offset from f_{OUT}		-149		
		f_{OUT} = 4097 MHz, 70-MHz offset from f_{OUT}		-150		
		f_{OUT} = 4697 MHz, 70-MHz offset from f_{OUT}		-148		
		f_{OUT} = 4903 MHz, 70-MHz offset from f_{OUT}		-148		
		f_{OUT} = 5503 MHz, 70-MHz offset from f_{OUT}		-149		
		f_{OUT} = 5803 MHz, 70-MHz offset from f_{OUT}		-147		
		f_{OUT} = 6303 MHz, 70-MHz offset from f_{OUT}		-142		
		f_{OUT} = 6497 MHz, 70-MHz offset from f_{OUT}		-142		
		f_{OUT} = 6997 MHz, 70-MHz offset from f_{OUT}		-146		
		f_{OUT} = 7297 MHz, 70-MHz offset from f_{OUT}		-145		
		f_{OUT} = 7897 MHz, 70-MHz offset from f_{OUT}		-139		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPUR	Signal independent spurs	f_S		-60		dBm
		$3 * f_S / 2$		-101		
		$2 * f_S$		-66		
		$5 * f_S / 2$		-109		
		$3 * f_S$		-46		
NPR	Noise power ratio, peak	Signal spanning 90% of 3rd Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		42		dBc
		Signal spanning 90% of 4th Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		41		
		Signal spanning 90% of 5th Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		33		
ENOB	Effective number of bits	Calculated from peak NPR, 3rd Nyquist zone		8.7		bits
		Calculated from peak NPR, 4th Nyquist zone		8.6		
		Calculated from peak NPR, 5th Nyquist zone		7.2		
6.4 GSPS, SINGLE CHANNEL, NRZ MODE						
SFDR	Spurious free dynamic range, across full Nyquist zone	f_{OUT} = 97 MHz		80		dBc
		f_{OUT} = 897 MHz	60[1]	63		
		f_{OUT} = 1697 MHz		71		
		f_{OUT} = 2497 MHz		67		
		f_{OUT} = 3097 MHz		55		
IMD3	Third-order two tone intermodulation distortion	f_1 = 92 MHz, f_1 = 102 MHz, –6 dBFS/tone		-93		dBc
		f_1 = 892 MHz, f_1 = 902 MHz, –6 dBFS/tone		-69		
		f_1 = 847 MHz, f_1 = 947 MHz, –6 dBFS/tone		-71	-68	
		f_1 = 1692 MHz, f_1 = 1702 MHz, –6 dBFS/tone		-71		
		f_1 = 2492 MHz, f_1 = 2502 MHz, –6 dBFS/tone		-65		
		f_1 = 2447 MHz, f_1 = 2547 MHz, –6 dBFS/tone		-69		
		f_1 = 3092 MHz, f_1 = 3102 MHz, –6 dBFS/tone		-59		
NSD	Noise spectral density, sinusoidal output	f_{OUT} = 97 MHz, 70-MHz offset from f_{OUT}		-165		dBc/Hz
		f_{OUT} = 897 MHz, 70-MHz offset from f_{OUT}		-162		
		f_{OUT} = 1697 MHz, 70-MHz offset from f_{OUT}		-157		
		f_{OUT} = 2497 MHz, 70-MHz offset from f_{OUT}		-154		
		f_{OUT} = 3097 MHz, 70-MHz offset from f_{OUT}		-151		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPUR	Signal independent spurs	f_S / 2		-88		dBm
NPR	Noise power ratio, peak	Signal spanning 90% of 1st Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		48		dBc
ENOB	Effective number of bits	Calculated from peak NPR, 1st Nyquist zone		9.7		bits
6.4 GSPS, SINGLE CHANNEL, RTZ MODE						
SFDR	Spurious free dynamic range, across full Nyquist zone	f_{OUT} = 97 MHz		73		dBc
		f_{OUT} = 897 MHz		56		
		f_{OUT} = 1697 MHz		68		
		f_{OUT} = 2497 MHz		65		
		f_{OUT} = 3097 MHz		56		
		f_{OUT} = 3303 MHz		52		
		f_{OUT} = 3903 MHz		56		
		f_{OUT} = 4703 MHz		60		
		f_{OUT} = 5503 MHz		52		
		f_{OUT} = 6303 MHz		59		
IMD3	Third-order two tone intermodulation distortion	f_1 = 92 MHz, f_1 = 102 MHz, –6 dBFS/tone		-86		dBc
		f_1 = 892 MHz, f_1 = 902 MHz, –6 dBFS/tone		-66		
		f_1 = 847 MHz, f_1 = 947 MHz, –6 dBFS/tone		-69		
		f_1 = 1692 MHz, f_1 = 1702 MHz, –6 dBFS/tone		-69		
		f_1 = 2492 MHz, f_1 = 2502 MHz, –6 dBFS/tone		-66		
		f_1 = 2447 MHz, f_1 = 2547 MHz, –6 dBFS/tone		-65		
		f_1 = 3092 MHz, f_1 = 3102 MHz, –6 dBFS/tone		-59		
		f_1 = 3298 MHz, f_1 = 3308 MHz, –6 dBFS/tone		-59		
		f_1 = 3898 MHz, f_1 = 3908 MHz, –6 dBFS/tone		-59		
		f_1 = 3853 MHz, f_1 = 3953 MHz, –6 dBFS/tone		-63		
		f_1 = 4698 MHz, f_1 = 4708 MHz, –6 dBFS/tone		-64		
		f_1 = 5498 MHz, f_1 = 5508 MHz, –6 dBFS/tone		-55		
		f_1 = 5453 MHz, f_1 = 5553 MHz, –6 dBFS/tone		-63		
		f_1 = 6298 MHz, f_1 = 6308 MHz, –6 dBFS/tone		-66		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise spectral density, sinusoidal output	f_{OUT} = 97 MHz, 70-MHz offset from f_{OUT}		-149		dBc/Hz
		f_{OUT} = 897 MHz, 70-MHz offset from f_{OUT}		-155		
		f_{OUT} = 1697 MHz, 70-MHz offset from f_{OUT}		-154		
		f_{OUT} = 2497 MHz, 70-MHz offset from f_{OUT}		-152		
		f_{OUT} = 3097 MHz, 70-MHz offset from f_{OUT}		-149		
		f_{OUT} = 3303 MHz, 70-MHz offset from f_{OUT}		-148		
		f_{OUT} = 3903 MHz, 70-MHz offset from f_{OUT}		-149		
		f_{OUT} = 4703 MHz, 70-MHz offset from f_{OUT}		-147		
		f_{OUT} = 5503 MHz, 70-MHz offset from f_{OUT}		-147		
		f_{OUT} = 6303 MHz, 70-MHz offset from f_{OUT}		-142		
SPUR	Signal independent spurs	f_S / 2		-88		dBm
		f_S		-55		
NPR	Noise power ratio, peak	Signal spanning 90% of 1st Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		40		dBc
		Signal spanning 90% of 2nd Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		32		
ENOB	Effective number of bits	Calculated from peak NPR, 1st Nyquist zone		8.4		bits
		Calculated from peak NPR, 2nd Nyquist zone		7.1		
6.4 GSPS, SINGLE CHANNEL, RF MODE						
SFDR	Spurious free dynamic range, across full Nyquist zone	f_{OUT} = 3303 MHz		57		dBc
		f_{OUT} = 3903 MHz		57		
		f_{OUT} = 4703 MHz		58		
		f_{OUT} = 5503 MHz	50[1]	56		
		f_{OUT} = 6303 MHz		56		
		f_{OUT} = 6497 MHz		54		
		f_{OUT} = 7297 MHz		50		
		f_{OUT} = 8097 MHz		50		
		f_{OUT} = 8897 MHz		54		
		f_{OUT} = 9497 MHz		52		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	Third-order two tone intermodulation distortion	f_1 = 3298 MHz, f_1 = 3308 MHz, –6 dBFS/tone		-58		dBc
		f_1 = 3898 MHz, f_1 = 3908 MHz, –6 dBFS/tone		-63		
		f_1 = 3853 MHz, f_1 = 3953 MHz, –6 dBFS/tone		-62		
		f_1 = 4698 MHz, f_1 = 4708 MHz, –6 dBFS/tone		-62		
		f_1 = 5498 MHz, f_1 = 5508 MHz, –6 dBFS/tone		-54		
		f_1 = 5453 MHz, f_1 = 5553 MHz, –6 dBFS/tone		-60	-53	
		f_1 = 6298 MHz, f_1 = 6308 MHz, –6 dBFS/tone		-61		
		f_1 = 6492 MHz, f_1 = 6502 MHz, –6 dBFS/tone		-60		
		f_1 = 7292 MHz, f_1 = 7302 MHz, –6 dBFS/tone		-51		
		f_1 = 8092 MHz, f_1 = 8102 MHz, –6 dBFS/tone		-52		
		f_1 = 8892 MHz, f_1 = 8902 MHz, –6 dBFS/tone		-56		
		f_1 = 9492 MHz, f_1 = 9502 MHz, –6 dBFS/tone		-46		
NSD	Noise spectral density, sinusoidal output	f_{OUT} = 3303 MHz, 70-MHz offset from f_{OUT}		-151		dBc/Hz
		f_{OUT} = 3903 MHz, 70-MHz offset from f_{OUT}		-152		
		f_{OUT} = 4703 MHz, 70-MHz offset from f_{OUT}		-150		
		f_{OUT} = 5503 MHz, 70-MHz offset from f_{OUT}		-150		
		f_{OUT} = 6303 MHz, 70-MHz offset from f_{OUT}		-145		
		f_{OUT} = 6497 MHz, 70-MHz offset from f_{OUT}		-145		
		f_{OUT} = 7297 MHz, 70-MHz offset from f_{OUT}		-147		
		f_{OUT} = 8097 MHz, 70-MHz offset from f_{OUT}		-145		
		f_{OUT} = 8897 MHz, 70-MHz offset from f_{OUT}		-143		
		f_{OUT} = 9497 MHz, 70-MHz offset from f_{OUT}		-137		
SPUR	Signal independent spurs	f_S / 2		-88		dBm
		f_S		-55		
		3 * f_S / 2		-88		

6.7 Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NPR	Noise power ratio, peak	Signal spanning 90% of 2nd Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		42		dBc
		Signal spanning 90% of 3rd Nyquist zone, notch at center of Nyquist zone of 5% of Nyquist zone		32		
ENOB	Effective number of bits	Calculated from peak NPR, 2nd Nyquist zone		8.7		bits
		Calculated from peak NPR, 3rd Nyquist zone		7.1		

(1) SFDR MIN specification is the worst of HD2, HD3 and HD5.

6.8 Timing Requirements

Typical values at TA = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

			MIN	NOM	MAX	UNIT
INPUT CLOCK (CLKIN+, CLKIN-)						
f_{CLK}	Input clock frequency		800		6400	MHz
LVDS INTERFACE						
f_{BIT}	Dx[11:0]+/- DDR data rate				1600	Mbps
UI	Dx[11:0]+/- DDR data unit interval		625			ps
$t_{SU(LVDS)}$	Setup time, Dx[11:0]+/– and DxSTR+/– valid to DxCLK+/– rising or falling edge	All LVDS buses		-375	-240	ps
$t_{H(LVDS)}$	Hold time, DxCLK+/– rising or falling edge to Dx[11:0]+/– and DxSTR+/– transition	All LVDS buses		495	565	ps
f_{DCLK}	DxCLK+/- DDR data clock frequency				800	MHz
TRIGGER CLOCK						
$F_{TRIGCLKMAX}$	Trigger clock maximum frequency			100		MHz
$t_{S\_TRIGCLK}$	setup time for NCO_SEL[3:0] and NCOBANKSEL to TRIGCLK rising edge			3.5		ns
$t_{H\_TRIGCLK}$	hold time for NCO_SEL[3:0] and NCOBANKSEL to TRIGCLK rising edge			-1.5		ns
SYSREF (SYSREF+, SYSREF-)						
$t_{INV(SYSREF)}$	Width of invalid SYSREF capture region of CLK± period, indicating setup or hold time violation, as measured by SYSREF_POS status register(1)			48		ps
$t_{INV(TEMP)}$	Drift of invalid SYSREF capture region over temperature, positive number indicates a shift toward MSB of SYSREF_POS register			-0.12		ps/°C
$t_{INV(VDDHAF)}$	Drift of invalid SYSREF capture region over VDDHAF supply voltage, positive number indicates a shift toward MSB of SYSREF_POS register			0.33		ps/mV
$t_{STEP(SP)}$	Delay of SYSREF_SEL LSB	SYSREF_ZOOM = 0		22		ps
		SYSREF_ZOOM = 1		9		
$t_{(PH\_SYS)}$	Minimum SYSREF± assertion duration after SYSREF± rising edge event			4		ns
RESET						
t_{RESET}	Minimum $\overline{\text{RESET}}$ pulse width			25		ns

(1) Use SYSREF_POS to select an optimal SYSREF_SEL value for the SYSREF capture, see the section Multi-Device Synchronization (SYSREF+/-) for more information on SYSREF windowing. The invalid region, specified by $t_{INV(SYSREF)}$, indicates the portion of the CLK± period(t_{CLK}), as measured by SYSREF_SEL, that may result in a setup and hold violation. Verify that the timing skew between SYSREF± and CLK± over system operating conditions from the nominal conditions (that used to find optimal SYSREF_SEL) does not result in the invalid region occurring at the selected SYSREF_SEL position in SYSREF_POS, otherwise a temperature dependent SYSREF_SEL selection may be needed to track the skew between CLK± and SYSREF±.

6.9 Switching Characteristics

Typical values at TA = +25°C, minimum and maximum values over operating free-air temperature range, typical supply voltages, single channel (MODE2) at 6.4 GSPS, single tone amplitude = 0 dBFS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LATENCY						
T_{DAC}	DAC sampling period			1 / f_{CLK}		s
t_{LAT}	digital input to DAC output sample latency	single clock mode, 4 LVDS banks for 1 DAC		35.5		T_{DAC}
		single clock mode, 2 LVDS banks per DAC		20.5		
		single clock mode, 1 LVDS bank per DAC		12.5		
		dual clock mode, 2 LVDS banks per DAC		35.5		
		dual clock mode, 1 LVDS bank per DAC		20.5		
t_{PDI}	Input clock rising edge cross-over to output sample cross-over			680		ps
SERIAL PROGRAMMING INTERFACE						
$F_{s\_c\_r}$	serial clock frequency reading				100	MHz
$F_{s\_c\_w}$	serial clock frequency writing				200	MHz
F_{s_cts}	serial clock frequency temp sensor				1	MHz
t_{P_W}	serial clock period for writing		5			ns
t_{P_R}	serial clock period for reading		10			ns
t_{PH}	serial clock pulse width high		2			ns
t_{PL}	serial clock pulse width low		2			ns
t_{SU}	SDI setup		1			ns
t_H	SDI hold		1			ns
t_{IZ}	SDI TRI-STATE				1	ns
t_{ODZ}	SDO driven to TRI-STATE	200 fF load	0		1.5	ns
t_{OZD}	SDO TRI-STATE to driven	200 fF load	0		1.5	ns
t_{OD}	SDO output delay	200 fF load	0		6	ns
t_{CSS}	$\overline{SCS}$ setup		1			ns
t_{CSH}	$\overline{SCS}$ hold		1			ns
t_{IAG}	Inter-access gap		1			ns

6.10 Typical Characteristics

Typical values at T_A = 25°C, nominal supply voltages, COARSE_CUR_A/B = 0xFF (I_{FS_SWITCH} = 21 mA), output from VOUTA± in single-channel modes, A_{OUT} = 0 dBFS, f_{CLK} = 3.2 GHz in dual channel NRZ, RTZ and RF mode, f_{CLK} = 6.4 GHz in dual channel 2xRF and single channel NRZ, RTZ and RF mode, filtered, SHUNTREF_EN = 0x0FFF (unless otherwise noted);

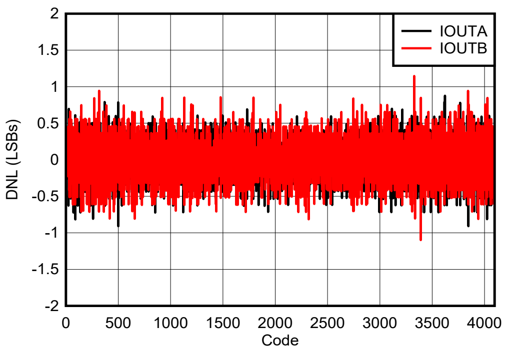


図 6-1. Output Current DNL vs Code

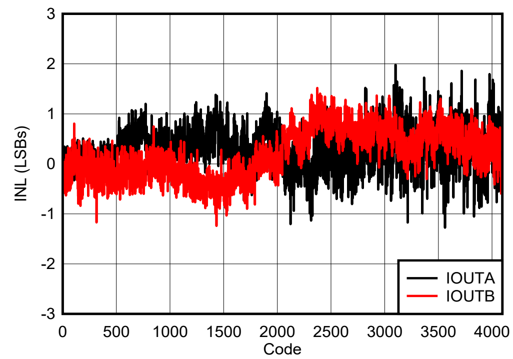
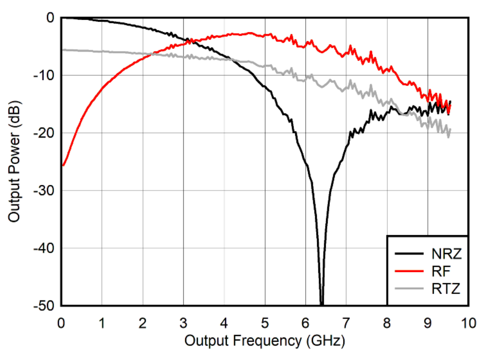
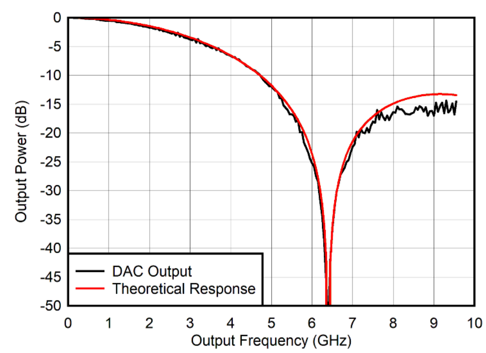


図 6-2. Output Current INL vs Code



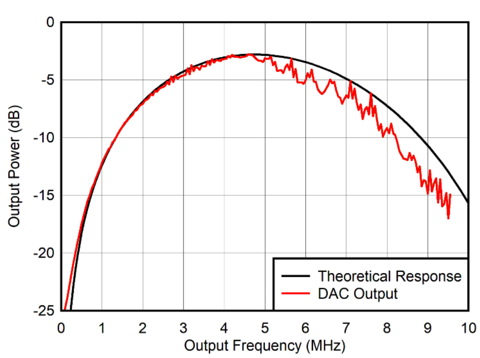
f_{CLK} = 6.4 GHz, relative to NRZ mode at low frequency, ripple at > 5 GHz are due to cable reflections

図 6-3. Single Channel: Output Power vs Output Frequency and Mode



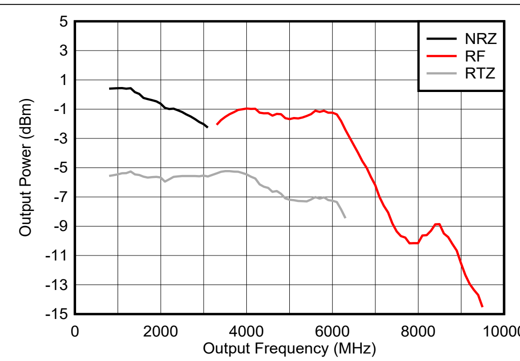
f_{CLK} = 6.4 GHz, relative to NRZ mode at low frequency, ripple at > 5 GHz are due to cable reflections

図 6-4. Single Channel NRZ Mode: Output Power vs Output Frequency



f_{CLK} = 6.4 GHz, relative to NRZ mode at low frequency, ripple at > 5 GHz are due to cable reflections

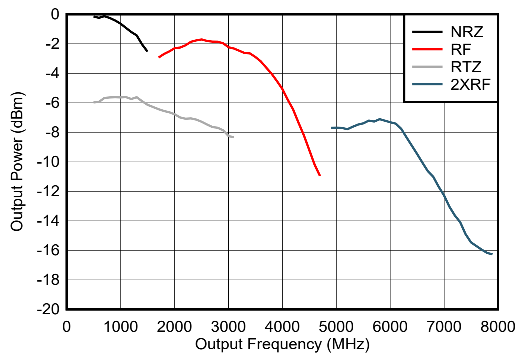
図 6-5. Single Channel RF Mode: Output Power vs Output Frequency



F_{SAMPLE} = 6.4GSPS, cable and transformer loss removed

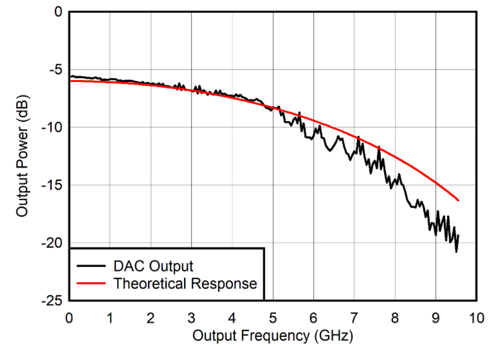
図 6-6. Single Channel Mode: DAC12DL3200EVM Output Power vs Output Frequency

6.10 Typical Characteristics (continued)



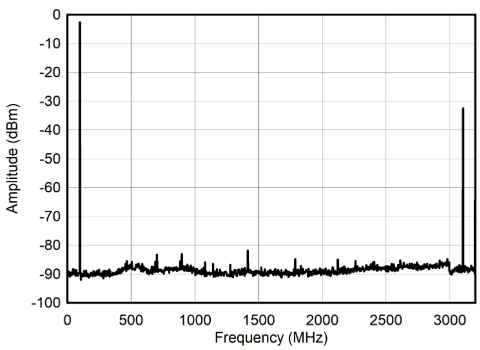
F_{SAMPLE} = 3.2 GSPS, cable and transformer loss removed

図 6-7. Dual Channel Modes: DAC12DL3200EVM Output Power vs Output Frequency



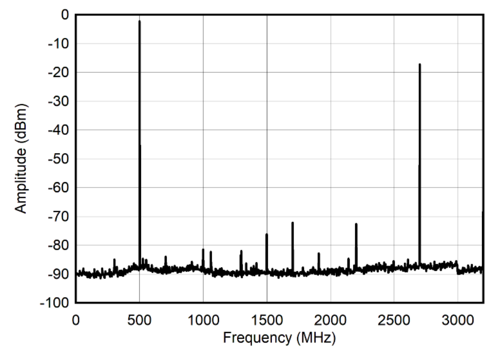
f_{CLK} = 6.4 GHz, relative to NRZ mode at low frequency, ripple at > 5 GHz are due to cable reflections

図 6-8. Single Channel RTZ Mode: Output Power vs Output Frequency



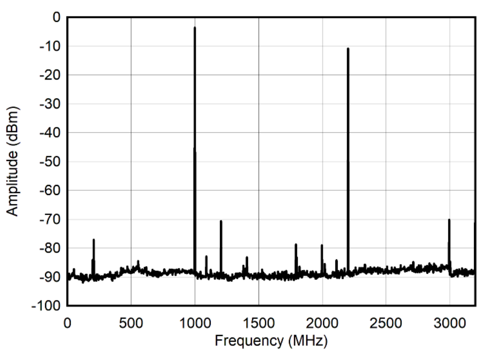
f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-9. Dual Channel NRZ Mode: Single Tone Spectrum at 100 MHz



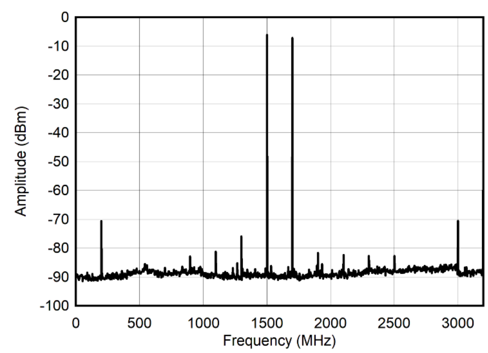
f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-10. Dual Channel NRZ Mode: Single Tone Spectrum at 500 MHz



f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

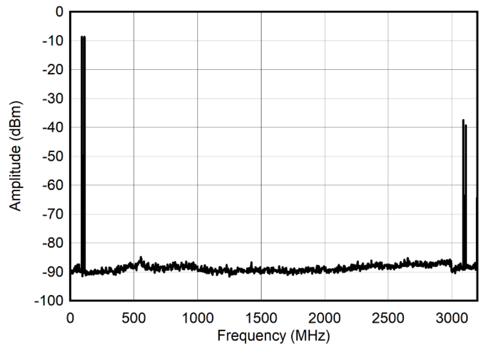
図 6-11. Dual Channel NRZ Mode: Single Tone Spectrum at 1 GHz



f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

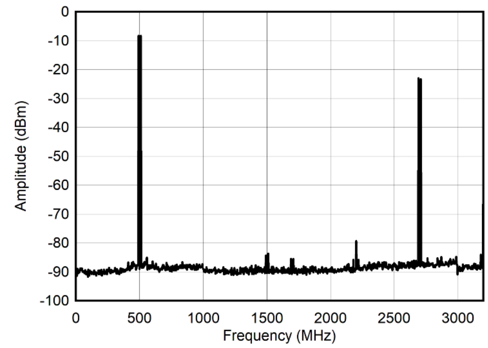
図 6-12. Dual Channel NRZ Mode: Single Tone Spectrum at 1.5 GHz

6.10 Typical Characteristics (continued)



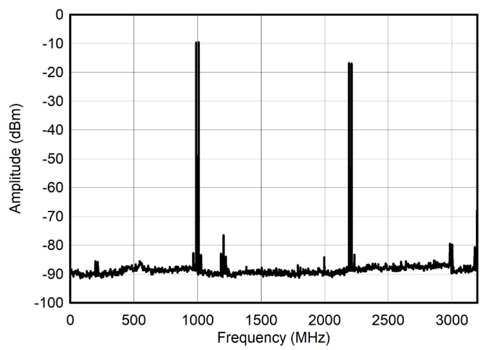
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-13. Dual Channel NRZ Mode: Dual Tone Spectrum at 100 MHz ± 10 MHz



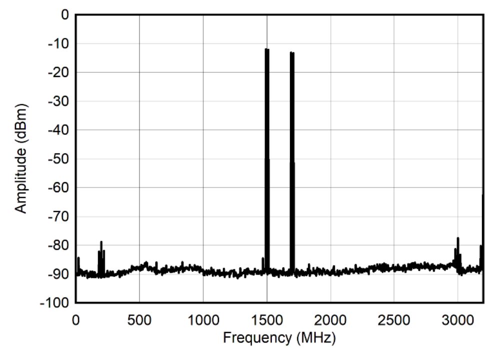
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-14. Dual Channel NRZ Mode: Dual Tone Spectrum at 500 MHz ± 10 MHz



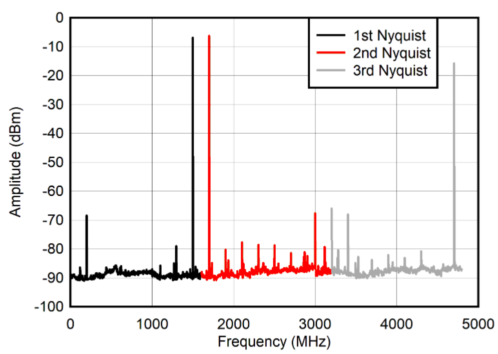
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-15. Dual Channel NRZ Mode: Dual Tone Spectrum at 1 GHz ± 10 MHz



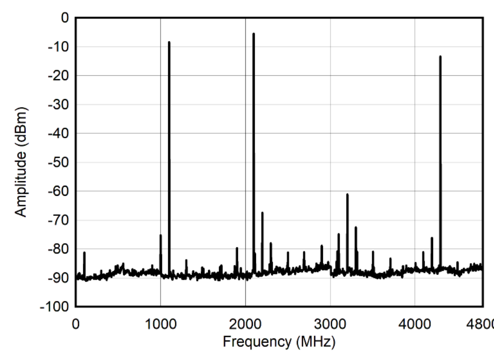
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-16. Dual Channel NRZ Mode: Dual Tone Spectrum at 1.5 GHz ± 10 MHz



f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

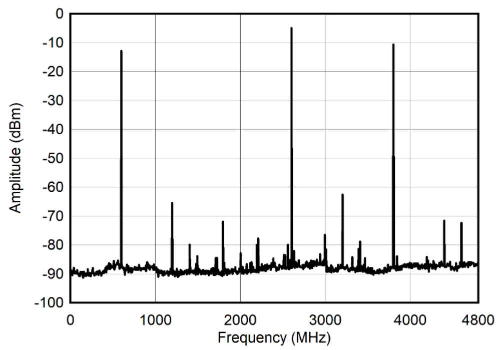
図 6-17. Dual Channel RF Mode: Single Tone Spectrum at 1.7 GHz



f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

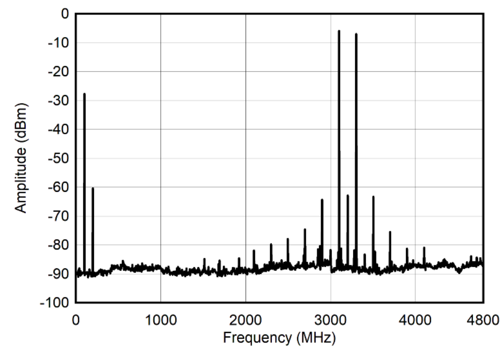
図 6-18. Dual Channel RF Mode: Single Tone Spectrum at 2.1 GHz

6.10 Typical Characteristics (continued)



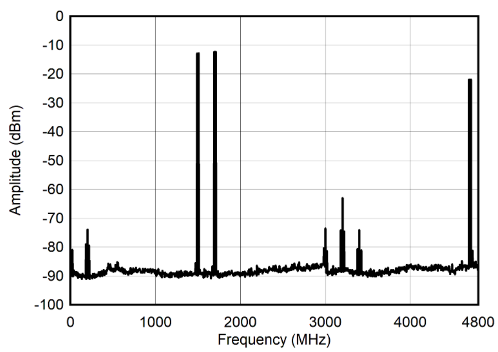
f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

図 6-19. Dual Channel RF Mode: Single Tone Spectrum at 2.6 GHz



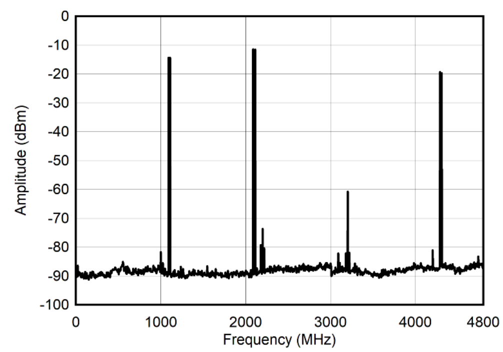
f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

図 6-20. Dual Channel RF Mode: Single Tone Spectrum at 3.1 GHz



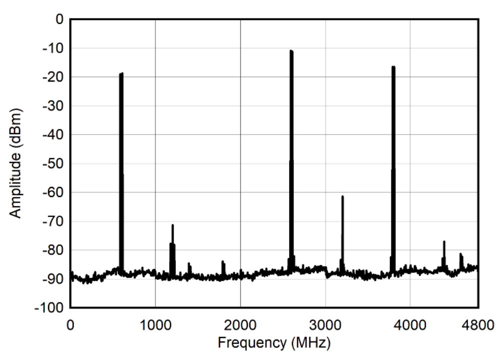
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

図 6-21. Dual Channel RF Mode: Dual Tone Spectrum at 1.7G Hz ± 10 MHz



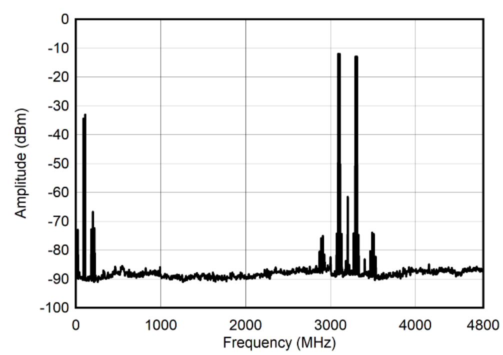
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

図 6-22. Dual Channel RF Mode: Dual Tone Spectrum at 2.1 GHz ± 10 MHz



each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

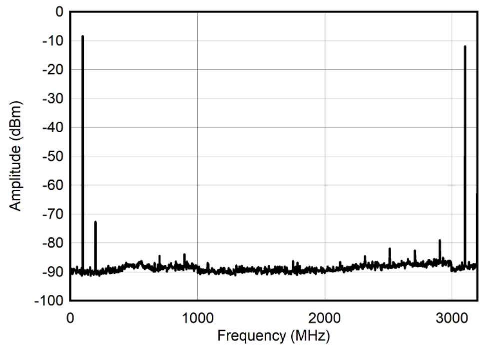
図 6-23. Dual Channel RF Mode: Dual Tone Spectrum at 2.6 GHz ± 10 MHz



each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st, 2nd and 3rd Nyquist Zones Displayed

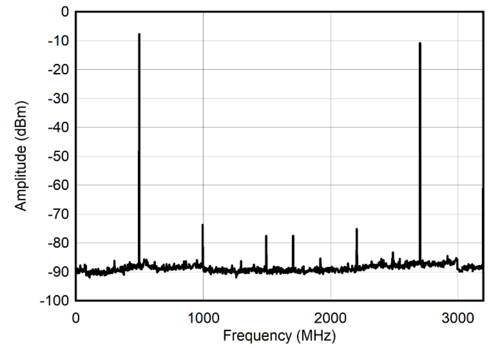
図 6-24. Dual Channel RF Mode: Dual Tone Spectrum at 3.1 GHz ± 10 MHz

6.10 Typical Characteristics (continued)



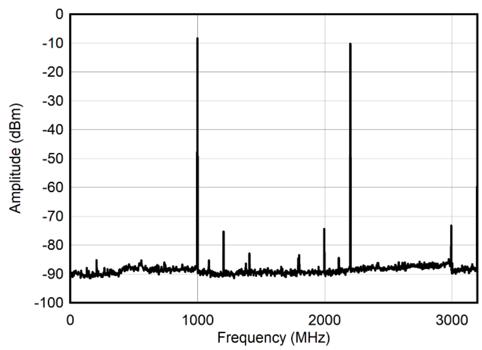
f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-25. Dual Channel RTZ Mode: Single Tone Spectrum at 100 MHz



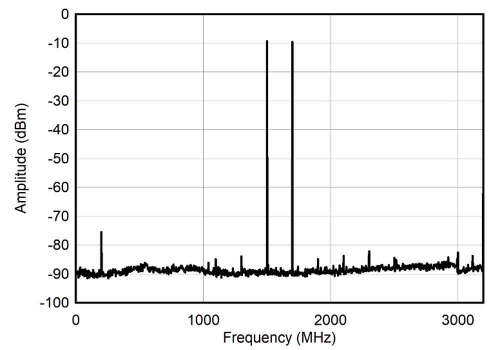
f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-26. Dual Channel RTZ Mode: Single Tone Spectrum at 500 MHz



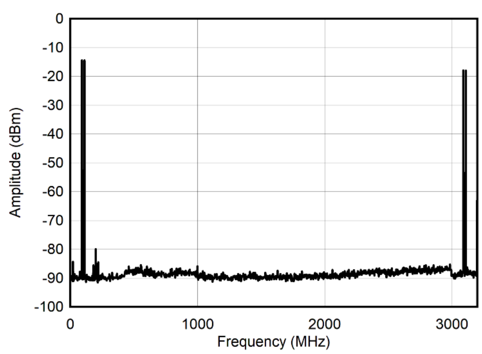
f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-27. Dual Channel RTZ Mode: Single Tone Spectrum at 1 GHz



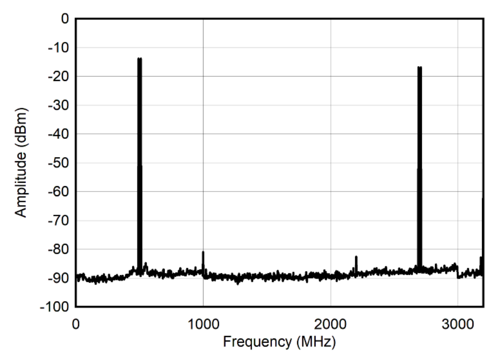
f_{CLK} = 3.2G Hz, 1st and 2nd Nyquist Zones Displayed

図 6-28. Dual Channel RTZ Mode: Single Tone Spectrum at 1.5 GHz



each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

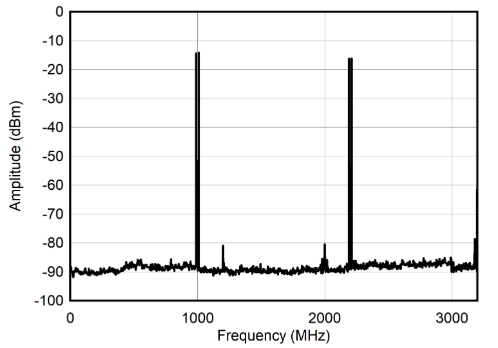
図 6-29. Dual Channel RTZ Mode: Dual Tone Spectrum at 100 MHz ± 10 MHz



each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

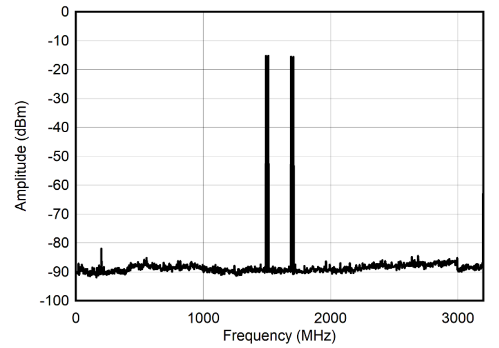
図 6-30. Dual Channel RTZ Mode: Dual Tone Spectrum at 500 MHz ± 10 MHz

6.10 Typical Characteristics (continued)



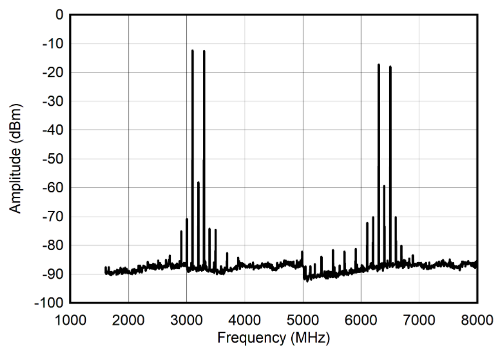
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-31. Dual Channel RTZ Mode: Dual Tone Spectrum at 1 GHz ± 10 MHz



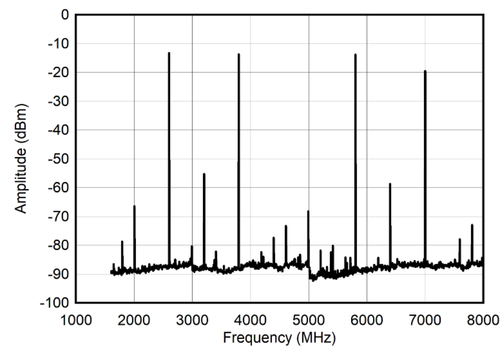
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-32. Dual Channel RTZ Mode: Dual Tone Spectrum at 1.5 GHz ± 10 MHz



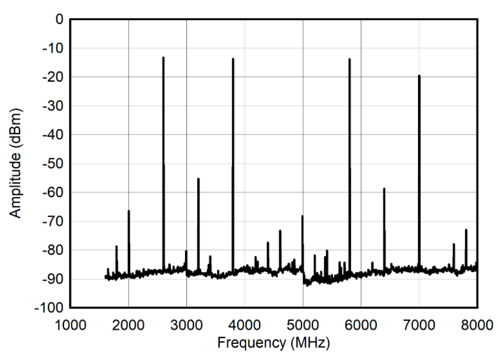
f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

図 6-33. Dual Channel 2xRF Mode: Single Tone Spectrum at 3.3 to 6.3 GHz



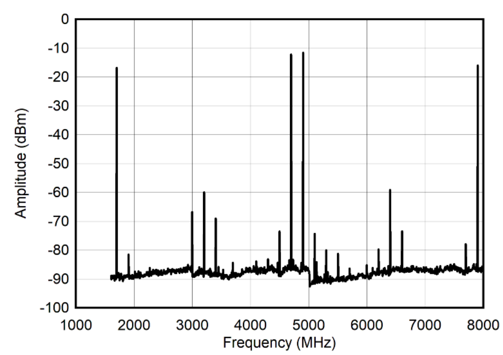
f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

図 6-34. Dual Channel 2xRF Mode: Single Tone Spectrum at 3.8 to 5.8 GHz



f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

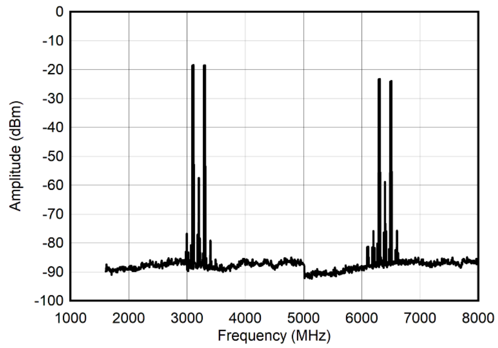
図 6-35. Dual Channel 2xRF Mode: Single Tone Spectrum at 4.3 to 5.3 GHz



f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

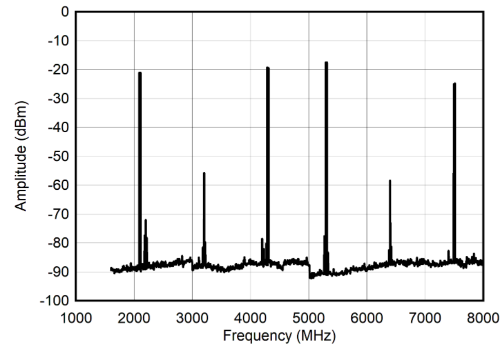
図 6-36. Dual Channel 2xRF Mode: Single Tone Spectrum at 4.7 to 4.9 GHz

6.10 Typical Characteristics (continued)



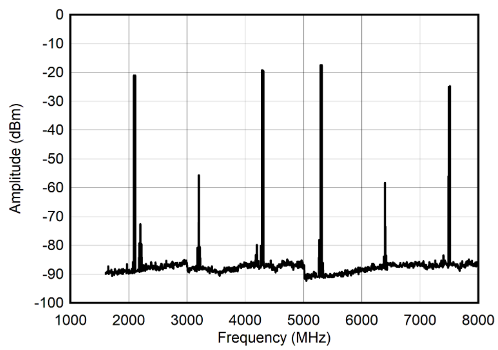
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

図 6-37. Dual Channel 2xRF Mode: Dual Tone Spectrum at 3.3 to 6.3 GHz ± 10 MHz



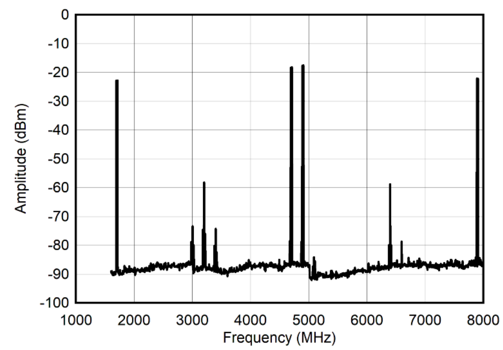
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

図 6-38. Dual Channel 2xRF Mode: Dual Tone Spectrum at 3.8 to 5.8 GHz ± 10 MHz



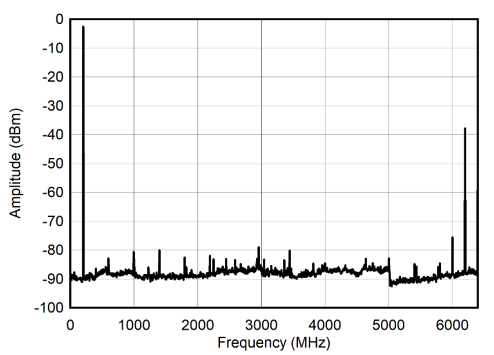
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

図 6-39. Dual Channel 2xRF Mode: Dual Tone Spectrum at 4.3 to 5.3 GHz ± 10 MHz



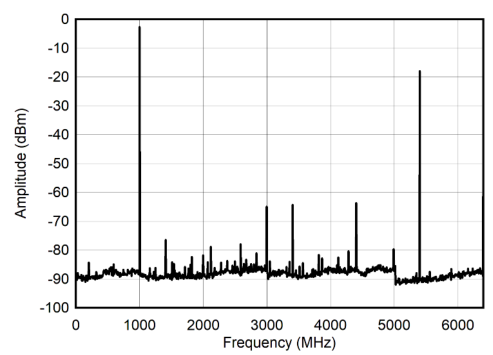
each tone at -6 dBFS, f_{CLK} = 3.2 GHz, 1st through 5th Nyquist Zones Displayed

図 6-40. Dual Channel 2xRF Mode: Dual Tone Spectrum at 4.7 to 4.9 GHz ± 10 MHz



f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

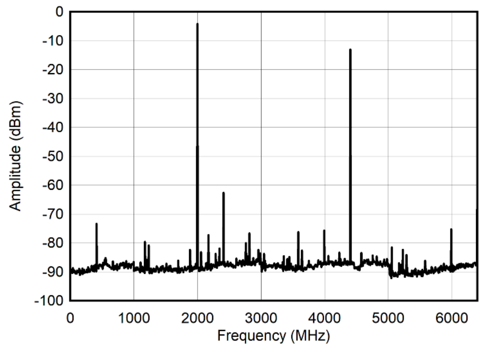
図 6-41. Single Channel NRZ Mode: Single Tone Spectrum at 200 MHz



f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

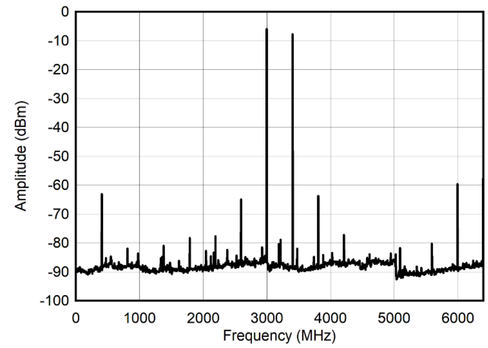
図 6-42. Single Channel NRZ Mode: Single Tone Spectrum at 1 GHz

6.10 Typical Characteristics (continued)



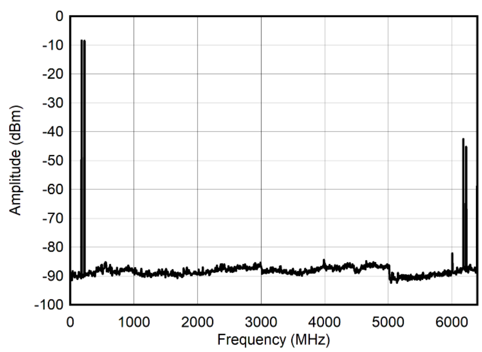
f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-43. Single Channel NRZ Mode: Single Tone Spectrum at 2 GHz



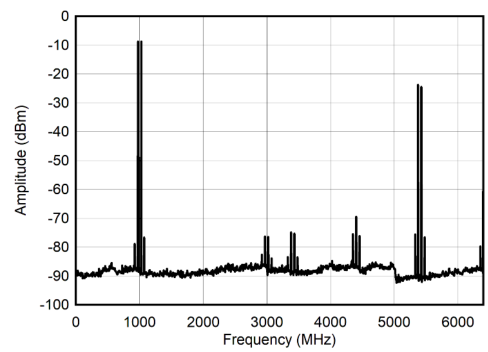
f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-44. Single Channel NRZ Mode: Single Tone Spectrum at 3 GHz



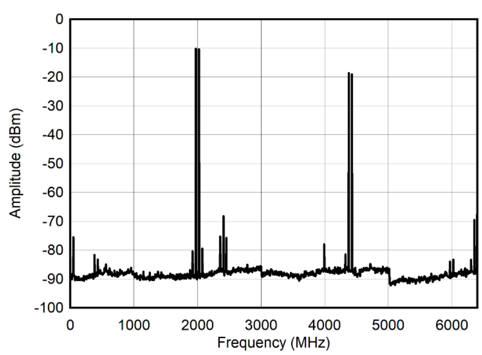
each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-45. Single Channel NRZ Mode: Dual Tone Spectrum at 200 MHz ± 25 MHz



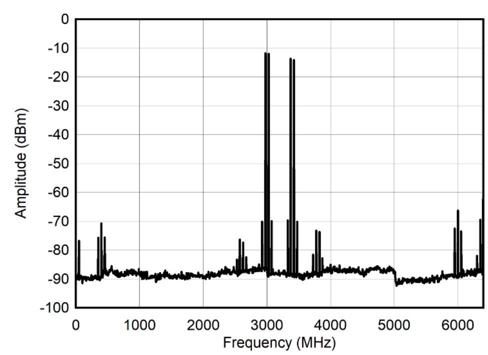
each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-46. Single Channel NRZ Mode: Dual Tone Spectrum at 1 GHz ± 25 MHz



each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

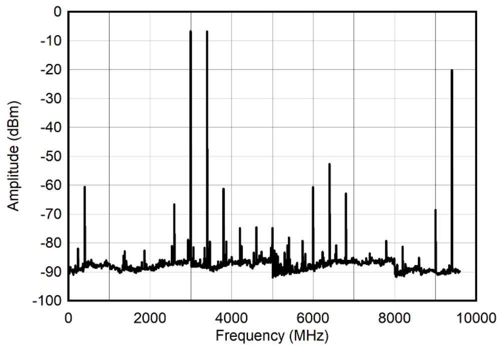
図 6-47. Single Channel NRZ Mode: Dual Tone Spectrum at 2 GHz ± 25 MHz



each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

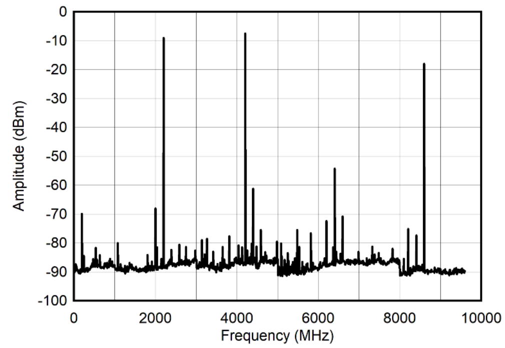
図 6-48. Single Channel NRZ Mode: Dual Tone Spectrum at 3 GHz ± 25 MHz

6.10 Typical Characteristics (continued)



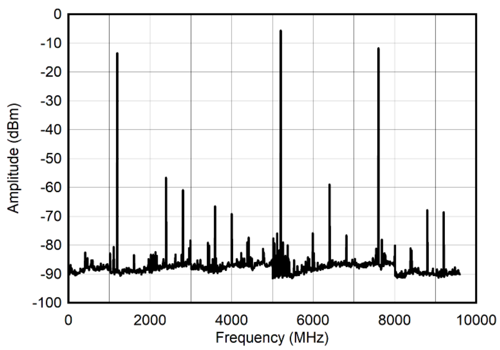
f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

図 6-49. Single Channel RF Mode: Single Tone Spectrum at 3.4 GHz



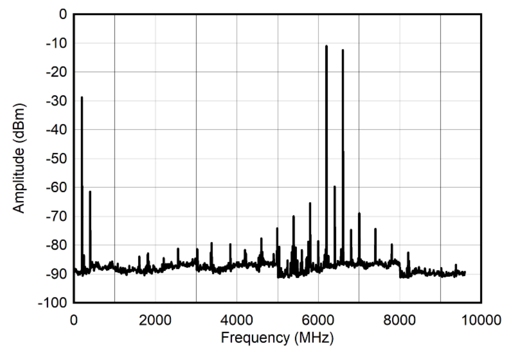
f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

図 6-50. Single Channel RF Mode: Single Tone Spectrum at 4.2 GHz



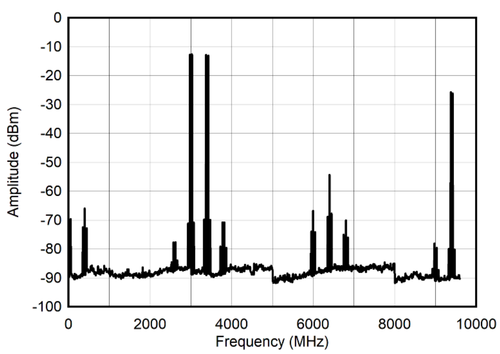
f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

図 6-51. Single Channel RF Mode: Single Tone Spectrum at 5.2 GHz



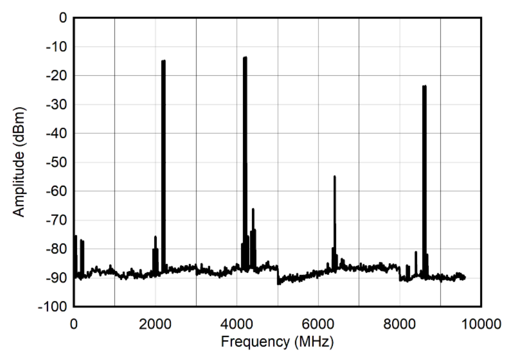
f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

図 6-52. Single Channel RF Mode: Single Tone Spectrum at 6.2 GHz



each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

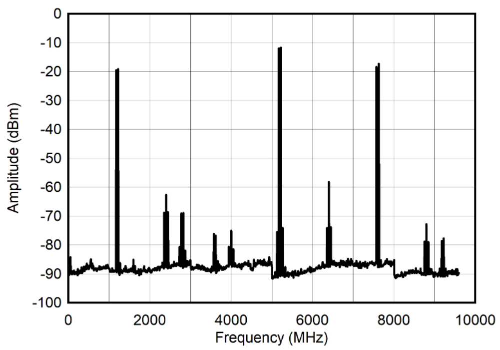
図 6-53. Single Channel RF Mode: Dual Tone Spectrum at 3.4 GHz ± 25 MHz



each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

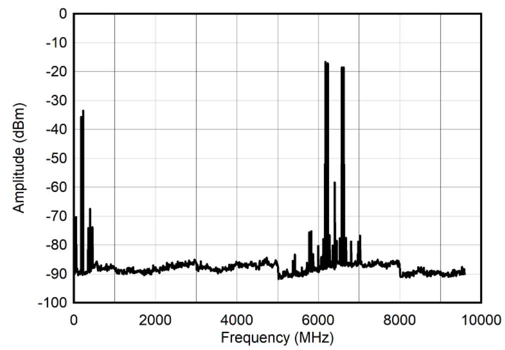
図 6-54. Single Channel RF Mode: Dual Tone Spectrum at 4.2 GHz ± 25 MHz

6.10 Typical Characteristics (continued)



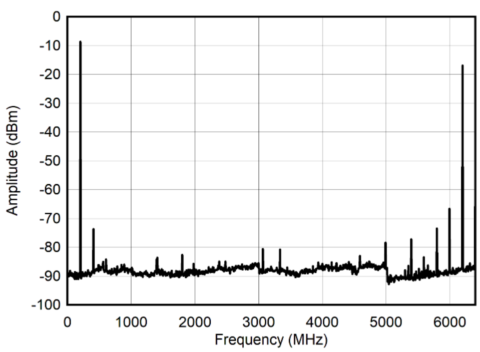
each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

図 6-55. Single Channel RF Mode: Dual Tone Spectrum at 5.2 GHz ± 25 MHz



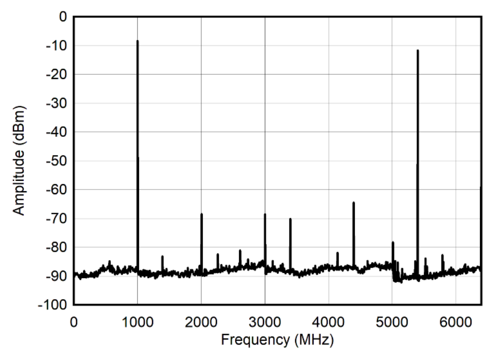
each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st through 3rd Nyquist Zones Displayed

図 6-56. Single Channel RF Mode: Dual Tone Spectrum at 6.2 GHz ± 25 MHz



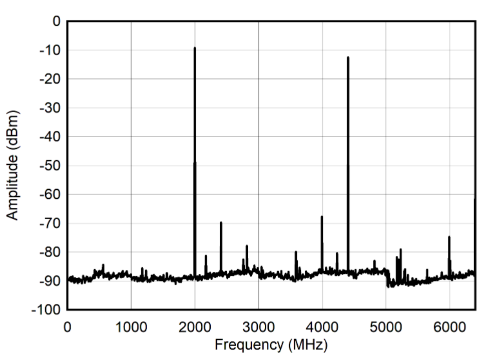
f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-57. Single Channel RTZ Mode: Single Tone Spectrum at 200 MHz



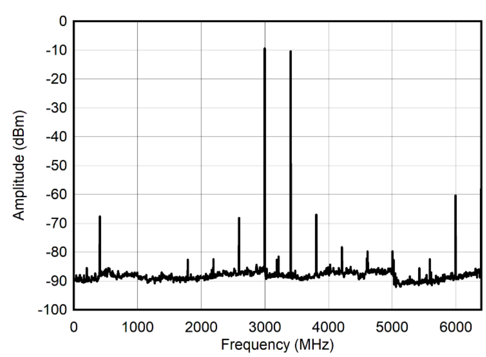
f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-58. Single Channel RTZ Mode: Single Tone Spectrum at 1 GHz



f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

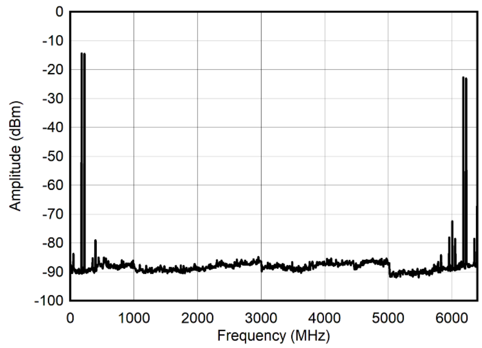
図 6-59. Single Channel RTZ Mode: Single Tone Spectrum at 2 GHz



f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

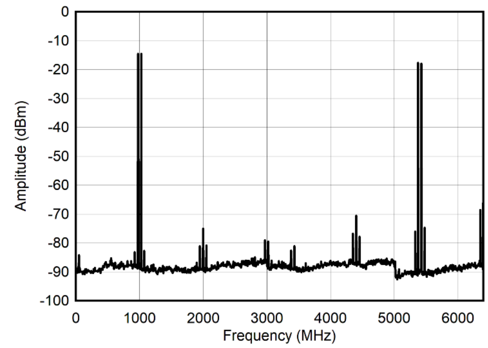
図 6-60. Single Channel RTZ Mode: Single Tone Spectrum at 3 GHz

6.10 Typical Characteristics (continued)



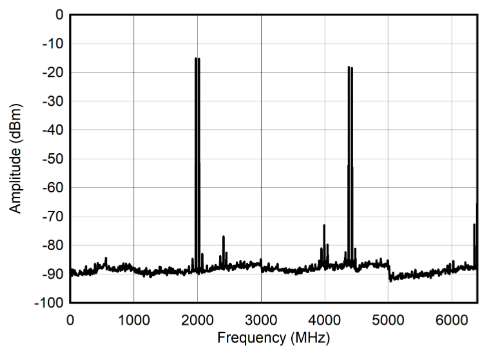
each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-61. Single Channel RTZ Mode: Dual Tone Spectrum at 200 MHz ± 25 MHz



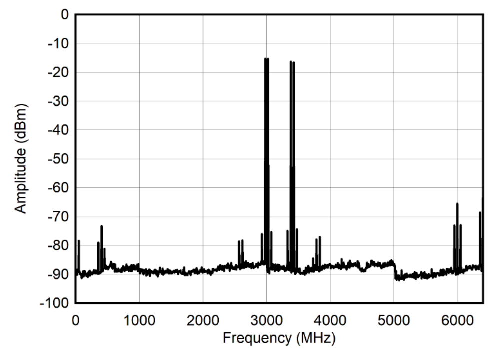
each tone at -6d BFS, f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-62. Single Channel RTZ Mode: Dual Tone Spectrum at 1 GHz ± 25 MHz



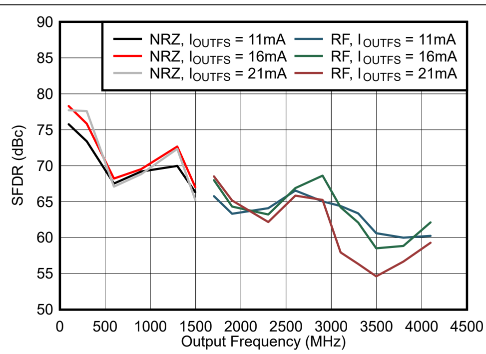
each tone at -6 dBFS, f_{CLK} = 6.4 GHz, 1st and 2nd Nyquist Zones Displayed

図 6-63. Single Channel RTZ Mode: Dual Tone Spectrum at 2 GHz ± 25 MHz



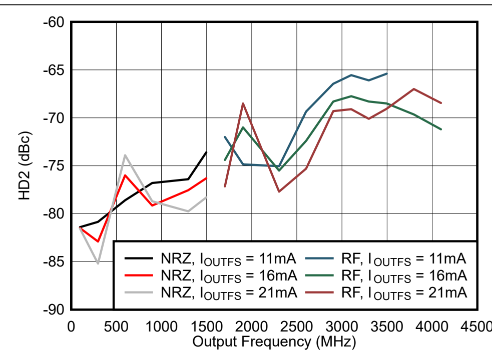
each tone at -6d BFS, f_{CLK} = 6.4GHz, 1st and 2nd Nyquist Zones Displayed

図 6-64. Single Channel RTZ Mode: Dual Tone Spectrum at 3 GHz ± 25 MHz



f_{CLK} = 3.2 GHz

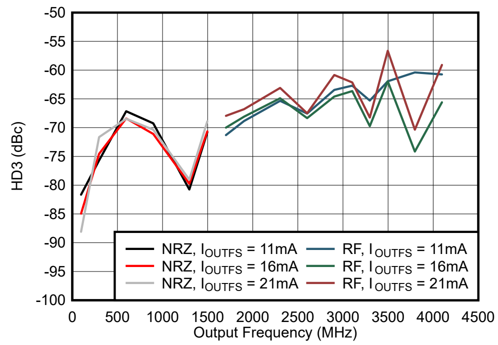
図 6-65. Dual Channel NRZ and RF Mode: SFDR vs Output Frequency and Output Current



f_{CLK} = 3.2 GHz

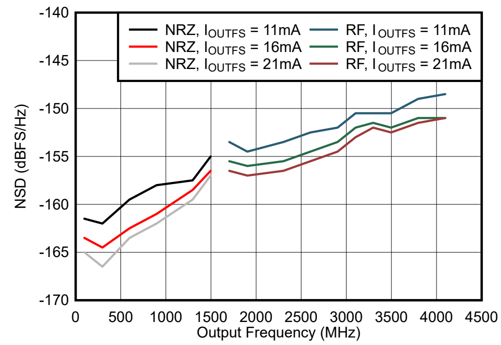
図 6-66. Dual Channel NRZ and RF Mode: HD2 vs Output Frequency and Output Current

6.10 Typical Characteristics (continued)



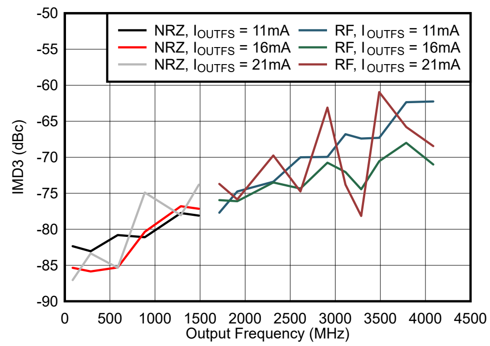
f_{CLK} = 3.2 GHz

図 6-67. Dual Channel NRZ and RF Mode: HD3 vs Output Frequency and Output Current



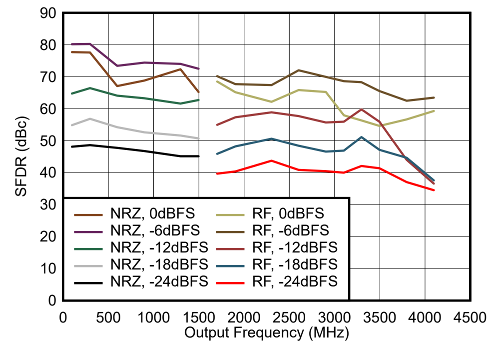
f_{CLK} = 3.2 GHz

図 6-68. Dual Channel NRZ and RF Mode: NSD vs Output Frequency and Output Current



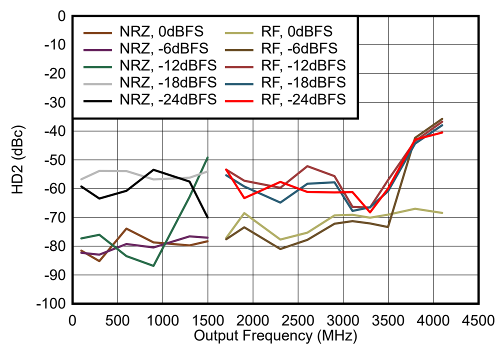
f_{CLK} = 3.2 GHz, tone spacing = 20 MHz

図 6-69. Dual Channel NRZ and RF Mode: IMD3 vs Output Frequency and Output Current



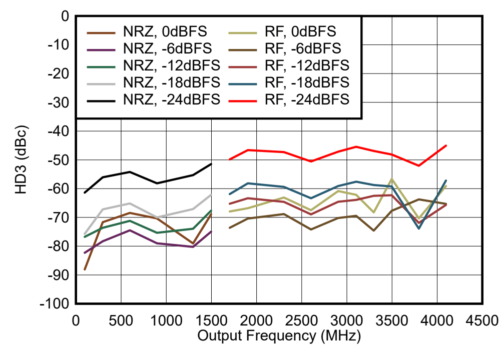
f_{CLK} = 3.2 GHz

図 6-70. Dual Channel NRZ and RF Mode: SFDR vs Output Frequency and Digital Level



f_{CLK} = 3.2 GHz

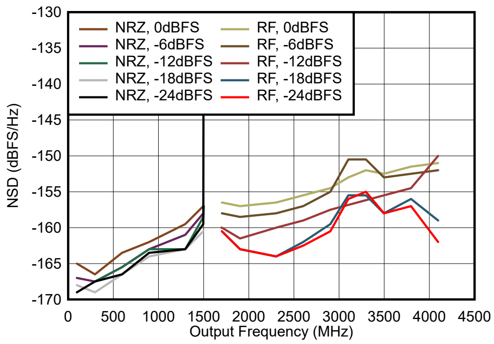
図 6-71. Dual Channel NRZ and RF Mode: HD2 vs Output Frequency and Digital Level



f_{CLK} = 3.2 GHz

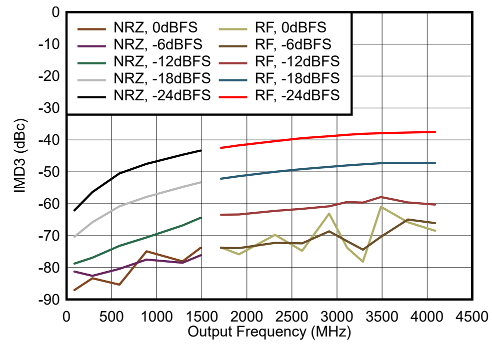
図 6-72. Dual Channel NRZ and RF Mode: HD3 vs Output Frequency and Digital Level

6.10 Typical Characteristics (continued)



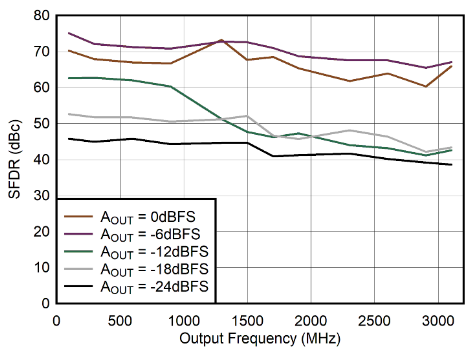
f_{CLK} = 3.2 GHz

図 6-73. Dual Channel NRZ and RF Mode: NSD vs Output Frequency and Digital Level



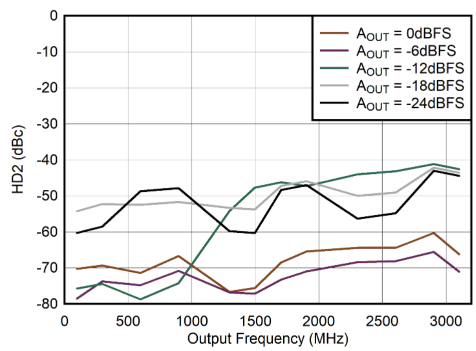
f_{CLK} = 3.2 GHz, tone spacing = 20 MHz

図 6-74. Dual Channel NRZ and RF Modes: IMD3 vs Output Frequency and Digital Level



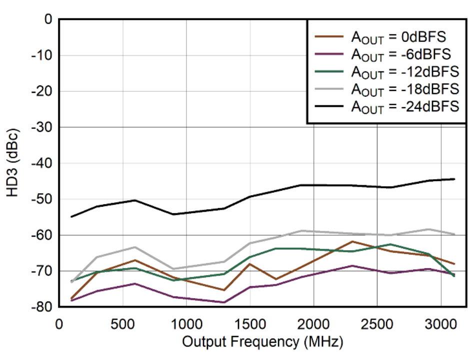
f_{CLK} = 3.2 GHz

図 6-75. Dual Channel RTZ Mode: SFDR vs Output Frequency and Digital Level



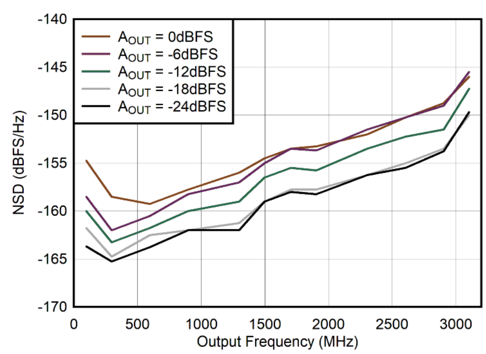
f_{CLK} = 3.2 GHz

図 6-76. Dual Channel RTZ Mode: HD2 vs Output Frequency and Digital Level



f_{CLK} = 3.2 GHz

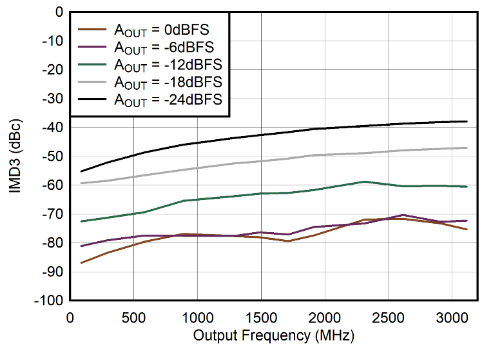
図 6-77. Dual Channel RTZ Mode: HD3 vs Output Frequency and Digital Level



f_{CLK} = 3.2 GHz, 70 MHz offset

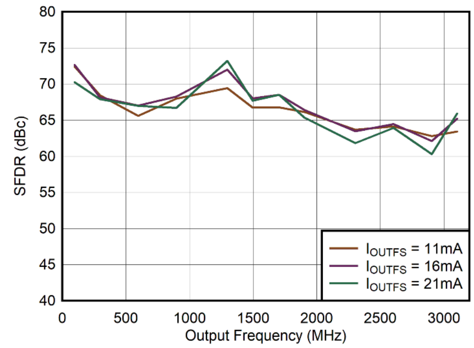
図 6-78. Dual Channel RTZ Mode: NSD vs Output Frequency and Digital Level

6.10 Typical Characteristics (continued)



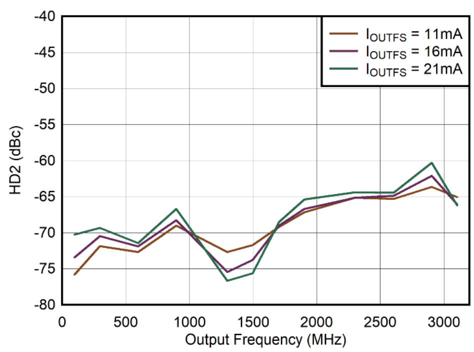
f_{CLK} = 3.2 GHz, tone spacing = 20 MHz

図 6-79. Dual Channel RTZ Mode: IMD3 vs Output Frequency and Digital Level



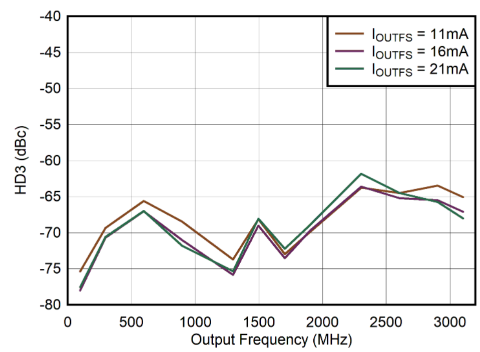
f_{CLK} = 3.2 GHz

図 6-80. Dual Channel RTZ Mode: SFDR vs Output Frequency and Output Current



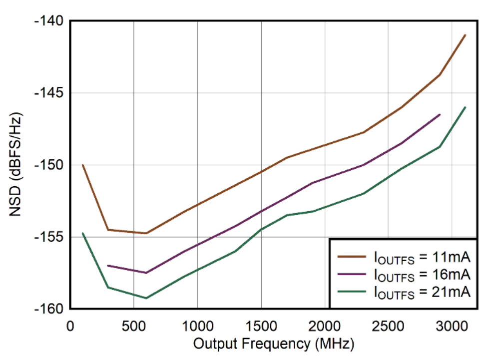
f_{CLK} = 3.2 GHz

図 6-81. Dual Channel RTZ Mode: HD2 vs Output Frequency and Output Current



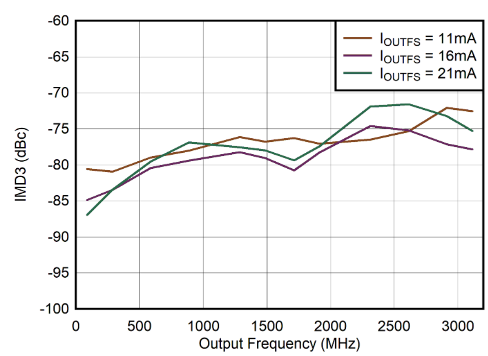
f_{CLK} = 3.2 GHz

図 6-82. Dual Channel RTZ Mode: HD3 vs Output Frequency and Output Current



f_{CLK} = 3.2 GHz, 70 MHz offset

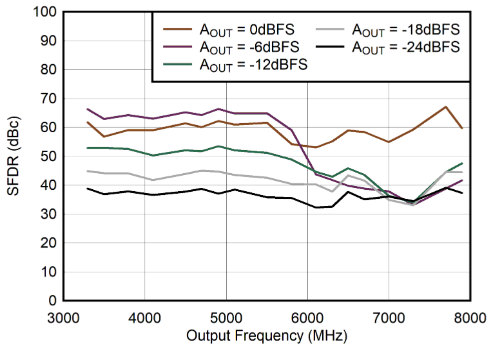
図 6-83. Dual Channel RTZ Mode: NSD vs Output Frequency and Output Current



f_{CLK} = 3.2 GHz, tone spacing = 20 MHz

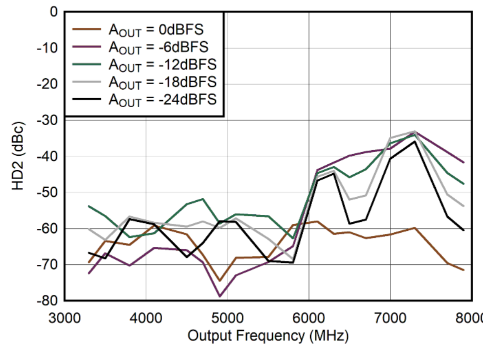
図 6-84. Dual Channel RTZ Mode: IMD3 vs Output Frequency and Output Current

6.10 Typical Characteristics (continued)



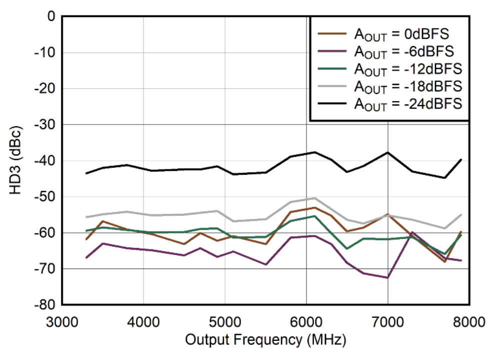
f_{CLK} = 6.4 GHz

図 6-85. Dual Channel 2xRF Mode: SFDR vs Output Frequency and Digital Level



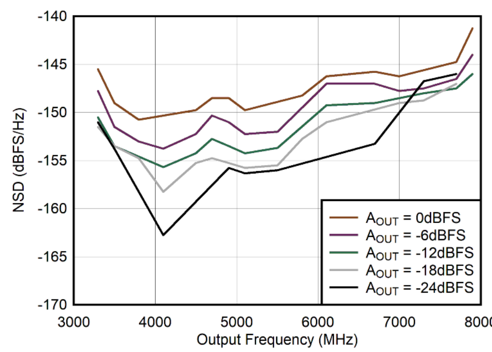
f_{CLK} = 6.4 GHz

図 6-86. Dual Channel 2xRF Mode: HD2 vs Output Frequency and Digital Level



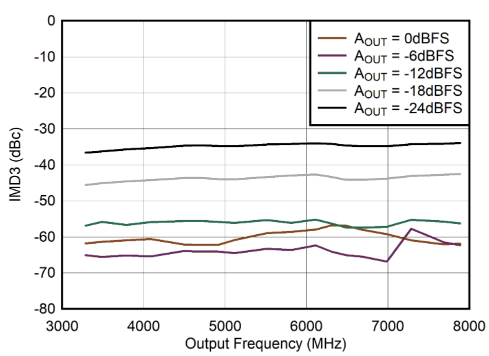
f_{CLK} = 6.4 GHz

図 6-87. Dual Channel 2xRF Mode: HD3 vs Output Frequency and Digital Level



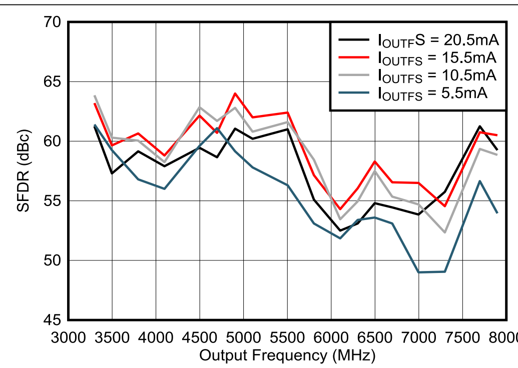
f_{CLK} = 6.4 GHz

図 6-88. Dual Channel 2xRF Mode: NSD vs Output Frequency and Digital Level



f_{CLK} = 6.4 GHz, tone spacing = 20 MHz

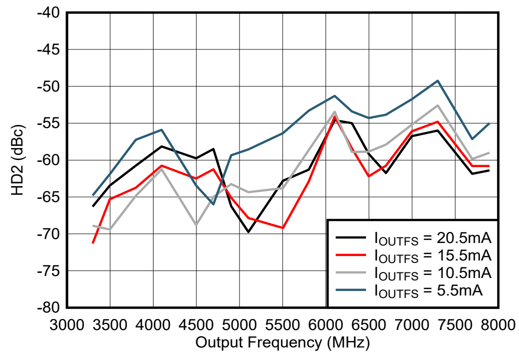
図 6-89. Dual Channel 2xRF Mode: IMD3 vs Output Frequency and Digital Level



f_{CLK} = 6.4 GHz

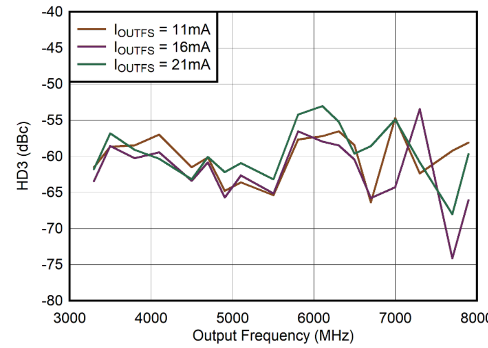
図 6-90. Dual Channel 2xRF Mode: SFDR vs Output Frequency and Output Current

6.10 Typical Characteristics (continued)



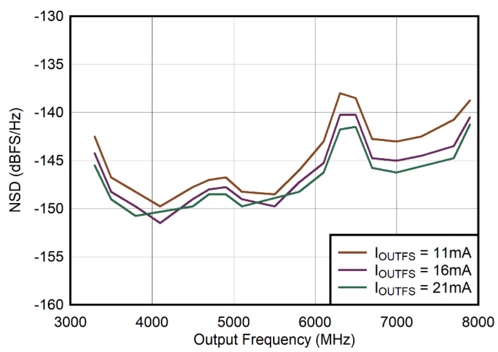
f_{CLK} = 6.4 GHz

図 6-91. Dual Channel 2xRF Mode: HD2 vs Output Frequency and Output Current



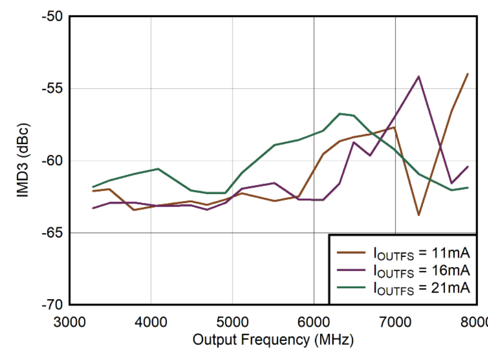
f_{CLK} = 6.4 GHz

図 6-92. Dual Channel 2xRF Mode: HD3 vs Output Frequency and Output Current



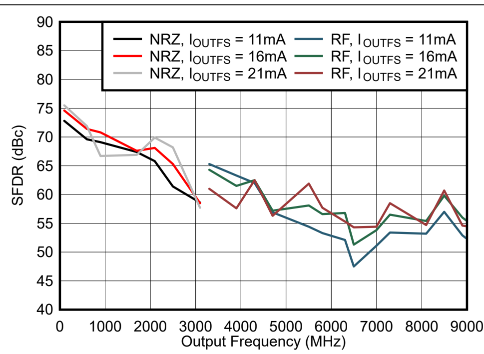
f_{CLK} = 6.4 GHz

図 6-93. Dual Channel 2xRF Mode: NSD vs Output Frequency and Output Current



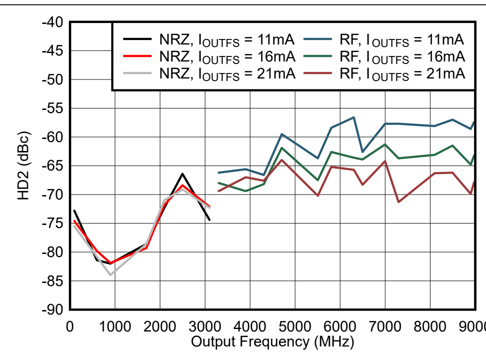
f_{CLK} = 6.4 GHz, tone spacing = 20 MHz

図 6-94. Dual Channel 2xRF Mode: IMD3 vs Output Frequency and Output Current



f_{CLK} = 6.4 GHz

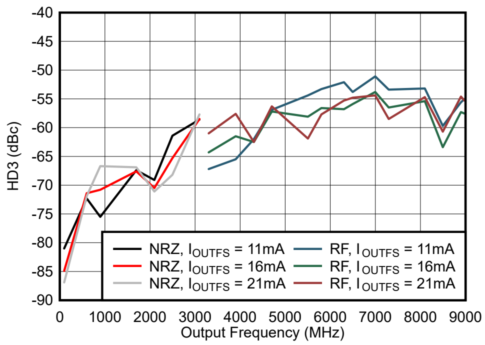
図 6-95. Single Channel NRZ and RF Modes: SFDR vs Output Frequency and Output Current



f_{CLK} = 6.4 GHz

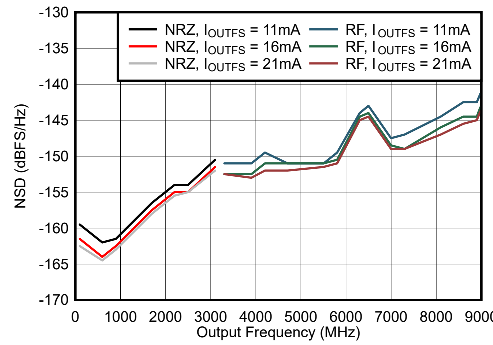
図 6-96. Single Channel NRZ and RF Modes: HD2 vs Output Frequency and Output Current

6.10 Typical Characteristics (continued)



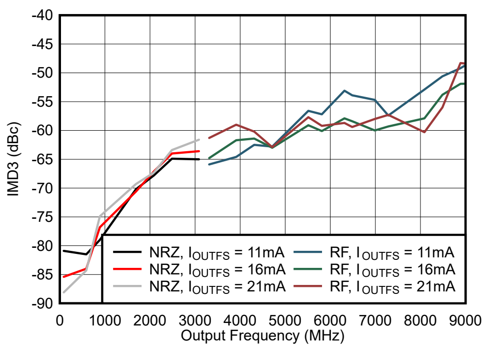
f_{CLK} = 6.4 GHz

図 6-97. Single Channel NRZ and RF Modes: HD3 vs Output Frequency and Output Current



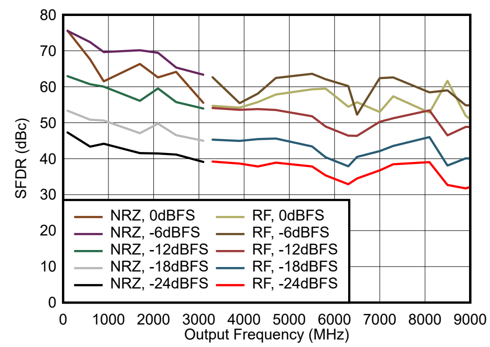
f_{CLK} = 6.4 GHz

図 6-98. Single Channel NRZ and RF Modes: NSD vs Output Frequency and Output Current



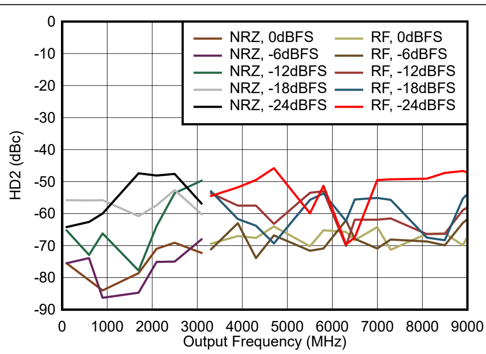
f_{CLK} = 6.4 GHz, tone spacing = 20 MHz

図 6-99. Single Channel NRZ and RF Modes: IMD3 vs Output Frequency and Output Current



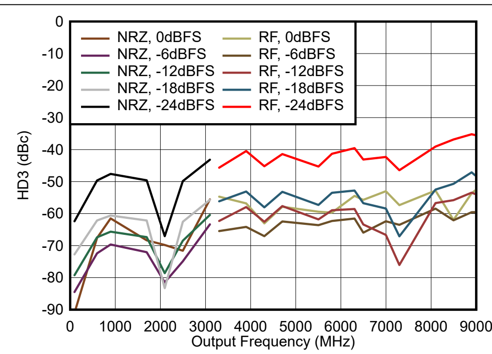
f_{CLK} = 6.4 GHz

図 6-100. Single Channel NRZ and RF Modes: SFDR vs Output Frequency and Digital Level



f_{CLK} = 6.4 GHz

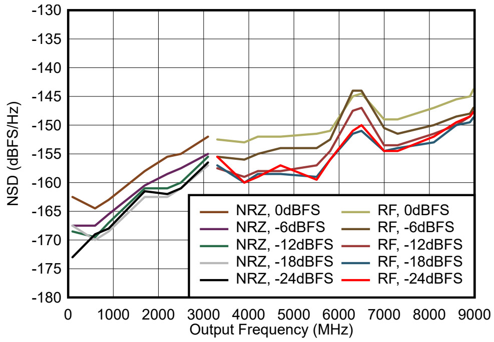
図 6-101. Single Channel NRZ and RF Modes: HD2 vs Output Frequency and Digital Level



f_{CLK} = 6.4 GHz

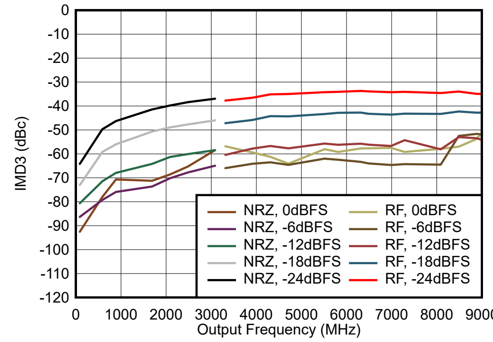
図 6-102. Single Channel NRZ and RF Modes: HD3 vs Output Frequency and Digital Level

6.10 Typical Characteristics (continued)



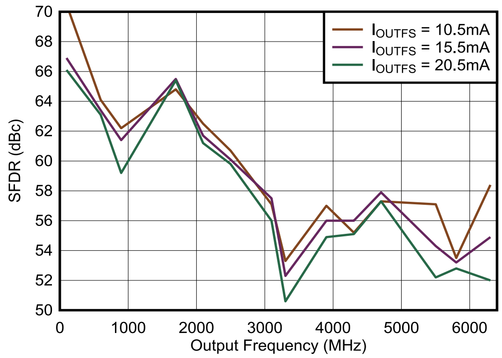
f_{CLK} = 6.4 GHz

図 6-103. Single Channel NRZ and RF Modes: Noise Spectral Density vs Output Frequency and Digital Level



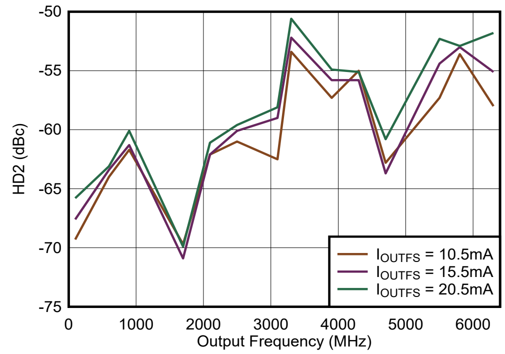
f_{CLK} = 6.4 GHz, tone spacing = 20 MHz

図 6-104. Single Channel NRZ and RF Modes: IMD3 vs Output Frequency and Digital Level



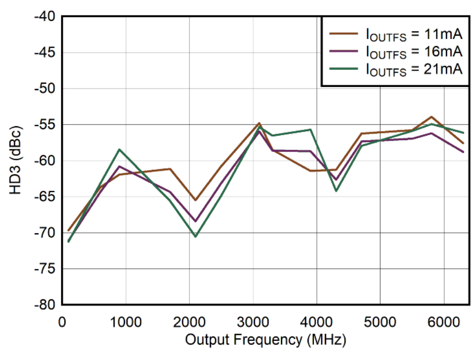
f_{CLK} = 6.4 GHz

図 6-105. Single Channel RTZ Mode: SFDR vs Output Frequency and Output Current



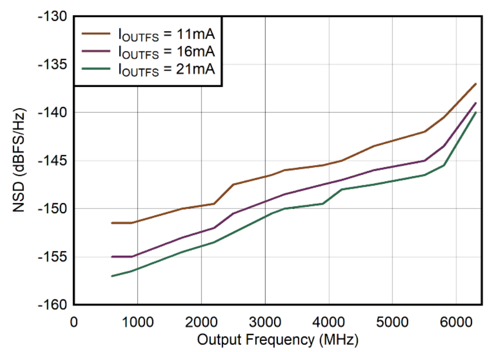
f_{CLK} = 6.4 GHz

図 6-106. Single Channel RTZ Mode: HD2 vs Output Frequency and Output Current



f_{CLK} = 6.4 GHz

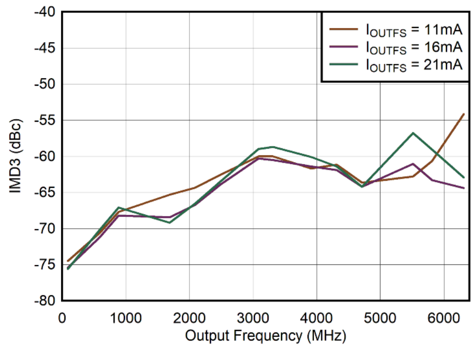
図 6-107. Single Channel RTZ Mode: HD3 vs Output Frequency and Output Current



f_{CLK} = 6.4 GHz, 70 MHz offset

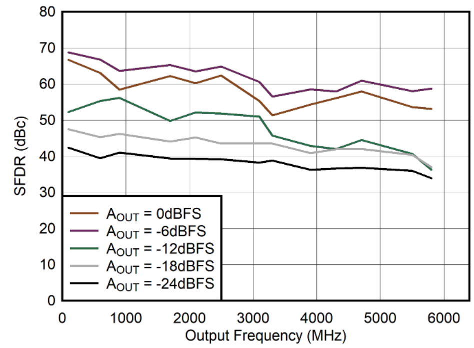
図 6-108. Single Channel RTZ Mode: NSD vs Output Frequency and Output Current

6.10 Typical Characteristics (continued)



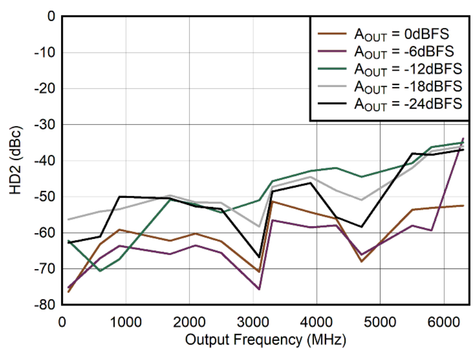
f_{CLK} = 6.4 GHz, tone spacing = 20 MHz

図 6-109. Single Channel RTZ Mode: IMD3 vs Output Frequency and Output Current



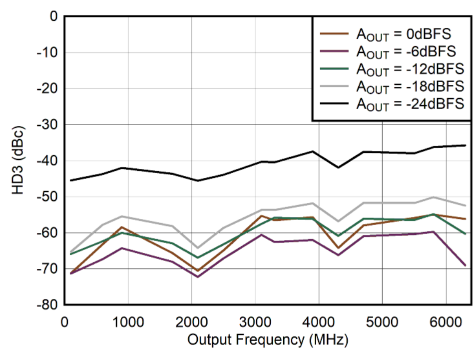
f_{CLK} = 6.4 GHz

図 6-110. Single Channel RTZ Mode: SFDR vs Output Frequency and Digital Level



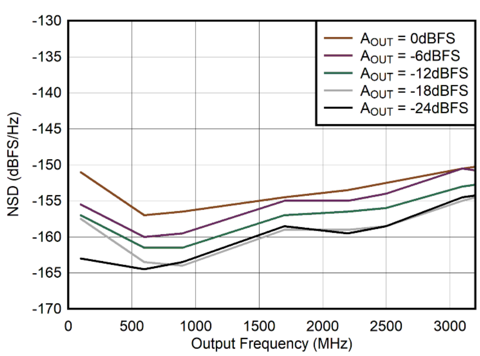
f_{CLK} = 6.4 GHz

図 6-111. Single Channel RTZ Mode: HD2 vs Output Frequency and Digital Level



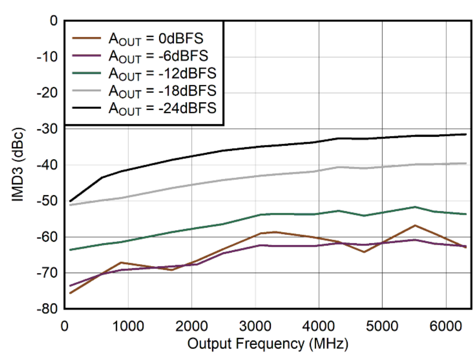
f_{CLK} = 6.4 GHz

図 6-112. Single Channel RTZ Mode: HD3 vs Output Frequency and Digital Level



f_{CLK} = 6.4 GHz, 70 MHz offset

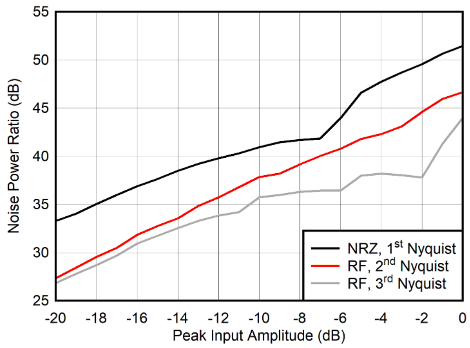
図 6-113. Single Channel RTZ Mode: NSD vs Output Frequency and Digital Level



f_{CLK} = 6.4 GHz, tone spacing = 20 MHz

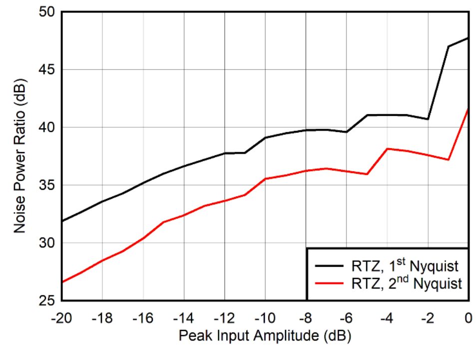
図 6-114. Single Channel RTZ Mode: IMD3 vs Output Frequency and Digital Level

6.10 Typical Characteristics (continued)



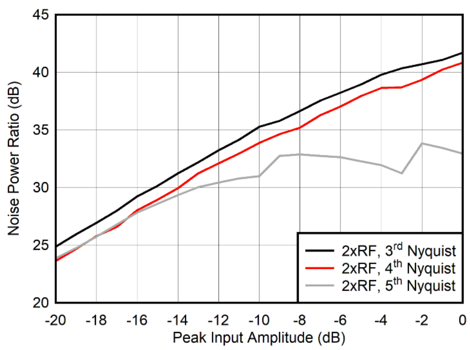
Signal 90% Nyquist BW, 5% notch in center, PAR = 11.4 dB, f_{CLK} = 3.2 GHz

図 6-115. Dual Channel NRZ and RF Modes: NPR vs Digital Level



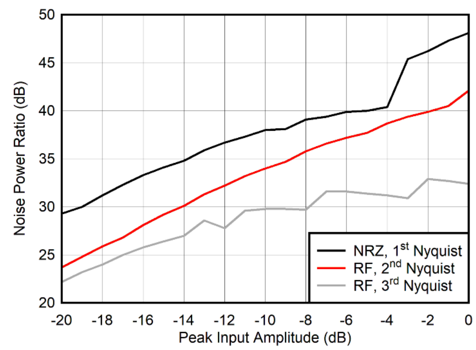
Signal 90% Nyquist BW, 5% notch in center, PAR = 11.4 dB, f_{CLK} = 3.2 GHz

図 6-116. Dual Channel RTZ Mode: NPR vs Digital Level



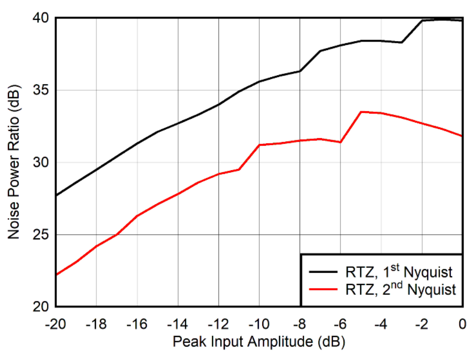
Signal 90% Nyquist BW, 5% notch in center, PAR = 11.4 dB, f_{CLK} = 6.4 GHz

図 6-117. Dual Channel 2xRF Mode: NPR vs Digital Level



Signal 90% Nyquist BW, 5% notch in center, PAR = 11.4 dB, f_{CLK} = 6.4 GHz

図 6-118. Single Channel NRZ and RF Modes: NPR vs Digital Level



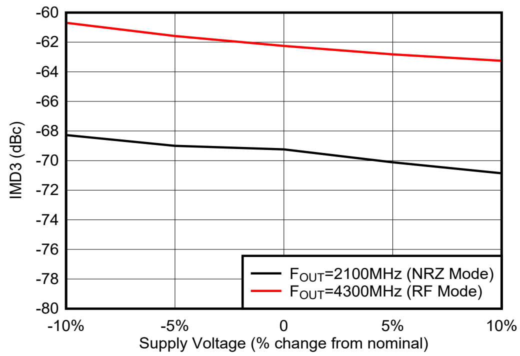
Signal 90% Nyquist BW, 5% notch in center, PAR = 11.4 dB, f_{CLK} = 6.4 GHz

図 6-119. Single Channel RTZ Mode: NPR vs Digital Level

F_{OUT} = 995 MHz, input clock phase noise removed

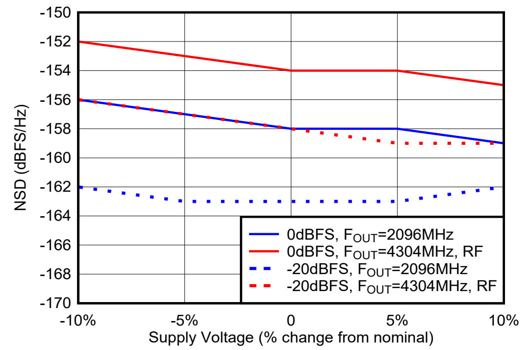
図 6-120. Single Channel NRZ Mode: Additive Phase Noise

6.10 Typical Characteristics (continued)



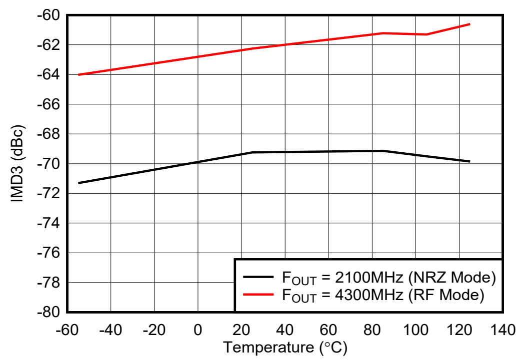
50 MHz tone spacing, -6dBFS/tone, all supplies changed together

図 6-121. Single Channel Mode: IMD3 vs Supply Voltage



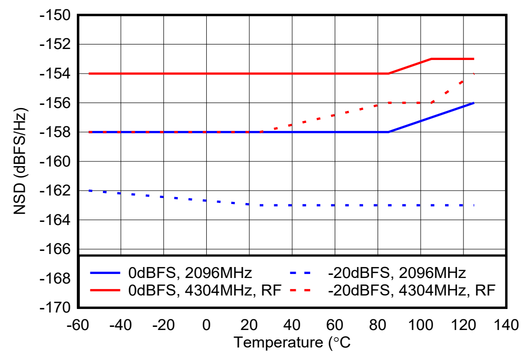
70 MHz offset, all supplies changed together

図 6-122. Single Channel Mode: NSD vs Supply Voltage



50 MHz tone spacing, -6dBFS/tone

図 6-123. Single Channel Mode: IMD3 vs Temperature



70 MHz offset

図 6-124. Single Channel Mode: NSD vs Temperature

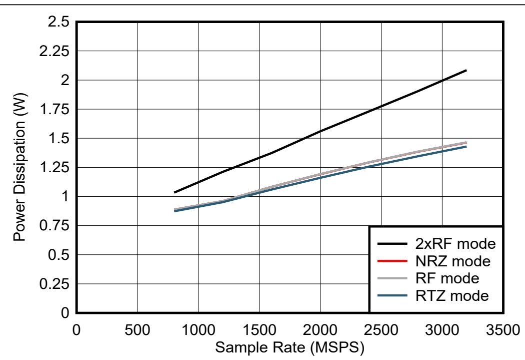


図 6-125. Dual Channel Mode: Power Dissipation vs Sample Rate

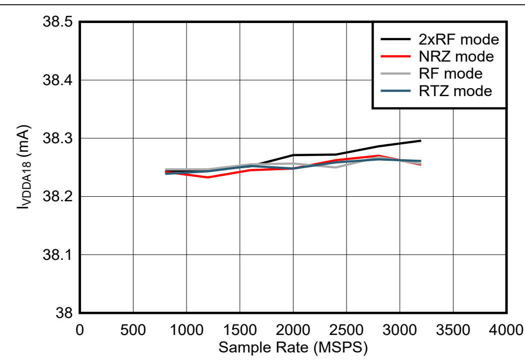


図 6-126. Dual Channel Mode: I_{VDDA18} vs Sample Rate

6.10 Typical Characteristics (continued)

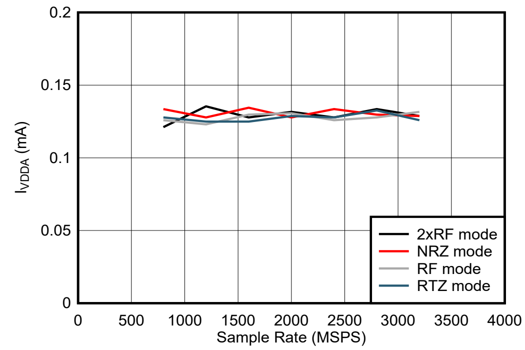


図 6-127. Dual Channel Mode: I_{VDDA} vs Sample Rate

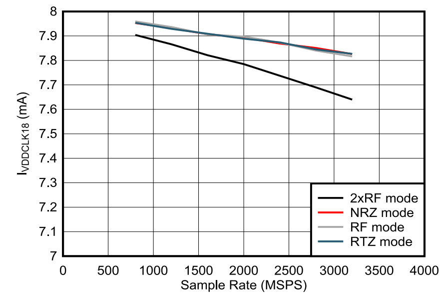


図 6-128. Dual Channel Mode: $I_{VDDCLK18}$ vs Sample Rate

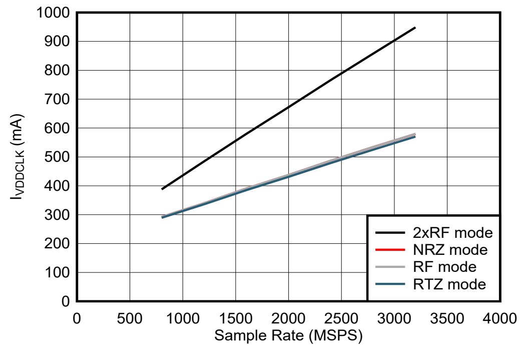


図 6-129. Dual Channel Mode: I_{VDDCLK} vs Sample Rate

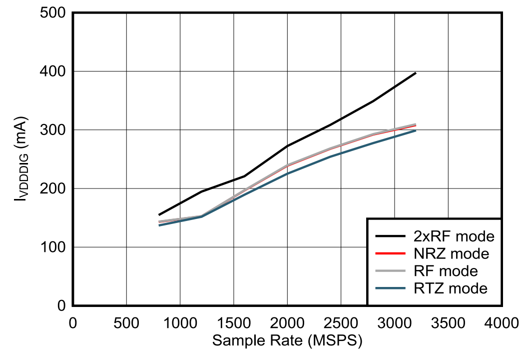


図 6-130. Dual Channel Mode: I_{VDDDIG} vs Sample Rate

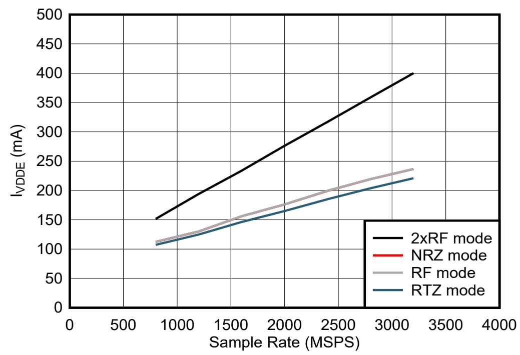


図 6-131. Dual Channel Mode: I_{VDDE} vs Sample Rate

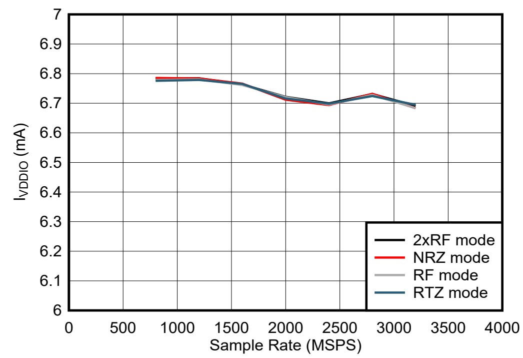


図 6-132. Dual Channel Mode: I_{VDDIO} vs Sample Rate

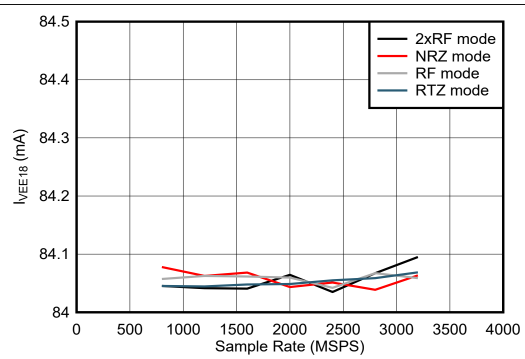


図 6-133. Dual Channel Mode: I_{VEE18} vs Sample Rate

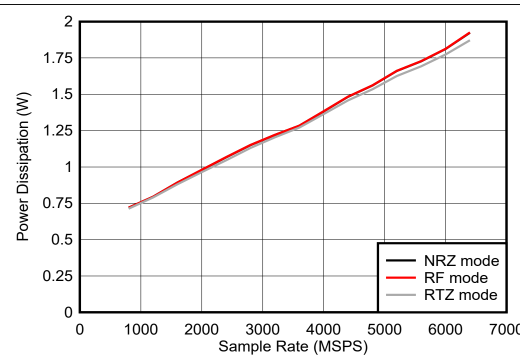


図 6-134. Single Channel Mode: Power Dissipation vs Sample Rate

6.10 Typical Characteristics (continued)

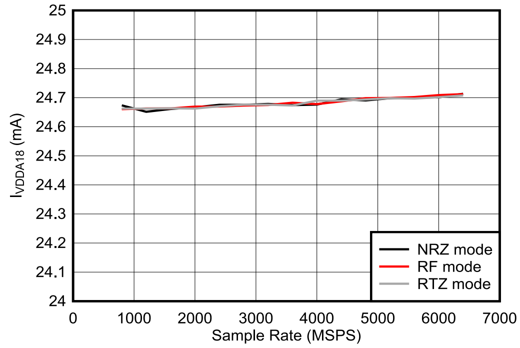


図 6-135. Single Channel Mode: I_{VDDA18} vs Sample Rate

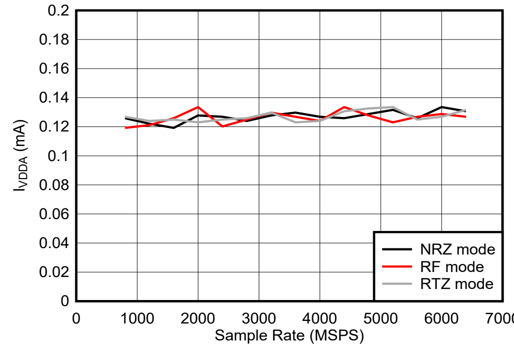


図 6-136. Single Channel Mode: I_{VDDA} vs Sample Rate

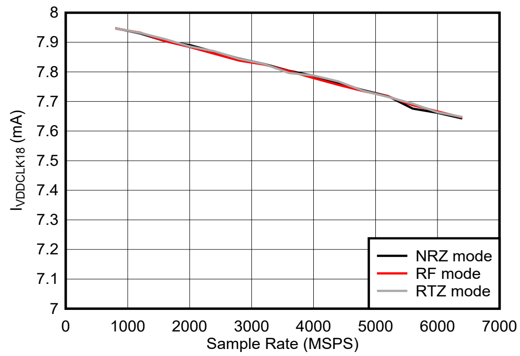


図 6-137. Single Channel Mode: $I_{VDDCLK18}$ vs Sample Rate

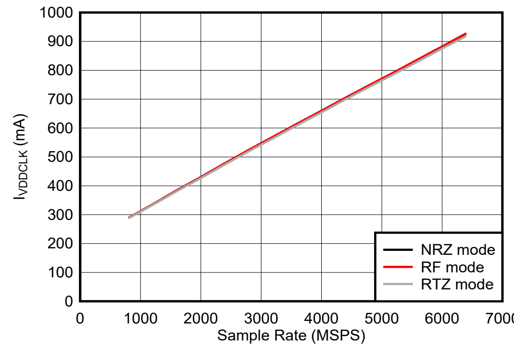


図 6-138. Single Channel Mode: I_{VDDCLK} vs Sample Rate

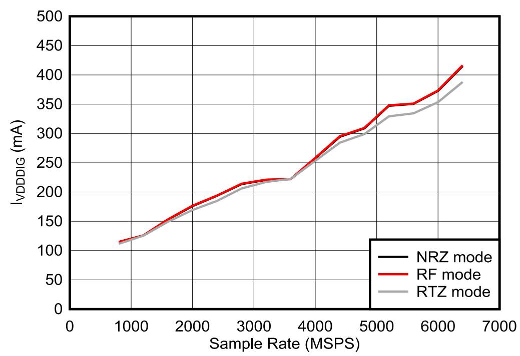


図 6-139. Single Channel Mode: I_{VDDDIG} vs Sample Rate

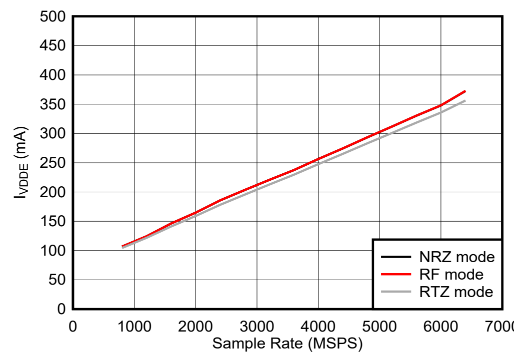


図 6-140. Single Channel Mode: I_{VDDE} vs Sample Rate

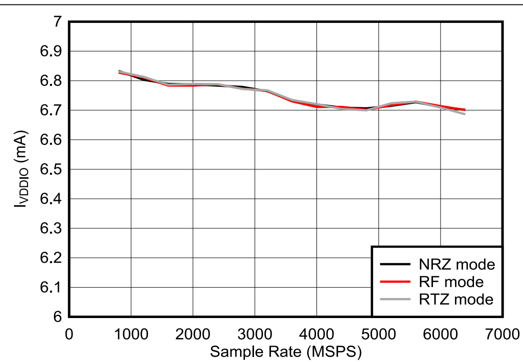


図 6-141. Single Channel Mode: I_{VDDIO} vs Sample Rate

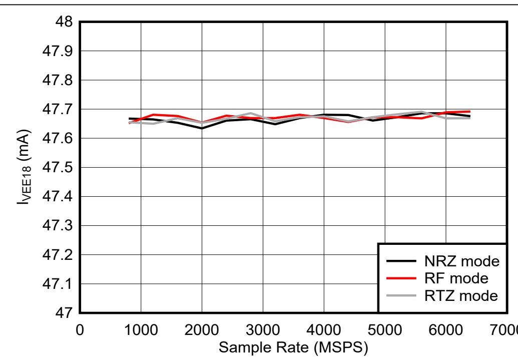


図 6-142. Single Channel Mode: I_{VEE} vs Sample Rate

7 Detailed Description

7.1 Overview

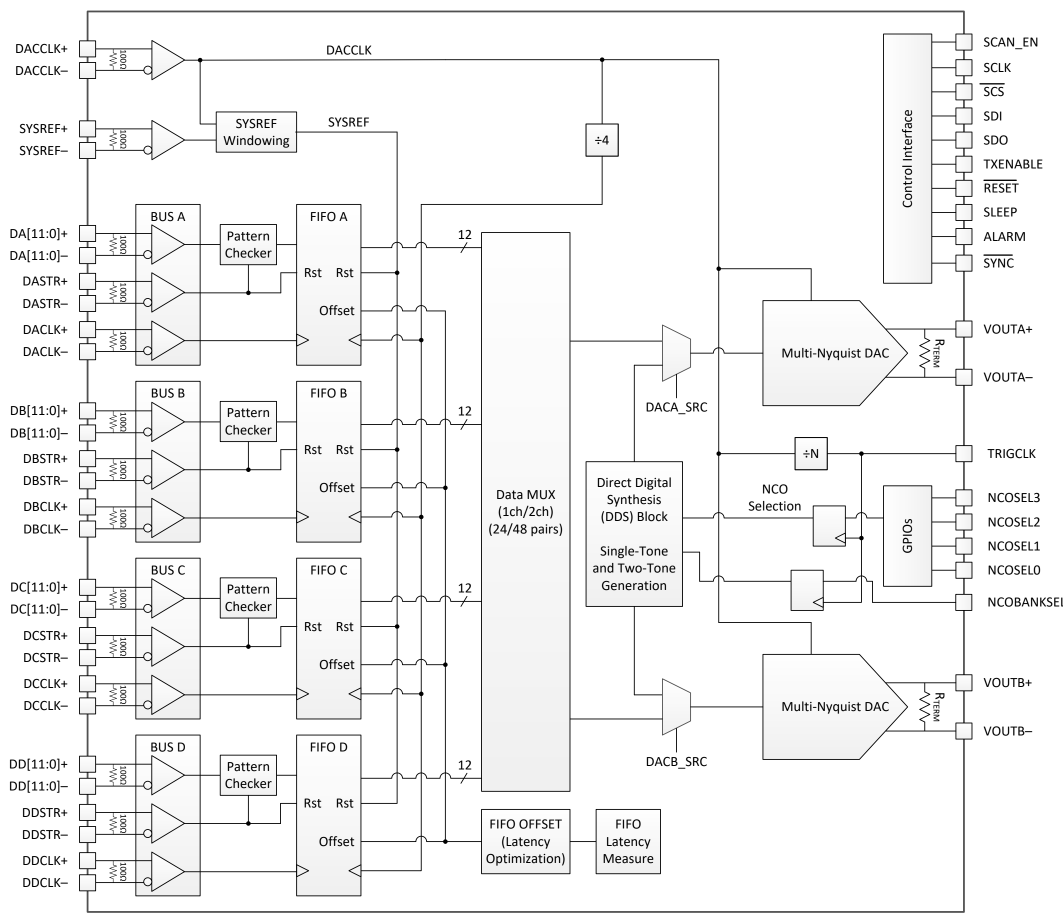
The DAC12DL3200 is a dual channel, RF sampling digital-to-analog converter (DAC) capable of input and output rates of up to 3.2-GSPS in dual channel mode or 6.4-GSPS in single channel mode. The DAC can transmit signal bandwidths beyond 2 GHz at carrier frequencies approaching 8 GHz when using the multi-Nyquist output modes. The high output frequency range enables direct sampling through C-band (8 GHz) and beyond.

The DAC12DL3200 can be used as an I/Q baseband DAC in dual channel mode. The high sampling rate and output frequency range also makes the DAC12DL3200 capable of arbitrary waveform generation (AWG) and direct digital synthesis (DDS). An integrated DDS block enables single tone and two tone generation on chip.

The DAC12DL3200 has a parallel LVDS interface that consists of up to 48 LVDS pairs and 4 DDR LVDS clocks. A strobe signal is used to synchronize the interface which can be sent over the least significant bit (LSB) or optionally over dedicated strobe LVDS lanes. Each LVDS pair is capable of up to 1.6 Gbps. The LVDS interface has a total latency of 6 to 8 ns (depending on mode of operation) from digital data input to analog output for latency sensitive applications.

Multi-device synchronization is supported using a synchronization signal (SYSREF). SYSREF windowing eases synchronization in multi-device systems. The clocking scheme is compatible with JESD204B clocking devices.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DAC Output Modes

DAC12DL3200 consists of a multi-Nyquist DAC core capable of direct transmission through the third Nyquist zone. The high output frequency capabilities are enabled by specific output waveforms that alter the output waveform response. In other words, the waveforms change the frequency response of the DAC to enhance the DAC images in alternate Nyquist zones. The output waveform can be selected in the MXMODE register. A list of output modes along with their properties and uses are provided in 表 7-1 and in the following sections. Note that T_S is the period of the sampling clock provided to the DACCLK input. The output waveform responses shown in this section do not consider the effect of the DAC analog bandwidth or external passive or active signal chain components.

表 7-1. Summary of Multi-Nyquist Output Modes and Uses

DAC MODE	USABLE OPERATING MODES	PASSES DC	OPTIMAL NYQUIST ZONE	PEAK THEORETICAL OUTPUT POWER(1)
Non-return-to-zero (NRZ)	Single DAC, Dual DAC	Yes	1	0 dBFS
Return-to-zero (RZ)	Single DAC, Dual DAC	Yes	1, 2	–6 dBFS
Radio Frequency (RF)	Single DAC, Dual DAC	No	2	–2.8 dBFS
2x Radio Frequency (2xRF)	Dual DAC with 2x DACCLK	No	3, 4, 5	–8.8 dBFS

(1) Peak power here does not include the effect of analog output bandwidth due to parasitic passive components or external components

7.3.1.1 NRZ Mode

Non-return-to-zero (NRZ) mode is the standard zero-order hold output waveform. The sample is output from the DAC and held until the next sample is output. The timing diagram for NRZ mode is given in 図 7-1. This output waveform can be thought of as a rectangular filter in time domain resulting in a sinc response in the frequency domain. The result is a frequency response that has significant power loss in the 2nd and 3rd Nyquist zones and a null at the sampling rate. It is meant for 1st Nyquist operation only. A plot of the frequency response of NRZ mode is shown in 図 7-2.

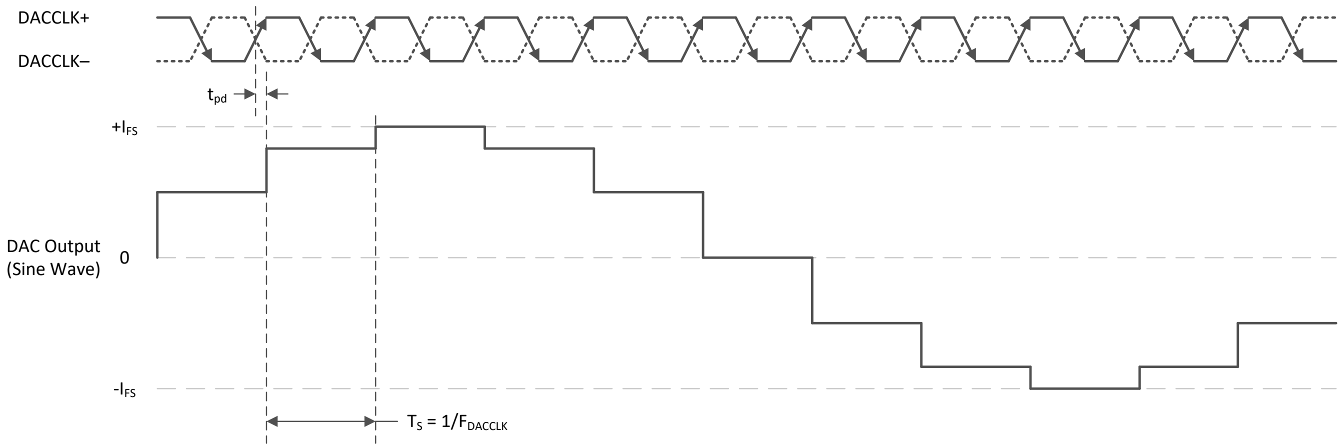


図 7-1. NRZ Mode Timing Diagram

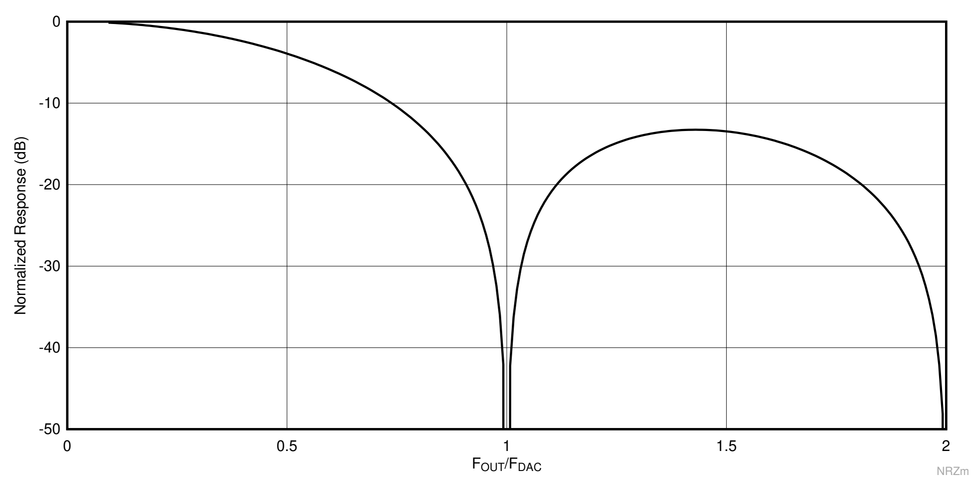


図 7-2. NRZ Mode Output Waveform Frequency Response

7.3.1.2 RTZ Mode

Return-to-zero (RTZ) mode is similar to the standard zero-order hold output waveform used by DACs, however the response adds a return-to-zero pulse for the second half of the sample period. The timing diagram for RTZ mode is given in 図 7-3. This output waveform can be thought of as a rectangular filter in time domain that is half the length of which is used in NRZ mode, resulting in a sinc response that is expanded by two times in the frequency domain. The result is a frequency response with less power loss in the 2nd Nyquist zone and a null at twice the sampling rate. It can be used for 1st and 2nd Nyquist zone applications. The return-to-zero pulse provides a flatter response through the first Nyquist zone at a tradeoff of 6-dB lower peak power. A plot of the frequency response of RTZ mode is shown in 図 7-4.

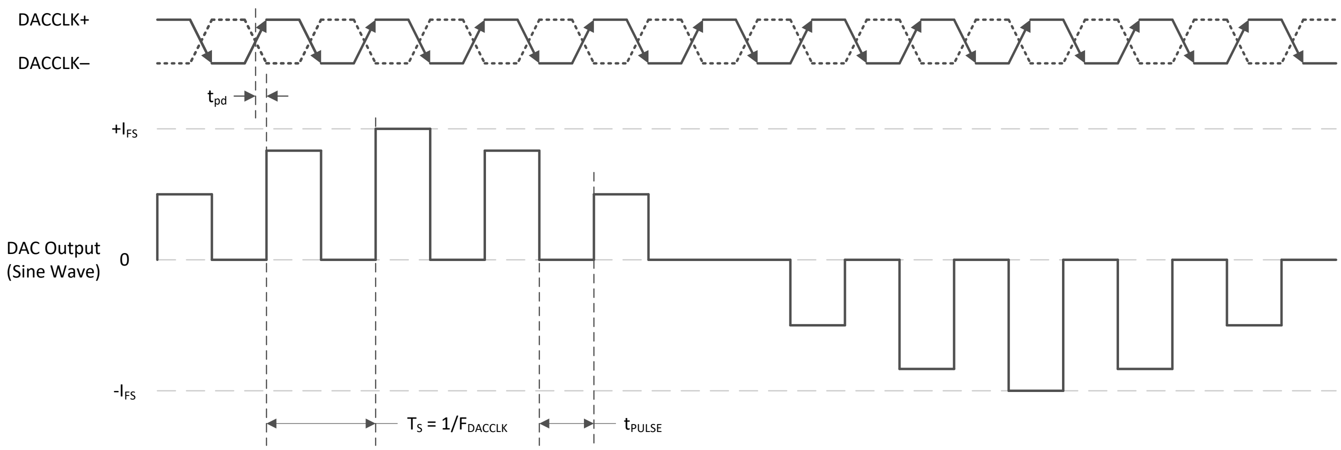


図 7-3. RTZ Mode Timing Diagram

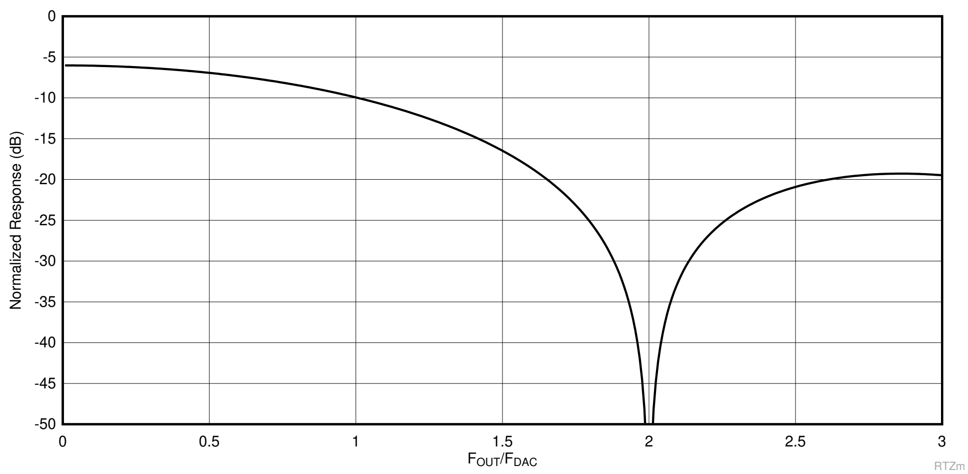


図 7-4. RTZ Mode Output Waveform Response

7.3.1.3 RF Mode

RF mode adds a mixing function to the DAC output response by inverting the sample halfway through the sample period. The result is a sinc response that peaks and provides maximum flatness in the 2nd Nyquist zone. The timing diagram for RF mode is given in 図 7-5. A plot of the frequency response of RF mode is shown in 図 7-6.

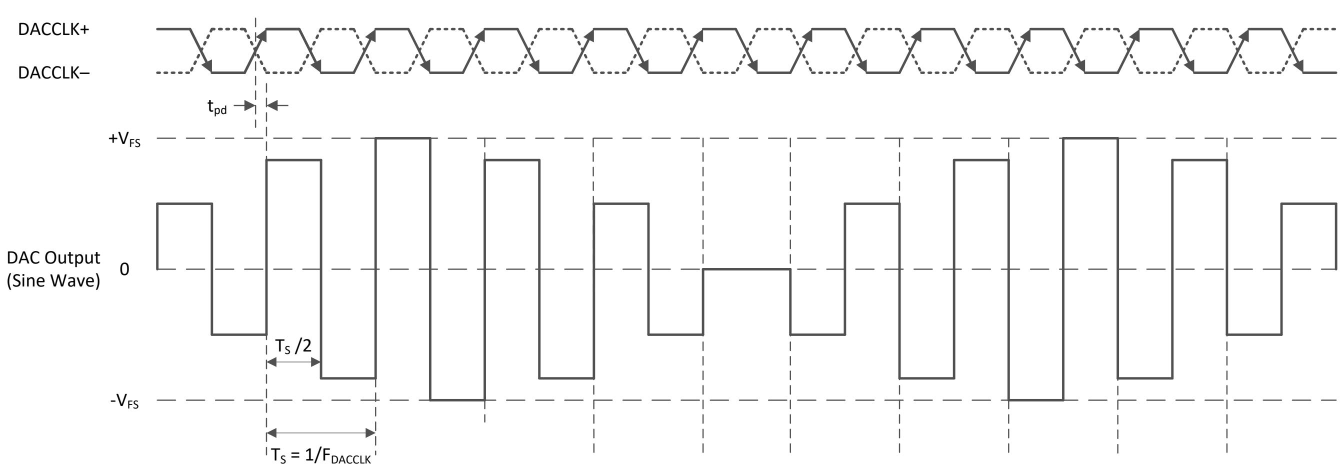


図 7-5. RF Mode Timing Diagram

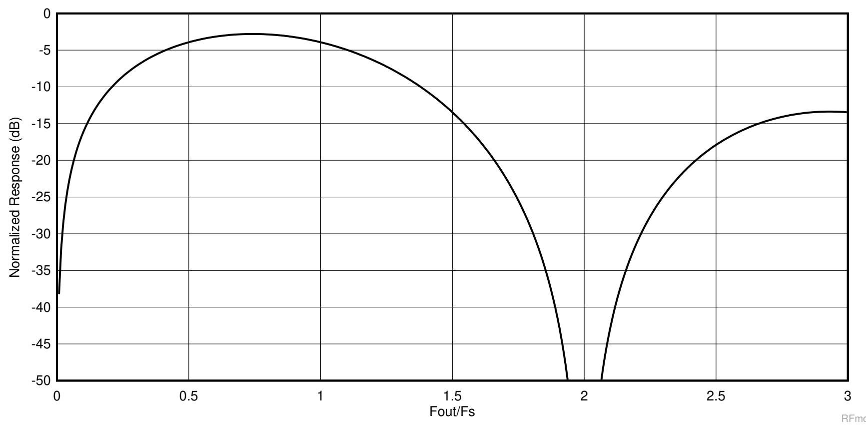


図 7-6. RF Mode Output Waveform Response

7.3.1.4 2xRF Mode

2xRF mode is a combination of RF mode (return to complement) for the first half of the sample period and a return-to-zero for the second half of the sample period. The result is a sinc response that peaks and provides maximum flatness in the 3rd, 4th and 5th Nyquist zones. 2xRF mode is only available in dual channel mode and requires an input clock at twice the DAC sample rate. The timing diagram for 2xRF mode is given in 図 7-7. A plot of the frequency response of RF mode is shown in 図 7-8.

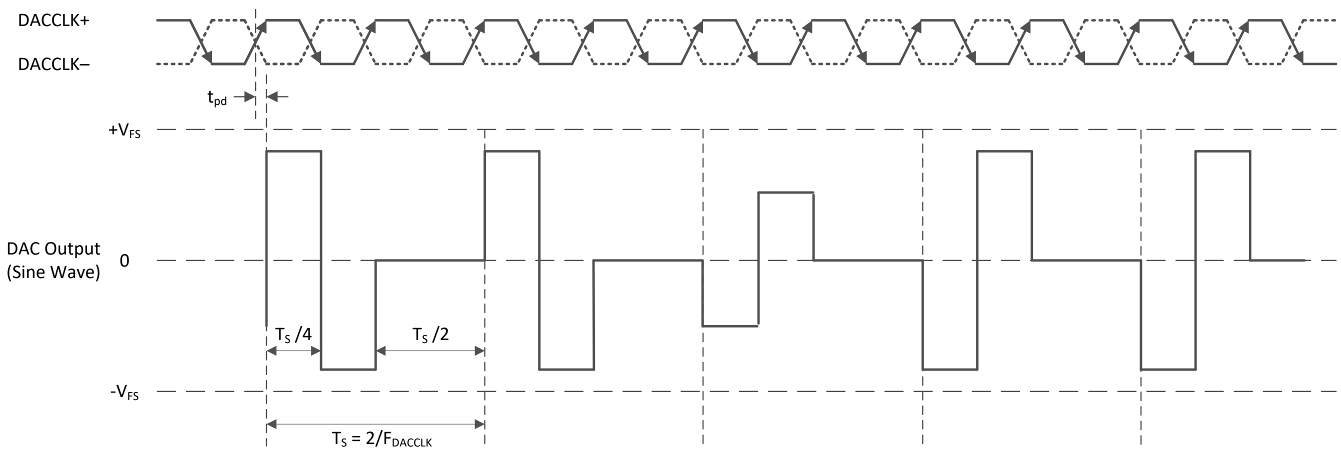


図 7-7. 2xRF Mode Timing Diagram

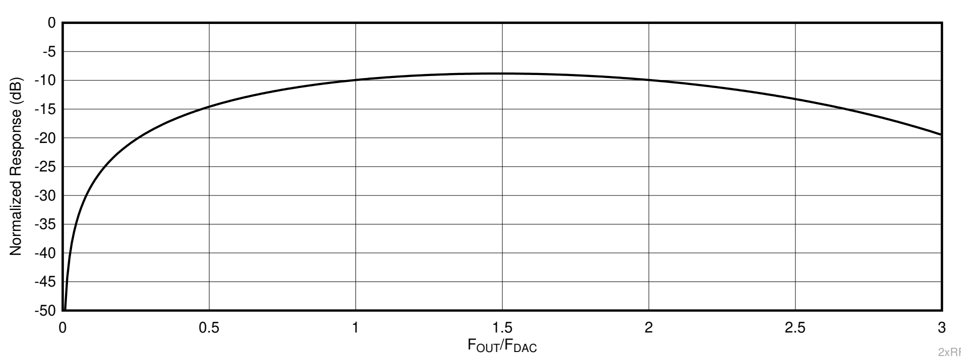


図 7-8. 2xRF Mode Output Waveform Frequency Response

7.3.2 DAC Output Interface

The DAC output is designed for high output frequencies of 8 GHz and above. Careful layout and component choices are needed in order to achieve high output frequencies. The full frequency response of the DAC can be found by combining the analog frequency response of the DAC to the output mode responses shown in セクション 7.3.1.

7.3.2.1 DAC Output Structure

DAC12DL3200 analog output structure is shown in 図 7-9 for one DAC channel. The outputs VOUTx+/- must have a DC path to an external supply voltage, and the DAC sink current from the external supply. A differential termination resistance sits between the two current output pins, VOUTx+/-. The current steering switch array connects to the outputs and steers current between the output pins based on the digital code. A constant DC current bias, I_{BIAS}, draws current from both outputs regardless of the digital code.

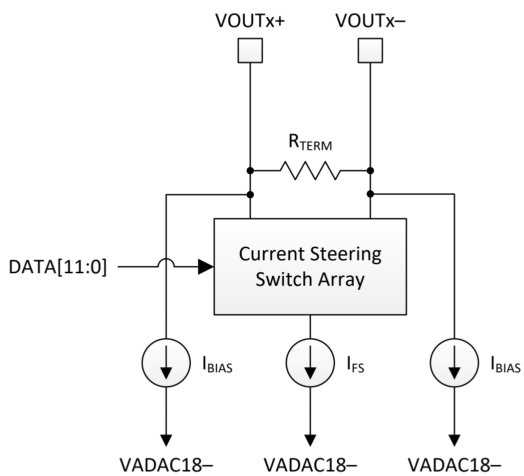


図 7-9. DAC12DL3200 Analog Output Structure

Examples of conversions from digital codes to currents on the VOUTx+/- outputs are given in 表 7-2. The currents provided include both the current steered portion and the bias currents on each leg.

表 7-2. Example Code to Current Conversions

2's COMPLEMENT	IOUTx+ CURRENT	IOUTx- CURRENT
0111 1111 1111	$I_{FS} + I_{BIAS}$	I_{BIAS}
0011 1111 1111	¾ $I_{FS} + I_{BIAS}$	¼ $I_{FS} + I_{BIAS}$
0000 0000 0000	½ $I_{FS} + I_{BIAS}$	½ $I_{FS} + I_{BIAS}$
1100 0000 0001	¼ $I_{FS} + I_{BIAS}$	¾ $I_{FS} + I_{BIAS}$
1000 0000 0000	I_{BIAS}	$I_{FS} + I_{BIAS}$

7.3.2.2 Full-scale Current Adjustment

The total DAC output current is set through the external RBIAS resistor and the COARSE_CUR_A/B and the FINE_CUR_A and FINE_CUR_B registers. There is a switched fullscale current and a static fullscale current. The switched current is divided between VOUTA/B+ and VOUTA/B- in proportion to the digital signal value at the DAC. The static current is fixed at the output of each ball VOUTA/B+ and VOUTA/B-.

The equation for the total DAC switched output current is

$$I_{FSSWITCH} = \frac{3.6k\Omega}{R_{bias}} \times (5mA + 1mA * COARSE + 0.0156mA * FINE)$$

where

- R_{bias} is the external bias resistor

- COARSE is the value of the register COARSE_CUR_A/B (0 to 15)
- FINE is the value of register FINE_CUR_A/FINE_CUR_B (0 to 63)

The static current is a fixed fraction of the switched current

$$I_{FSSTATIC} = 0.125{*}I_{FSSWITCH} \quad (1)$$

With a 3.6kΩ bias resistor, COARSE_CUR_A/B = 15 and FINE_CUR_A/B = 31, $I_{FSSWITCHED}$ is nominaly 20.5mA and $I_{FSSTATIC}$ nominally 2.56mA (on each ball + and -).

7.3.2.3 Example Analog Output Interfaces

There are numerous ways to interface with the DAC analog output. A few are shown below. In all cases a DC path for current must be provided from a positive voltage source, typically VADAC18+. Further, the voltage at each output pin must be within the compliance voltage range for all digital codes.

The most common interface makes use of a transformer or balun. Some transformers have a center tap that can be used to provide a DC bias to the secondary transformer winding. This is demonstrated in 図 7-10. For a center-tapped transformer the center tap should be tied to the VDDA18A and VDDA18B supply voltages. RF choke inductors can be used to provide the DC bias for baluns without a center tap as shown in 図 7-11. The chokes should be well matched and carefully laid out in order to optimize even order distortion suppression. Many high frequency baluns will not have a center tap for the DC bias.

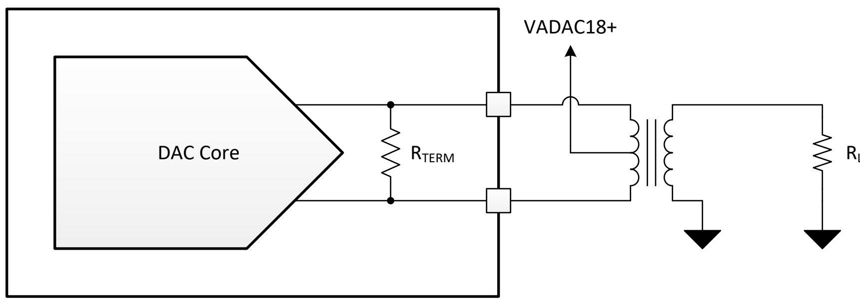


図 7-10. DAC Output Interface using Center-Tapped Transformer

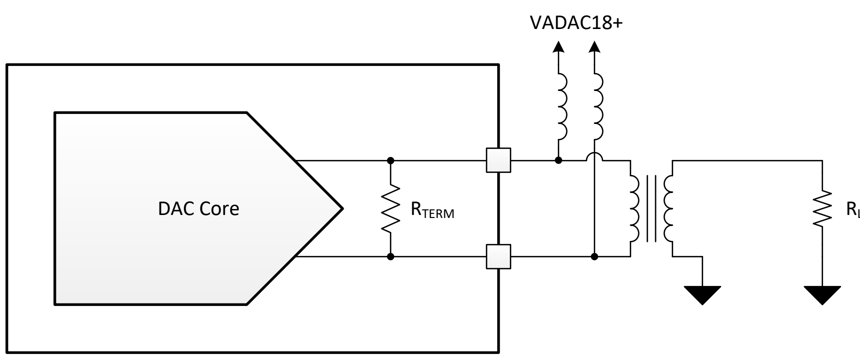


図 7-11. DAC Output Interface using RF Chokes and Transformer

Both transformer and balun output interfaces will not pass DC and low frequency signals. Instead, a higher bias voltage should be used with pull-up resistors to bias the DAC within its compliance voltage range. Careful supply sequencing is required to prevent damage to the DAC if VBIAS exceeds the absolute maximum rated voltage. In all cases, voltages at the DAC pins must be within the absolute maximum rated voltages.

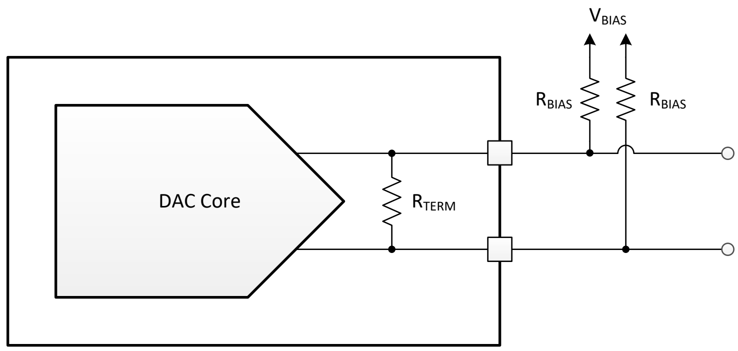


図 7-12. DAC Output Interface with DC Coupling

7.3.3 LVDS Interface

Data is provided to DAC12DL3200 through a parallel low-voltage differential signaling (LVDS) interface. The high input data rate capabilities of the DAC require up to four 12-bit buses resulting in a total of 48 LVDS lanes at up to 1.6 Gbps per lane. Up to four source-synchronous dual-data rate (DDR) clocks, one per 12-bit LVDS bus, are used to simplify interface timing requirements. In addition, four synchronization strobes (DxSTR+/–) can be used in conjunction with SYSREF+/- to achieve deterministic latency through the DAC. The strobes are also used to align the data in modes with multiple input buses per DAC. Flexible interface modes allow a tradeoff in the number of lanes, bit rates and DAC sample rates. The modes are described in 表 7-3. Each mode is described in additional detail in the following sections.

Data samples in all modes are sent to the DAC from earliest sample to latest sample based on the LVDS bus alphabetic order. For example, in MODE0 the first two samples for channel A are sent in order from buses A and B, while the first two samples for channel B are sent in order from buses C and D (See 図 7-14).

表 7-3. DAC12DL3200 Operating Modes

MODE	LVDS_MODE	DCM_MODE	DESCRIPTION	# DACs	TOTAL BUSES	MAX F_{BIT} (Mbps)	MAX F_S (Mbps)	MAX F_{CLK} (MHz)
0	1	0	Dual channel, 2 LVDS banks/channel	2	4	1600	3200	3200
	1	1	2xRF, Dual channel, 2 LVDS banks/channel	2	4	1600	3200	6400
1	0	0	Dual channel, 1 LVDS bank/channel	2	2	1600	1600	1600
	0	1	2xRF, Dual channel, 1 LVDS bank/channel	2	2	1600	1600	3200
2	2	0	Single channel, 4 LVDS banks/channel	1	4	1600	6400	6400

7.3.3.1 MODE0: Two LVDS banks per channel

MODE0 uses two 12-bit LVDS data buses per channel. Due to the high bit rate, each 12-bit LVDS bus has its own dual-data rate (DDR) clock to maximize timing windows resulting in four total data clocks. This mode allows half of the maximum data rate into dual DACs. 表 7-4 shows the LVDS bus, data clock and strobe assignments for each channel. 図 7-13 shows the block diagram for this mode for further understanding, including the signal assignments.

表 7-4. MODE0 LVDS Bus, Data Clock and Strobe Signal Assignments

DAC CHANNEL	LVDS BUSES	DATA CLOCKS	STROBE USED
A	A, B	DACLK, DBCLK	DASTR, DBSTR
B	C, D	DCCLK, DDCLK	DCSTR, DDSTR

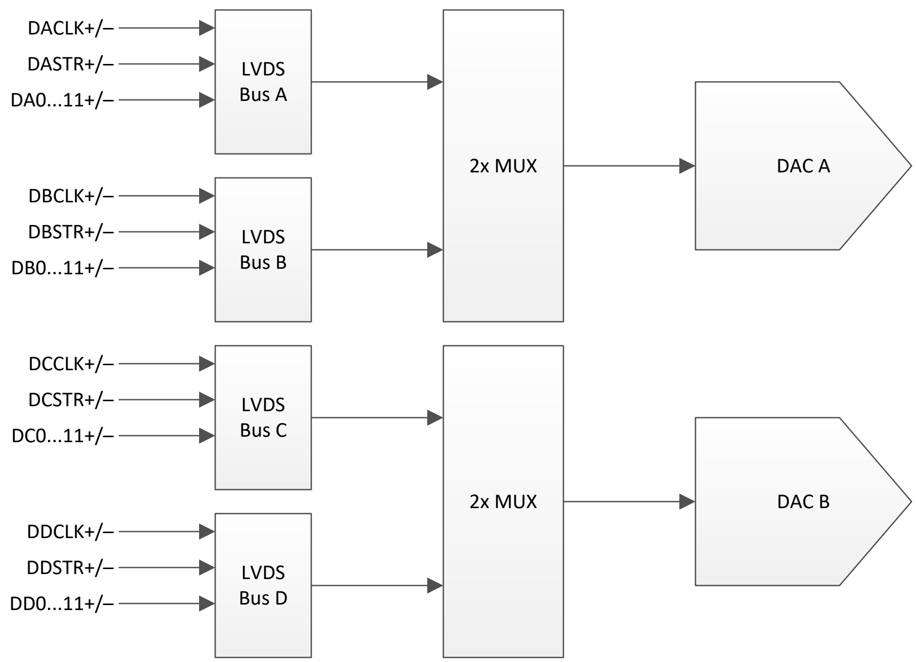


図 7-13. MODE0 Block Diagram

図 7-14 shows the functional timing diagram for MODE0. Four 12-bit buses are used, with buses A and B for DAC channel A data and buses C and D for DAC channel B data. There is no strict timing skew requirement between LVDS buses (e.g. A to B or A to D) as long as the internal FIFOs maintain sufficient offset between read and write pointers.

Having the LVDS banks staggered as shown in 図 7-14 allows the data from each bank to arrive as it is needed and results in minimal latency from each bank. If the LVDS banks have their clocks aligned, then the data on buses B and D are provided to the chip 1 DAC clocks before it is needed.

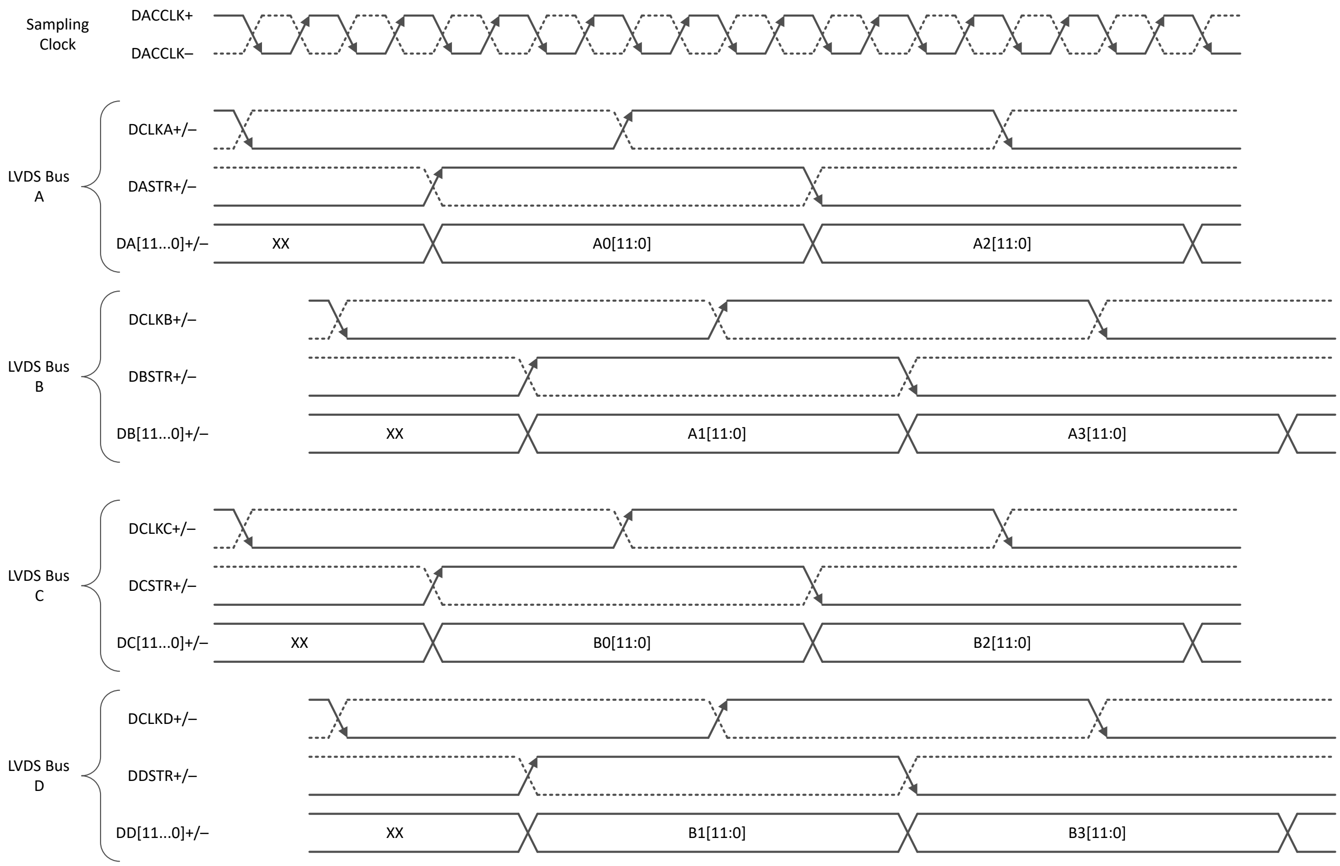


図 7-14. MODE0 Functional Timing Diagram

7.3.3.2 MODE1: One LVDS bank per channel

MODE1 uses one 12-bit LVDS data bus per channel. One dual-data rate (DDR) clock is used for each 12-bit LVDS data bus resulting in two total data clocks. This mode allows one fourth of the maximum sampling rate of the DAC. 表 7-5 shows the LVDS bus, data clock and strobe assignments for each channel. 図 7-15 shows the block diagram for this mode for further understanding, including the signal assignments.

表 7-5. MODE1 LVDS Bus, Data Clock and Strobe Signal Assignments

DAC CHANNEL	LVDS BUSES	DATA CLOCKS	STROBE USED
A	A	DACLK	DASTR
B	C	DCCLK	DCSTR

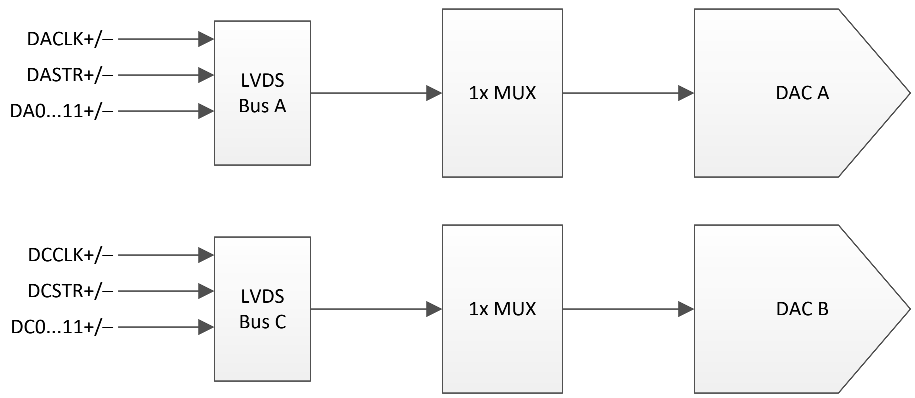


図 7-15. MODE1 Block Diagram

図 7-16 shows the functional timing diagram for MODE1. Two 12-bit buses are used, with bus A for DAC channel A data and bus C for DAC channel B data. There is no strict timing skew requirement between LVDS buses (e.g. A to C) as long as the internal FIFOs maintain sufficient offset between read and write pointers.

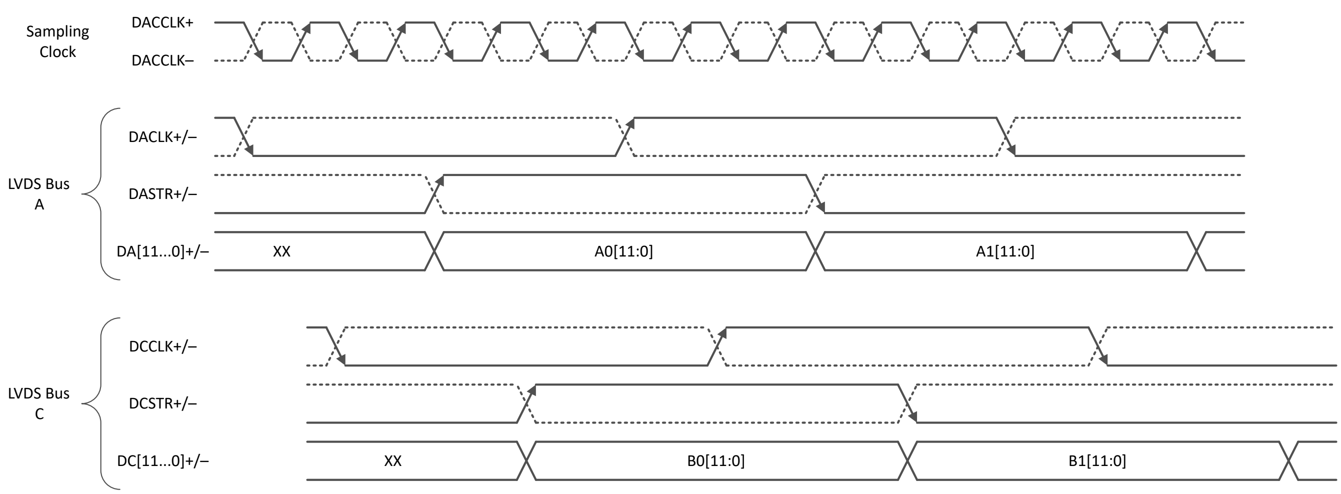


図 7-16. MODE1 Functional Timing Diagram

7.3.3.3 MODE2: Four LVDS banks, single channel mode

MODE2 uses a single DAC channel fed by four 12-bit LVDS data buses resulting in 48 LVDS lanes total. Due to the high bit rate, each 12-bit LVDS bus has its own dual-data rate (DDR) clock to maximize timing windows. This mode allows the maximum data rate into a single DAC. 表 7-6 shows the LVDS bus, data clock and strobe assignments for each channel. 図 7-17 shows the block diagram for this mode for further understanding, including the signal assignments.

表 7-6. MODE2 LVDS Bus, Data Clock and Strobe Assignments

DAC CHANNEL	LVDS BUSES	DATA CLOCKS	STROBE USED
A or B	A, B, C, D	DACLK, DBCLK, DCCLK, DDCLK	DASTR, DBSTR, DCSTR, DDSTR

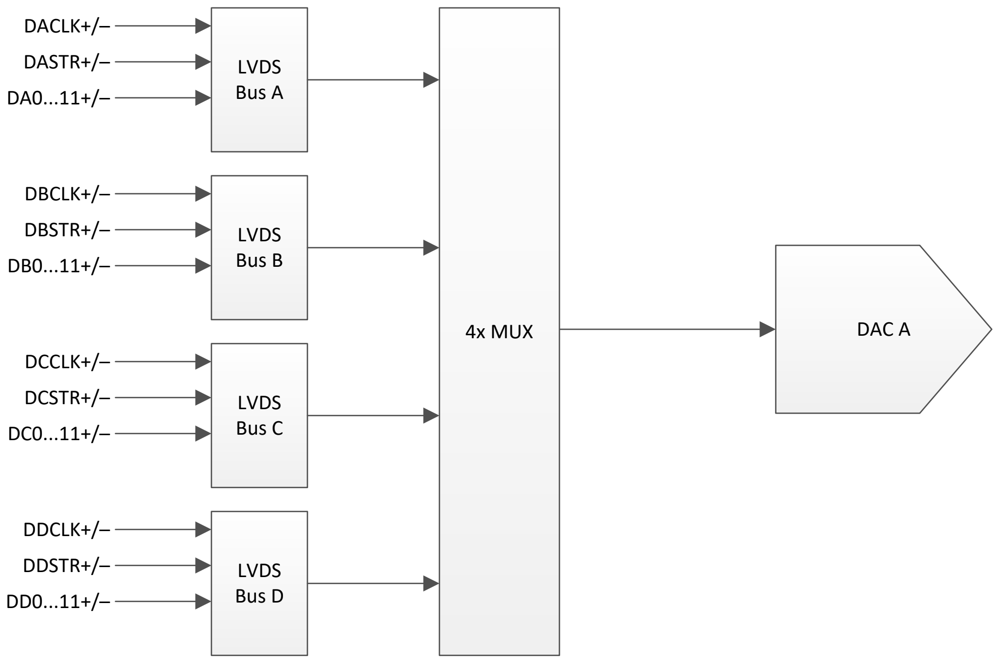


図 7-17. MODE2 Block Diagram

図 7-18 shows the functional timing diagram for MODE2. Four 12-bit buses are used (A, B, C and D) to send data to the DAC. There is no strict timing skew requirement between LVDS buses (e.g. A to B or A to D) as long as the internal FIFOs maintain sufficient offset between read and write pointers.

Having the LVDS banks staggered as shown in 図 7-18 allows the data from each bank to arrive as it is needed and results in minimal latency from each bank. If the LVDS banks have their clocks aligned, then the data on bank 3 is provided to the chip 3 DAC clocks before it is needed.

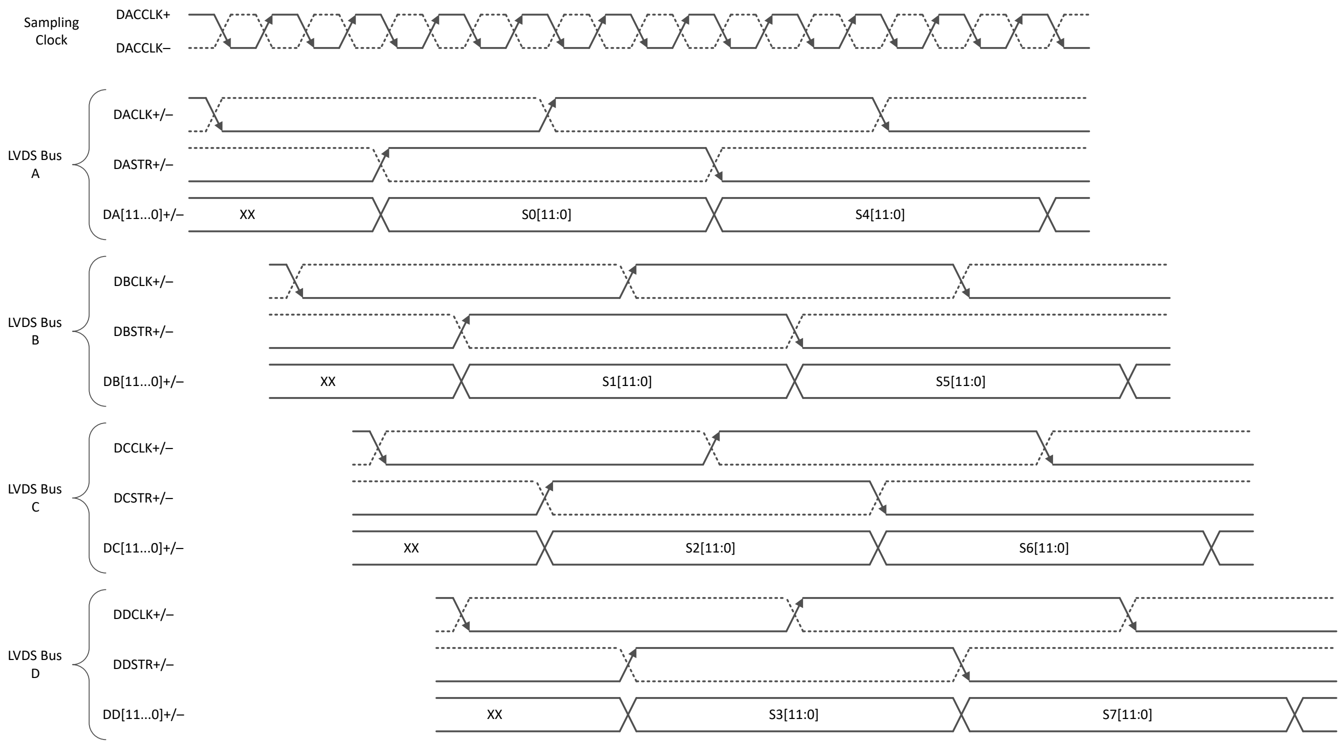


図 7-18. MODE2 Functional Timing Diagram

7.3.3.4 LVDS Interface Input Strobe

The LVDS strobe can be provided on either the dedicated strobe pin or the LSB of the data pins. The strobe can be provided at any multiple of 4 LVDS clocks, which is equivalent to 8 input samples per LVDS bus per DAC. The strobe must be provided on the rising edge of the LVDS clock and coincide with the data captured on that edge. The LVDS strobe is used to reset the FIFO write pointer for each LVDS bus.

When the strobe is provided on the LSB, the actual pin that is used is determined by the LVDS input width set by LVDS_RESOLUTION.

When using the LSB for the strobe pin, a couple of LVDS clocks are required to switch between using the LSB for strobe and using it for data. The user should make sure the data on this bit is held at zero during this transition. The dedicated strobe input needs to be tied low in order to use a strobe on the LSB. If using LSB_SYNC instead of the $\overline{\text{SYNC}}$ pin to switch the LSB between strobe and data, the $\overline{\text{SYNC}}$ input must be tied high.

When the LSB is being used as a strobe (either $\overline{\text{SYNC}}$ is low or register LSB_SYNC=1), the LSB of the input data passed to the datapath will be zero.

Note that there is only one FIFO_DLY setting for the chip. When the FIFO is aligned to the LVDS strobe it aligns to the strobe for LVDS bus 0 (if bus 0 is enabled). Otherwise it aligns to bus 2. This means that in dual DAC mode, it is required that the strobes for the LVDS buses used for DACB must be aligned to the strobes for the LVDS buses for DACA within the FIFO tolerance.

7.3.3.5 FIFO Operation

DAC12DL3200 uses a source-synchronous interface to simplify signal timing. The DDR data clocks are sent from the logic device along with the data such that propagation delays through the logic device and receiving DAC are well matched over all process, voltage and temperature variations. Test patterns can be used to verify proper timing at all LVDS input receivers. Internal FIFOs absorb skew between the data clock domains before being aligned to the DAC sampling clock domain (DACCLK). Each LVDS data bus should have matched trace lengths relative to the associated data clock (e.g. DACLK for bus A), however each bus does not have to be trace length matched to the others due to the internal FIFOs. For example, the signals for bus A (DACLK, DASTR, DA0…11) should be matched in length, but they do not need to be length matched to the signals for bus B.

7.3.3.5.1 Using FIFO Delay Readback Values

The FIFO_DLY_R0 through FIFO_DLY_R3 values provide an approximate value for FIFO_DLY that would result in the sample being used just as it arrives for each channel. These values are asynchronously sampled between clock domains and may vary from channel to channel even with exactly the same relationship between DCLK and DACCLK.

If all four LVDS clocks have the same relationship to the consuming DACCLK (i.e., LVDS clocks DACLK - DDCLK are staggered as shown in LVDS Input waveforms), all FIFO_DLY_R* values should vary by no more than 1 (in a circular sense). If the LVDS clocks are aligned in time, this will result in successive FIFO_DLY_R* values increasing by 1±1. The user must select a FIFO_DLY setting that will work for all banks.

The valid programming range for FIFO_DLY and FIFO_DLY_R* is shown in the following table.

表 7-7. FIFO_DLY and FIFO_DLY_R* range per mode

LVDS_MODE**=2 &** DCM_EN**=0 or** LVDS_MODE**=1 &** DCM_EN**=1**	LVDS_MODE**=1 &** DCM_EN**=0 or** LVDS_MODE**=0 &** DCM_EN**=1**	LVDS_MODE**=0 &** DCM_EN**=0**
0-31	0-15	0-7

7.3.3.5.2 FIFO Delay Handling

Data from the LVDS banks are latched into the write side of the FIFO using the LVDS clock. The user must set FIFO_DLY to an appropriate value to ensure that the data is read away from the point where it is changing. To help with this, the FIFO_DLY_R* registers provide the user with an approximate FIFO_DLY setting that would result in the data being sampled just as it arrives under current conditions.

The number of usable settings for FIFO_DLY is determined by LVDS_MODE and DCM_EN as shown in 図 7-19.

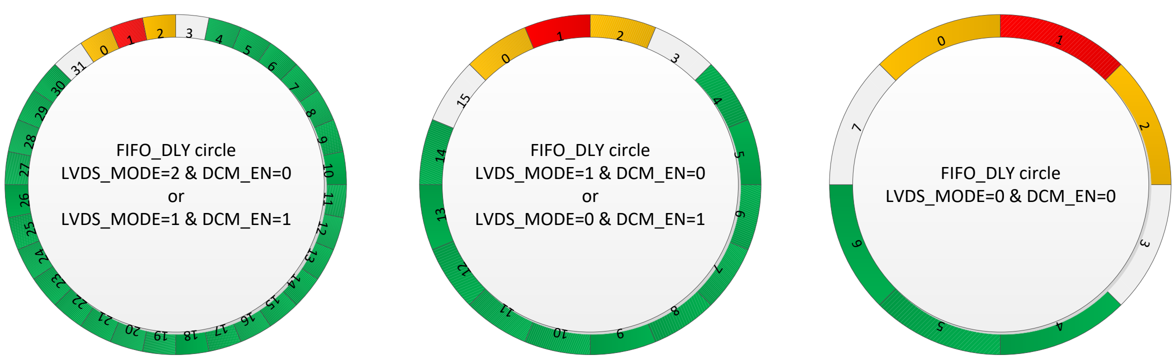


図 7-19. FIFO_DLY Circles

In the above picture we will assume that if FIFO_DLY=1, it would result in the data being sampled just as the input latch is changing. Ideally, FIFO_DLY_R* would report "1" in this condition. In reality, this is not a precise measurement and it will only report a value close to this setting. If minimum latency is not a concern, it may be sufficient to just select a FIFO_DLY value on the opposite side of the circle from the FIFO_DLY_R* value.

Setting FIFO_DLY to a value before (counter-clockwise from) the FIFO_DLY_R* value will result in the lowest possible latency. For example, if running in LVDS_MODE=2, with FIFO_DLY_R*=1, a value of 30 may be an appropriate low latency setting while a value of 4 would be a high latency setting.

If the goal is to create a system with minimum latency, the user will need to characterize the system to find the optimal value of FIFO_DLY that will consistently work across process, voltage and temperature (PVT). The less variation that exists between the SYSREF, LVDSCLK, and DEVCLK, the tighter the FIFO_DLY can be set.

Note that if the LVDS strobe is used to align the DACCLK domain side of the FIFO instead of SYSREF, additional margin should be added to FIFO_DLY to allow for inconsistent setup of the FIFO from one alignment to the next. It is not possible to have deterministic latency using the LVDS strobe.

To help with system characterization, underflow and overflow alarms are provided in FIFO_ALM. It is important to realize toggling data must be provided on the input for these alarms to work. Constant input data will not generate alarms. See FIFO Over/Under Flow Alarming.

To characterize the FIFO_DLY for minimum latency with SYSREF:

1. Align the system using SYSREF (refer to section Startup Procedure with LVDS Input)
2. Read the FIFO_DLY_R* values to determine a reasonable starting point for FIFO_DLY characterization.
3. Set a FIFO_DLY value that is near the sampling point. For example, if FIFO_DLY_R*=1, a setting for 30 might be a good starting point.
4. Characterize the system over PVT and monitor FIFO_ALM for any alarms.
5. If alarms occurred, move FIFO_DLY one setting counter-clockwise and repeat from step 3. If no alarms occurred, move FIFO_DLY one setting clockwise and repeat from step 3. The goal is to determine the tightest setting that will not cause alarms.

It is important to understand that there will be some number of FIFO_DLY settings that are unusable. In 4-banks per DAC mode this may be as many as 4 settings. Reducing the LVDS rate will reduce the number of invalid FIFO_DLY settings.

7.3.3.5.3 FIFO Delay and NCO Operation

The setting for FIFO_DLY shifts the timing of the NCO sync with respect to SYSREF. When DCM_EN=0, the sync is shifted later in time by modulo(FIFO_DLY, 8) DACCLKs with respect to FIFO_DLY =0. When DCM_EN=1, the sync is shifted later in time by modulo(FIFO_DLY, 16) DACCLKs with respect to FIFO_DLY=0. If attempting to output a specific NCO phase with respect to sysref, the FFH_PHASE_A/FFH_PHASE_B registers will need to include the desired setting for FIFO_DLY .

7.3.3.5.4 FIFO Over/Under Flow Alarming

Each of the capture flops on the read side of the FIFO is actually constructed of 3 flops (see 図 7-20). This allows detection of close timing violations that could corrupt the data flop and is used for detecting under and overflow alarms. This will only detect slow drifts. It will not detect sudden jumps in the operation that might jump over the alarm detection. This will also only detect alarms if the violation occurs when the data is changing. Constant input data will not produce alarms.

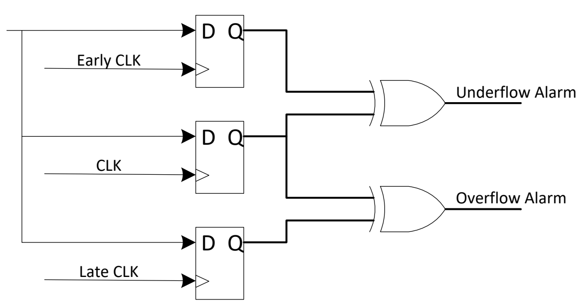


図 7-20. Datapath Showing FIFO Over/Under Flow Alarming

7.3.4 Multi-Device Synchronization (SYSREF+/-)

Synchronizing multiple DAC12DL3200 involves two synchronization functions as illustrated by 図 7-21. The first is to synchronize the DACCLK clock domain in all DAC devices which includes clock dividers and FIFO outputs pointers. Secondly, the data clock domain (LVDS interface) must be synchronized using an input strobe signal from either the DxSTR input or LSB data lane of each bus (bit x, where x = [12 - LVDS_RESOLUTION]).Using the LSB eliminates the need for the DxSTR signals eliminating up to four LVDS pairs. Synchronization using DxSTR and LSB is described in セクション 7.3.3.4.

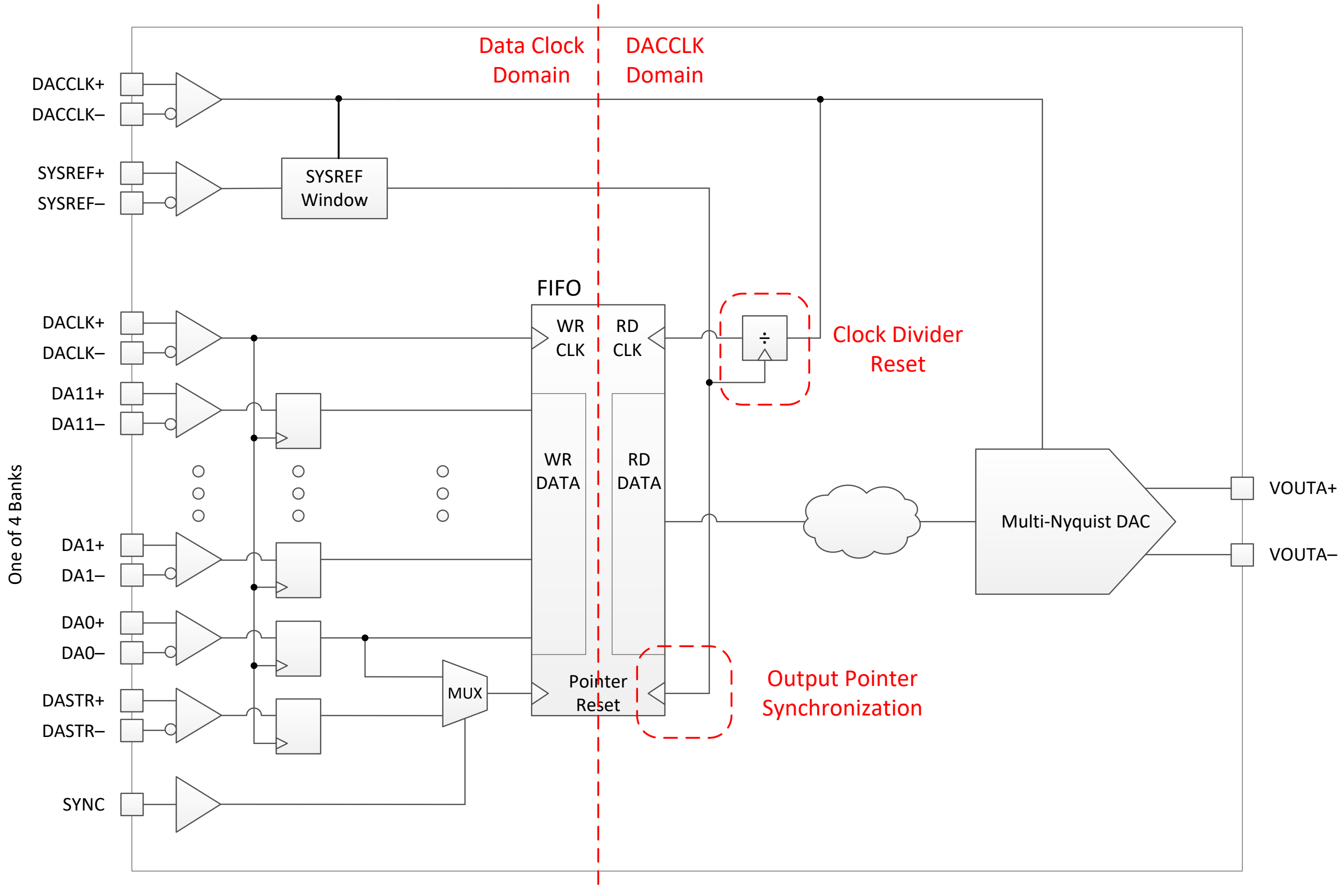


図 7-21. FIFO Synchronization Logic Diagram

7.3.4.1 DACCLK Domain Synchronization

DACCLK domain synchronization is accomplished by providing SYSREF to each DAC and capturing it in the same DACCLK cycle at each DAC. SYSREF can be a continuous signal or a single pulse, however if run continuously it must be an integer division of DACCLK/(8*# LVDS buses per channel), meaning DACCLK/(8*# LVDS buses per channel*n) where n is any integer greater than or equal to 1. SYSREF can also be run continuously during synchronization and shutoff after synchronization has been achieved by disabling SYSREF processing through the SPI interface before stopping the SYSREF signal.

7.3.4.2 SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)

The SYSREF windowing block is used to first detect the position of SYSREF relative to the DEVCLK rising edge and then to select a desired SYSREF sampling instance, to maximize setup and hold timing margins. In many cases a single SYSREF sampling position (SYSREF_SEL) is sufficient to meet timing for all systems (part-to-part variation) and conditions (temperature and voltage variations). However, the feature can also be used by the system to expand the timing window by tracking the movement of SYSREF as operating conditions change or to remove system-to-system variation at production test by finding a unique optimal value at nominal conditions for each system.

Use of the SYSREF windowing block is as follows. First, the device clock and SYSREF should be applied to the device. The location of SYSREF relative to the device clock cycle is determined and stored in SYSREF_POS. Each bit of SYSREF_POS represents a potential SYSREF sampling position. If a bit in SYSREF_POS is set to '1', then the corresponding SYSREF sampling position has a potential setup or hold violation. Upon determining the valid SYSREF sampling positions (the positions of SYSREF_POS that are set to '0') the desired sampling position can be chosen by setting SYSREF_SEL to the value corresponding to that SYSREF_POS position. In general the middle sampling position between two setup and hold instances should be chosen. Ideally, SYSREF_POS and SYSREF_SEL should be performed at the system's nominal operating conditions (temperature and supply voltage) to provide maximum margin for operating condition variations. This process can be performed at final test and the optimal SYSREF_SEL setting can be stored for use at every system power up. Further, SYSREF_POS can be used to characterize the skew between DEVCLK and SYSREF over operating conditions for a system by sweeping the system temperature and supply voltages. For systems that have large variations in DEVCLK to SYSREF skew this characterization can be used to track the optimal SYSREF sampling position as system operating conditions change. In general, a single value can be found that meets timing over all conditions for well matched systems, such as those where DEVCLK and SYSREF come from a single clocking device.

The step size between each SYSREF_POS sampling position can be adjusted using SYSREF_ZOOM. When SYSREF_ZOOM is set to '0', the delay steps are more coarse. When SYSREF_ZOOM is set to '1', the delay steps finer steps. In general, SYSREF_ZOOM should always be used (SYSREF_ZOOM = 1) unless a transition region (defined by 1's in SYSREF_POS) is not seen, which is possible for low clock rates. Bits 0 and 15 of SYSREF_POS will always be set to '1' since it cannot be determined if these settings are close to a timing violation, although the actual valid window could extend beyond these sampling positions. The value programmed into SYSREF_SEL is the decimal number representing the desired bit location in SYSREF_POS.

The table below shows some example SYSREF_POS readings and the optimal SYSREF_SEL settings. In general, lower values of SYSREF_SEL should be selected due to variation of the delays over supply voltage, however in the second example a value of 8 provides additional margin and may be selected instead.

表 7-8. Examples of SYSREF_POS Readings and SYSREF_SEL Selections

SYSREF_POS**[15:0]**	**OPTIMAL** SYSREF_SEL **SETTING**
b11100000_00011001	8 or 9
b10011000_00110001	2 or 8
b11100000_00000001	6 or 7
b10000011_00000001	4
b11100011_00011001	6

To use the SYSREF windowing:

1. Apply SYSREF and DEVCLK
2. Set SYSREF_RECV_SLEEP=0, SYSREF_POS_SEL=0, and SYSREF_ZOOM=1
3. Set SYSREF_PROC_EN=1
4. Read SYSREF_POS and determine proper setting for SYSREF_SEL. If proper sampling point cannot be determined, set SYSREF_ZOOM=0 and retry.

The SYSREF_POS register can report either an accumulation of all the SYSREF edges seen since SYSREF_PS_EN transitioned from 0 to 1 (infinite persistence) or just the last SYSREF edge (when SYSREF_PS_EN=0). The user should reset the persistence after changing SYSREF_POS_SEL.

7.3.5 Alarms

DAC12DL3200 contains a number of alarms that can be used to determine whether the DAC is operating optimally, marginally, or in a faulty state. These alarms are sticky, such that if an error occurs then the alarm will be set and remain set until 1's are written to that alarm register to reset the alarm.

The alarms are not valid until the part is fully programmed and operating. At this point, the alarm registers should all be cleared. They can then be monitored periodically, or by watching the ALARM pin, to determine if an alarm has occurred. The alarms that trigger the ALARM pin can be selected by unmasking the alarms in register ALM_MASK.

If an alarm occurs, the DAC can be programmed to mute the output signal until all alarms have been cleared. When this occurs, the faulty condition should be fixed by the system before resuming operation.

The alarms include:

- FIFO empty alarm
- FIFO full alarm
- LVDS Clock alarm
- LVDS Strobe alarm
- TRIGCLK realignment alarm
- Clock realignment alarm
- Clock alignment alarm

7.4 Device Functional Modes

7.4.1 Direct Digital Synthesis (DDS) Mode

The DAC12DL3200 contains two numerically controlled oscillators (NCOs) that can optionally be used for direct digital synthesis of tones for each DAC. The block diagram for the DDS is shown in 図 7-22. There are two NCO banks, each with 16 separate 32-bit NCOs. The banks can be used separately for each DAC, or together to provide 32 NCOs for one DAC. The two NCOs can be summed as a two tone source for one DAC. The NCO can be selected either through registers NCO_SEL_A and NCO_SEL_B, or through balls NCOSEL[0:3] and NCOBANKSEL.

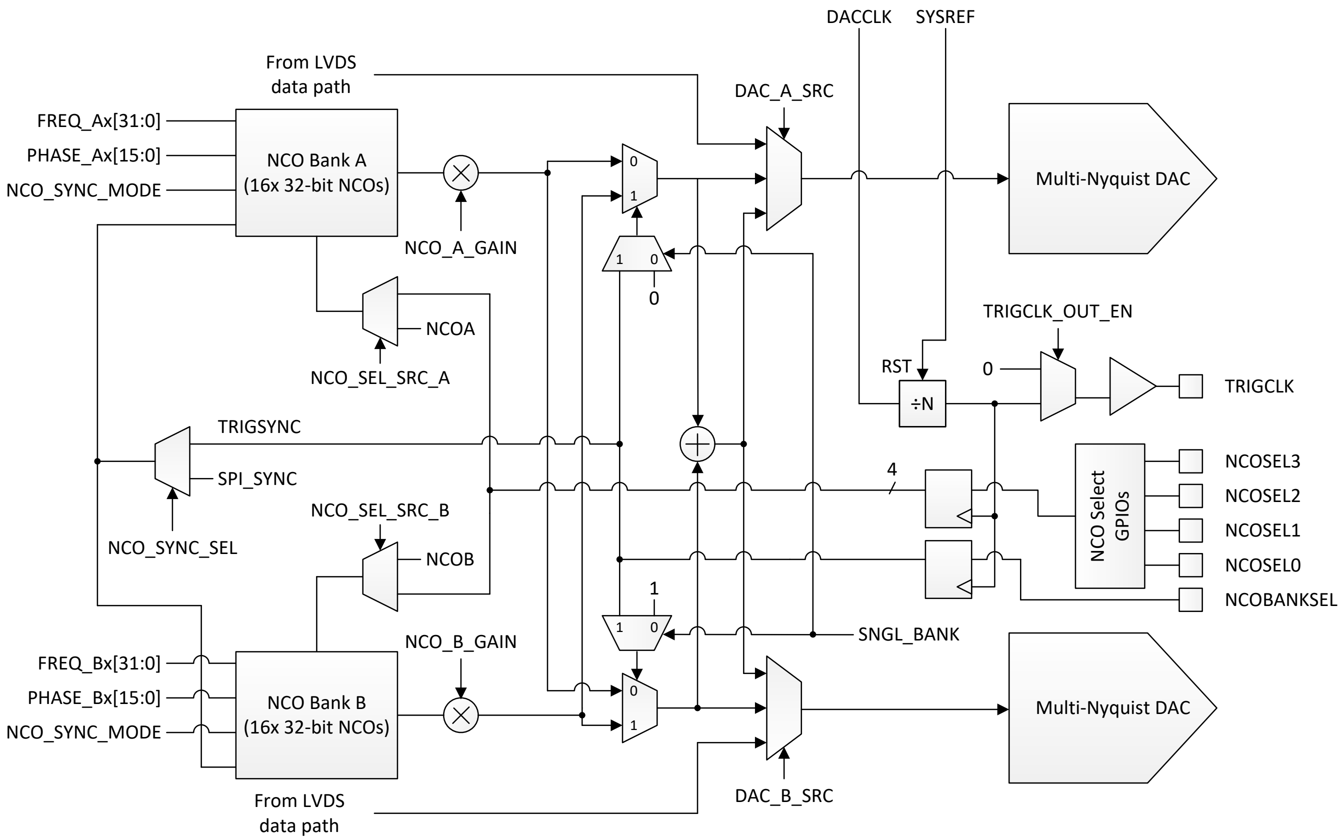


図 7-22. DDS Block Diagram

7.4.1.1 NCO Gain Scaling

The NCO output value is internally scaled based on the dither setting to ensure that the output will not saturate. The scaling point is selected to prevent unnecessary quantization error.

The sine wave generation produces full-scale positive values that are one LSB higher than can be represented by the DAC output. In addition, ~1/2 LSB of dither is added to the signal before rounding. Thus setting NCO_GAIN_A or NCO_GAIN_B to values below 0x0003 results in clipping for some frequencies. This range also needs to be taken into account when summing the two NCOs.

When $\overline{\text{TXENABLE}}$ transitions low, the output of the NCO is linearly scaled to zero in a programmable number of clocks set by NCO_RAMPRATE . The same setting is used when $\overline{\text{TXENABLE}}$ transition high.

7.4.1.2 NCO Phase Continuous Operation

To operate the NCO in phase continuous mode, the user can change the frequency word instead of switching to a different NCO. NCO_CHG_BLK must be used when changing frequency values while NCO_EN =1. Phase continuous operation is only supported using FFH_FREQ_A[0] and FFH_FREQ_B[0].

7.4.1.3 Trigger Clock

The trigger clock (TRIGCLK) is an output clock generated by dividing the input CLK+/- according to register TRIG_DIV. The trigger clock is output when TRIG_OUT_EN=1 and NCO_EN=1.

The divider is reset on each rising edge of SYSREF. If a SYSREF edge is detected that realigns the system clock divider, CLK_REALIGNED_ALM (register SYS_ALM) will be set. If this occurs, the trigger clock location will have moved even though TRIG_REALIGNED_ALM is not set. The TRIG_REALIGNED_ALM is set when a SYSREF edge realigns the trigger clock divider. When TRIG_REALIGNED_ALM occurs without CLK_REALIGNED_ALM or CLK_ALIGNMENT_ALM, this indicates that the SYSREF period is not an integer multiple of the trigger clock period. Be aware that if the CLK_REALIGNED_ALM occurs while NCO_EN is high, the state of the NCO accumulators may be corrupted.

NCOBANKSEL and NCOSEL[3:0] inputs are sampled by TRIGCLK, even when TRIG_OUT_EN=0. This allows the user to turn on the trigger clock output to find the phase of the trigger clock, and then turn it off to prevent the output from injecting noise into the DAC.

The value sampled by TRIGCLK is applied to both channels with a fixed relationship to the effective SYSREF edge.

If the SYSREF location changes during operation, it may require 2 SYSREF pulses at the new location to properly realign the trigger clock.

Be aware that the trigger clock may respond to changes in SYSREF position even though SYSREF_ALIGN_EN=0. If this occurs TRIG_REALIGNED_ALM will be set. If SYSREF returns to its correct position, the trigger clock will also return to its correct position. However, if SYSREF remains at the new alignment, the entire system must be realigned (using SYSREF_ALIGN_EN) to restore the proper relationship between SYSREF and trigger clock

7.5 Programming

7.5.1 Using the Serial Interface

The serial interface is accessed using the following four pins: serial clock (SCLK), serial data in (SDI), serial data out (SDO), and serial interface chip-select ($\overline{SCS}$). Register access is enabled through the $\overline{SCS}$ pin.

7.5.1.1 $\overline{SCS}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

7.5.1.2 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

7.5.1.3 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. Setup and hold times with respect to the SCLK must be observed.

7.5.1.4 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the R/W bit and register address portion of read bus cycles.

7.5.1.5 Serial Interface Operation

As shown in 図 7-23, each register access consists of 24 bits. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be accessed. During write operations, the last eight bits are the data written to the addressed register. The data are shifted in MSB first. During read operations, the last eight bits on SDI are ignored and, during this time, the SDO outputs the data from the addressed register.

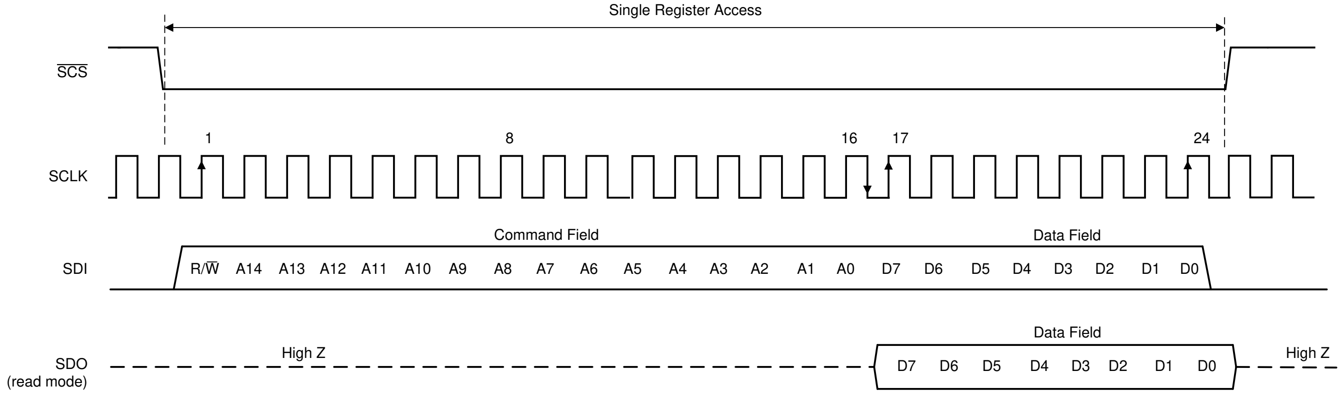


図 7-23. Serial Interface Protocol: Single Read/Write

7.5.1.6 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifies the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{SCS}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8-bit transfer of the streaming transaction. Register bit ASCEND controls whether the address value ascends (increments) or descends (decrements). 図 7-24 shows the streaming mode transaction details.

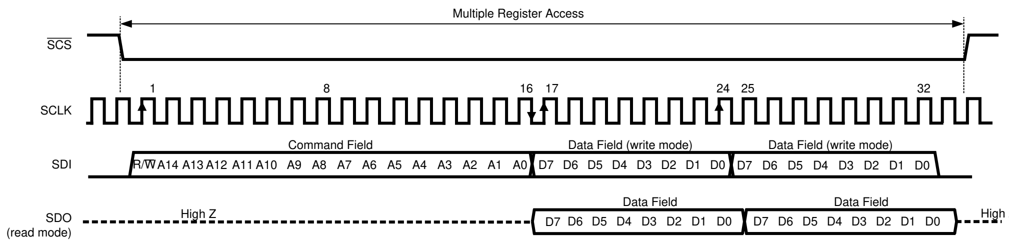


図 7-24. Serial Interface Protocol: Streaming Read/Write

See セクション 7.5.2 for detailed information regarding the registers.

7.5.2 SPI Register Map

表 7-10 lists the SPI registers. All register addresses not listed in 表 7-10 should be considered as reserved locations and the register contents should not be modified. Reserved fields should be written to their default settings. Multi-byte registers are always in little-endian format (least significant byte stored at the lowest address).

The different register types are listed in 表 7-9.

表 7-9. Register Types

Type	Description
R	Read Only
R/W	Read and Write
W1C	Write 1 to Clear

表 7-10. SPI Registers

Address	Acronym	Register Name	Section
0h	CONFIG_A	Configuration A	Go
2h	DEVICE_CONFIG	Device Configuration	Go
3h	CHIP_TYPE	Chip Type	Go
4h	CHIP_ID	Chip Identification	Go
6h	CHIP_VERSION	Chip Version	Go
Ch	VENDOR_ID	Vendor Identification	Go
20h	PIN_CFG	Pin Configuration	Go
21h	TXEN_SEL	Transmitter Enable Control Selection	Go
22h	TXEN	Transmitter Enable Configuration	Go
3Ch	IO_STATE	Current State of Input IOs	Go
48h	DCM_EN	Dual Clock Mode	Go
50h	TRIG_DIV	Trigger Clock Divide	Go
51h	TRIG_OUT_EN	Trigger Clock Output Enable	Go
80h	SYSREF_CTRL	SYSREF Control	Go
90h	SYSREF_POS	SYSREF Capture Position	Go
100h	DP_EN	Datapath Enable	Go

表 7-10. SPI Registers (continued)

Address	Acronym	Register Name	Section
101h	CH_CFG	Channel Configuration	Go
106h	LVDS_CFG	LSB Strobe Control	Go
107h	LVDS_TERM	LVDS Termination Configuration	Go
140h	DITH_EN	DAC Dither Enable	Go
160h	MXMODE	DAC Output Mode	Go
170h	COARSE_CUR	Coarse Current Control (DAC A and B)	Go
171h	CUR_A	Current Control for DAC A	Go
172h	CUR_B	Current Control for DAC B	Go
180h	SPIDAC_CHG_BLK	SPIDAC Change Block	Go
181h	SPIDAC_VALUE	Sample Value for SPIDAC Mode	Go
1A0h	SHUNTREF-EN	Enable Shunt Regulators	Go
200h	FIFO_DLY	FIFO Delay	Go
210h	FIFO_DLY_R0	Current FIFO Delay for FIFO0	Go
211h	FIFO_DLY_R1	Current FIFO Delay for FIFO1	Go
212h	FIFO_DLY_R2	Current FIFO Delay for FIFO2	Go
213h	FIFO_DLY_R3	Current FIFO Delay for FIFO3	Go
220h	FIFO_ALIGN	FIFO Alignment Control	Go
300h	NCO_SYNC	NCO Sync Source Select	Go
301h	NCO_SPISEL	NCO Fast-Frequency Hopping Frequency Selection	Go
303h	NCO_BANKCFG	NCO Bank Configuration	Go
308h	NCO_EN	NCO Enable	Go
310h	SPI_SYNC	SPI Sync	Go
320h	NCO_CHG_BLK	NCO Change Blocking	Go
330h	NCO_RAMPRATE	NCO Ramp Rate Control	Go
331h	NCO_CONFIG	NCO Ramp Rate Control	Go
332h	NCO_GAIN_A	Gain Backoff for NCO A	Go
334h	NCO_GAIN_B	Gain Backoff for NCO B	Go
400h	FFH_FREQ_A[15:0]	Frequency Word for Fast-Frequency Hopping	Go
440h	FFH_FREQ_B[15:0]	Frequency Word for Fast-Frequency Hopping	Go
480h	FFH_PHASE_A[15:0]	Phase Word for Fast-Frequency Hopping	Go
4A0h	FFH_PHASE_B[15:0]	Phase Word for Fast-Frequency Hopping	Go
700h	TS_TEMP	Temperature Reading in Celsius	Go
701h	TS_SLEEP	Temperature Sensor Sleep	Go
710h	IOTEST_CFG	IOTEST Configuration	Go
711h	IOTEST_CTRL	IOTEST Control	Go
712h	IOTEST_SUM	IOTEST Status	Go
720h	IOTEST_PAT[7:0]	IOTEST Pattern Memory	Go
750h	IOTEST_STAT0	IOTEST Bank0 Failure Status	Go
752h	IOTEST_STAT1	IOTEST Bank1 Failure Status	Go
754h	IOTEST_STAT2	IOTEST Bank2 Failure Status	Go
756h	IOTEST_STAT3	IOTEST Bank3 Failure Status	Go
760h	IOTEST_CAP0[7:0]	IOTEST Bank0 Capture Memory	Go
770h	IOTEST_CAP1[7:0]	IOTEST Bank1 Capture Memory	Go
780h	IOTEST_CAP2[7:0]	IOTEST Bank2 Capture Memory	Go
790h	IOTEST_CAP3[7:0]	IOTEST Bank3 Capture Memory	Go

表 7-10. SPI Registers (continued)

Address	Acronym	Register Name	Section
800h	SYNC_STATUS	Synchronization Status	Go
820h	FIFO_ALM	FIFO Alarm Status	Go
821h	LVDS_ALM	LVDS Strobe Alarm	Go
822h	SYS_ALM	System Alarm Status	Go
823h	ALM_MASK	Alarm Mask	Go
824h	MUTE_MASK	DAC Mute Mask	Go
900h	FUSE_STATUS	Fuse Status	Go
B02h	SYSREF_PS_EN	SYSREF Windowing Persistence Enable	Go

7.5.2.1 CONFIG_A Register (Address = 0h) [reset = 30h]

CONFIG_A is shown in 図 7-25 and described in 表 7-11.

Return to the Summary Table.

Configuration A (default: 0x30)

図 7-25. CONFIG_A Register

7	6	5	4	3	2	1	0
SOFT_RESET	RESERVED	ASCEND	RESERVED	RESERVED			
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h			

表 7-11. CONFIG_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0h	Writing a 1 to this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing and will always read zero. After writing this bit, the part may take up to 5 ns to reset. During this time, do not perform any SPI transactions.
6	RESERVED	R/W	0h	
5	ASCEND	R/W	1h	0 : Address is decremented during streaming reads/writes 1 : Address is incremented during streaming reads/writes (default)
4	RESERVED	R	1h	Always read 1.
3-0	RESERVED	R/W	0h	

7.5.2.2 DEVICE_CONFIG Register (Address = 2h) [reset = 00h]

DEVICE_CONFIG is shown in 図 7-26 and described in 表 7-12.

Return to the Summary Table.

Device Configuration (default: 0x00)

図 7-26. DEVICE_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED						MODE	
R/W-0h						R/W-0h	

表 7-12. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	

表 7-12. DEVICE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	MODE	R/W	0h	0 : Normal operation (default) 1 : Full operation with reduced power/performance (not supported). 2 : Sleep operation (low power, fast resume). This will sleep both DACs, clock receiver, bandgap, LVDS receivers, and temp sensor. 3 : Full power down (lowest power, slowest resume).

7.5.2.3 CHIP_TYPE Register (Address = 3h) [reset = 04h]

CHIP_TYPE is shown in 図 7-27 and described in 表 7-13.

Return to the Summary Table.

Chip Type (read-only: 0x04)

図 7-27. CHIP_TYPE Register

7	6	5	4	3	2	1	0
RESERVED				CHIP_TYPE			
R/W-0h				R-4h			

表 7-13. CHIP_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-0	CHIP_TYPE	R	4h	Always returns 0x4, indicating that the part is a high speed DAC.

7.5.2.4 CHIP_ID Register (Address = 4h) [reset = 3Ah]

CHIP_ID is shown in 図 7-28 and described in 表 7-14.

Return to the Summary Table.

Chip Identification (read-only)

図 7-28. CHIP_ID Register

15	14	13	12	11	10	9	8
CHIP_ID							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHIP_ID							
R-3Ah							

表 7-14. CHIP_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CHIP_ID	R	003Ah	Always returns 3A, indicating it is a DAC12DL3200

7.5.2.5 CHIP_VERSION Register (Address = 6h) [reset = 2h]

CHIP_VERSION is shown in 図 7-29 and described in 表 7-15.

Return to the Summary Table.

Chip Version (read-only)

図 7-29. CHIP_VERSION Register

7	6	5	4	3	2	1	0
CHIP_VERSION							
R-2h							

表 7-15. CHIP_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHIP_VERSION	R	2h	

7.5.2.6 VENDOR_ID Register (Address = Ch) [reset = 0451h]

VENDOR_ID is shown in 図 7-30 and described in 表 7-16.

Return to the Summary Table.

Vendor Identification (default: 0x0451)

図 7-30. VENDOR_ID Register

15	14	13	12	11	10	9	8
VENDOR_ID							
R-451h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VENDOR_ID							
R-451h							

表 7-16. VENDOR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_ID	R	451h	

7.5.2.7 PIN_CFG Register (Address = 20h) [reset = 00h]

PIN_CFG is shown in 図 7-31 and described in 表 7-17.

Return to the Summary Table.

Pin Configuration (default: 0x00)

図 7-31. PIN_CFG Register

7	6	5	4	3	2	1	0
RESERVED							SLEEP_CFG
R/W-0h							R/W-0h

表 7-17. PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SLEEP_CFG	R/W	0h	Set the behavior of the sleep input (SLEEP pin on part): 0: Asserting the pin is equivalent to setting MODE = 2 1: Asserting the pin is equivalent to setting MODE = 3 Note: Asserting the sleep input only affects the behavior of the part, not the value in the MODE register.

7.5.2.8 TXEN_SEL Register (Address = 21h) [reset = 0Fh]

TXEN_SEL is shown in 図 7-32 and described in 表 7-18.

Return to the Summary Table.

Transmitter Enable Control Selection (default: 0x0F)

図 7-32. TXEN_SEL Register

7	6	5	4	3	2	1	0
RESERVED				AUTOMUTE_B	AUTOMUTE_A	USE_TXEN_B	USE_TXEN_A
R/W-0h				R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 7-18. TXEN_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	AUTOMUTE_B	R/W	1h	When set, DACB is automatically muted by alarms whose mute mask is not set. When cleared, DACB is not automatically muted by any alarms.
2	AUTOMUTE_A	R/W	1h	When set, DACA is automatically muted by alarms whose mute mask is not set. When cleared, DACA is not automatically muted by any alarms.
1	USE_TXEN_B	R/W	1h	0: DACB is controlled by the txenable input (TXENABLE pin on part). In this mode, TXEN_B is ignored. 1: DACB is controlled by TXEN_B. In this mode the txenable input does not affect DACB.
0	USE_TXEN_A	R/W	1h	[0] USE_TXEN_A 0: DACA is controlled by the txenable input (TXENABLE pin on part). In this mode, TXEN_A is ignored. 1: DACA is controlled by TXEN_A. In this mode the txenable input does not affect DACA.

7.5.2.9 TXEN Register (Address = 22h) [reset = 00h]

TXEN is shown in 図 7-33 and described in 表 7-19.

Return to the Summary Table.

Transmitter Enable Configuration (default: 0x00)

図 7-33. TXEN Register

7	6	5	4	3	2	1	0
RESERVED						TXEN_B	TXEN_A
R/W-0h						R/W-0h	R/W-0h

表 7-19. TXEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	TXEN_B	R/W	0h	When USE_TXEN_B = 1, this bit controls the transmitter enable for DACB.
0	TXEN_A	R/W	0h	When USE_TXEN_A = 1, this bit controls the transmitter enable for DACA.

7.5.2.10 IO_STATE Register (Address = 3Ch) [reset = 0h]

IO_STATE is shown in 図 7-34 and described in 表 7-20.

Return to the Summary Table.

Current State of Input IOs (read-only)

図 7-34. IO_STATE Register

7	6	5	4	3	2	1	0
SLEEP_IN	SYNCB_IN	TXENABLE_IN	NCO_BANKSEL_IN	NCO_SEL_IN			
R-0h	R-0h	R-0h	R-0h	R-0h			

表 7-20. IO_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEEP_IN	R	0h	Returns the current state of the sleep input.
6	SYNCB_IN	R	0h	Returns the current state of the sync_n input.
5	TXENABLE_IN	R	0h	Returns the current state of the txenable input.
4	NCO_BANKSEL_IN	R	0h	Returns the sampled value on nco_banksel at the last rising edge of trig_c. This value will not update if DEVCLK is not running.
3-0	NCO_SEL_IN	R	0h	Returns the sampled value on nco_sel at the last rising edge of trig_c. This value will not update if DEVCLK is not running.

7.5.2.11 DCM_EN Register (Address = 48h) [reset = 0h]

DCM_EN is shown in 図 7-35 and described in 表 7-21.

Return to the Summary Table.

Dual Clock Mode (default:0x00)

図 7-35. DCM_EN Register

7	6	5	4	3	2	1	0
RESERVED							DCM_EN
R/W-0h							R/W-0h

表 7-21. DCM_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	DCM_EN	R/W	0h	0: Single Clock Mode (SCM) – DAC puts out each sample for one clock 1: Dual Clock Mode (DCM) – DAC puts out each sample for two clocks Note: This register should only be changed when DP_EN=0 Note: Enabling transmission while DCM_EN=1 && LVDS_MODE=2 will result in undefined behavior. Enabling transmission while DCM_EN=0 && (MXMODE_A=3 || MXMODE_B=3) will result in undefined behavior.

7.5.2.12 TRIG_DIV Register (Address = 50h) [reset = 0h]

TRIG_DIV is shown in 図 7-36 and described in 表 7-22.

Return to the Summary Table.

Trigger Clock Divide (default: 0x7F)

図 7-36. TRIG_DIV Register

7	6	5	4	3	2	1	0
RESERVED	TRIG_DIV						
R/W-0h	R/W-0h						

表 7-22. TRIG_DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-0	TRIG_DIV	R/W	0h	FTRIGCLK = FDEVCLK / 8 /(DCM_EN+1)/ (TRIG_DIV+1) Note: TRIG_DIV should be programmed to keep the output clock <100MHz. Note: This register should only be changed when NCO_EN=0

7.5.2.13 TRIG_OUT_EN Register (Address = 51h) [reset = 00h]

TRIG_OUT_EN is shown in 図 7-37 and described in 表 7-23.

Return to the Summary Table.

Trigger Clock Output Enable (default: 0x00)

図 7-37. TRIG_OUT_EN Register

7	6	5	4	3	2	1	0
RESERVED							TRIG_OUT_EN
R/W-0h							R/W-0h

表 7-23. TRIG_OUT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	TRIG_OUT_EN	R/W	0h	0: trig_clk output is driven low 1: The trigger clock (trig_c) is driven on the trig_clk output whenever NCO_EN is high.

7.5.2.14 SYSREF_CTRL Register (Address = 80h) [reset = 002000h]

SYSREF_CTRL is shown in 図 7-38 and described in 表 7-24.

Return to the Summary Table.

SYSREF Control (default: 0x200000)

図 7-38. SYSREF_CTRL Register

15	14	13	12	11	10	9	8
SYSREF_PROC_EN	RESERVED	SYSREF_RECV_SLEEP	RESERVED				SYSREF_POS_SEL
R/W-0h	R/W-0h	R/W-1h	R-0h				R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SYSREF_ZOOM	SYSREF_SEL			
R-0h			R/W-0h	R/W-0h			

表 7-24. SYSREF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SYSREF_PROC_EN	R/W	0h	When set, this bit enables the SYSREF processor. When this is enabled, the system receives and processes each new SYSREF edge. User should always clear SYSREF_RECV_SLEEP before setting this bit. This bit is provided to allow the SYSREF receiver to stabilize before allowing the SYSREF to come to the digital.
14	RESERVED	R/W	0h	
13	SYSREF_RECV_SLEEP	R/W	1h	Clear this bit to enable the SYSREF receiver circuit. User should always clear SYSREF_PROC_EN before setting this bit.
12-9	RESERVED	R	0h	
8	SYSREF_POS_SEL	R/W	0h	Always write 0.
7-6	RESERVED	R	0h	
4	SYSREF_ZOOM	R/W	0h	Set this bit to “zoom” in the SYSREF strobe status (impacts SYSREF_POS and the step size of SYSREF_SEL).
3-0	SYSREF_SEL	R/W	0h	Set this field to select which SYSREF delay to use. Set this based on the results returned by SYSREF_POS.

7.5.2.15 SYSREF_POS Register (Address = 90h) [reset = 0h]

SYSREF_POS is shown in 図 7-39 and described in 表 7-25.

Return to the Summary Table.

SYSREF Capture Position (read-only)

図 7-39. SYSREF_POS Register

15	14	13	12	11	10	9	8
SYSREF_POS							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYSREF_POS							
R-0h							

表 7-25. SYSREF_POS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SYSREF_POS	R	0h	Returns a 16-bit status value that indicates the position of the SYSREF edge with respect to DEVCLK. Use this to determine the proper programming for SYSREF_SEL and SYSREF_ZOOM. For CHIP_VERSION=2, this register can report either an accumulation of all the SYSREF edges seen since SYSREF_PS_EN transitioned from 0 to 1 (infinite persistence) or just the last SYSREF edge (when SYSREF_PS_EN=0). The user should reset the persistence after changing SYSREF_POS_SEL

7.5.2.16 DP_EN Register (Address = 100h) [reset = 00h]

DP_EN is shown in 図 7-40 and described in 表 7-26.

Return to the Summary Table.

Datapath Enable (default: 0x00)

図 7-40. DP_EN Register

7	6	5	4	3	2	1	0
RESERVED							DP_EN
R/W-0h							R/W-0h

表 7-26. DP_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	DP_EN	R/W	0h	Setting this bit enables datapath operation. When cleared, the datapath is held in reset. This bit should be set after the chip is configured for proper operation. Note: This register should only be changed from 0 to 1 when FUSE_DONE=1 and NCO_EN=0.

7.5.2.17 CH_CFG Register (Address = 101h) [reset = 02h]

CH_CFG is shown in 図 7-41 and described in 表 7-27.

Return to the Summary Table.

Channel Configuration (default: 0x02).

Note: This register should only be changed when DP_EN=0.

Note: When neither DAC is using LVDS as the source, LVDS_MODE and DCM_EN are still used to determine the max DACCLK rate. See 表 7-3. Note: Enabling transmission while LVDS_MODE=2 && DCM_EN=1 will result in undefined behavior.

図 7-41. CH_CFG Register

7	6	5	4	3	2	1	0
DACB_SRC		DACA_SRC		RESERVED		LVDS_MODE	
R/W-0h		R/W-0h		R/W-0h		R/W-2h	

表 7-27. CH_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DACB_SRC	R/W	0h	0: Disable (DACB powered down) 1: LVDS 2: NCO 3: SPIDAC
5-4	DACA_SRC	R/W	0h	0: Disable (DACA powered down) 1: LVDS 2: NCO 3: SPIDAC
3-2	RESERVED	R/W	0h	
1-0	LVDS_MODE	R/W	2h	0: 1 bank per DAC 1: 2 banks per DAC 2: 4 banks per DAC 3: RESERVED

7.5.2.18 LVDS_CFG Register (Address = 106h) [reset = 00h]

LVDS_CFG is shown in 図 7-42 and described in 表 7-28.

Return to the Summary Table.

LSB Strobe Control (default: 0x00)

図 7-42. LVDS_CFG Register

7	6	5	4	3	2	1	0
RESERVED	LVDS_RESOLUTION			RESERVED			LSB_SYNC
R/W-0h	R/W-0h			R/W-0h			R/W-0h

表 7-28. LVDS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	LVDS_RESOLUTION	R/W	0h	The value of LVDS_RESOLUTION will determine the operating resolution according to the following table: 0: 12-bit input mode 1: 11-bit input mode 2: 10-bit input mode 3: 9-bit input mode >3: 8-bit input mode
3-1	RESERVED	R/W	0h	
0	LSB_SYNC	R/W	0h	When set, this bit causes the LSB of the LVDS data to be used as SYNC regardless of the state of the sync_n input.

7.5.2.19 LVDS_TERM Register (Address = 107h) [reset = 01h]

LVDS_TERM is shown in 図 7-43 and described in 表 7-29.

Return to the Summary Table.

LVDS Termination Configuration (default: 0x01)

図 7-43. LVDS_TERM Register

7	6	5	4	3	2	1	0
RESERVED							LVDS_TERM
R/W-0h							R/W-1h

表 7-29. LVDS_TERM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	LVDS_TERM	R/W	1h	When set, this bit causes the LVDS inputs to be differentially terminated with 100 Ohms. If this bit isn't set there is no termination resistance between the pairs.

7.5.2.20 DITH_EN Register (Address = 140h) [reset = 00h]

DITH_EN is shown in 図 7-44 and described in 表 7-30.

Return to the Summary Table.

DAC Dither Enable (default: 0x00).

Note: Changes to this register may only be made while TXENABLE (ball or register) for the channels being reconfigured is low.

図 7-44. DITH_EN Register

7	6	5	4	3	2	1	0
RESERVED				DITH_EN_B		DITH_EN_A	
R/W-0h				R/W-0h		R/W-0h	

図 7-44. DITH_EN Register (continued)

表 7-30. DITH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-2	DITH_EN_B	R/W	0h	0: Dither Disabled 1: Use +1 to -2 LSBs of dither 2: Use +3 to -4 LSBs of dither 3: Use +7 to -8 LSBs of dither
1-0	DITH_EN_A	R/W	0h	0: Dither Disabled 1: Use +1 to -2 LSBs of dither 2: Use +3 to -4 LSBs of dither 3: Use +7 to -8 LSBs of dither

7.5.2.21 MXMODE Register (Address = 160h) [reset = 00h]

MXMODE is shown in 図 7-45 and described in 表 7-31.

Note: This register should only be changed when DP_EN=0.

Note: Enabling transmission while DCM_EN=0 && (MXMODE_A=3 || MXMODE_B=3) will result in undefined behavior.

Return to the Summary Table.

DAC Pulse Mode (default: 0x00)

図 7-45. MXMODE Register

7	6	5	4	3	2	1	0
RESERVED		MXMODE_B		RESERVED		MXMODE_A	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 7-31. MXMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	MXMODE_B	R/W	0h	Specify the DAC pulse format for DACB. 0 : Normal mode (non-return-to-zero) (sinc nulls at n*FS) 1 : Mixed Mode (return to inverse) (sinc nulls at DC and 2n*FS) 2 : Return-to-Zero (RTZ) (sinc nulls at 2n*FS) 3 : 2XRF Mode (zero, signal, inverse, zero) – requires DCM_EN=1
3-2	RESERVED	R/W	0h	
1-0	MXMODE_A	R/W	0h	Specify the DAC pulse format for DACA. 0 : Normal mode (non-return-to-zero) (sinc nulls at n*FS) 1 : Mixed Mode (return to inverse) (sinc nulls at DC and 2n*FS) 2 : Return-to-Zero (RTZ) (sinc nulls at 2n*FS) 3 : 2XRF Mode (zero, signal, inverse, zero) – requires DCM_EN=1

7.5.2.22 COARSE_CUR Register (Address = 170h) [reset = 00h]

COARSE_CUR is shown in 図 7-46 and described in 表 7-32.

Return to the Summary Table.

Coarse Current Control (DAC A and B) (default: 0x00)

図 7-46. COARSE_CUR Register

7	6	5	4	3	2	1	0
COARSE_CUR_B				COARSE_CUR_A			
R/W-0h				R/W-0h			

表 7-32. COARSE_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	COARSE_CUR_B	R/W	0h	Coarse current control for DAC B.
3-0	COARSE_CUR_A	R/W	0h	Coarse current control for DAC A.

7.5.2.23 CUR_A Register (Address = 171h) [reset = 9Fh]

CUR_A is shown in 図 7-47 and described in 表 7-33.

Return to the Summary Table.

Current Control for DAC A (default: 0x9f)

図 7-47. CUR_A Register

7	6	5	4	3	2	1	0
CUR_EN_A	RESERVED	FINE_CUR_A					
R/W-1h	R/W-0h	R/W-1Fh					

表 7-33. CUR_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CUR_EN_A	R/W	1h	Current enable for DAC A. If this is disabled, user needs to pulldown their DAC output bias to avoid reliability concerns. Disabling this causes the DAC to lose its DC operating point and will take some time to recover when it is turned on.
6	RESERVED	R/W	0h	
5-0	FINE_CUR_A	R/W	1Fh	Fine current control for DAC A.

7.5.2.24 CUR_B Register (Address = 172h) [reset = 9Fh]

CUR_B is shown in 図 7-48 and described in 表 7-34.

Return to the Summary Table.

Current Control for DAC B (default: 0x9f)

図 7-48. CUR_B Register

7	6	5	4	3	2	1	0
CUR_EN_B	RESERVED	FINE_CUR_B					
R/W-1h	R/W-0h	R/W-1Fh					

表 7-34. CUR_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CUR_EN_B	R/W	1h	Current enable for DAC B. If this is disabled, user needs to pulldown their DAC output bias to avoid reliability concerns. Disabling this causes the DAC to lose its DC operating point and will take some time to recover when it is turned on.
6	RESERVED	R/W	0h	
5-0	FINE_CUR_B	R/W	1Fh	Fine current control for DAC B.

7.5.2.25 SPIDAC_CHG_BLK Register (Address = 180h) [reset = 00h]

SPIDAC_CHG_BLK is shown in 図 7-49 and described in 表 7-35.

Return to the Summary Table.

SPIDAC Change Block (default: 0x00)

図 7-49. SPIDAC_CHG_BLK Register

7	6	5	4	3	2	1	0
RESERVED							SPIDAC_CHG_BLK
R/W-0h							R/W-0h

表 7-35. SPIDAC_CHG_BLK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SPIDAC_CHG_BLK	R/W	0h	When set, changes to the SPIDAC_VALUE are not propagated to the high speed clocks and any DAC configured to use the SPIDAC continues to use its current value. When cleared, the SPIDAC_VALUE is used by the DAC's. The user must set this before changing SPIDAC_VALUE if DP_EN=1.

7.5.2.26 SPIDAC_VALUE Register (Address = 181h) [reset = 0000h]

SPIDAC_VALUE is shown in 図 7-50 and described in 表 7-36.

Return to the Summary Table.

Sample value for SPIDAC Mode (default: 0x0000)

図 7-50. SPIDAC_VALUE Register

15	14	13	12	11	10	9	8
SPIDAC_VALUE							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPIDAC_VALUE							
R/W-0h							

表 7-36. SPIDAC_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SPIDAC_VALUE	R/W	0h	This field defines the constant sample value fed to a DAC configured to use the SPIDAC. Changes to this register are synchronously applied to both DACs. See DACA_SRC and DACB_SRC. This value should only be changed when DP_EN=0 or SPIDAC_CHG_BLK=1. Note: Changes to the value can only propagate to the DAC output when SPIDAC_CHG_BLK is clear.

7.5.2.27 SHUNTREG_EN Register (Address = 1A0h-1A1h) [reset = 0000h]

SHUNTREG_EN is shown in 図 7-51 and described in 表 7-37.

Return to the Summary Table.

Enable Shunt Regulators (default: 0x0000). Recommended setting used in device characterization is 0x0FFF.

図 7-51. SHUNTREG_EN Register

15	14	13	12	11	10	9	8
SHUNTREG_CLKDIST_EN	SHUNTREG_CLKGEN_EN	SHUNTREG_SYSREF_EN	RESERVED	SHUNTREG_MUX_DACB_EN		SHUNTREG_SWDRV_DACB_EN	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

図 7-51. SHUNTREG_EN Register

7	6	5	4	3	2	1	0
SHUNTREG_CLKDRV_DACB_EN		SHUNTREG_MUX_DACA_EN		SHUNTREG_SWDRV_DACA_EN		SHUNTREG_CLKDRV_DACA_EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 7-37. SHUNTREG_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SHUNTREG_CLKDIST_EN	R/W	0h	Enable shunt regulators on SYSREF receiver.
14	SHUNTREG_CLKGEN_EN	R/W	0h	Enable shunt regulators on clock distribution supply.
	SHUNTREG_SYSREF_EN	R/W	0h	Enable shunt regulators on SYSREF receiver.
12	RESERVED	R/W	0h	Reserved.
11:10	SHUNTREG_MUX_DACB_EN	R/W	0h	Enable shunt regulators on the DACB MUX supplies.
9:8	SHUNTREG_SWDRV_DACB_EN	R/W	0h	Enable shunt regulators on the DACB Switch Driver supplies.
7:6	SHUNTREG_CLKDRV_DACB_EN	R/W	0h	Enable shunt regulators on the DACB Clock Driver supplies.
5:4	SHUNTREG_MUX_DACA_EN	R/W	0h	Enable shunt regulators on the DACA MUX supplies.
3:2	SHUNTREG_SWDRV_DACA_EN	R/W	0h	Enable shunt regulators on the DACA Switch Driver supplies.
1:0	SHUNTREG_CLKDRV_DACA_EN	R/W	0h	Enable shunt regulators on the DACA Clock Driver supplies.

7.5.2.28 FIFO_DLY Register (Address = 200h) [reset = 0h]

FIFO_DLY is shown in 図 7-52 and described in 表 7-38.

Return to the Summary Table.

FIFO Delay (default: 0x08)

図 7-52. FIFO_DLY Register

7	6	5	4	3	2	1	0
RESERVED			FIFO_DLY				
R/W-0h			R/W-0h				

表 7-38. FIFO_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	

表 7-38. FIFO_DLY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	FIFO_DLY	R/W	0h	This sets the number of DAC clocks after the effective SYSREF edge before the first samples are expected to be available at the back of the FIFO. Note: Changes to this register should only be made while TXENABLE is low for both DACs. Note: This register should only be changed when NCO_EN=0. This register does affect the NCO alignment with respect to SYSREF. See セクション 7.3.3.5.3.

7.5.2.29 FIFO_DLY_R0 Register (Address = 210h) [reset = 0h]

FIFO_DLY_R0 is shown in 図 7-53 and described in 表 7-39.

Return to the Summary Table.

Current FIFO Delay for FIFO0 (read-only)

図 7-53. FIFO_DLY_R0 Register

7	6	5	4	3	2	1	0
RESERVED			FIFO_DLY_R0				
R-0h			R-0h				

表 7-39. FIFO_DLY_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	FIFO_DLY_R0	R	0h	This reports the approximate setting for FIFO_DLY that would result in sample being used just as it arrives under current conditions. (This is the approximate number of DAC clocks after the effective SYSREF edge when the first sample is available at the back of the FIFO.)

7.5.2.30 FIFO_DLY_R1 Register (Address = 211h) [reset = 0h]

FIFO_DLY_R1 is shown in 図 7-54 and described in 表 7-40.

Return to the Summary Table.

Current FIFO Delay for FIFO1 (read-only)

図 7-54. FIFO_DLY_R1 Register

7	6	5	4	3	2	1	0
RESERVED			FIFO_DLY_R1				
R-0h			R-0h				

表 7-40. FIFO_DLY_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	FIFO_DLY_R1	R	0h	This reports the approximate setting for FIFO_DLY that would result in sample being used just as it arrives under current conditions. (This is the approximate number of DAC clocks after the effective SYSREF edge when the first sample is available at the back of the FIFO minus 1.)

7.5.2.31 FIFO_DLY_R2 Register (Address = 212h) [reset = 0h]

FIFO_DLY_R2 is shown in 図 7-55 and described in 表 7-41.

Return to the Summary Table.

Current FIFO Delay for FIFO2 (read-only)

図 7-55. FIFO_DLY_R2 Register

7	6	5	4	3	2	1	0
RESERVED			FIFO_DLY_R2				
R-0h			R-0h				

表 7-41. FIFO_DLY_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	FIFO_DLY_R2	R	0h	This reports the approximate setting for FIFO_DLY that would result in sample being used just as it arrives under current conditions. (This is the approximate number of DAC clocks after the effective SYSREF edge when the first sample is available at the back of the FIFO minus 2 for LVDS_MODE==0 and minus 0 otherwise.)

7.5.2.32 FIFO_DLY_R3 Register (Address = 213h) [reset = 0h]

FIFO_DLY_R3 is shown in 図 7-56 and described in 表 7-42.

Return to the Summary Table.

Current FIFO Delay for FIFO3 (read-only)

図 7-56. FIFO_DLY_R3 Register

7	6	5	4	3	2	1	0
RESERVED			FIFO_DLY_R3				
R-0h			R-0h				

表 7-42. FIFO_DLY_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	FIFO_DLY_R3	R	0h	This reports the approximate setting for FIFO_DLY that would result in sample being used just as it arrives under current conditions. (This is the approximate number of DAC clocks after the effective SYSREF edge when the first sample is available at the back of the FIFO minus 3 for LVDS_MODE==0 and minus 1 otherwise.)

7.5.2.33 FIFO_ALIGN Register (Address = 220h) [reset = 0h]

FIFO_ALIGN is shown in 図 7-57 and described in 表 7-43.

Return to the Summary Table.

FIFO Alignment Control (default: 0x00)

図 7-57. FIFO_ALIGN Register

7	6	5	4	3	2	1	0
RESERVED						LVDS_STROBE_ALIGN	SYSREF_ALIGN_EN
R/W-0h						R/W-0h	R/W-0h

図 7-57. FIFO_ALIGN Register (continued)

表 7-43. FIFO_ALIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	LVDS_STROBE_ALIGN	R/W	0h	Writing ‘1’ to this register when it is ‘0’ will cause the FIFO to re-align to the LVDS receiver. If LVDS bank 0 is in use, it will be used for alignment. Otherwise, LVDS bank 2 will be used. (Continuous alignment is not performed because the LVDS clock is asynchronous to the DAC clock and may cause realignment each time alignment is performed.) The alignment will cause a CLK_REALIGNED_ALM if realignment occurs. This bit should only be set while DP_EN=1, the DAC data path is zeroed (TXENABLE ball or register is low), and NCO_EN=0. Note: This bit aligns to the current internal operating alignment of the LVDS receiver circuitry. Alignment does not wait for an actual strobe to be provided on the LVDS bank and can be performed even if a strobe is not currently being provided. However, it is important that an LVDS strobe be provided to align the LVDS receiver prior to aligning the FIFO with this bit. Note: Once the system has been synchronized to SYSREF, this bit cannot be used again until the part has been reset or DP_EN has been returned to zero.
0	SYSREF_ALIGN_EN	R/W	0h	When this register is set, the FIFO re-aligns to each detected SYSREF edge. This bit should only be high while DP_EN=1, transmit_en_a=0, transmit_en_b=0, and NCO_EN=0. When a mis-aligned SYSREF edge occurs while this bit is set, CLK_REALIGNED_ALM will be set and the clocks will re-align. When this register is clear, the FIFO does not re-align on SYSREF edges. However, mis-aligned SYSREF edges are still reported in CLK_ALIGNMENT_ALM. Note: It is possible that a SYSREF edge provided very near the SPI clock edge that commits the write of this bit will be processed for alignment even though it technically arrived at the chip pins prior to the SPI clock edge.

7.5.2.34 NCO_SYNC Register (Address = 300h) [reset = 00h]

NCO_SYNC is shown in 図 7-58 and described in 表 7-44.

Return to the Summary Table.

NCO Sync Source Select (default: 0x00)

Note: This register should only be changed when NCO_EN=0.

Note: You cannot use the same SYSREF edge to align the FIFO and to sync the NCO since FIFO alignment requires NCO_EN=0.

図 7-58. NCO_SYNC Register

7	6	5	4	3	2	1	0
RESERVED		NCO_CHG_SRC_B	NCO_CHG_SRC_A	RESERVED		NCO_SYNC_SRC	
R/W-0h		R/W-0h	R/W-0h	R/W-0h		R/W-0h	

表 7-44. NCO_SYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	

表 7-44. NCO_SYNC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	NCO_CHG_SRC_B	R/W	0h	0: NCO B will use the NCO accumulator specified in NCO_SEL_B. 1: NCO B accumulator selection is performed using the nco_sel[3:0] and nco_banksel inputs and occurs on the rising edge of trig_c. Note: If nco_sel[3:0] and nco_banksel are not changed synchronous to trig_c, the part may temporarily switch to an unintended accumulator before switching to the correct one.
4	NCO_CHG_SRC_A	R/W	0h	0: NCO A will use the NCO accumulator specified in NCO_SEL_A. 1: NCO A selection is performed using the nco_sel[3:0] and nco_banksel inputs and occurs on the rising edge of trig_c. Note: If nco_sel[3:0] and nco_banksel are not changed synchronous to trig_c, the part may temporarily switch to an unintended NCO before switching to the correct one.
3-2	RESERVED	R/W	0h	
1-0	NCO_SYNC_SRC	R/W	0h	0: Setting SPI_SYNC will immediately reset the NCO accumulators (both A & B) 1: Setting SPI_SYNC will cause the NCO accumulators to reset on the next SYSREF rising edge. 2: Setting SPI_SYNC will cause the NCO accumulators to reset on the next rising edge of trig_c with nco_banksel = 1. 3: RESERVED

7.5.2.35 NCO_SPISEL Register (Address = 301h) [reset = 0000h]

NCO_SPISEL is shown in 図 7-59 and described in 表 7-45.

Note: This register should only be changed when NCO_EN=0 or NCO_CHG_BLK=1.

Return to the Summary Table.

NCO Fast-Frequency Hopping Frequency Selection (default: 0x0000)

図 7-59. NCO_SPISEL Register

15	14	13	12	11	10	9	8
RESERVED			NCO_SEL_B				
R/W-0h			R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			NCO_SEL_A				
R/W-0h			R/W-0h				

表 7-45. NCO_SPISEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12-8	NCO_SEL_B	R/W	0h	Selects which frequency/phase values to use for NCO B if NCO_CHG_SRC_B = 0. The MSB here selects which NCO bank to use. (0=A, 1=B)
7-5	RESERVED	R/W	0h	
4-0	NCO_SEL_A	R/W	0h	Selects which frequency/phase values to use for NCO A if NCO_CHG_SRC_A = 0. The MSB here selects which NCO bank to use. (0=A, 1=B)

7.5.2.36 NCO_BANKCFG Register (Address = 303h) [reset = 00h]

NCO_BANKCFG is shown in 図 7-60 and described in 表 7-46.

Note: This register should only be changed when NCO_EN=0 or NCO_CHG_BLK=1.

Return to the Summary Table.

NCO Bank Configuration (default: 0x00)

図 7-60. NCO_BANKCFG Register

7	6	5	4	3	2	1	0
RESERVED						NCO_BANKCFG	
R/W-0h						R/W-0h	

表 7-46. NCO_BANKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	NCO_BANKCFG	R/W	0h	0: The value of nco_sel[3:0] sampled on trig_c selects the respective A and B channel NCO accumulator. 1: The value of nco_sel[3:0] sampled on trig_c selects the same NCO accumulator for both A and B channels based on the value of nco_banksel (0=A, 1=B). This makes it look like there are 32 NCO accumulators and nco_banksel is the MSB of nco_sel. 2: The value of nco_sel[3:0] sampled on trig_c changes only the accumulator for the NCO selected by nco_banksel. (0=A, 1=B). Only one of the two NCO's can change per trig_c in this mode. In this case, nco_banksel is more like an NCO select. 3: RESERVED NOTE: This register should only be changed when NCO_EN=0.

7.5.2.37 NCO_EN Register (Address = 308h) [reset = 00h]

NCO_EN is shown in 図 7-61 and described in 表 7-47.

Return to the Summary Table.

NCO Enable (default: 0x00)

図 7-61. NCO_EN Register

7	6	5	4	3	2	1	0
RESERVED							NCO_EN
R/W-0h							R/W-0h

表 7-47. NCO_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	NCO_EN	R/W	0h	Setting this bit enables NCO operation. When this bit is cleared, the entire NCO is held in reset. This bit should be set after the NCO operation is configured and DP_EN=1.

7.5.2.38 SPI_SYNC Register (Address = 310h) [reset = 00h]

SPI_SYNC is shown in 図 7-62 and described in 表 7-48.

Return to the Summary Table.

SPI Sync (default: 0x00)

図 7-62. SPI_SYNC Register

7	6	5	4	3	2	1	0
RESERVED							SPI_SYNC
R/W-0h							R/W-0h

図 7-62. SPI_SYNC Register (continued)

表 7-48. SPI_SYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SPI_SYNC	R/W	0h	Writing ‘1’ to this register when it is ‘0’ will trigger synchronization events that are bound to this register (see NCO_SYNC_SRC). This register will return the last value written.

7.5.2.39 NCO_CHG_BLK Register (Address = 320h) [reset = 00h]

NCO_CHG_BLK is shown in 図 7-63 and described in 表 7-49.

Return to the Summary Table.

NCO Change Blocking (default: 0x00)

図 7-63. NCO_CHG_BLK Register

7	6	5	4	3	2	1	0
RESERVED							NCO_CHG_BLK
R/W-0h							R/W-0h

表 7-49. NCO_CHG_BLK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	NCO_CHG_BLK	R/W	0h	When set, changes to NCO_SEL_A, NCO_SEL_B, FFH_FREQ_A, FFH_FREQ_B, FFH_PHASE_A, and FFH_PHASE_B, are not propagated to the high speed clocks and the NCOs continue to use their current values. When cleared, the NCO’s use the values from these registers. The user must set this if changing any of these values while NCO_EN=1. Note: Phase continuous operation is only supported from FFH_FREQ_A[0] and FFH_FREQ_B[0]. Note: Changing frequency values during operation only makes sense if phase coherency is unimportant since the user cannot control when the frequency change will take effect.

7.5.2.40 NCO_RAMPRATE Register (Address = 330h) [reset = 00h]

NCO_RAMPRATE is shown in 図 7-64 and described in 表 7-50.

Note: If NCO_MODE=1 and both DACs use the NCO source and transmit_en_a != transmit_en_b, the rampup/ rampdown behavior is undefined.

Return to the Summary Table.

NCO Ramp Rate Control (default: 0x00)

図 7-64. NCO_RAMPRATE Register

7	6	5	4	3	2	1	0
RESERVED					NCO_RAMPRATE		
R/W-0h					R/W-0h		

表 7-50. NCO_RAMPRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	

表 7-50. NCO_RAMPRATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	NCO_RAMPRATE	R/W	0h	Each of the NCO sources is linearly ramped up/down over the specified number of DEVCLK cycles when transmission is enabled/ disabled. 0: 0 DEVCLK cycles 1: 16 DEVCLK cycles 2: 32 DEVCLK cycles 3: 64 DEVCLK cycles 4: 128 DEVCLK cycles 5: 256 DEVCLK cycles 6: 512 DEVCLK cycles 7: 1024 DEVCLK cycles Note: This register should only be changed when TXENABLE (ball or register) is low.

7.5.2.41 NCO_CONFIG Register (Address = 331h) [reset = 02h]

NCO_CONFIG is shown in 図 7-65 and described in 表 7-51.

Note: This register should only be changed when TXENABLE (ball or register) is low.

Return to the Summary Table.

NCO Configuration (default: 0x02)

図 7-65. NCO_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED						NCO_DITH_EN	NCO_MODE
R/W-0h						R/W-1h	R/W-0h

表 7-51. NCO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	NCO_DITH_EN	R/W	1h	Setting this bit causes the NCO to use sub-LSB dither prior to rounding to smooth out the quantization noise. It may be useful to turn this off for certain frequencies where the quantization error is not a concern.
0	NCO_MODE	R/W	0h	0: NCOs operate independently 1: NCOs are summed to create the final NCO output. If both DACA and DACB use the NCO source, they will both get the summed value in this mode.

7.5.2.42 NCO_GAIN_A Register (Address = 332h) [reset = 0003h]

NCO_GAIN_A is shown in 図 7-66 and described in 表 7-52.

Return to the Summary Table.

Gain backoff for NCO A (default: 0x0003)

図 7-66. NCO_GAIN_A Register

15	14	13	12	11	10	9	8
NCO_GAIN_A							
R/W-3h							
7	6	5	4	3	2	1	0
NCO_GAIN_A							
R/W-3h							

図 7-66. NCO_GAIN_A Register (continued)

表 7-52. NCO_GAIN_A Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_GAIN_A	R/W	3h	This setting is the gain backoff for NCO A. This backoff is applied independent of NCO_MODE. The gain is equal to 1-(x/2^{16}). Note: Setting DITH_EN_A>0 automatically reduces the gain to prevent clipping from the NCO. The value programmed here is added to the required backoff for dither. The final gain will saturate at zero. Note: Setting this value below the default will result in saturation for some frequencies. Note: This register should only be changed when NCO_EN=0.

7.5.2.43 NCO_GAIN_B Register (Address = 334h) [reset = 0003h]

NCO_GAIN_B is shown in 図 7-67 and described in 表 7-53.

Return to the Summary Table.

Gain backoff for NCO B (default: 0x0003)

図 7-67. NCO_GAIN_B Register

15	14	13	12	11	10	9	8
NCO_GAIN_B							
R/W-3h							
7	6	5	4	3	2	1	0
NCO_GAIN_B							
R/W-3h							

表 7-53. NCO_GAIN_B Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_GAIN_B	R/W	3h	This setting is the gain backoff for NCO B. This backoff is applied independent of NCO_MODE. The gain is equal to 1-(x/2^{16}). Note: Setting DITH_EN_B>0 automatically reduces the gain to prevent clipping from the NCO. The value programmed here is added to the required backoff for dither. The final gain will saturate at zero. Note: Setting this value below the default will result in saturation for some frequencies. Note: This register should only be changed when NCO_EN=0.

7.5.2.44 FFH_FREQ_A[15:0] Register (Address = 400h) [reset = 0h]

FFH_FREQ_A[15:0] is shown in 図 7-68 and described in 表 7-54.

Return to the Summary Table.

Frequency Word for Fast-Frequency Hopping (default: {16{0x00000000}}). The FFH setting for NCO_SEL_A=0 will be at the lowest address, and then increment by 4*n for NCO_SEL_A = n.

図 7-68. FFH_FREQ_A[15:0] Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFH_FREQ_A																															
R/W-0h																															

表 7-54. FFH_FREQ_A[15:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FFH_FREQ_A	R/W	0h	The NCO frequency (F_{NCO}) is: F_{NCO} = FREQ_A * 2^{-32} * F_{DAC} F_{DAC} is the sample frequency of the DAC. FREQ_A is the integer value of this register. This register can be interpreted as signed or unsigned (both interpretations are valid). Use this equation to determine the value to program: FREQ_A = 2^{32} * F_{NCO} /F_{DAC} Note: Changing this register after the NCO has been synchronized will result in non-deterministic NCO phase. If deterministic phase is required, the NCO should be re-synchronized after changing this register. Note: This register should only be changed when NCO_EN=0 or NCO_CHG_BLK=1.

7.5.2.45 FFH_FREQ_B[15:0] Register (Address = 440h) [reset = 0h]

FFH_FREQ_B[15:0] is shown in 図 7-69 and described in 表 7-55.

Return to the Summary Table.

Frequency Word for Fast-Frequency Hopping (default: {16{0x00000000}}). The FFH setting for NCO_SEL_B=0 will be at the lowest address, and then increment by 4*n for NCO_SEL_B = n.

図 7-69. FFH_FREQ_B[15:0] Register

31-0
FFH_FREQ_B
R/W-0h

表 7-55. FFH_FREQ_B[15:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FFH_FREQ_B	R/W	0h	The NCO frequency (F_{NCO}) is: F_{NCO} = FREQ_B * 2^{-32} * F_{DAC} F_{DAC} is the sample frequency of the DAC. FREQ_B is the integer value of this register. This register can be interpreted as signed or unsigned (both interpretations are valid). Use this equation to determine the value to program: FREQ_B = 2^{32} * F_{NCO} /F_{DAC} Note: Changing this register after the NCO has been synchronized will result in non-deterministic NCO phase. If deterministic phase is required, the NCO should be re-synchronized after changing this register. Note: This register should only be changed when NCO_EN=0 or NCO_CHG_BLK=1.

7.5.2.46 FFH_PHASE_A[15:0] Register (Address = 480h) [reset = 0h]

FFH_PHASE_A[15:0] is shown in 図 7-70 and described in 表 7-56.

Return to the Summary Table.

Phase Word for Fast-Frequency Hopping (default: {16{0x0000}}). The FFH setting for NCO_SEL_A=0 will be at the lowest address, and then increment by 2*n for NCO_SEL_A = n.

図 7-70. FFH_PHASE_A[15:0] Register

15	14	13	12	11	10	9	8
FFH_PHASE_A							
R/W-0h							

図 7-70. FFH_PHASE_A[15:0] Register (continued)

7	6	5	4	3	2	1	0
FFH_PHASE_A							
R/W-0h							

表 7-56. FFH_PHASE_A[15:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FFH_PHASE_A	R/W	0h	Phase is added late so this register can be written during operation to change the phase without needing to reset the NCO. This value is left justified into a 32−bit field and then added to the phase accumulator. The phase (in radians) is PHASE_A * 2^{-16} * 2π. This register can be interpreted as signed or unsigned. Note: This register should only be changed when NCO_EN=0 or NCO_CHG_BLK=1.

7.5.2.47 FFH_PHASE_B[15:0] Register (Address = 4A0h) [reset = 0h]

FFH_PHASE_B[15:0] is shown in 図 7-71 and described in 表 7-57.

Return to the Summary Table.

Phase Word for Fast-Frequency Hopping (default: {16{0x0000}}). The FFH setting for NCO_SEL_B=0 will be at the lowest address, and then increment by 2*n for NCO_SEL_B = n.

図 7-71. FFH_PHASE_B[15:0] Register

15	14	13	12	11	10	9	8
FFH_PHASE_B							
R/W-0h							
7	6	5	4	3	2	1	0
FFH_PHASE_B							
R/W-0h							

表 7-57. FFH_PHASE_B[15:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FFH_PHASE_B	R/W	0h	Phase is added late so this register can be written during operation to change the phase without needing to reset the NCO. This value is left justified into a 32−bit field and then added to the phase accumulator. The phase (in radians) is PHASE_B * 2^{-16} * 2π. This register can be interpreted as signed or unsigned. Note: This register should only be changed when NCO_EN=0 or NCO_CHG_BLK=1.

7.5.2.48 TS_TEMP Register (Address = 700h) [reset = 0h]

TS_TEMP is shown in 図 7-72 and described in 表 7-58.

Return to the Summary Table.

Temperature Reading in Celsius (read-only)

図 7-72. TS_TEMP Register

7	6	5	4	3	2	1	0
TS_TEMP							
R-0h							

表 7-58. TS_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TS_TEMP	R	0h	Returns the temperature sensor reading in degrees Celsius. This is a signed value. Note: Reads of this register require slower SPI timing. See AC-Spec -> SPI Interface. Note: The temperature sensor cannot perform a reading unless SLEEP=0, MODE=0 and TS_SLEEP=0.

7.5.2.49 TS_SLEEP Register (Address = 701h) [reset = 00h]

TS_SLEEP is shown in 図 7-73 and described in 表 7-59.

Return to the Summary Table.

Temperature Sensor Sleep (default: 0x00)

図 7-73. TS_SLEEP Register

7	6	5	4	3	2	1	0
RESERVED							TS_SLEEP
R/W-0h							R/W-0h

表 7-59. TS_SLEEP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	TS_SLEEP	R/W	0h	If temperature conversions are not needed, set this bit to sleep the temperature sensor.

7.5.2.50 IOTEST_CFG Register (Address = 710h) [reset = 00h]

IOTEST_CFG is shown in 図 7-74 and described in 表 7-60.

Return to the Summary Table.

IOTEST Configuration (default: 0x00)

図 7-74. IOTEST_CFG Register

7	6	5	4	3	2	1	0
IOTEST_EN[3:0]				RESERVED		IOTEST_STRB_LOCK	IOTEST_CONT
R/W-0h				R/W-0h		R/W-0h	R/W-0h

表 7-60. IOTEST_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IOTEST_EN[3:0]	R/W	0h	When set, IOTEST_EN[i] enables IO testing for LVDS bank i (assuming that the LVDS bank is currently configured for operation). Note: When any bit of this register is set, no LVDS data is passed through to the output of the DAC.
3-2	RESERVED	R/W	0h	
1	IOTEST_STRB_LOCK	R/W	0h	Setting this bit prevents the LVDS strobe from re-aligning the LVDS counters. (It does not prevent the strobe alignment alarms.) Use this to allow a pattern on the strobe pin that is different from the normal strobe pattern.

表 7-60. IOTEST_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IOTEST_CONT	R/W	0h	0: IOTEST will stop when the first error is detected 1: IOTEST will run until manually stopped

7.5.2.51 IOTEST_CTRL Register (Address = 711h) [reset = 00h]

IOTEST_CTRL is shown in 図 7-75 and described in 表 7-61.

Return to the Summary Table.

IOTEST Control (default: 0x00)

図 7-75. IOTEST_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							IOTEST_TRIG
R/W-0h							R/W-0h

表 7-61. IOTEST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	IOTEST_TRIG	R/W	0h	Writing ‘1’ to this register when it is ‘0’ will start the IOTEST at the beginning of the next frame and clear the IOTEST_STAT* registers. Writing ‘0’ to this register will stop the IOTEST if it is running. If this register is ‘1’, use IOTEST_RUN to see if the test is actually running or has been stopped due to a captured failure.

7.5.2.52 IOTEST_SUM Register (Address = 712h) [reset = 0h]

IOTEST_SUM is shown in 図 7-76 and described in 表 7-62.

Return to the Summary Table.

IOTEST Status (read-only)

図 7-76. IOTEST_SUM Register

7	6	5	4	3	2	1	0
IOTEST_RUN[3:0]				IOTEST_MISS3_SUM	IOTEST_MISS2_SUM	IOTEST_MISS1_SUM	IOTEST_MISS0_SUM
R-0h				R-0h	R-0h	R-0h	R-0h

表 7-62. IOTEST_SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IOTEST_RUN[3:0]	R	0h	IOTEST_RUN[i] will be set any time the IOTEST is running on LVDS bank i.
3	IOTEST_MISS3_SUM	R	0h	This bit will be set any time a failure is reported in IOTEST_MISS3. This bit is cleared by clearing the failures in IOTEST_MISS3.
2	IOTEST_MISS2_SUM	R	0h	This bit will be set any time a failure is reported in IOTEST_MISS2. This bit is cleared by clearing the failures in IOTEST_MISS2.
1	IOTEST_MISS1_SUM	R	0h	This bit will be set any time a failure is reported in IOTEST_MISS1. This bit is cleared by clearing the failures in IOTEST_MISS1.
0	IOTEST_MISS0_SUM	R	0h	This bit will be set any time a failure is reported in IOTEST_MISS0. This bit is cleared by clearing the failures in IOTEST_MISS0.

7.5.2.53 IOTEST_PAT[7:0] Register (Address = 720h) [reset = 0h]

IOTEST_PAT[7:0] is shown in 図 7-77 and described in 表 7-63.

Return to the Summary Table.

IOTEST Pattern Memory (default: {8{0x0000}}).

This is the 8-word pattern memory containing the 16-bit words for the LVDS IOTEST. The first sample of the frame should be at the lowest address.

Each of the 8 words has this format:

図 7-77. IOTEST_PAT[7:0] Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_DATA[12:8]				
R/W-0h			R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOTEST_DATA[7:0]							
R/W-0h							

表 7-63. IOTEST_PAT[7:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12-0	IOTEST_DATA	R/W	0h	[12]: Defines the expected state of the strobe pin. [11:0]: Defines the expected state of the data pins. Note: The falling edge data for the strobe pin should always be set to zero.

7.5.2.54 IOTEST_STAT0 Register (Address = 750h) [W1C, reset = NA]

IOTEST_STAT0 is shown in 図 7-78 and described in 表 7-64.

Return to the Summary Table.

IOTEST Bank0 Failure Status

図 7-78. IOTEST_STAT0 Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_MISS0[12:8]				
R/W-0h			W1C				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOTEST_MISS0[7:0]							
W1C							

表 7-64. IOTEST_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12-0	IOTEST_MISS0	W1C	NA	[12]: Failure on strobe pin [11:0]: Failure on indicated data pin

7.5.2.55 IOTEST_STAT1 Register (Address = 752h) [W1C, reset = NA]

IOTEST_STAT1 is shown in 図 7-79 and described in 表 7-65.

Return to the Summary Table.

IOTEST Bank1 Failure Status

図 7-79. IOTEST_STAT1 Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_MISS1[12:8]				
R/W-0h			W1C				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOTEST_MISS1[7:0]							
W1C							

表 7-65. IOTEST_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12-0	IOTEST_MISS1	W1C	NA	[12]: Failure on strobe pin [11:0]: Failure on indicated data pin

7.5.2.56 IOTEST_STAT2 Register (Address = 754h) [W1C, reset = NA]

IOTEST_STAT2 is shown in 図 7-80 and described in 表 7-66.

Return to the Summary Table.

IOTEST Bank2 Failure Status (write-to-clear)

図 7-80. IOTEST_STAT2 Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_MISS2[12:8]				
R/W-0h			W1C				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOTEST_MISS2[7:0]							
W1C							

表 7-66. IOTEST_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12-0	IOTEST_MISS2	W1C	NA	[12]: Failure on strobe pin [11:0]: Failure on indicated data pin

7.5.2.57 IOTEST_STAT3 Register (Address = 756h) [reset = 0h]

IOTEST_STAT3 is shown in 図 7-81 and described in 表 7-67.

Return to the Summary Table.

IOTEST Bank3 Failure Status (write-to-clear)

図 7-81. IOTEST_STAT3 Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_MISS3[12:8]				
R/W-0h			W1C				

図 7-81. IOTEST_STAT3 Register (continued)

7	6	5	4	3	2	1	0
IOTEST_MISS3[7:0]							
W1C							

表 7-67. IOTEST_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12-0	IOTEST_MISS3	W1C	NA	[12]: Failure on strobe pin [11:0]: Failure on indicated data pin

7.5.2.58 IOTEST_CAP0[7:0] Register (Address = 760h) [read only, reset = NA]

IOTEST_CAP0[7:0] is shown in 図 7-82 and described in 表 7-68.

Return to the Summary Table.

IOTEST Bank0 Capture Memory (read-only)

This is the 8-word capture memory containing the 13-bit captured words from the bank. If the test was run with IOTEST_CONT = 0 and IOTEST_MISS0 != 0, this memory will contain the captured frame with the error. Since it contains the entire frame, more than one error may be present. The first sample of the frame will be at the lowest address.

Note: The capture memory should only be read while IOTEST_RUN[0] = 0.

図 7-82. IOTEST_CAP0[7:0] Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_CAP_DATA[12:8]				
R-0h			R-0h				
7	6	5	4	3	2	1	0
IOTEST_CAP_DATA[7:0]							
R-0h							

表 7-68. IOTEST_CAP0[7:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	
12-0	IOTEST_CAP_DATA	R	0h	[12]: Captured data for strobe pin [11:0]: Captured data for indicated data pin

7.5.2.59 IOTEST_CAP1[7:0] Register (Address = 770h) [reset = 0h]

IOTEST_CAP1[7:0] is shown in 図 7-83 and described in 表 7-69.

Return to the Summary Table.

IOTEST Bank1 Capture Memory (read-only)

This is the 8-word capture memory containing the 13-bit captured words from the bank. If the test was run with IOTEST_CONT = 0 and IOTEST_MISS0 != 0, this memory will contain the captured frame with the error. Since it contains the entire frame, more than one error may be present. The first sample of the frame will be at the lowest address.

Note: The capture memory should only be read while IOTEST_RUN[1] = 0.

図 7-83. IOTEST_CAP1[7:0] Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_CAP_DATA[12:8]				
R-0h			R-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOTEST_CAP_DATA[7:0]							
R-0h							

表 7-69. IOTEST_CAP1[7:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	
12-0	IOTEST_CAP_DATA	R	0h	[12]: Captured data for strobe pin [11:0]: Captured data for indicated data pin

7.5.2.60 IOTEST_CAP2[7:0] Register (Address = 780h) [reset = 0h]

IOTEST_CAP2[7:0] is shown in 図 7-84 and described in 表 7-70.

Return to the Summary Table.

IOTEST Bank2 Capture Memory (read-only)

This is the 8-word capture memory containing the 13-bit captured words from the bank. If the test was run with IOTEST_CONT = 0 and IOTEST_MISS2 != 0, this memory will contain the captured frame with the error. Since it contains the entire frame, more than one error may be present. The first sample of the frame will be at the lowest address.

Note: The capture memory should only be read while IOTEST_RUN[2] = 0.

図 7-84. IOTEST_CAP2[7:0] Register

15	14	13	12	11	10	9	8
RESERVED			IOTEST_CAP_DATA[12:8]				
R-0h			R-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOTEST_CAP_DATA[7:0]							
R-0h							

表 7-70. IOTEST_CAP2[7:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	
12-0	IOTEST_CAP_DATA	R	0h	[12]: Captured data for strobe pin [11:0]: Captured data for indicated data pin

7.5.2.61 IOTEST_CAP3[7:0] Register (Address = 790h) [reset = 0h]

IOTEST_CAP3[7:0] is shown in 図 7-85 and described in 表 7-71.

Return to the Summary Table.

IOTEST Bank3 Capture Memory (read-only)

This is the 8-word capture memory containing the 13-bit captured words from the bank. If the test was run with IOTEST_CONT = 0 and IOTEST_MISS3 != 0, this memory will contain the captured frame with the error. Since it contains the entire frame, more than one error may be present. The first sample of the frame will be at the lowest address.

Note: The capture memory should only be read while IOTEST_RUN[3] = 0.

図 7-85. IOTEST_CAP3[7:0] Register

15	14	13	12	11	10	9	8
RESERVED			:	:			
R-0h			R-0h	R-0h			
7	6	5	4	3	2	1	0
IOTEST_CAP_DATA[7:0]							
R-0h							

表 7-71. IOTEST_CAP3[7:0] Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	
12-0	IOTEST_CAP_DATA	R	0h	[12]: Captured data for strobe pin [11:0]: Captured data for indicated data pin

7.5.2.62 SYNC_STATUS Register (Address = 800h) [W1C, reset = NA]

SYNC_STATUS is shown in 図 7-86 and described in 表 7-72.

Return to the Summary Table.

Synchronization Status (default: 0x00)

図 7-86. SYNC_STATUS Register

7	6	5	4	3	2	1	0
LVDS_STROBE_DET[3:0]				RESERVED			SYSREF_DET
W1C				R/W-0h			W1C

表 7-72. SYNC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LVDS_STROBE_DET[3:0]	W1C	NA	[i]: Bit is set when a strobe is detected for LVDS bank i. Write 1 to clear the bit and allow it to be re-detected. These bits are also cleared on the rising edge of LVDS_STROBE_ALIGN.
3-1	RESERVED	R/W	0h	
0	SYSREF_DET	W1C	NA	This bit is set when a SYSREF is detected. Write 1 to clear the bit and allow it to be re-detected. This bit is also cleared on the rising edge of SYSREF_ALIGN_EN.

7.5.2.63 FIFO_ALM Register (Address = 820h) [W1C, reset = NA]

FIFO_ALM is shown in 図 7-87 and described in 表 7-73.

Note: These registers will only detect alarms on input data transitions. Constant input data will not produce alarms.

Return to the Summary Table.

FIFO Alarm Status (default: 0x00)

図 7-87. FIFO_ALM Register

7	6	5	4	3	2	1	0

図 7-87. FIFO_ALM Register (continued)

FIFO_EMPTY_ALM	FIFO_FULL_ALM
W1C	W1C

表 7-73. FIFO_ALM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FIFO_EMPTY_ALM	W1C	0h	FIFO_EMPTY_ALM[i] is set if the FIFO for bank i is almost empty. FIFOs that are not enabled will never generate an alarm. Write 1 to a bit to clear the alarm.
3-0	FIFO_FULL_ALM	W1C	0h	FIFO_FULL_ALM[i] is set if the FIFO for bank i is almost full. FIFOs that are not enabled will never generate an alarm. Write 1 to a bit to clear the alarm.

7.5.2.64 LVDS_ALM Register (Address = 821h) [W1C, reset = NA]

LVDS_ALM is shown in 図 7-88 and described in 表 7-74.

Return to the Summary Table.

LVDS Strobe Alarm (default: 0x00)

図 7-88. LVDS_ALM Register

7	6	5	4	3	2	1	0
LVDS_CLK_ALM				STROBE_ALM			
W1C				W1C			

表 7-74. LVDS_ALM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LVDS_CLK_ALM	W1C	0h	LVDS_CLK_ALM[i] is set if the respective LVDS bank is configured for use and the LVDS clock is not running. The LVDS clock must miss at least half of its edges within 8 LVDS periods to ensure detection. Write 1 to a bit to clear the alarm.
3-0	STROBE_ALM	W1C	0h	STROBE_ALM[i] is set if the strobe for LVDS bank i arrives at an unexpected position. Unless IOTEST_STRB_LOCK was set when the error occured, this has caused the input side of the FIFO to re-align. Write 1 to a bit to clear the alarm.

7.5.2.65 SYS_ALM Register (Address = 822h) [W1C, reset = NA]

SYS_ALM is shown in 図 7-89 and described in 表 7-75.

Return to the Summary Table.

System Alarm Status (default: 0x00)

図 7-89. SYS_ALM Register

7	6	5	4	3	2	1	0
RESERVED					TRIG_REALIGNED_ALM	CLK_ALIGNMENT_ALM	CLK_REALIGNED_ALM
R/W-0h					W1C	W1C	W1C

表 7-75. SYS_ALM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	

表 7-75. SYS_ALM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TRIG_REALIGNED_ALM	W1C	NA	This bit is set if SYSREF re-aligns the trigger clock divider. This generally occurs if the SYSREF period is not correct. The SYSREF period must be an integer multiple of the Trigger Clock period. This is not intended to detect small changes in SYSREF alignment. The CLK_ALIGNMENT_ALM should be used for this purpose. Write 1 to clear the alarm.
1	CLK_ALIGNMENT_ALM	W1C	NA	This bit is set if SYSREF_ALIGN_EN=0, and a SYSREF edge is detected at an incorrect alignment. Write 1 to clear the alarm.
0	CLK_REALIGNED_ALM	W1C	NA	This bit is set if a detected SYSREF edge or LVDS strobe re-aligns the clocks. Write 1 to clear the alarm.

7.5.2.66 ALM_MASK Register (Address = 823h) [reset = 00h]

ALM_MASK is shown in 図 7-90 and described in 表 7-76.

Return to the Summary Table.

Alarm Mask (default: 0x00)

図 7-90. ALM_MASK Register

7	6	5	4	3	2	1	0
FIFO_ALM_MASK	LVDS_CLK_ALM_MASK	STROBE_ALM_MASK	RESERVED		TRIG_REALIGNED_ALM_MASK	CLK_ALIGNMENT_ALM_MASK	CLK_REALIGNED_ALM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0b	R/W-0b

表 7-76. ALM_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIFO_ALM_MASK	R/W	0h	When set, alarms from the FIFO_ALM registers are masked and will not impact the alarm output.
6	LVDS_CLK_ALM_MASK	R/W	0h	When set, alarms from the LVDS_CLK_ALM registers are masked and will not impact the alarm output.
5	STROBE_ALM_MASK	R/W	0h	When set, alarms from the STROBE_ALM registers are masked and will not impact the alarm output.
4-3	RESERVED	R/W	0h	
2	TRIG_REALIGNED_ALM_MASK	R/W	0b	When set, alarms from the TRIG_REALIGNED_ALM register are masked and will not impact the alarm output.
1	CLK_ALIGNMENT_ALM_MASK	R/W	0b	When set, alarms from the CLK_ALIGNMENT_ALM register are masked and will not impact the alarm output.
0	CLK_REALIGNED_ALM_MASK	R/W	0b	When set, alarms from the CLK_REALIGNED_ALM register are masked and will not impact the alarm output.

7.5.2.67 MUTE_MASK Register (Address = 824h) [reset = 07h]

MUTE_MASK is shown in 図 7-91 and described in 表 7-77.

Return to the Summary Table.

DAC Mute Mask (default: 0x07)

図 7-91. MUTE_MASK Register

7	6	5	4	3	2	1	0
FIFO_MUTE_MASK	LVDS_CLK_MUTE_MASK	STROBE_MUTE_MASK	RESERVED		TRIG_REALIGNED_MUTE_MASK	CLK_ALIGNMENT_MUTE_MASK	CLK_REALIGNED_MUTE_MASK

図 7-91. MUTE_MASK Register (continued)

R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1b	R/W-1b	R/W-1b

表 7-77. MUTE_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIFO_MUTE_MASK	R/W	0h	Alarms from the FIFO_ALM registers will mute the DAC unless this bit is set.
6	LVDS_CLK_MUTE_MASK	R/W	0h	Alarms from the LVDS_CLK_ALM registers will mute the DAC unless this bit is set.
5	STROBE_MUTE_MASK	R/W	0h	Alarms from the STROBE_ALM registers will mute the DAC unless this bit is set.
4-3	RESERVED	R/W	0h	
2	TRIG_REALIGNED_MUTE_MASK	R/W	1b	Alarms from the TRIG_REALIGNED_ALM register will mute the DAC unless this bit is set.
1	CLK_ALIGNMENT_MUTE_MASK	R/W	1b	Alarms from the CLK_ALIGNMENT_ALM register will mute the DAC unless this bit is set.
0	CLK_REALIGNED_MUTE_MASK		1b	Alarms from the CLK_REALIGNED_ALM register will mute the DAC unless this bit is set.

7.5.2.68 FUSE_STATUS Register (Address = 900h) [reset = 00h]

FUSE_STATUS is shown in 図 7-92 and described in 表 7-78.

Return to the Summary Table.

Fuse Status (default: variable)

図 7-92. FUSE_STATUS Register

7	6	5	4	3	2	1	0
RESERVED							FUSE_DONE
R-00h							R-0b

表 7-78. FUSE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	01h	RESERVED
FUSE_DONE	Fuse Done	R	0b	Returns '1' when the fuse controller has finished loading registers from the FuseROM.

7.5.2.69 SYSREF_PS_EN Register (Address = B02h) [reset = 0x00]

SYSREF_PS_EN is shown in 図 7-93 and described in 表 7-79. This function is only available for CHIP_VERSION=2.

Return to the Summary Table.

SYSREF_PS_EN (default: 0x00)

図 7-93. SYSREF_PS_EN Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED - always write 0x0				SYSREF_PS_EN
R/W-0h			R/W-0h				R/W-0b

表 7-79. SYSREF_PS_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000b	RESERVED
4-1	RESERVED	R/W	0x0	RESERVED - always write 0x0
0	SYSREF_PS_EN	R/W	0	When set, SYSREF_POS will contain 1's for all positions that have been detected as near the SYSREF edge since this bit was set. When cleared, SYSREF_POS will only contain 1's for the last SYSREF edge that was detected.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Startup Procedure with LVDS Input

The list below is the startup procedure when using the LVDS input:

1. Start the DEVCLK
2. Apply power per the order in the power sequence section
3. Assert Reset
4. De-assert Reset – Fuse ROM load will automatically begin
5. Program part configuration (CH_CFG , DCM_EN , MXMODE_*, etc.)
6. Wait for Fuse ROM load to complete (FUSE_DONE =1)
7. Apply LVDS signals (and SYSREF if used) to inputs. This may have been done at any earlier point if desired, but must be stable by here.
8. Set DP_EN =1
9. Clear LVDS_CLK_ALM & STROBE_ALM
10. Synchronize the system
    a. If using LVDS Strobes for alignment:
        i. Set LVDS_STROBE_ALIGN =1
        ii. Wait for LVDS_STROBE_DET =1
    b. If using SYSREF for alignment:
        i. See SYSREF Windowing to enable and align synchronous SYSREF capturing.
        ii. Set SYSREF_ALIGN_EN =1
        iii. Wait for SYSREF_DET =1
        iv. Set SYSREF_ALIGN_EN =0
11. Configure FIFO_DLY (this may be done early but should be complete by here)
12. Clear all SYS_ALM bits
13. Wait for 100 DACCLK cycles for corrupted data to be flushed.
14. Enable Transmission using the $\overline{\text{TXENABLE}}$ pin or TXEN_A/B registers.

8.1.2 Startup Procedure With NCO Operation

The following list is the startup procedure in NCO only mode:

1. Start the DEVCLK
2. Apply power
3. Assert Reset
4. De-assert Reset – Fuse ROM load will automatically begin
5. Program part configuration (CH_CFG , DCM_EN , MXMODE_* , etc.) including the desired NCO configuration. Programming frequency and phase settings does not require using NCO_CHG_BLK as long as NCO_EN =0.
6. Wait for Fuse ROM load to complete (FUSE_DONE =1)
7. Apply SYSREF (if used) to inputs. This may have been done at any earlier point if desired, but must be stable by here.
8. Set DP_EN
9. If using LVDS inputs, clear LVDS_CLK_ALM & STROBE_ALM
10. Synchronize the system

   a. If using LVDS Strobes for alignment:
      i. Set LVDS_STROBE_ALIGN
      ii. Wait for LVDS_STROBE_DET =1
   b. If using SYSREF for alignment
      i. See SYSREF Windowing to enable and align synchronous SYSREF capturing.
      ii. Set SYSREF_ALIGN_EN
      iii. Wait for SYSREF_DET =1
      iv. Clear SYSREF_ALIGN_EN
11. If using only the NCO, it is possible to continue without synchronization if no synchronization is desired.
12. Configure FIFO_DLY (this may be done early but should be complete by here)
13. Set NCO_EN
14. Synchronize the NCO accumulators using the method selected in NCO_SYNC_SRC .
15. Clear all SYS_ALM bits
16. Wait for 100 DACCLK cycles for corrupted data to be flushed.
17. Enable Transmission using the $\overline{\text{TXENABLE}}$ pin or TXEN_A/B registers.

When operating only the NCO (no LVDS), the part will automatically run at some unknown alignment without aligning to SYSREF. If SYSREF alignment is desired, the user should align to SYSREF before setting NCO_EN = 1.

8.1.3 Interface Test Pattern and Timing Verification

The device provides the ability for the user to provide a repeating 8-sample sequence on the LVDS inputs and verify that the data can be properly received. It also provides debug facilities to help the user determine where the failures are occurring.

The test can be run both stop-on-fail (which allows the user to read the failing data frame to see what bits are failing and at what point in the pattern) or continue-on-fail (which allows the user to get a quick overview of which datalines are having problems).

Individual LVDS banks can be masked allowing the user to capture failures on selected banks.

1. Start the DEVCLK
2. Apply power
3. Assert Reset
4. De-assert Reset – Fuse ROM load will automatically begin
5. Configure CH_CFG and DCM_EN according to the desired mode of operation. Only LVDS banks that are used in the selected mode will be tested.
6. Start LVDS data into the part using the proper strobe period. Note that it is possible to use either the LSB strobe or the dedicated strobe pin. If using the LSB strobe, set SYNCB low (using either the pin or the register bit).
7. Set DP_EN=1
8. Synchronize the system
    a. If using LVDS Strobes for alignment:
        i. Set LVDS_STROBE_ALIGN=1
        ii. Wait for LVDS_STROBE_DET=1
    b. If using SYSREF for alignment
        i. See SYSREF Windowing to enable and align synchronous SYSREF capturing.
        ii. Set SYSREF_ALIGN_EN=1
        iii. Wait for SYSREF_DET=1
        iv. Set SYSREF_ALIGN_EN=0
9. Check LVDS_STROBE_DET to ensure all the required LVDS strobes have been detected. Be sure to reset the bits before reading them. (Note that it is still possible to run the IOTEST if some strobes are not working. To do this, ensure that SYSREF is not being used so the FIFO does not corrupt the data. Then continue performing the test. The test will likely fail, but will provide visibility into what is occurring on the strobe line.)
10. Configure FIFO_DLY (this may be done early but should be complete by here)
11. Configure the IOTEST data patterns in IOTEST_PAT, and IOTEST_CONT.
12. Set IOTEST_STRB_LOCK=1 (if desired).
13. If using an LSB strobe and the pattern tests the LSb in data operation, set LSB_SYNC=0 and sync_n=1.
14. Set IOTEST_EN=1
15. Enable Transmission using txenable or TXEN_A/B.
16. Start the test using IOTEST_TRIG.
17. If IOTEST_CONT = 0, monitor IOTEST_RUN until the test stops and then inspect the results. If IOTEST_CONT = 1, monitor the faults using IOTEST_SUM or IOTEST_MISS* fields in registers IOTEST_STAT0 - IOTEST_STAT3.

8.2 Typical Application

The DAC12DL3200 can be used in a wide range of applications including radar, electronic warfare, satellite communications, test equipment (communications testers and arbitrary waveform generators) and software-defined radios (SDRs).

The low latency of the DAC12DL3200, in combination with the low latency ADC12DL3200, make it particularly suitable for electronic warfare applications where a fast return of the pulse is important to as closely match the reflected pulse in time. 図 8-1 shows a block diagram for an electronic warfare digital radio. The received radio pulse (after amplification) is input to the ADC12DL3200, the digital signal transferred to the FPGA for digital signal processing (for example frequency or delay shifting), and output by the DAC12DL3200 at the same frequency as the input to the ADC. The DAC and ADC are clocked by the LMK04828.

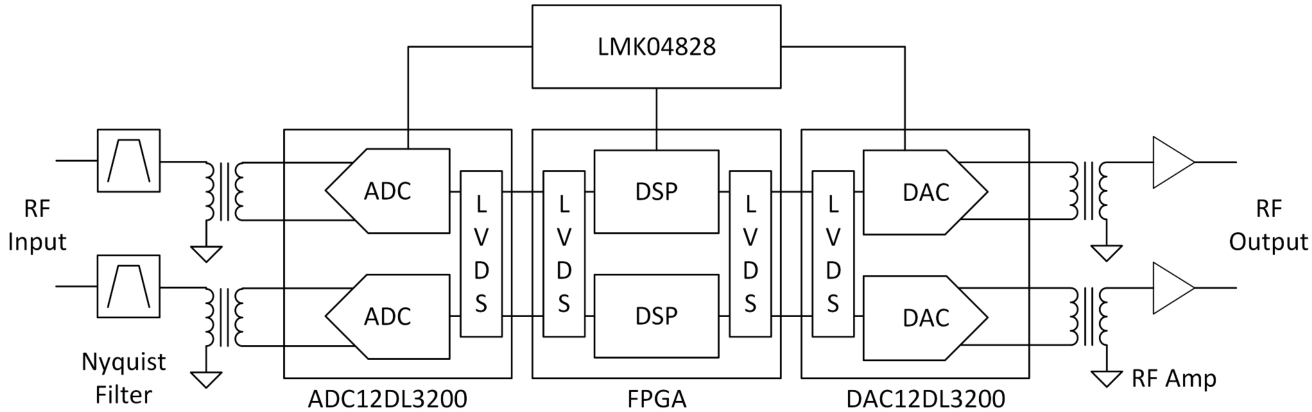


図 8-1. System Block Diagram for a Electronics Warfare Digital Radio

8.2.1 Design Requirements

The system parameters for an example low latency digital radio is listed in 表 8-1.

表 8-1. Digital Radio System Parameters

Function	Value
# of Channels	2
RF Frequency	2.0 - 2.8 GHz
ADC/DAC sample rate	3.2 GSPS
ADC/DAC clock frequency	3.2 GHz
DAC Output Mode	RF Mode
Total Latency (analog input to analog output)	< 50 ns

8.2.2 Detailed Design Procedure

The design operates in 2nd Nyquist zone for the DAC and ADC with a sample rate of 3.2 GSPS (3.2 GHz clock). The DAC is used in RF mode to enhance 2nd Nyquist zone output power. A frequency range of 2.0 to 2.8 GHz is reasonable for design of the Nyquist filter at the ADC input.

The ADC and DAC use the same LMK04828 clock source, which is important for cancellation of the clock phase noise between the ADC input and DAC output. A Xilinx XCKU060 Kintex® UltraScale™ FPGA is used for the FPGA to loopback data from the ADC12DL3200 to DAC12DL3200. No signal processing is included in the FPGA firmware, as that is beyond the scope of this example.

8.2.3 Application Curves

A linear frequency chirp signal with 200 MHz BW, 146.5 MHz/µs and 1.36 µs repetition rate centered at 2.4 GHz was input to the ADC12DL3200. Analog input signal is shown in 図 8-2. The signal after loopback at the DAC12DL3200 output is shown in 図 8-3, and matches well the analog input.

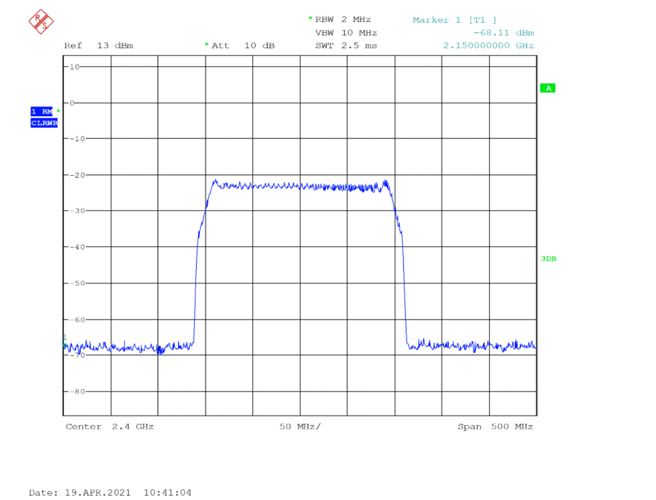


図 8-2. RF Signal at ADC Input

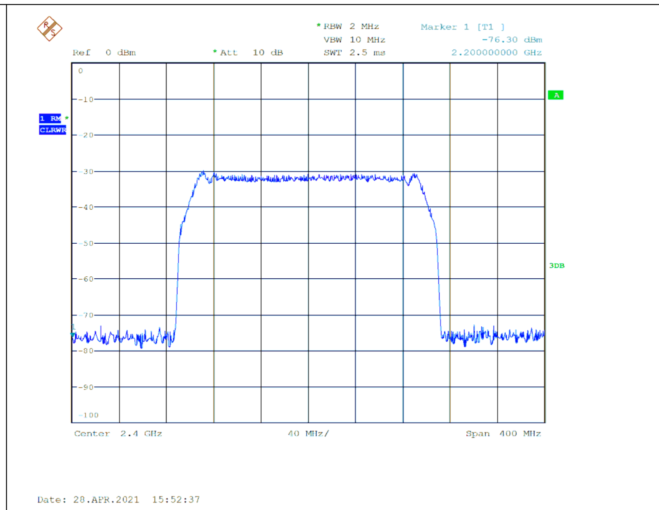


図 8-3. RF Signal at DAC Output

The DAC12DL3200 and ADC12DL3200 latency depend on mode and are 30.5 clock cycles for the DAC and 26 clock cyles for the ADC. At 3.2 GHz, one clock period is 313 ps and therefore the total DAC and ADC latency is 17.7 ns. The latency through the FPGA depends on the FPGA firmware. With significant optimization, a latency of < 20 ns (without signal processing) is possible. To demonstrate an optimized latency, the ADC MSB output was looped back to the DAC MSB input with an latency optimized FPGA firmware. 図 8-4 shows the ADC input to DAC output, with a latency of 32.6 ns, meeting the system design requirement.

図 8-4. ADC Input to DAC Output Time for MSB loopback test.

8.3 Power Supply Recommendations

The device requires three different power-supply voltages. 1.8 VDC is required for the VDDA18A, VDDA18B, VDDCLK18, VDDIO, and VDDSYS18 power buses, 1.0 VDC is required for the VDDCLK10, VDDDIG, VDDEA, VDDEB, VDDHAF, VDDL2A and VDDL2B power buses and -1.8 VDC is required for the VEEAM18 and VEEBM18 power buses.

The recommended power-supply architecture uses high-efficiency switching converters to step down the voltage from a higher rail, followed by a second stage of regulation to provide switching noise reduction and improved voltage accuracy.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS82084 and similar devices.

Recommended low dropout (LDO) linear regulators include the TPS7A91 and similar devices.

Recommended dual positive and negative low dropout (LDO) linear regulator with an integral charge pump include the LM27762 and similar devices.

The switcher output should use a filter designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Make a note of the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed.

Do not share VDDDIG with the analog supply voltages in order to prevent digital switching noise from coupling into the analog signal chain. If some supplies are shared, apply careful power supply filtering to limit digital noise at the analog supply pins.

Several power buses can be combined to use a common regulator when using some type of isolation.

8.3.1 Power Up and Down Sequence

At power up and down, the supplies (including the VOUTA+/- and VOUTB+/- bias voltages) can be applied in any order as long as the cumulative time in a state where only some supplies are active is less than one year.

8.4 Layout

8.4.1 Layout Guidelines

There are many critical signals that require specific care during board design:

1. Analog output signals
2. CLK and SYSREF
3. LVDS data inputs at up to 1.6 Gbps
4. Power connections
5. Ground connections

Items 1 and 2 must be routed for excellent signal quality at high frequencies. Use the following general practices for these signals:

1. Route using loosely coupled 100-Ω differential traces. This routing minimizes impact of corners and length matching serpentines on pair impedance.
2. Provide adequate pair-to-pair spacing to minimize crosstalk.
3. Provide adequate ground plane pour spacing to minimize coupling with the high-speed traces.
4. Use smoothly radiused corners. Avoid 45- or 90-degree bends.
5. Incorporate ground plane cutouts at component landing pads to avoid impedance discontinuities at these locations. Cutout below the landing pads on one or multiple ground planes to achieve a pad size or stackup height that achieves the needed 50-Ω, single-ended impedance.
6. Avoid routing traces near irregularities in the reference ground planes. Irregularities include ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie vias adjacent to any high-speed signal vias.
8. When high-speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top or bottom of the vias. If layer selection is not flexible, use back-drilled or buried, blind vias to eliminate stubs.

The LVDS data inputs must be routed with sufficient signal quality using the following general practices:

1. Route using tightly coupled 100-Ω differential traces to minimize the routing area and decrease crosstalk between adjacent data pairs.
2. Use smoothly radiused corners or 45-degree bends. Avoid 90-degree bends.
3. Avoid routing traces near irregularities in the reference ground planes. Irregularities include ground plane clearances associated with power and signal vias and through-hole component leads.
4. Provide symmetrically located ground tie vias adjacent to any high-speed signal vias.
5. Data, clock, and strobe pairs must be sufficiently delay matched to provide adequate timing margin at the receiver. If routing on multiple layers, trace lengths must be compensated for the delay mismatch introduced by the effective dielectric constant of each layer.

In addition, TI recommends performing signal quality simulations of the critical signal traces before committing to fabrication. Perform insertion loss, return loss, and time domain reflectometry (TDR) evaluations. The power and ground connections for the device are also very important. These rules must be followed:

1. Provide low-resistance connection paths to all power and ground pins.
2. Use multiple power layers if necessary to access all pins.
3. Avoid narrow isolated paths that increase connection resistance.
4. Use a signal, ground, or power circuit board stackup to maximum coupling between the ground and power planes.

8.4.2 Layout Example

図 8-5 through 図 8-8 provide examples of the critical traces routed on the device evaluation module (EVM).

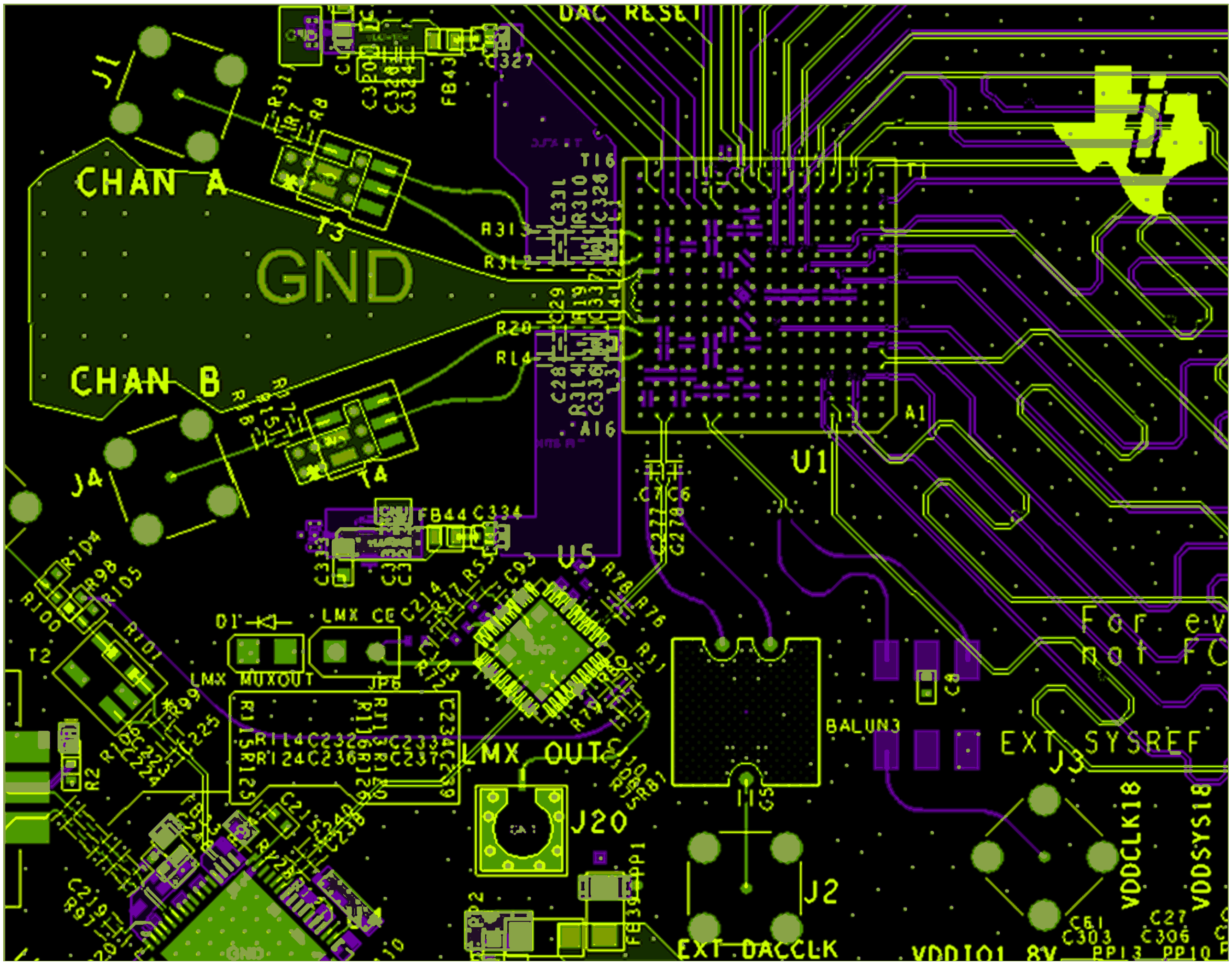


図 8-5. Top (green traces) and Bottom (purple traces) Routing of DAC CLK and SYSREF

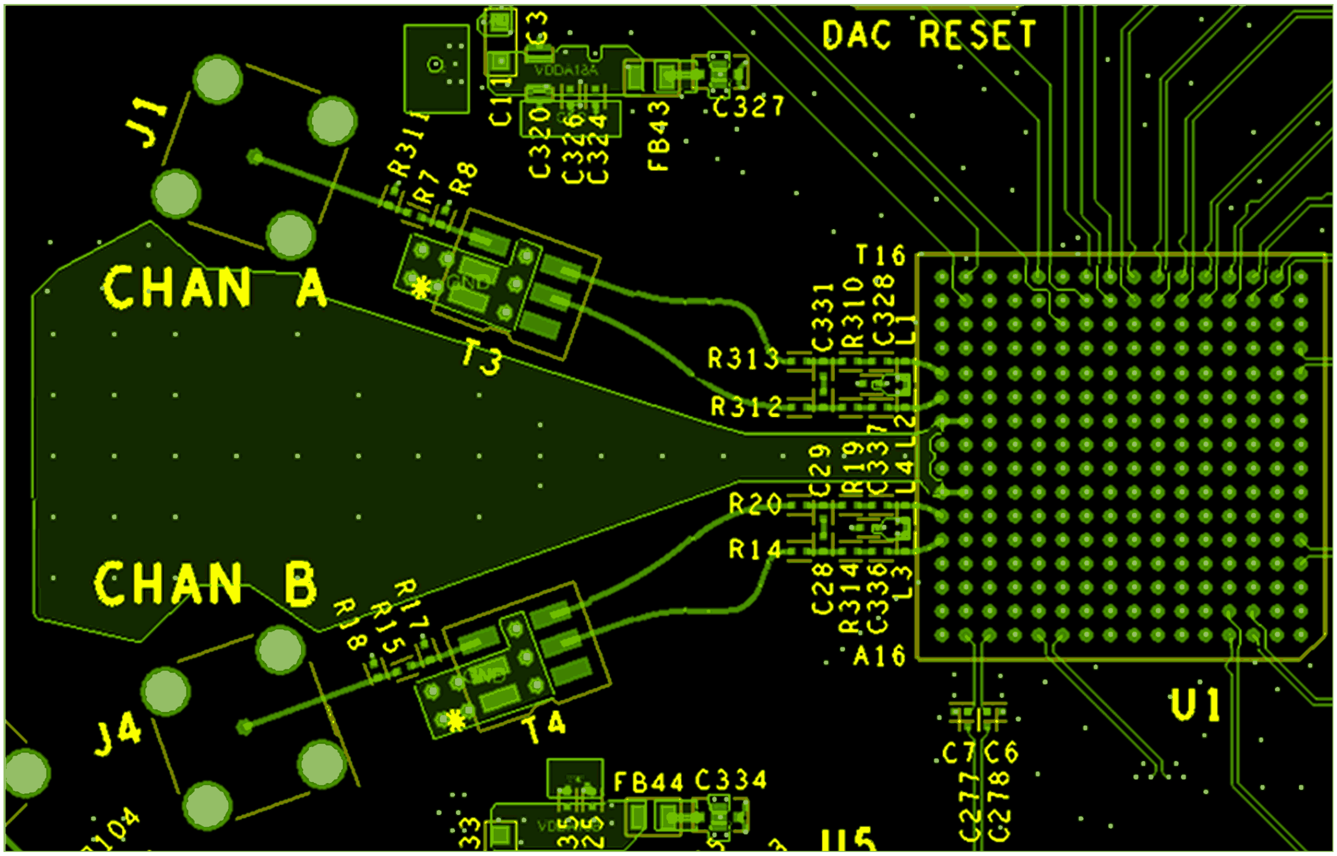


図 8-6. DAC Output Channels Routed on Top Layer

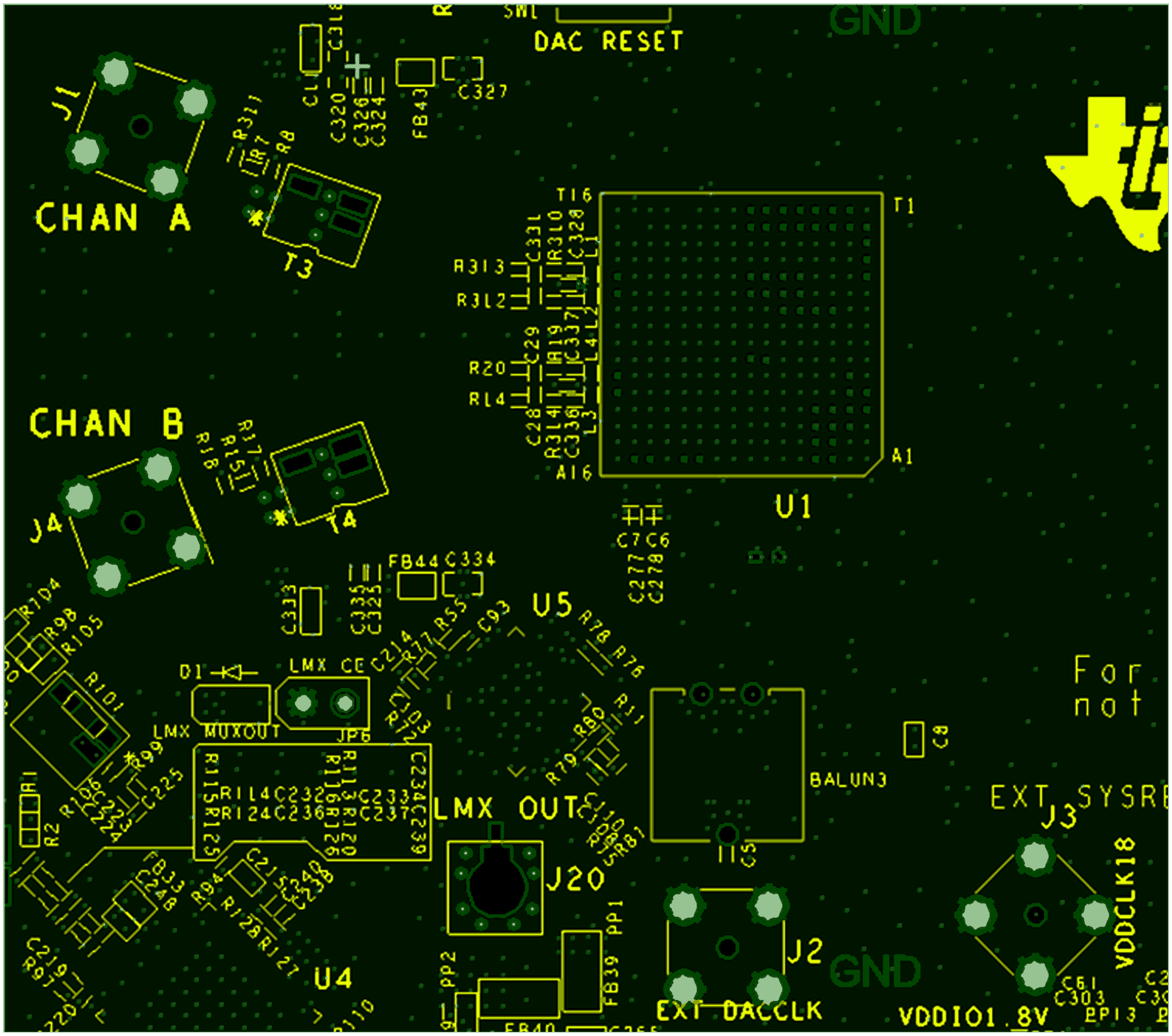


図 8-7. PCB cutouts under output transformers T3 and T4 on layers 2 thru 5.

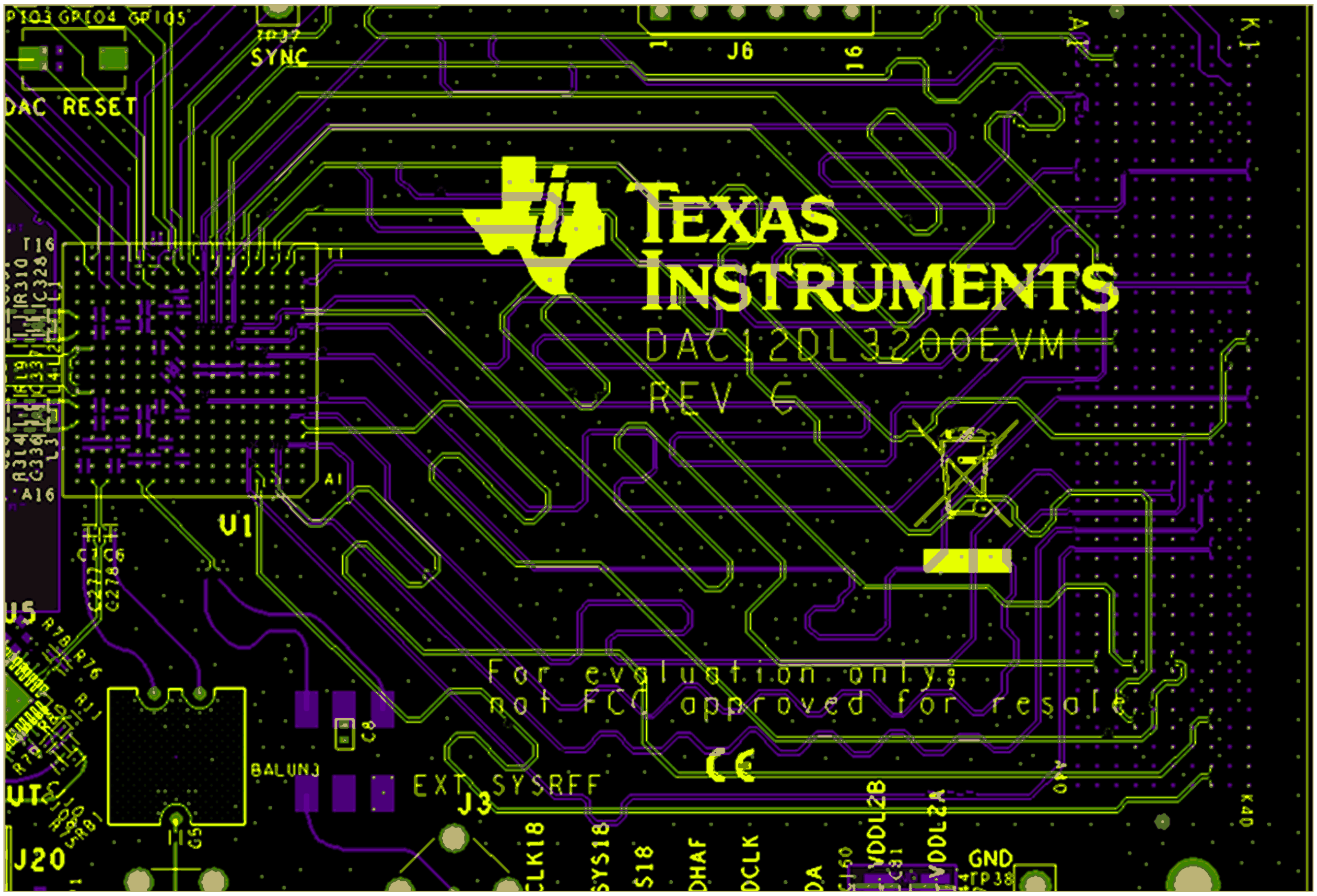


図 8-8. LVDS input data routing on top and bottom layers

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

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TI E2E™ is a trademark of Texas Instruments.
Kintex® is a registered trademark of Xilinx.
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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC12DL3200ACF	Active	Production	FCBGA (ACF) | 256	90 | JEDEC TRAY (5+1)	-	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC12DL32
DAC12DL3200ALJ	Active	Production	FCBGA (ALJ) | 256	90 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 85	DAC12DL32 PB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

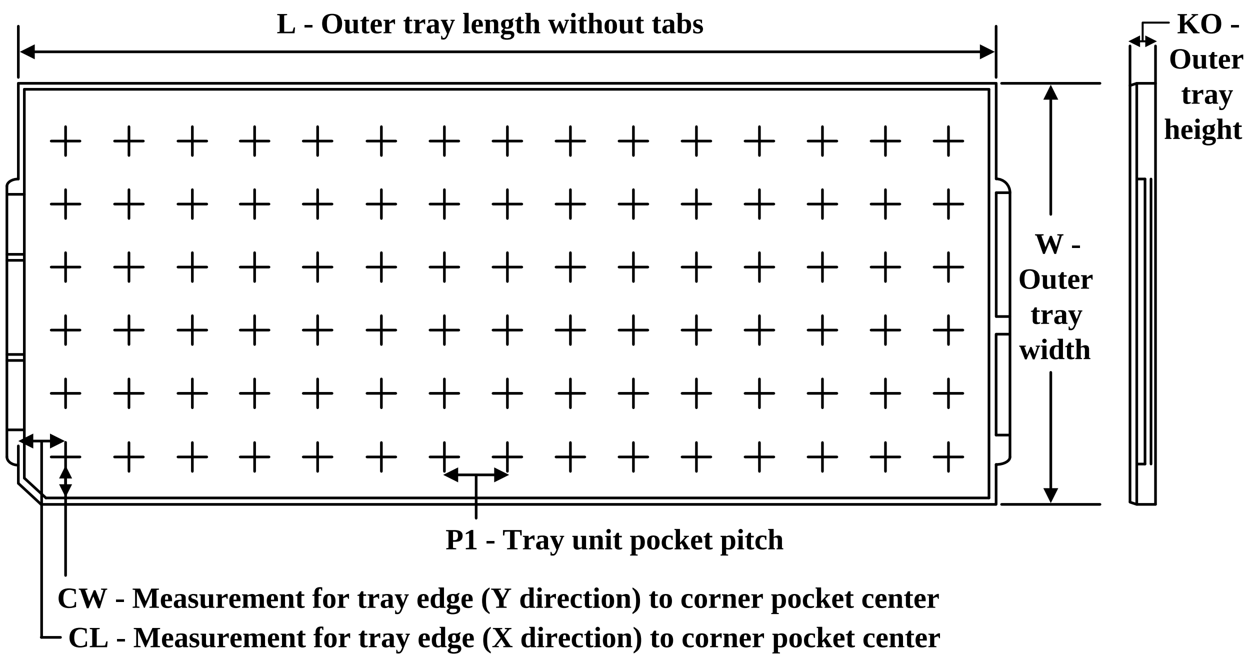
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

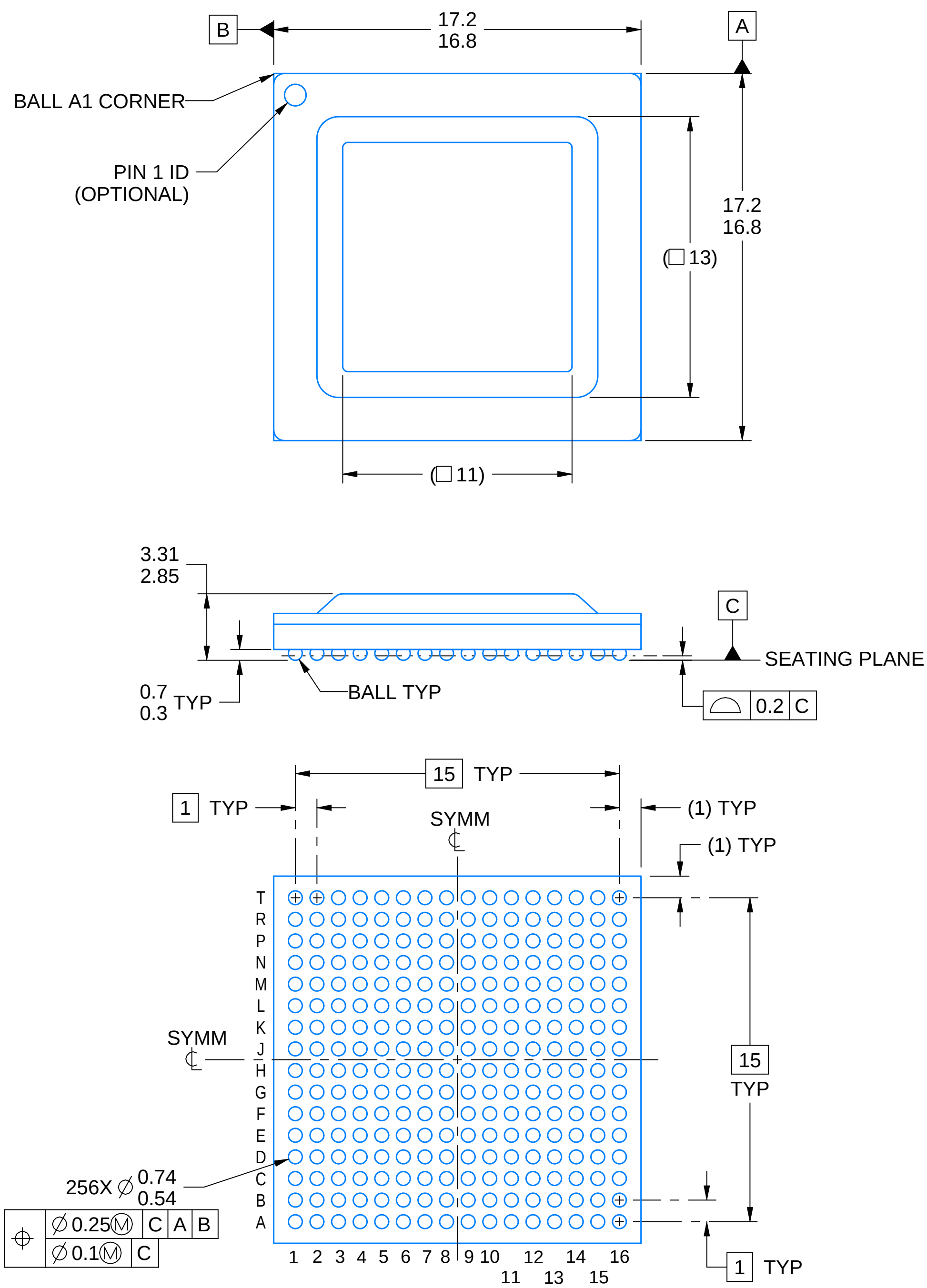
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

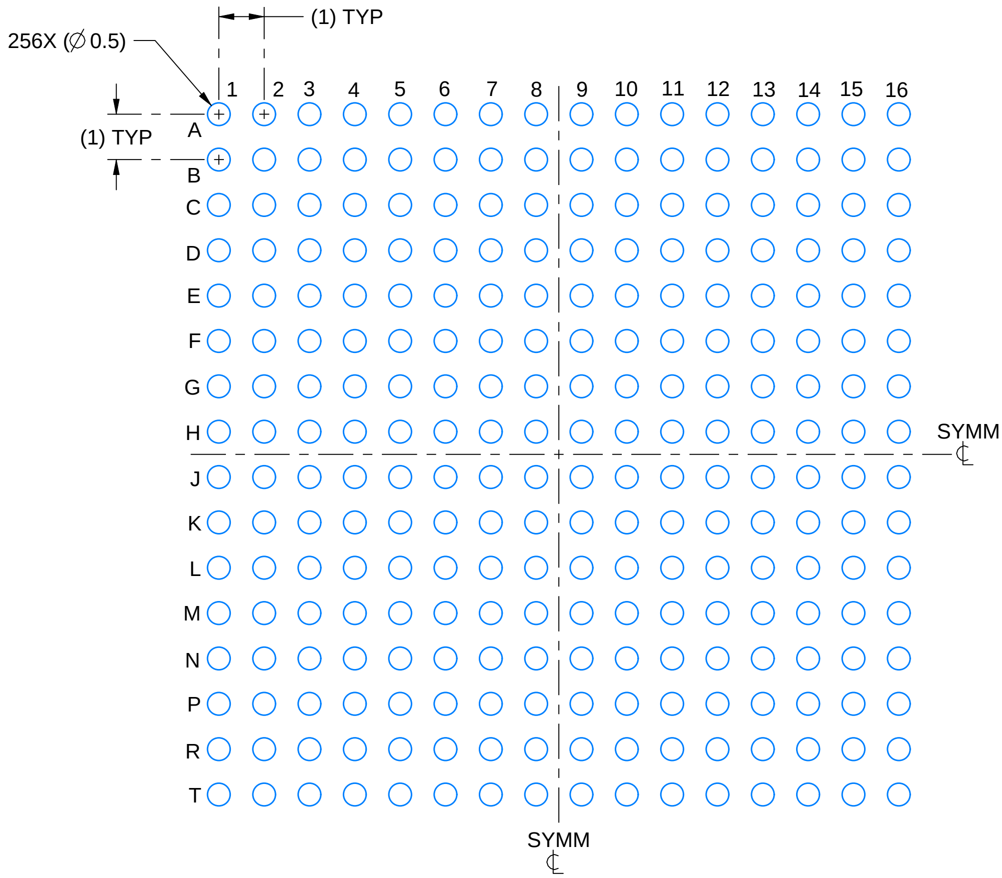
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC12DL3200ACF	ACF	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
DAC12DL3200ALJ	ALJ	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2



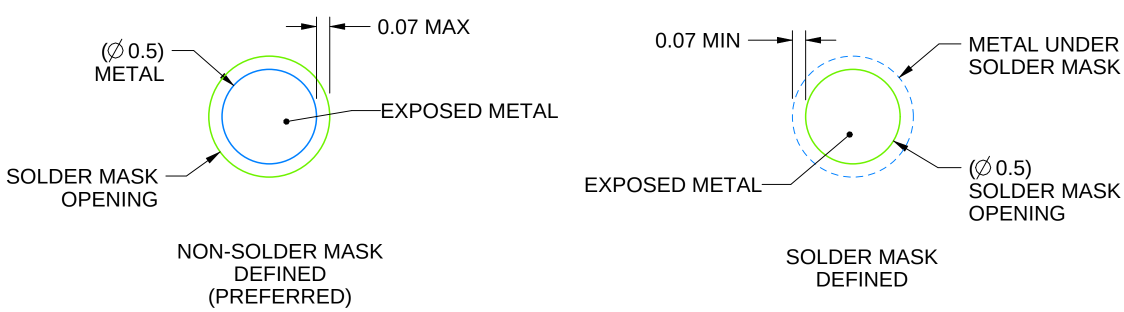
4225401/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SNOWN
SCALE:6X

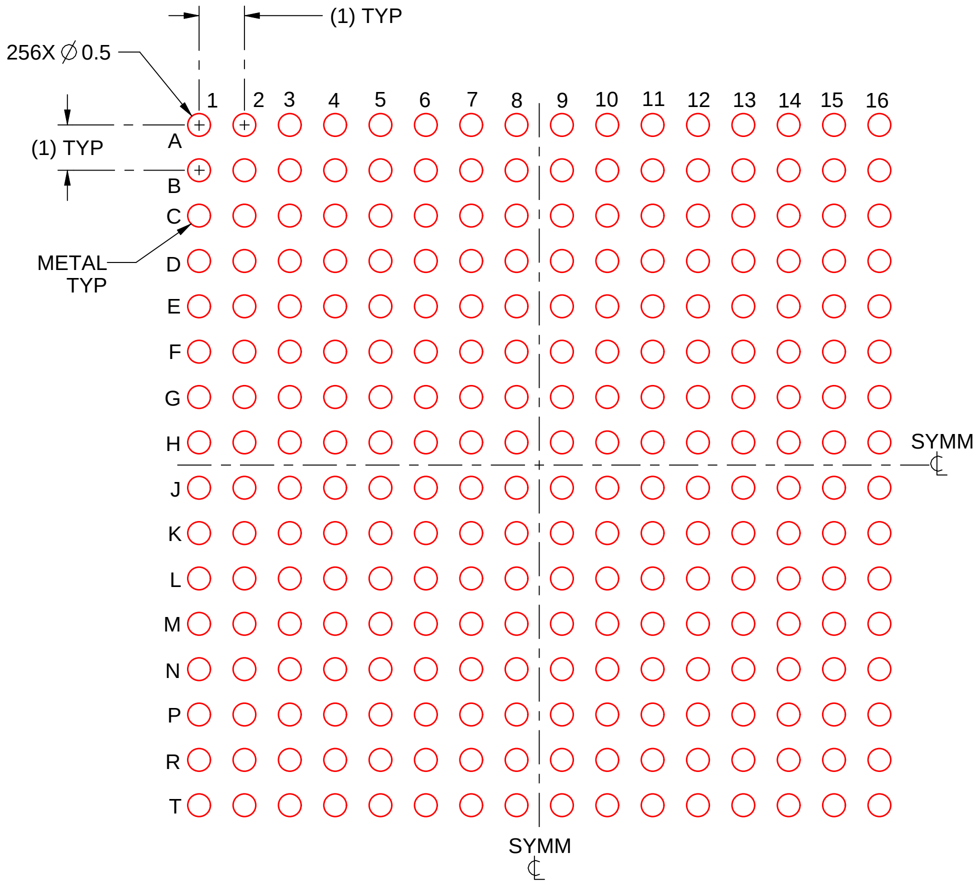


SOLDER MASK DETAILS
NOT TO SCALE

4225401/C 03/2023

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

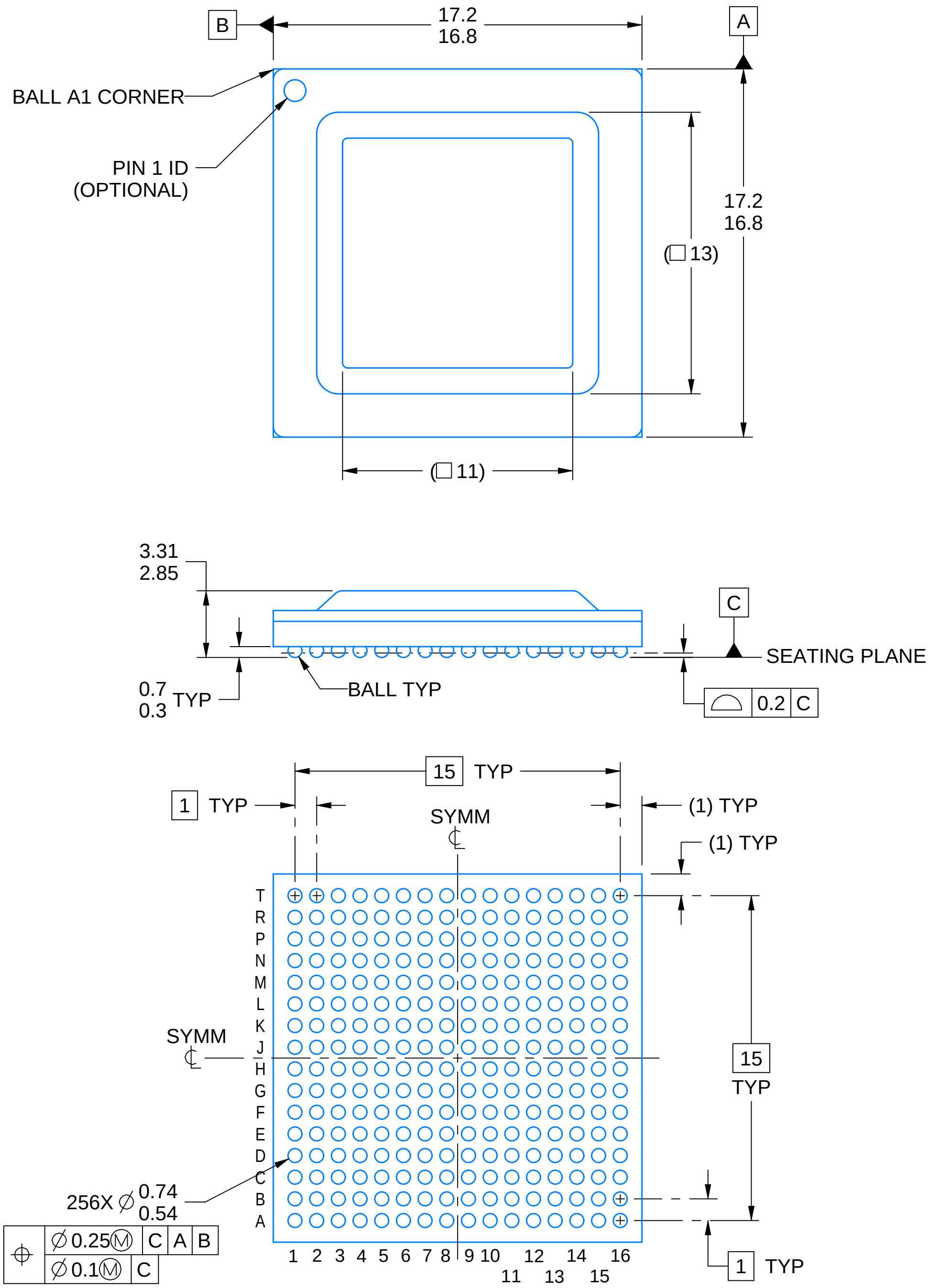


SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

4225401/C 03/2023

NOTES: (continued)

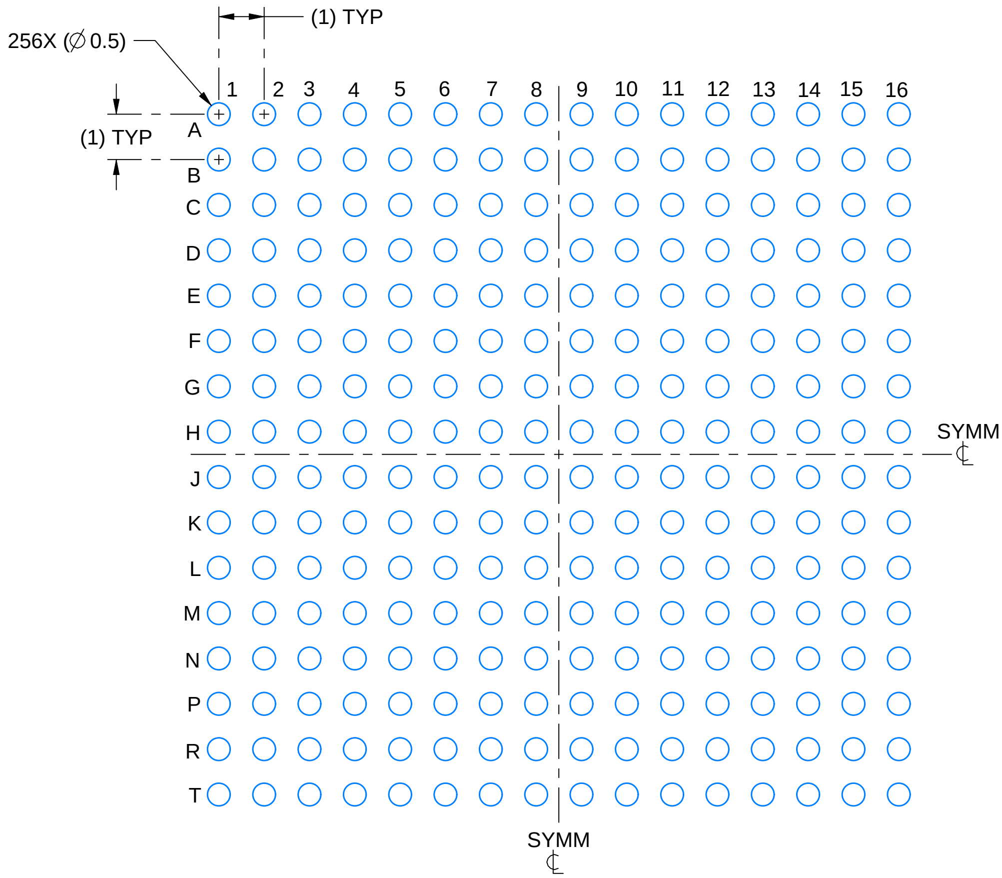
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



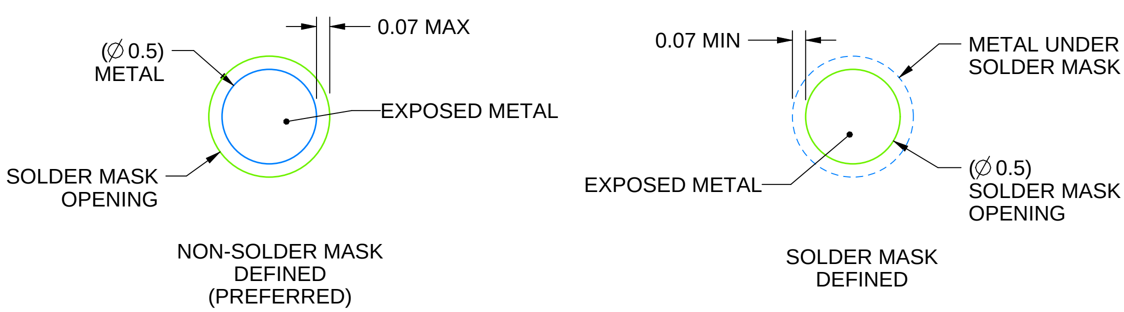
4223888/D 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pb-Free die bump and solder ball.
4. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SNOWN
SCALE:6X

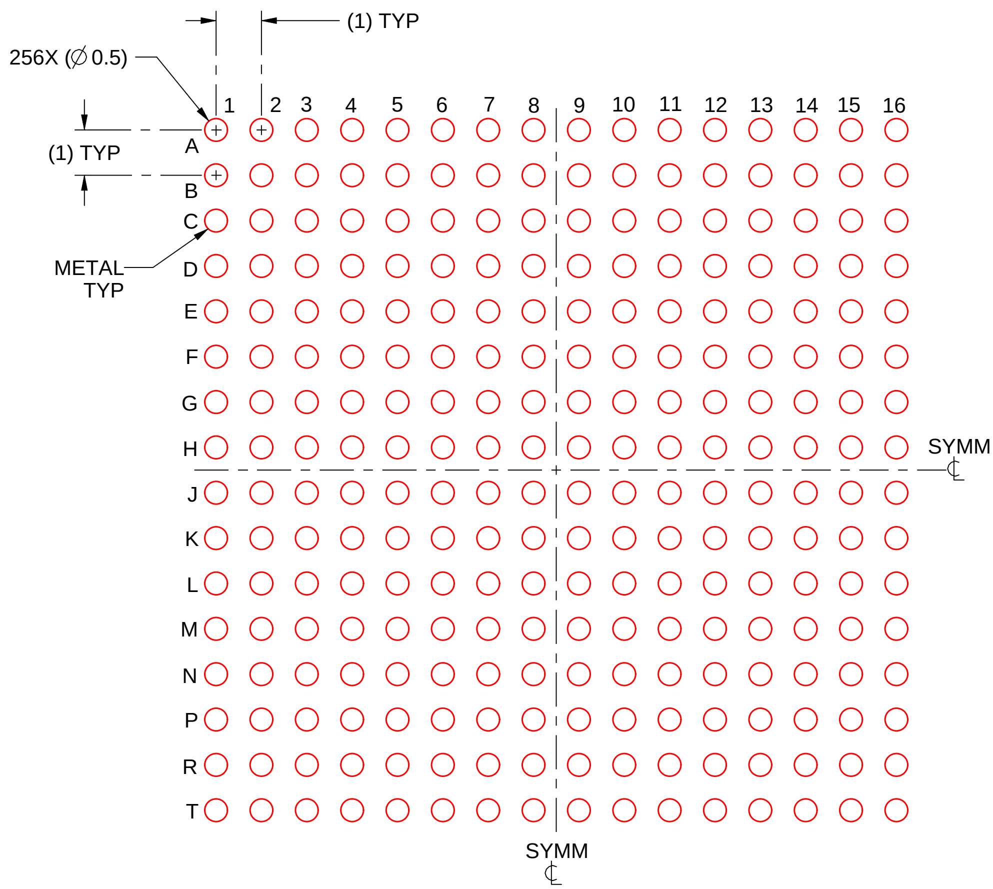


SOLDER MASK DETAILS
NOT TO SCALE

4223888/D 03/2023

NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

4223888/D 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.