DAC121C081およびDAC121C085 12ビットMicro Power D/Aコンバータ、I²C互換インターフェイス搭載

1 特長

- 12ビットの単調性を保証
- 低消費電力の動作: 3.3Vで最大値156µA
- 拡張電源電圧範囲: 2.7V～5.5V
- I²C互換の2線式インターフェイス、Standard (100kHz)、Fast (400kHz)、High-Speed (3.4MHz)モードをサポート
- レール・ツー・レール電圧出力
- 非常に小型のパッケージ
- 分解能: 12ビット
- INL: ±8LSB (最大値)
- DNL: 0.6/–0.5LSB (最大値)
- セトリング時間: 8.5µs (最大値)
- ゼロコード誤差: 10mV (最大値)
- フルスケール誤差: -0.7%FS (最大値)
- 供給電力
  - 通常: 380µW (3V) / 730µW (5V) (標準値)
  - パワーダウン時: 0.5µW (3V) / 0.9µW (5V) (標準値)

2 アプリケーション

- 産業用プロセス制御
- 携帯測定機器
- デジタル・ゲインおよびオフセットの調整
- プログラム可能な電圧源および電流源
- 試験用機器

3 概要

DAC121C081は12ビット、シングル・チャネル、電圧出力のD/Aコンバータ(DAC)で、2.7V～5.5Vの電源で動作します。出力アンプではレール・ツー・レールの出力が可能で、セトリング時間は8.5µsです。DAC121C081は電源電圧を基準として使い、最も広い動的出力範囲を提供します。5Vでの動作時、消費電流は通常値で132µAです。6ピンのSOTおよびWSONパッケージで供給され、3つのアドレス・オプションをピンにより選択できます。

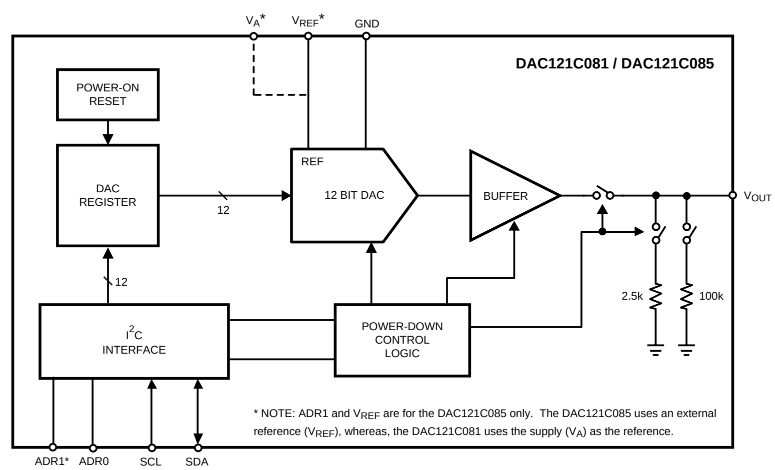
代替品として、DAC121C085は9つのI²Cアドレシング・オプションがあり、外部基準電圧を使用します。性能やセトリング時間はDAC121C081と同じで、8リードのVSSOPで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DAC121C081	WSON (6)	2.20mm×2.50mm
	SOT (6)	1.60mm×2.90mm
DAC121C085	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (January 2016) から Revision F に変更 — **Page**

- Changed V_{OUT} and V_A descriptions. 4
- Added column to Table 2. 19

Revision D (March 2013) から Revision E に変更 — **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 1
- Added addresses that the DAC responds to on the I2C bus. 18

Revision C (March 2013) から Revision D に変更 — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format 29

5 概要（続き）

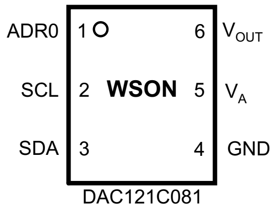
DAC121C081およびDAC121C085で使用する2線式のI^2C互換シリアル・インターフェイスは、High-Speedモード(3.4MHz)も含む3つの速度モードすべてで動作します。外部アドレス選択ピンにより、2線式バスごとに3つまでのDAC121C081、または9つまでのDAC121C085デバイスを使用できます。DAC121C081には、追加のアドレス・オプションを使用できるピン互換の代替品もあります。

DAC121C081およびDAC121C085には16ビットのレジスタが内蔵されており、動作モード、パワーダウン条件、出力電圧を制御できます。パワー・オン・リセット回路により、0VまでのDAC出力電力が保証されます。パワーダウン機能により、消費電力は1マイクロワット未満まで減少します。低消費電力と小型のパッケージから、これらのDACはバッテリ駆動の機器で使用するための非常に優れた選択肢です。各DACは、拡張産業用温度範囲の-40℃～+125℃で動作します。

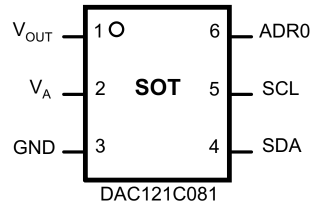
DAC121C081およびDAC121C085は、どちらもピン互換なDACファミリの一部であり、このファミリには分解能が8および10ビットの製品も含まれています。8ビットDACについては、DAC081C081とDAC081C085を参照してください。10ビットDACについては、DAC101C081とDAC101C085を参照してください。

6 Pin Configuration and Functions

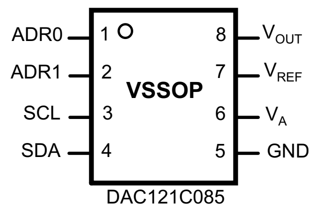
NGF Package
6-Pins WSON
Top View



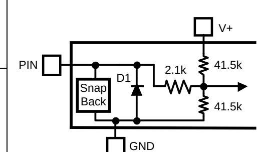
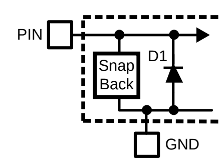
DDC Package
6-Pin SOT
Top View



DGK Package
8-Pins VSSOP
Top View



Pin Functions

PIN				TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	WSON	SOT	VSSOP			
ADR0	1	6	1	Digital Input, three levels	Tri-state Address Selection Input. Sets the two Least Significant Bits (A1 and A0) of the 7-bit slave address. (see Table 1)	
ADR1	—	—	2	Digital Input, three levels	Tri-state Address Selection Input. Sets Bits A6 and A3 of the 7-bit slave address. (see Table 1)	
GND	4	3	5	Ground	Ground for all on-chip circuitry	—
SCL	2	5	3	Digital Input	Serial Clock Input. SCL is used together with SDA to control the transfer of data in and out of the device.	
SDA	3	4	4	Digital Input/Output	Serial Data bi-directional connection. Data is clocked into or out of the internal 16-bit register relative to the clock edges of SCL. This is an open-drain data line that must be pulled to the supply (V_A) by an external pullup resistor.	
V_{OUT}	6	1	8	Analog Output	Analog Output Voltage	—
V_A	5	2	6	Supply	Power supply input. For the SOT and WSON versions, this supply is used as the reference. Must be decoupled to GND.	—
VREF	—	—	7	Supply	Unbufferred reference voltage. For the VSSOP, this supply is used as the reference. V_{REF} must be free of noise and decoupled to GND.	—
PAD	(LLP only)	—	—	Ground	Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.	—

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2][3]

	MIN	MAX	UNIT
Supply voltage, V_A	–0.3	6.5	V
Voltage on any input pin	–0.3	6.5	V
Input current at any pin[4]		±10	mA
Package input current[4]		±20	mA
Power consumption at T_A = 25°C		See[5]	
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds 5.5 V or is less than GND, the current at that pin should be limited to 10 mA. The 20-mA maximum package input current ratings limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(5) The absolute maximum junction temperature (T_{Jmax}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{Jmax}, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula PDMAX = ($T_{Jmax} - T_A$) / θ_{JA}. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed).

7.2 ESD Ratings

				VALUE	UNIT
DAC081C081 in NGF Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except 2 and 3	±2500	V
			Pins 2 and 3	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101	All pins except 2 and 3	±1000	
			Pins 2 and 3	±1000	
		Machine model (MM)	All pins except 2 and 3	±250	
			Pins 2 and 3	±350	
DAC081C081 in DDC Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except 4 and 5	±2500	V
			Pins 4 and 5	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101	All pins except 4 and 5	±1000	
			Pins 4 and 5	±1000	
		Machine model (MM)	All pins except 4 and 5	±250	
			Pins 4 and 5	±350	
DAC081C085 in DGK Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except 3 and 4	±2500	V
			Pins 3 and 4	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101	All pins except 3 and 4	±1000	
			Pins 3 and 4	±1000	
		Machine model (MM)	All pins except 3 and 4	±250	
			Pins 3 and 4	±350	

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Operating temperature, T_A	−40	125	°C
Supply voltage, V_A	2.7	5.5	V
Reference voltage, V_{REFIN}	1	V_A	V
Digital input voltage(2)	0	5.5	V
Output load	0	1500	pF

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(2) The inputs are protected as shown in the following. Input voltage magnitudes up to 5.5 V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3 V, the digital input pins can be driven with a 5-V logic device.

7.4 Thermal Information

THERMAL METRIC(1)(2)(3)		DAC121C081		DAC121C085	UNIT
		NGF (WSON)	DDC (SOT)	DGK (VSSOP)	
		6 PINS	6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	190	250	240	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Soldering process must comply with Texas Instruments' *Reflow Temperature Profile Specifications*, SNOA549.
(3) Reflow temperature profiles are different for lead-free packages.

7.5 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, C_L = 200 pF to GND, input code range 48 to 4047. All Maximum and Minimum limits apply for $T_{MIN} \le T_A \le T_{MAX}$ and all Typical limits are at T_A = 25°C, unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX(2)	UNIT
STATIC PERFORMANCE						
INL	Resolution		12			Bits
	Monotonicity		12			Bits
	Integral Non-Linearity			2.2	8	LSB
			–8	–1.5		
DNL	Differential Non-Linearity			0.18	0.6	LSB
			–0.5	–0.12		LSB
ZE	Zero Code Error	I_{OUT} = 0		1.1	10	mV
FSE	Full-Scale Error	I_{OUT} = 0		–0.1	−0.7	%FSR
GE	Gain Error	All ones Loaded to DAC register		–0.2	−0.7	%FSR
ZCED	Zero Code Error Drift			–20		µV/°C
TC GE	Gain Error Tempco	V_A = 3 V		–0.7		ppm FSR/°C
		V_A = 5 V		–1		
ANALOG OUTPUT CHARACTERISTICS (V_{OUT})						
	Output voltage range(3)	DAC121C085	0		V_{REF}	V
		DAC121C081	0		V_A	
ZCO	Zero code output	V_A = 3 V, I_{OUT} = 200 µA		1.3		mV
		V_A = 5 V, I_{OUT} = 200 µA		7		
FSO	Full scale output	V_A = 3 V, I_{OUT} = 200 µA		2.984		V
		V_A = 5 V, I_{OUT} = 200 µA		4.989		
I_{OS}	Output short-circuit current (I_{SOURCE})	V_A = 3 V, V_{OUT} = 0 V, Input Code = FFFh.		56		mA
		V_A = 5 V, V_{OUT} = 0 V, Input Code = FFFh.		69		
I_{OS}	Output short-circuit current (I_{SINK})	V_A = 3 V, V_{OUT} = 3 V, Input Code = 000h.		–52		mA
		V_A = 5 V, V_{OUT} = 5 V, Input Code = 000h.		–75		
I_O	Continuous output current(3)	Available on the DAC output			11	mA
C_L	Maximum load capacitance	R_L = ∞		1500		pF
		R_L = 2 kΩ		1500		
Z_{OUT}	DC output impedance			7.5		Ω
REFERENCE INPUT CHARACTERISTICS (DAC121C085 only)						
V_{REF}	Input range minimum		1	0.2		V
	Input range maximum				V_A	V
	Input impedance			120		kΩ
LOGIC INPUT CHARACTERISTICS (SCL, SDA)						
V_{IH}	Input high voltage		0.7 × V_A			V
V_{IL}	Input low voltage				0.3 × V_A	V
I_{IN}	Input current				±1	µA
C_{IN}	Input pin capacitance(3)				3	pF
V_{HYST}	Input hysteresis		0.1 × V_A			V
LOGIC INPUT CHARACTERISTICS (ADR0, ADR1)						
V_{IH}	Input high voltage		V_A- 0.5			V

(1) Values shown in this table are design targets and are subject to change before product release.
(2) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(3) This parameter is specified by design and/or characterization and is not tested in production.

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, C_L = 200 pF to GND, input code range 48 to 4047. All Maximum and Minimum limits apply for $T_{MIN} \le T_A \le T_{MAX}$ and all Typical limits are at T_A = 25°C, unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX(2)	UNIT
V_{IL}	Input low voltage					0.5	V
I_{IN}	Input current					±1	µA
LOGIC OUTPUT CHARACTERISTICS (SDA)							
V_{OL}	Output low voltage	I_{SINK} = 3 mA				0.4	V
		I_{SINK} = 6 mA				0.6	
I_{OZ}	High-impedence output leakage current					±1	µA
POWER REQUIREMENTS							
V_A	Supply voltage minimum			2.7			V
	Supply voltage maximum					5.5	
Normal -- V_{OUT} set to midscale. 2-wire interface quiet (SCL = SDA = V_A). (output unloaded)							
I_{ST_VA-1}	V_A **DAC121C081** supply current	V_A = 2.7 V to 3.6 V			105	156	µA
		V_A = 4.5 V to 5.5 V			132	214	
I_{ST_VA-5}	V_A **DAC121C085** supply current	V_A = 2.7 V to 3.6 V			86	118	µA
		V_A = 4.5 V to 5.5 V			98	152	
I_{ST_VREF}	V_{REF} supply current (DAC121C085 only)	V_A = 2.7 V to 3.6 V			37	43	µA
		V_A = 4.5 V to 5.5 V			53	61	
P_{ST}	Power consumption (V_A and V_{REF} for DAC121C085)(4)	V_A = 3 V			380		µW
		V_A = 5 V			730		
Continuous Operation -- 2-wire interface actively addressing the DAC and writing to the DAC register. (output unloaded)							
I_{CO_VA-1}	V_A **DAC121C081** supply current	f_{SCL}=400 kHz	V_A = 2.7 V to 3.6 V		134	220	µA
			V_A = 4.5 V to 5.5 V		192	300	
		f_{SCL} = 3.4 MHz	V_A = 2.7 V to 3.6 V		225	320	µA
			V_A = 4.5 V to 5.5 V		374	500	
I_{CO_VA-5}	V_A **DAC121C085** supply current	f_{SCL} = 400 kHz	V_A = 2.7 V to 3.6 V		101	155	µA
			V_A = 4.5 V to 5.5 V		142	220	
		f_{SCL} = 3.4 MHz	V_A = 2.7 V to 3.6 V		193	235	µA
			V_A = 4.5 V to 5.5 V		325	410	
I_{CO_VREF}	V_{REF} supply current (DAC121C085 only)		V_A = 2.7 V to 3.6 V		33.5	55	µA
			V_A = 4.5 V to 5.5 V		49.5	71.4	
P_{CO}	Power consumption (V_A and V_{REF} for DAC121C085)	f_{SCL} = 400 kHz	V_A = 3 V		480		µW
			V_A = 5 V		1.06		mW
		f_{SCL} = 3.4 MHz	V_A = 3 V		810		µW
			V_A = 5 V		2.06		mW
Power Down -- 2-wire interface quiet (SCL = SDA = V_A) after PD mode written to DAC register. (output unloaded)							
I_{PD}	Supply current (V_A and V_{REF} for DAC121C085)	All power-down modes	V_A = 2.7 V to 3.6		0.13	1.52	µA
			V_A = 4.5 V to 5.5 V		0.15	3.25	
P_{PD}	Power consumption (V_A and V_{REF} for DAC121C085)	All power-down modes	V_A = 3 V		0.5		µW
			V_A = 5 V		0.9		

(4) To ensure accuracy, it is required that V_A and V_{REF} be well bypassed.

7.6 AC and Timing Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, R_L = Infinity, C_L = 200 pF to GND. All Maximum and Minimum limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$ and all Typical limits are at T_A = 25°C, unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(3)	MAX(2)(3)	UNIT
t_s	Output Voltage Settling Time(4)	400h to C00h code change R_L = 2 kΩ, C_L = 200 pF		6	8.5	µs
SR	Output Slew Rate			1		V/µs
	Glitch Impulse	Code change from 800h to 7FFh		12		nV-sec
	Digital Feedthrough			0.5		nV-sec
	Multiplying Bandwidth(5)	V_{REF} = 2.5 V ± 0.1 Vpp		160		kHz
	Total Harmonic Distortion(5)	V_{REF} = 2.5 V ± 0.1 Vpp input frequency = 10 kHz		70		dB
t_{WU}	Wake-Up Time	V_A = 3 V		0.8		µs
		V_A = 5 V		0.5		µs
DIGITAL TIMING SPECS (SCL, SDA)						
f_{SCL}	Serial Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
		High Speed Mode, C_b = 100 pF			3.4	MHz
		High Speed Mode, C_b = 400 pF			1.7	MHz
t_{LOW}	SCL Low Time	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
		High Speed Mode, C_b = 100 pF	160			ns
		High Speed Mode, C_b = 400 pF	320			ns
t_{HIGH}	SCL High Time	Standard Mode	4			µs
		Fast Mode	0.6			µs
		High Speed Mode, C_b = 100 pF	60			ns
		High Speed Mode, C_b = 400 pF	120			ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode	250			ns
		Fast Mode	100			ns
		High Speed Mode	10			ns
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		0.9	µs
		High Speed Mode, C_b = 100 pF	0		70	ns
		High Speed Mode, C_b = 400 pF	0		150	ns
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
		High Speed Mode	160			ns
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard Mode	4			µs
		Fast Mode	0.6			µs
		High Speed Mode	160			ns
t_{BUF}	Bus free time between a stop and start condition	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
$t_{SU;STO}$	Setup time for a stop condition	Standard Mode	4			µs
		Fast Mode	0.6			µs
		High Speed Mode	160			ns

(1) Values shown in this table are design targets and are subject to change before product release.
(2) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.
(3) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Applies to the Multiplying DAC configuration. In this configuration, the reference is used as the analog input. The value loaded in the DAC Register will digitally attenuate the signal at Vout.

AC and Timing Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, R_L = Infinity, C_L = 200 pF to GND. All Maximum and Minimum limits apply for $T_{MIN} \le T_A \le T_{MAX}$ and all Typical limits are at T_A = 25°C, unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(3)	MAX(2)(3)	UNIT
t_{rDA}	Rise time of SDA signal	Standard Mode			1000	ns
		Fast Mode	20+0.1C_b		300	
		High Speed Mode, C_b = 100 pF	10		80	
		High Speed Mode, C_b = 400 pF	20		160	
t_{fDA}	Fall time of SDA signal	Standard Mode			250	ns
		Fast Mode	20+0.1C_b		250	
		High Speed Mode, C_b = 100 pF	10		80	
		High Speed Mode, C_b = 400 pF	20		160	
t_{rCL}	Rise time of SCL signal	Standard Mode			1000	ns
		Fast Mode	20+0.1C_b		300	
		High Speed Mode, C_b = 100 pF	10		40	
		High Speed Mode, C_b = 400 pF	20		80	
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit.	Standard Mode			1000	ns
		Fast Mode	20+0.1C_b		300	
		High Speed Mode, C_b = 100 pF	10		80	
		High Speed Mode, C_b = 400 pF	20		160	
t_{fCL}	Fall time of a SCL signal	Standard Mode			300	ns
		Fast Mode	20+0.1C_b		300	
		High Speed Mode, C_b = 100 pF	10		40	
		High Speed Mode, C_b = 400 pF	20		80	
C_b	Capacitive load for each bus line (SCL and SDA)				400	pF
t_{SP}	Pulse Width of spike suppressed(6)(4)	Fast Mode			50	ns
		High Speed Mode			10	
t_{outz}	SDA output delay (see the *Additional Timing Information* section)	Fast Mode		87	270	ns
		High Speed Mode		38	60	

(6) Spike suppression filtering on SCL and SDA will supress spikes that are less than 50 ns for standard-fast mode and less than 10ns for hs-mode.

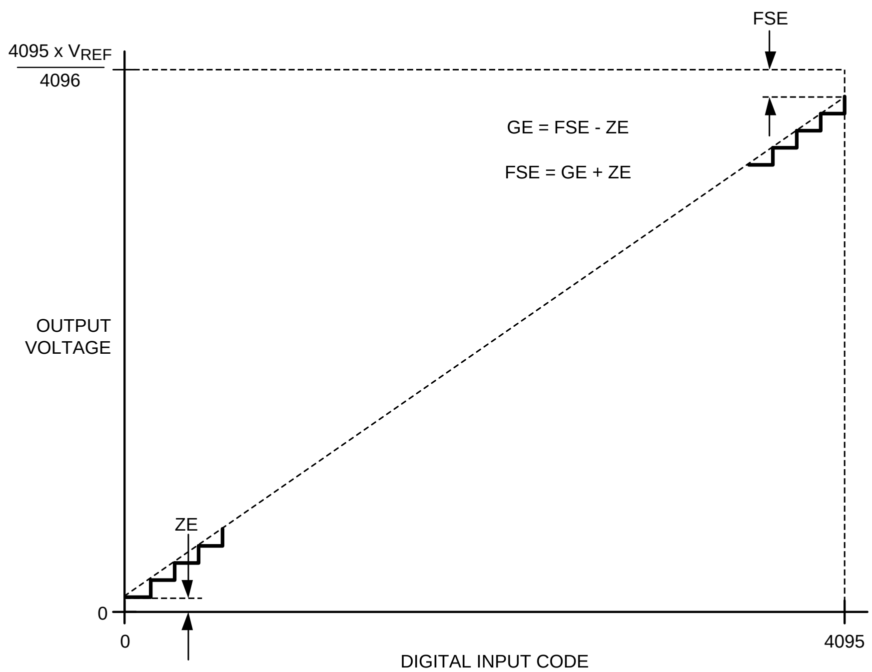


Figure 1. Input / Output Transfer Characteristic

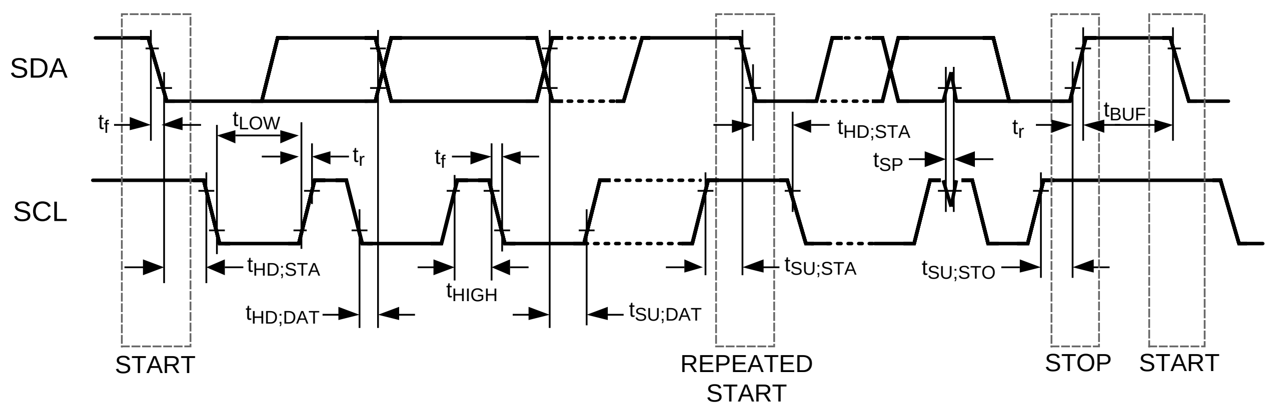


Figure 2. Serial Timing Diagram

7.7 Typical Characteristics

$V_{REF} = V_A$, f_{SCL} = 3.4 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

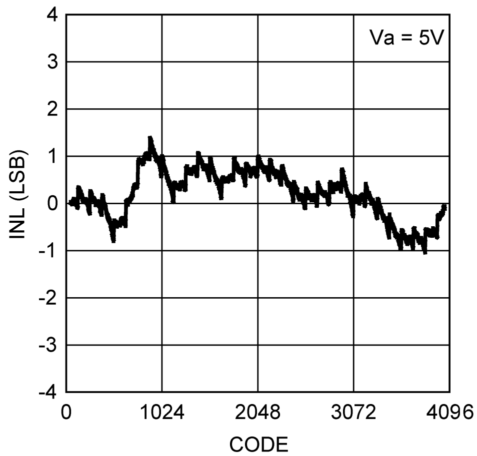


Figure 3. INL

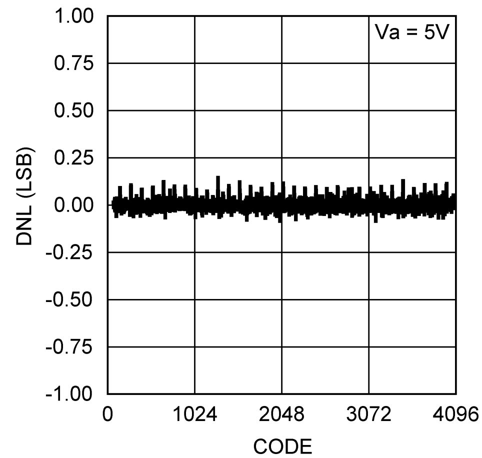


Figure 4. DNL

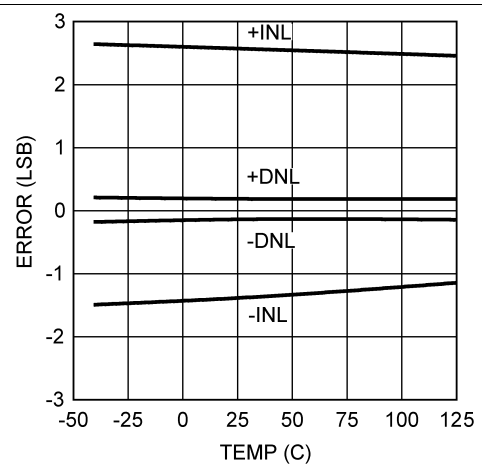


Figure 5. INL/DNL vs Temperature at V_A = 3 V

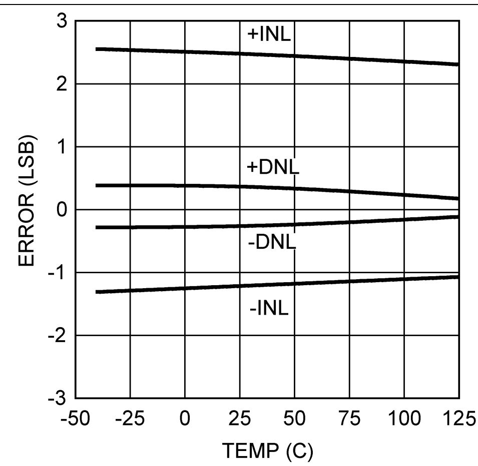


Figure 6. INL/DNL vs Temperature at V_A = 5 V

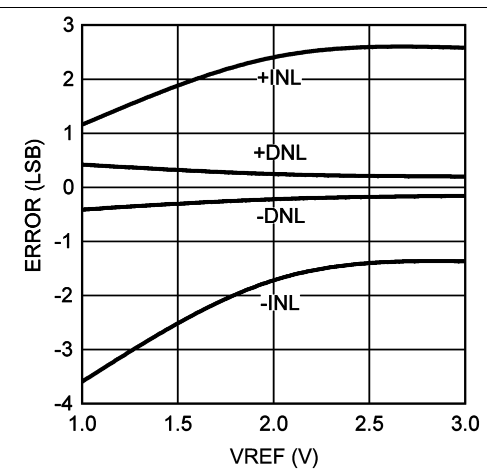


Figure 7. INL/DNL vs V_{REFIN} at V_A = 3 V

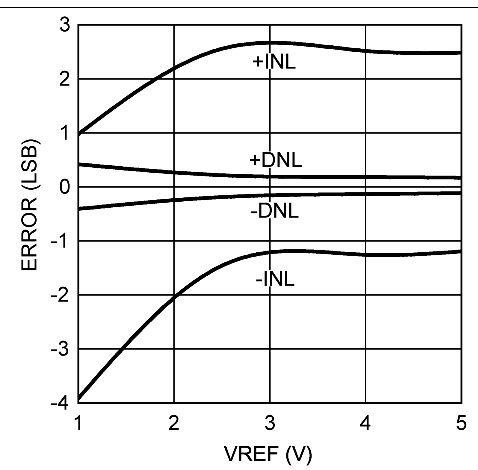


Figure 8. INL/DNL vs V_{REFIN} at V_A = 5 V

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCL} = 3.4 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

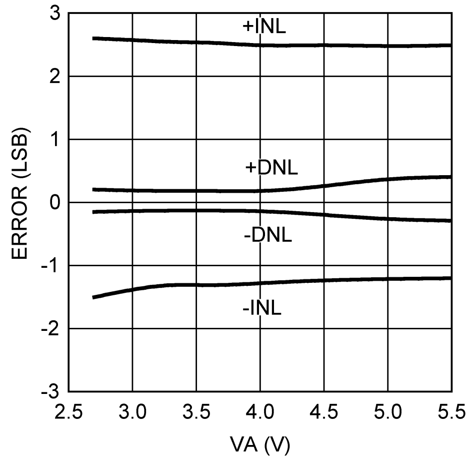


Figure 9. INL/DNL vs V_A

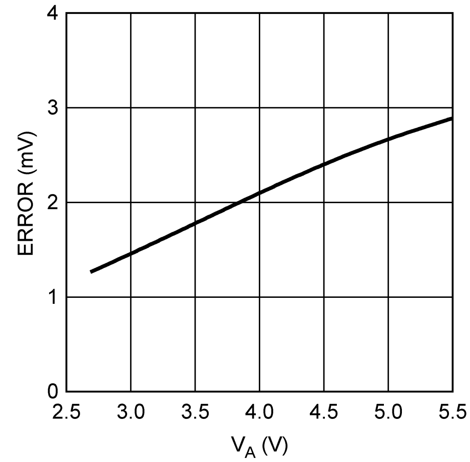


Figure 10. Zero Code Error vs V_A

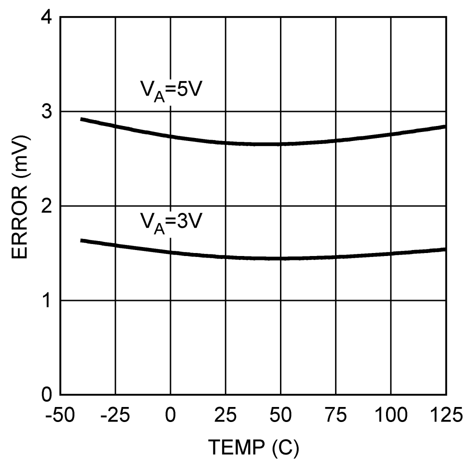


Figure 11. Zero Code Error vs Temperature

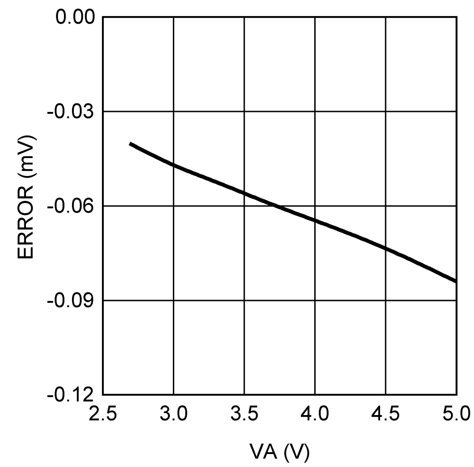


Figure 12. Full Scale Error vs V_A

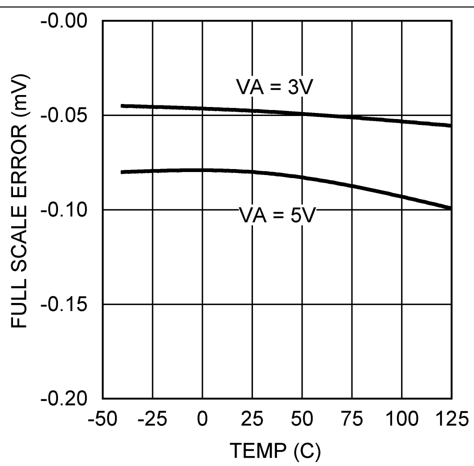


Figure 13. Full Scale Error vs Temperature

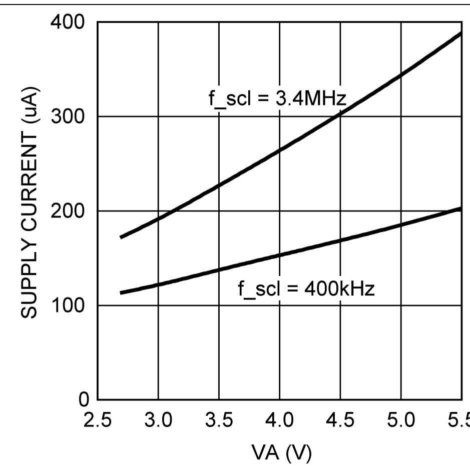


Figure 14. Total Supply Current vs V_A

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCL} = 3.4 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

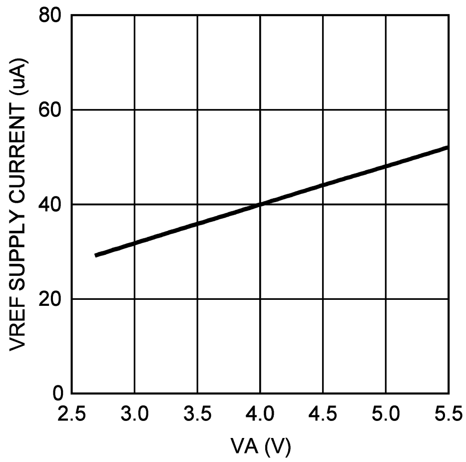


Figure 15. V_{REF} Supply Current vs V_A

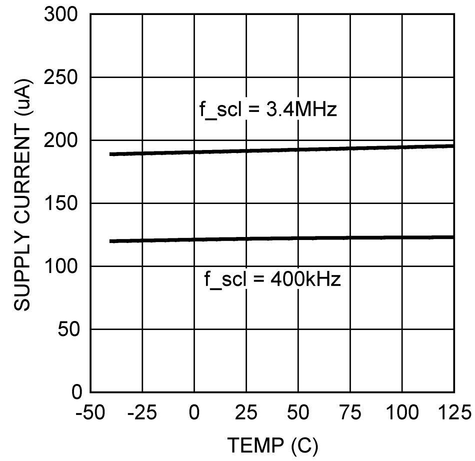


Figure 16. Total Supply Current vs Temperature at V_A = 3 V

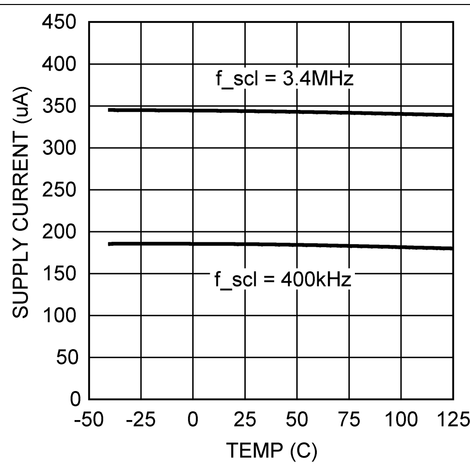


Figure 17. Total Supply Current vs Temperature at V_A = 5 V

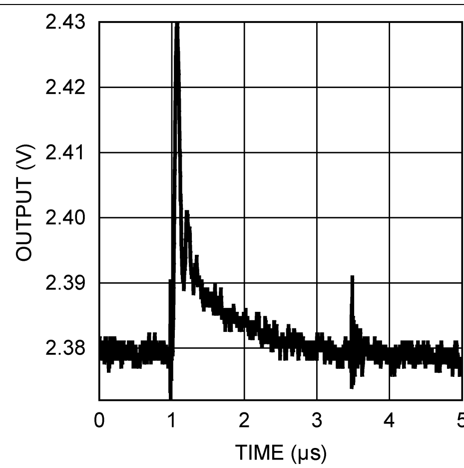


Figure 18. 5-V Glitch Response

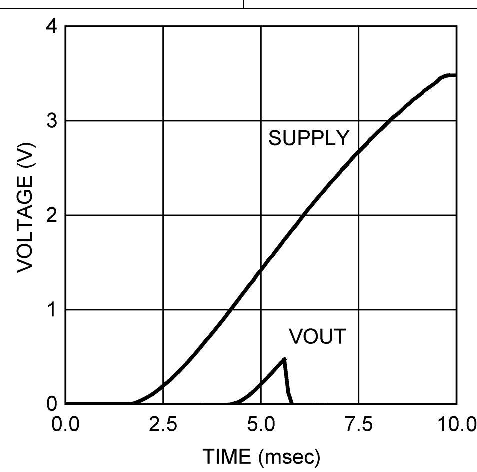


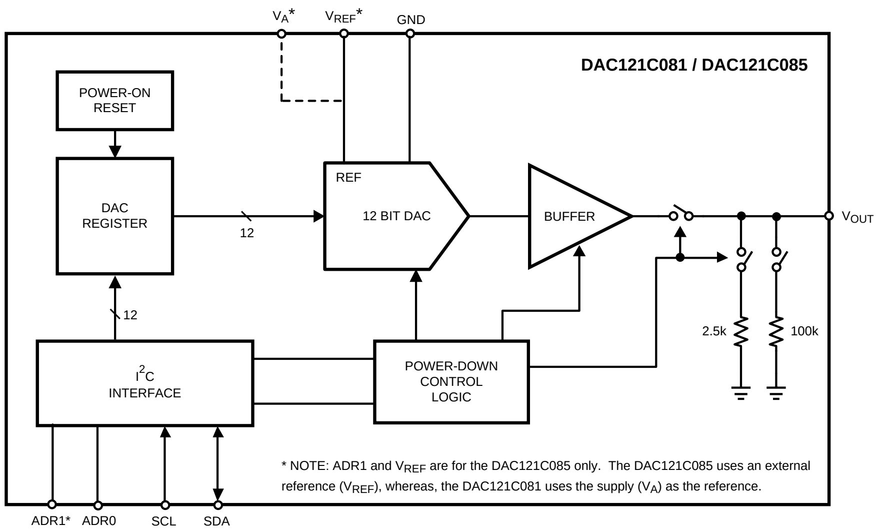
Figure 19. Power-On Reset

8 Detailed Description

8.1 Overview

The DAC121C081 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Section

The DAC121C081 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer.

For simplicity, a single resistor string is shown in Figure 20. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_{REF} \times (D / 4096)$$

where D is the decimal equivalent of the binary code that is loaded into the DAC register. (1)

D can take on any integer value from 0 to 4095. This configuration ensures that the DAC is monotonic.

Feature Description (continued)

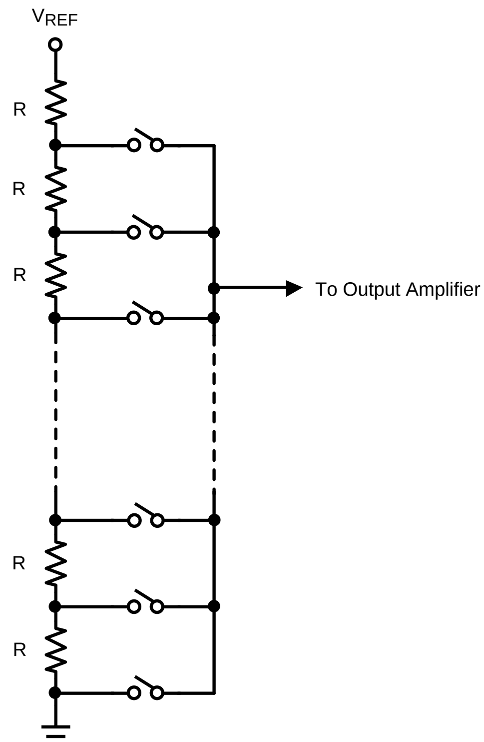


Figure 20. DAC Resistor String

8.3.2 Output Amplifier

The output amplifier is rail-to-rail, providing an output voltage range of 0 V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes. The output capabilities of the amplifier are described in the *Electrical Characteristics*.

The output amplifiers are capable of driving a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the *Electrical Characteristics*.

8.3.3 Reference Voltage

The DAC121C081 uses the supply (V_A) as the reference. With that said, V_A must be treated as a reference. The analog output is only as clean as the reference (V_A). TI recommends driving the reference with a voltage source with low-output impedance.

The DAC121C085 comes with an external reference supply pin (V_{REF}). For the DAC121C085, it is important that V_{REF} be kept as clean as possible.

Applications Information describes a handful of ways to drive the reference appropriately. See *Using References as Power Supplies* for details.

Feature Description (continued)

8.3.4 Serial Interface

The I²C-compatible interface operates in all three speed modes. Standard mode (100 kHz) and Fast mode (400 kHz) are functionally the same and will be referred to as Standard-Fast mode in this document. High-Speed mode (3.4MHz) is an extension of Standard-Fast mode and will be referred to as Hs-mode in this document. The following diagrams describe the timing relationships of the clock (SCL) and data (SDA) signals. Pullup resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled up externally. The appropriate pullup resistor values depends on the total bus capacitance and operating speed.

8.3.4.1 Basic I²C Protocol

The I²C interface is bi-directional and allows multiple devices to operate on the same bus. To facilitate this bus configuration, each device has a unique hardware address which is referred to as the slave address. To communicate with a particular device on the bus, the controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit. If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled high. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a Stop condition on the bus.

All communication on the bus begins with either a Start condition or a Repeated Start condition. The protocol for starting the bus varies between Standard-Fast mode and Hs-mode. In Standard-Fast mode, the master generates a Start condition by driving SDA from high to low while SCL is high. In Hs-mode, starting the bus is more complicated. See *High-Speed (Hs) Mode* for the full details of a Hs-mode Start condition. A Repeated Start is generated to either address a different device, or switch between read and write modes. The master generates a Repeated Start condition by driving SDA low while SCL is high. Following the Repeated Start, the master sends out the slave address and a read/write bit as shown in Figure 21. The bus continues to operate in the same speed mode as before the Repeated Start condition.

All communication on the bus ends with a Stop condition. In either Standard-Fast mode or Hs-Mode, a Stop condition occurs when SDA is pulled from low to high while SCL is high. After a Stop condition, the bus remains idle until a master generates a Start condition.

See the Phillips I²C® Specification (Version 2.1 Jan, 2000) for a detailed description of the serial interface.

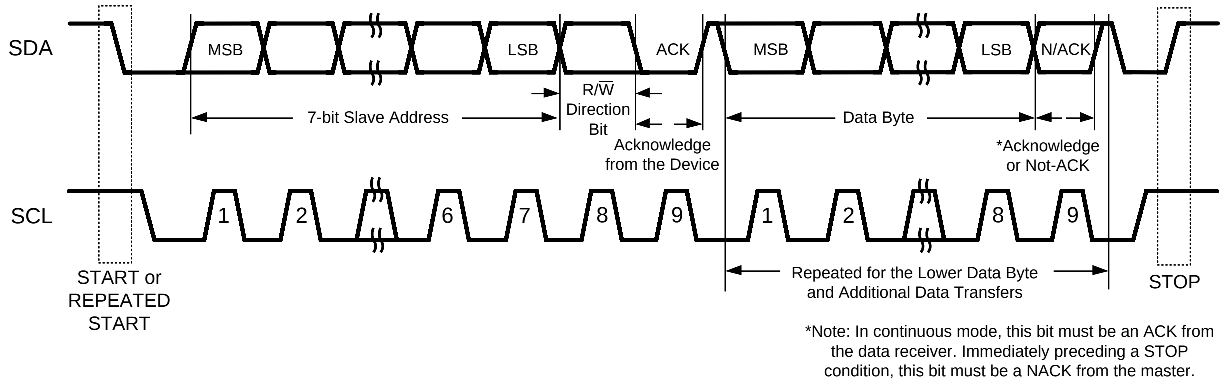


Figure 21. Basic Operation

Feature Description (continued)

8.3.4.2 Standard-Fast Mode

In Standard-Fast mode, the master generates a start condition by driving SDA from high to low while SCL is high. The Start condition is always followed by a 7-bit slave address and a Read/Write bit. After these eight bits have been transmitted by the master, SDA is released by the master and the DAC121C081 either ACKs or NACKs the address. If the slave address matches, the DAC121C081 ACKs the master. If the address doesn't match, the DAC121C081 NACKs the master.

For a **write** operation, the master follows the ACK by sending the upper eight data bits to the DAC121C081. Then the DAC121C081 ACKs the transfer by driving SDA low. Next, the lower eight data bits are sent by the master. The DAC121C081 then ACKs the transfer. At this point, the DAC output updates to reflect the contents of the 16-bit DAC register. Next, the master either sends another pair of data bytes, generates a Stop condition to end communication, or generates a Repeated Start condition to communicate with another device on the bus.

For a **read** operation, the DAC121C081 sends out the upper eight data bits of the DAC register. This is followed by an ACK by the master. Next, the lower eight data bits of the DAC register are sent to the master. The master then produces a NACK by letting SDA be pulled high. The NACK is followed by a master-generated Stop condition to end communication on the bus, or a Repeated Start to communicate with another device on the bus.

8.3.4.3 High-Speed (Hs) Mode

For Hs-mode, the sequence of events to begin communication differ slightly from Standard-Fast mode. Figure 22 describes this in further detail. Initially, the bus begins running in Standard-Fast mode. The master generates a Start condition and sends the 8-bit Hs master code (00001XXX) to the DAC121C081. Next, the DAC121C081 responds with a NACK. Once the SCL line has been pulled to a high level, the master switches to Hs-mode by increasing the bus speed and generating a Repeated Start condition (driving SDA low while SCL is pulled high). At this point, the master sends the slave address to the DAC121C081, and communication continues as shown in Figure 21.

When the master generates a Repeated Start condition while in Hs-mode, the bus stays in Hs-mode awaiting the slave address from the master. The bus continues to run in Hs-mode until a Stop condition is generated by the master. When the master generates a Stop condition on the bus, the bus must be started in Standard-Fast mode again before increasing the bus speed and switching to Hs-mode. ns16705

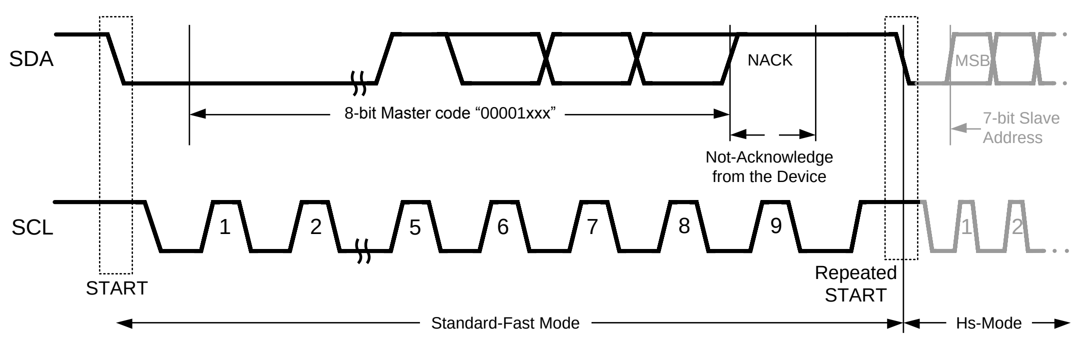


Figure 22. Beginning Hs-Mode Communication

8.3.4.4 I²C Slave (Hardware) Address

The DAC has a seven-bit I²C slave address. For the VSSOP version of the DAC, this address is configured by the ADR0 and ADR1 address selection inputs. For the DAC121C081, the address is configured by the ADR0 address selection input. ADR0 and ADR1 can be grounded, left floating, or tied to V_A. If desired, the address selection inputs can be set to $V_A/2$ rather than left floating. The state of these inputs sets the address the DAC responds to on the I²C bus (see Table 1). In addition to the selectable slave address, there is also a broadcast address (1001000) for all DAC121C081's and DAC121C085's on the 2-wire bus. When the bus is addressed by the broadcast address, all the DAC121C081's and DAC121C085's will respond and update synchronously. Figure 24 and Figure 25 describe how the master device should address the DAC through the I²C-Compatible interface.

Feature Description (continued)

Keep in mind that the address selection inputs (ADR0 and ADR1) are only sampled until the DAC is correctly addressed with a non-broadcast address. At this point, the ADR0 and ADR1 inputs TRI-STATE and the slave address is locked. Changes to ADR0 and ADR1 will not update the selected slave address until the device is power-cycled.

Table 1. Slave Addresses

Slave Address [A6 - A0]	DAC121C085 (VSSOP)		DAC121C081 (SOT AND WSON)(1)	Do Not Use(2)
	ADR1	ADR0	ADR0	
0001100	Floating	Floating	Floating	1000110
0001101	Floating	GND	GND	1000110
0001110	Floating	V_A	V_A	1000111
0001000	GND	Floating	---------------	1000100
0001001	GND	GND	---------------	1000100
0001010	GND	V_A	---------------	1000101
1001100	V_A	Floating	---------------	1100110
1001101	V_A	GND	---------------	1100110
1001110	V_A	V_A	---------------	1100111
1001000	--------------- Broadcast Address ---------------			1100100

(1) Pin-compatible alternatives to the DAC121C081 options are available with additional address options.
(2) These addresses should not be used by other I^2C devices on the I^2C bus. Using these addresses can cause the DAC121C081/085 to not respond when addressed by the assigned Slave Address.

8.3.5 Power-On Reset

The power-on reset circuit controls the output voltage of the DAC during power up. Upon application of power, the DAC register is filled with zeros and the output voltage is 0 V. The output remains at 0 V until a valid write sequence is made to the DAC.

When resetting the device, it is crutial that the V_A supply be lowered to a maximum of 200 mV before the supply is raised again to power up the device. Dropping the supply to within 200 mV of GND during a reset will ensure the ADC performs as specified.

8.3.6 Simultaneous Reset

The broadcast address allows the I^2C master to write a single word to multiple DACs simultaneously. Provided that all of the DACs exist on a single I^2C bus, every DAC updates when the broadcast address is used to address the bus. This feature allows the master to reset all of the DACs on a shared I^2C bus to a specific digital code. For instance, if the master writes a power-down code to the bus with the broadcast address, all of the DACs powers down simultaneously.

8.3.7 Additional Timing Information: t_{outz}

The t_{outz} specification is provided to aid the design of the I^2C bus. After the SCL bus is driven low by the I^2C master, the SDA bus will be held for a short time by the DAC121C081. This time is referred to as t_{outz}. The following figure illustrates the relationship between the fall of SCL, at the 30% threshold, to the time when the DAC begins to transition the SDA bus. The t_{outz} specification only applies when the DAC is in control of the SDA bus. The DAC is only in control of the bus during an ACK by the DAC121C081 or a data byte read from the DAC (see Figure 25).

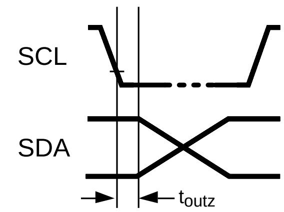


Figure 23. Data Output Timing

The t_{outz} specification is typically 87 ns in Standard-Fast Mode and 38 ns in Hs-Mode.

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The DAC121C081 has three power-down modes. In power-down mode, the supply current drops to 0.13 µA at 3 V and 0.15 µA at 5 V (typical). The DAC121C081 is put into power-down mode by writing a one to PD1 and/or PD0. The outputs can be set to high impedance, terminated by 2.5 kΩ to GND, or terminated by 100 kΩ to GND (see Figure 26).

The bias generator, output amplifier, resistor string, and other linear circuitry are all shut down in any of the power-down modes. When the DAC121C081 is powered down, the value written to the DAC register, including the power-down bits, is saved. While the DAC is in power-down, the saved DAC register contents can be read back. When the DAC is brought out of power-down mode, the DAC register contents will be overwritten and V_{OUT} will be updated with the new 12-bit data value.

The time to exit power-down (Wake-Up Time) is typically 0.8 µs at 3 V and 0.5 µs at 5 V.

8.5 Programming

8.5.1 Writing to the DAC Register

To write to the DAC, the master addresses the part with the correct slave address (A6-A0) and writes a zero to the read/write bit. If addressed correctly, the DAC returns an ACK to the master. The master then sends out the upper data byte. The DAC responds by sending an ACK to the master. Next, the master sends the lower data byte to the DAC. The DAC responds by sending an ACK again. At this point, the master either sends the upper byte of the next data word to be converted by the DAC, generates a Stop condition to end communication, or generates a Repeated Start condition to begin communication with another device on the bus. Until generating a Stop condition, the master can continuously write the upper and lower data bytes to the DAC register. This allows for a maximum DAC conversion rate of 188.9 kilo-conversions per second in Hs-mode.

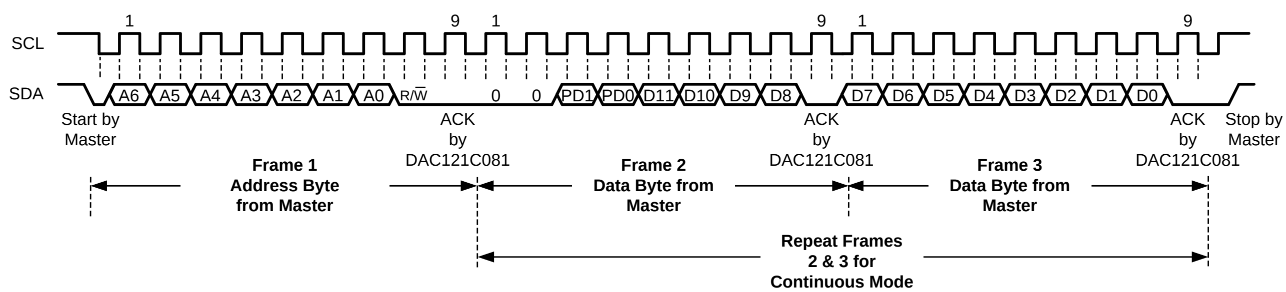


Figure 24. Typical Write to the DAC Register

Programming (continued)

8.5.2 Reading from the DAC Register

To read from the DAC register, the master addresses the part with the correct slave address (A6-A0) and writes a one to the read/write bit. If addressed correctly, the DAC returns an ACK to the master. Next, the DAC sends out the upper data byte. The master responds by sending an ACK to the DAC to indicate that it wants to receive another data byte. Then the DAC sends the lower data byte to the master. Assuming only one 16-bit data word is read, the master sends a NACK after receiving the lower data byte. At this point, the master either generates a Stop condition to end communication, or a Repeated Start condition to begin communication with another device on the bus.

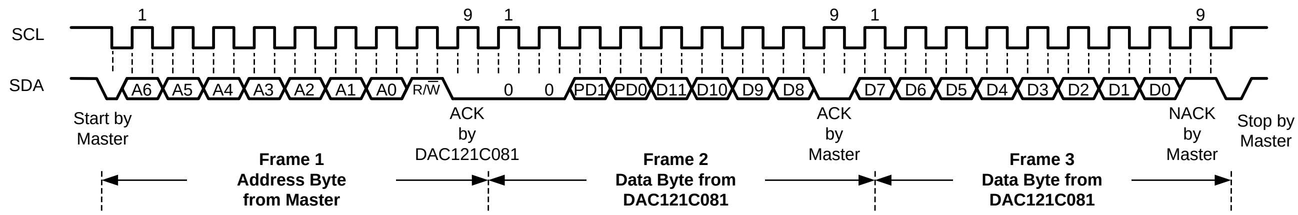


Figure 25. Typical Read from the DAC Register

8.6 Registers

8.6.1 DAC Register

The DAC register, Figure 26, has sixteen bits. The first two bits are always zero. The next two bits determine the mode of operation (normal mode or one of three power-down modes). The final twelve bits of the shift register are the data bits. The data format is straight binary (MSB first, LSB last), with twelve 0s corresponding to an output of 0 V and twelve 1s corresponding to a full-scale output of V_A – 1 LSB. When writing to the DAC Register, V_{OUT} will update on the rising edge of the ACK following the lower data byte.

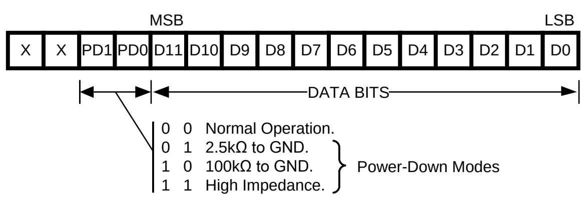


Figure 26. DAC Register Contents

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Bipolar Operation

The DAC121C081 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 27. This circuit provides an output voltage range of ±5 V. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5 V.

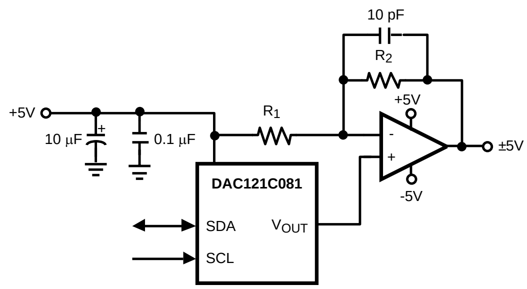


Figure 27. Bipolar Operation

The output voltage of this circuit for any code is found to be, as shown in Equation 2:

$V_O = (V_A \times (D / 4096) \times ((R1 + R2) / R1) – V_A \times R2 / R1)$

where D is the input code in decimal form. (2)

Equation 3 shows that with V_A = 5 V and R1 = R2,

$V_O = (10 \times D / 4096) – 5\ V$ (3)

A list of rail-to-rail amplifiers suitable for this application are indicated in Table 2.

Table 2. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typ V_{OS}	Typ I_{SUPPLY}
LMP7701	SOT-23	37 uV	0.79 mA
LMV841	SC70-5	50 uV	1 mA
LMC7111	SOT-23	0.9 mV	25 µA
LM7301	SO-8, SOT-23	0.03 mV	620 µA
LM8261	SOT-23	0.7 mV	1 mA

9.1.2 DSP/Microprocessor Interfacing

Interfacing the DAC121C081 to microprocessors and DSPs is quite simple. The following guidelines are offered to simplify the design process.

9.1.2.1 Interfacing to the 2-wire Bus

Figure 28 shows a microcontroller interfacing to the DAC121C081 through the 2-wire bus. Pullup resistors (Rp) should be chosen to create an appropriate bus rise time and to limit the current that will be sunk by the open-drain outputs of the devices on the bus. See the $I^2C^{®}$ Specification for further details. Typical pullup values to use in Standard-Fast mode bus applications are 2 kΩ to 10 kΩ. SCL and SDA series resisters (R_S) near the DAC121C081 are optional. If high-voltage spikes are expected on the 2-wire bus, series resistors should be used to filter the voltage on SDA and SCL. The value of the series resistance must be picked to ensure the V_{IL} threshold can be achieved. If used, R_S is typically 51 Ω.

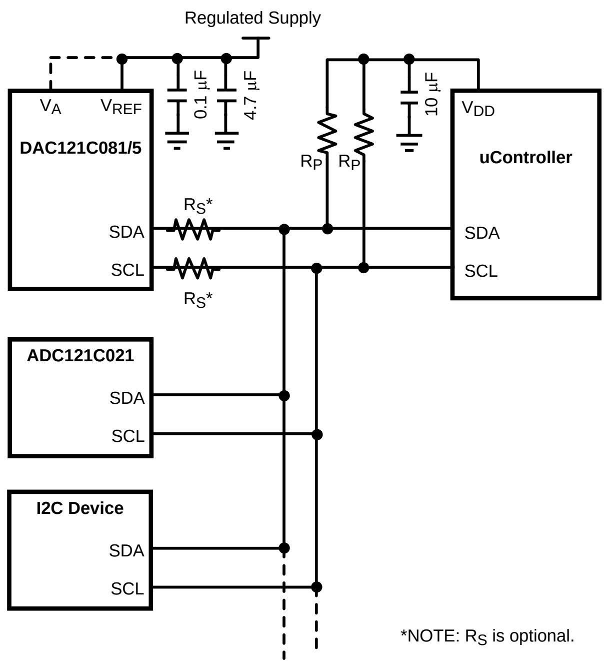


Figure 28. Serial Interface Connection Diagram

9.1.2.2 Interfacing to a Hs-mode Bus

Interfacing to a Hs-mode bus is very similar to interfacing to a Standard-Fast mode bus. In Hs-mode, the specified rise time of SCL is shortened. To create a faster rise time, the master device (microcontroller) can drive the SCL bus high and low. In other words, the microcontroller can drive the line high rather than leaving it to the pullup resistor. It is also possible to decrease the value of the pullup resistors or increase the pullup current to meet the tighter timing specs. See the $I^2C^{®}$ Specification for further details.

9.2 Typical Application

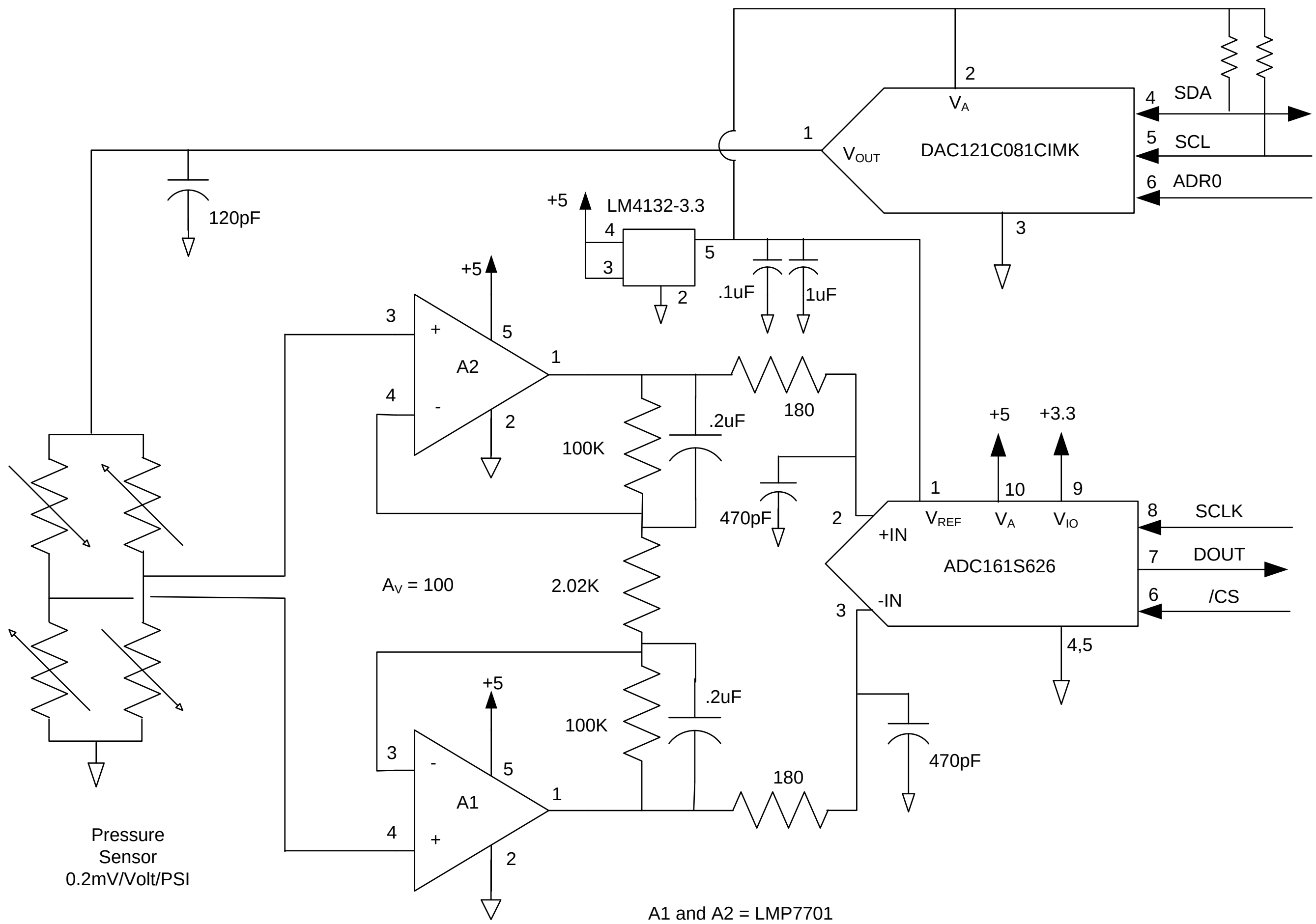


Figure 29. Pressure Sensor Gain Adjust

9.2.1 Design Requirements

A positive supply only data acquisition system capable of digitizing a pressure sensor output. In addition to digitizing the pressure sensor output, the system designer can use the DAC121C081 to correct for gain errors in the pressure sensor output by adjusting the bias voltage to the bridge pressure sensor.

9.2.2 Detailed Design Procedure

As shown in Equation 4, the output of the pressure sensor is relative to the imbalance of the resistive bridge times the output of the DAC121C081, thus providing the desired gain correction.

$$\text{Pressure Sensor Output} = (\text{DAC\_Output} \times [(R2 / (R1 + R2) - (R4 / (R3 + R4)] \quad (4)$$

Likewise for the ADC161S626, Equation 5 shows that the ADC output is function of the Pressure Sensor Output times relative to the ratio of the ADC input divided by the DAC121C081 output voltage.

$$\text{ADC161S626 Output} = (\text{Pressure Sensor Output} \times 100 /(2 \times \text{VREF})) \times 2^{16} \quad (5)$$

Typical Application (continued)

9.2.3 Application Curve

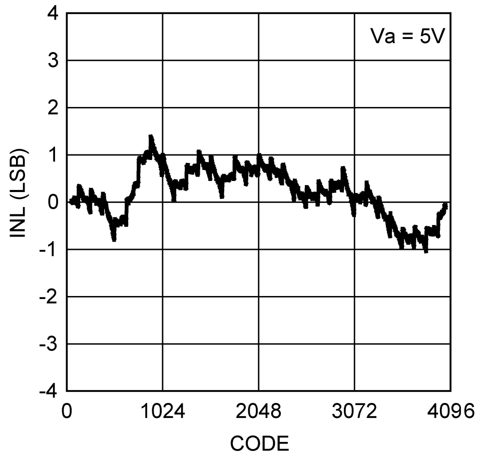


Figure 30. INL vs Input Code

10 Power Supply Recommendations

10.1 Using References as Power Supplies

While the simplicity of the DAC121C081 implies ease of use, it is important to recognize that the path from the reference input (V_A for the DAC121C081 and V_{REF} for the DAC121C085) to V_{OUT} will have essentially zero Power Supply Rejection Ratio (PSRR). Therefore, it is necessary to provide a noise-free supply voltage to the reference. To use the full dynamic range of the DAC121C085, the supply pin (V_A) and V_{REF} can be connected together and share the same supply voltage. Because the DAC121C081 consumes very little power, a reference source may be used as the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used. Listed below are a few reference and power supply options for the DAC121C081. When using the DAC121C081, it is important to treat the analog supply (V_A) as the reference.

10.1.1 LM4132

The LM4132, with its 0.05% accuracy over temperature, is a good choice as a reference source for the DAC121C081. The 4.096-V version is useful if a 0-V to 4.095-V output range is desirable or acceptable. Bypassing the LM4132 V_{IN} pin with a 0.1-µF capacitor and the V_{OUT} pin with a 2.2-µF capacitor improves stability and reduces output noise. The LM4132 comes in a space-saving 5-pin SOT-23.

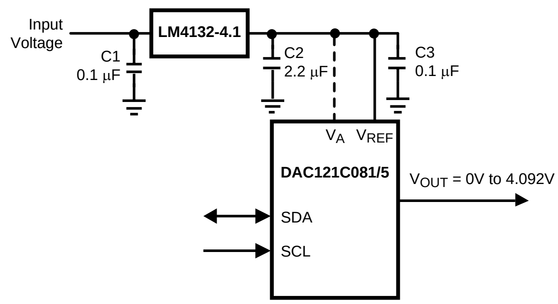


Figure 31. The LM4132 as a Power Supply

10.1.2 LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a reference for the DAC121C081. It is available in 4.096-V and 5-V versions and comes in a space-saving, 3-pin SOT-23.

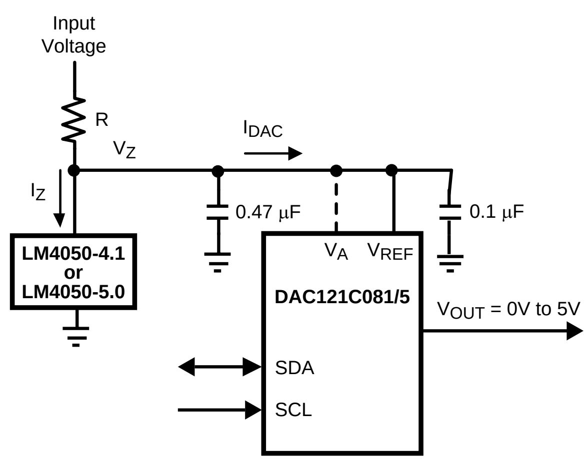


Figure 32. The LM4050 as a Power Supply

Using References as Power Supplies (continued)

The minimum resistor value in the circuit of Figure 32 must be chosen such that the maximum current through the LM4050 does not exceed its 15-mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, and the DAC121C081 drawing zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC121C081 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC121C081 draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min)) / I_Z(max)$$

where

- $V_Z(min)$ is the nominal LM4050 output voltage ± the LM4050 output tolerance over temperature.
- $I_Z(max)$ is the maximum allowable current through the LM4050. (6)

and

$$R(max) = (V_{IN}(min) - V_Z(max)) / ((I_{DAC}(max) + I_Z(min))$$

where

- $V_Z(max)$ is the nominal LM4050 output voltage ± the LM4050 output tolerance over temperature.
- $I_{DAC}(max)$ is the maximum DAC121C081 supply current.
- $I_Z(min)$ is the minimum current required by the LM4050 for proper regulation. (7)

10.1.3 LP3985

The LP3985 is a low noise, ultra low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC121C081. It comes in 3-V, 3.3-V and 5-V versions, among others, and sports a low 30-µV noise specification at low frequencies. Because low-frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

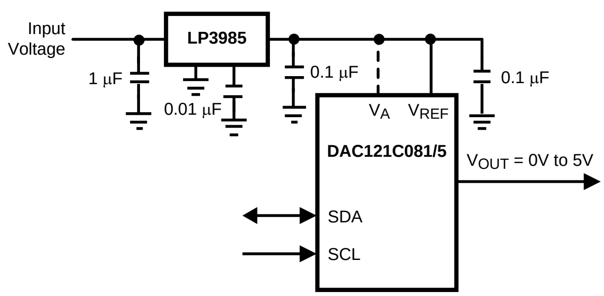


Figure 33. Using the LP3985 Regulator

An input capacitance of 1 µF without any ESR requirement is required at the LP3985 input, while a 1-µF ceramic capacitor with an ESR requirement of 5 mΩ to 500 mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

10.1.4 LP2980

The LP2980 is an ultra low dropout regulator with a 0.5% or 1% accuracy over temperature, depending upon grade. It is available in 3-V, 3.3-V, and 5-V versions, among others.

Using References as Power Supplies (continued)

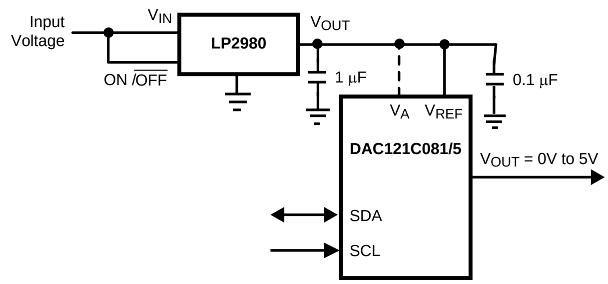


Figure 34. Using the LP2980 Regulator

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1-µF over temperature, but values of 2.2 µF or more will provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 (SNOS733) data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

11 Layout

11.1 Layout Guidelines

For best accuracy and minimum noise, the printed-circuit board containing the DAC121C081 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located on the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design uses a *fencing* technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC121C081. Special care is required to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC121C081 power supply should be bypassed with a 4.7-µF and a 0.1-µF capacitor as close as possible to the device with the 0.1 µF right at the device supply pin. The 4.7-µF capacitor should be a tantalum type and the 0.1-µF capacitor should be a low ESL, low ESR type. The power supply for the DAC121C081 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. These clock and data lines should have controlled impedances.

11.2 Layout Example

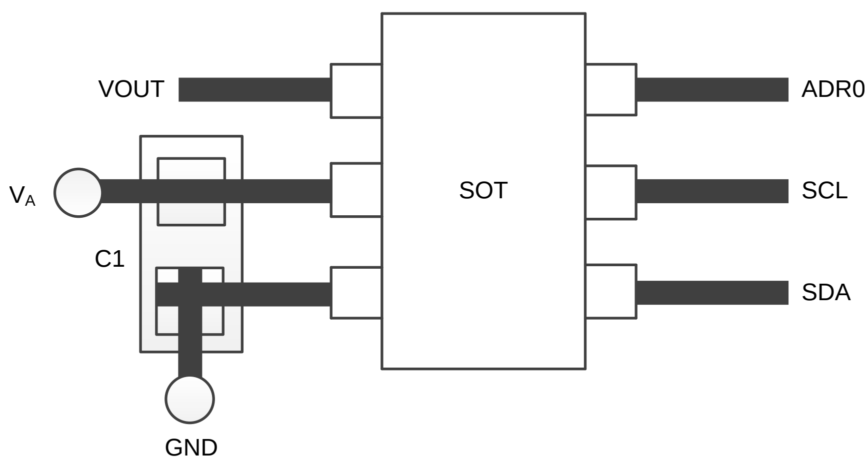


Figure 35. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの関連用語

12.1.1.1 仕様の定義

微分非直線性**(DNL)**は、理想的なステップ・サイズである1LSBからの最大偏差です。1LSBはV_{REF}/4096 = V_A/4096です。

デジタル・フィードスルーは、DACの出力が更新されないとき、デジタル入力からDACのアナログ出力へ注入されるエネルギーの測定値です。この値は、データバス上のフルスケール・コード変化を用いて測定します。

フルスケール誤差は、DACにフルスケール・コード(FFFh)をロードしたときの実際の出力電圧と、V_A × 4095/4096の値との差です。

ゲイン誤差は、伝達関数の理想カーブからの偏差です。ゼロスケール誤差とフルスケール誤差から、GE = FSE - ZEで計算できます。ここでGEはゲイン誤差、FSEはフルスケール誤差、ZEはゼロ誤差です。

グリッチ・インパルスは、DACレジスタへの入力コードが変化したとき、アナログ出力へ注入されるエネルギーです。グリッチの面積として、ナノボルト-秒単位で規定されます。

積分非直線性**(INL)**は、入力から出力への伝達関数を経由する直線に対して、各コードにどれだけの偏差があるかの測定値です。任意のコードについて、この直線からの差異は、そのコード値の中間から測定されます。エンド・ポイント法が使用されます。本製品のINLは、限られた範囲について、*Electrical Characteristics*に従って規定されます。

最下位ビット**(LSB)**は、ワード内の全ビットのうち、値または重み付けが最も小さいビットです。この値は

LSB = V_{REF} / 2^nで示されます。

ここで V_{REF}は本製品の電源電圧、*n*はDACの解像度のビット数で、DAC121C081の場合は12です。 (8)

最大負荷容量は、DACが出力の安定性を維持したまま駆動できる最大の容量です。

単調性は、入力コードが増加するときに、DACの出力が決して減少しない、単調上昇となる条件を意味します。

最上位ビット**(MSB)**は、ワード内の全ビットのうち、値や重み付けが最も大きいビットです。この値はV_Aの1/2です。

マルチプライング帯域は、DACにフルスケール・コードをロードした状態で、出力振幅がV_{REFIN}上の入力正弦波よりも3dB低くなる周波数です。

電力効率は、全消費電流に対する出力電流の比です。出力電流は、電源から供給されます。消費電流と出力電流との差は、負荷がない状態でデバイスが消費する電力です。

セトリング時間は、入力コードを更新した後、出力が最終値の1/2LSBの範囲内に落ち着くまでの時間です。

全高調波歪み**(THD)**は、V_{REFIN}に理想的な正弦波が与えられたとき、DAC出力に現れる高調波です。THDはdBで表されます。

ウェイクアップ時間は、出力がパワーダウン・モードから復帰するまでの時間です。この時間は、下位データ・バイトのACKビットにおけるSCLの立ち上がりエッジから、出力電圧がパワーダウン電圧の0Vから変化するまでの時間で測定されます。

ゼロコード誤差は、コード000hを入力したときにDAC出力に現れる出力誤差(電圧)です。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下をを参照してください:

- *『LP2980-N Micropower 50mA超低ドロップアウト、SOT-23パッケージのレギュレータ』*、SNOS733

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

関連リンク (continued)

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
DAC121C081	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DAC121C085	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 商標

I^{2}C is a registered trademark of Phillips Corporation..
All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC121C081CIMK/G4	Active	Production	SOT-23-THIN (DDC) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X84C
DAC121C081CIMK/G4.A	Active	Production	SOT-23-THIN (DDC) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X84C
DAC121C081CIMK/NO.A	Active	Production	SOT-23-THIN (DDC) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X84C
DAC121C081CIMK/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X84C
DAC121C081CISD/NO.A	Active	Production	WSON (NGF) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X87
DAC121C081CISD/NOPB	Active	Production	WSON (NGF) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X87
DAC121C081CISDX/NO.A	Active	Production	WSON (NGF) | 6	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X87
DAC121C081CISDX/NOPB	Active	Production	WSON (NGF) | 6	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X87
DAC121C085CIMM/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X90C
DAC121C085CIMM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X90C
DAC121C085CIMMX/NO.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X90C
DAC121C085CIMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X90C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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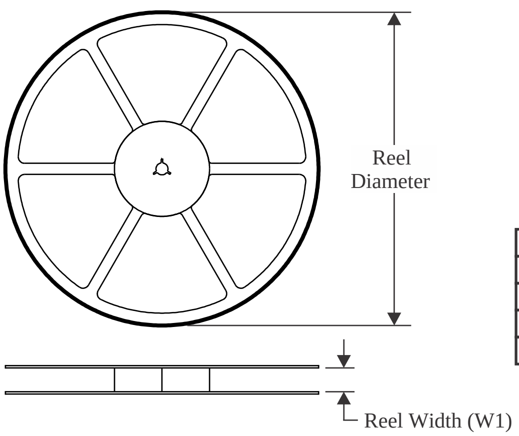
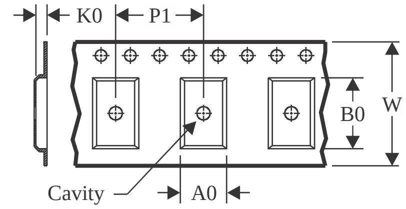
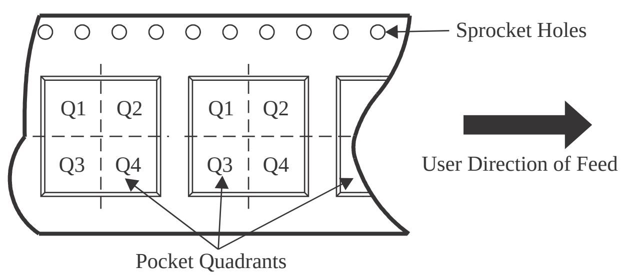
TAPE AND REEL INFORMATION





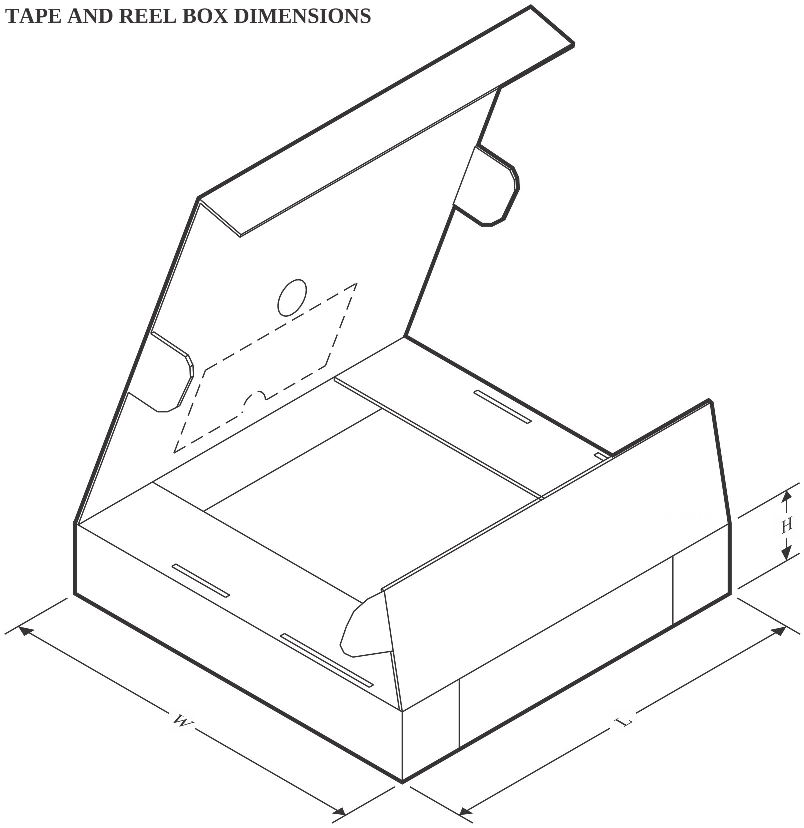
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

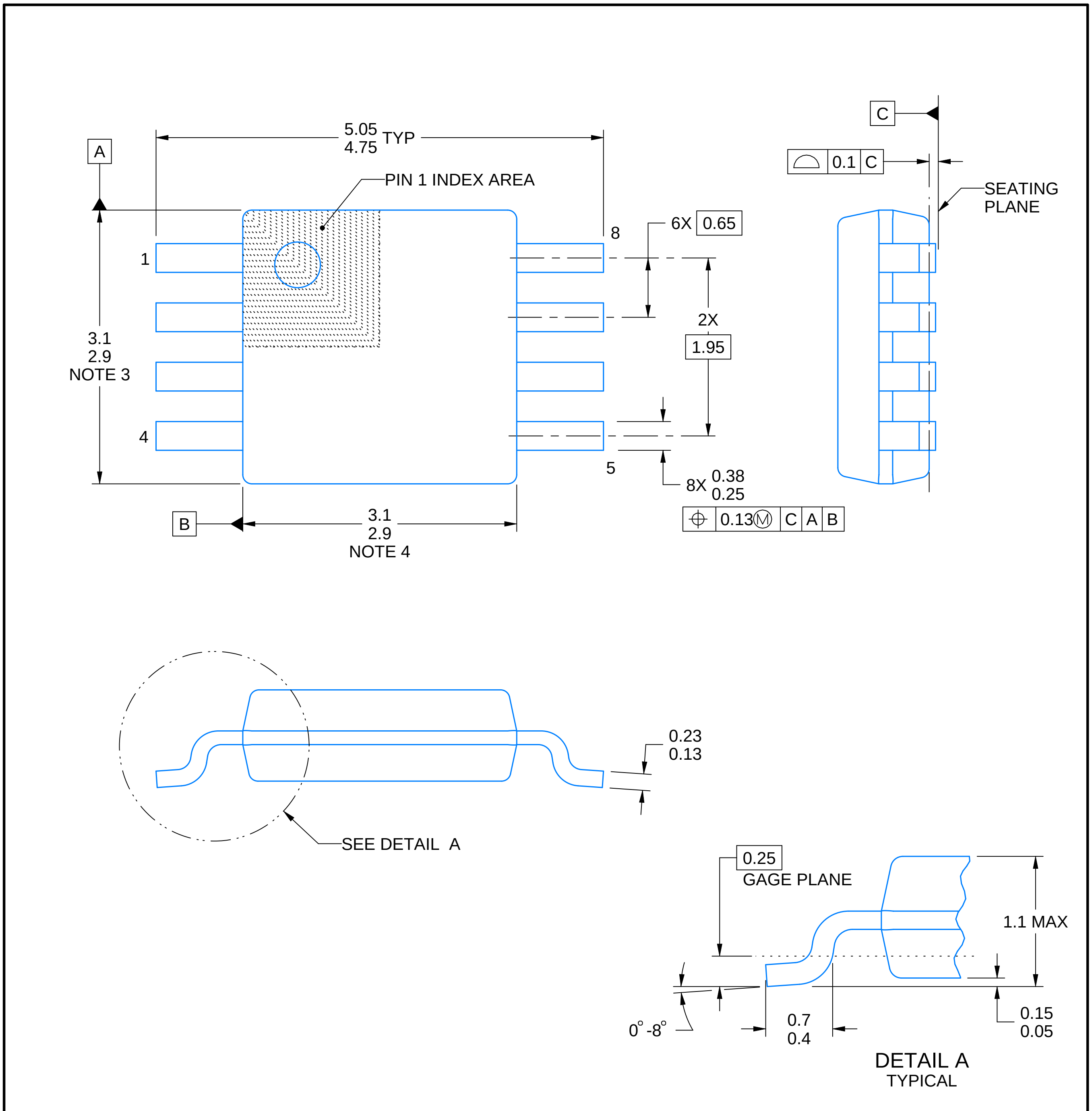
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC121C081CIMK/G4	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121C081CIMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121C081CISD/NOPB	WSON	NGF	6	1000	177.8	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC121C081CISDX/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC121C085CIMM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC121C085CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC121C081CIMK/G4	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
DAC121C081CIMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
DAC121C081CISD/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
DAC121C081CISDX/ NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
DAC121C085CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
DAC121C085CIMMX/ NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0



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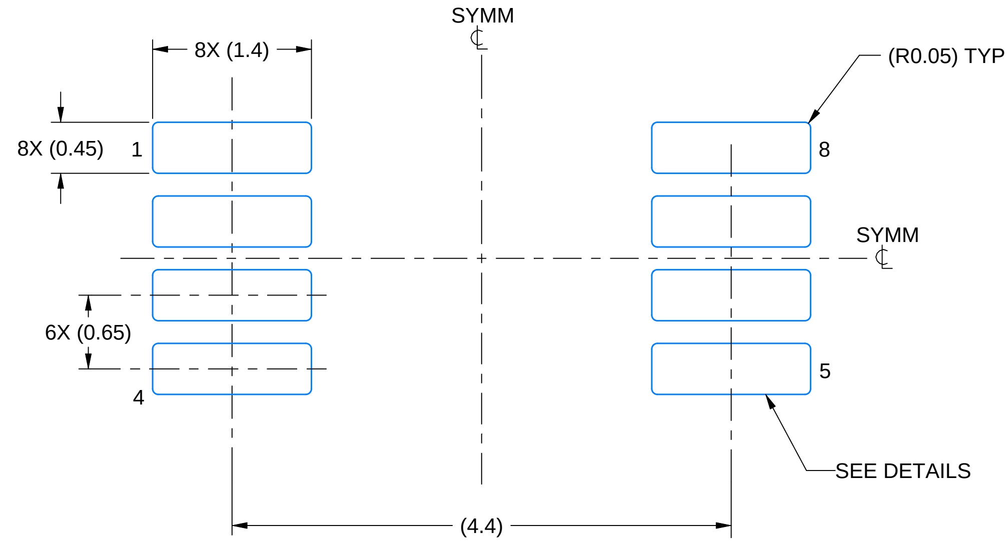
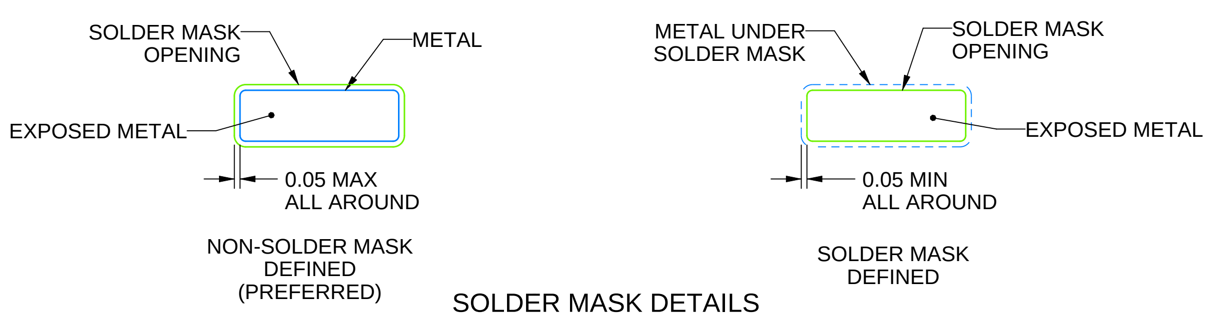
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

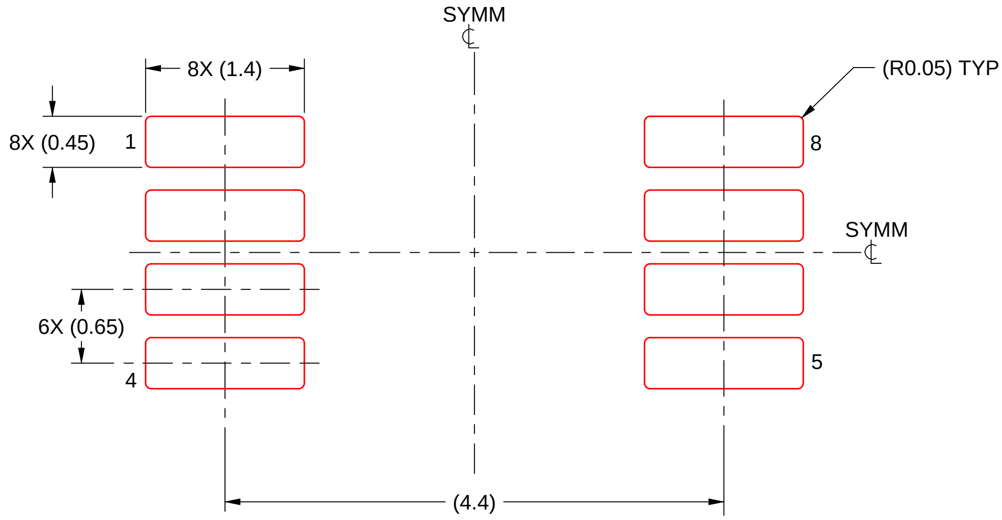


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

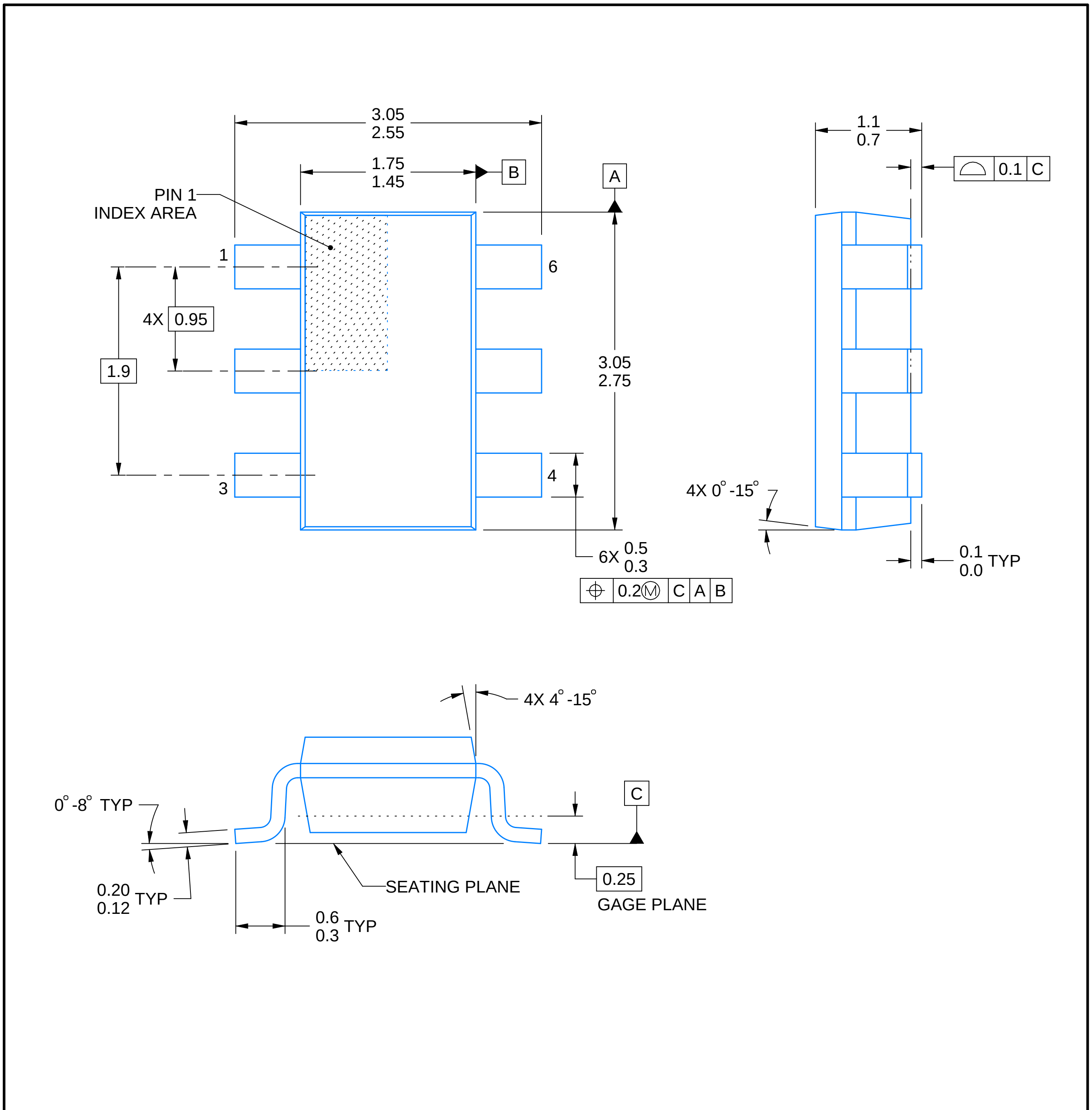


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

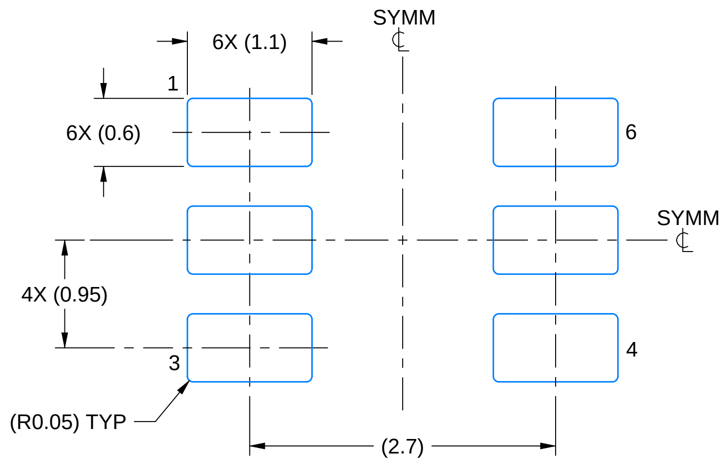
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



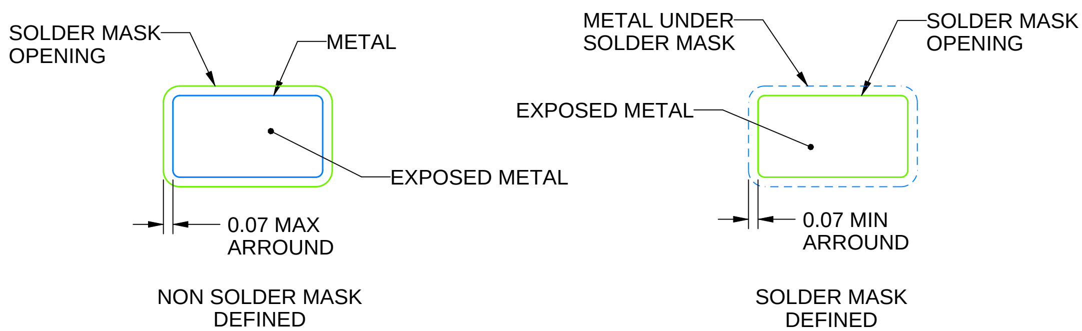
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

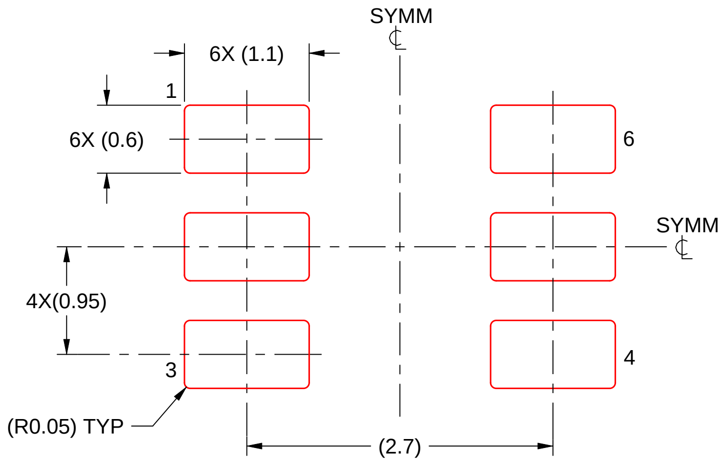


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



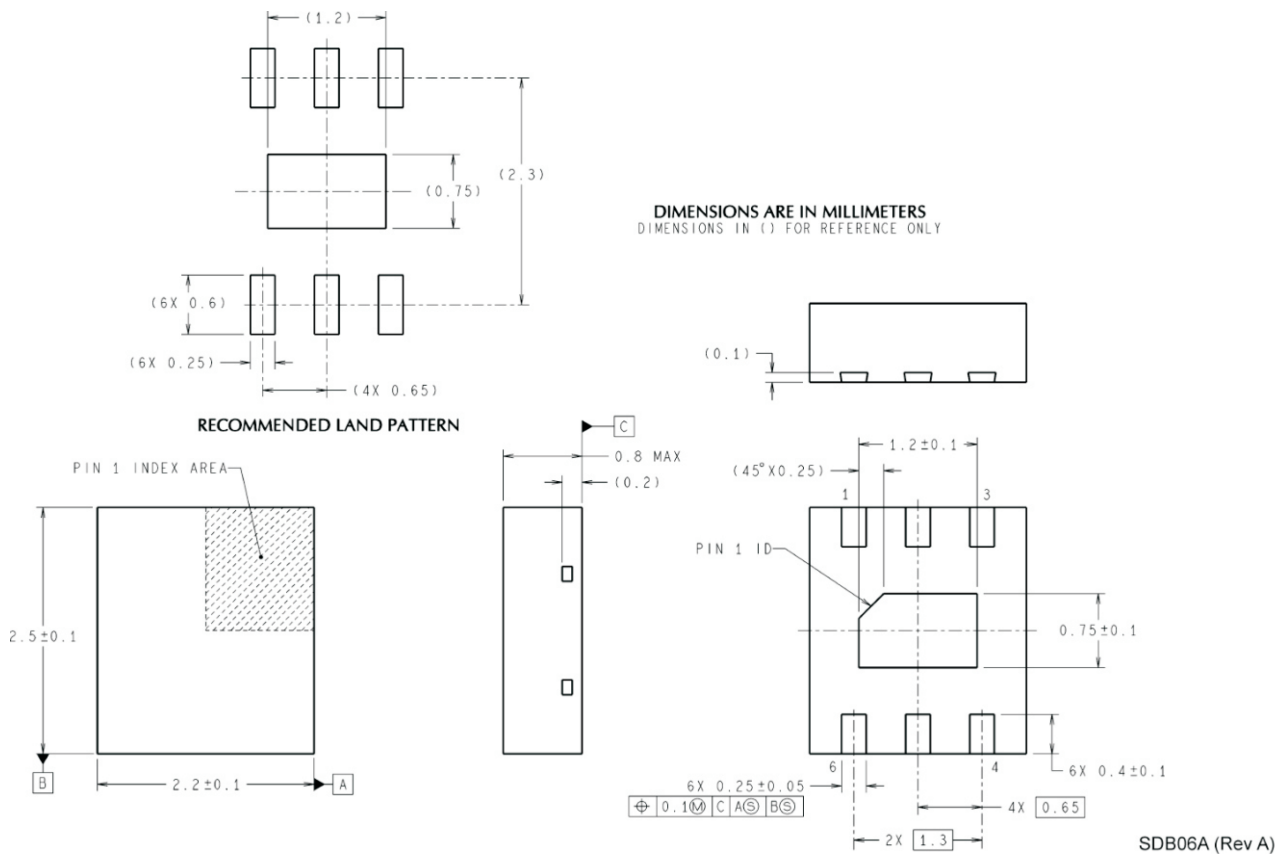
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

NGF0006A



(1.2)
(2.3)
(0.75)
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(6X 0.6)
(6X 0.25)
(4X 0.65)
RECOMMENDED LAND PATTERN
(0.1)
C
0.8 MAX
(0.2)
1.2±0.1
(45°X0.25)
PIN 1 INDEX AREA
PIN 1 ID
2.5±0.1
0.75±0.1
B
2.2±0.1
A
6X 0.4±0.1
6X 0.25±0.05
0.1 M C A S B S
4X 0.65
2X 1.3
SDB06A (Rev A)

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