JAJSAL1G – MAY 2006 – REVISED JUNE 2016

DAC082S085 8ビット、マイクロパワー、デュアル回路、レール・ツー・レール出力D/Aコンバータ

1 特長

- 単調性を保証
- 低電力動作
- レール・ツー・レール電圧出力
- パワーオン・リセット時に出力0V
- 同時出力更新
- 広い電源電圧範囲: 2.7V～5.5V
- 業界最小のパッケージ
- パワーダウン・モード
- 主な仕様
  - 分解能: 8ビット
  - INL: ±0.5LSB (最大値)
  - DNL: 0.18 / –0.13LSB (最大値)
  - セトリング時間: 4.5µs (最大値)
  - ゼロコード誤差: 15 mV (最大値)
  - フルスケール誤差: -0.75% FS (最大値)
  - 消費電力
    - 通常動作: 0.6mW (3V) / 1.6mW (5V) (標準値)
    - パワーダウン時: 0.3µW (3V) / 0.8µW (5V) (標準値)

2 アプリケーション

- バッテリ駆動計測器
- デジタル・ゲインおよびオフセットの調整
- プログラム可能な電圧源および電流源
- プログラム可能なアッテネータ

3 概要

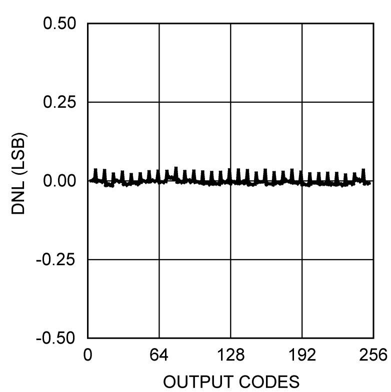
DAC082S085は、変換に必要な機能をすべて備えた汎用のデュアル、8ビット、電圧出力D/Aコンバータ(DAC)です。2.7V～5.5Vの単一電源で動作し、消費電力は3V時に0.6mW、5V時に1.6mWです。DAC082S085は10ピンのSONおよびVSSOPパッケージで供給されます。10ピンWSONパッケージを使用した場合、DAC082S085はクラス最小のデュアルDACです。オンチップの出力アンプによりレール・ツー・レール出力が可能で、3線式のシリアル・インターフェイスは電源電圧範囲の全体にわたって40MHzまでのクロック速度で動作します。競合製品は、電源電圧が2.7V～3.6Vの範囲で、クロック速度は25MHzまでに制限されています。シリアル・インターフェイスは、標準の SPI™、QSPI、MICROWIRE、DSPインターフェイスと互換性があります。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DAC082S085	VSSOP (10)	3.00mm×3.00mm
	WSON (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

V_A = 3VにおけるDNL



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (March 2013) から Revision G に変更	**Page**
• 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加	1
• Changed *Thermal Information* table	6

Revision E (March 2013) から Revision F に変更	**Page**
• Changed layout of National Data Sheet to TI format	22

5 Description (continued)

The reference for the DAC082S085 serves both channels and can vary in voltage between 1 V and V_A, providing the widest possible output dynamic range. The DAC082S085 has a 16-bit input shift register that controls the outputs to be updated, the mode of operation, the power-down condition, and the binary input data. Both outputs can be updated simultaneously or individually depending on the setting of the two mode of operation bits.

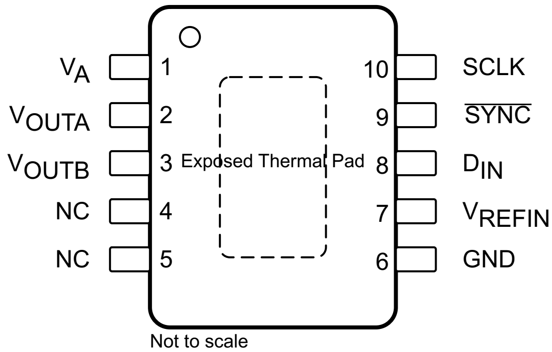
A power-on reset circuit ensures that the DAC output powers up to 0 V and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt with three different termination options.

The low power consumption and small packages of the DAC082S085 make it an excellent choice for use in battery-operated equipment.

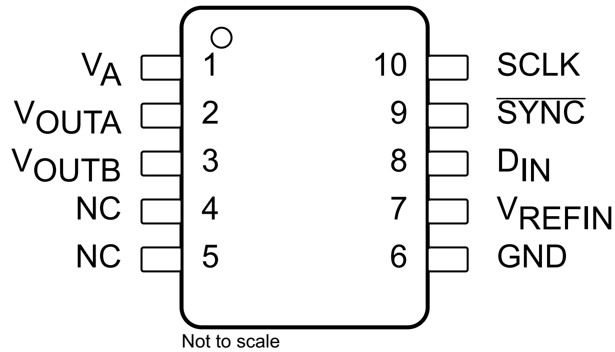
The DAC082S085 is one of a family of pin-compatible DACs, including the 10-bit DAC102S085 and the 12-bit DAC124S085. The DAC082S085 operates over the extended industrial temperature range of −40°C to 105°C.

6 Pin Configuration and Functions

DSC Package
10-Pin WSON
Top View



DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_A	Supply	Power supply input. Must be decoupled to GND.
2	V_{OUTA}	Analog Output	Channel A analog output voltage.
3	V_{OUTB}	Analog Output	Channel B analog output voltage.
4	NC	—	Not connected
5	NC	—	Not connected
6	GND	Ground	Ground reference for all on-chip circuitry.
7	V_{REFIN}	Analog Input	Unbuffered reference voltage shared by all channels. Must be decoupled to GND.
8	D_{IN}	Digital Input	Serial data input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
9	$\overline{SYNC}$	Digital Input	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
10	SCLK	Digital Input	Serial clock input. Data is clocked into the input shift register on the falling edges of this pin.
PAD	PAD	Ground	Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Supply voltage, V_A		6.5	V
Voltage on any input pin	–0.3	6.5	V
Input current at any pin(4)		10	mA
Package input current(4)		20	mA
Power consumption at T_A = 25°C	See(5)		
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds 5.5 V or is less than GND, the current at that pin must be limited to 10 mA. The 20-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A) / $R_{\theta JA}$. The values for maximum power dissipation is reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed).

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2500	V
		Machine model (MM)	±250	

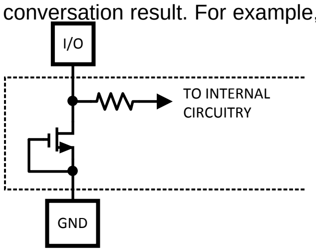
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human-body model is 100-pF capacitor discharged through a 1.5-kΩ resistor. Machine model is 220 pF discharged through 0 Ω.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Operating temperature, T_A	–40	105	°C
Supply voltage, V_A	2.7	5.5	V
Reference voltage, V_{REFIN}	1	V_A	V
Digital input voltage(2)	0	5.5	V
Output load	0	1500	pF
SCLK frequency		Up to 40	MHz

(1) All voltage are measured with respect to GND = 0 V, unless otherwise specified.
(2) The inputs are protected as shown below. Input voltage magnitudes up to 5.5 V, regardless of V_A, does not cause errors in the conversation result. For example, if V_A is 3 V, the digital input pins can be driven with a 5-V logic device.



7.4 Thermal Information

THERMAL METRIC(1)		DAC082S085 DGS (VSSOP) 10 PINS	DAC082S085 DSC (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240	250	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.3	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.9	23.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.6	23.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 3 to 252. All limits are at T_A = 25°C, unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
STATIC PERFORMANCE								
	Resolution	$T_{MIN} \le T_A \le T_{MAX}$			8			Bits
	Monotonicity	$T_{MIN} \le T_A \le T_{MAX}$			8			Bits
INL	Integral non-linearity	T_A = 25°C				±0.14		LSB
		$T_{MIN} \le T_A \le T_{MAX}$					±0.5	
DNL	Differential non-linearity	V_A = 2.7 V to 5.5 V	T_A = 25°C	Max		0.04		LSB
				Min		−0.02		
			$T_{MIN} \le T_A \le T_{MAX}$		−0.13		0.18	
ZE	Zero code error	I_{OUT} = 0	T_A = 25°C			4		mV
			$T_{MIN} \le T_A \le T_{MAX}$				15	
FSE	Full-scale error	I_{OUT} = 0	T_A = 25°C			−0.1		%FSR
			$T_{MIN} \le T_A \le T_{MAX}$				−0.75	
GE	Gain error	All ones Loaded to DAC register	T_A = 25°C			−0.2		%FSR
			$T_{MIN} \le T_A \le T_{MAX}$			−1		
ZCED	Zero code error drift					−20		µV/°C
TC GE	Gain error tempco	V_A = 3 V				−0.7		ppm/°C
		V_A = 5 V				–1		
OUTPUT CHARACTERISTICS								
	Output voltage(3)	$T_{MIN} \le T_A \le T_{MAX}$			0		V_{REFIN}	V
I_{OZ}	High-impedance output leakage current(3)	$T_{MIN} \le T_A \le T_{MAX}$					±1	µA
ZCO	Zero code output	V_A = 3 V, I_{OUT} = 200 µA				1.3		mV
		V_A = 3 V, I_{OUT} = 1 mA				6		
		V_A = 5 V, I_{OUT} = 200 µA				7		
		V_A = 5 V, I_{OUT} = 1 mA				10		
FSO	Full-scale output	V_A = 3 V, I_{OUT} = 200 µA				2.984		V
		V_A = 3 V, I_{OUT} = 1 mA				2.934		
		V_A = 5 V, I_{OUT} = 200 µA				4.989		
		V_A = 5 V, I_{OUT} = 1 mA				4.958		
I_{OS}	Output short-circuit current (source)	V_A = 3 V, V_{OUT} = 0 V, Input Code = FFh				–56		mA
		V_A = 5 V, V_{OUT} = 0 V, Input Code = FFh				–69		
	Output short-circuit current (sink)	V_A = 3 V, V_{OUT} = 3 V, Input Code = 00h				52		mA
		V_A = 5 V, V_{OUT} = 5 V, Input Code = 00h				75		
I_O	Continuous output current(3)	Available on each DAC output	$T_{MIN} \le T_A \le T_{MAX}$				11	mA
C_L	Maximum load capacitance	R_L = ∞				1500		pF
		R_L = 2 kΩ				1500		

(1) To ensure accuracy, it is required that V_A and V_{REFIN} be well bypassed.
(2) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(3) This parameter is specified by design or characterization and is not tested in production.

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 3 to 252. All limits are at T_A = 25°C, unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
Z_{OUT}	DC output impedance					7.5		Ω
REFERENCE INPUT CHARACTERISTICS								
VREFIN	Input range minimum	T_A = 25°C				0.2		V
		$T_{MIN} \le T_A \le T_{MAX}$			1			V
	Input range maximum	$T_{MIN} \le T_A \le T_{MAX}$					V_A	V
	Input impedance					60		kΩ
LOGIC INPUT CHARACTERISTICS								
I_{IN}	Input current[3]	$T_{MIN} \le T_A \le T_{MAX}$					±1	µA
V_{IL}	Input low voltage[3]	V_A = 3 V		T_A = 25°C		0.9		V
				$T_{MIN} \le T_A \le T_{MAX}$			0.6	
		V_A = 5 V		T_A = 25°C		1.5		
				$T_{MIN} \le T_A \le T_{MAX}$			0.8	
V_{IH}	Input high voltage[3]	V_A = 3 V		T_A = 25°C		1.4		V
				$T_{MIN} \le T_A \le T_{MAX}$	2.1			
		V_A = 5 V		T_A = 25°C		2.1		
				$T_{MIN} \le T_A \le T_{MAX}$	2.4			
C_{IN}	Input capacitance[3]	$T_{MIN} \le T_A \le T_{MAX}$					3	pF
POWER REQUIREMENTS								
V_A	Supply voltage minimum	$T_{MIN} \le T_A \le T_{MAX}$			2.7			V
	Supply voltage maximum	$T_{MIN} \le T_A \le T_{MAX}$					5.5	
I_N	Normal supply current (output unloaded)	f_{SCLK} = 30 MHz	V_A = 2.7 V to 3.6 V	T_A = 25°C		210		µA
				$T_{MIN} \le T_A \le T_{MAX}$			270	
			V_A = 4.5 V to 5.5 V	T_A = 25°C		320		
				$T_{MIN} \le T_A \le T_{MAX}$			410	
		f_{SCLK} = 0	V_A = 2.7 V to 3.6 V			190		
			V_A = 4.5 V to 5.5 V			290		
I_{PD}	Power down supply current (output unloaded, SYNC = DIN = 0 V after PD mode loaded)	All PD Modes[3]	V_A = 2.7 V to 3.6 V	T_A = 25°C		0.1		µA
				$T_{MIN} \le T_A \le T_{MAX}$			1	
			V_A = 4.5 V to 5.5 V	T_A = 25°C		0.15		µA
				$T_{MIN} \le T_A \le T_{MAX}$			1	
P_N	Normal supply power (output unloaded)	f_{SCLK} = 30 MHz	V_A = 2.7 V to 3.6 V	T_A = 25°C		0.6		mW
				$T_{MIN} \le T_A \le T_{MAX}$			1	
			V_A = 4.5 V to 5.5 V	T_A = 25°C		1.6		
				$T_{MIN} \le T_A \le T_{MAX}$			2.3	
		f_{SCLK} = 0	V_A = 2.7 V to 3.6 V			0.6		
			V_A = 4.5 V to 5.5 V			1.5		
P_{PD}	Power down supply current (output unloaded, SYNC = DIN = 0 V after PD mode loaded)	All PD Modes[3]	V_A = 2.7 V to 3.6 V	T_A = 25°C		0.3		µW
				$T_{MIN} \le T_A \le T_{MAX}$			3.6	
			V_A = 4.5 V to 5.5 V	T_A = 25°C		0.8		
				$T_{MIN} \le T_A \le T_{MAX}$			5.5	

7.6 Timing Requirements

The following specifications apply for V_A = +2.7V to +5.5V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 3 to 252. All other limits are at T_A = 25°C, unless otherwise specified. (1)

				MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency	T_A = 25°C			40		MHz
		$T_{MIN} \le T_A \le T_{MAX}$				30	
t_s	Output voltage settling time(2)	40h to C0h code change R_L = 2 kΩ, C_L = 200 pF	T_A = 25°C		3		µs
			$T_{MIN} \le T_A \le T_{MAX}$			4.5	
SR	Output slew rate				1		V/µs
	Glitch Impulse	Code change from 80h to 7Fh			12		nV-sec
	Digital feedthrough				0.5		nV-sec
	Digital crosstalk				1		nV-sec
	DAC-to-DAC crosstalk				3		nV-sec
	Multiplying bandwidth	V_{REFIN} = 2.5 V ± 0.1 Vpp			160		kHz
	Total harmonic distortion	V_{REFIN} = 2.5 V ± 1 Vpp input frequency = 10 kHz			70		dB
t_{WU}	Wake-up time	V_A = 3 V			6		µs
		V_A = 5 V			39		
$1/f_{SCLK}$	SCLK cycle time	T_A = 25°C			25		ns
		$T_{MIN} \le T_A \le T_{MAX}$		33			
t_{CH}	SCLK high time	T_A = 25°C			7		ns
		$T_{MIN} \le T_A \le T_{MAX}$		10			
t_{CL}	SCLK low time	T_A = 25°C			7		ns
		$T_{MIN} \le T_A \le T_{MAX}$		10			
t_{SS}	$\overline{SYNC}$ setup time prior to SCLK falling edge	T_A = 25°C			4		ns
		$T_{MIN} \le T_A \le T_{MAX}$		10			
t_{DS}	Data setup time prior to SCLK falling edge	T_A = 25°C			1.5		ns
		$T_{MIN} \le T_A \le T_{MAX}$		3.5			
t_{DH}	Data hold time after SCLK falling edge	T_A = 25°C			1.5		ns
		$T_{MIN} \le T_A \le T_{MAX}$		3.5			
t_{CFSR}	SCLK fall prior to rise of $\overline{SYNC}$	T_A = 25°C			0		ns
		$T_{MIN} \le T_A \le T_{MAX}$		3			
t_{SYNC}	$\overline{SYNC}$ high time	T_A = 25°C			6		ns
		$T_{MIN} \le T_A \le T_{MAX}$		10			

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(2) This parameter is specified by design or characterization and is not tested in production.

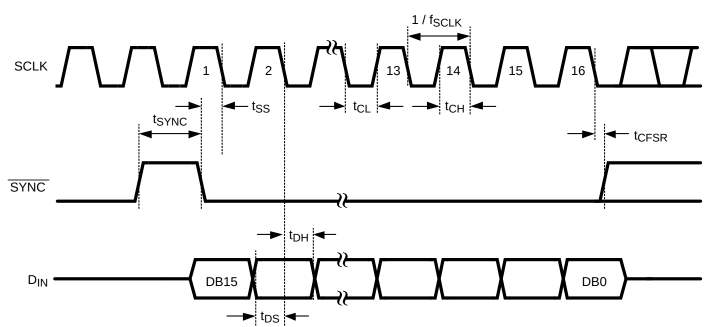


Figure 1. Serial Timing Diagram

7.7 Typical Characteristics

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 3 to 252, unless otherwise stated

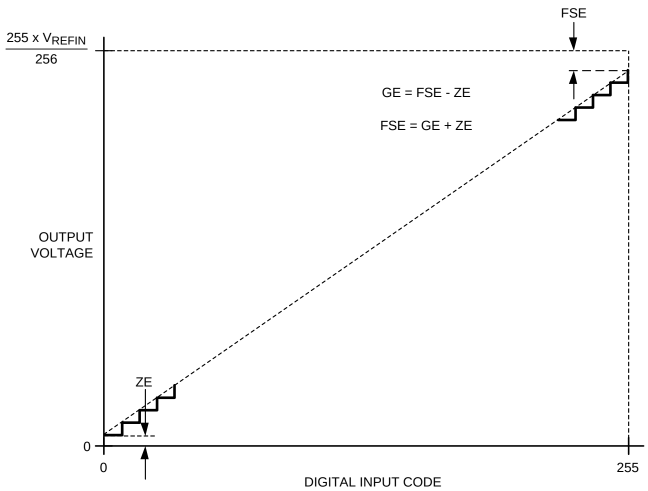


Figure 2. Input and Output Transfer Characteristic

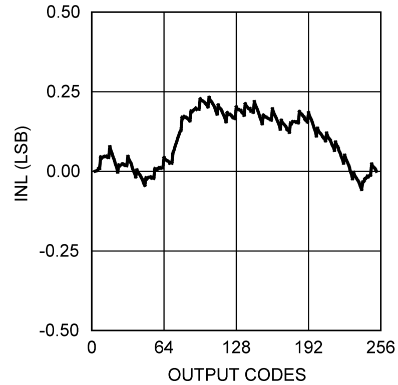


Figure 3. INL at V_A = 3 V

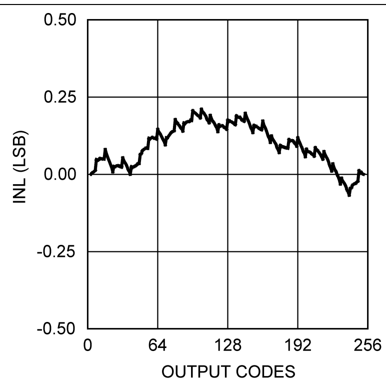


Figure 4. INL at V_A = 5 V

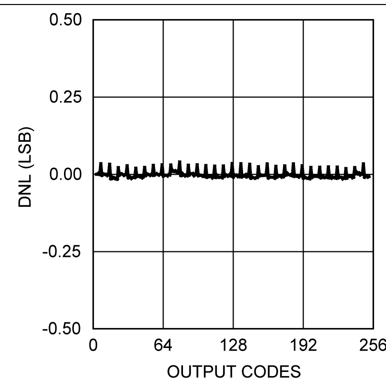


Figure 5. DNL at V_A = 3 V

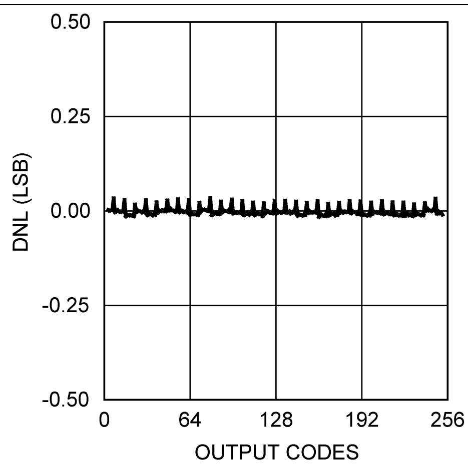


Figure 6. DNL at V_A = 5 V

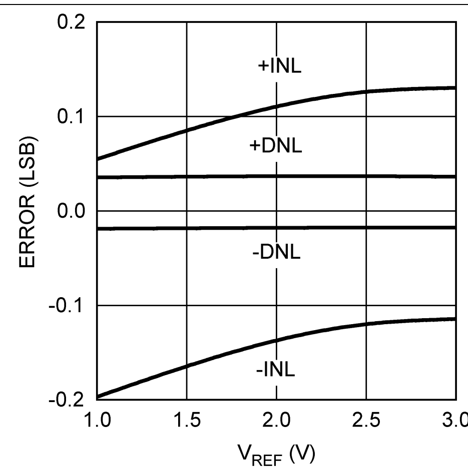


Figure 7. INL/DNL vs V_{REFIN} at V_A = 3 V

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 3 to 252, unless otherwise stated

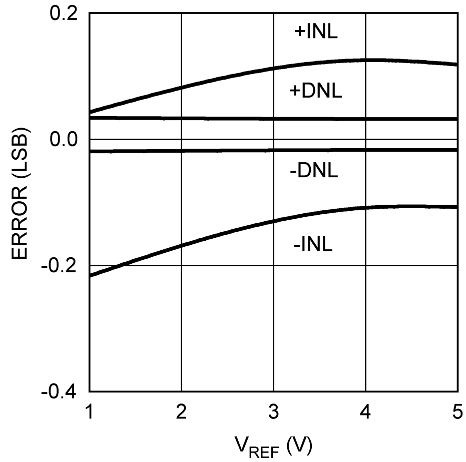


Figure 8. INL/DNL vs V_{REFIN} at V_A = 5 V

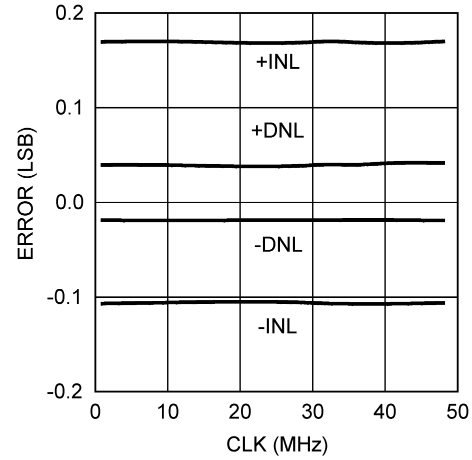


Figure 9. INL/DNL vs f_{SCLK} at V_A = 2.7 V

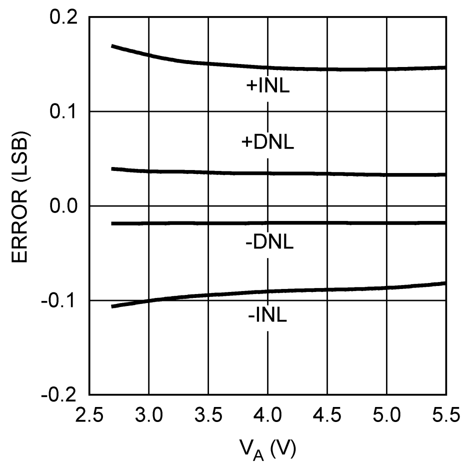


Figure 10. INL/DNL vs V_A

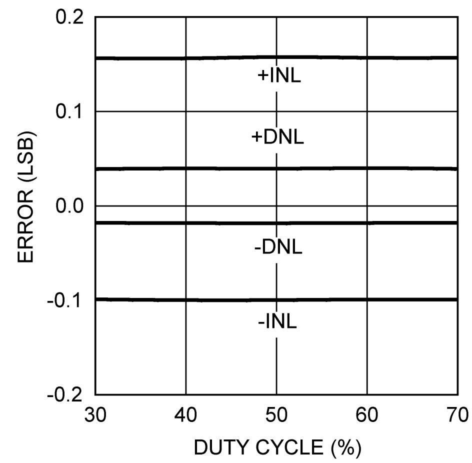


Figure 11. INL/DNL vs Clock Duty Cycle at V_A = 3 V

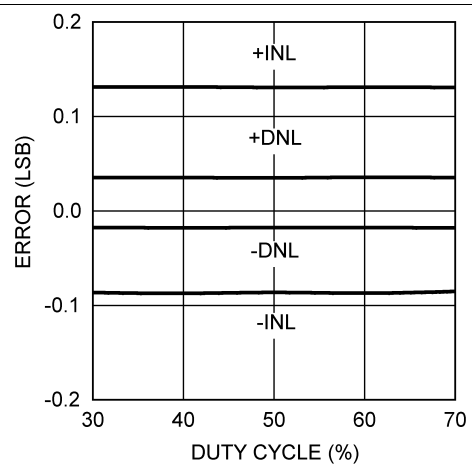


Figure 12. INL/DNL vs Clock Duty Cycle at V_A = 5 V

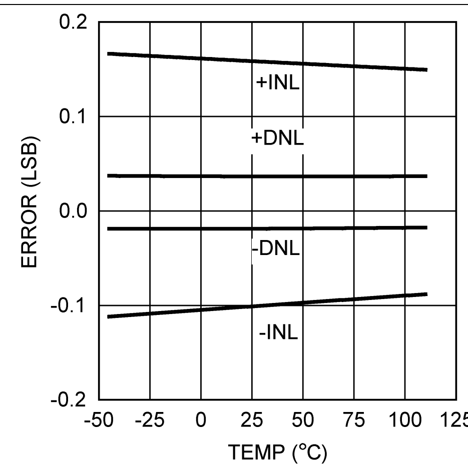


Figure 13. INL/DNL vs Temperature at V_A = 3 V

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 3 to 252, unless otherwise stated

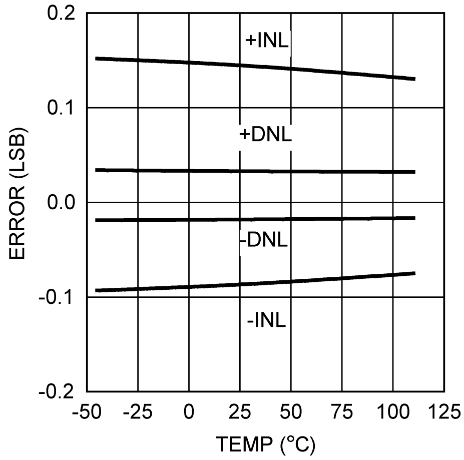


Figure 14. INL/DNL vs Temperature at V_A = 5 V

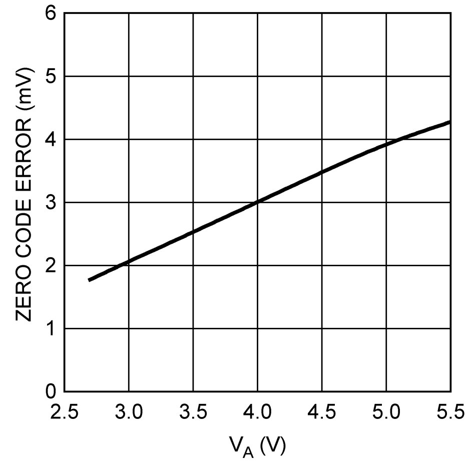


Figure 15. Zero Code Error vs V_A

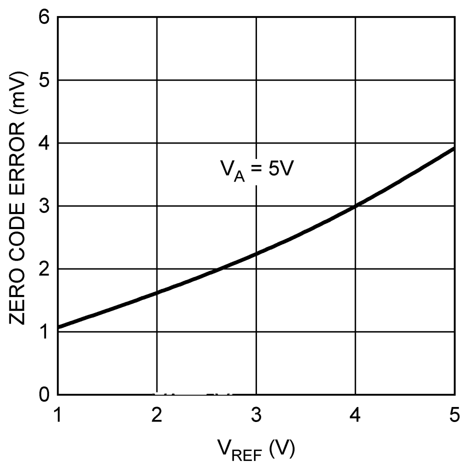


Figure 16. Zero Code Error vs V_{REFIN}

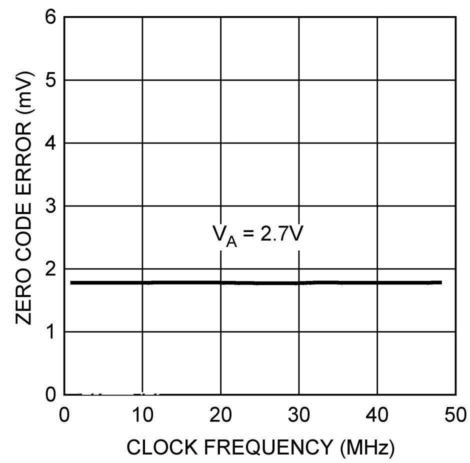


Figure 17. Zero Code Error vs f_{SCLK}

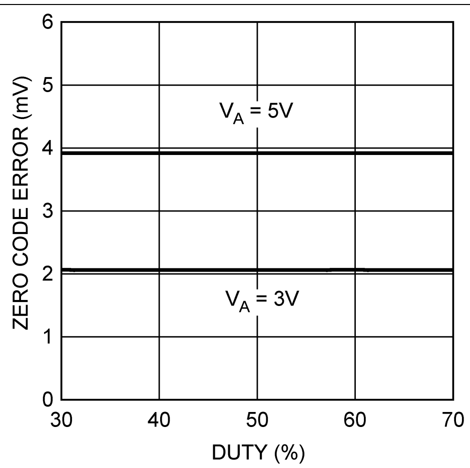


Figure 18. Zero Code Error vs Clock Duty Cycle

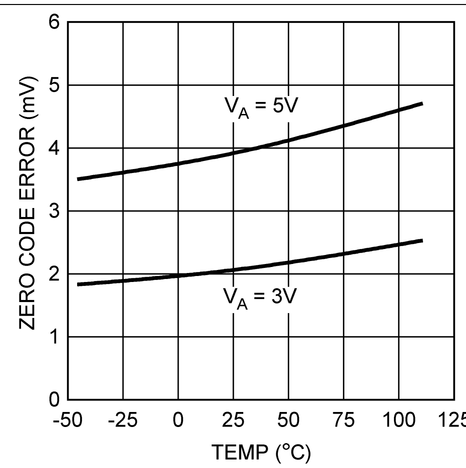


Figure 19. Zero Code Error vs Temperature

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 3 to 252, unless otherwise stated

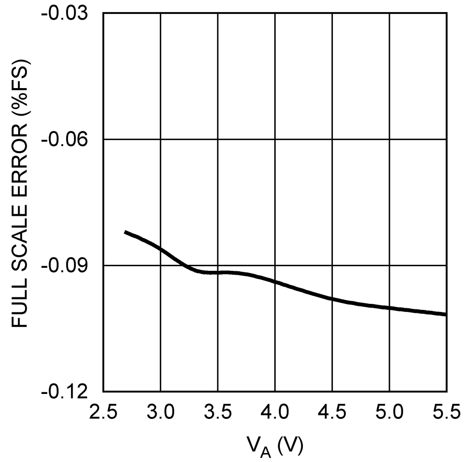


Figure 20. Full-Scale Error vs V_A

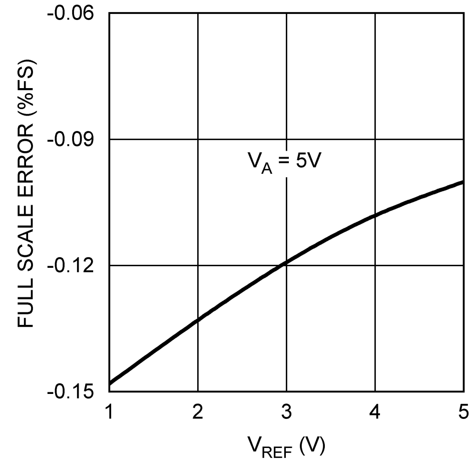


Figure 21. Full-Scale Error vs V_{REFIN}

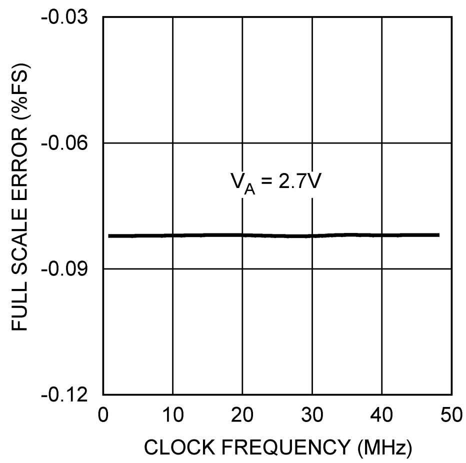


Figure 22. Full-Scale Error vs f_{SCLK}

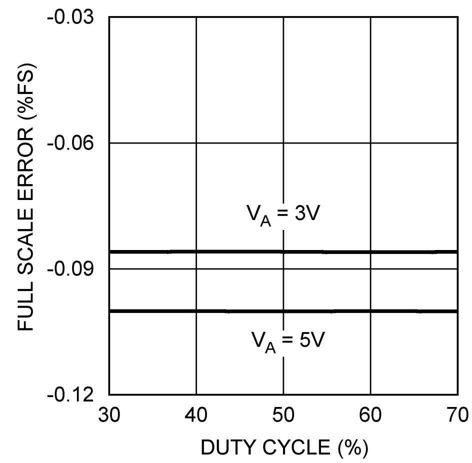


Figure 23. Full-Scale Error vs Clock Duty Cycle

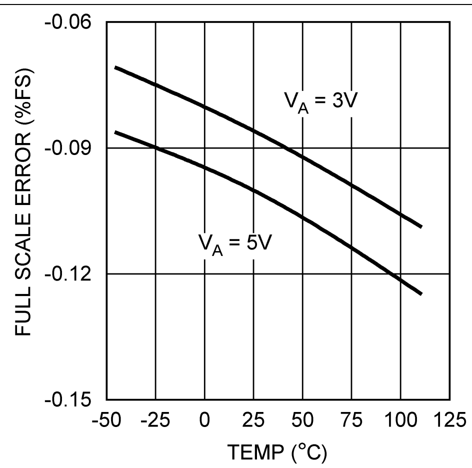


Figure 24. Full-Scale Error vs Temperature

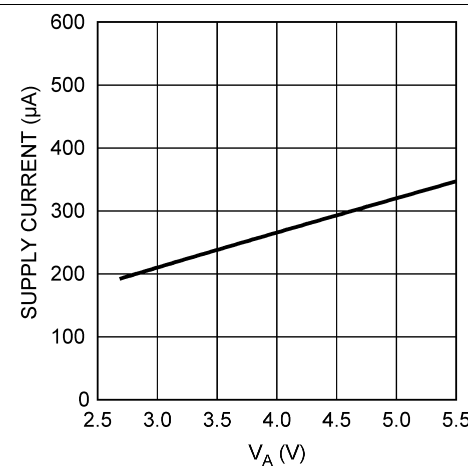


Figure 25. Supply Current vs V_A

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 3 to 252, unless otherwise stated

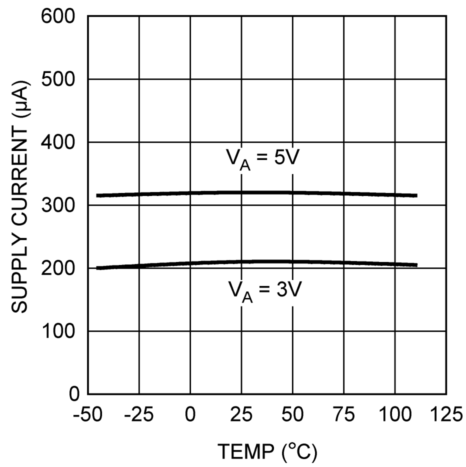


Figure 26. Supply Current vs Temperature

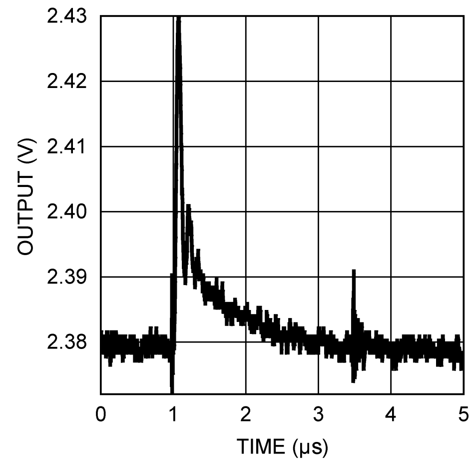


Figure 27. 5-V Glitch Response

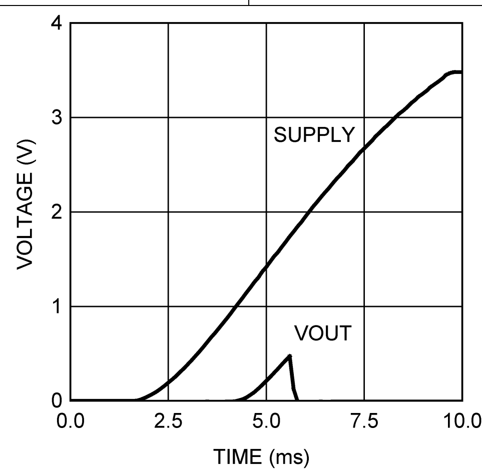


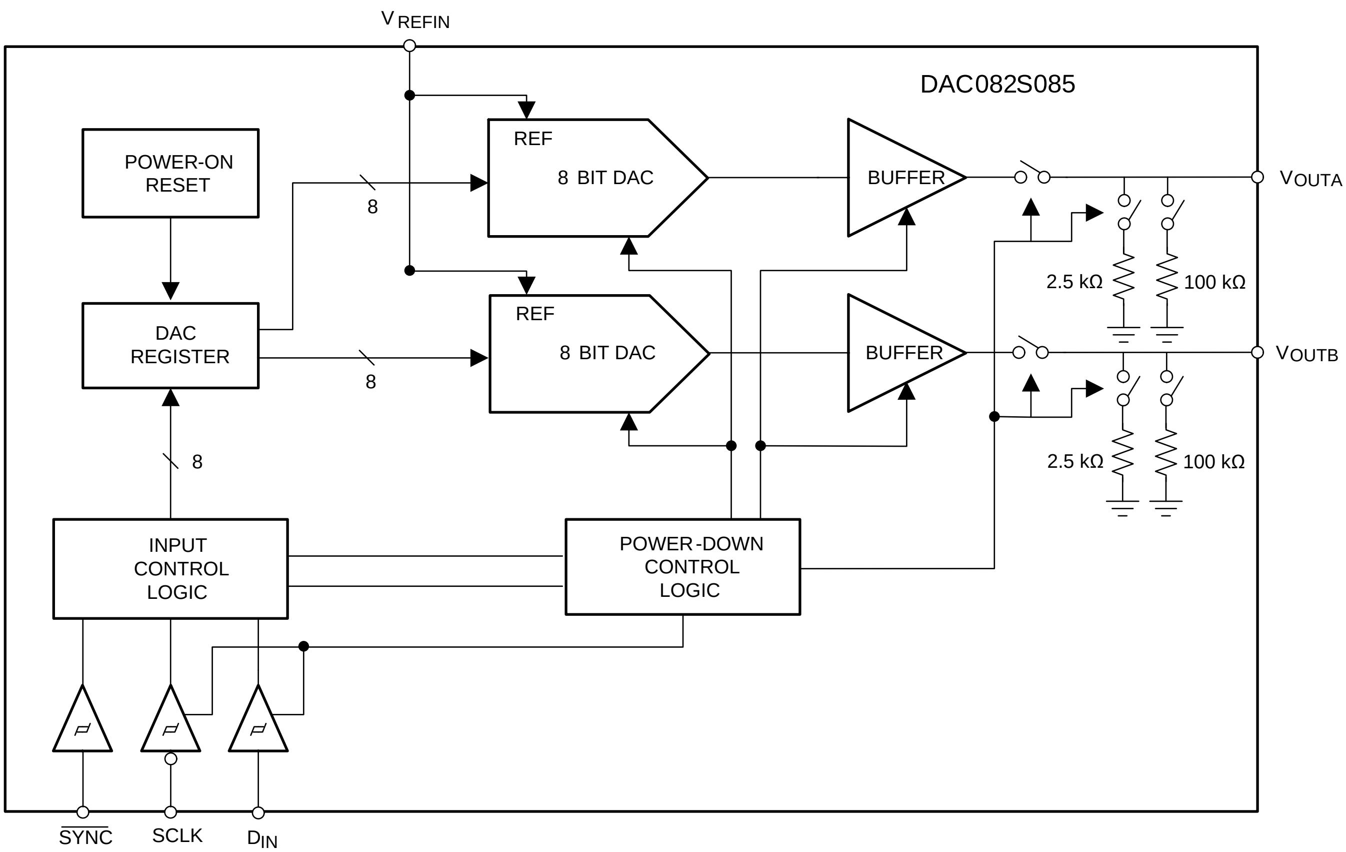
Figure 28. Power-On Reset

8 Detailed Description

8.1 Overview

The DAC082S085 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer.

8.2 Functional Block Diagram



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8.2.1 Feature Description

8.2.1.1 DAC Architecture

The DAC082S085 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer. The reference voltage is externally applied at V_{REFIN} and is shared by both DACs.

For simplicity, a single resistor string is shown in Figure 29. This string consists of 256 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage calculated in Equation 1:

$$V_{OUTA,B} = V_{REFIN} \times (D / 256)$$

where

- D is the decimal equivalent of the binary code that is loaded into the DAC register. (D can take on any value between 0 and 255. This configuration ensures that the DAC is monotonic.) (1)

Functional Block Diagram (continued)

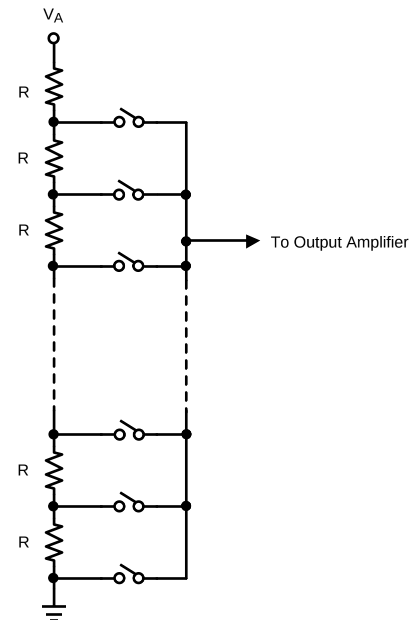

Figure 29. DAC Resistor String

8.2.1.2 Output Amplifiers

The output amplifiers are rail-to-rail, providing an output voltage range of 0 V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes. The output capabilities of the amplifier are described in *Electrical Characteristics*.

The output amplifiers are capable of driving a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the *Electrical Characteristics*.

8.2.1.3 Reference Voltage

The DAC082S085 uses a single external reference that is shared by both channels. The reference pin, V_{REFIN}, is not buffered and has an input impedance of 60 kΩ. TI recommends that V_{REFIN} be driven by a voltage source with low output impedance. The reference voltage range is 1 V to V_A, providing the widest possible output dynamic range.

8.2.1.4 Power-On Reset

The power-on reset circuit controls the output voltages of both DACs during power-up. Upon application of power, the DAC registers are filled with zeros and the output voltages are 0 V. The outputs remain at 0 V until a valid write sequence is made to the DAC.

8.3 Device Functional Modes

8.3.1 Power-Down Modes

The DAC082S085 has four power-down modes, two of which are identical. In power-down mode, the supply current drops to 20 µA at 3 V and 30 µA at 5 V. The DAC082S085 is set in power-down mode by setting OP1 and OP0 to 11. Because this mode powers down both DACs, the first two bits of the shift register are used to select different output terminations for the DAC outputs. Setting A1 and A0 to 00 or 11 causes the outputs to be tri-stated (a high impedance state). While setting A1 and A0 to 01 or 10 causes the outputs to be terminated by 2.5 kΩ or 100 kΩ to ground respectively (see Table 1).

Device Functional Modes (continued)

Table 1. Power-Down Modes

A1	A0	OP1	OP0	OPERATING MODE
0	0	1	1	High-Z outputs
0	1	1	1	2.5 kΩ to GND
1	0	1	1	100 kΩ to GND
1	1	1	1	High-Z outputs

The bias generator, output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC registers are unaffected when in power-down. Each DAC register maintains its value prior to the DAC082S085 being powered down unless it is changed during the write sequence which instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with $\overline{\text{SYNC}}$ and D_{IN} idled low and SCLK disabled. The time to exit power-down (Wake-Up Time) is typically t_{WU} µs as stated in *Timing Requirements*.

8.4 Programming

8.4.1 Serial Interface

The three-wire interface is compatible with SPI™, QSPI, and MICROWIRE, as well as most DSPs and operates at clock rates up to 40 MHz. See Figure 1 for information on a write sequence.

A write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Once $\overline{\text{SYNC}}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid misclocking data into the shift register, it is critical that $\overline{\text{SYNC}}$ not be brought low simultaneously with a falling edge of SCLK (see Figure 1). On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the DAC channel address, mode of operation or register contents) is executed. At this point the $\overline{\text{SYNC}}$ line may be kept low or brought high. Any data and clock pusles after the 16th falling clock edge are ignored. In either case, $\overline{\text{SYNC}}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{\text{SYNC}}$.

Because the $\overline{\text{SYNC}}$ and D_{IN} buffers draw more current when they are high, they must be idled low between write sequences to minimize power consumption.

8.4.2 Input Shift Register

The input shift register, Figure 30, has sixteen bits. The first bit must be set to 0 and the second bit is an address bit. The address bit determines whether the register data is for DAC A or DAC B. This bit is followed by two bits that determine the mode of operation (writing to a DAC register without updating the outputs of both DACs, writing to a DAC register and updating the outputs of both DACs, writing to the register of both DACs and updating their outputs, or powering down both outputs). The final twelve bits of the shift register are the data bits. The data format is straight binary (MSB first, LSB last), with all 0s corresponding to an output of 0 V and all 1s corresponding to a full-scale output of V_{REFIN} – 1 LSB. The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See Figure 1.

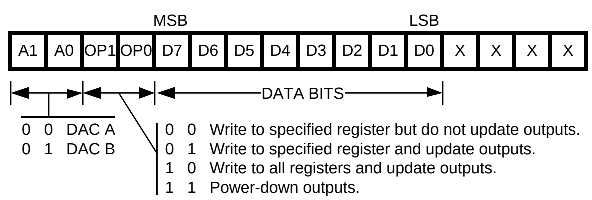

Figure 30. Input Register Contents

Normally, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, the data transfer to the shift register is aborted and the write sequence is invalid. Under this condition, the DAC register is not updated and there is no change in the mode of operation or in the DAC output voltages.

Programming (continued)

8.4.3 DSP and Microprocessor Interfacing

Interfacing the DAC082S085 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

8.4.3.1 ADSP-2101/ADSP2103 Interfacing

Figure 31 shows a serial interface between the DAC082S085 and the ADSP-2101/ADSP2103. The DSP must be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and must be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the TX register after the SPORT mode has been enabled.

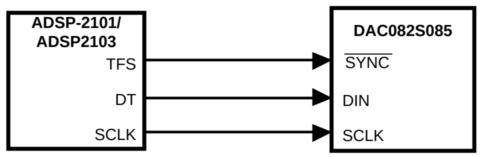

Figure 31. ADSP-2101/2103 Interface

8.4.3.2 80C51/80L51 Interface

A serial interface between the DAC082S085 and the 80C51/80L51 microcontroller is shown in Figure 32. The $\overline{\text{SYNC}}$ signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is transmitted to the DAC082S085. Because the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the DAC082S085 requires data with the MSB first.

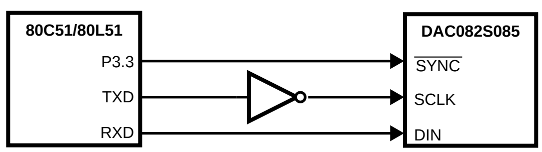

Figure 32. 80C51/80L51 Interface

8.4.3.3 68HC11 Interface

A serial interface between the DAC082S085 and the 68HC11 microcontroller is shown in Figure 33. The $\overline{\text{SYNC}}$ line of the DAC082S085 is driven from a port line (PC7 in the figure), similar to the 80C51/80L51.

The 68HC11 must be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 must be raised to end the write sequence.

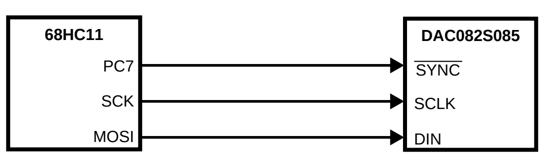

Figure 33. 68HC11 Interface

Programming (continued)

8.4.3.4 Microwire Interface

Figure 34 shows an interface between a Microwire-compatible device and the DAC082S085. Data is clocked out on the rising edges of the SK signal. As a result, the SK of the Microwire device must be inverted before driving the SCLK of the DAC082S085.

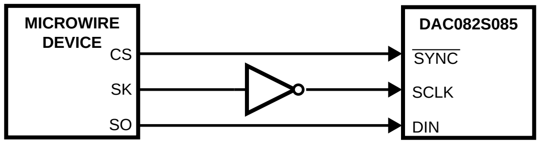

Figure 34. Microwire Interface

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DAC082S085 is designed for single-supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 35. This circuit provides an output voltage range of ±5 V. A rail-to-rail amplifier must be used if the amplifier supplies are limited to ±5 V.

9.2 Typical Application

9.2.1 Bipolar Operation

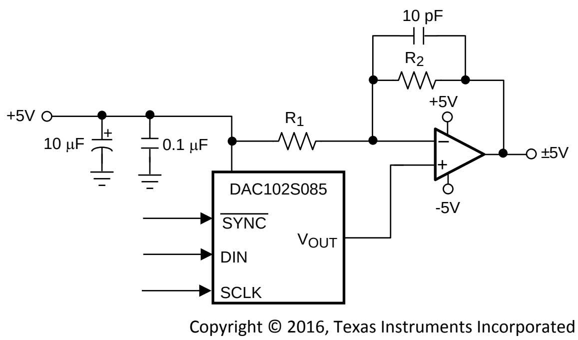

Figure 35. Bipolar Operation

9.2.1.1 Design Requirements

- The DAC082S085 uses a single supply.
- The output is required to be bipolar with a voltage range of ±5 V.
- Dual supplies are used for the output amplifier.

Typical Application (continued)

9.2.1.2 Detailed Design Procedure

The output voltage of this circuit for any code is found to be

$V_O = (V_A \times (D / 256) \times ((R1 + R2) / R1) – V_A \times R2 / R1)$ (2)

$V_O = (10 \times D / 256) – 5\ V$

where

- D is the input code in decimal form (With V_A = 5 V and R1 = R2) (3)

Table 2 lists the rail-to-rail amplifiers suitable for this application.

Table 2. Some Rail-to-Rail Amplifiers

AMP	PKGS	TYP V_{OS}	TYP I_{SUPPLY}
LMC7111	8-pin PDIP, 5-pin SOT-23	0.9 mV	25 µA
LM7301	8-pin SO, 5-pin SOT-23	0.03 mV	620 µA
LM8261	5-pin SOT-23	0.7 mV	1 mA

9.2.1.3 Application Curve

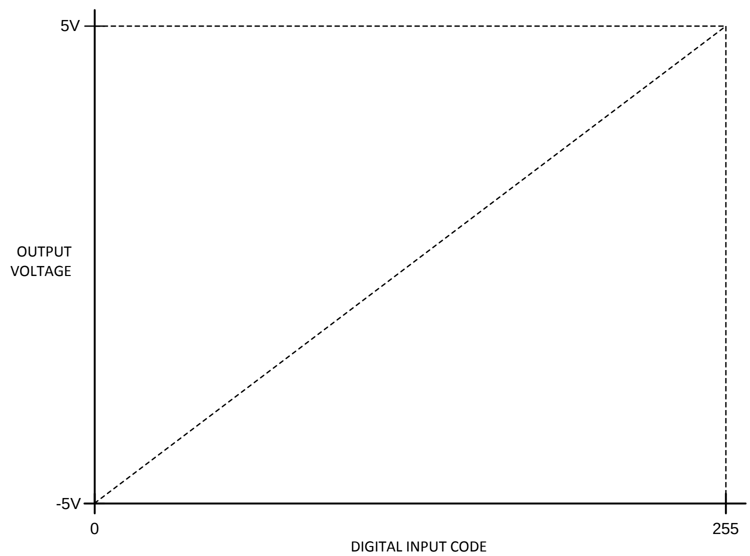

Figure 36. Bipolar Input / Output Transfer Characteristic

10 Power Supply Recommendations

While the simplicity of the DAC082S085 implies ease of use, it is important to recognize that the path from the reference input (V_{REFIN}) to the VOUTs has essentially zero Power Supply Rejection Ratio (PSRR). Therefore, it is necessary to provide a noise-free supply voltage to V_{REFIN}. To use the full dynamic range of the DAC082S085, the supply pin (V_A) and V_{REFIN} can be connected together and share the same supply voltage.

10.1 Using References as Power Supplies

Because the DAC082S085 consumes very little power, a reference source may be used as the reference input or the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used. Listed below are a few reference and power supply options for the DAC082S085.

Using References as Power Supplies (continued)

10.1.1 LM4130

The LM4130, with its 0.05% accuracy over temperature, is a good choice as a reference source for the DAC082S085. The 4.096-V version is useful if a 0 to 4.095-V output range is desirable or acceptable. Bypassing the LM4130 VIN pin with a 0.1-µF capacitor and the VOUT pin with a 2.2-µF capacitor improves stability and reduces output noise. The LM4130 comes in a space-saving, 5-pin SOT-23.

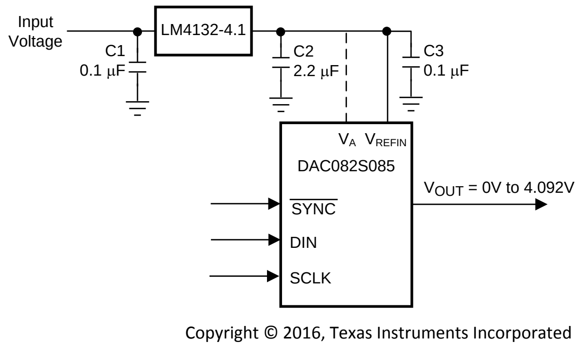

Figure 37. The LM4130 as a Power Supply

10.1.2 LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a reference for the DAC082S085. It is available in 4.096-V and 5-V versions and comes in a space-saving, 3-pin SOT-23.

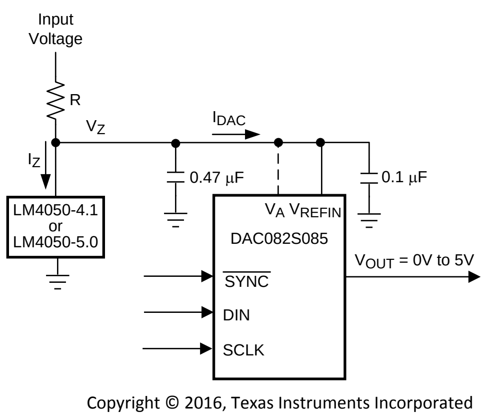

Figure 38. The LM4050 as a Power Supply

The minimum resistor value in the circuit of Figure 38 must be chosen such that the maximum current through the LM4050 does not exceed its 15-mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, and the DAC082S085 drawing zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC082S085 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC082S085 draws its maximum current. These conditions can be summarized in Equation 4 and Equation 5:

$$R(min) = (V_{IN}(max) - V_Z(min)) / I_Z(max) \quad (4)$$

$$R(max) = (V_{IN}(min) - V_Z(max)) / ((I_{DAC}(max) + I_Z(min))$$

where

- $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature

Using References as Power Supplies (continued)

- I_Z(max) is the maximum allowable current through the LM4050
- I_Z(min) is the minimum current required by the LM4050 for proper regulation
- I_{DAC}(max) is the maximum DAC082S085 supply current (5)

10.1.3 LP3985

The LP3985 is a low-noise, ultra-low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC082S085. It comes in 3-V, 3.3-V, and 5-V versions, among others, and sports a low 30-µV noise specification at low frequencies. Because low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving, 5-pin SOT-23 and 5-bump DSBGA packages.

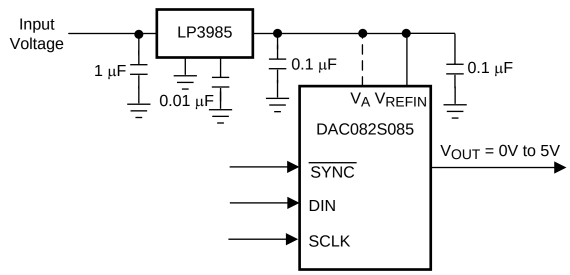

Figure 39. Using the LP3985 Regulator

An input capacitance of 1 µF without any ESR requirement is required at the LP3985 input, while a 1-µF ceramic capacitor with an ESR requirement of 5 mΩ to 500 mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

10.1.4 LP2980

The LP2980 is an ultra-low dropout regulator with a 0.5% or 1% accuracy over temperature, depending upon grade. It is available in 3-V, 3.3-V, and 5-V versions, among others.

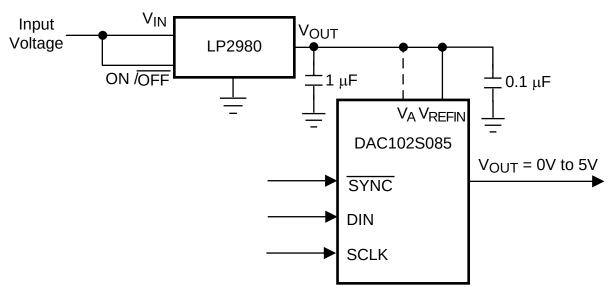

Figure 40. Using the LP2980 Regulator

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1-µF over temperature, but values of 2.2 µF or more provide even better performance. The ESR of this capacitor must be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

11 Layout

11.1 Layout Guidelines

For best accuracy and minimum noise, the printed-circuit board containing the DAC082S085 must have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes must be placed in the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design uses a *fencing* technique to prevent the mixing of analog and digital ground current. Separate ground planes must only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC082S085. Take special care to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC082S085 power supply must be bypassed with a 10-µF and a 0.1-µF capacitor as close as possible to the device with the 0.1 µF right at the device supply pin. The 10-µF capacitor must be a tantalum type and the 0.1-µF capacitor must be a low ESL, low ESR type. The power supply for the DAC082S085 must only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines must have controlled impedances.

11.2 Layout Example

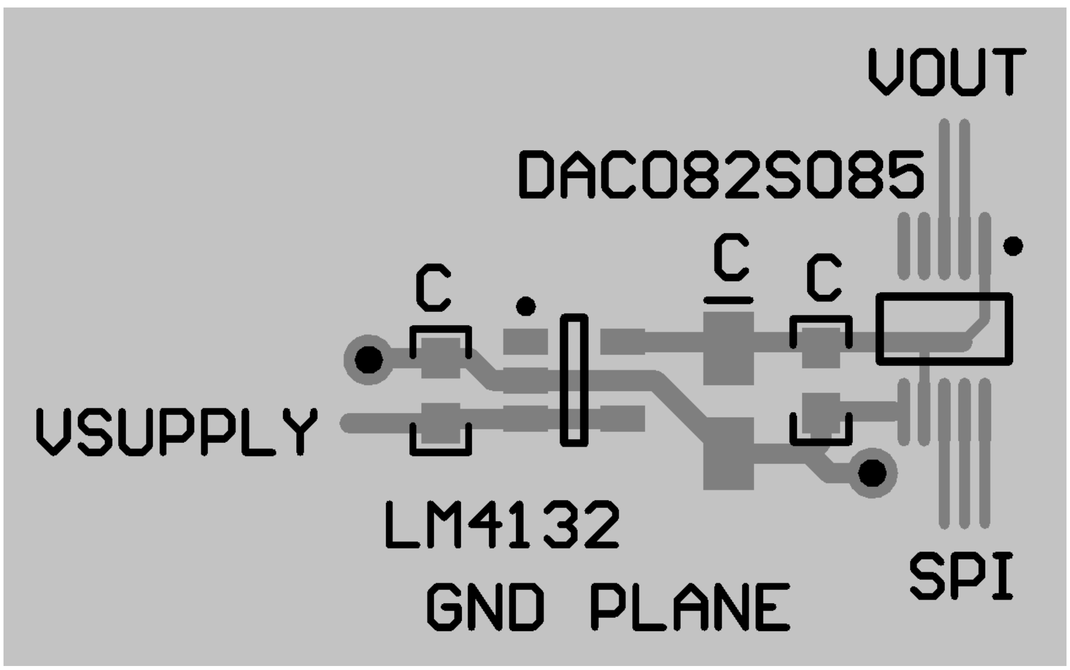

Figure 41. DAC082S085 Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの関連用語

12.1.1.1 仕様の定義

微分非直線性**(DNL)**は、理想的なステップ・サイズである1LSBからの最大偏差です。1LSBはV_{REF}/256 = V_A/256です。

DAC間クロストークは、他のDACの出力がフルスケールで変化したとき、別のDAC出力に伝達されるグリッチ・インパルスです。

デジタル・クロストークは、他のDACの入力レジスタがフルスケールで変化したとき、変換スケールの中点で別のDAC出力に伝達されるグリッチ・インパルスです。

デジタル・フィードスルーは、DAC出力が更新されないとき、デジタル入力からDACのアナログ出力へ注入されるエネルギーの測定値です。この値は、データバス上のフルスケール・コード変化を用いて測定します。

フルスケール誤差は、DACにフルスケール・コード(FFFh)をロードしたときの実際の出力電圧と、V_A × 255/256の値との差です。

ゲイン誤差は、伝達関数の理想カーブからの偏差です。ゼロスケール誤差とフルスケール誤差から、GE = FSE - ZEで計算できます。ここでGEはゲイン誤差、FSEはフルスケール誤差、ZEはゼロ誤差です。

グリッチ・インパルスは、DACレジスタへの入力コードが変化したとき、アナログ出力へ注入されるエネルギーです。グリッチの面積として、ナノボルト-秒単位で規定されます。

積分非直線性**(INL)**は、入力から出力への伝達関数を経由する直線に対して、各コードにどれだけの偏差があるかの測定値です。特定のコードについて、この直線からの差異は、そのコード値の中間から測定されます。エンド・ポイント法が使用されます。本製品のINLは、限られた範囲について、電気的特性表に従って規定されます。

最下位ビット**(LSB)**は、ワード内の全ビットのうち、値または重み付けが最も小さいビットです。この値は

$LSB = V_{REF} / 2^n$で示されます。

ここで

- V_{REF}は本製品の電源電圧です。
- nはDACの分解能(ビット数)で、DAC082S085では8です。 (6)

最大負荷容量は、DACが出力の安定性を維持したまま駆動できる最大の容量です。

単調性は、入力コードが増加するときに、DACの出力が決して減少しない、単調上昇となる条件を意味します。

最上位ビット**(MSB)**は、ワード内の全ビットのうち、値や重み付けが最も大きいビットです。この値はV_Aの1/2です。

マルチプライング帯域は、DACにフルスケール・コードをロードした状態で、出力振幅がV_{REFIN}上の入力正弦波よりも3dB低くなる周波数です。

電力効率は、全消費電流に対する出力電流の比です。出力電流は、電源から供給されます。消費電流と出力電流との差は、負荷がない状態でデバイスが消費する電力です。

セトリング時間は、入力コードを更新した後、出力が最終値の1/2LSBの範囲内に落ち着くまでの時間です。

全高調波歪み**(THD)**は、V_{REFIN}に理想的な正弦波が与えられたとき、DAC出力に現れる高調波です。THDはdBで表されます。

ウェイクアップ時間は、出力がパワーダウン・モードから復帰するまでの時間です。16番目のSCLKパルスの立ち下がりエッジから、出力電圧がパワーダウン電圧0Vから変化するまでの時間です。

ゼロコード誤差は、コード000hを入力したときにDAC出力に現れるる出力誤差(電圧)です。

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

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12.5 静電気放電に関する注意事項

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC082S085CIMM/NO.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X76C
DAC082S085CIMM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X76C
DAC082S085CIMMX/NO.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X76C
DAC082S085CIMMX/NOPB	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X76C
DAC082S085CISD/NO.A	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X77C
DAC082S085CISD/NOPB	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X77C
DAC082S085CISDX/NO.A	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X77C
DAC082S085CISDX/NOPB	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X77C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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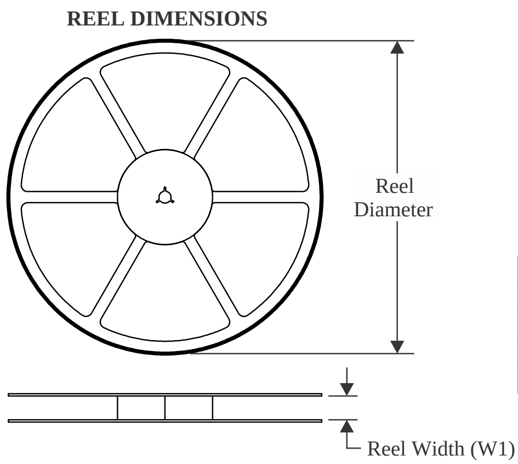
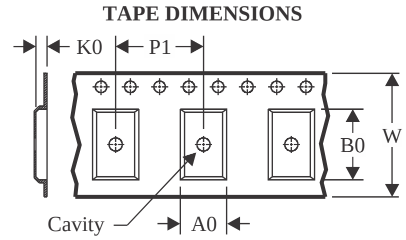
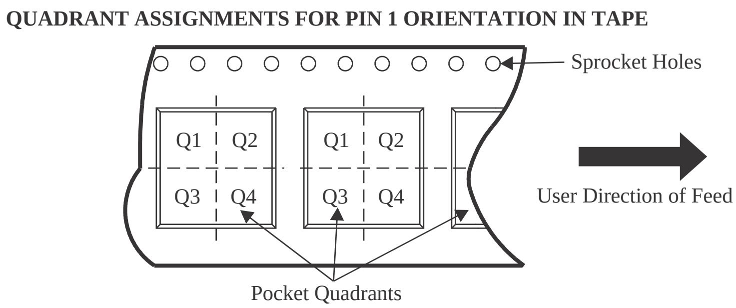
TAPE AND REEL INFORMATION





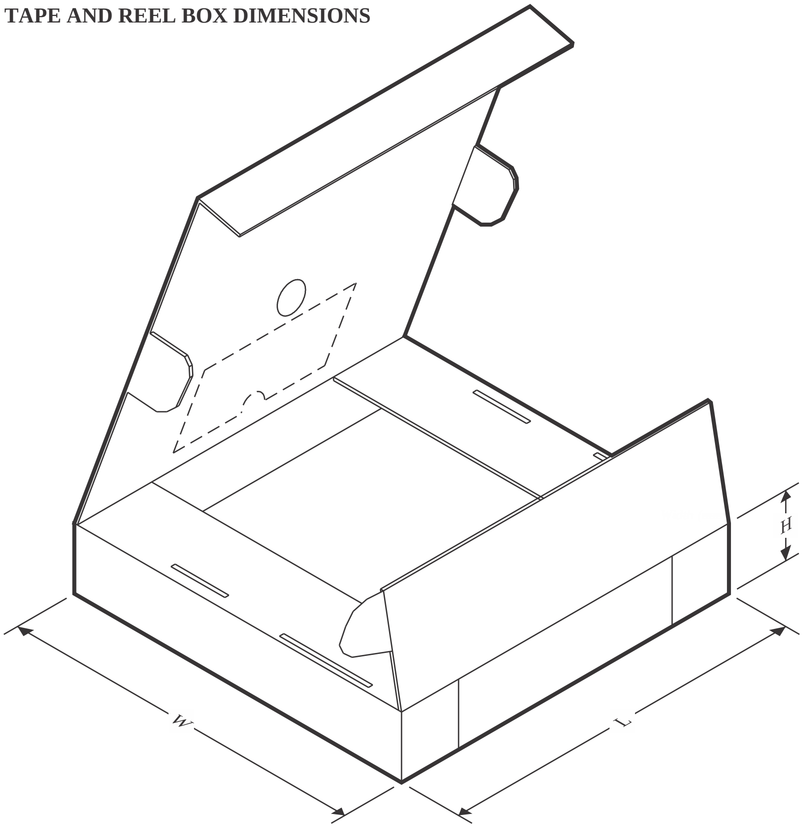
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC082S085CIMM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC082S085CIMMX/ NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC082S085CISD/NOPB	WSON	DSC	10	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DAC082S085CISDX/ NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

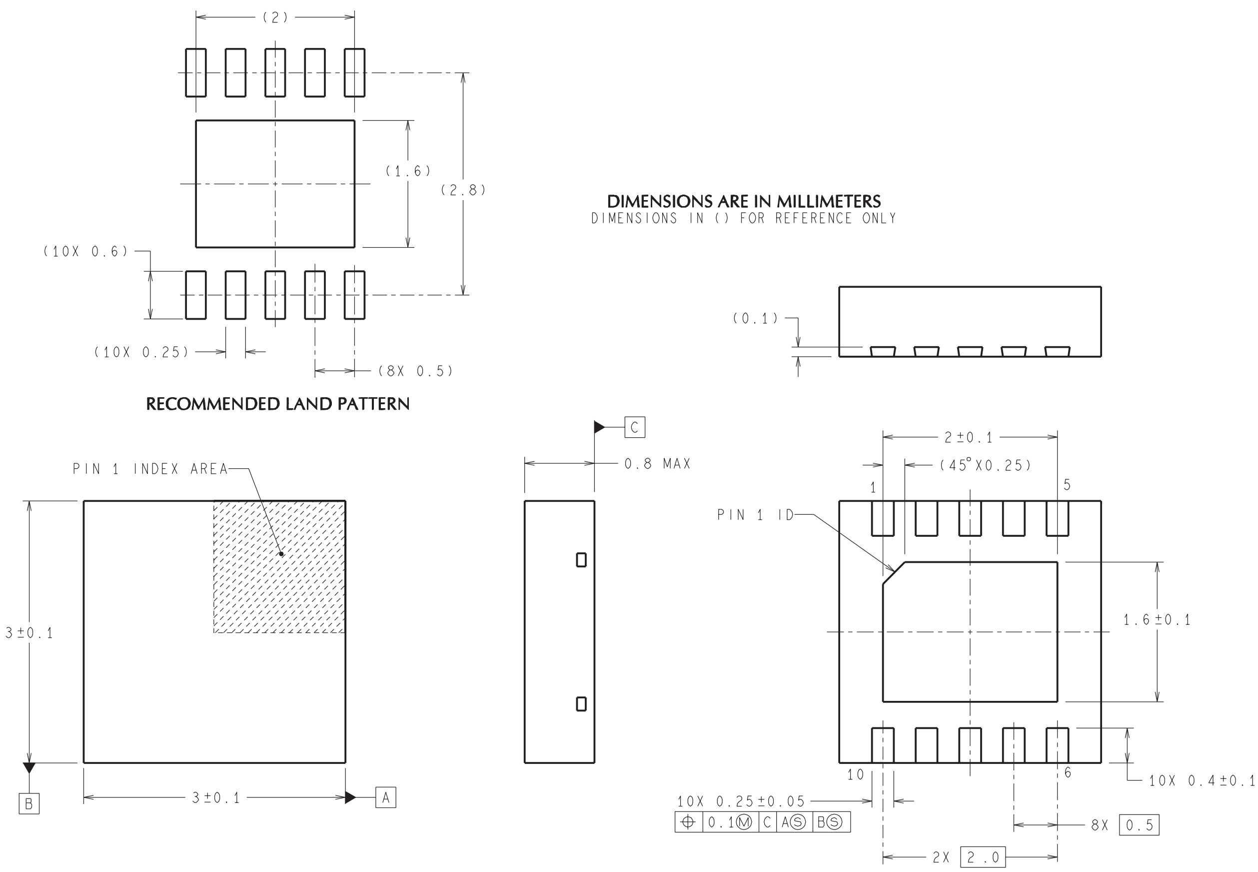
TAPE AND REEL BOX DIMENSIONS



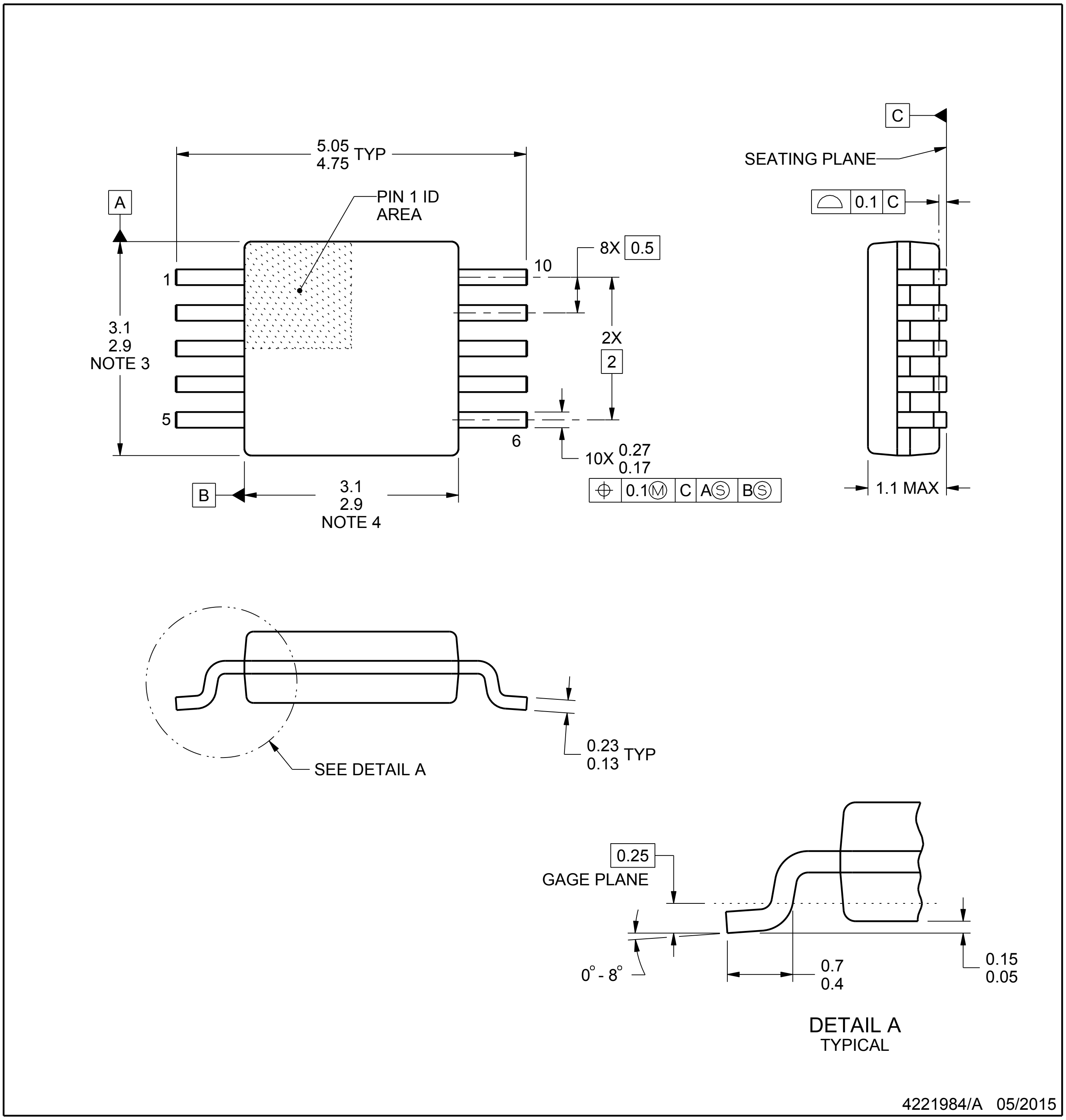
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC082S085CIMM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
DAC082S085CIMMX/ NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
DAC082S085CISD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
DAC082S085CISDX/ NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

DSC0010A

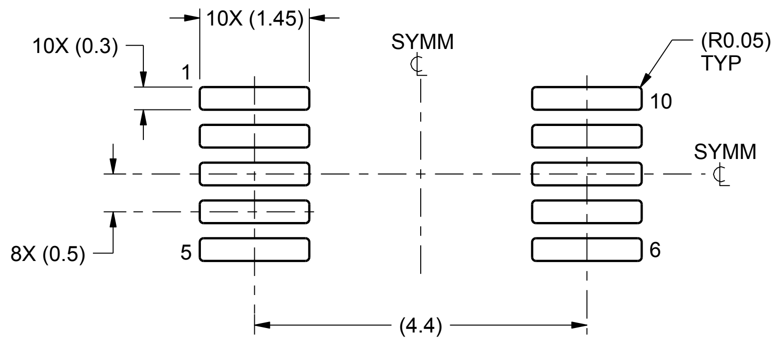


SDA10A (Rev A)

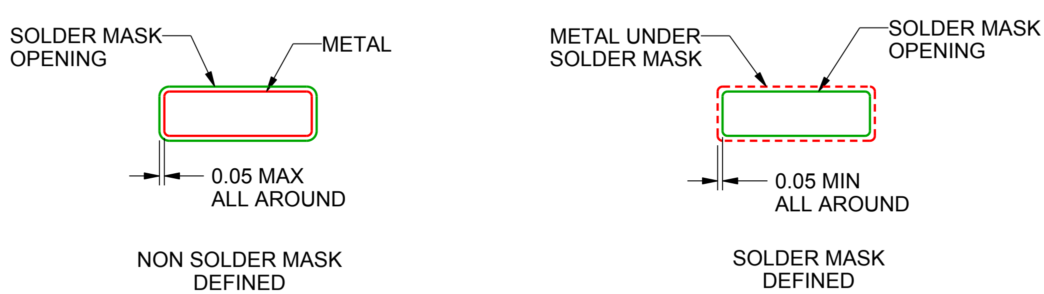


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

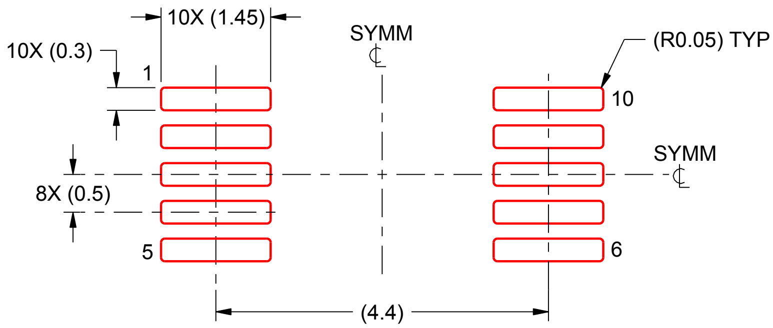


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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