CSD87381P Synchronous Buck NexFET™ Power Block II

1 Features

- Half-Bridge Power Block
- 90% System Efficiency at 10 A
- Up to 15 A Operation
- High Density – 3 × 2.5 mm LGA Footprint
- Double Side Cooling Capability
- Ultra-Low Profile – 0.48 mm Max
- Optimized for 5 V Gate Drive
- Low Switching Losses
- Low Inductance Package
- RoHS Compliant
- Halogen Free
- Pb Free

2 Applications

- Synchronous Buck Converters
  - High Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters

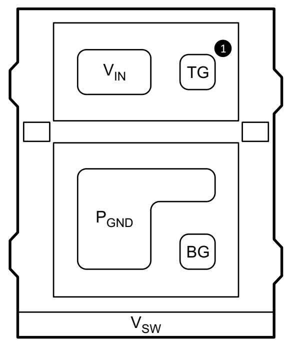
3 Description

The CSD87381P NexFET™ power block II is a highly optimized design for synchronous buck applications offering high current and high efficiency capability in a small 3 mm × 2.5 mm outline. Optimized for 5 V gate drive applications, this product offers an efficient and flexible solution capable of providing a high density power supply when paired with any 5 V gate driver from an external controller/driver.

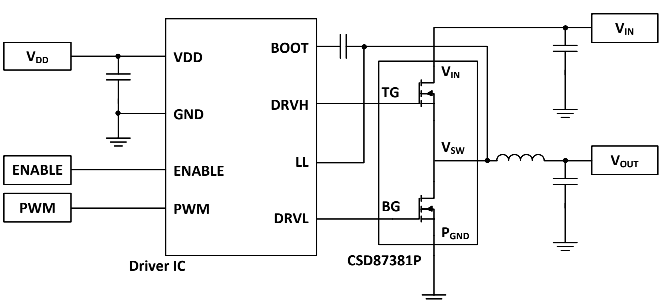
Device Information[1]

Device	Media	Qty	Package	Ship
CSD87381P	13-Inch Reel	2500	3 × 2.5 LGA	Tape and Reel
CSD87381PT	7-Inch Reel	250		

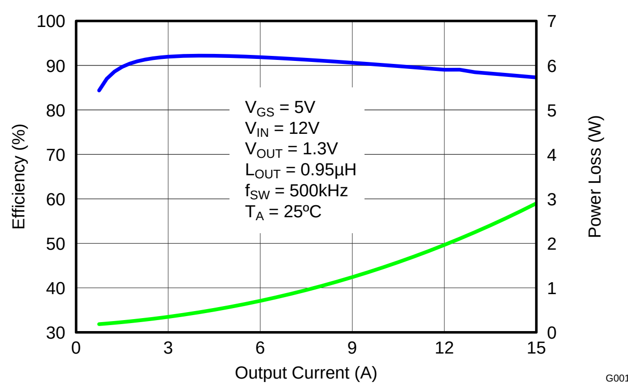
(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Circuit



Typical Power Block Efficiency and Power Loss



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2014) to Revision F — **Page**

- Changed capacitance units to read pF in Figure 15 ... 8
- Changed capacitance units to read pF in Figure 16 ... 8

Changes from Revision D (May 2014) to Revision E — **Page**

- Changed "Pb Free terminal plating" feature to state "Pb Free" ... 1

Changes from Revision C (January 2014) to Revision D — **Page**

- Updated data sheet to reflect new standards ... 1
- Corrected device dimensions ... 1

Changes from Revision B (May 2013) to Revision C — **Page**

- Updated title ... 1
- Added small reel info ... 1
- Added unit to test condition in Electrical Characteristics ... 4
- Added a link for Figure 29 in Electrical Performance ... 14

Changes from Revision A (March 2013) to Revision B — **Page**

- Changed $R_{\theta JC\text{-}PCB}$ To: $R_{\theta JC}$ in the Thermal Information table ... 4
- Changed Figure 15 ... 7

Changes from Original (March 2013) to Revision A — **Page**

- Changes to a Product Preview device ... 1

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage		V_{IN} to P_{GND}	–0.8	30	V
		V_{SW} to P_{GND}		30	
		V_{SW} to P_{GND} (10 ns)		32	
		T_G to V_{SW}	–8	10	
		B_G to P_{GND}	–8	10	
I_{DM}	Pulsed Current Rating (2)			40	A
P_D	Power Dissipation (3)			4	W
E_{AS}	Avalanche Energy	Sync FET, I_D = 27, L = 0.1 mH		36	mJ
		Control FET, I_D = 20, L = 0.1 mH		20	
T_J	Operating Junction		–55	150	°C
T_{stg}	Storage Temperature Range		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse Duration ≤50 µs, duty cycle ≤0.01
(3) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu

5.2 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

			MIN	MAX	UNIT
V_{GS}	Gate Drive Voltage		4.5	8	V
V_{IN}	Input Supply Voltage			24	V
f_{SW}	Switching Frequency	C_{BST} = 0.1 µF (min)	200	1500	kHz
Operating Current		No Airflow		15	A
		With Airflow (200 LFM)		20	
		With Airflow + Heat Sink		25	
T_J	Operating Temperature			125	°C

5.3 Power Block Performance

T_A = 25° (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power Loss (1)	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 8 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 µH, T_J = 25ºC		1		W
I_{QVIN}	V_{IN} Quiescent Current	T_G to T_{GR} = 0 V B_G to P_{GND} = 0 V		10		µA

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5 V driver IC.

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) (1)			184	°C/W
	Junction-to-ambient thermal resistance (max Cu) (2)(1)			84	
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package) (1)			4.9	
	Junction-to-case thermal resistance (P_{GND} pin) (1)			1.65	

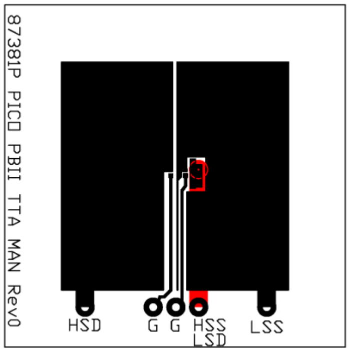
(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu.

5.5 Electrical Characteristics

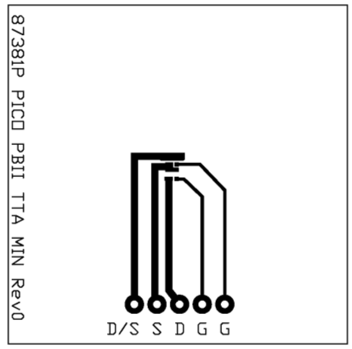
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 10 V			100			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.1		1.9	1		1.7	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_{DS} = 8 A		15.7	18.9		7	8.4	mΩ
		V_{GS} = 8 V, I_{DS} = 8 A		13.6	16.3		6.3	7.6	
g_{fs}	Transconductance	V_{DS} = 10 V, I_{DS} = 8 A		40			89		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input Capacitance (1)	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		434	564		1020	1320	pF
C_{OSS}	Output Capacitance (1)			225	293		308	400	pF
C_{RSS}	Reverse Transfer Capacitance (1)			9.1	11.8		40	52	pF
R_G	Series Gate Resistance (1)			5	6.4		1.25	2.5	Ω
Q_g	Gate Charge Total (4.5 V) (1)	V_{DS} = 15 V, I_{DS} = 8 A		3.9	5		8.9	11.5	nC
Q_{gd}	Gate Charge – Gate-to-Drain			0.9			2.5		nC
Q_{gs}	Gate Charge – Gate-to-Source			1.2			2		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.7			1.3		nC
Q_{OSS}	Output Charge	V_{DD} = 12 V, V_{GS} = 0 V		4.9			8.5		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 8 A, R_G = 2 Ω		6.7			7.9		ns
t_r	Rise Time			19.3			16.3		ns
$t_{d(off)}$	Turn Off Delay Time			10.6			16.8		ns
t_f	Fall Time			3			2.9		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode Forward Voltage	I_{DS} = 8 A, V_{GS} = 0 V		0.85			0.79		V
Q_{rr}	Reverse Recovery Charge	V_{dd} = 15 V, I_F = 8 A, di/dt = 300 A/µs		8			16		nC
t_{rr}	Reverse Recovery Time			13			17		ns

(1) Specified by design



Max $R_{\theta JA}$ = 84°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 184°C/W when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.6 Typical Power Block Characteristics

T_J = 125°C, unless stated otherwise. For Figure 3 and Figure 4, the Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.

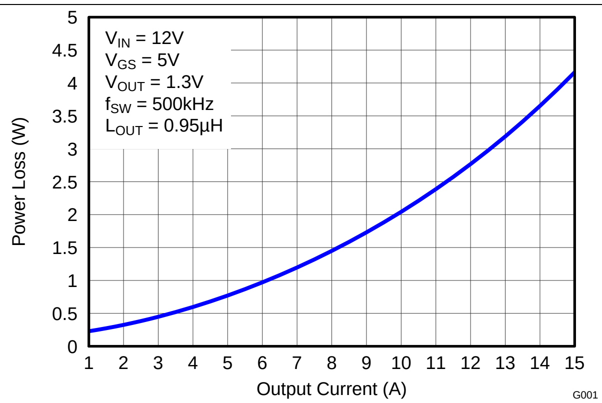


Figure 1. Power Loss vs Output Current

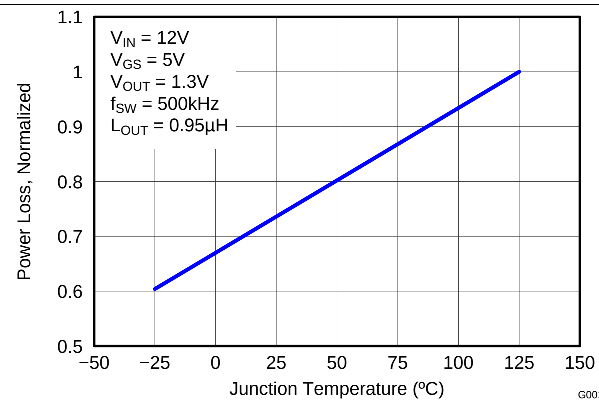


Figure 2. Normalized Power Loss vs Temperature

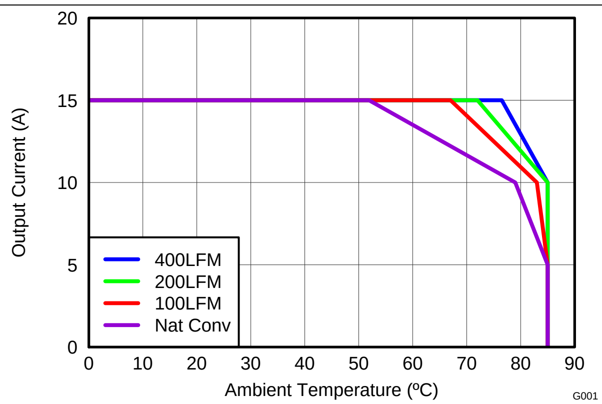


Figure 3. Safe Operating Area – PCB Horizontal Mount

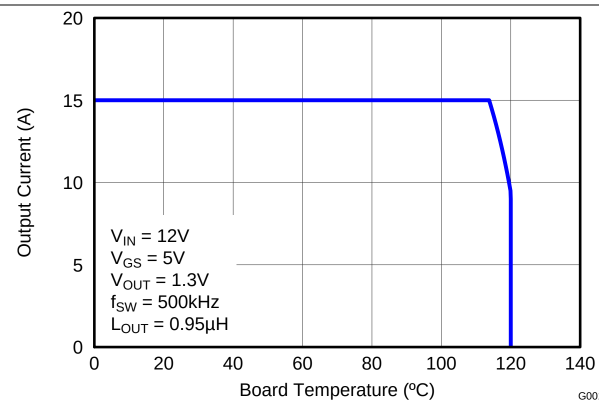


Figure 4. Typical Safe Operating Area

Typical Power Block Characteristics (continued)

T_J = 125°C, unless stated otherwise. For Figure 3 and Figure 4, the Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.

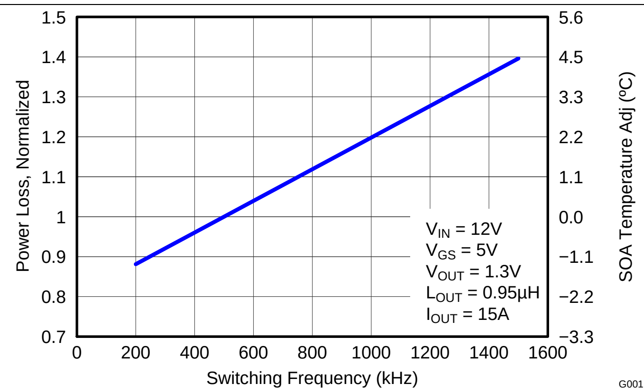


Figure 5. Normalized Power Loss vs Switching Frequency

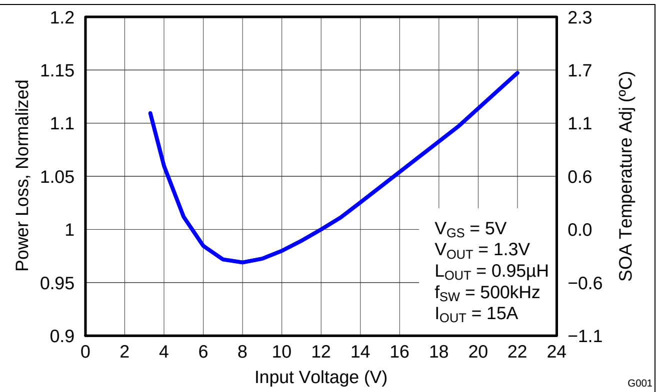


Figure 6. Normalized Power Loss vs Input Voltage

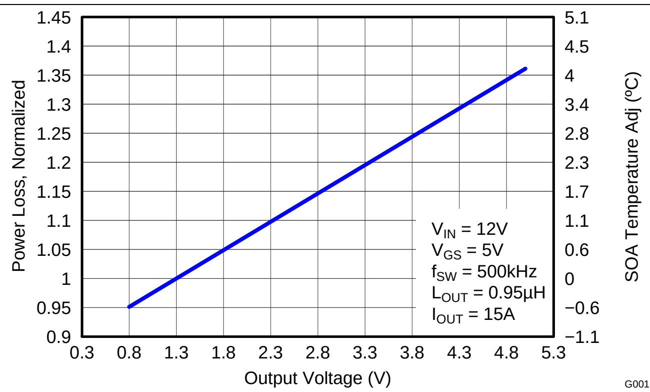


Figure 7. Normalized Power Loss vs Output Voltage

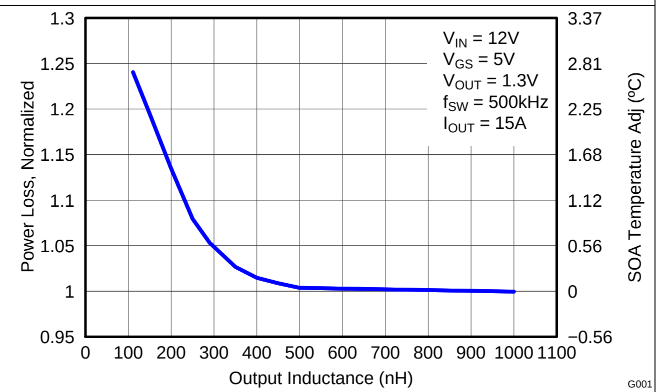


Figure 8. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

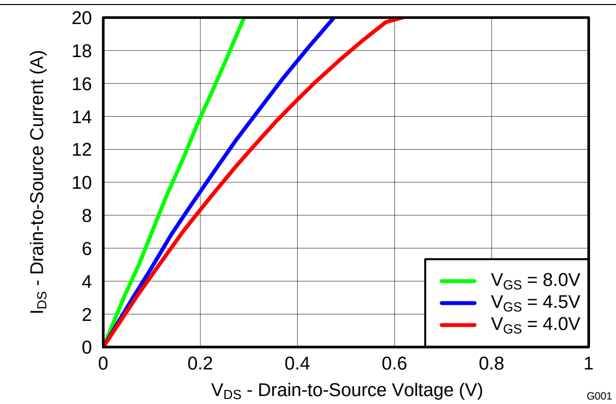


Figure 9. Control MOSFET Saturation

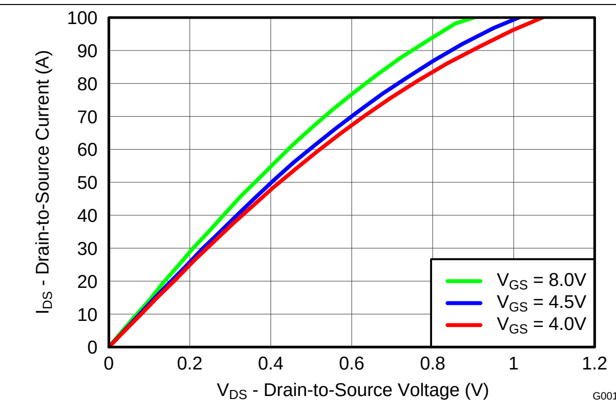


Figure 10. Sync MOSFET Saturation

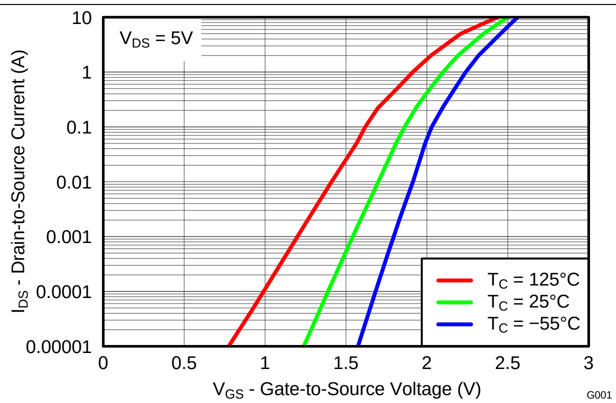


Figure 11. Control MOSFET Transfer

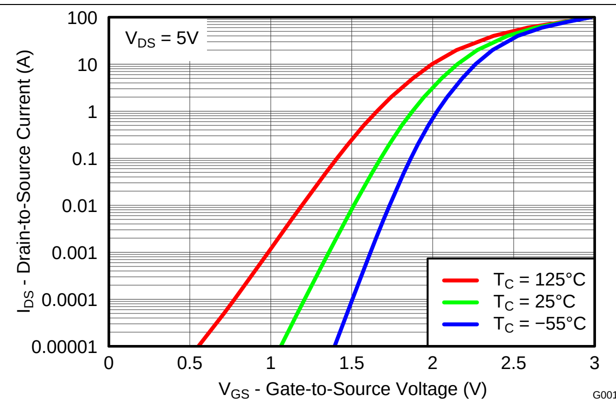


Figure 12. Sync MOSFET Transfer

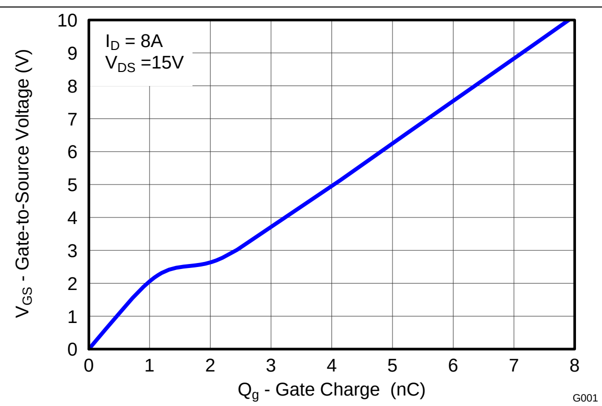


Figure 13. Control MOSFET Gate Charge

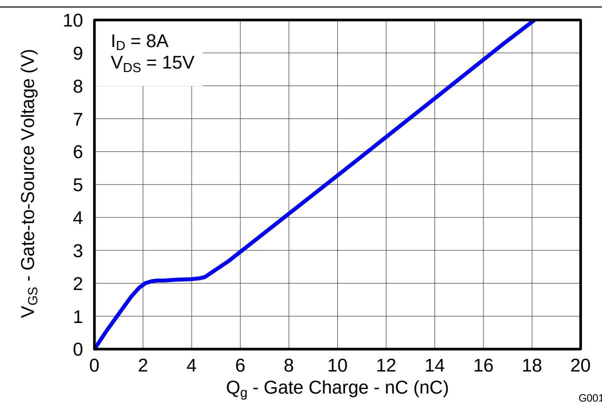


Figure 14. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

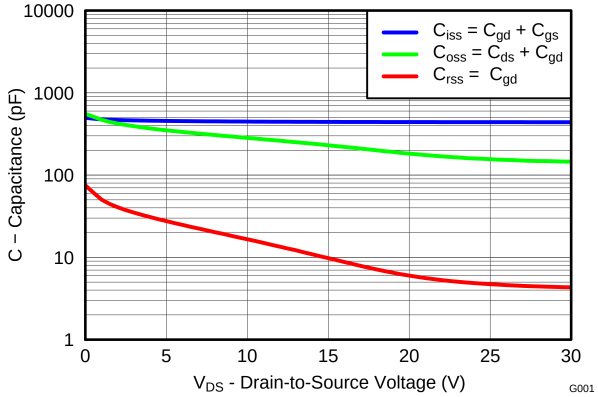


Figure 15. Control MOSFET Capacitance

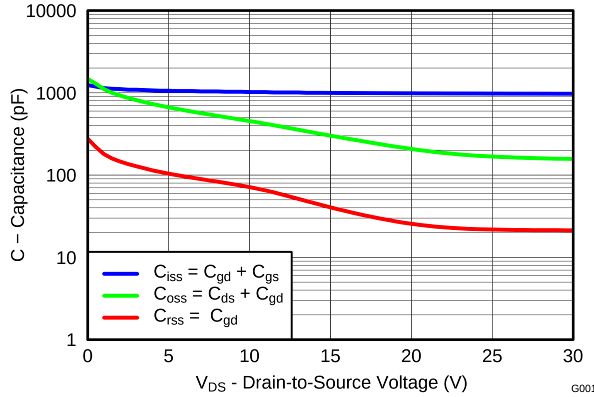


Figure 16. Sync MOSFET Capacitance

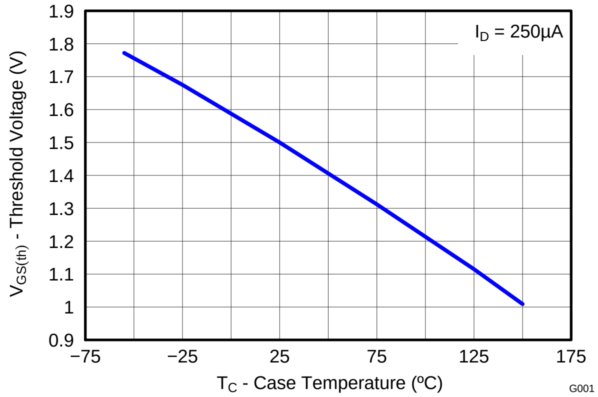


Figure 17. Control MOSFET $V_{GS(th)}$

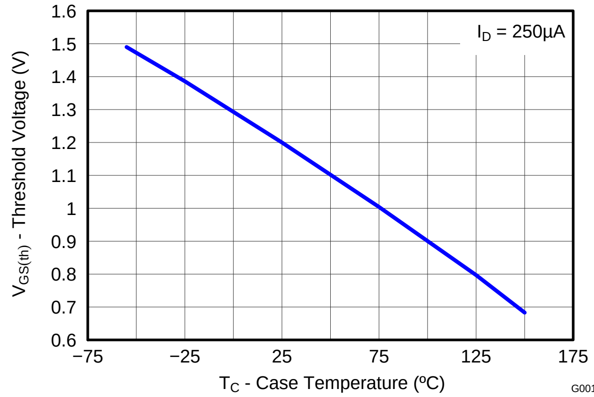


Figure 18. Sync MOSFET $V_{GS(th)}$

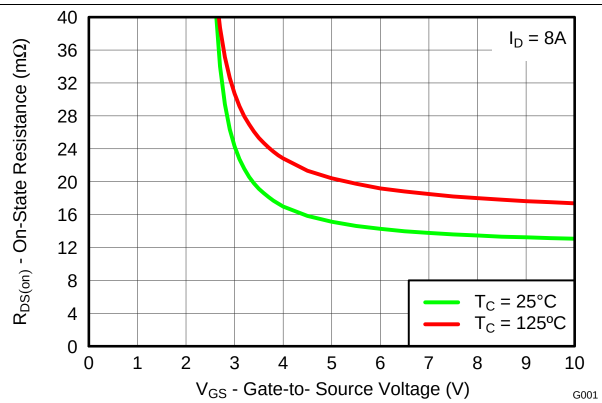


Figure 19. Control MOSFET $R_{DS(on)}$ vs V_{GS}

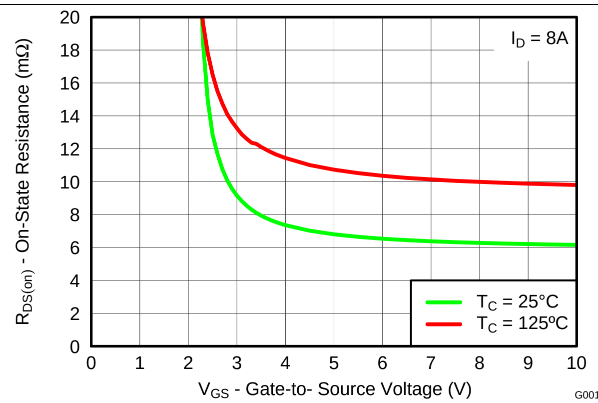


Figure 20. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

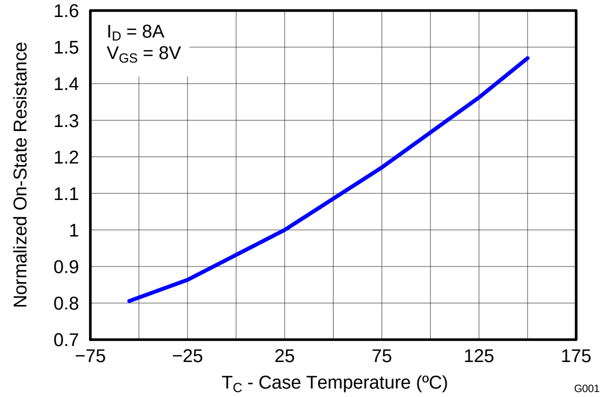


Figure 21. Control MOSFET Normalized $R_{DS(on)}$

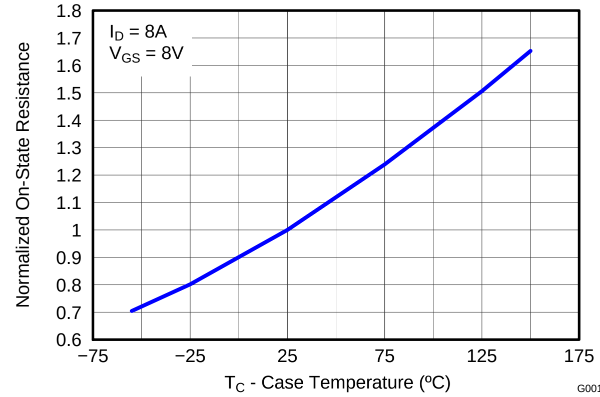


Figure 22. Sync MOSFET Normalized $R_{DS(on)}$

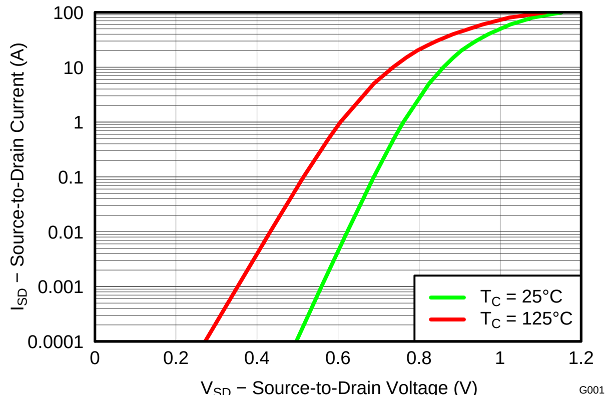


Figure 23. Control MOSFET Body Diode

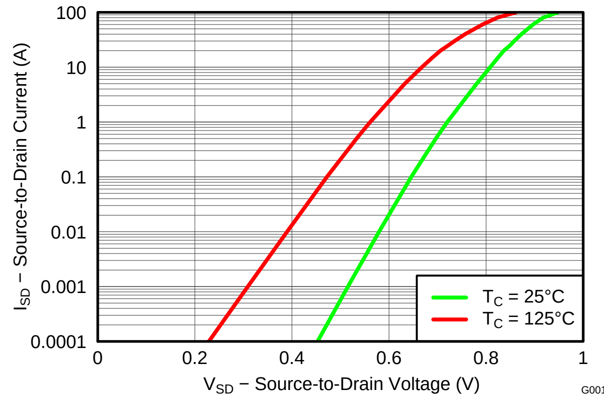


Figure 24. Sync MOSFET Body Diode

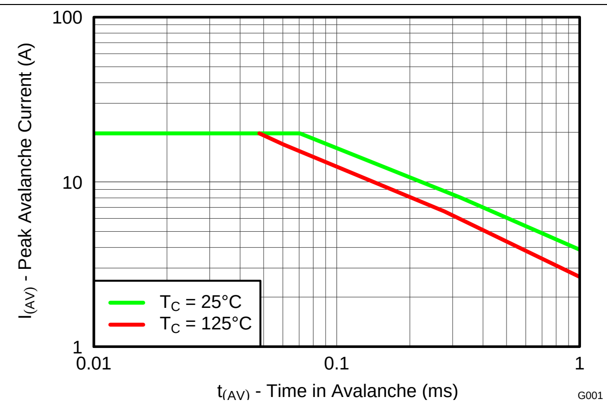


Figure 25. Control MOSFET Unclamped Inductive Switching

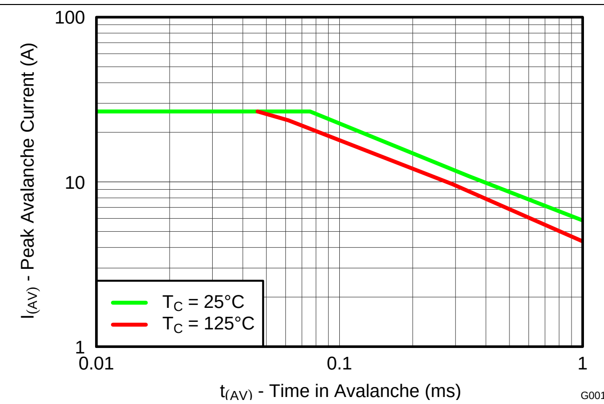


Figure 26. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI ' s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87381P NexFET power block is an optimized design for synchronous buck applications using 5 V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed, which is tailored towards a more systems-centric environment. System-level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.1 Power Loss Curves

MOSFET-centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, TI has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87381P as a function of load current. This curve is measured by configuring and running the CSD87381P as it would be in the final application (see Figure 27). The measured power loss is the CSD87381P loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.2 Safe Operating Curves (SOA)

The SOA curves in the CSD87381P data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness.

6.1.3 Normalized Curves

The normalized curves in the CSD87381P data sheet provide guidance on the power loss and SOA adjustments based on their application-specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of systems conditions. The primary y-axis is the normalized change in power loss, and the secondary y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve, and the change in temperature is subtracted from the SOA curve.

Application Information (continued)

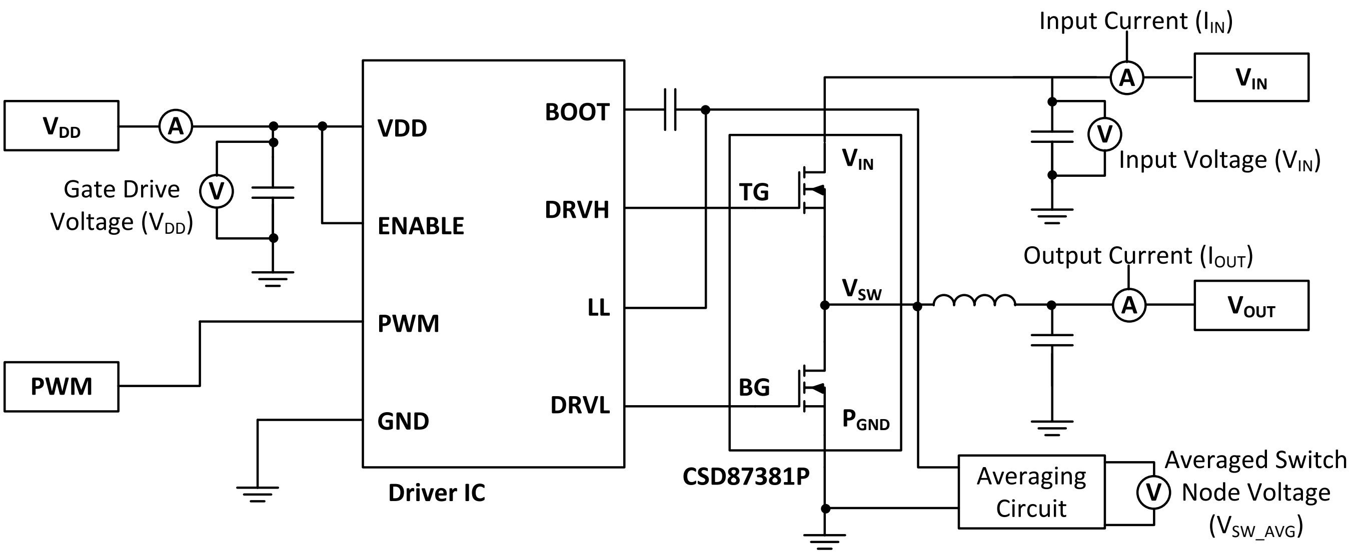


Figure 27. Typical Application

Application Information (continued)

6.1.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.1.4.1 Design Example

Operating Conditions:

- Output Current = 8 A
- Input Voltage = 4 V
- Output Voltage = 1 V
- Switching Frequency = 800 kHz
- Inductor = 0.2 µH

6.1.4.2 Calculating Power Loss

- Power Loss at 8 A = 1.44 W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.06 (Figure 6)
- Normalized Power Loss for output voltage ≈ 0.97 (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.11 (Figure 5)
- Normalized Power Loss for output inductor ≈ 1.13 (Figure 8)
- **Final calculated power loss = 1.44 W × 1.06 × 0.97 × 1.11 × 1.13 ≈ 1.86 W**

6.1.4.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 0.7ºC (Figure 6)
- SOA adjustment for output voltage ≈ –0.3ºC (Figure 7)
- SOA adjustment for switching frequency ≈ 1.03ºC (Figure 5)
- SOA adjustment for output inductor ≈ 1.5ºC (Figure 8)
- **Final calculated SOA adjustment = 0.7 + (–0.3) + 1.3 + 1.5 ≈ 2.2ºC**

In the previous design example, the estimated power loss of the CSD87381P would increase to 1.86 W. In addition, the maximum allowable board or ambient temperature, or both, would have to decrease by 2.2ºC. Figure 28 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
3. Adjust the SOA board or ambient temperature by subtracting the temperature adjustment value.

Application Information (continued)

In the design example, the SOA temperature adjustment yields a reduction in allowable board or ambient temperature of 2.2ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.

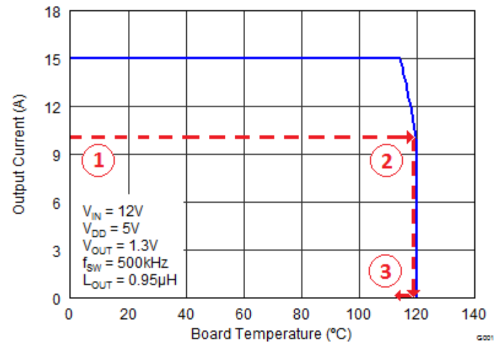


Figure 28. Power Block SOA

7 Layout

7.1 Layout Guidelines

7.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. The following provides a brief description on how to address each parameter.

7.1.2 Electrical Performance

The CSD87381P has the ability to switch voltages at rates greater than 10 kV/µs. Take care with the PCB layout design and placement of the input capacitors, inductor, and output capacitors.

- The placement of the input capacitors relative to VIN and PGND pins of CSD87381P device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 29). The example in Figure 29 uses 1 x 10 nF 0402 25 V and 4 x 10 µF 1206 25 V ceramic capacitors (TDK part number C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power stage, C21, C5, C8, C19, and C18 should follow in order.
- The switching node of the output inductor should be placed relatively close to the Power Block II CSD87381P VSW pins. Minimizing the VSW node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. See Figure 29. (1)

7.1.3 Thermal Performance

The CSD87381P has the ability to utilize the PGND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that wicks down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 29 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

7.2 Layout Example

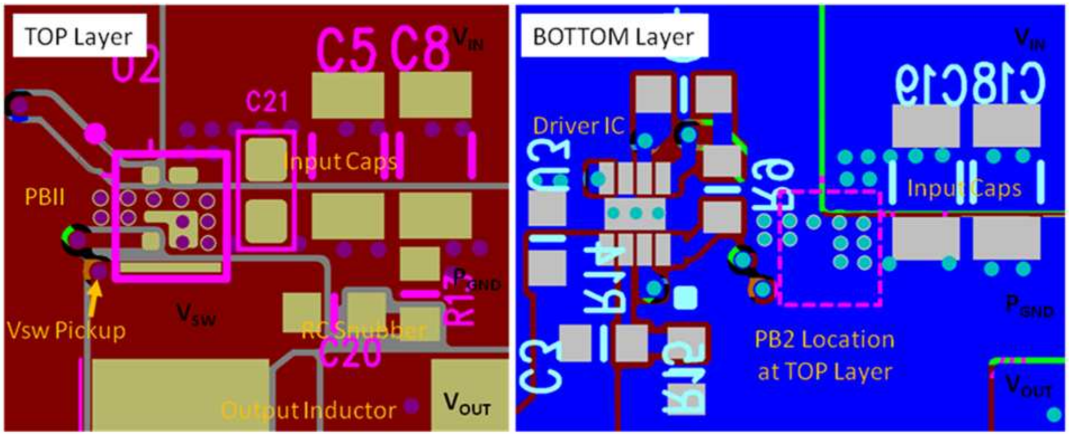


Figure 29. Recommended PCB Layout (Top Down View)

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

8 Device and Documentation Support

8.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.3 Glossary

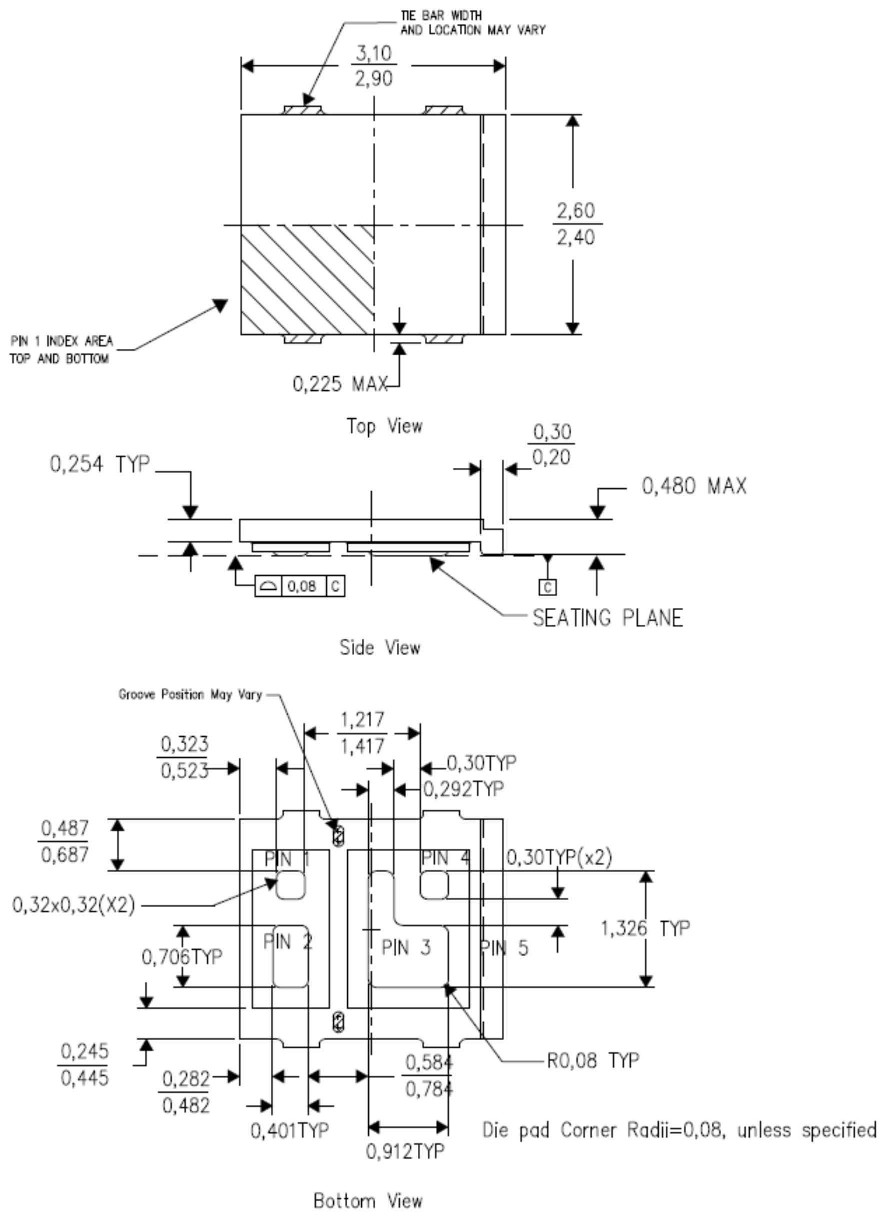
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

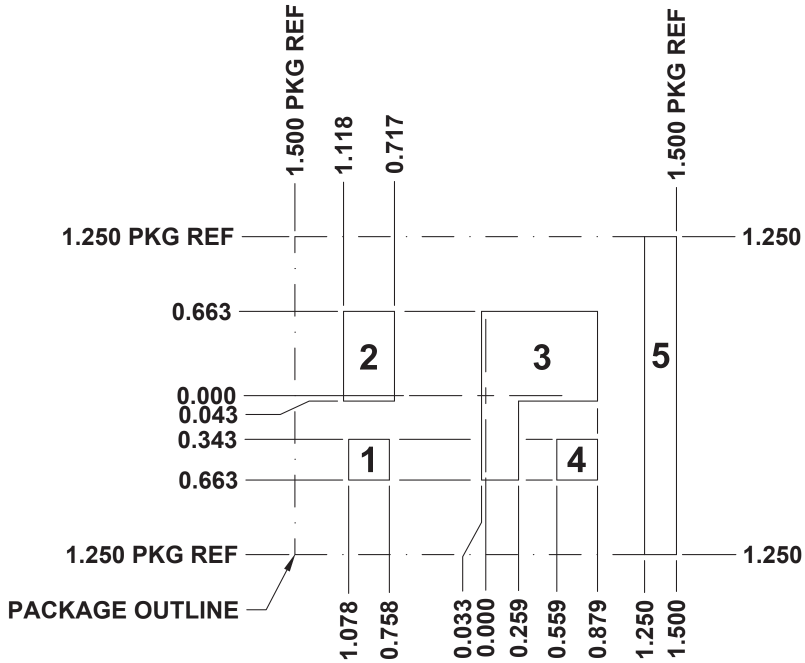
9.1 CSD87381P Package Dimensions



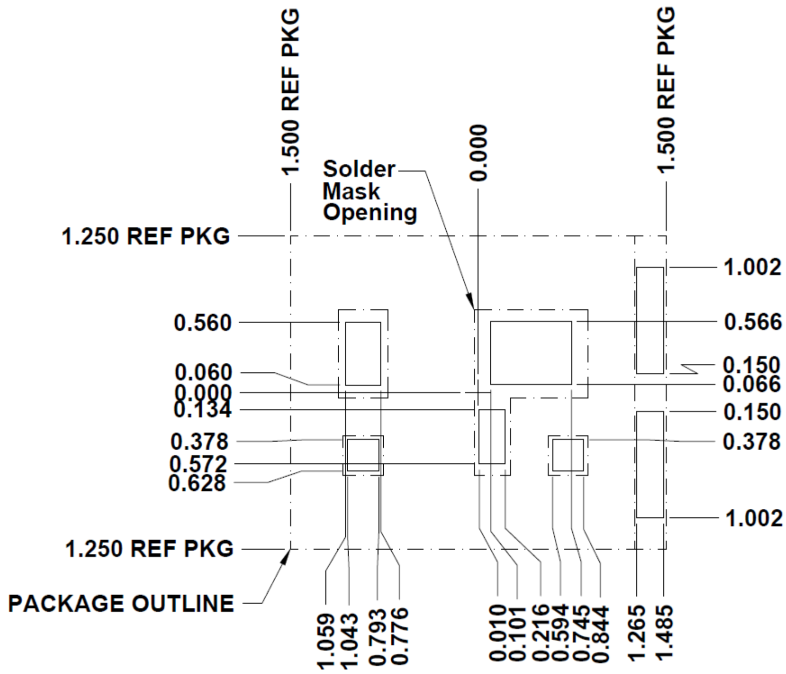
Pin Configuration

Position	Designation
Pin 1	TG
Pin 2	V_{IN}
Pin 3	P_{GND}
Pin 4	BG
Pin 5	V_{SW}

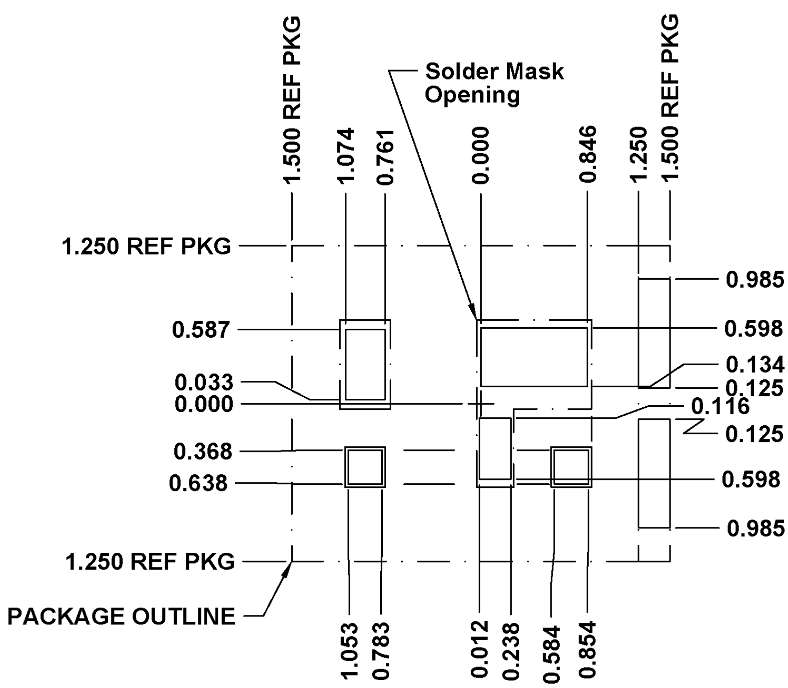
9.2 Land Pattern Recommendation



9.3 Stencil Recommendation (100 µm)

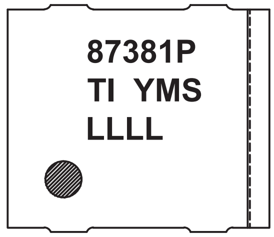


9.4 Stencil Recommendation (125 µm)

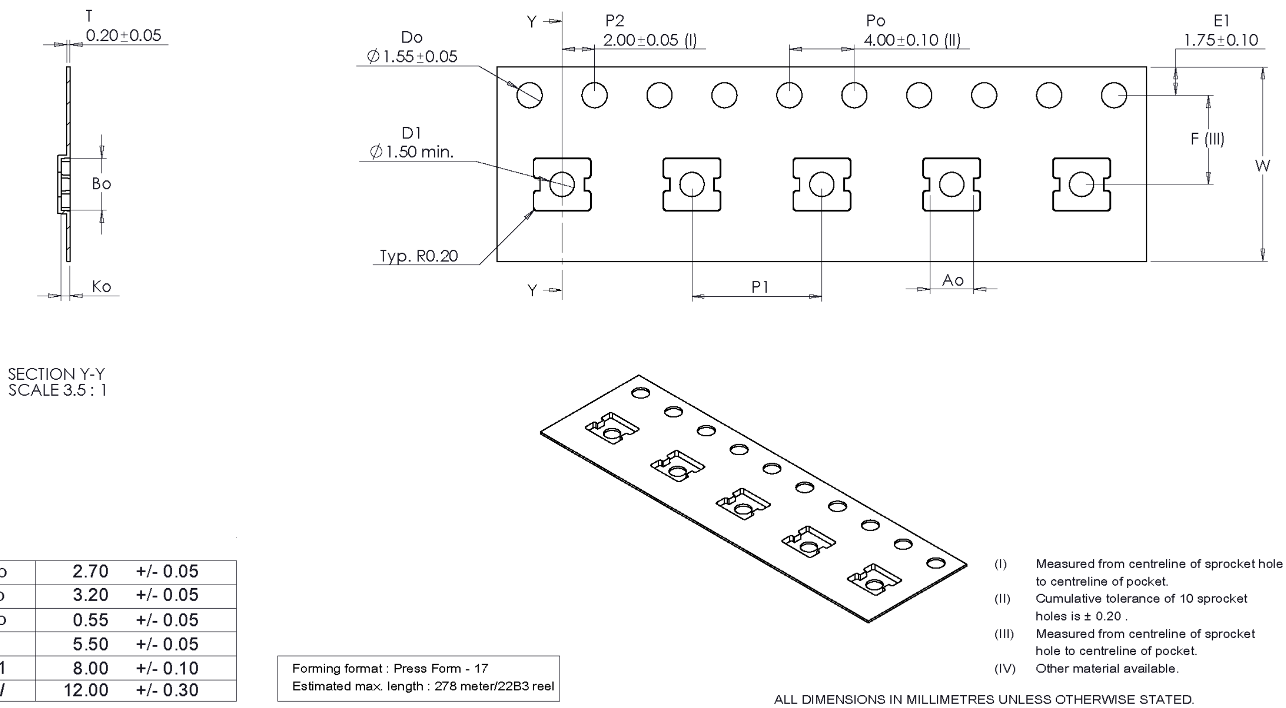


For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

9.5 Pin Drawing



9.6 CSD87381P Embossed Carrier Tape Dimensions



Ao	2.70	+/- 0.05
Bo	3.20	+/- 0.05
Ko	0.55	+/- 0.05
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press Form - 17
Estimated max. length : 278 meter/22B3 reel

(1) Pin 1 is oriented in the top-left quadrant of the tape enclosure (closest to the carrier tape sprocket holes).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD87381P	Active	Production	PTAB (MPC) | 5	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87381P
CSD87381P.B	Active	Production	PTAB (MPC) | 5	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87381P
CSD87381PG4.B	Active	Production	PTAB (MPC) | 5	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87381P
CSD87381PT	Active	Production	PTAB (MPC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87381P
CSD87381PT.B	Active	Production	PTAB (MPC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87381P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

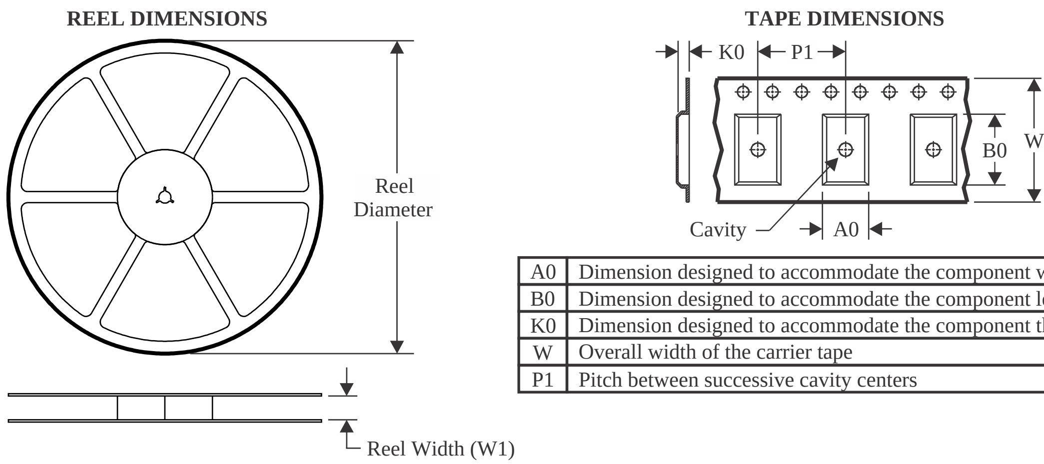
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

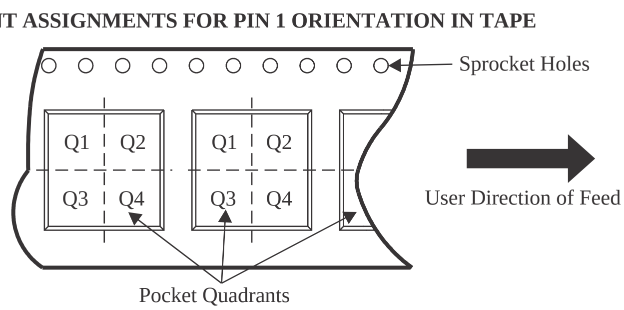
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



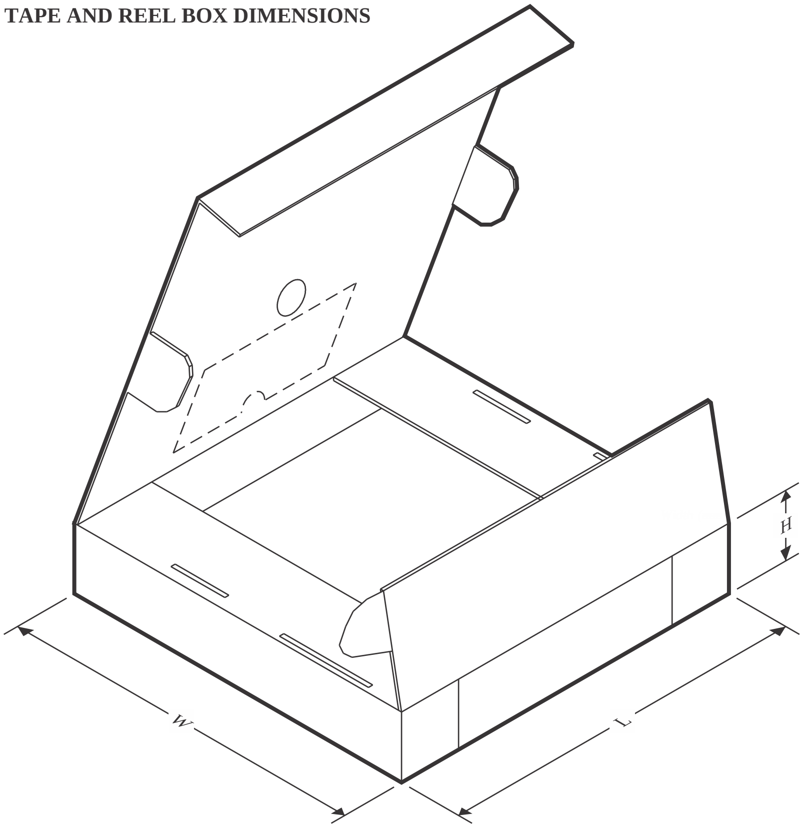
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87381P	PTAB	MPC	5	2500	330.0	12.4	2.7	3.2	0.55	8.0	12.0	Q1
CSD87381PT	PTAB	MPC	5	250	180.0	12.4	2.7	3.2	0.55	8.0	12.0	Q1

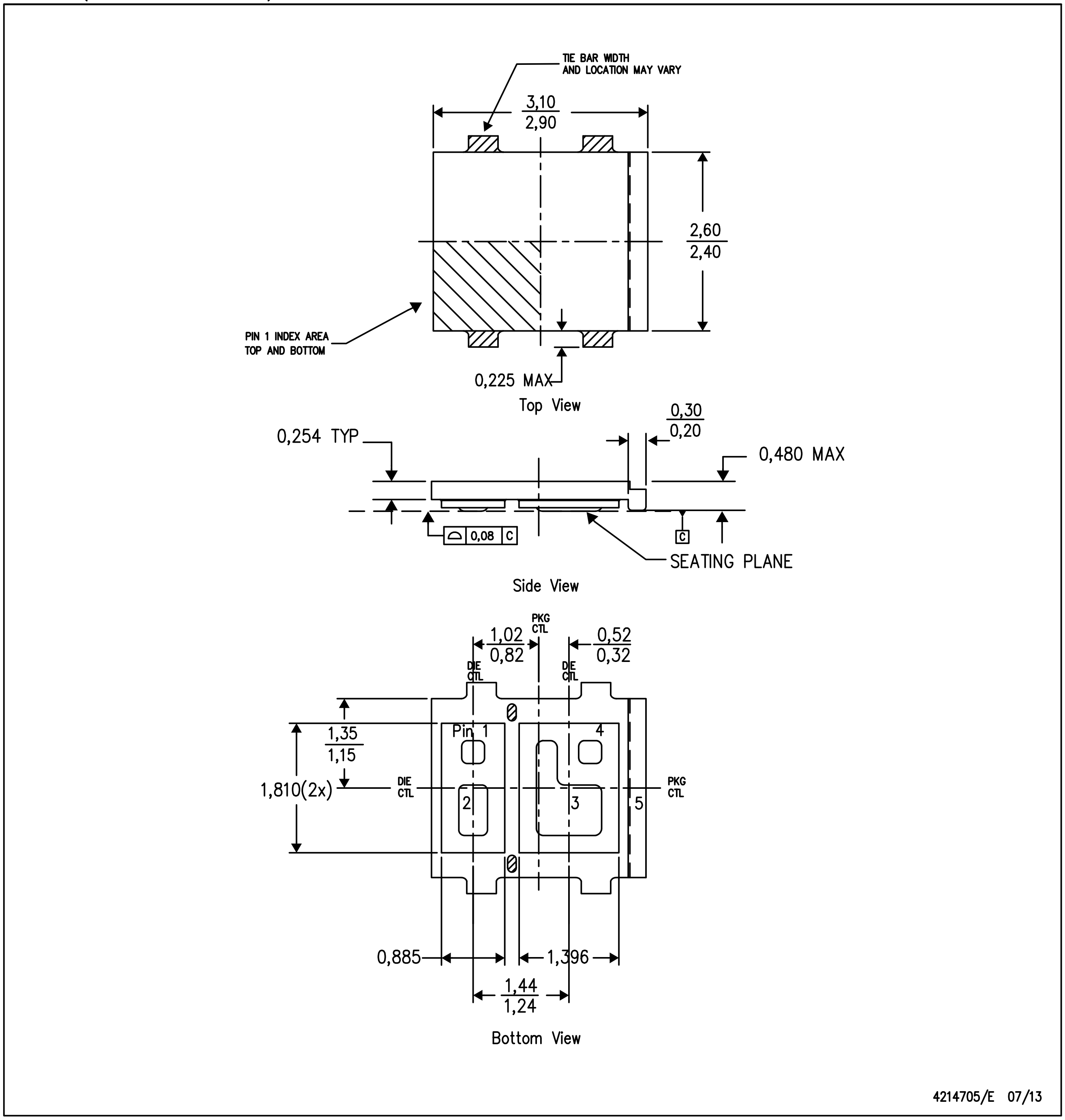
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87381P	PTAB	MPC	5	2500	346.0	346.0	33.0
CSD87381PT	PTAB	MPC	5	250	182.0	182.0	20.0

MPC (R–PTAB–X5) PowerTab



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.