

Dual 20 V N-Channel NexFET™ Power MOSFETs

FEATURES

- Common Source Connection
- Low Drain to Drain On-Resistance
- Space Saving SON 3.3 x 3.3 mm Plastic Package
- Optimized for 5 V Gate Drive
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free

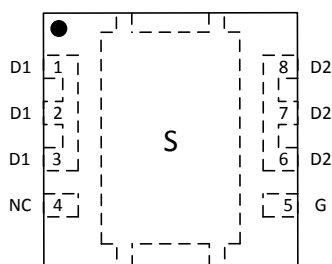
APPLICATIONS

- Adaptor or USB Input Protection for Notebook PCs and Tablets

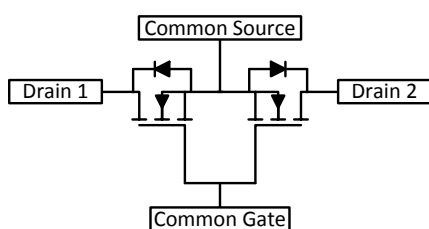
DESCRIPTION

The CSD85312Q3E is a 20 V common-source, dual N-channel device designed for adaptor or USB input protection. This SON 3.3 x 3.3 mm device has low drain to drain on-resistance that minimizes losses and offers low component count for space constrained multi-cell battery charging applications.

Top View



Circuit Image



PRODUCT SUMMARY

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain to Source Voltage	20	V
Q_g	Gate Charge Total (4.5 V)	11.7	nC
Q_{gd}	Gate Charge Gate to Drain	1.6	nC
$R_{DD(on)}$	Drain to Drain On Resistance ($Q_1 + Q_2$)	$V_{GS} = 4.5\text{ V}$	11.7 mΩ
		$V_{GS} = 8\text{ V}$	10.3 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD85312Q3E	SON 3.3 x 3.3 mm Plastic Package	13 Inch Reel	2500	Tape and Reel

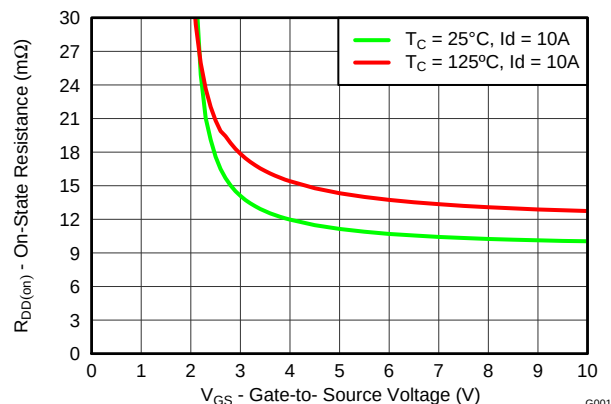
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	+10/-8	V
I_D	Continuous Drain Current (Package Limited)	39	A
	Continuous Drain Current ⁽¹⁾	12	A
I_{DM}	Pulsed Drain Current ⁽²⁾	76	A
P_D	Power Dissipation	2.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 38\text{ A}, L = 0.1\text{ mH}, R_G = 25\text{ }\Omega$	72	mJ

(1) Typical $R_{\theta JA} = 63^\circ\text{C/W}$ on 1 inch² (2 oz.) on 0.060 inch thick FR4PCB

(2) Pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

V_{GS} vs. $R_{DD(on)}$



G001



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0 V, I _D = 250 μA	20			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0 V, V _{DS} = 16 V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0 V, V _{GS} = +10/−8 V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.85	1.10	1.40	V
R _{DD(on)}	Drain to Drain On Resistance (Q1 + Q2)	V _{GS} = 4.5 V, I _D = 10 A		11.7	14.0	mΩ
		V _{GS} = 8 V, I _D = 10 A		10.3	12.4	mΩ
g _{fs}	Transconductance	V _{DS} = 10 V, I _D = 10 A		99		S
Dynamic Characteristics ⁽¹⁾						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 10 V, f = 1 MHz		1840	2390	pF
C _{oss}	Output Capacitance			492	640	pF
C _{rss}	Reverse Transfer Capacitance			31	40	pF
R _G	Series Gate Resistance			5.5	11	Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 10 V, I _D = 10 A		11.7	15.2	nC
Q _{gd}	Gate Charge Gate to Drain			1.6		nC
Q _{gs}	Gate Charge Gate to Source			3.5		nC
Q _{g(th)}	Gate Charge at V _{th}			1.8		nC
Q _{oss}	Output Charge	V _{DS} = 10 V, V _{GS} = 0 V		8.9		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 10 V, V _{GS} = 4.5 V, I _{DS} = 10 A, R _G = 2 Ω		11		ns
t _r	Rise Time			27		ns
t _{d(off)}	Turn Off Delay Time			24		ns
t _f	Fall Time			6		ns
Diode Characteristics ⁽¹⁾						
V _{SD}	Diode Forward Voltage	I _{SD} = 10 A, V _{GS} = 0 V	0.8		1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 10 V, I _F = 10 A, di/dt = 300 A/μs		15		nC
t _{rr}	Reverse Recovery Time			23		ns

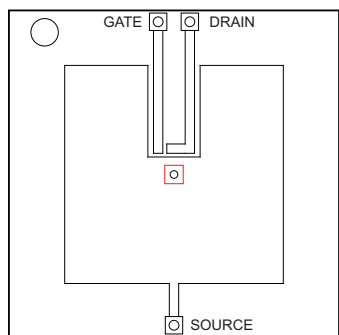
(1) All Dynamic and Diode Characteristics were measured with respect to one of the two drains, with the other left floating.

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

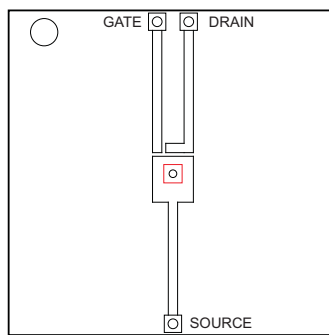
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			3.0	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			63	°C/W

- R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), 2-oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 63^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2
oz. (0.071 mm thick)
Cu.



M0137-02

Max $R_{\theta JA} = 150^{\circ}\text{C/W}$
when mounted on a
minimum pad area of 2
oz. (0.071 mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

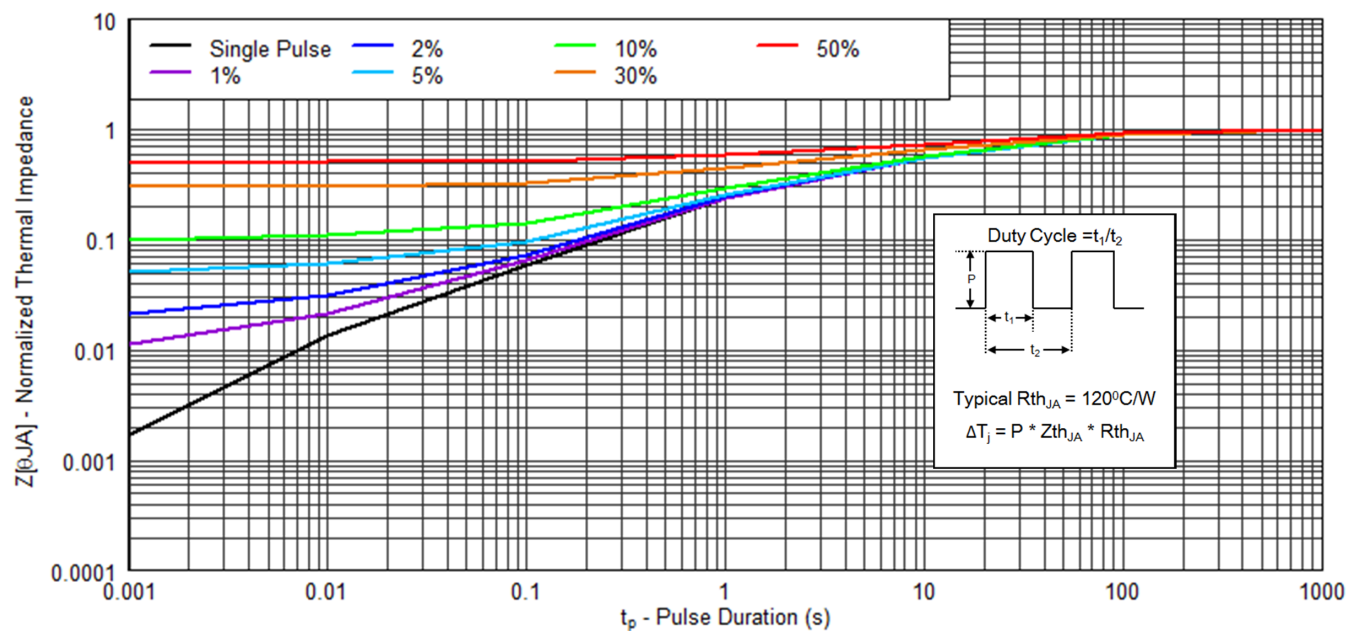


Figure 1. Transient Thermal Impedance

5201

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

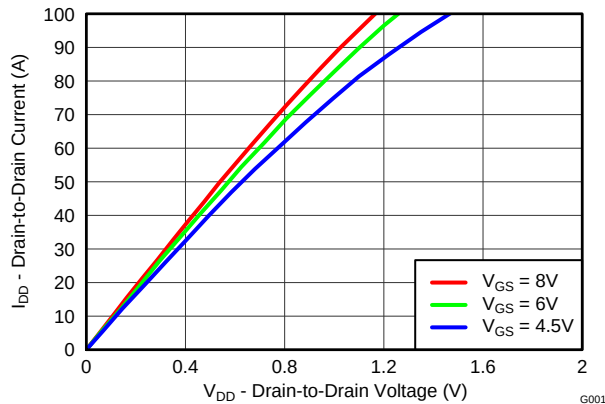


Figure 2. Saturation Characteristics

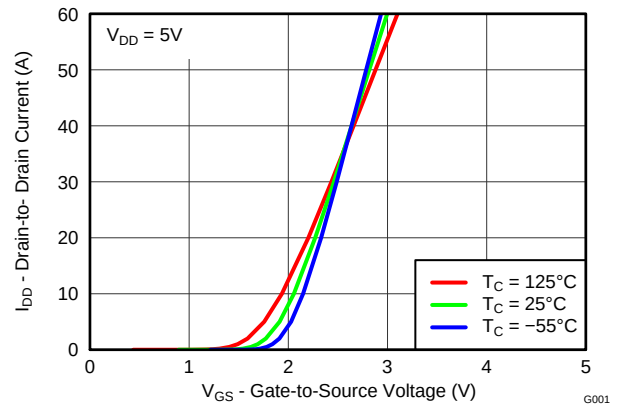


Figure 3. Transfer Characteristics

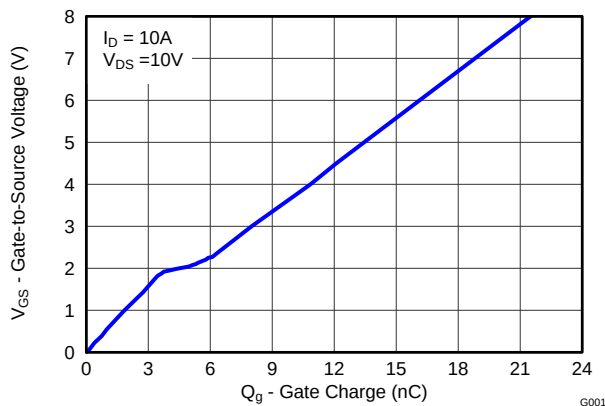


Figure 4. Gate Charge

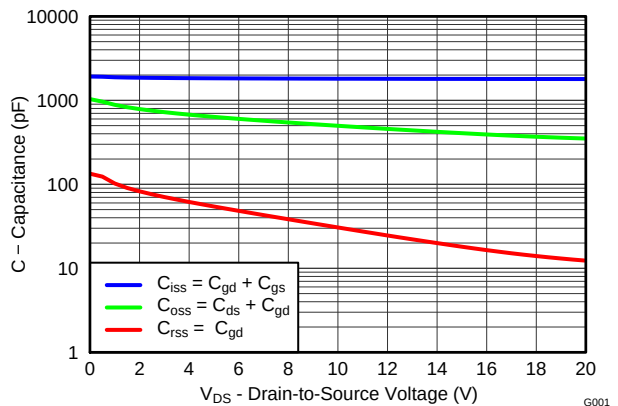


Figure 5. Capacitance

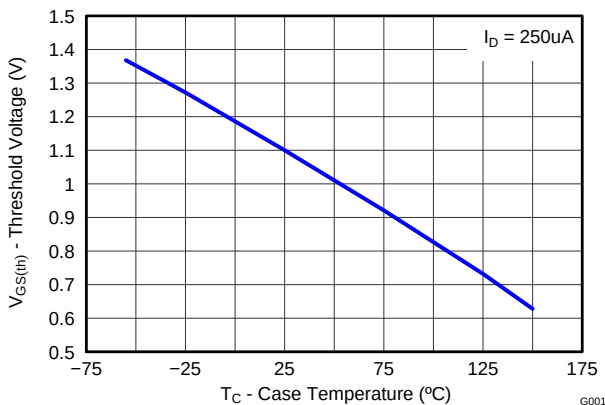


Figure 6. Threshold Voltage vs. Temperature

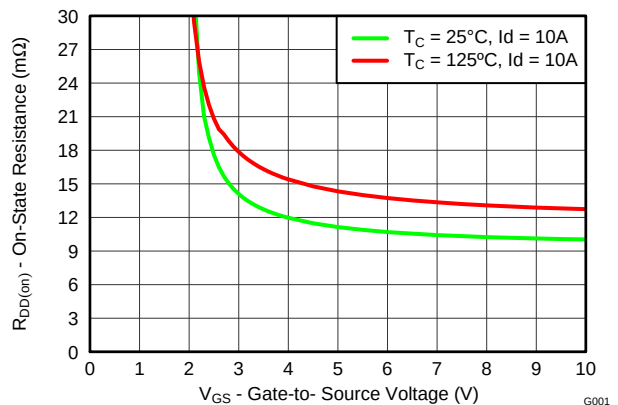


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

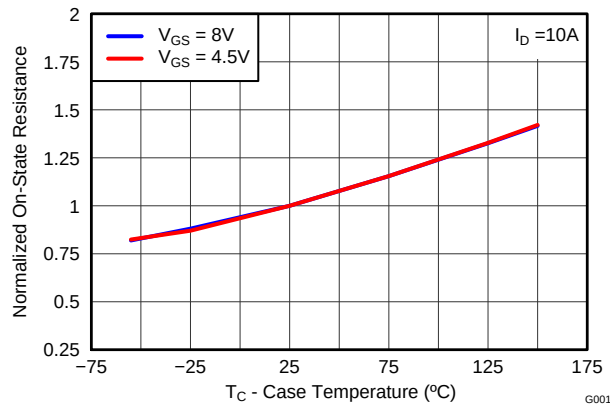


Figure 8. Normalized On-State Resistance vs. Temperature

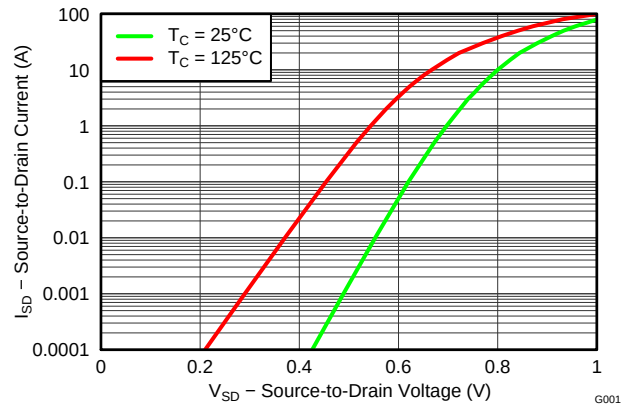


Figure 9. Typical Diode Forward Voltage

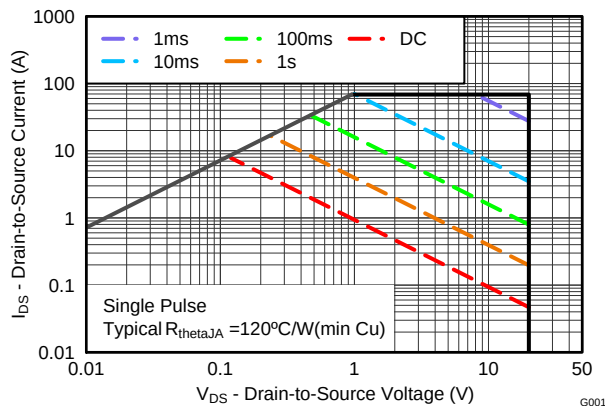


Figure 10. Maximum Safe Operating Area

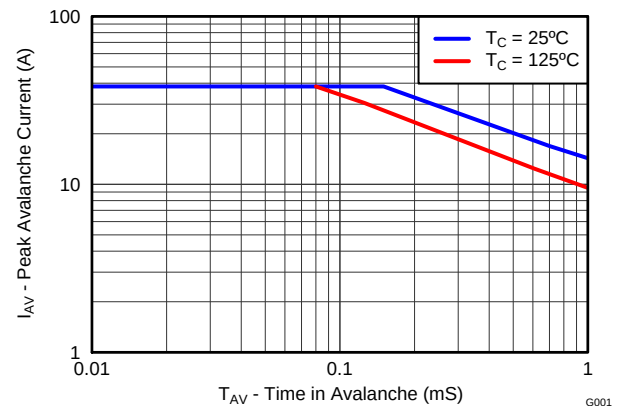


Figure 11. Single Pulse Unclamped Inductive Switching

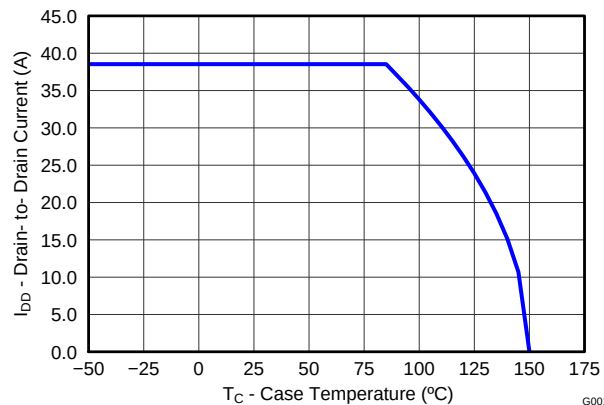


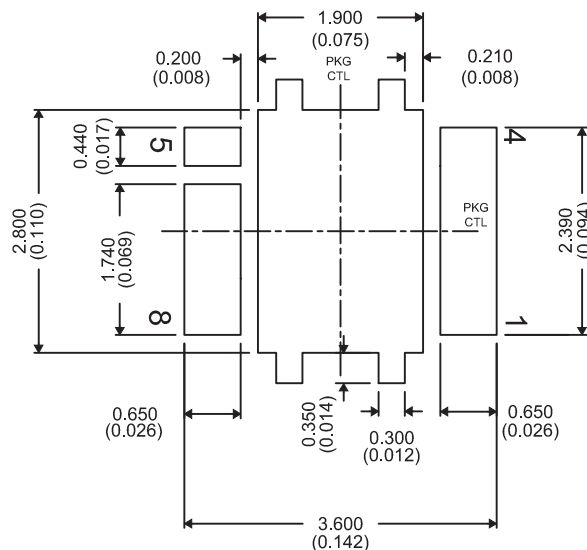
Figure 12. Maximum Drain Current vs. Temperature

CSD85312Q3E Package Dimensions

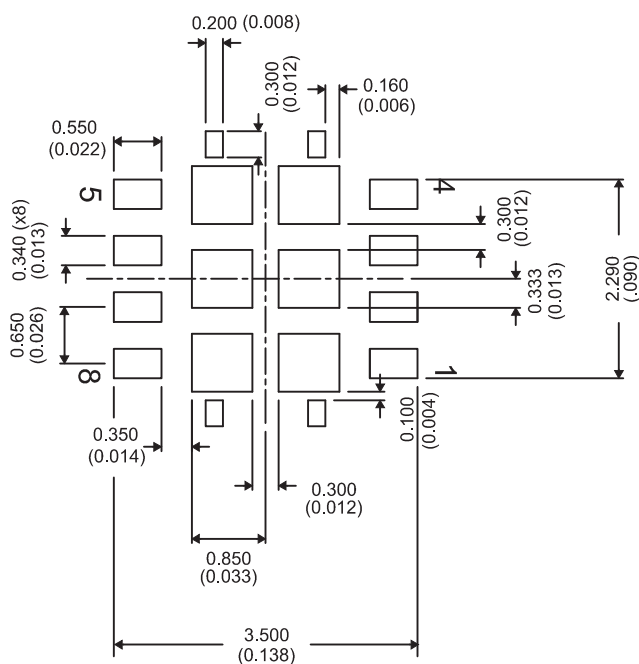


Position	Designation
Pin 1 – 3	Drain 1
Pin 4	No Connect
Pin 5	Gate
Pin 6 – 8	Drain 2
Pin 9 (Thermal Pad)	Source

Recommended PCB Pattern



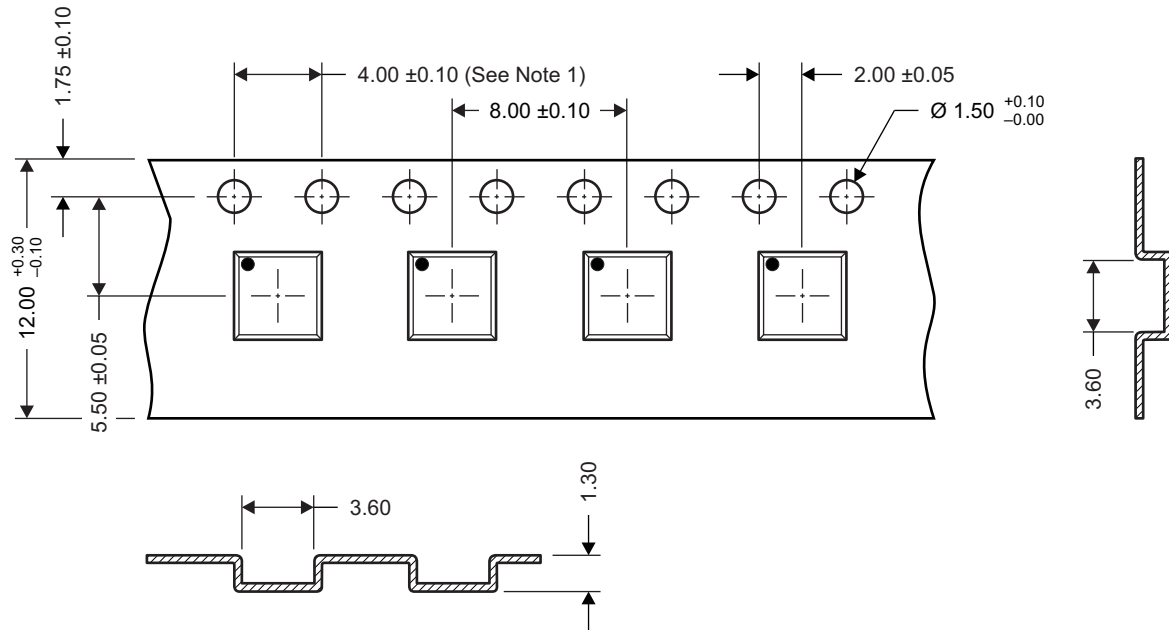
Recommended Stencil Opening



1. All Dimensions are in millimeters (inches)
2. Stencil Opening Thickness 4 mils

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q3E Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD85312Q3E	Active	Production	VSON (DPA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	85312E
CSD85312Q3E.B	Active	Production	VSON (DPA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	85312E

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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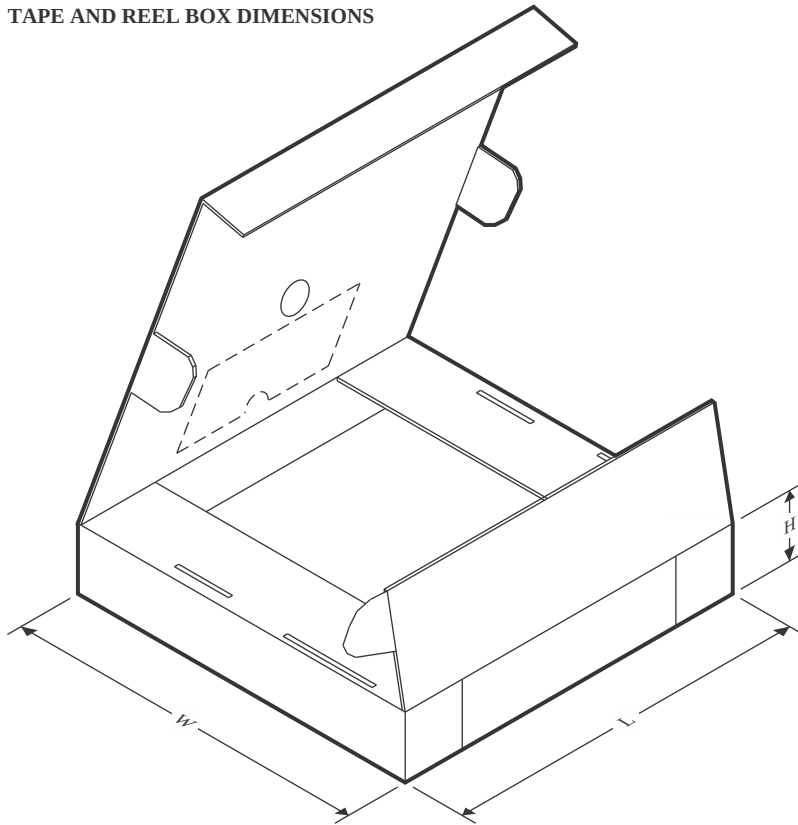
TAPE AND REEL INFORMATION



*All dimensions are nominal

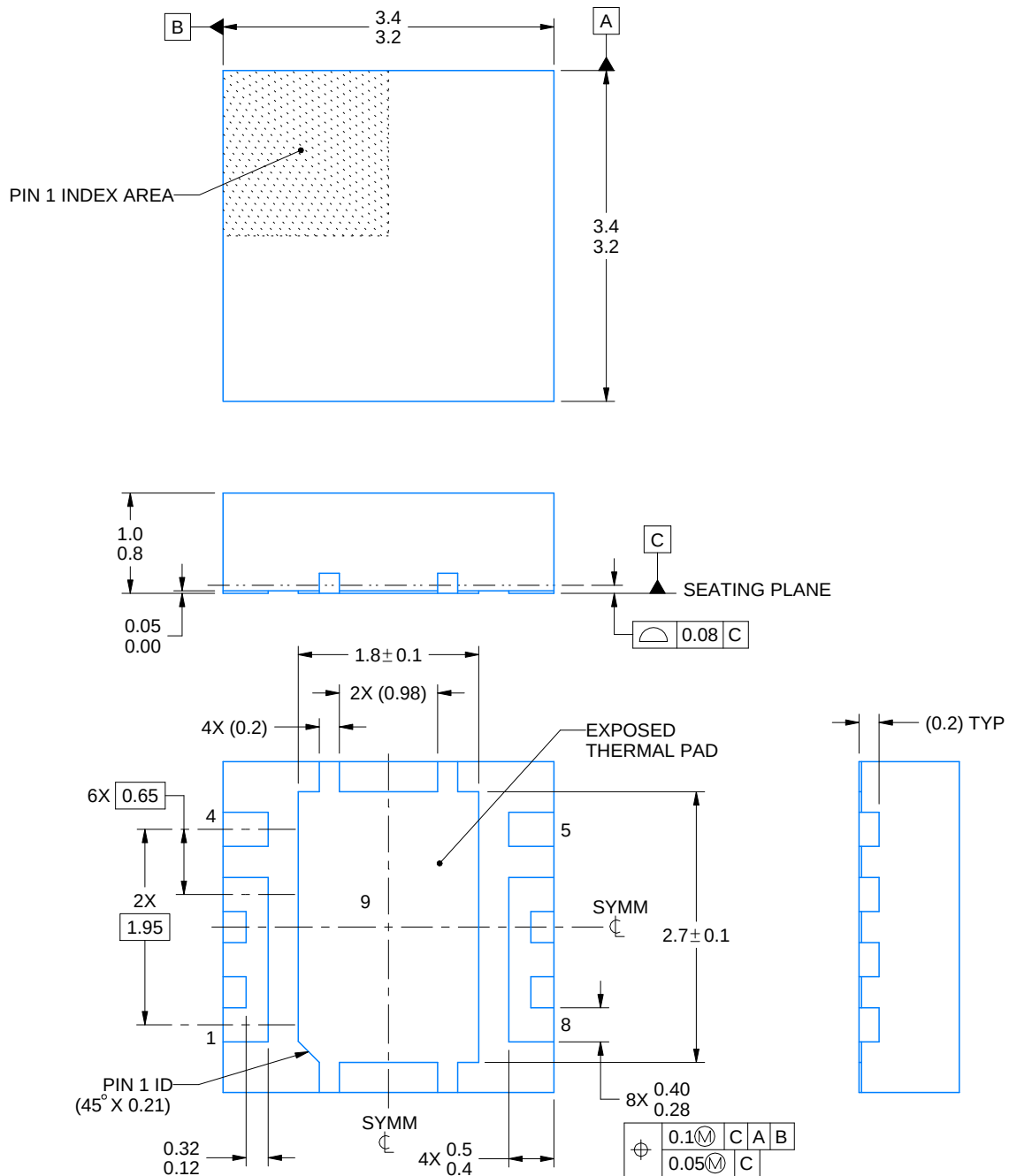
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD85312Q3E	VSON	DPA	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD85312Q3E	VSON	DPA	8	2500	346.0	346.0	33.0



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NOTES:

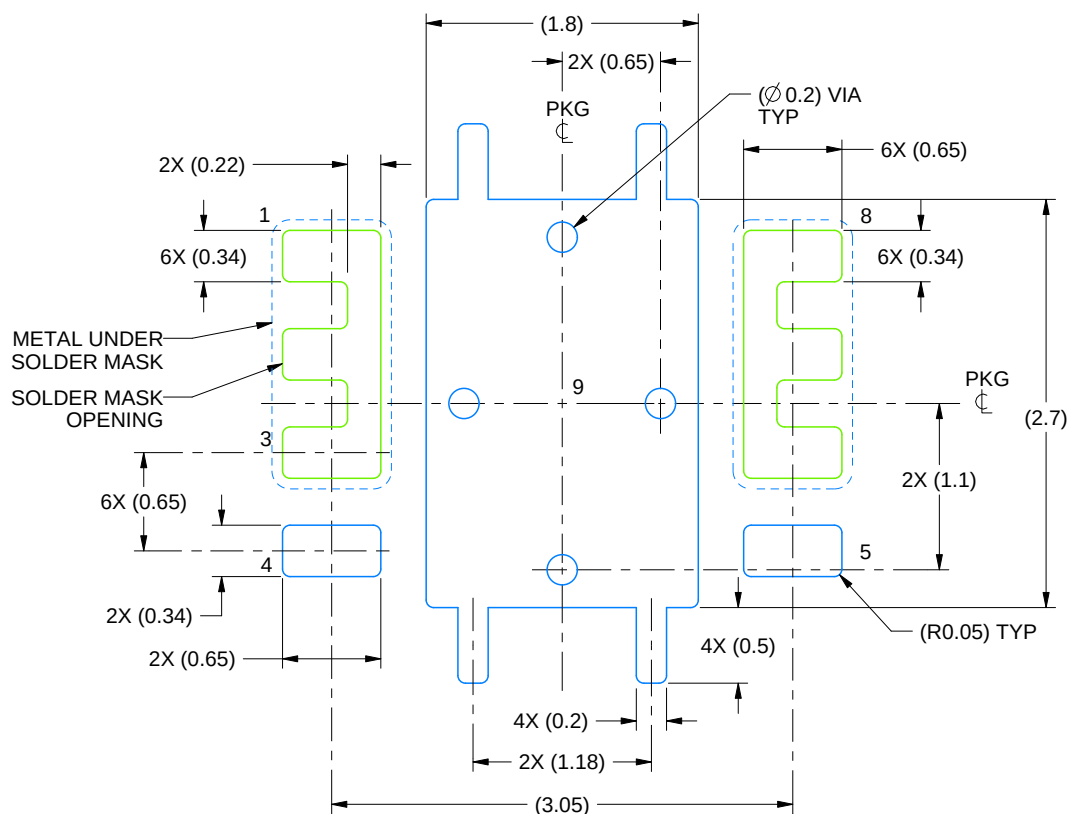
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

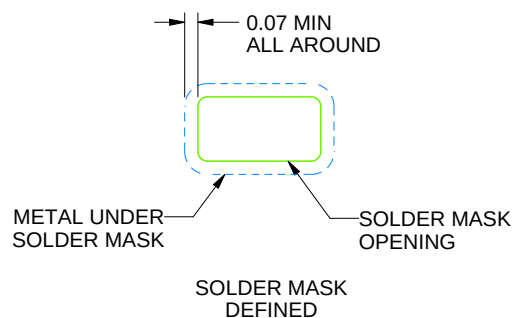
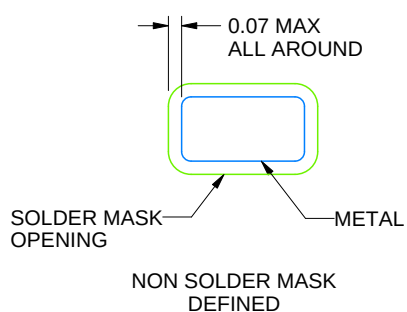
DPA0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

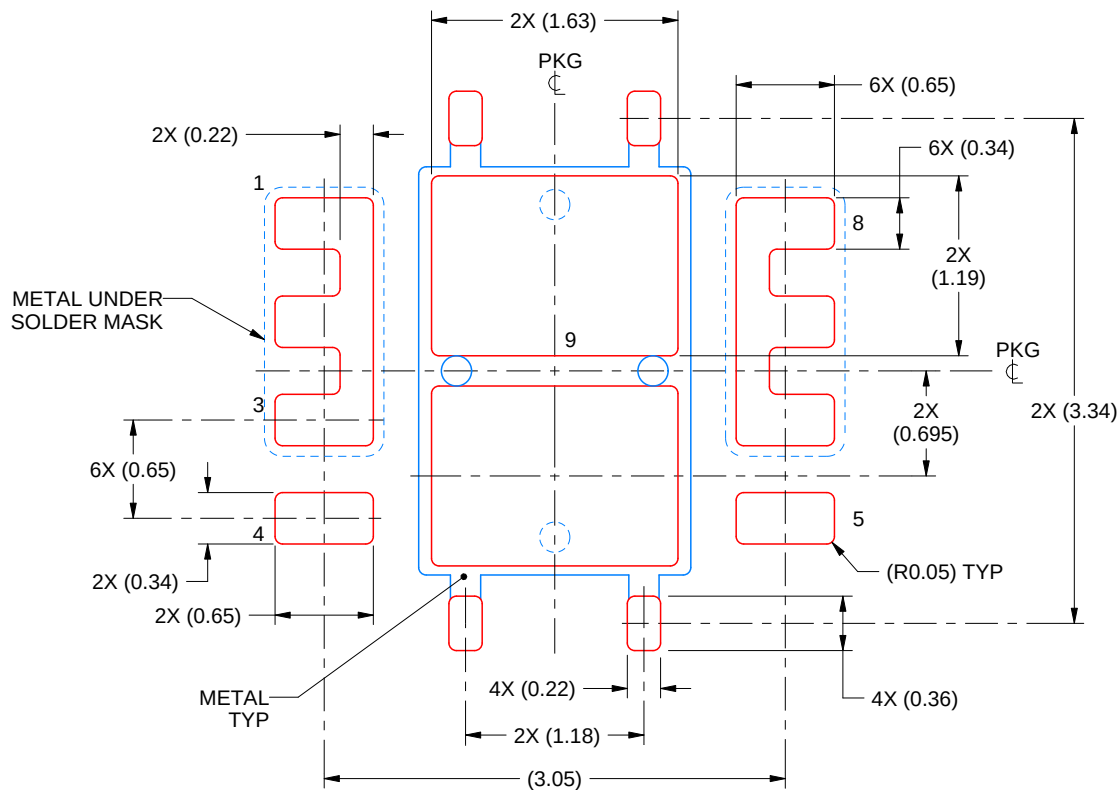
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DPA0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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