CSD75208W1015 Dual 20-V Common Source P-Channel NexFET™ Power MOSFET

1 Features

- Dual P-Channel MOSFETs
- Common Source Configuration
- Small Footprint 1 mm × 1.5 mm
- Gate-Source Voltage Clamp
- Gate ESD Protection –3 kV
- Pb Free
- RoHS Compliant
- Halogen Free

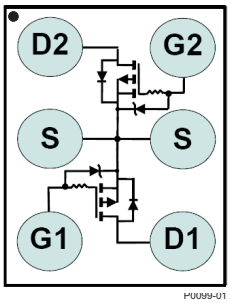
2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This device is designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on-resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	1.9		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.23		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	100	mΩ
		V_{GS} = –2.5 V	70	mΩ
		V_{GS} = –4.5 V	56	mΩ
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	V_{GS} = –1.8 V	190	mΩ
		V_{GS} = –2.5 V	120	mΩ
		V_{GS} = –4.5 V	90	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.8		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD75208W1015	3000	7-Inch Reel	1.0 mm × 1.5 mm Wafer Level Package	Tape and Reel
CSD75208W1015T	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

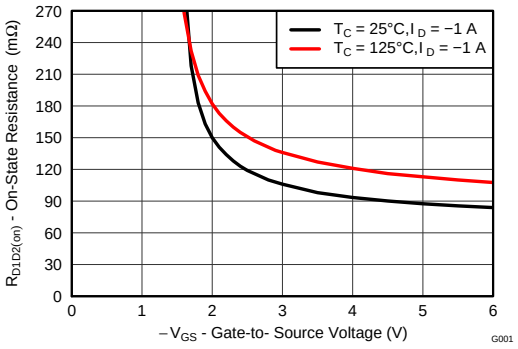
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_{D1D2}	Continuous Drain-to-Drain Current, T_C = 25°C	–1.6	A
	Pulsed Drain-to-Drain Current, T_C = 25°C(1)	–22	A
I_S	Continuous Source Pin Current	–3	A
	Pulsed Source Pin Current(1) (2)	–39	A
I_G	Continuous Gate Clamp Current	–0.5	A
	Pulsed Gate Clamp Current(1)	–7	A
P_D	Power Dissipation	0.75	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

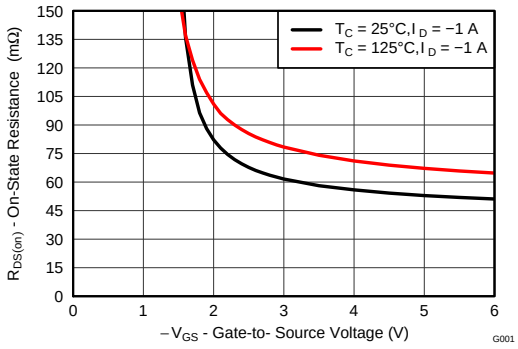
(1) Max $R_{\theta JA}$ = 165°C/W, pulse duration ≤100 µs, duty cycle ≤1%

(2) Both devices in parallel

$R_{D1D2(on)}$ vs V_{GS}



$R_{DS(on)}$ vs V_{GS}



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4 Revision History

Changes from Original (July 2014) to Revision A	Page
• Changed Figure 1.	4
• Added *Community Resources* and *Receiving Notification of Documentation Updates* sections to *Device and Documentation Support*.	7

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

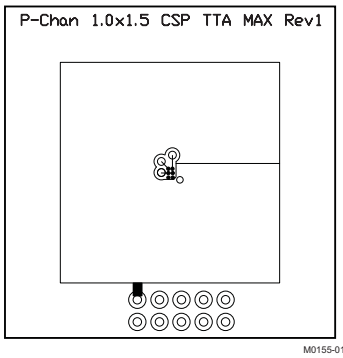
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–20			V
BV_{GSS}	Gate-to-Source Voltage	V_{DS} = 0 V, I_G = –250 μA	–6.1		–7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.5	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_D = –1 A		100	150	mΩ
		V_{GS} = –2.5 V, I_D = –1 A		70	88	mΩ
		V_{GS} = –4.5 V, I_D = –1 A		56	68	mΩ
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	V_{GS} = –1.8 V, I_{D1D2} = –1 A		190	285	mΩ
		V_{GS} = –2.5 V, I_{D1D2} = –1 A		120	150	mΩ
		V_{GS} = –4.5 V, I_{D1D2} = –1 A		90	108	mΩ
g_{fs}	Transconductance	V_{DS} = –2 V, I_D = –1 A		7.5		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		315	410	pF
C_{OSS}	Output Capacitance			132	172	pF
C_{RSS}	Reverse Transfer Capacitance			7.7	10	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –1 A		1.9	2.5	nC
Q_{gd}	Gate Charge, Gate-to-Drain			0.23		nC
Q_{gs}	Gate Charge, Gate-to-Source			0.48		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.31		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		2.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –1 A, R_G = 0 Ω		9		ns
t_r	Rise Time			5		ns
$t_{d(off)}$	Turn Off Delay Time			29		ns
t_f	Fall Time			11		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = –1 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = –10 V, I_F = –1 A, di/dt = 200 A/μs		4.3		nC
t_{rr}	Reverse Recovery Time			9		ns

5.2 Thermal Information

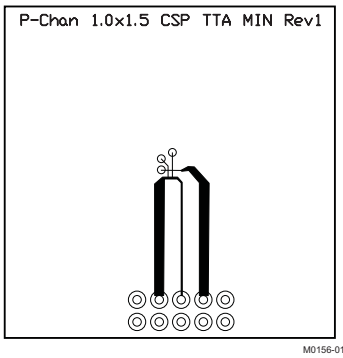
T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1) (2)		165		°C/W
	Junction-to-Ambient Thermal Resistance (2) (3)		95		

(1) Device mounted on FR4 material with minimum Cu mounting area
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Typ $R_{\theta JA}$ = 95°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Typ $R_{\theta JA}$ = 165°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

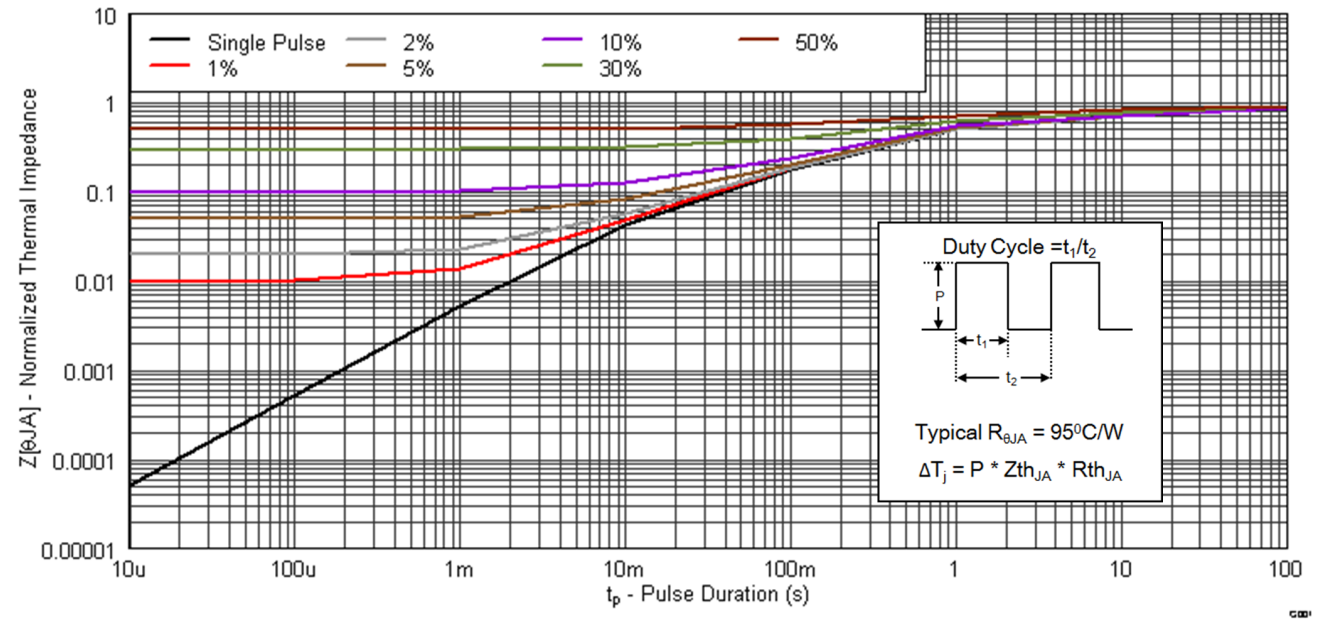


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

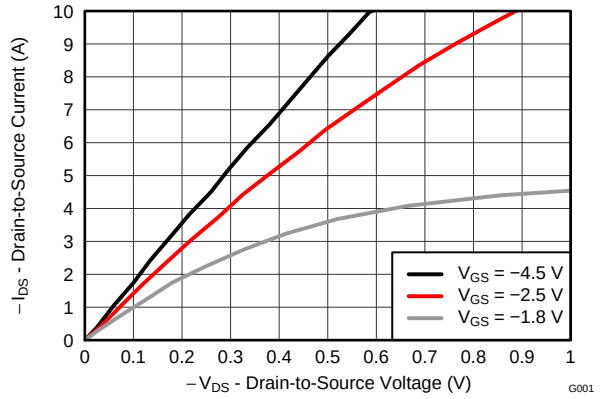


Figure 2. Saturation Characteristics

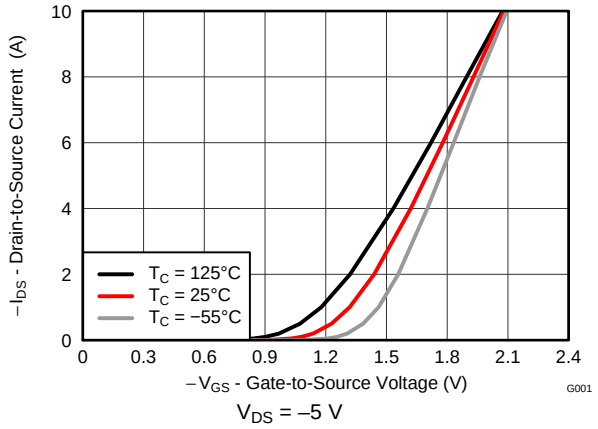


Figure 3. Transfer Characteristics

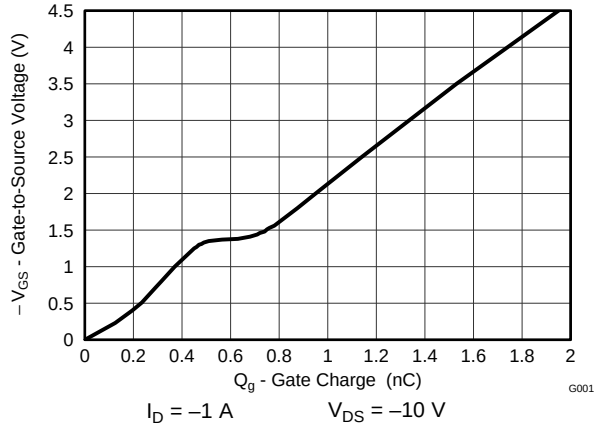


Figure 4. Gate Charge

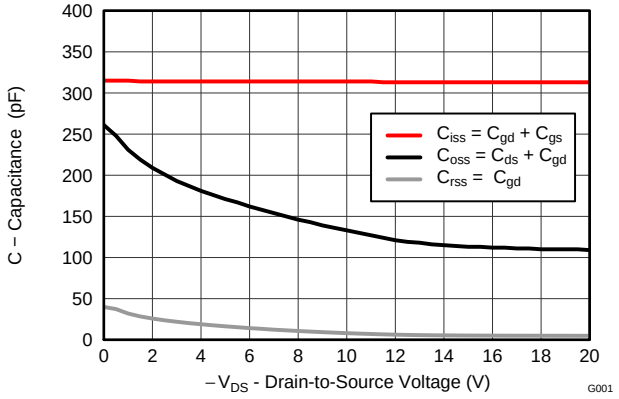


Figure 5. Capacitance

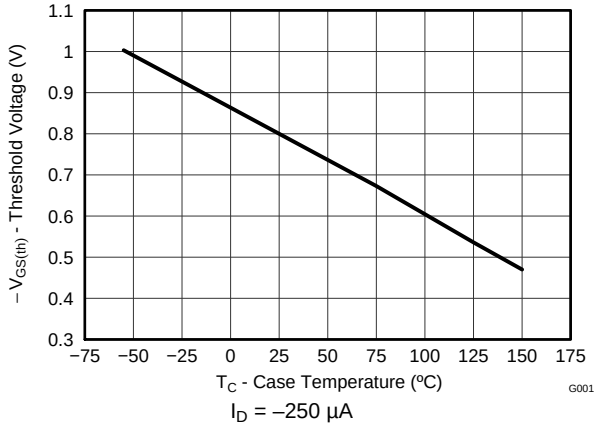


Figure 6. Threshold Voltage vs Temperature

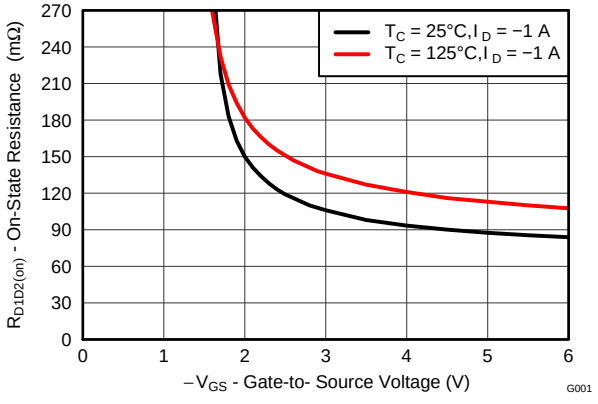


Figure 7. On-State Drain-to-Drain Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

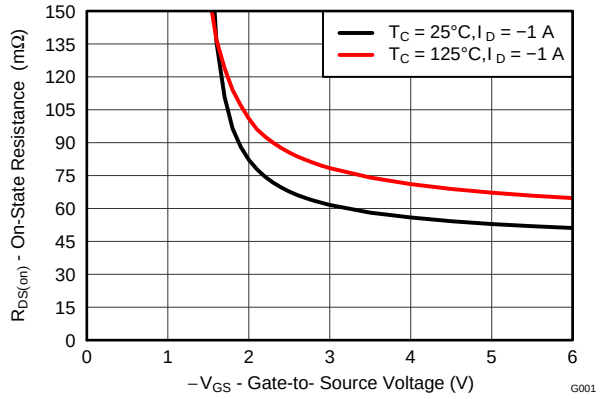


Figure 8. On-State Drain-to-Source Resistance vs Gate-to-Source Voltage

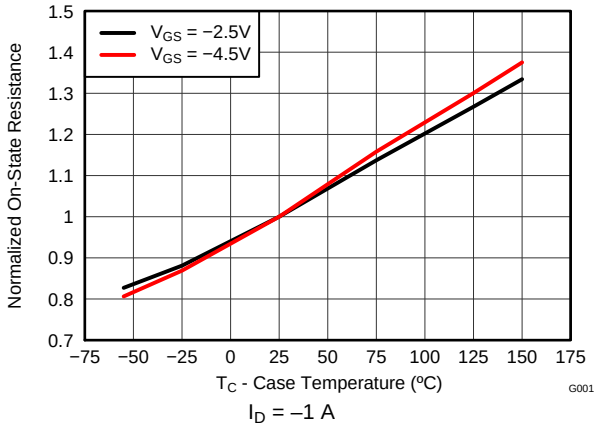


Figure 9. Normalized On-State Resistance vs Temperature

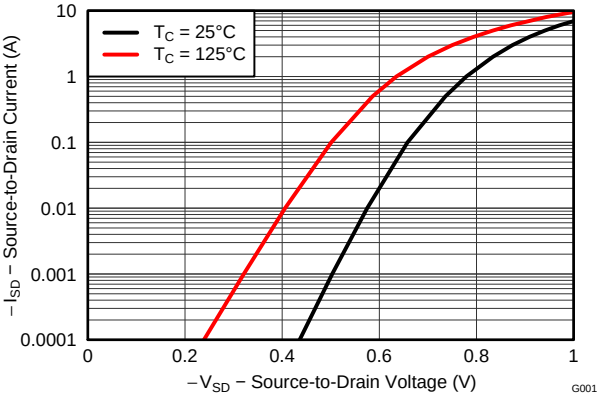


Figure 10. Typical Diode Forward Voltage

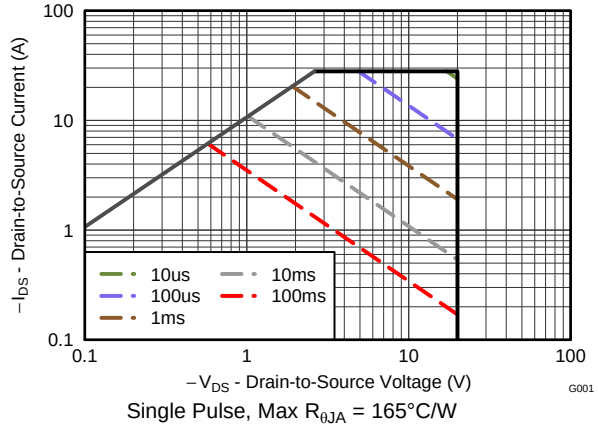


Figure 11. Maximum Safe Operating Area

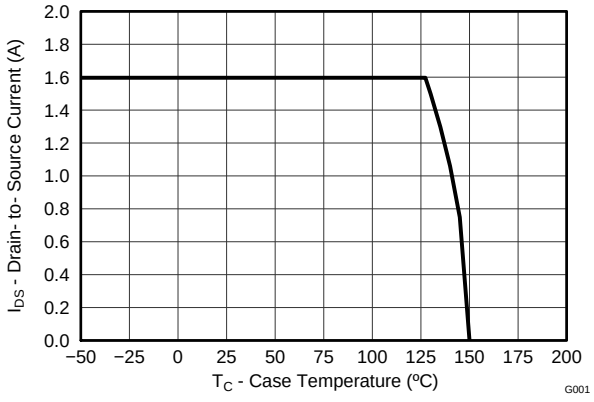


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

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6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

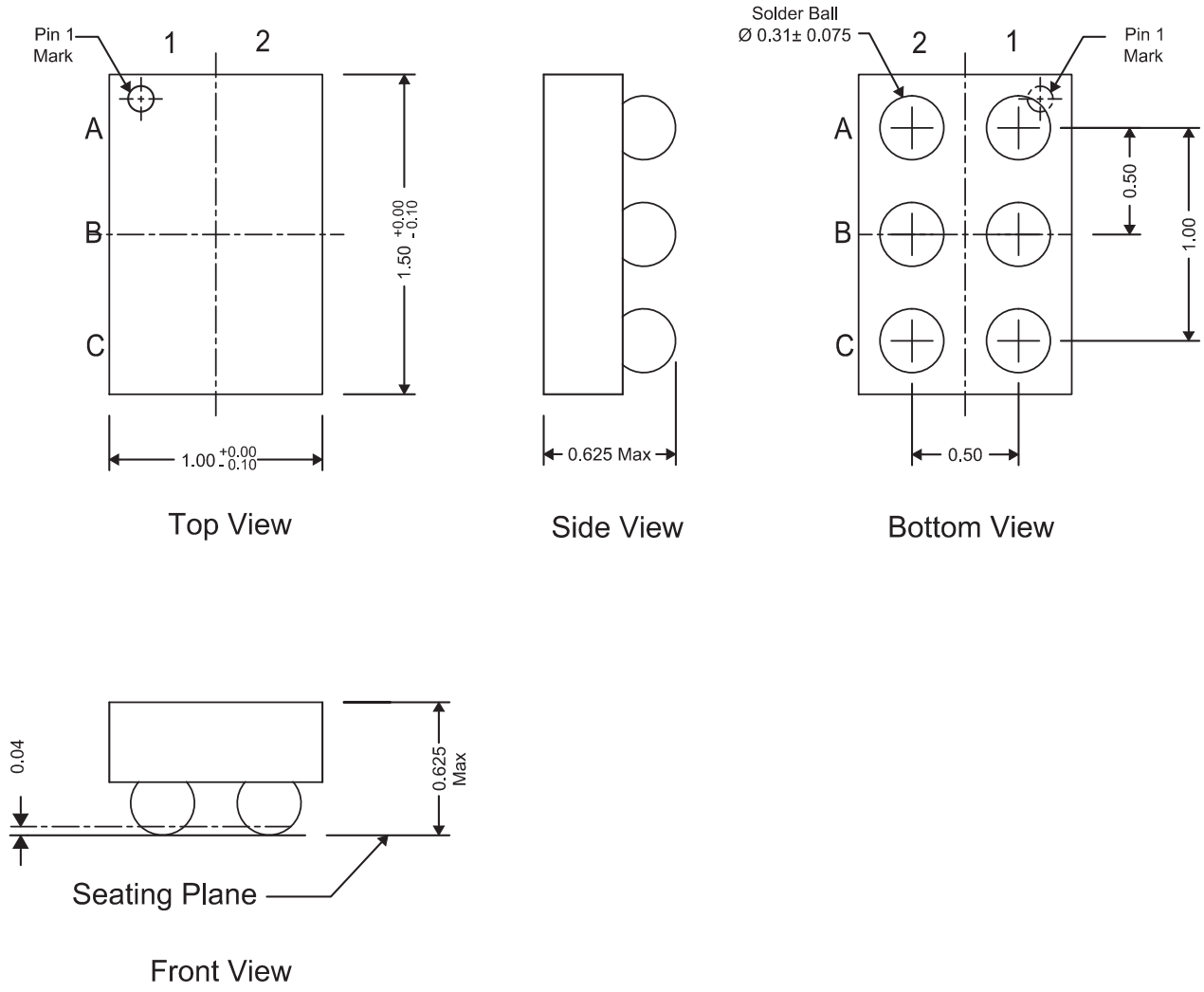
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD75208W1015 Package Dimensions

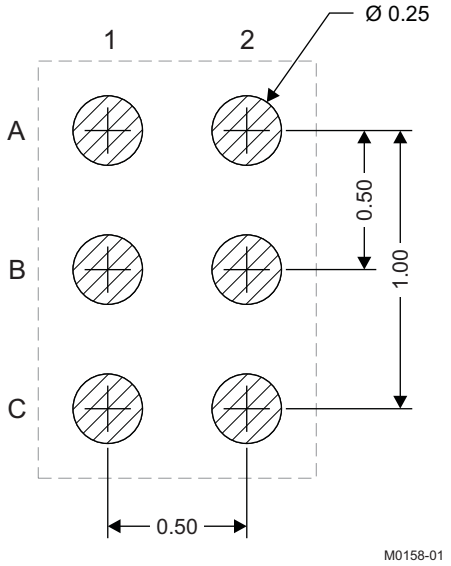


NOTE: All dimensions are in mm (unless otherwise specified).

Table 1. Pinout

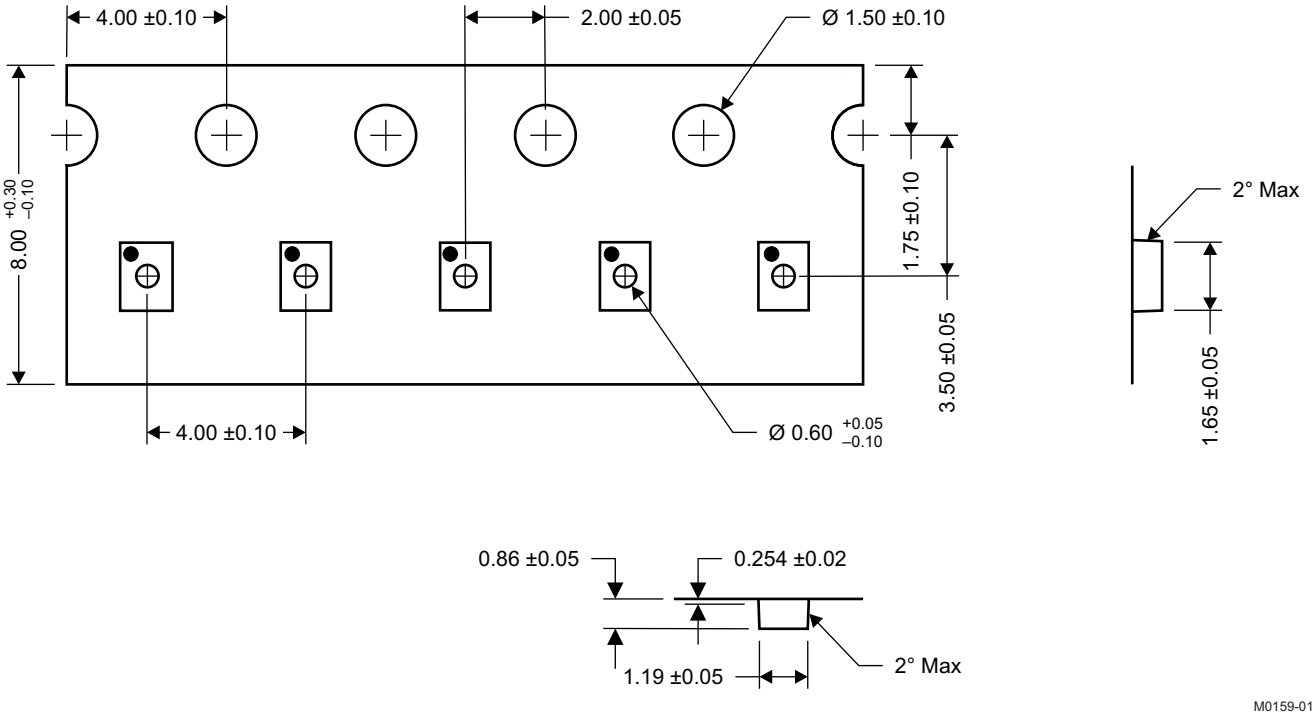
POSITION	DESIGNATION
B1, B2	Source
C1	Gate1
C2	Drain1
A2	Gate2
A1	Drain2

7.2 Recommended PCB Land Pattern



NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD75208W1015	Active	Production	DSBGA (YZC) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75208
CSD75208W1015.B	Active	Production	DSBGA (YZC) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75208
CSD75208W1015T	Active	Production	DSBGA (YZC) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75208
CSD75208W1015T.B	Active	Production	DSBGA (YZC) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75208

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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