



# CSD22204W –8 V P-Channel NexFET™ Power MOSFET

## 1 Features

- Low Resistance
- Small Footprint 1.5 mm × 1.5 mm
- Pb Free
- Gate ESD Protection
- RoHS Compliant
- Halogen Free
- Gate-Source Voltage Clamp

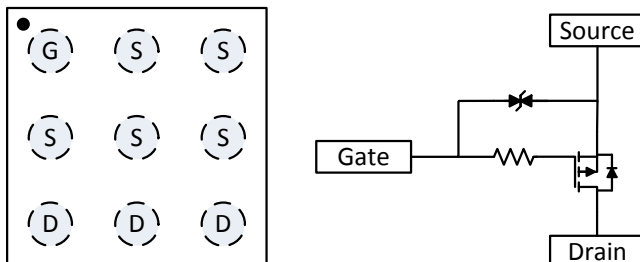
## 2 Applications

- Battery Management
- Battery Protection
- Load Switch Applications

## 3 Description

This –8 V, 8.2 mΩ, 1.5 mm × 1.5 mm device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on-resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View and Circuit Configuration



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	–8		V
$Q_g$	Gate Charge Total (–4.5 V)	18.9		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	4.2		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = -2.5\text{ V}$	11.5	mΩ
		$V_{GS} = -4.5\text{ V}$	8.2	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.7		V

## Ordering Information<sup>(1)</sup>

Device	Qty	Media	Package	Ship
CSD22204W	3000	7-Inch Reel	1.5 mm × 1.5 mm	Tape and Reel
CSD22204WT	250	7-Inch Reel	Wafer BGA Package	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

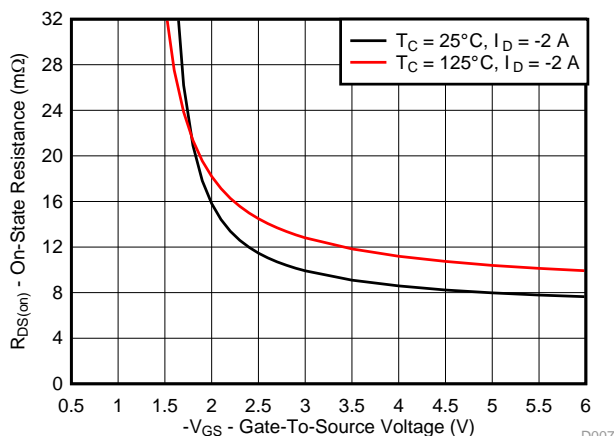
## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–8	V
$V_{GS}$	Gate-to-Source Voltage	–6	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	–5	A
	Pulsed Drain Current <sup>(2)</sup>	–80	A
$P_D$	Power Dissipation	1.7	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	–55 to 150	°C

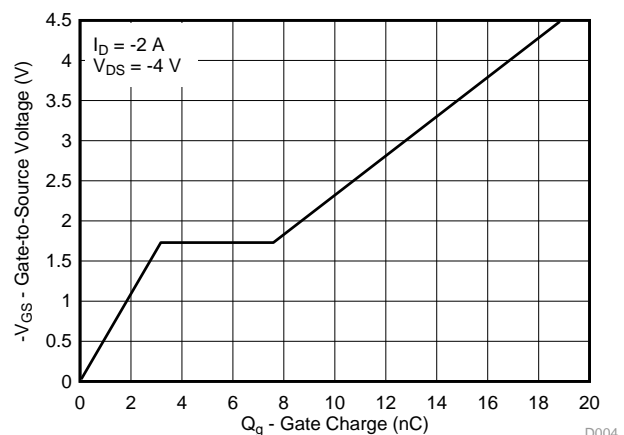
(1) Device operating at a temperature of 105°C.

(2) Typ  $R_{\theta JA} = 75^\circ\text{C/W}$ , Pulse width  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 1\%$ .

$R_{DS(on)}$  vs  $V_{GS}$



Gate Charge



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## 4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-Source Voltage	V <sub>GS</sub> = 0 V, I <sub>DS</sub> = -250 μA	-8			V
BV <sub>GSS</sub>	Gate-to-Source Voltage	V <sub>DS</sub> = 0 V, I <sub>G</sub> = -5 μA	-6			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -6.4 V			-1	μA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -6 V			-4	μA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = -250 μA	-0.45	-0.7	-0.95	V
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> = -2.5 V, I <sub>DS</sub> = -2 A		11.5	14.0	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -2 A		8.2	9.9	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = -0.8 V, I <sub>DS</sub> = -2 A		18		S
DYNAMIC CHARACTERISTICS						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -4 V, f = 1 MHz		870	1130	pF
C <sub>OSS</sub>	Output Capacitance			445	580	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			204	265	pF
R <sub>G</sub>	Series Gate Resistance			300		Ω
Q <sub>g</sub>	Gate Charge Total (-4.5 V)	V <sub>DS</sub> = -4 V, I <sub>D</sub> = -2 A		18.9	24.6	nC
Q <sub>gd</sub>	Gate Charge - Gate-to-Drain			4.2		nC
Q <sub>gs</sub>	Gate Charge - Gate-to-Source			3.2		nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			0.7		nC
Q <sub>OSS</sub>	Output Charge		V <sub>DS</sub> = -4 V, V <sub>GS</sub> = 0 V		3.1	
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = -4 V, V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -2 A, R <sub>G</sub> = 0 Ω		58		ns
t <sub>r</sub>	Rise Time			600		ns
t <sub>d(off)</sub>	Turn Off Delay Time			3450		ns
t <sub>f</sub>	Fall Time			2290		ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>DS</sub> = -2 A, V <sub>GS</sub> = 0 V		-0.7	-1.0	V

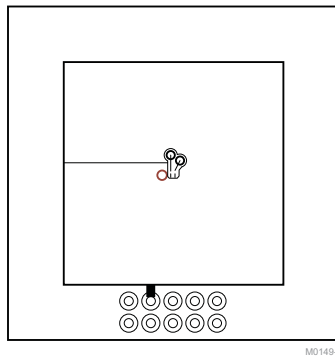
### 5.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

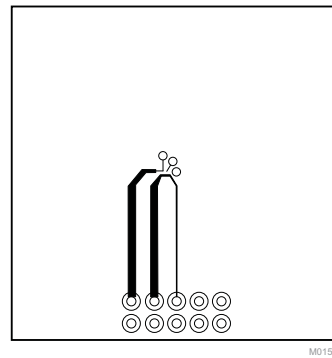
THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1)</sup>	75	$^\circ\text{C/W}$
	Junction-to-Ambient Thermal Resistance <sup>(2)</sup>	230	

(1) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.



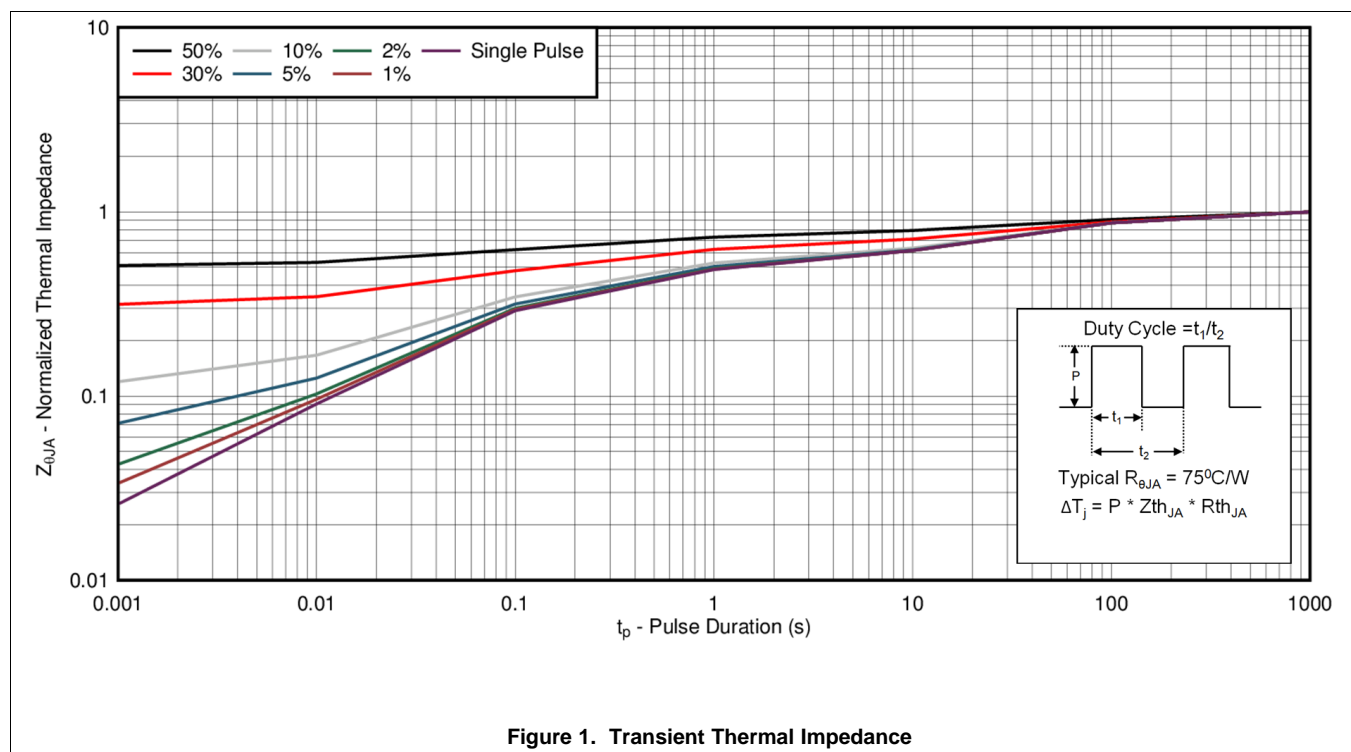
Typ  $R_{\theta JA} = 75^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> of 2 oz. Cu.



Typ  $R_{\theta JA} = 230^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2 oz. Cu.

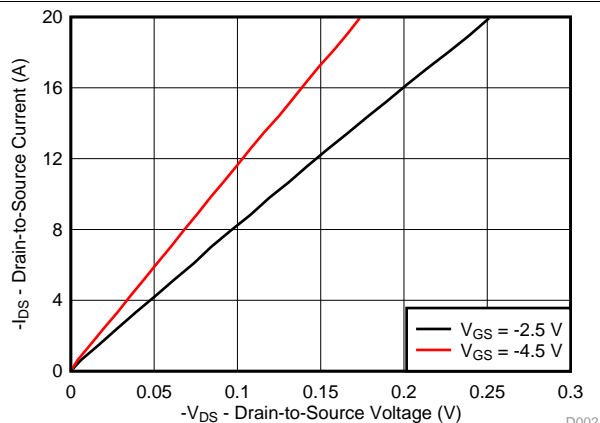
### 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

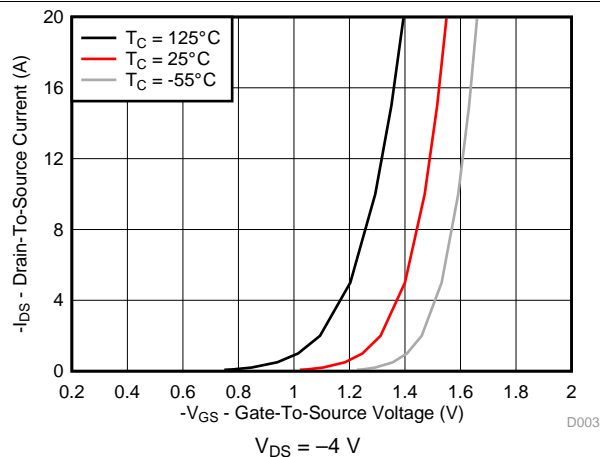


## Typical MOSFET Characteristics (continued)

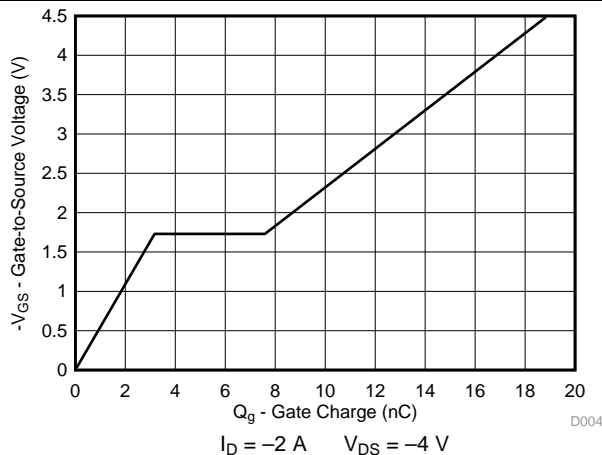
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



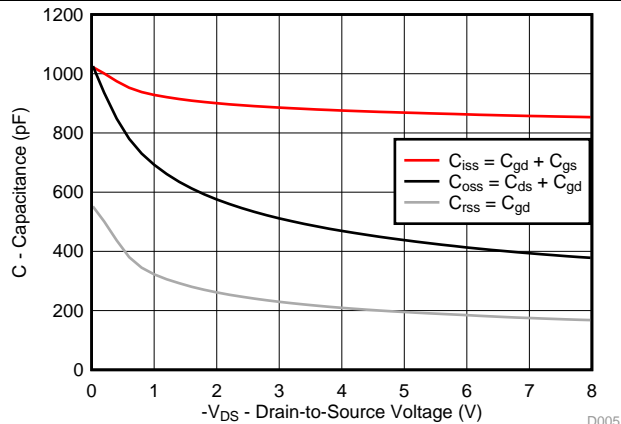
**Figure 2. Saturation Characteristics**



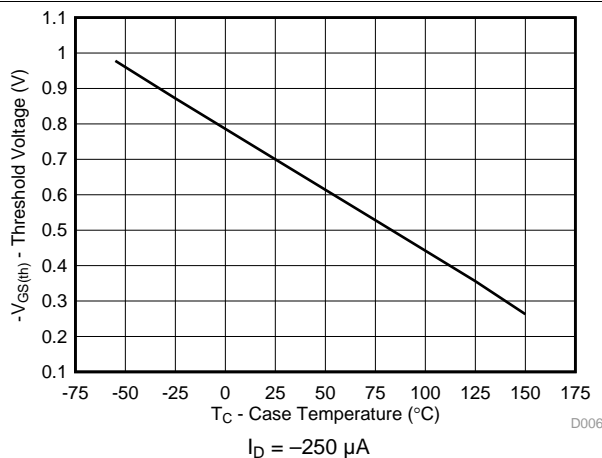
**Figure 3. Transfer Characteristics**



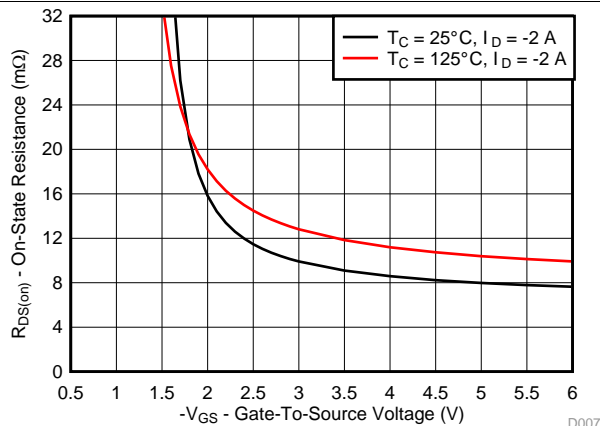
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



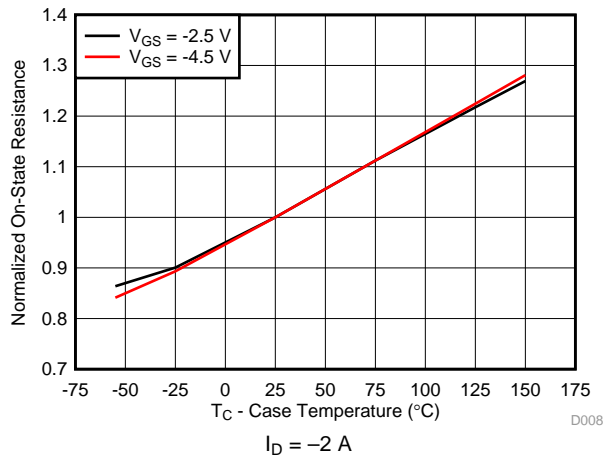
**Figure 6. Threshold Voltage vs Temperature**



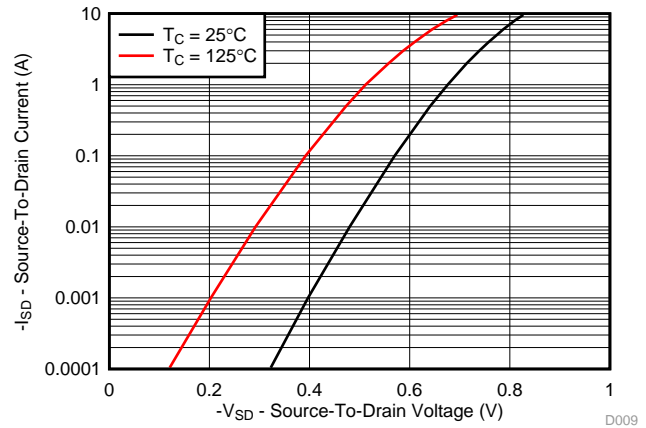
**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

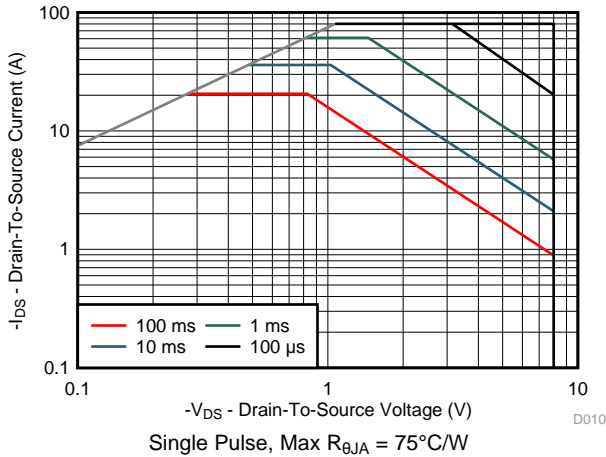
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



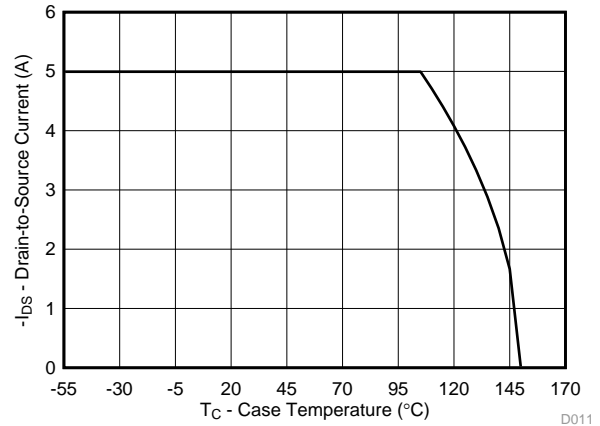
**Figure 8. Normalized On-State Resistance vs Temperature**



**Figure 9. Typical Diode Forward Voltage**



**Figure 10. Maximum Safe Operating Area**



**Figure 11. Maximum Drain Current vs Temperature**

## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

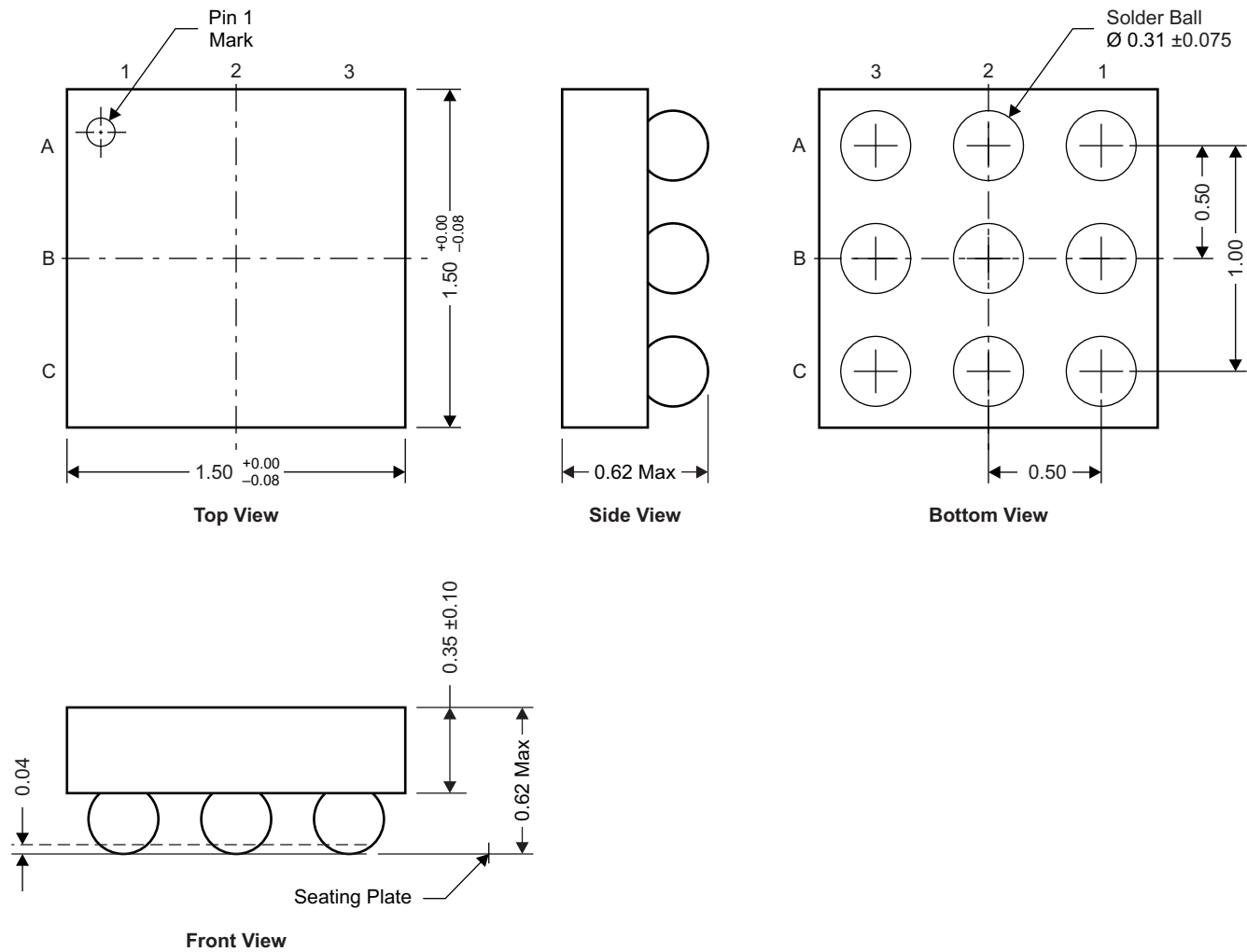
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation

### 7.1 CSD22204W Package Dimensions



NOTE: All dimensions are in mm (unless otherwise specified)

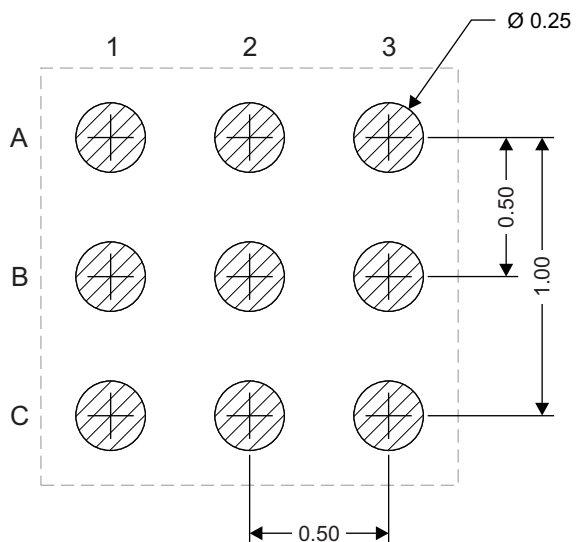
M0171-01

#### Pinout

POSITION	DESIGNATION
A1	Gate
A2, A3, B1, B2, B3	Source
C1, C2, C3	Drain



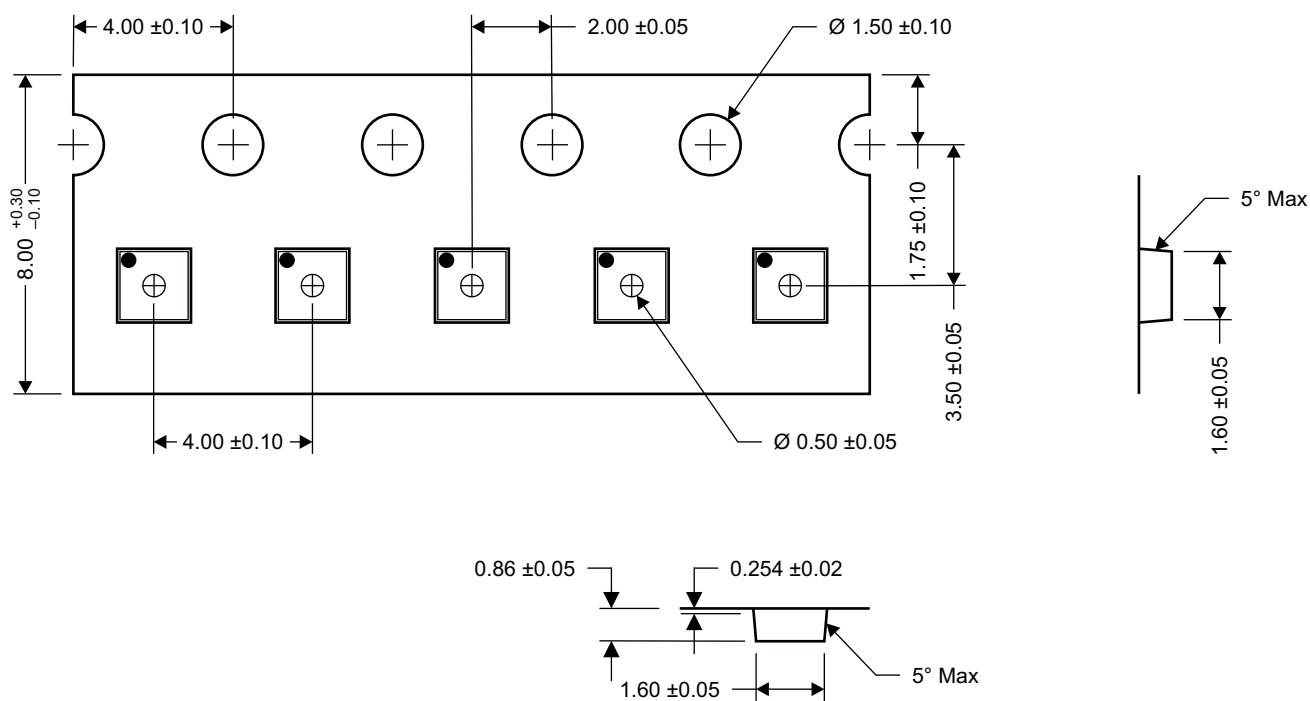
## 7.2 Recommended Land Pattern



M0172-01

NOTE: All dimensions are in mm (unless otherwise specified)

## 7.3 Tape and Reel Information



M0173-01

- NOTES:
1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
  2. Camber not to exceed 1mm in 100 mm, noncumulative over 250 mm
  3. Material: black static-dissipative polystyrene
  4. All dimensions are in mm (unless otherwise specified)
  5. Thickness:  $0.30 \pm 0.05$  mm
  6. MSL1 260°C (IR and convection) PbF reflow compatible

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD22204W	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		22204	<a href="#">Samples</a>
CSD22204WT	ACTIVE	DSBGA	YZF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		22204	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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