CSD22202W15 P-Channel NexFET™ Power MOSFET

1 Features

- Low Resistance
- Small Footprint 1.5 mm × 1.5 mm
- Pb Free
- Gate ESD Protection
- RoHS Compliant
- Halogen Free
- Gate-Source Voltage Clamp

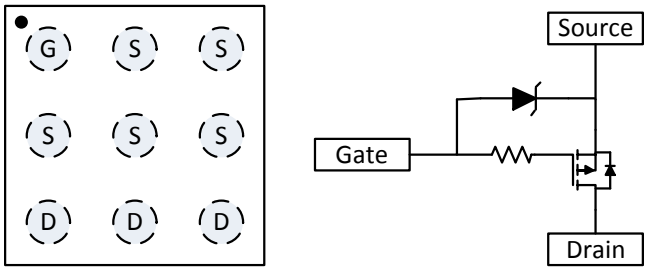
2 Applications

- Battery Management
- Battery Protection
- Load Switch Applications

3 Description

The device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View and Circuit Configuration



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–8		V
Q_g	Gate Charge Total (–4.5 V)	6.5		nC
Q_{gd}	Gate Charge Gate-to-Drain	1		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –2.5 V	14.5	mΩ
		V_{GS} = –4.5 V	10.2	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.8		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD22202W15	3000	7-Inch Reel	1.5 mm × 1.5 mm Wafer BGA Package	Tape and Reel
CSD22202W15T	250	7-Inch Reel		

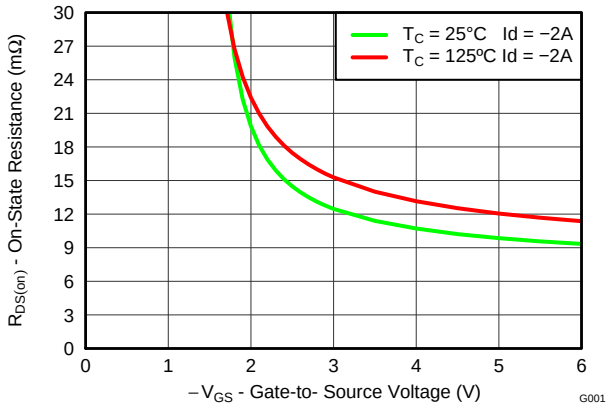
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

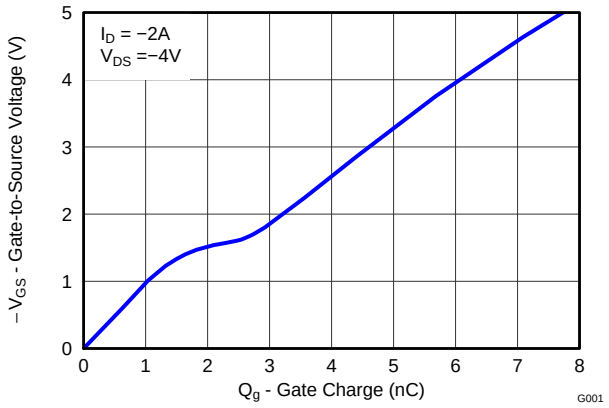
T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–8	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_D	Continuous Drain Current(1) (Silicon Limitted)	–10	A
	Pulsed Drain Current(2)	–48	
I_G	Continuous Gate Current(3)	–0.5	A
P_D	Power Dissipation(1)	1.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) $R_{\theta JA}$ = 75°C/W on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.
(2) Pulse width ≤ 300 µs, duty cycle ≤ 2%
(3) Limited by gate resistance.

$R_{DS(on)}$ vs V_{GS}



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

Changes from Revision A (July 2014) to Revision B **Page**

- Corrected typo, test condition V_{DS} is –6.4 V for I_{DDS} ... 3
- Corrected typo, test condition V_{GS} is –6 V for I_{GSS} ... 3

Changes from Original (June 2013) to Revision A **Page**

- Corrected "Drain to Drain Voltage" to state "Drain-to-Source Voltage" ... 1

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–8			V
BV_{GSS}	Gate-to-Source Voltage	V_{DS} = 0 V, I_G = –250 µA	–6			V
I_{DDS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –6.4 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.6	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –2.5 V, I_{DS} = –2 A		14.5	17.4	mΩ
		V_{GS} = –4.5 V, I_{DS} = –2 A		10.2	12.2	mΩ
g_{fs}	Transconductance	V_{DS} = –4 V, I_{DS} = –2 A		15.3		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –4 V, f = 1 MHz		1060	1390	pF
C_{OSS}	Output Capacitance			588	765	pF
C_{RSS}	Reverse Transfer Capacitance			192	250	pF
R_G	Series Gate Resistance			28		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –4 V, I_D = –2 A		6.5	8.4	nC
Q_{gd}	Gate Charge - Gate-to-Drain			1		nC
Q_{gs}	Gate Charge - Gate-to-Source			1.6		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.8		nC
Q_{OSS}	Output Charge	V_{DS} = –4 V, V_{GS} = 0 V		2.7		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –4 V, V_{GS} = –4.5 V, I_{DS} = –2 A, R_G = 10 Ω		10.4		ns
t_r	Rise Time			8.4		ns
$t_{d(off)}$	Turn Off Delay Time			109		ns
t_f	Fall Time			38		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = –2 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS} = –4 V, I_F = –2 A, di/dt = 200 A/µs		22		nC
t_{rr}	Reverse Recovery Time			19		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1)	75	°C/W
	Junction-to-Ambient Thermal Resistance (2)	210	

(1) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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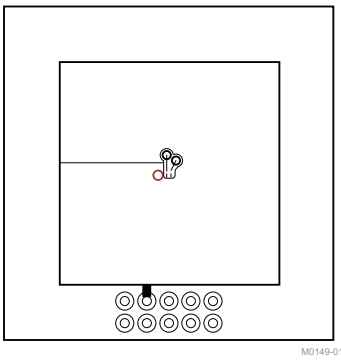
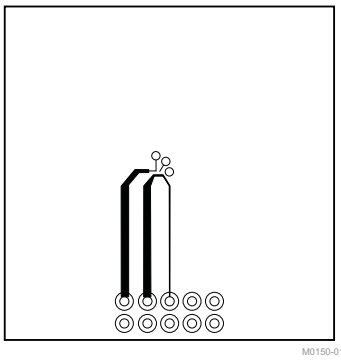


Typ $R_{\theta JA}$ = 75°C/W when mounted on 1inch^2 of 2 oz. Cu.



Typ $R_{\theta JA}$ = 210°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

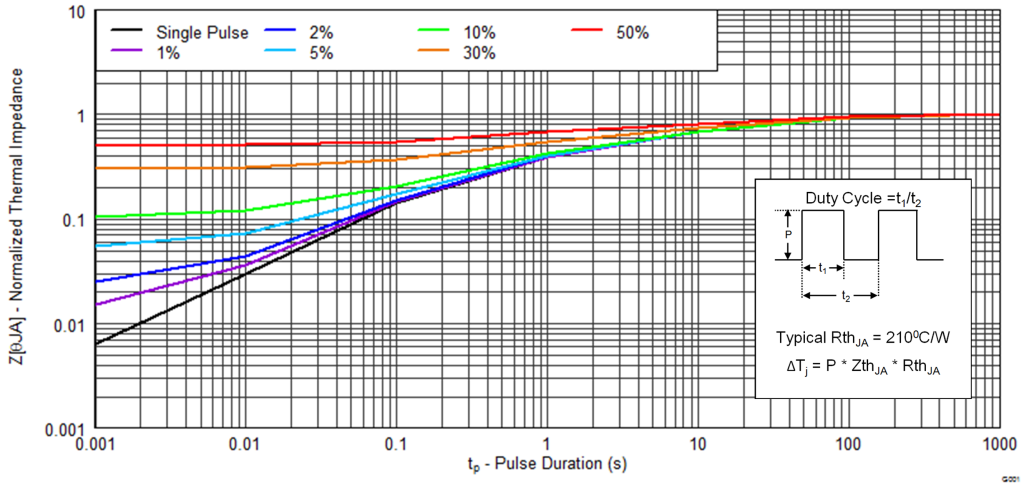


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

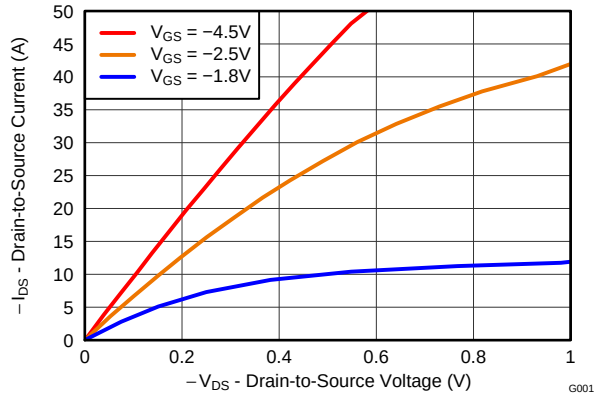

Figure 2. Saturation Characteristics

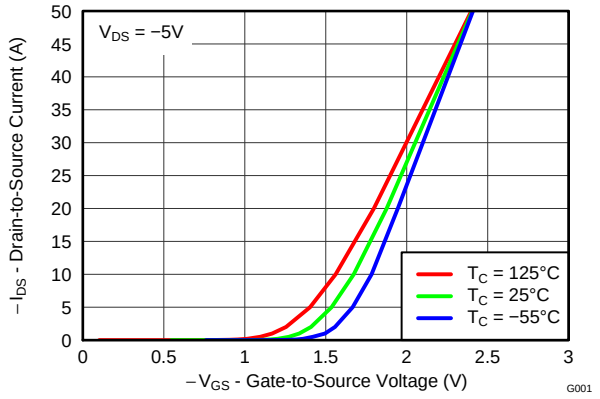

Figure 3. Transfer Characteristics

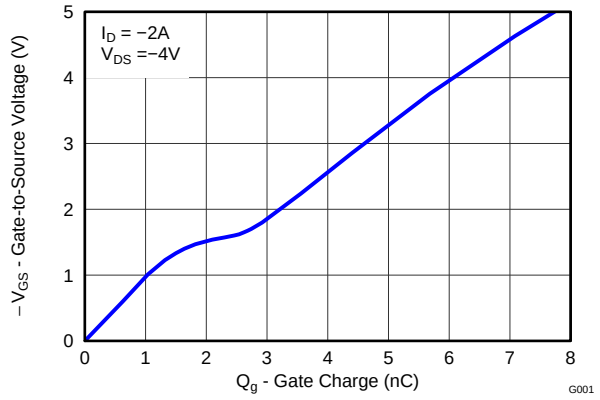

Figure 4. Gate Charge

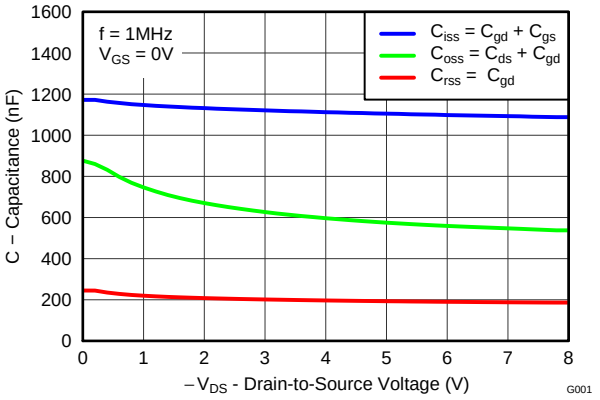

Figure 5. Capacitance

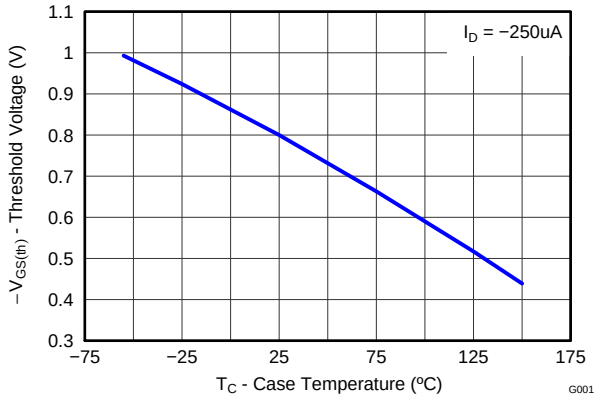

Figure 6. Threshold Voltage vs Temperature

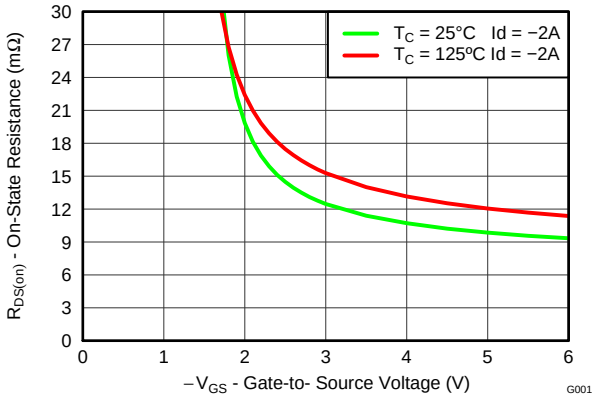

Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

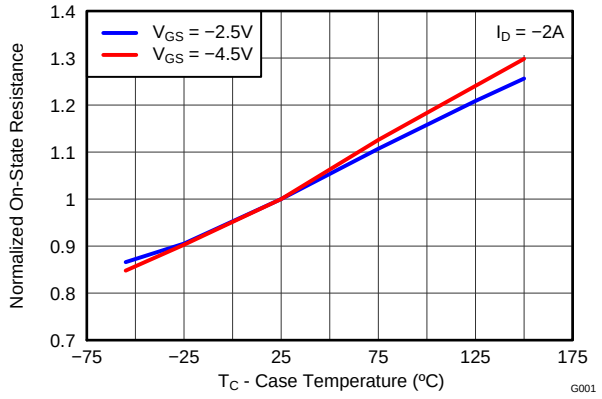

Figure 8. Normalized On-State Resistance vs Temperature

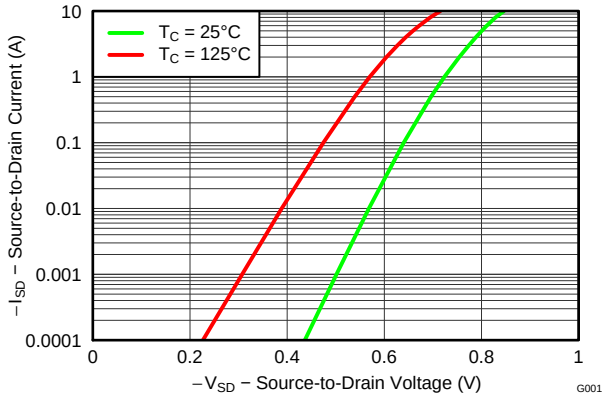

Figure 9. Typical Diode Forward Voltage

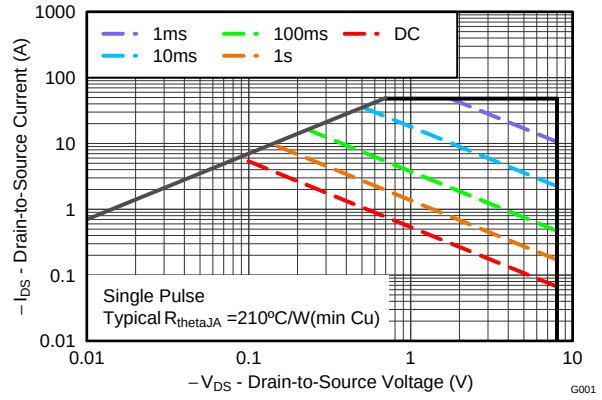

Figure 10. Maximum Safe Operating Area

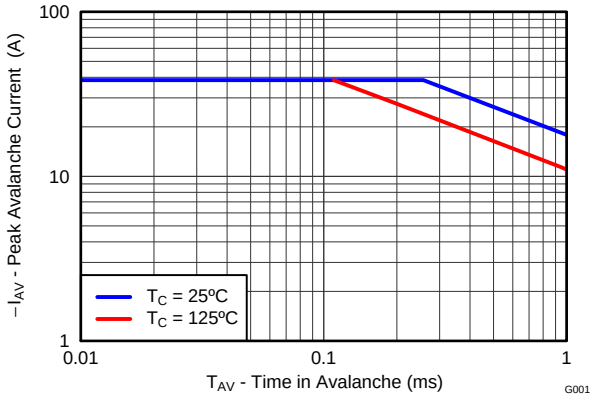

Figure 11. Single Pulse Unclamped Inductive Switching

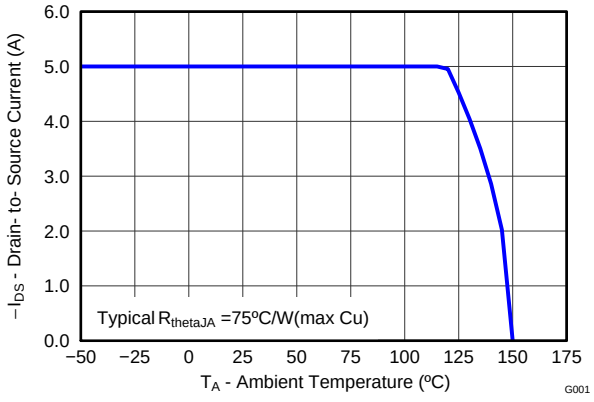

Figure 12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Trademarks

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6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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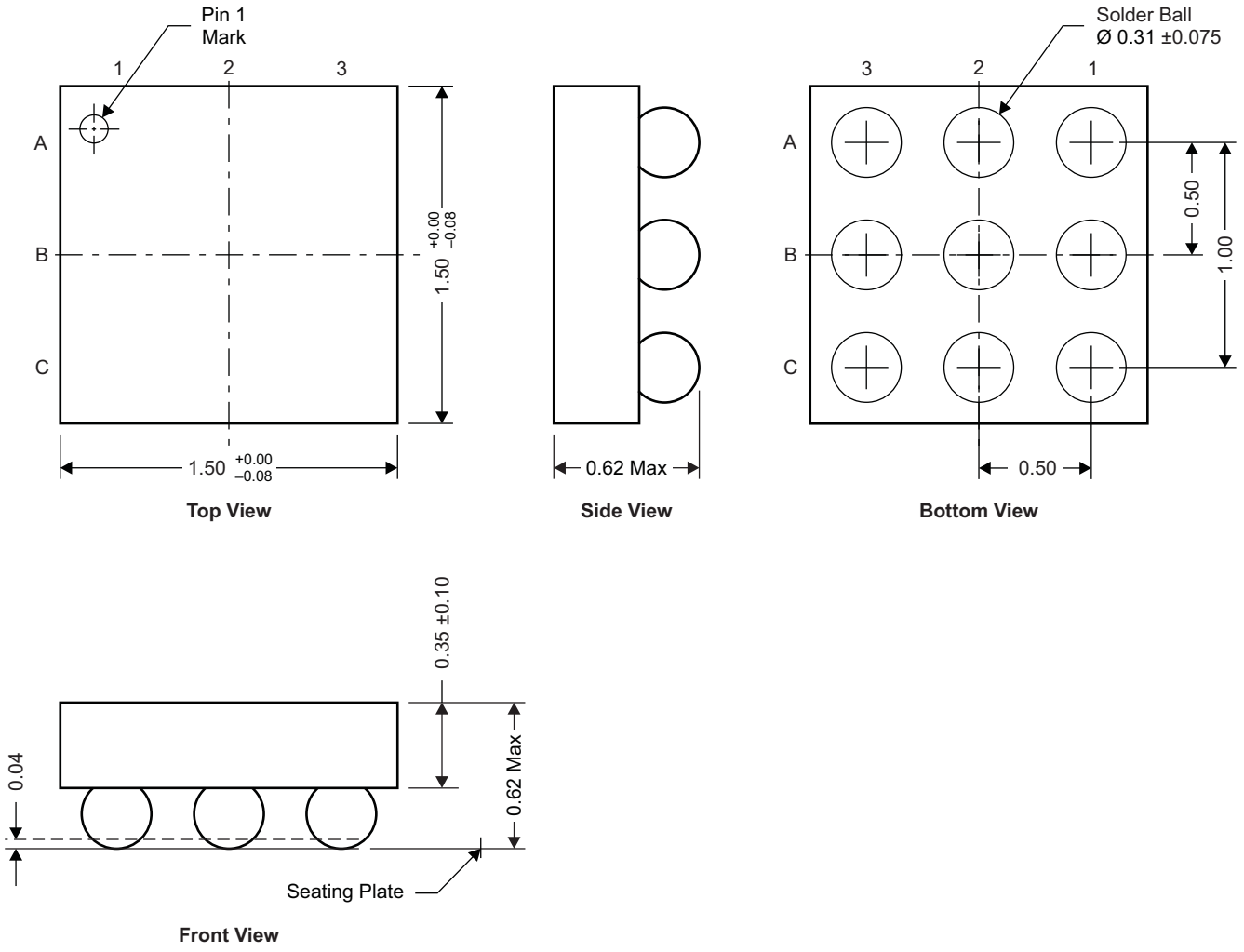
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD22202W15 Package Dimensions



NOTE: All dimensions are in mm (unless otherwise specified)

Table 1. Pinout

POSITION	DESIGNATION
A1	Gate
A2, A3, B1, B2, B3	Source
C1, C2, C3	Drain

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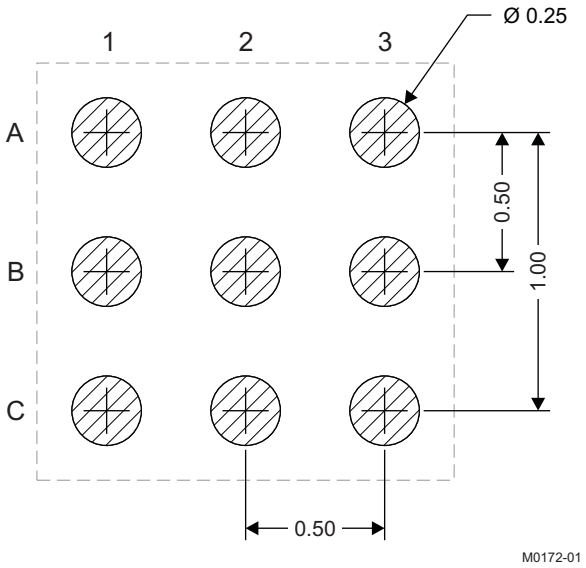
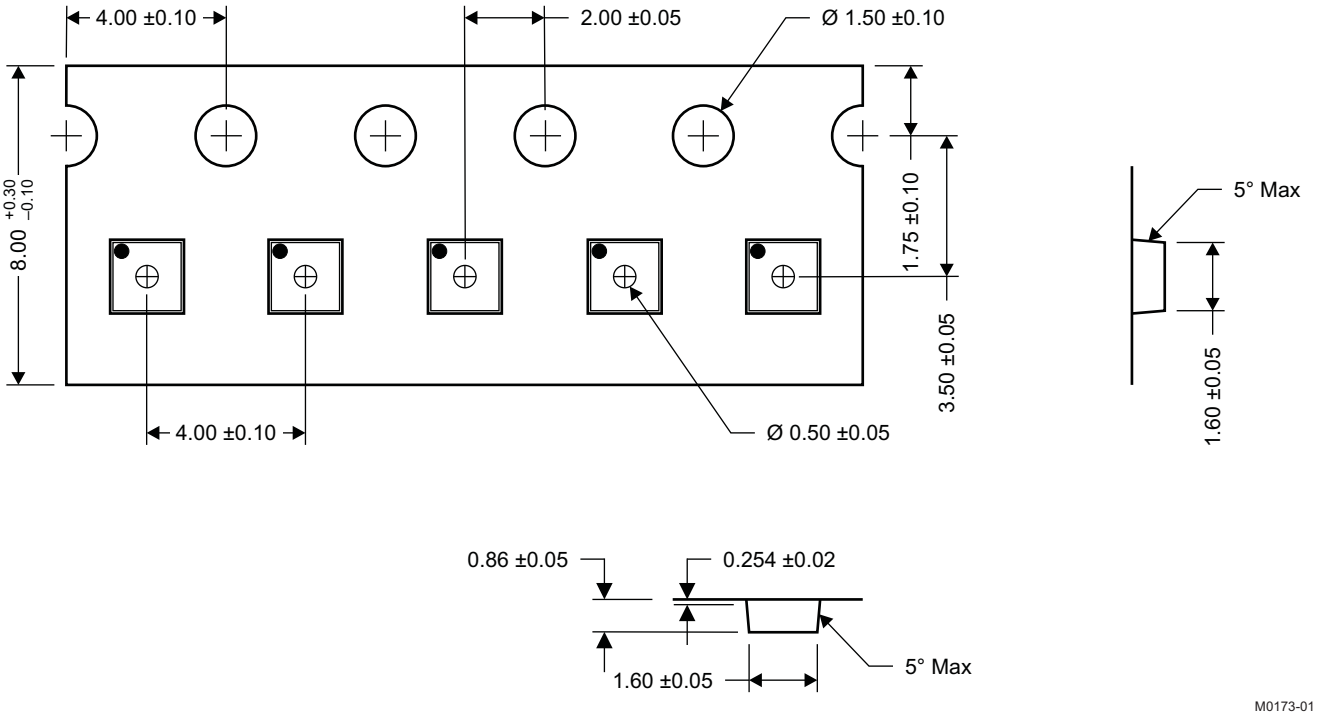
7.2 Recommended Land Pattern



NOTE: All dimensions are in mm (unless otherwise specified)

7.3 Tape and Reel Information



NOTES:
1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and convection) PbF-reflow compatible

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD22202W15	Active	Production	DSBGA (YZF) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22202
CSD22202W15.B	Active	Production	DSBGA (YZF) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22202

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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