

CSD19537Q3 100V、N チャネル NexFET™ パワー MOSFET

1 特長

- 非常に低い Q_g および Q_{gd}
- 低い熱抵抗
- アバランシェ定格
- 鉛不使用の端子メッキ処理
- RoHS に準拠
- ハロゲン不使用
- SON 3.3mm × 3.3mm プラスチック・パッケージ

2 アプリケーション

- 1 次側の絶縁コンバータ
- モーター制御

3 概要

この 100V、12.1mΩ、SON 3.3mm × 3.3mm の NexFET™ パワー MOSFET は、電力変換アプリケーションでの損失を最小限に抑えるように設計されています。

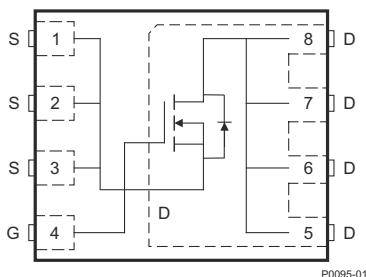


図 3-1.
上面図

製品概要

$T_A = 25^\circ\text{C}$		標準値	単位
V_{DS}	ドレイン - ソース間電圧	100	V
Q_g	ゲートの合計電荷 (10V)	16	nC
Q_{gd}	ゲート - ドレイン間ゲート電荷	2.9	nC
$R_{DS(on)}$	ドレイン - ソース間オン抵抗	$V_{GS} = 6V$	13.8 mΩ
		$V_{GS} = 10V$	12.1 mΩ
$V_{GS(th)}$	スレシヨルド電圧	3	V

注文情報⁽¹⁾

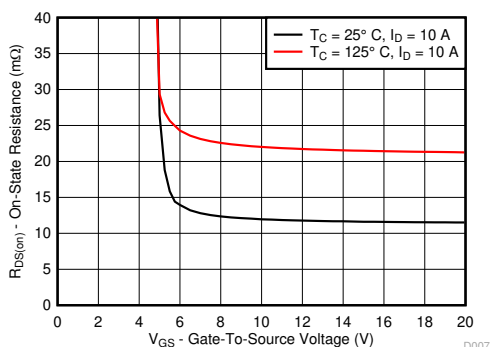
デバイス	メディア	数量	パッケージ	出荷形態
CSD19537Q3	13 インチ・リール	2500	SON 3.3mm × 3.3mm	テープ・アンド・リール
CSD19537Q3T	13 インチ・リール	250	プラスチック・パッケージ	リール

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

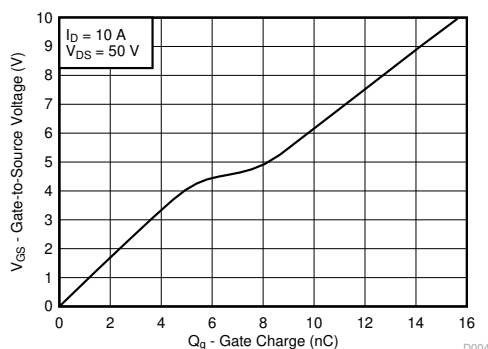
絶対最大定格

$T_A = 25^\circ\text{C}$		値	単位
V_{DS}	ドレイン - ソース間電圧	100	V
V_{GS}	ゲート - ソース間電圧	±20	V
I_D	連続ドレイン電流 (パッケージ制限)	50	A
	連続ドレイン電流 (シリコン制限)、 $T_C = 25^\circ\text{C}$	53	A
	連続ドレイン電流 ⁽¹⁾	9.7	A
I_{DM}	パルス・ドレイン電流 ⁽²⁾	219	A
P_D	消費電力 ⁽¹⁾	2.8	W
	消費電力、 $T_C = 25^\circ\text{C}$	83	W
T_J , T_{stg}	動作時の接合部温度、保存温度	-55~150	°C
E_{AS}	アバランシェ・エネルギー、単一パルス $I_D = 33A$, $L = 0.1mH$, $R_G = 25\Omega$	55	mJ

- (1) 厚さ 0.06in の FR4 PCB 上に構築された面積 1in²、2 オンスの Cu パッド上で、標準値 $R_{\theta JA} = 45^\circ\text{C/W}$ です。
- (2) 最大 $R_{\theta JC} = 1.5^\circ\text{C/W}$ 、パルス期間 $\leq 100\mu\text{s}$ 、デューティ・サイクル $\leq 1\%$ 。



$R_{DS(on)}$ と V_{GS} との関係



ゲート電荷



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4 Revision History

Changes from Revision A (May 2016) to Revision B (November 2022)	Page
• Corrected legend on ☒ 5-11	4

Changes from Revision * (August 2015) to Revision A (May 2016)	Page
• Corrected typo in X axis legend on ☒ 5-11	4

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

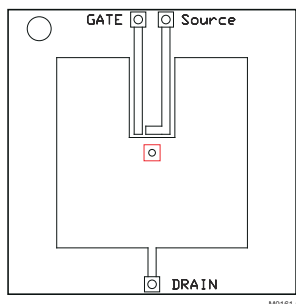
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 80 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.6	3	3.6	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 6 V, I _D = 10 A	13.8		16.6	mΩ
		V _{GS} = 10 V, I _D = 10 A	12.1		14.5	mΩ
g _{fs}	Transconductance	V _{DS} = 10 V, I _D = 10 A	45			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 50 V, f = 1 MHz		1290	1680	pF
C _{oss}	Output capacitance			251	326	pF
C _{rss}	Reverse transfer capacitance			13.3	17.3	pF
R _G	Series gate resistance	V _{DS} = 50 V, I _D = 10 A		1.2	2.4	Ω
Q _g	Gate charge total (10 V)			16	21	nC
Q _{gd}	Gate charge gate-to-drain			2.9		nC
Q _{gs}	Gate charge gate-to-source			5.5		nC
Q _{g(th)}	Gate charge at V _{th}			3.8		nC
Q _{oss}	Output charge		V _{DS} = 50 V, V _{GS} = 0 V		44	
t _{d(on)}	Turn on delay time	V _{DS} = 50 V, V _{GS} = 10 V, I _{DS} = 10 A, R _G = 0 Ω		5		ns
t _r	Rise time			3		ns
t _{d(off)}	Turn off delay time			10		ns
t _f	Fall time			3		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 10 A, V _{GS} = 0 V		0.8	1	V
Q _{rr}	Reverse recovery charge	V _{DS} = 50 V, I _F = 10 A, di/dt = 300 A/μs		134		nC
t _{rr}	Reverse recovery time			36		ns

5.2 Thermal Information

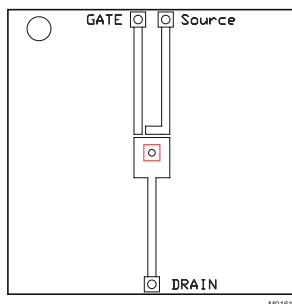
$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance, Note 1 and Note 2 ^{(1) (2)}			55	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in $\times$ 1.5-in (3.81-cm $\times$ 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.



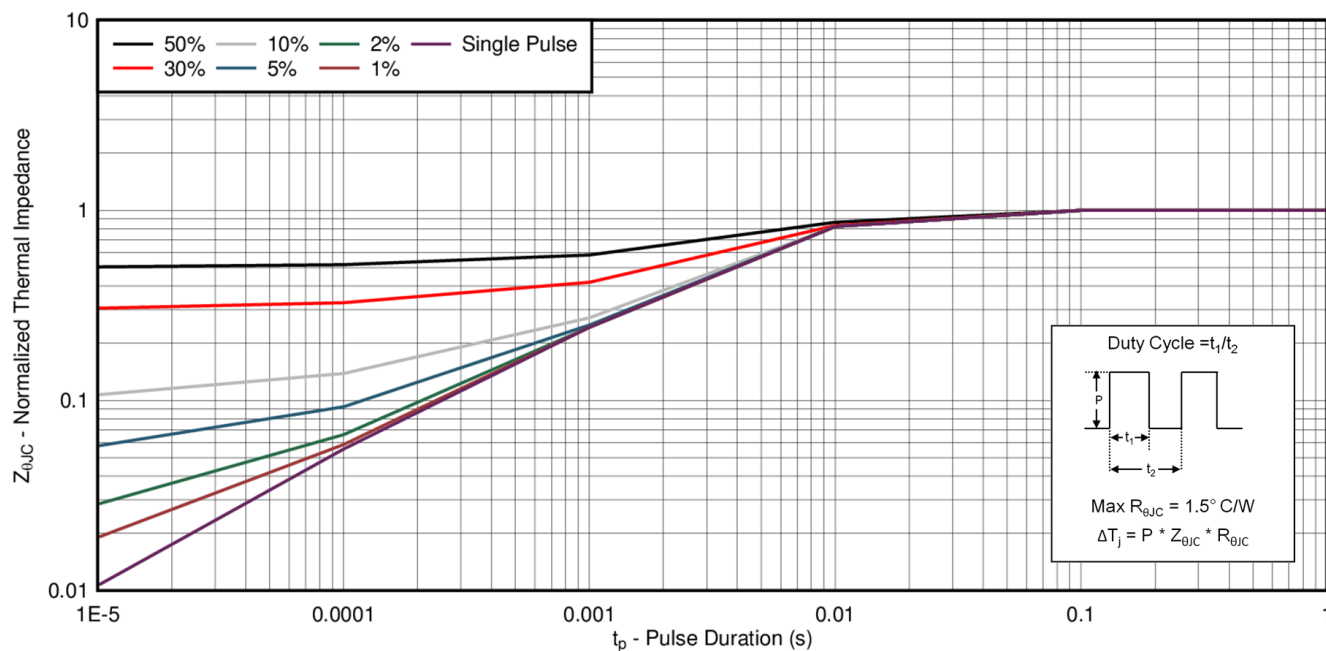
Max $R_{\theta JA} = 55^{\circ}\text{C/W}$ when mounted on 1 in² (6.45 cm²) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA} = 160^{\circ}\text{C/W}$ when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)



5-1. Transient Thermal Impedance

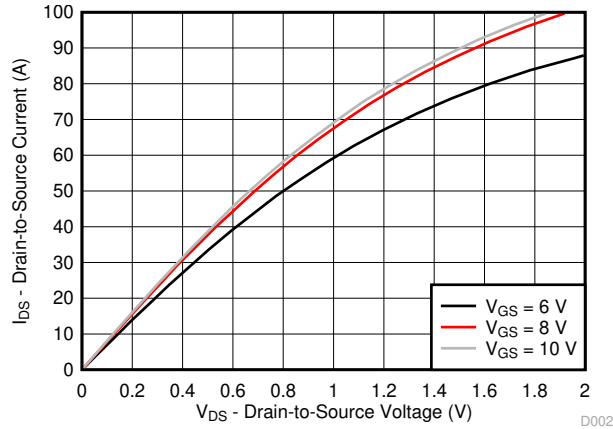


Figure 5-2. Saturation Characteristics

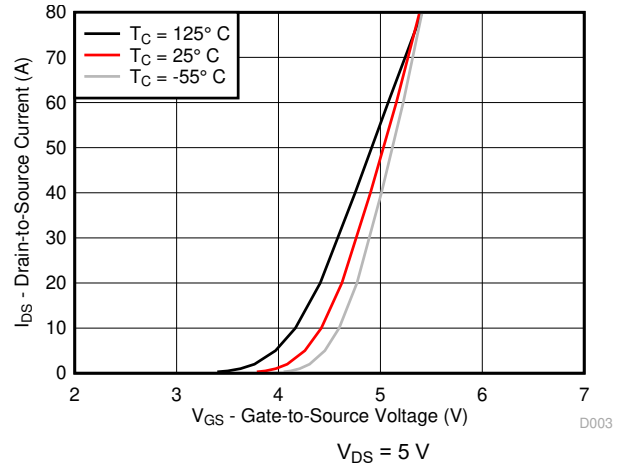


Figure 5-3. Transfer Characteristics

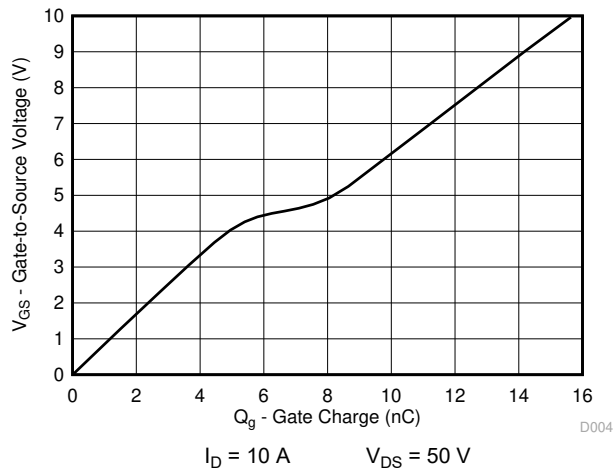


Figure 5-4. Gate Charge

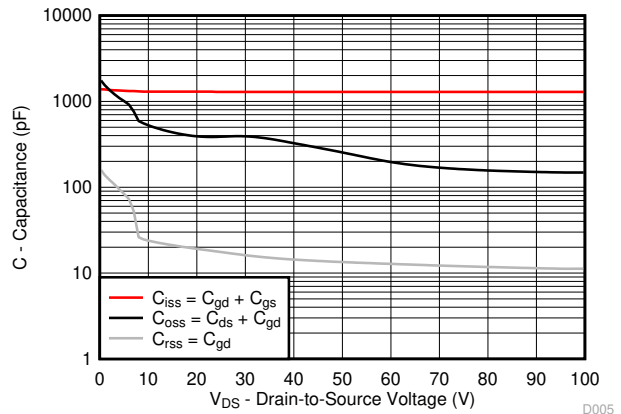


Figure 5-5. Capacitance

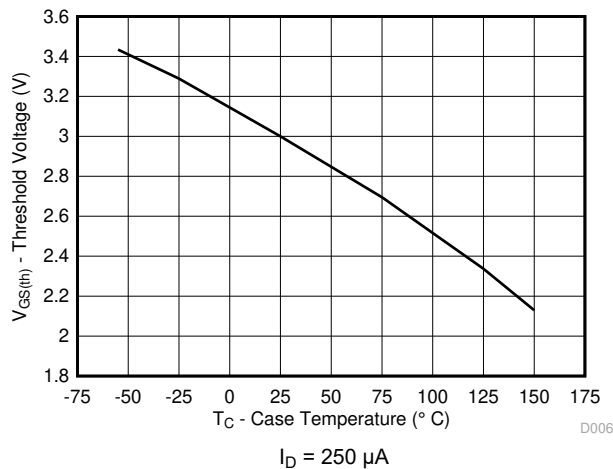


Figure 5-6. Threshold Voltage vs Temperature

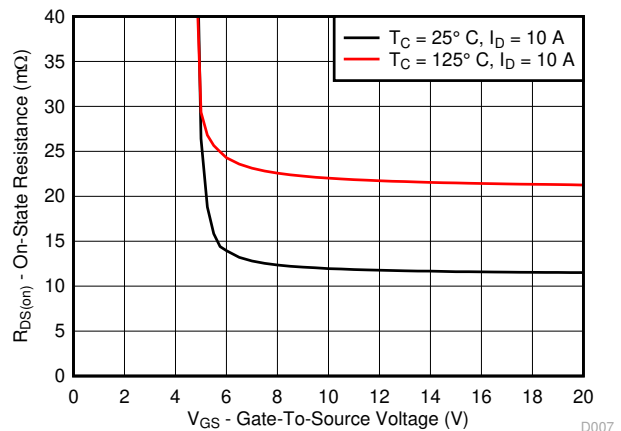
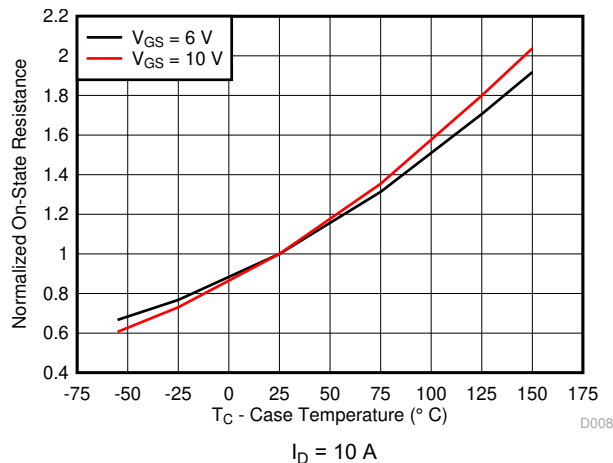
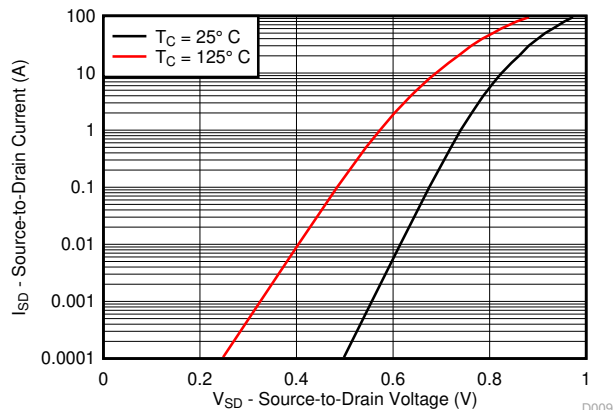


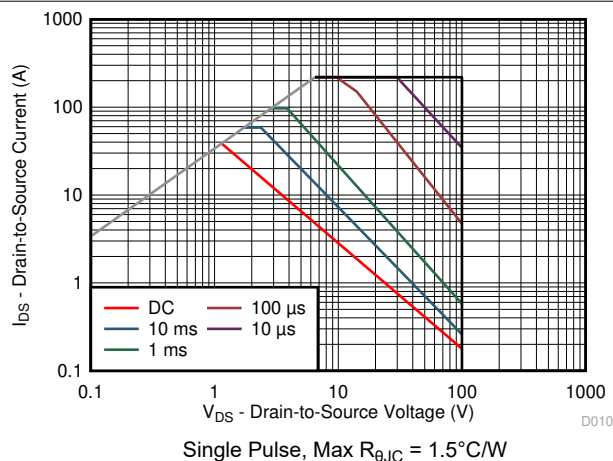
Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



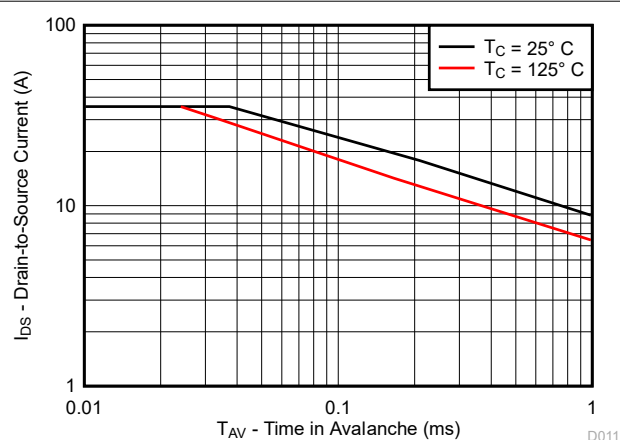
5-8. Normalized On-State Resistance vs Temperature



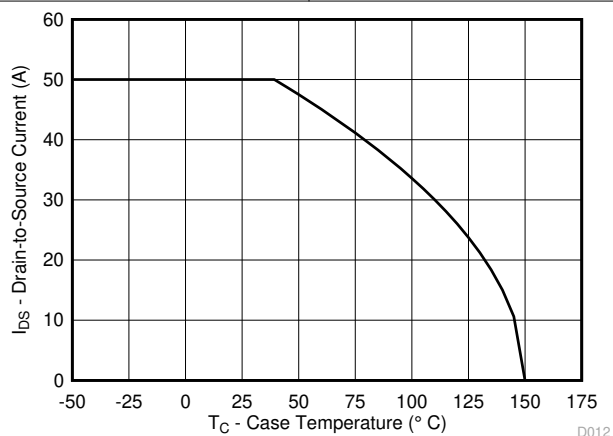
5-9. Typical Diode Forward Voltage



5-10. Maximum Safe Operating Area



5-11. Single Pulse Unclamped Inductive Switching



5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

[TI E2E™ Online Community](#) TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[Design Support](#) TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

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6.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

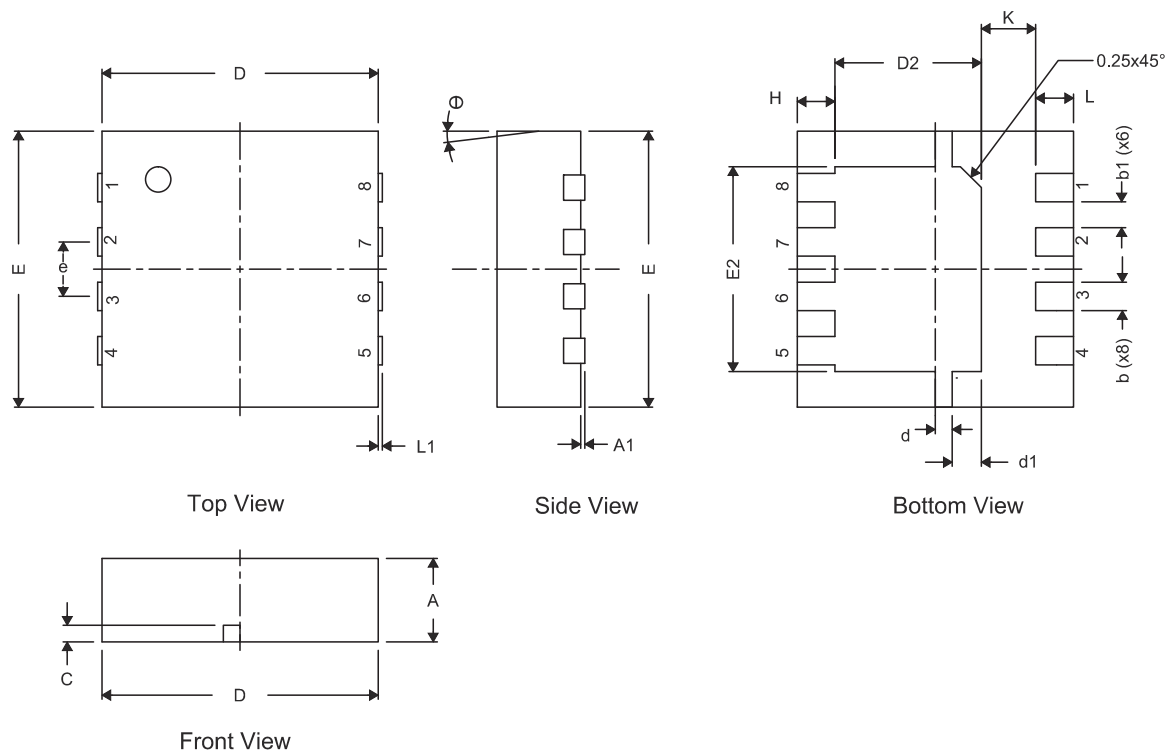
6.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

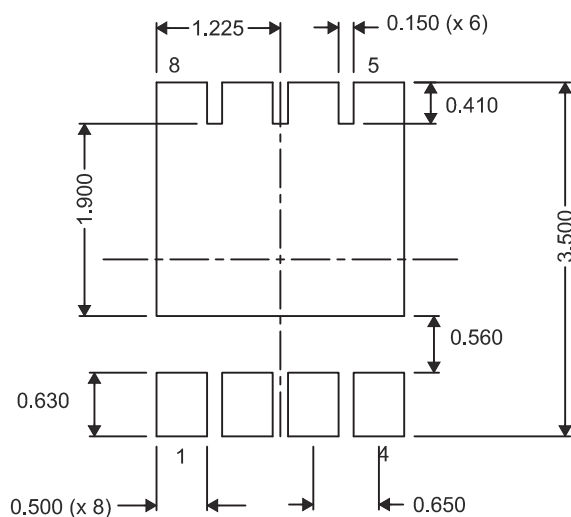
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



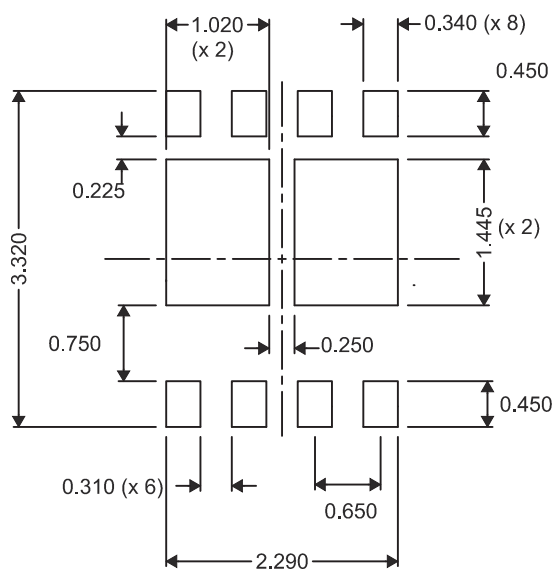
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



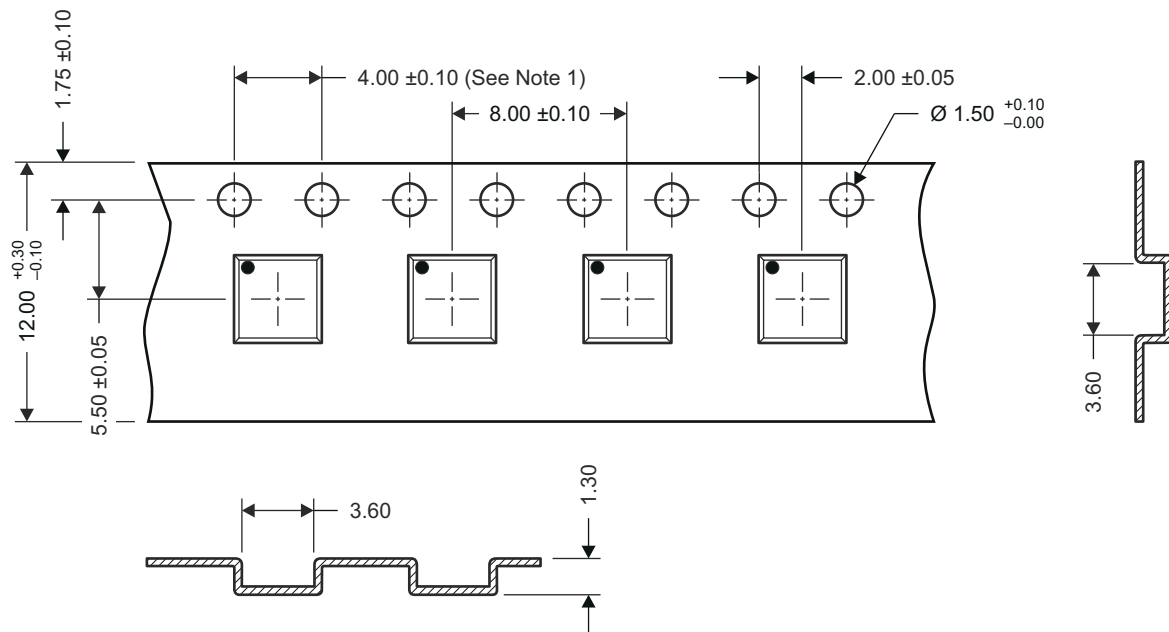
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19537Q3	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537
CSD19537Q3.B	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537
CSD19537Q3T	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537
CSD19537Q3T.B	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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