

CSD18537NQ5A 60-V N-Channel NexFET™ Power MOSFETs

1 Features

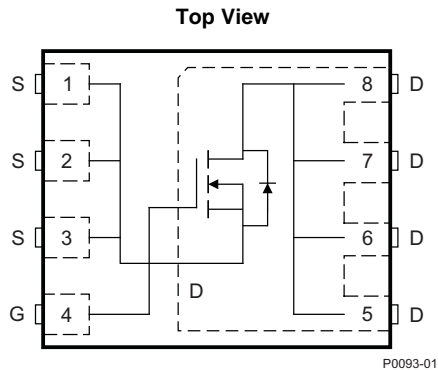
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm x 6 mm Plastic Package

2 Applications

- High-Side Synchronous Buck Converter
- Motor Control

3 Description

This 10 mΩ, 60 V, SON 5 mm x 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	14		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.3		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}$	13	mΩ
		$V_{GS} = 10\text{ V}$	10	mΩ
$V_{GS(th)}$	Threshold Voltage	3		V

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD18537NQ5A	2500	13-Inch Reel	SON 5 x 6 mm Plastic Package	Tape and Reel
CSD18537NQ5AT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package limited)	50	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	54	
	Continuous Drain Current ⁽¹⁾	11	
I_{DM}	Pulsed Drain Current ⁽²⁾	151	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	75	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 33\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	55	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 2.1^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

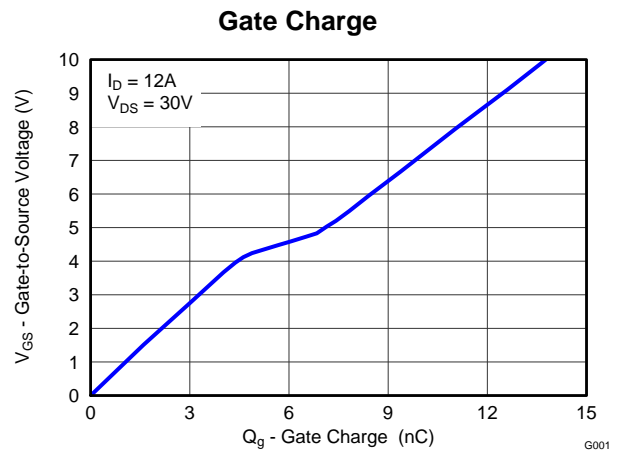
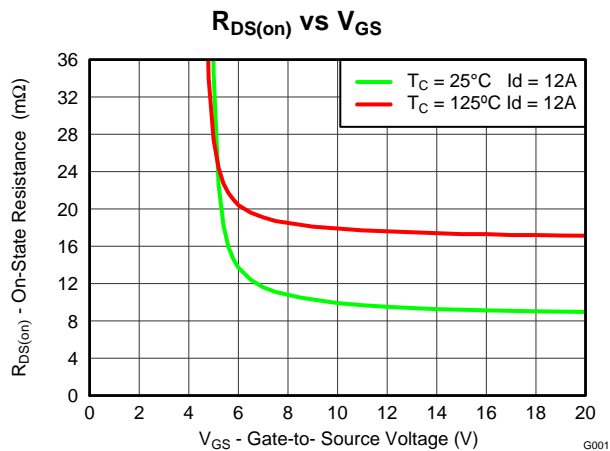


Table of Contents

1 Features	1	6.1 Trademarks	7
2 Applications	1	6.2 Electrostatic Discharge Caution	7
3 Description	1	6.3 Glossary	7
4 Revision History	2	7 Mechanical, Packaging, and Orderable Information	8
5 Specifications	3	7.1 Q5A Package Dimensions	9
5.1 Electrical Characteristics	3	7.2 Recommended PCB Pattern	10
5.2 Thermal Information	3	7.3 Recommended Stencil Opening	11
5.3 Typical MOSFET Characteristics	4	7.4 Q5A Tape and Reel Information	11
6 Device and Documentation Support	7		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2014) to Revision B	Page
• Reduced silicon current limit to 54 A due to increase in $R_{\theta JC}$	1
• Increased pulsed current limit to 151	1
• Added line for maximum power dissipation with case temperature held to 25°C	1
• Updated the pulsed current conditions	1
• Increased the maximum $R_{\theta JC}$ to 2.1 °C/W	3
• Updated Figure 1 from a normalized $R_{\theta JA}$ curve to an $R_{\theta JC}$ curve	4
• Updated Figure 10 to show an improved SOA	5
• Updated Figure 12 to show a 50-A package current limit	5

Changes from Original (June 2013) to Revision A	Page
• Added part number to title	1
• Added more information to description	1
• Updated ordering information to include small reel information	1
• Removed $T_C = 25^\circ\text{C}$ condition from package limited continuous drain current	1

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.6	3	3.5	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}, I_D = 12\text{ A}$		13	17	m Ω
		$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$		10	13	m Ω
g_{fs}	Transconductance	$V_{DS} = 30\text{ V}, I_D = 12\text{ A}$		62		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$		1140	1480	pF
C_{oss}	Output Capacitance			136	177	pF
C_{rss}	Reverse Transfer Capacitance			4	5.2	pF
R_G	Series Gate Resistance			5.5	11	Ω
Q_g	Gate Charge Total (10 V)	$V_{DS} = 30\text{ V}, I_D = 12\text{ A}$		14	18	nC
Q_{gd}	Gate Charge Gate-to-Drain			2.3		nC
Q_{gs}	Gate Charge Gate-to-Source			4.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			3.3		nC
Q_{oss}	Output Charge	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$		25		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 12\text{ A}, R_G = 0\ \Omega$		5.8		ns
t_r	Rise Time			4		ns
$t_{d(off)}$	Turn Off Delay Time			14.4		ns
t_f	Fall Time			3.2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	$I_{SD} = 12\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 30\text{ V}, I_F = 12\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		54		nC
t_{rr}	Reverse Recovery Time			40		ns

5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance ⁽¹⁾			2.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			50	

- $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches x 1.5-inches (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

CSD18537NQ5A

SLPS391B – JUNE 2013 – REVISED JULY 2014

www.ti.com



Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

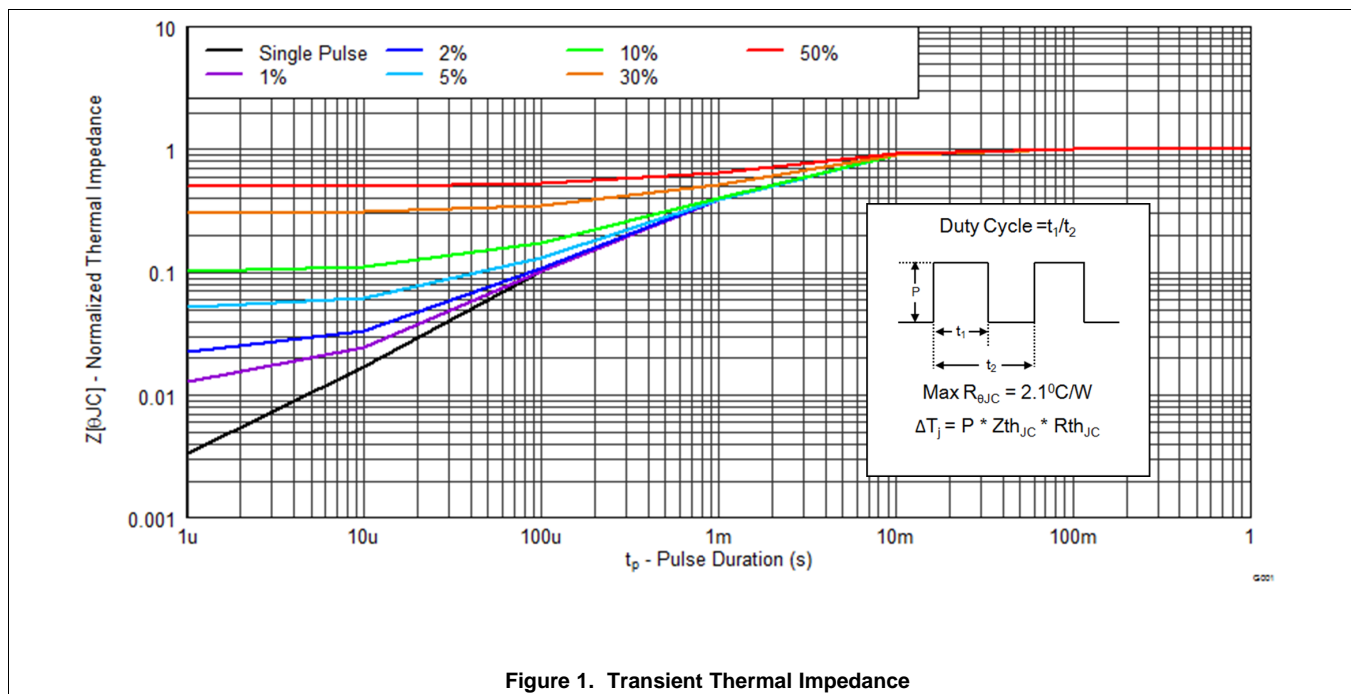


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

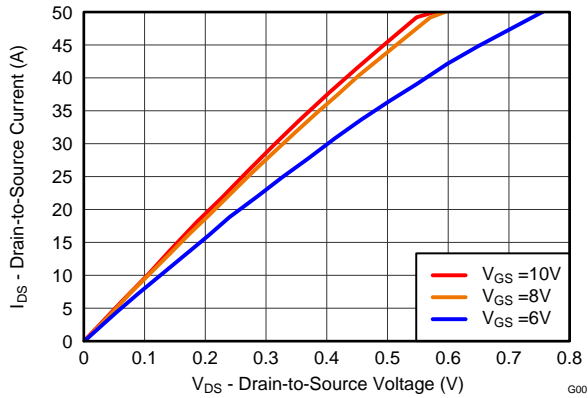


Figure 2. Saturation Characteristics

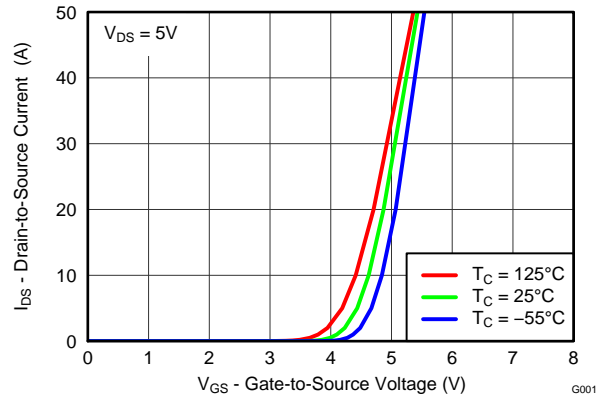


Figure 3. Transfer Characteristics

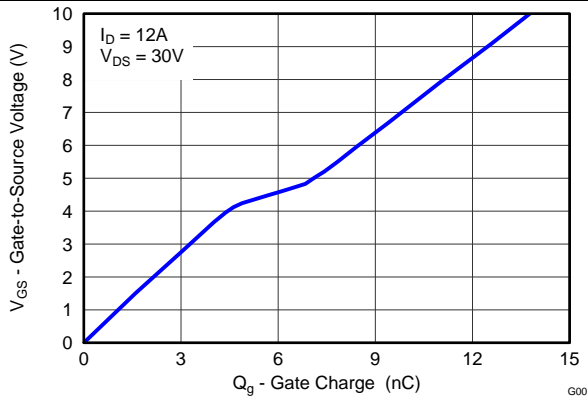


Figure 4. Gate Charge

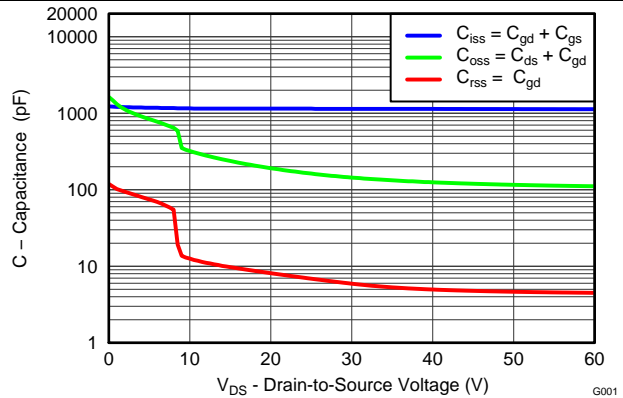


Figure 5. Capacitance

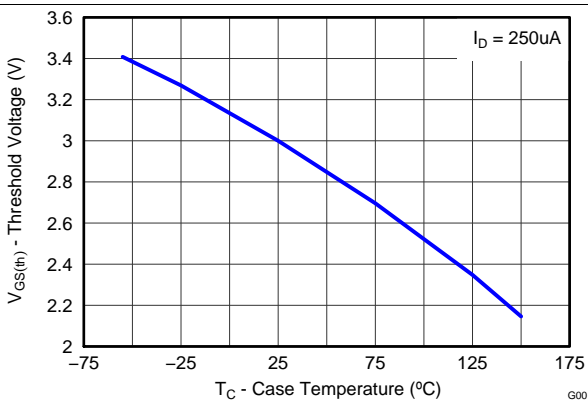


Figure 6. Threshold Voltage vs Temperature

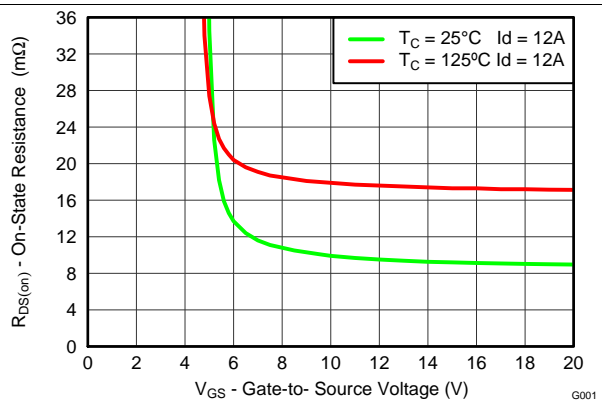


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

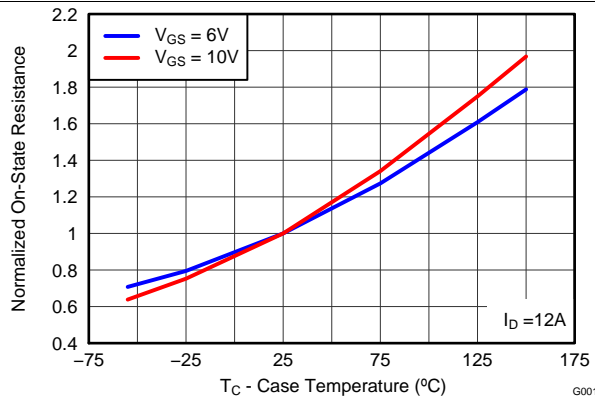


Figure 8. Normalized On-State Resistance vs Temperature

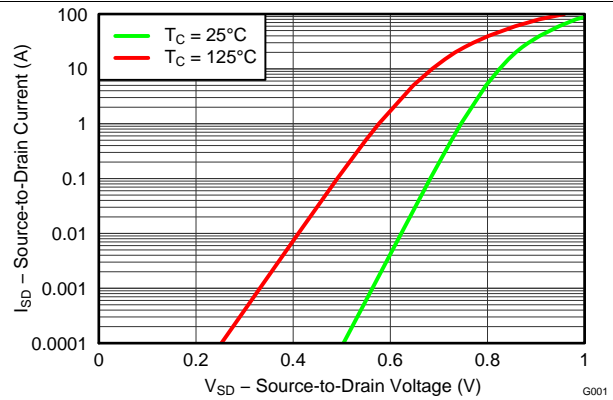


Figure 9. Typical Diode Forward Voltage

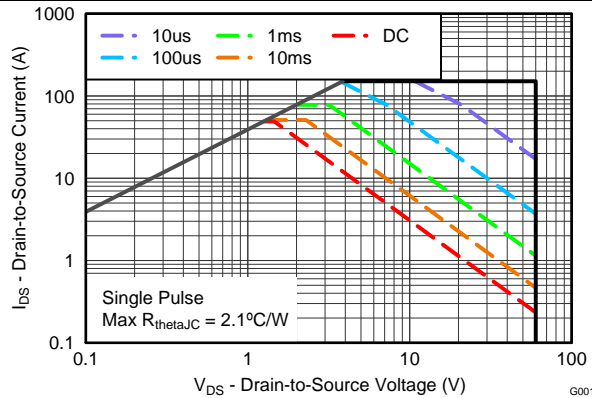


Figure 10. Maximum Safe Operating Area

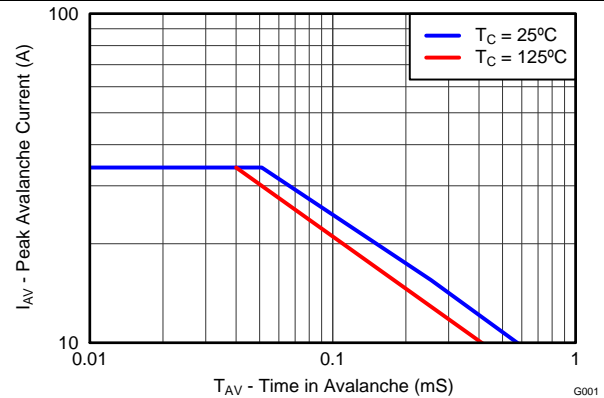


Figure 11. Single Pulse Unclamped Inductive Switching

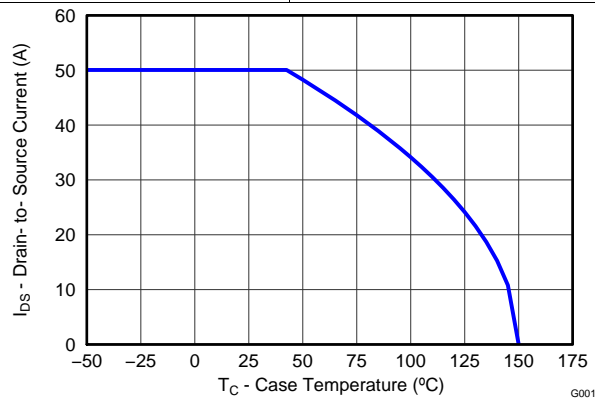


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

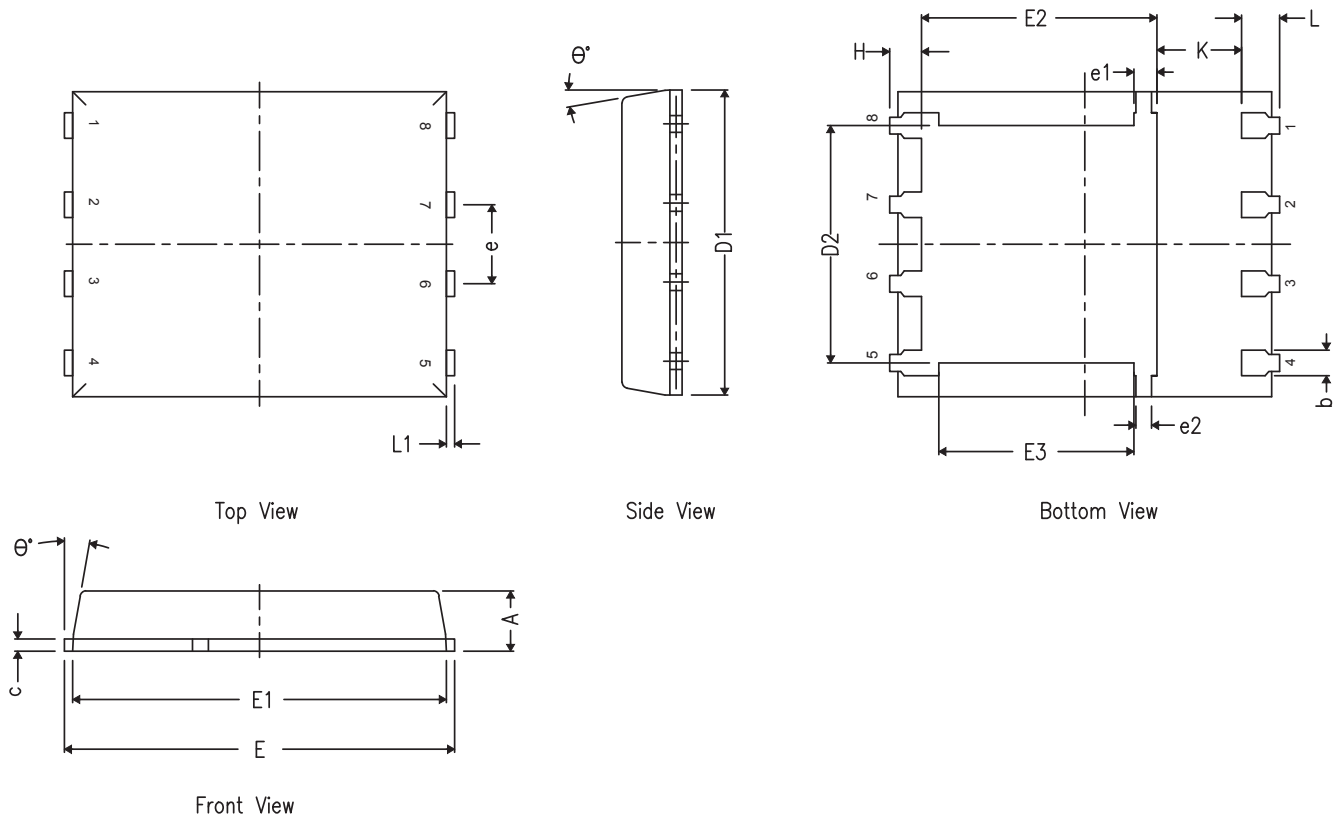
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5A Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	—	—
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°	—	12°

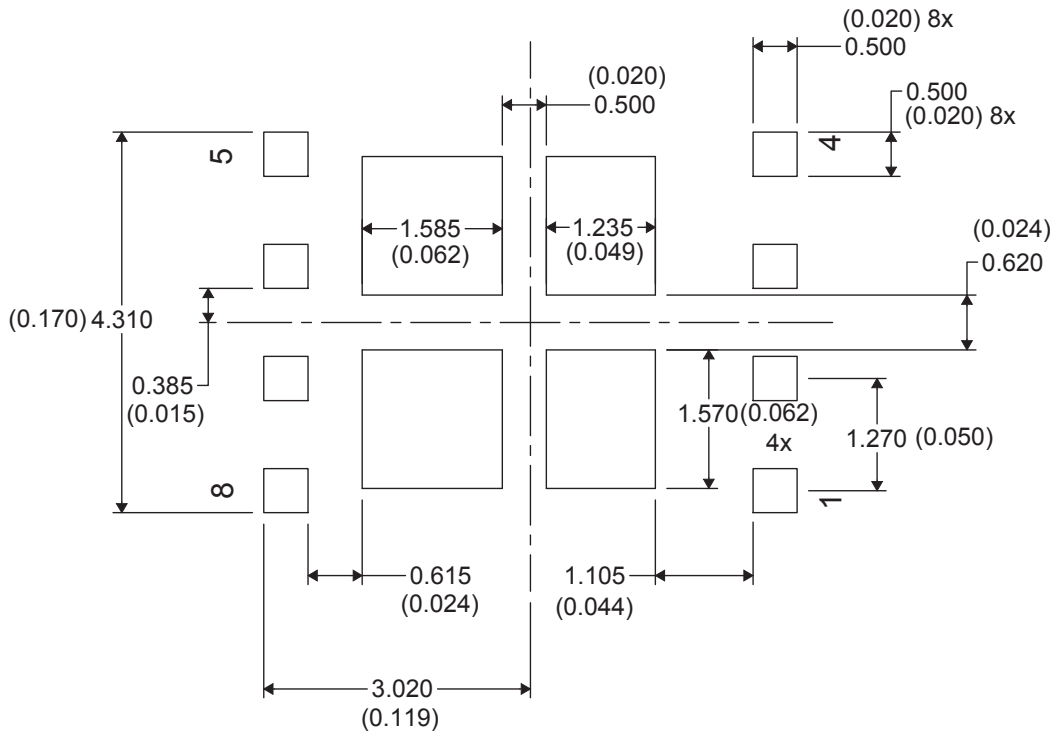
7.2 Recommended PCB Pattern



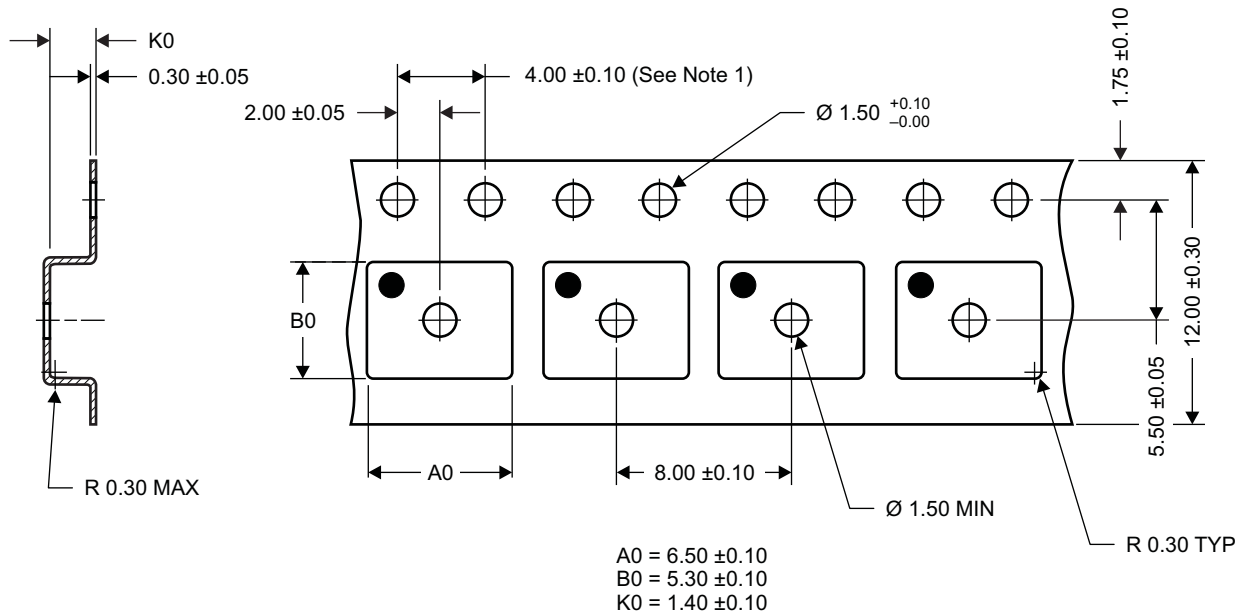
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



7.4 Q5A Tape and Reel Information



M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified).
- A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18537NQ5A	Active	Production	VSONP (DQJ) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18537N
CSD18537NQ5A.B	Active	Production	VSONP (DQJ) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18537N
CSD18537NQ5AT	Active	Production	VSONP (DQJ) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18537N
CSD18537NQ5AT.B	Active	Production	VSONP (DQJ) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18537N

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated