

# CSD17551Q3A 30-V N-Channel NexFET™ Power MOSFETs

## 1 Features

- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

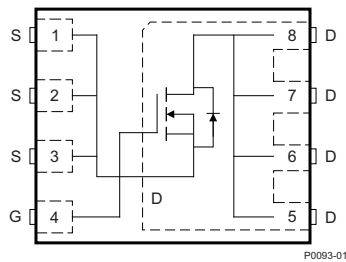
## 2 Applications

- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

## 3 Description

This 30 V, 7.8 mΩ, 3.3 mm × 3.3 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

**Top View**



P0093-01

### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	30		V
$Q_g$	Gate Charge Total (4.5 V)	6.0		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	1.5		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 4.5\text{ V}$	9.6	mΩ
		$V_{GS} = 10\text{ V}$	7.8	mΩ
$V_{GS(th)}$	Threshold Voltage	1.6		V

### Ordering Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17551Q3A	2500	13-Inch Reel	SON 3.3 mm × 3.3 mm Plastic Package	Tape and Reel
CSD17551Q3AT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

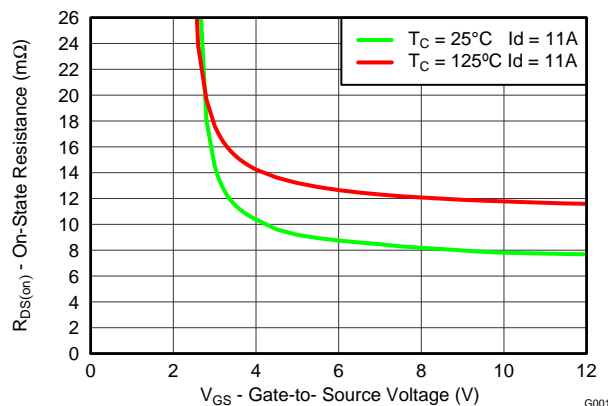
### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	48	A
	Continuous Drain Current, Silicon Limited	48	A
	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	12	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	71	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.6	W
$T_J$ , $T_{stg}$	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
$E_{AS}$	Avalanche Energy, single pulse $I_D = 25\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\text{ }\Omega$	31	mJ

(1) Typical  $R_{\theta JA} = 48^\circ\text{C/W}$  on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.

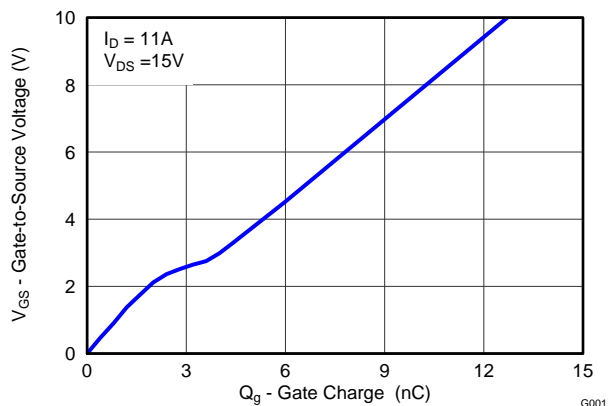
(2) Pulse duration ≤300 μs, duty cycle ≤2%

**$R_{DS(on)}$  vs  $V_{GS}$**



G001

**Gate Charge**



G001



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (June 2014) to Revision B</b>	<b>Page</b>
• Enhanced <a href="#">Description</a> text. ....	<b>1</b>
• Added <a href="#">Community Resources</a> section .....	<b>7</b>
• Updated package drawing. ....	<b>8</b>
• Updated PCB drawing. ....	<b>9</b>
• Updated Stencil Pattern drawing. ....	<b>9</b>

<b>Changes from Original (September 2012) to Revision A</b>	<b>Page</b>
• Changed "Pb-Free terminal plating" feature to state "Pb Free". ....	<b>1</b>
• Updated package dimensions. ....	<b>8</b>

## 5 Specifications

### 5.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V			1	μA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 20 V			100	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.1	1.6	2.1	V
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 11 A	9.6		11.8	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11 A	7.8		9	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 11 A	101			S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 15 V, f = 1 MHz	1050		1370	pF
C <sub>oss</sub>	Output capacitance		244		317	pF
C <sub>rss</sub>	Reverse transfer capacitance		24		31	pF
R <sub>G</sub>	Series gate resistance		1.5		3	Ω
Q <sub>g</sub>	Gate charge total (4.5 V)	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 11 A	6		7.8	nC
Q <sub>gd</sub>	Gate charge gate to drain		1.5			nC
Q <sub>gs</sub>	Gate charge gate to source		2.3			nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>		1.4			nC
Q <sub>oss</sub>	Output charge	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V	7.4			nC
t <sub>d(on)</sub>	Turn on delay time	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>DS</sub> = 11 A, R <sub>G</sub> = 2 Ω	8			ns
t <sub>r</sub>	Rise time		24			ns
t <sub>d(off)</sub>	Turn off delay time		12			ns
t <sub>f</sub>	Fall time		3.4			ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = 11 A, V <sub>GS</sub> = 0 V	0.8		1	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = 13.5 V, I <sub>F</sub> = 11 A, di/dt = 300 A/μs	13			nC
t <sub>rr</sub>	Reverse recovery time		14			ns

### 5.2 Thermal Information

(T<sub>A</sub> = 25°C unless otherwise stated)

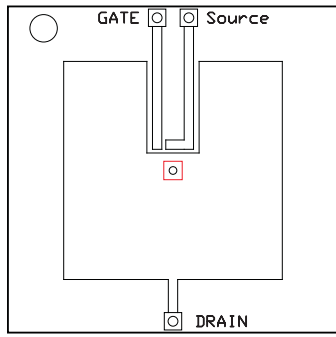
THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-case thermal resistance <sup>(1)</sup>			3.9	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			60	°C/W

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.

# CSD17551Q3A

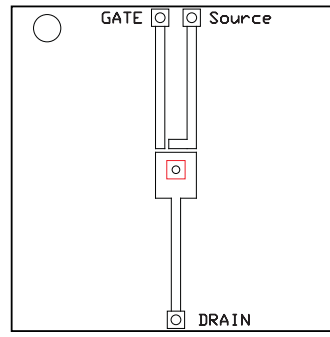
SLPS386B – SEPTEMBER 2012 – REVISED JANUARY 2016

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M0161-01

Max  $R_{\theta JA} = 60^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2 oz. (0.071 mm thick)  
Cu.

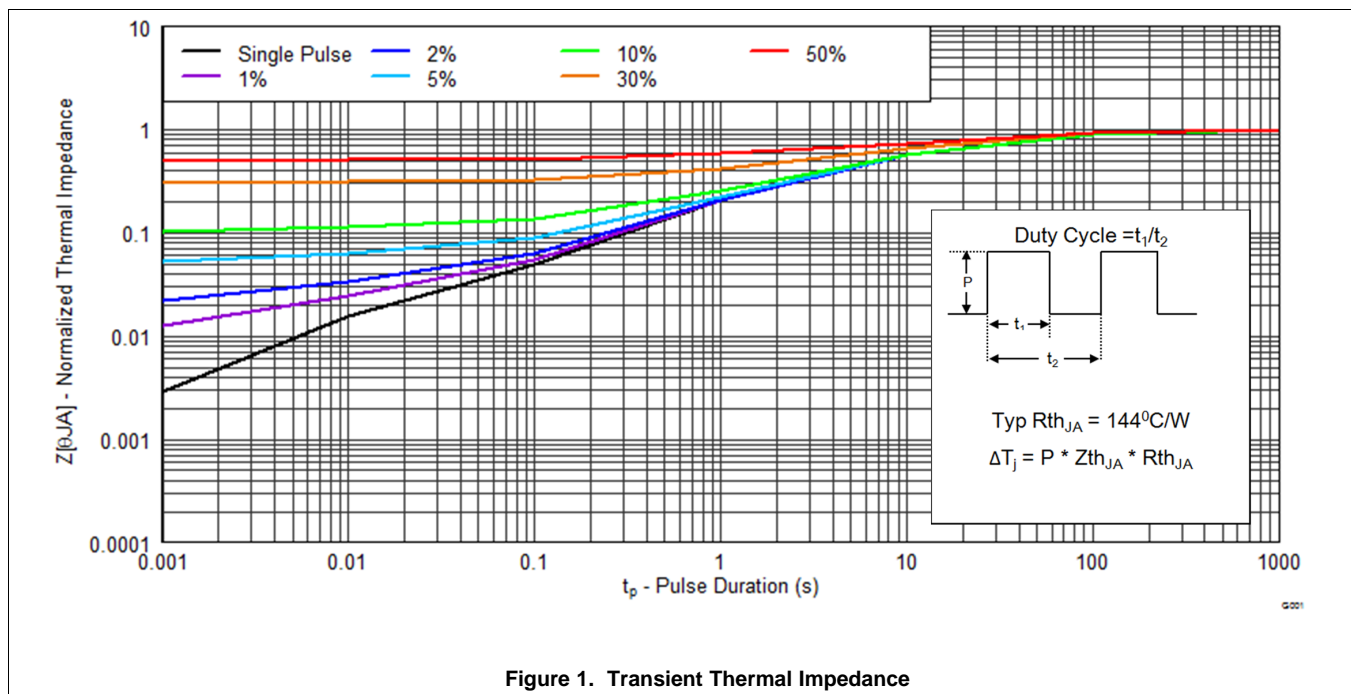


M0161-02

Max  $R_{\theta JA} = 144^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of 2  
oz. (0.071 mm thick)  
Cu.

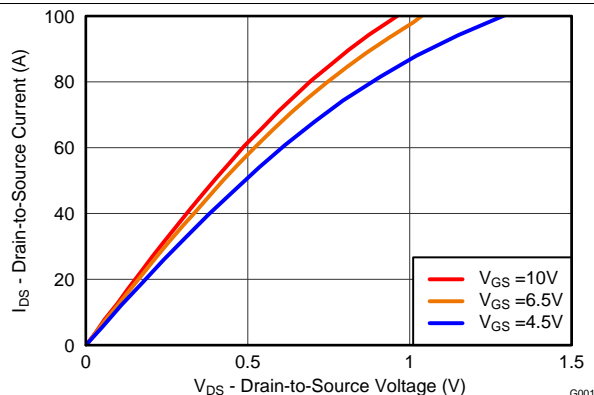
## 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

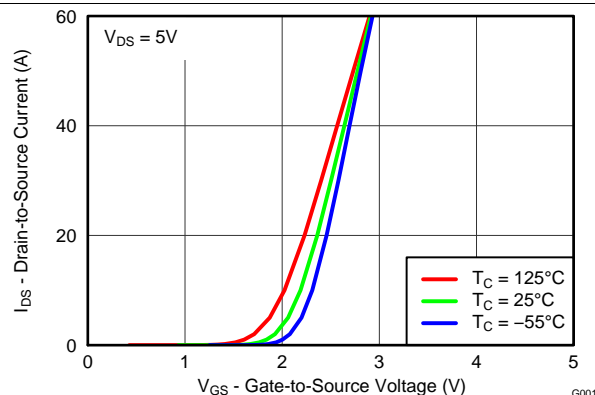


## Typical MOSFET Characteristics (continued)

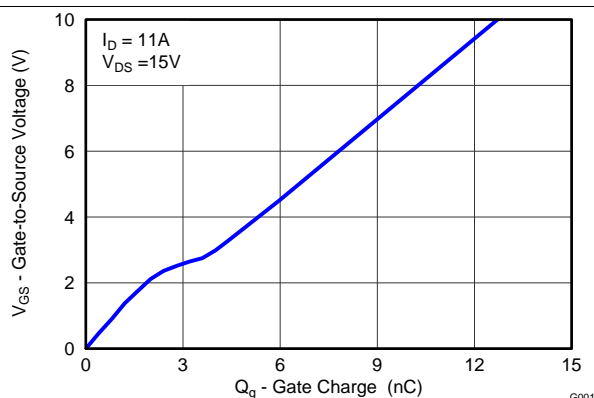
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



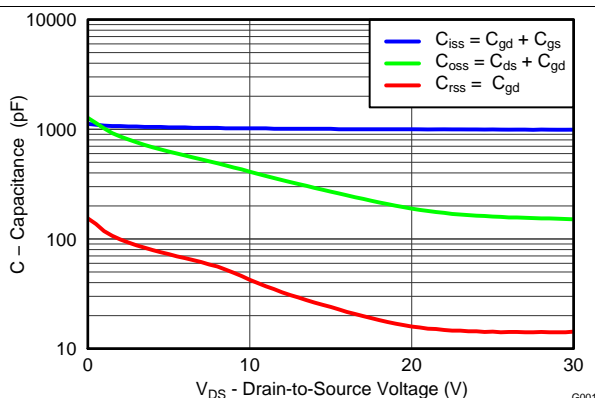
**Figure 2. Saturation Characteristics**



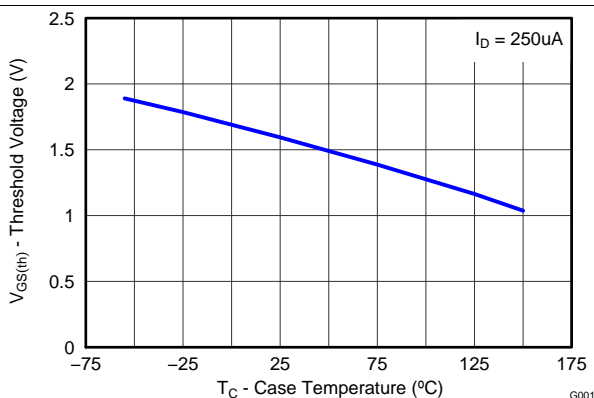
**Figure 3. Transfer Characteristics**



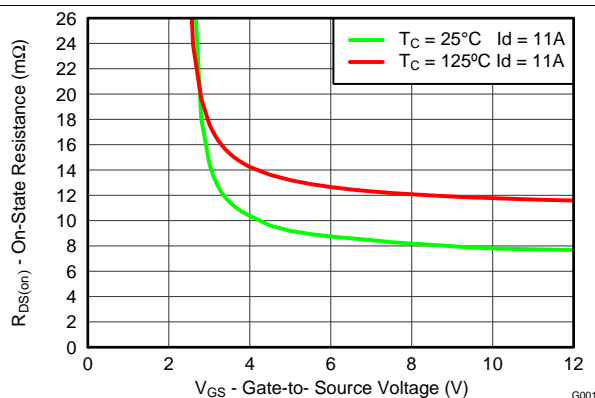
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs Temperature**



**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

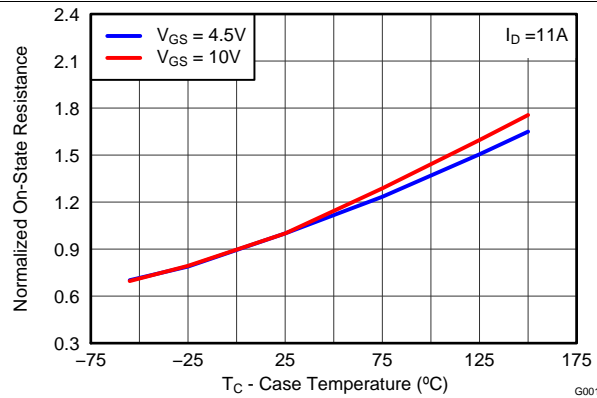


Figure 8. Normalized On-State Resistance vs Temperature

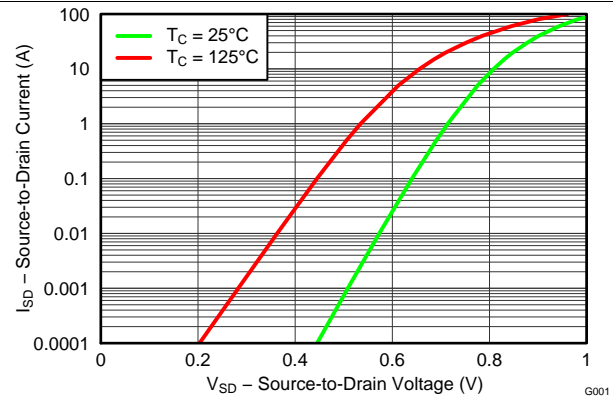


Figure 9. Typical Diode Forward Voltage

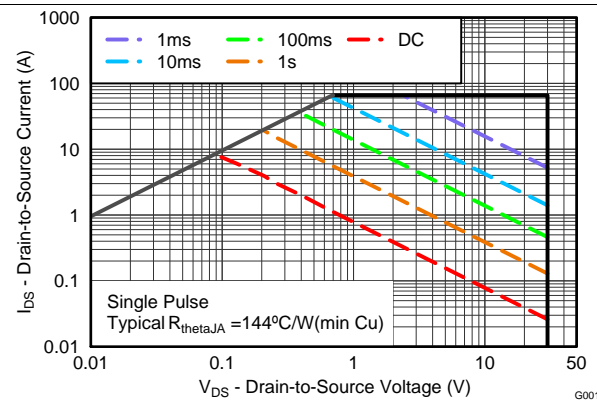


Figure 10. Maximum Safe Operating Area

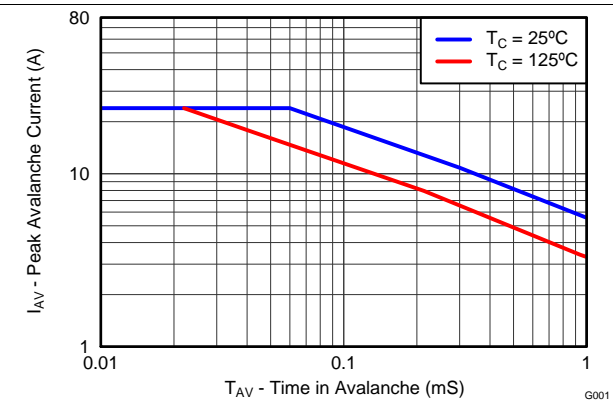


Figure 11. Single Pulse Unclamped Inductive Switching

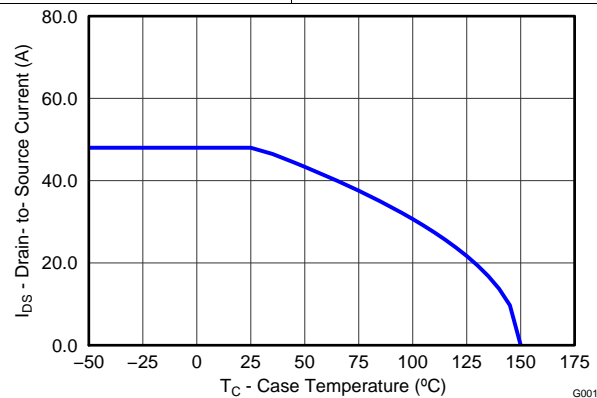


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.4 Glossary

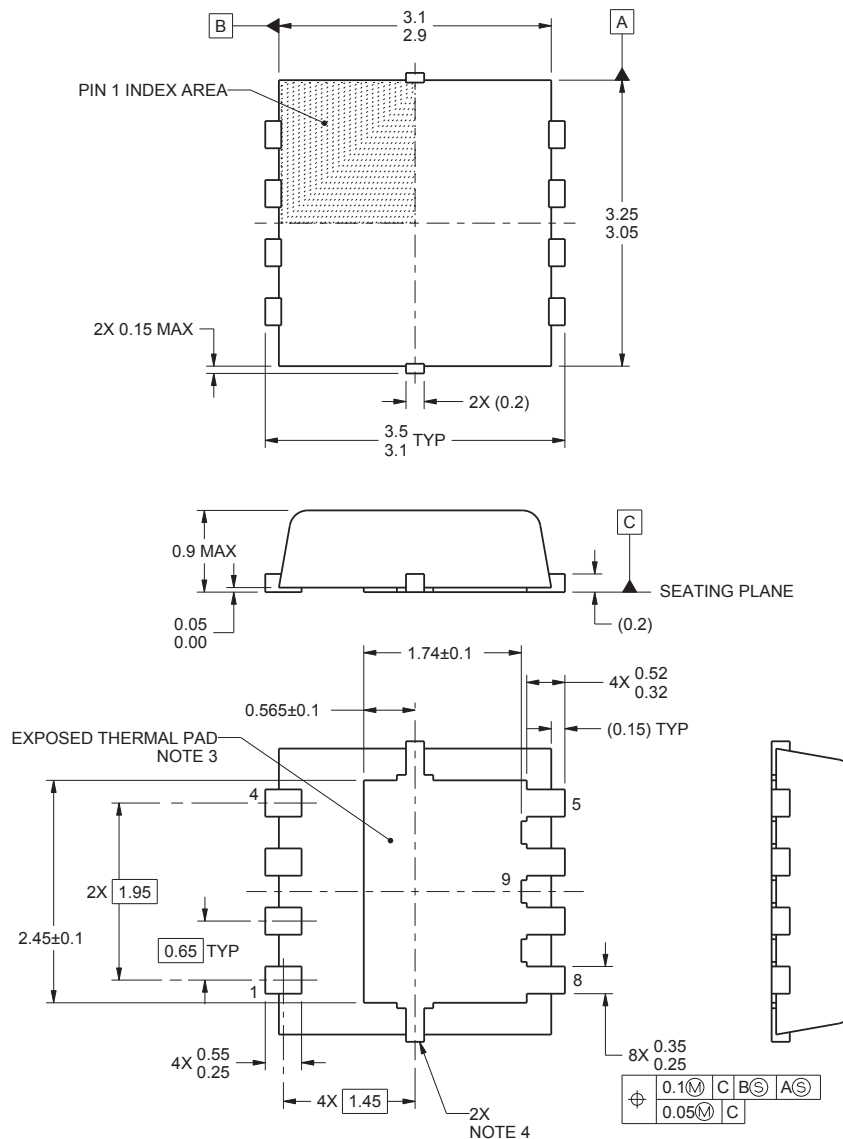
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

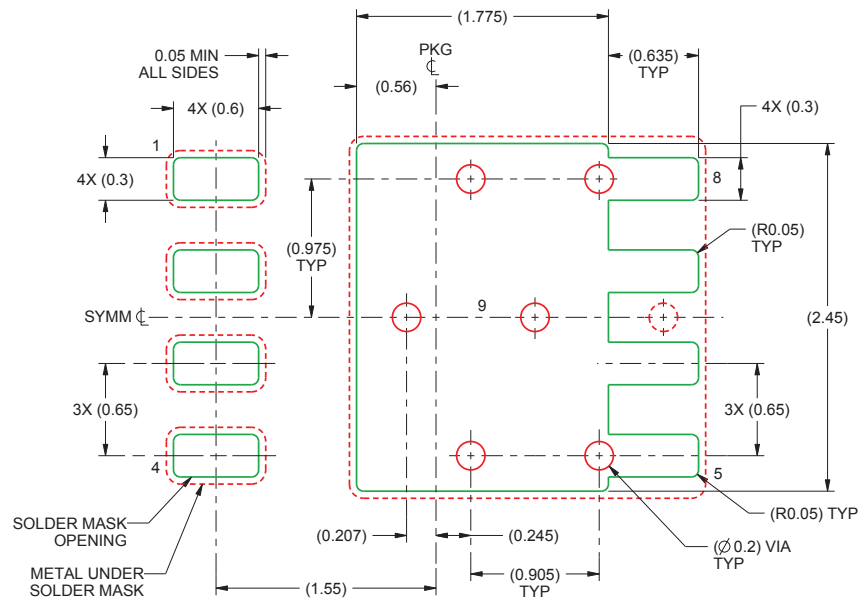
### 7.1 Q3A Package Dimensions



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.



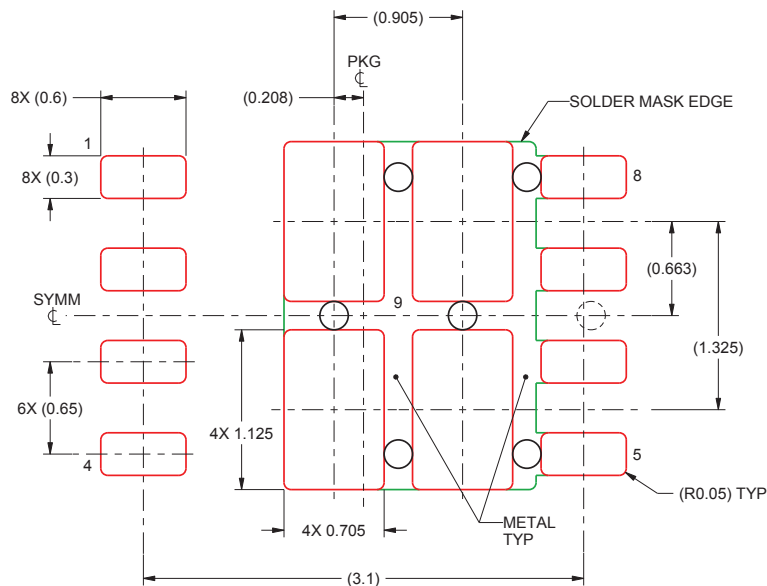
## 7.2 Q3A Recommended PCB Pattern



1. This package is designed to be soldered to a thermal pad on the board. For more information, see the *QFN/SON PCB Attachment* application report, [SLUA271](#).
2. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

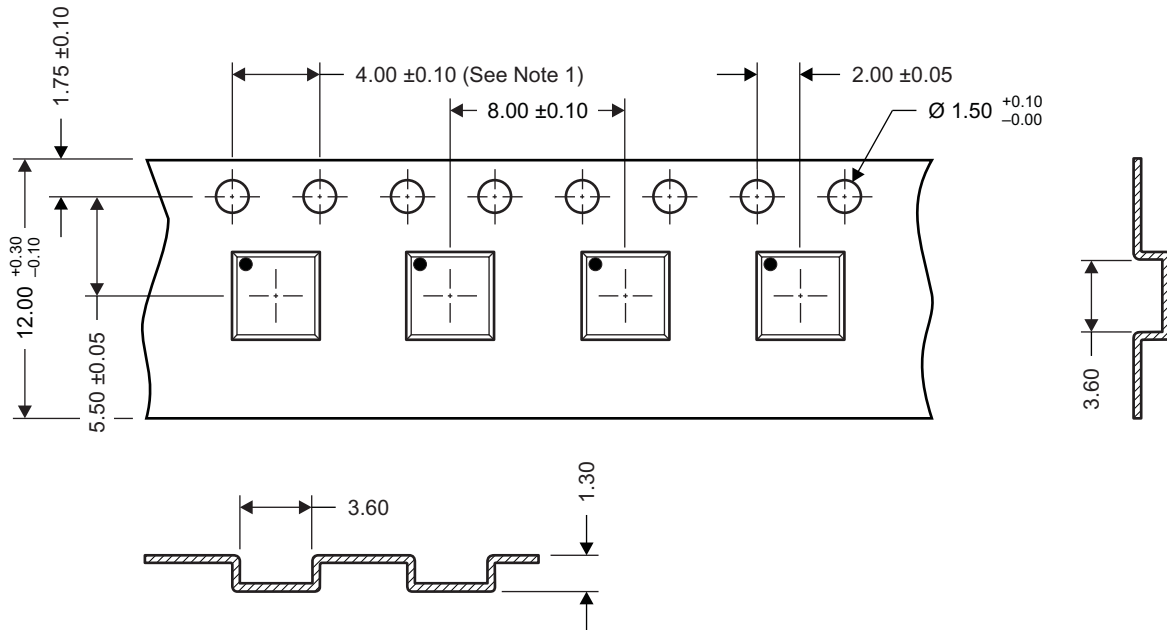
For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### 7.3 Q3A Recommended Stencil Pattern



1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 7.4 Q3A Tape and Reel Information



M0144-01

- Notes:
1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
  2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
  3. Material: black static-dissipative polystyrene
  4. All dimensions are in mm, unless otherwise specified.
  5. Thickness:  $0.30 \pm 0.05$  mm
  6. MSL1 260°C (IR and convection) PbF-reflow compatible

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD17551Q3A</a>	Active	Production	VSONP (DNH)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17551
CSD17551Q3A.B	Active	Production	VSONP (DNH)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17551

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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