



CSD17309Q3 30-V N-Channel NexFET™ Power MOSFET

1 Features

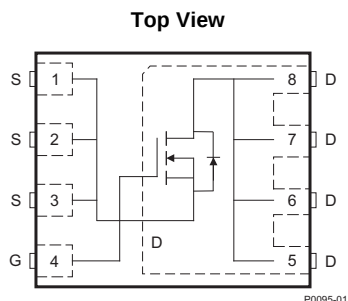
- Optimized for 5 V Gate Drive
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

2 Applications

- Notebook Point of Load
- Point of Load Synchronous Buck in Networking, Telecom, and Computing Systems

3 Description

This 30 V, 4.2 mΩ NexFET™ power MOSFET is designed to minimize losses in power conversion applications and optimized for 5 V gate drive applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	7.5		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.7		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 3\text{ V}$	6.3	mΩ
		$V_{GS} = 4.5\text{ V}$	4.9	
		$V_{GS} = 8\text{ V}$	4.2	
$V_{GS(th)}$	Threshold Voltage	1.2		V

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD17309Q3	13-Inch Reel	2500	SON 3.3 × 3.3 mm Plastic Package	Tape and Reel
CSD17309Q3T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current ⁽¹⁾	20	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	112	A
P_D	Power Dissipation ⁽¹⁾	2.8	W
T_J , T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse $I_D = 57\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	162	mJ

(1) Typical $R_{\theta JA} = 45^\circ\text{C/W}$ when mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

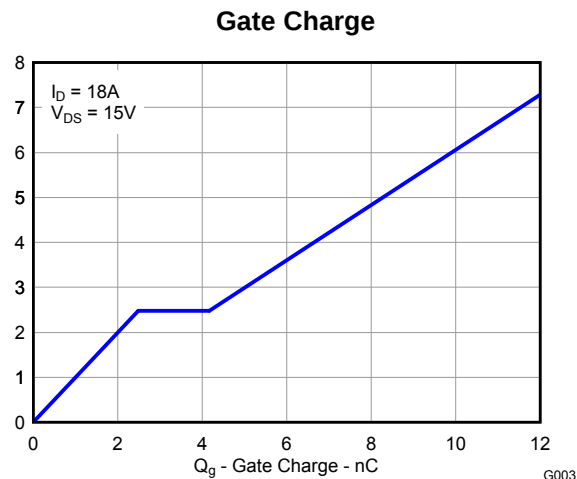
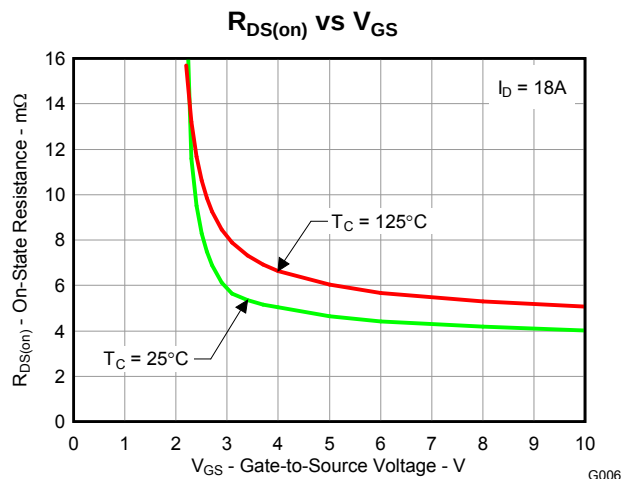


Table of Contents

1 Features	1	6.1 Trademarks	8
2 Applications	1	6.2 Electrostatic Discharge Caution	8
3 Description	1	6.3 Glossary	8
4 Revision History	2	7 Mechanical, Packaging, and Orderable Information	9
5 Specifications	3	7.1 Q3 Package Dimensions	9
5.1 Electrical Characteristics	3	7.2 Recommended PCB Pattern	10
5.2 Thermal Information	3	7.3 Recommended Stencil Opening	10
5.3 Typical MOSFET Characteristics	4	7.4 Q3 Tape and Reel Information	11
6 Device and Documentation Support	8		

4 Revision History

Changes from Revision A (October 2010) to Revision B Page

•	1
• Added 7" reel to Ordering Information	1
• Updated mechanical information	9

Changes from Original (March 2010) to Revision A Page

• Deleted the Package Marking Information section	11
---	-----------

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 24 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = +10 / –8 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.9	1.2	1.7	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 3 V, I _D = 18 A		6.3	8.5	mΩ
		V _{GS} = 4.5 V, I _D = 18 A		4.9	6.3	mΩ
		V _{GS} = 8 V, I _D = 18 A		4.2	5.4	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _D = 18 A		67		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		1150	1440	pF
C _{OSS}	Output Capacitance			580	750	pF
C _{RSS}	Reverse Transfer Capacitance			43	56	pF
R _g	Series Gate Resistance	V _{DS} = 15 V, I _D = 18 A		1.2	2.4	Ω
Q _g	Gate Charge Total (4.5 V)			7.5	10	nC
Q _{gd}	Gate Charge Gate-to-Drain			1.7		nC
Q _{gs}	Gate Charge Gate-to-Source			2.5		nC
Q _{g(th)}	Gate Charge at V _{th}			1.3		nC
Q _{OSS}	Output Charge	V _{DS} = 13 V, V _{GS} = 0 V		15		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 18 A , R _G = 2 Ω		6.1		ns
t _r	Rise Time			9.9		ns
t _{d(off)}	Turn Off Delay Time			13.2		ns
t _f	Fall Time			3.6		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{DS} = 18 A, V _{GS} = 0 V		0.85	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13 V, I _F = 18 A, di/dt = 300 A/μs		30		nC
t _{rr}	Reverse Recovery Time			23		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-Case Thermal Resistance ⁽¹⁾			2.0	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			57	

- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), Cu pad on a 1.5 inches × 1.5 inches thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² 2-oz.Cu.

CSD17309Q3

SLPS261B – MARCH 2010 – REVISED SEPTEMBER 2014

www.ti.com



M0161-01

Max $R_{\theta JA} = 57^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2 oz. (0.071 mm thick)
Cu.

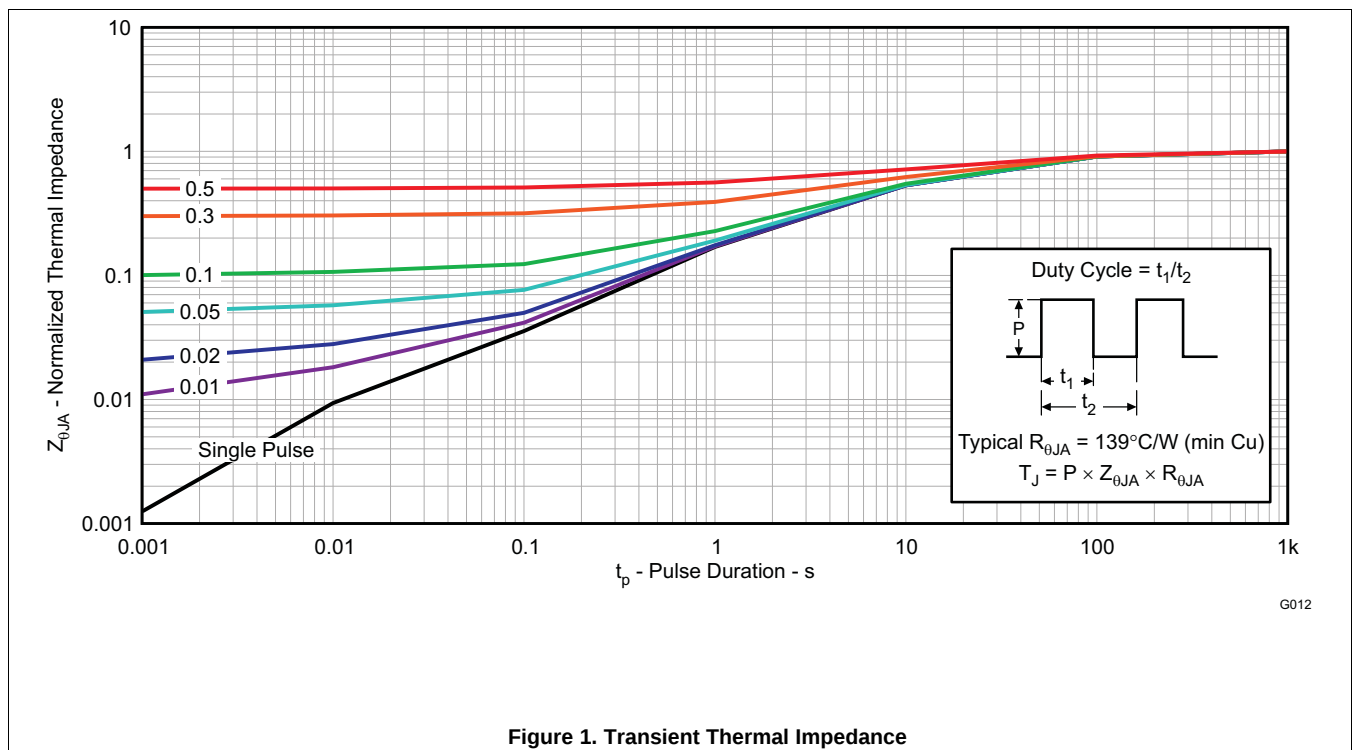


M0161-02

Max $R_{\theta JA} = 174^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2 oz. (0.071 mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

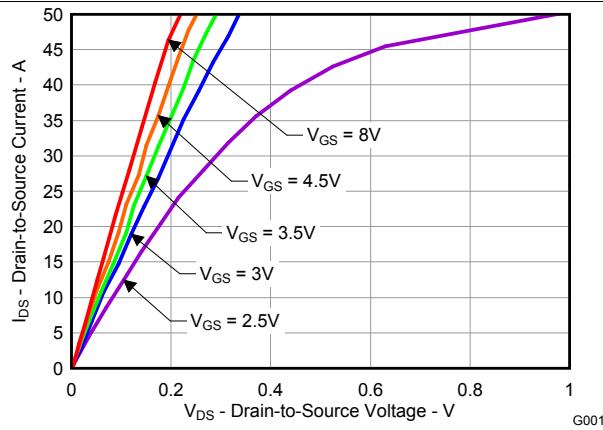


Figure 2. Saturation Characteristics

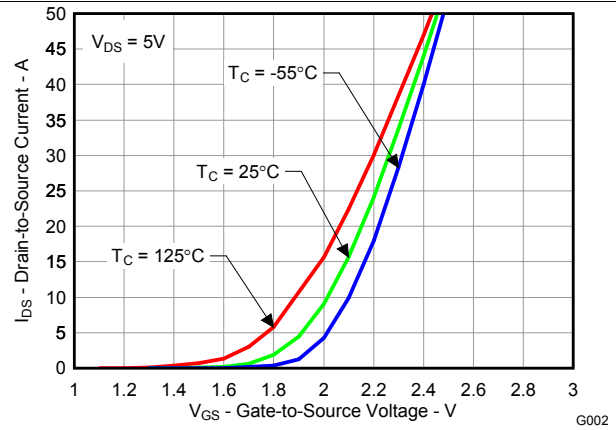


Figure 3. Transfer Characteristics

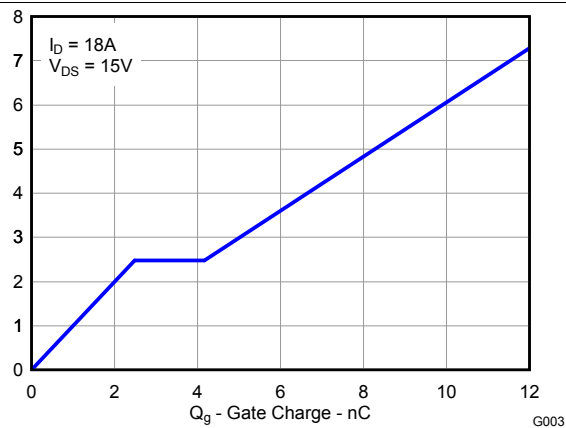


Figure 4. Gate Charge

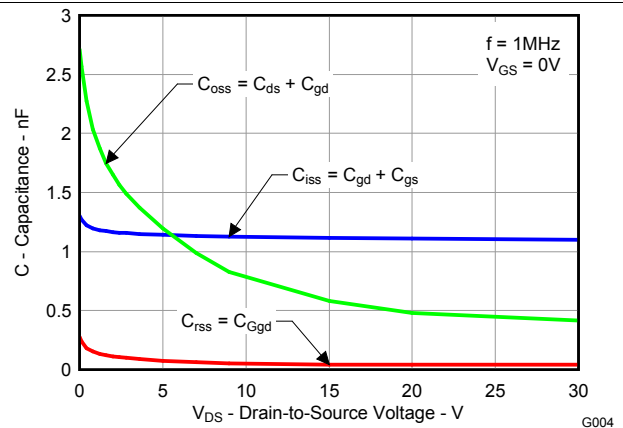


Figure 5. Capacitance

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

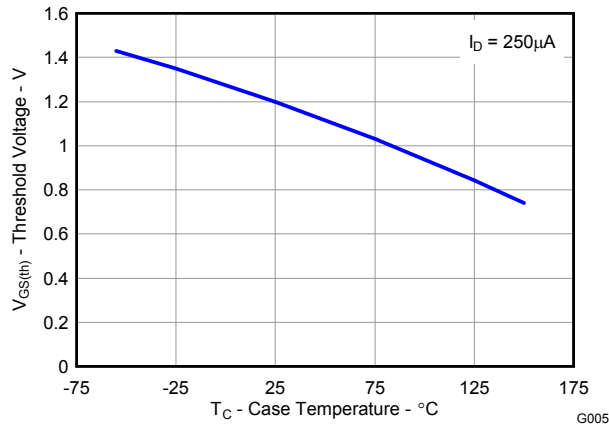


Figure 6. Threshold Voltage vs Temperature

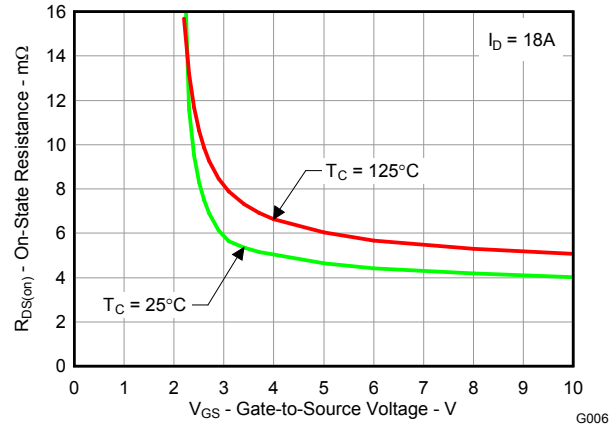


Figure 7. On-State Resistance vs Gate-to-Source Voltage

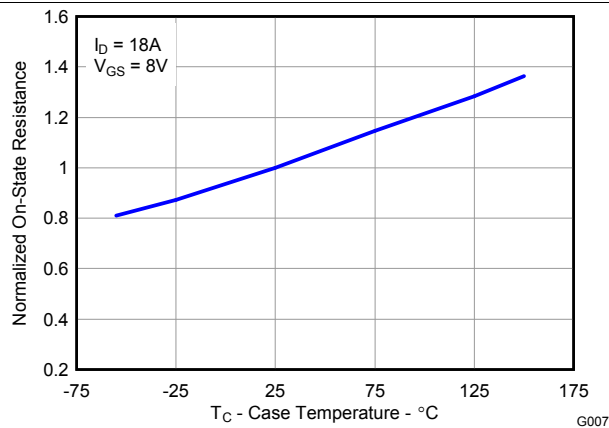


Figure 8. Normalized On-State Resistance vs Temperature

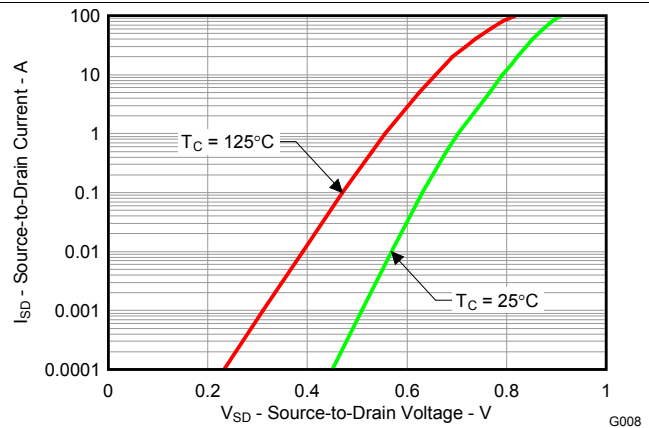
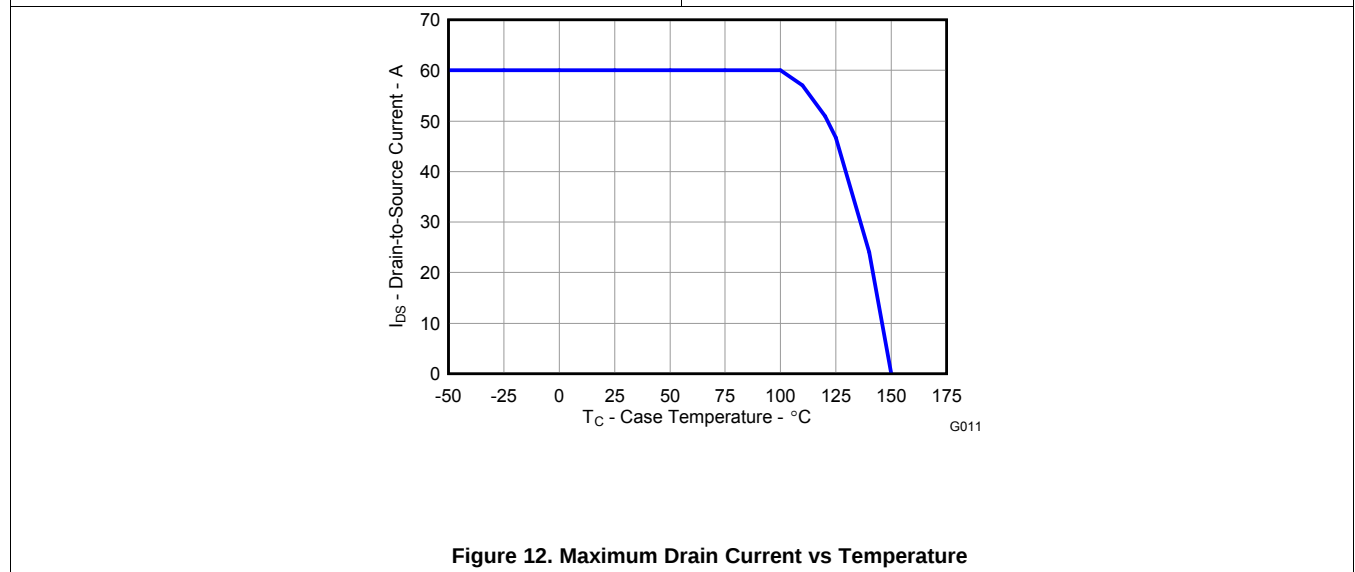
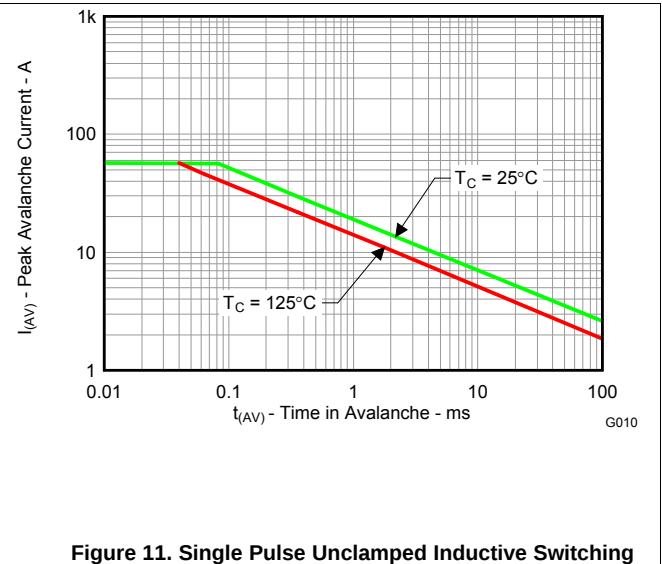
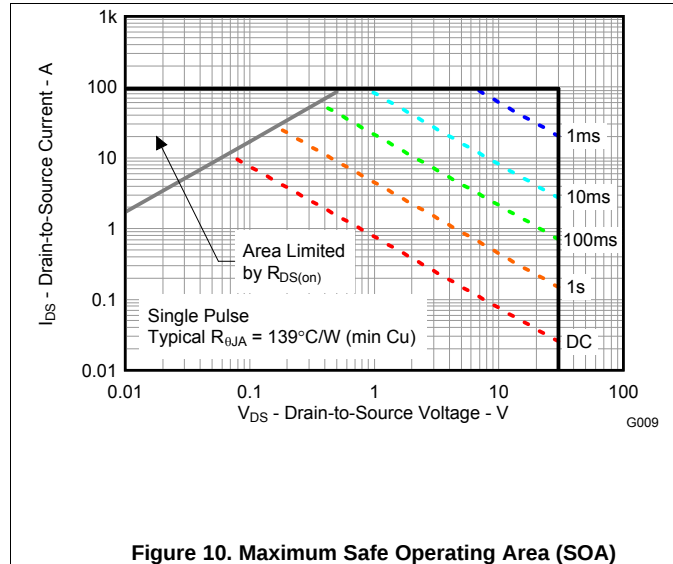


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

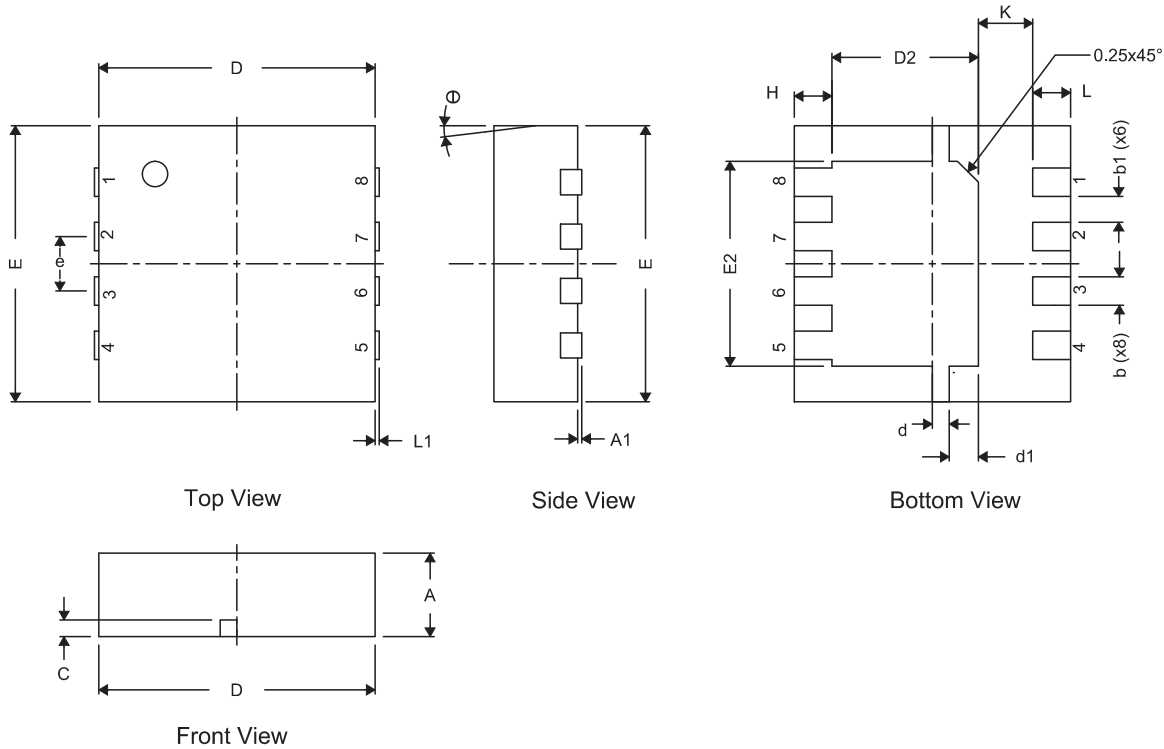
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

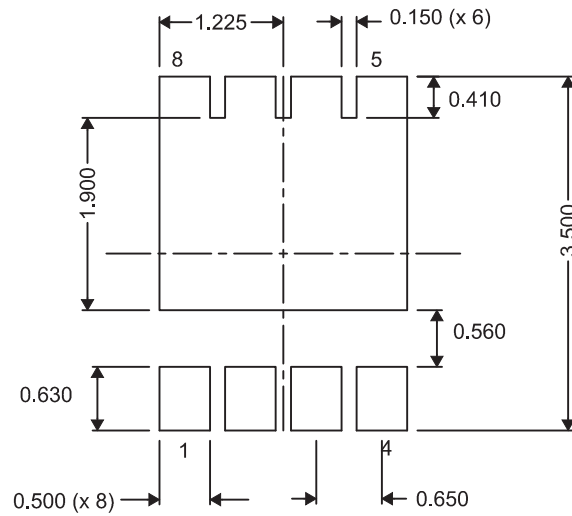
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



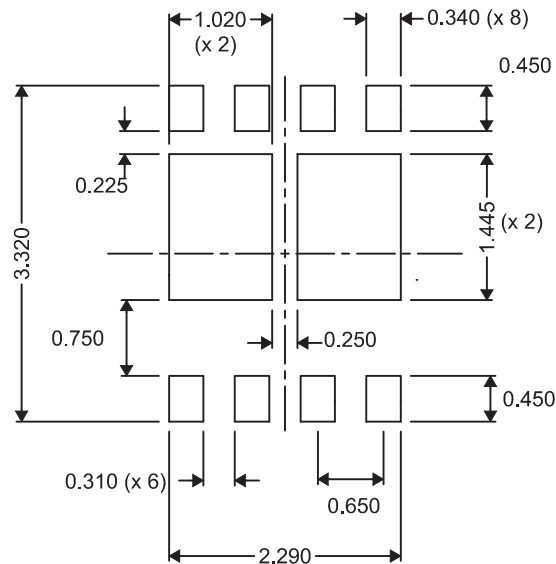
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



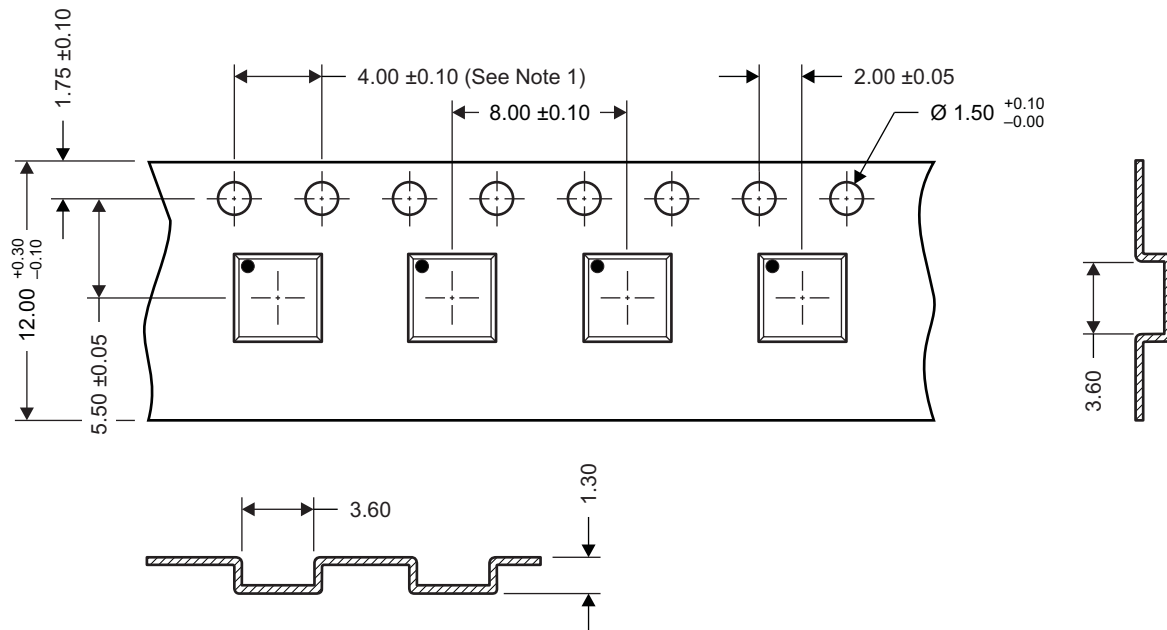
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17309Q3	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17309
CSD17309Q3.B	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17309

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated