30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD17302Q5A

FEATURES

- **Optimized for 5V Gate Drive**
- **Ultralow Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

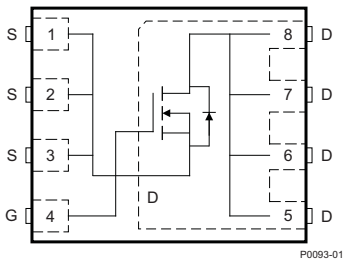
APPLICATIONS

- **Notebook Point of Load**
- **Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.

Top View



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	5.4		nC
Q_{gd}	Gate Charge Gate to Drain	1.2		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V	9.5	mΩ
		V_{GS} = 4.5V	7.3	mΩ
		V_{GS} = 8V	6.4	mΩ
$V_{GS(th)}$	Threshold Voltage	1.2		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17302Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

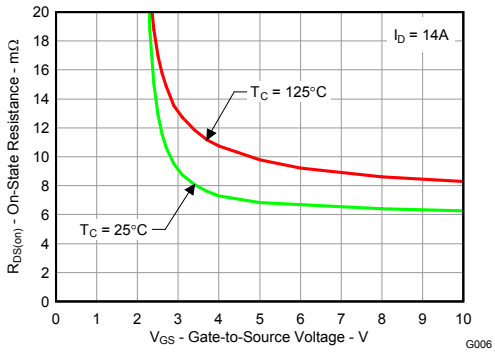
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	87	A
	Continuous Drain Current(1)	16	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	104	A
P_D	Power Dissipation(1)	3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 35A, L = 0.1mH, R_G = 25Ω	61	mJ

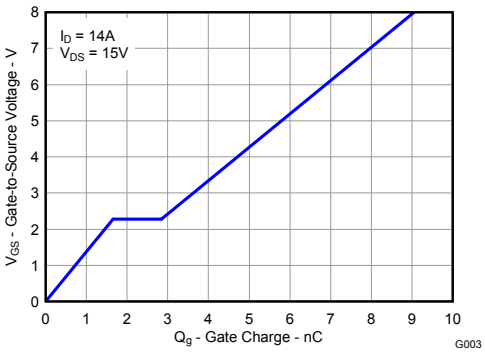
(1) Typical $R_{\theta JA}$ = 41°C/W on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

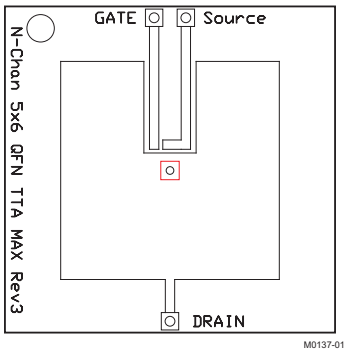
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250μA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10 / –8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	0.9	1.2	1.7	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V, I_D = 14A		9.5	12..8	mΩ
		V_{GS} = 4.5V, I_D = 14A		7.3	9	mΩ
		V_{GS} = 8V, I_D = 14A		6.4	7.9	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 14A		68		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		730	950	pF
C_{oss}	Output Capacitance			390	510	pF
C_{rss}	Reverse Transfer Capacitance			35	45	pF
R_G	Series Gate Resistance			0.8	1.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_D = 14A		5.4	7	nC
Q_{gd}	Gate Charge Gate to Drain			1.2		nC
Q_{gs}	Gate Charge Gate to Source			1.7		nC
$Q_{g(th)}$	Gate Charge at Vth			0.9		nC
Q_{oss}	Output Charge	V_{DS} = 13V, V_{GS} = 0V		9.5		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 14A, R_G = 2Ω		5.2		ns
t_r	Rise Time			8.4		ns
$t_{d(off)}$	Turn Off Delay Time			10.6		ns
t_f	Fall Time			3.1		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 14A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 13V, I_F = 14A, di/dt = 300A/μs		15.4		nC
t_{rr}	Reverse Recovery Time			17.5		ns

THERMAL CHARACTERISTICS

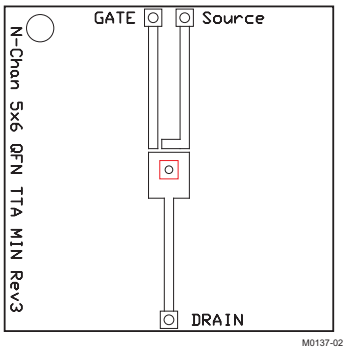
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1.8	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

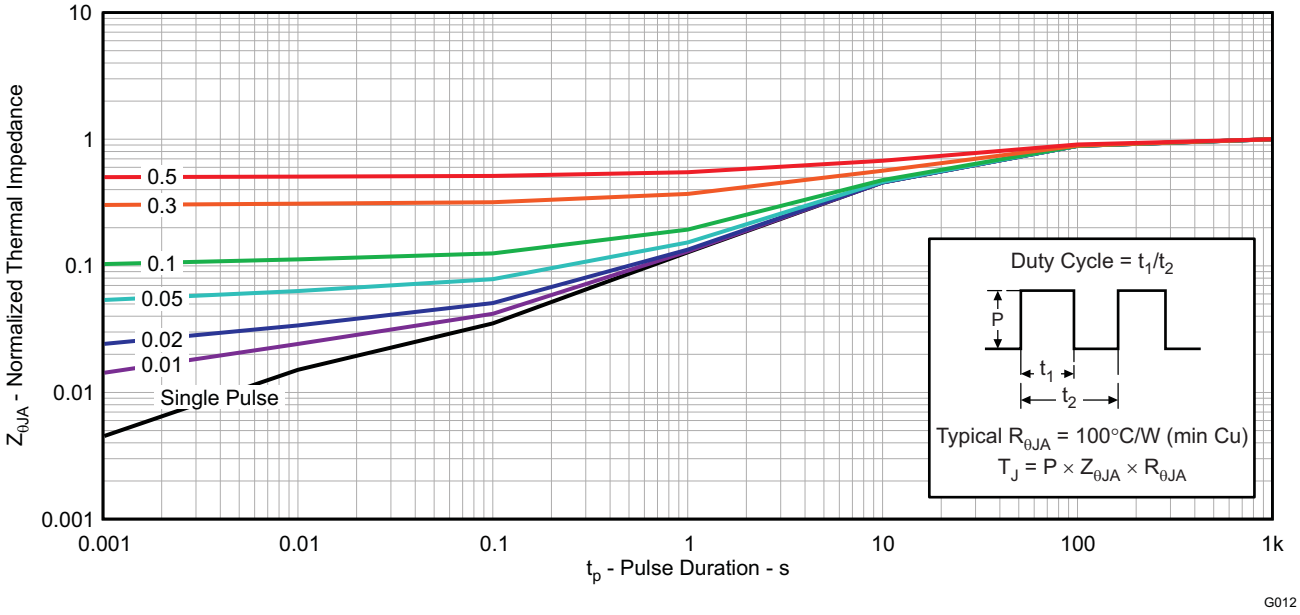


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

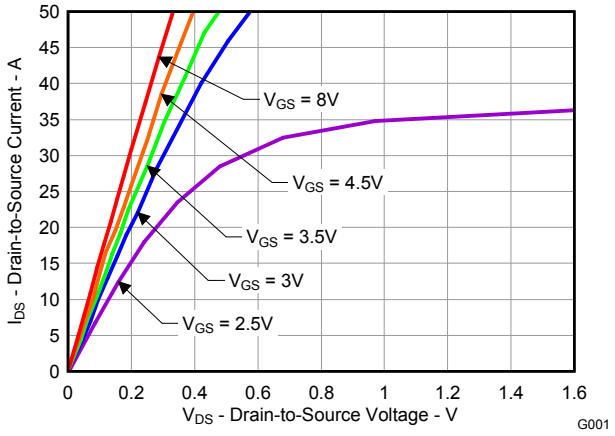


Figure 2. Saturation Characteristics

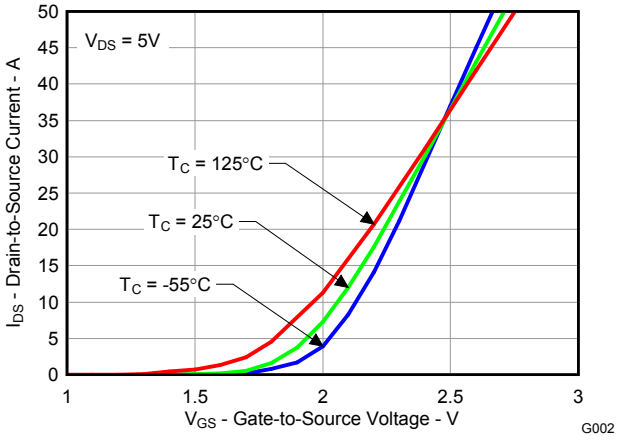


Figure 3. Transfer Characteristics

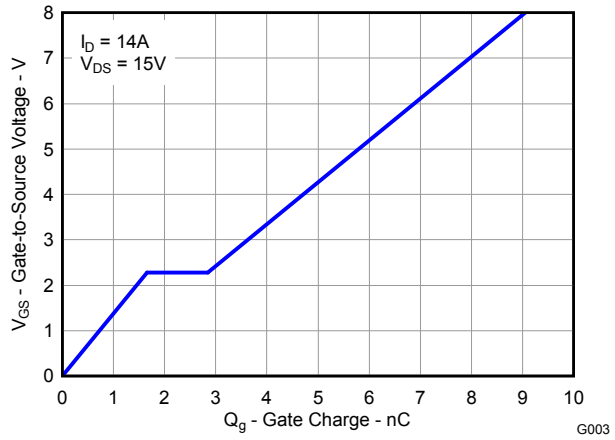


Figure 4. Gate Charge

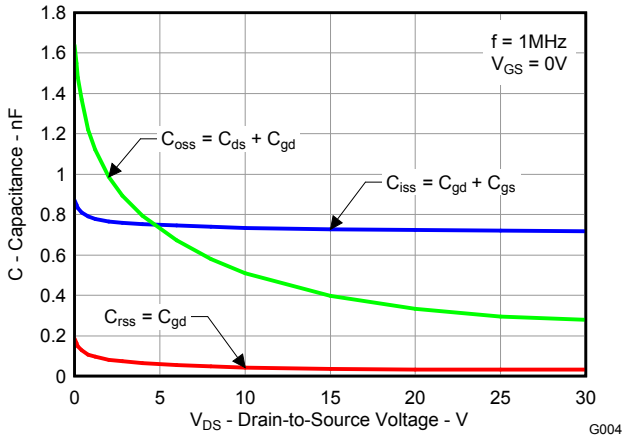


Figure 5. Capacitance

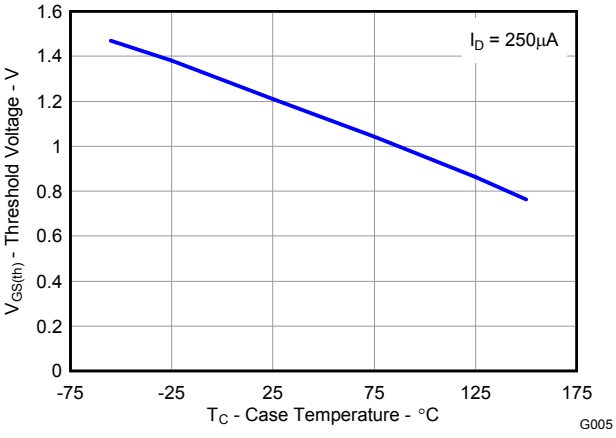


Figure 6. Threshold Voltage vs. Temperature

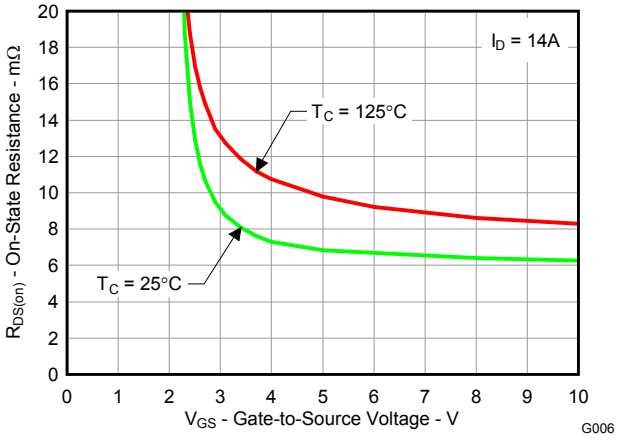


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

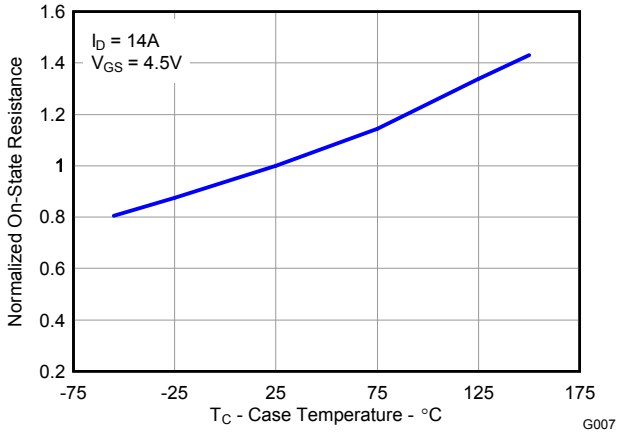


Figure 8. Normalized On-State Resistance vs. Temperature

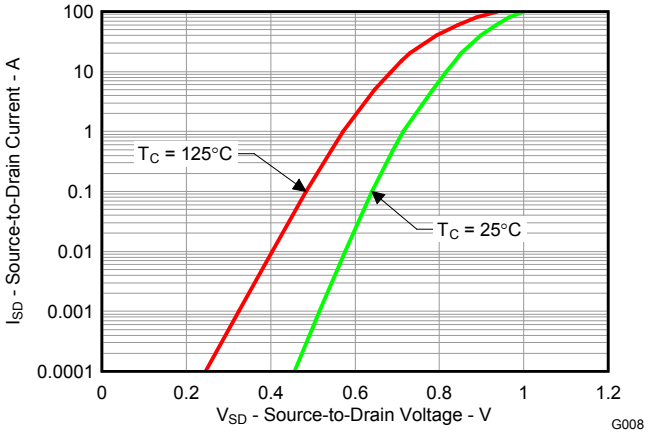


Figure 9. Typical Diode Forward Voltage

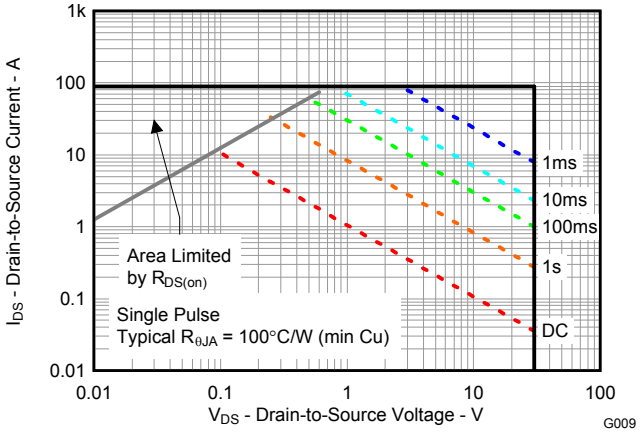


Figure 10. Maximum Safe Operating Area

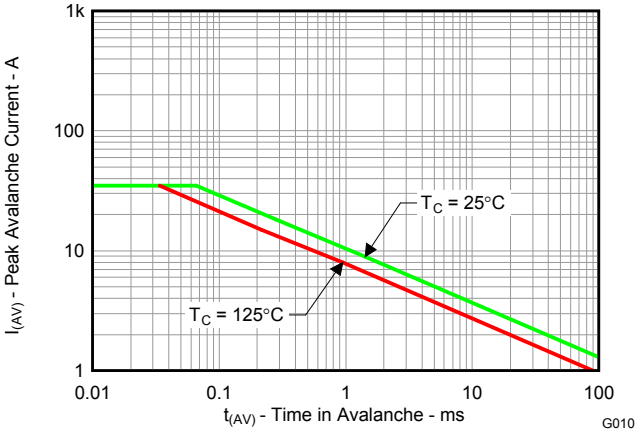


Figure 11. Single Pulse Unclamped Inductive Switching

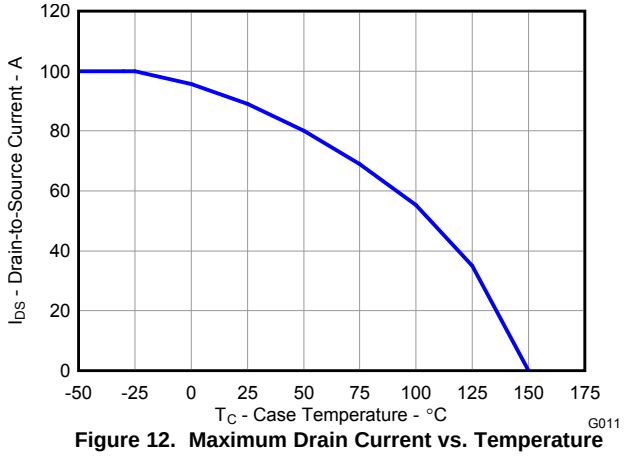
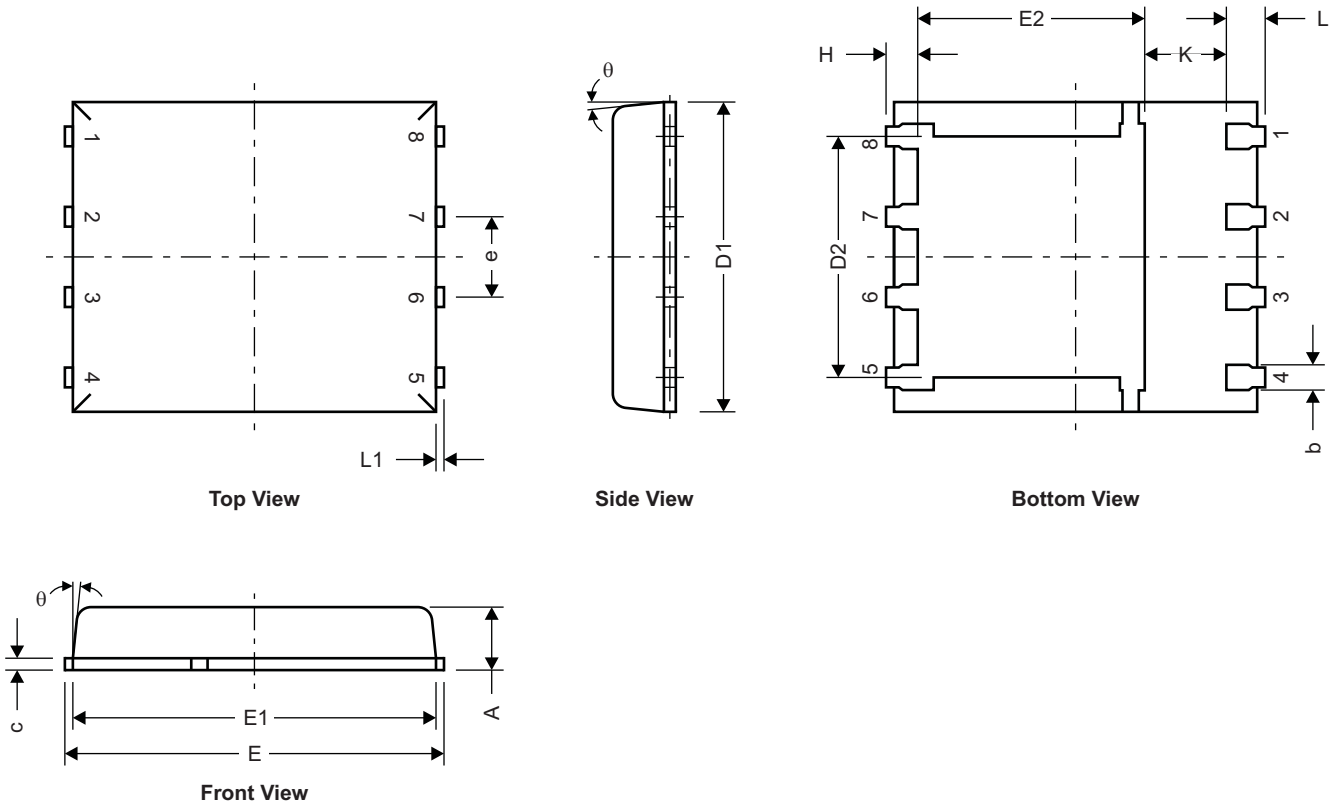


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

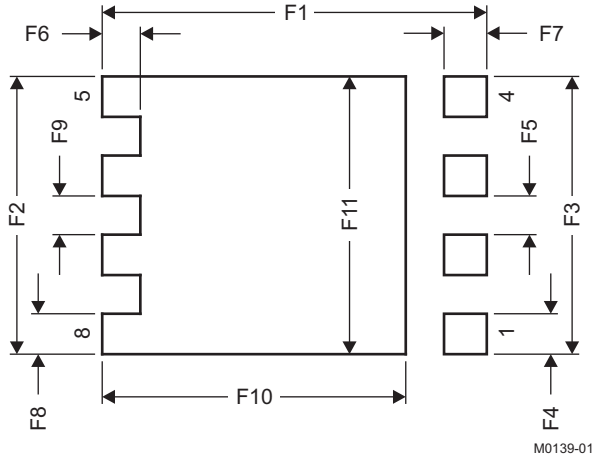
Q5A Package Dimensions



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

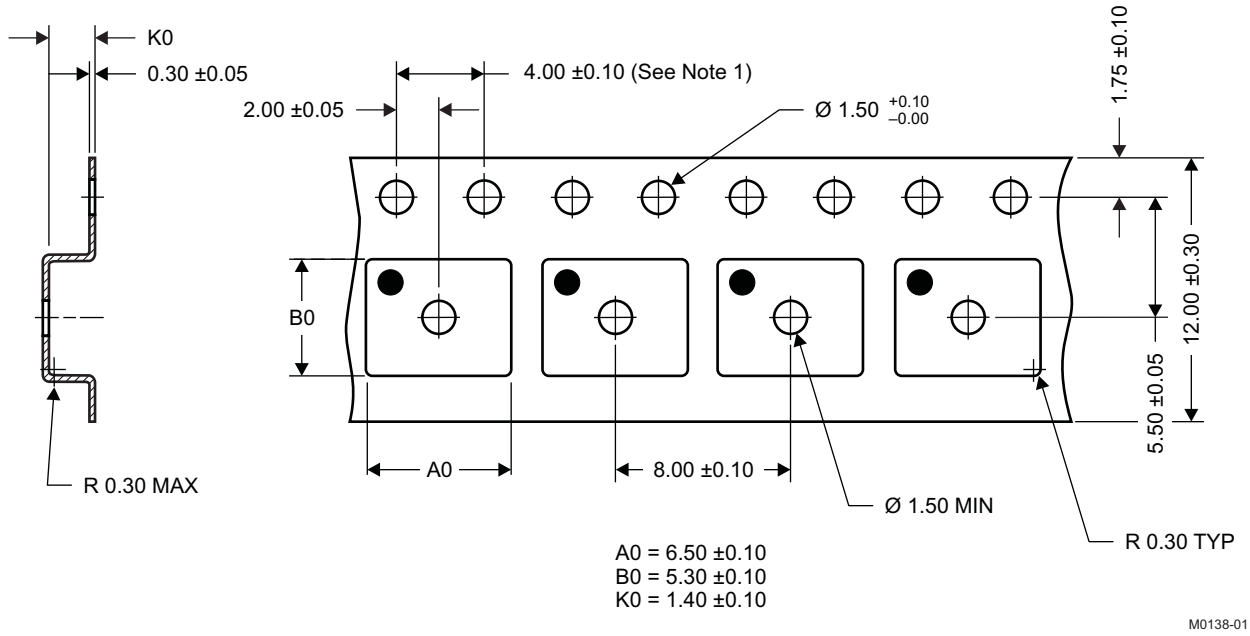
Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5A Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

REVISION HISTORY

Changes from Original (February 2010) to Revision A	Page
• Updated the Q5A Package Dimensions table. DIM c MAX was 0.30, DIM D2 MAX was 3.96, DIM e MIN was blank MAX was blank, DIM H NOM was 0.51 MAX was 0.61	6
• Deleted Note 6 from the Q5A Tape and Reel Information - "MSL1 260°C (IR and convection) PbF reflow compatible"	7
• Deleted the Package Marking Information section	7

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17302Q5A	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17302
CSD17302Q5A.B	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17302

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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