

CSD16570Q5B 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Extremely Low Resistance
- Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

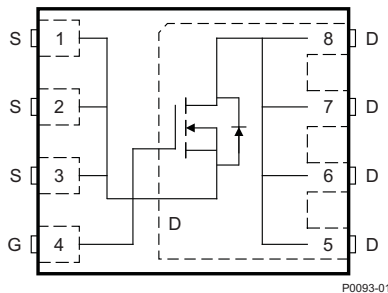
2 Applications

- ORing and Hot Swap Applications

3 Description

This 25 V, 0.49 mΩ, SON 5 × 6 mm NexFET™ power MOSFET is designed to minimize resistance for ORing and hot swap applications and is not designed for switching applications.

Top Icon



P0093-01

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	95		nC
Q_{gd}	Gate Charge Gate-to-Drain	31		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	0.68	mΩ
		$V_{GS} = 10\text{ V}$	0.49	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD16570Q5B	2500	13-Inch Reel	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD16570Q5BT	250	7-Inch Reel		

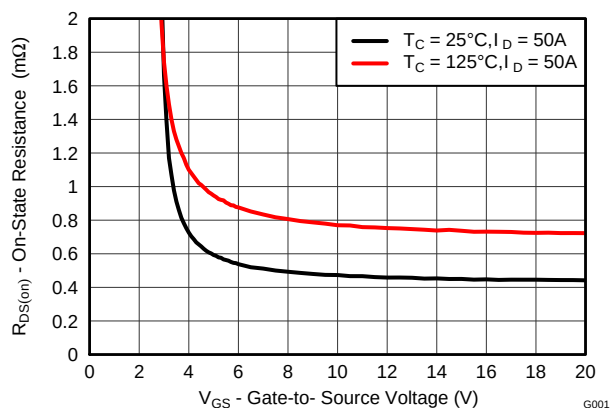
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

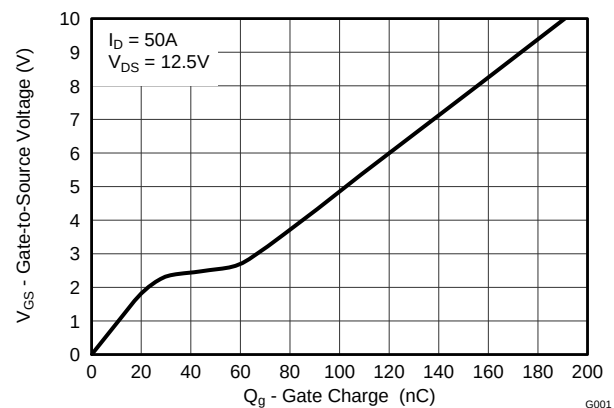
$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	456	
	Continuous Drain Current ⁽¹⁾	59	
I_{DM}	Pulsed Drain Current ⁽²⁾	400	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	195	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 98\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	480	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 0.8^\circ\text{C/W}$, Pulse duration ≤ 100 μs, duty cycle ≤ 1%

 $R_{DS(on)}$ vs V_{GS} 

G001

Gate Charge

G001



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4 Revision History

Changes from Original (July 2014) to Revision A	Page
• Added the <i>Receiving Notification of Documentation Updates</i> and <i>Community Resource</i> sections to <i>Device and Documentation Support</i>	7
• Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the <i>Recommended PCB Pattern</i> section diagram.....	9

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

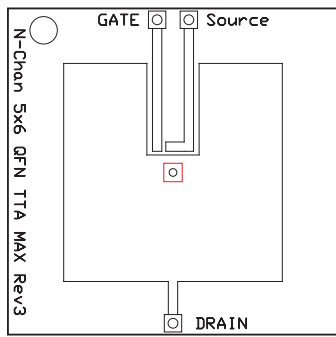
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	25			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 20 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.1	1.5	1.9	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V, I _D = 50 A	0.68		0.82	mΩ
		V _{GS} = 10 V, I _D = 50 A	0.49		0.59	mΩ
g _{fs}	Transconductance	V _{DS} = 2.5 V, I _D = 50 A	278			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 12 V, f = 1 MHz	10700		14000	pF
C _{oss}	Output Capacitance		1660		2160	pF
C _{rss}	Reverse Transfer Capacitance		996		1290	pF
R _G	Series Gate Resistance		1.8		3.6	Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 12.5 V, I _D = 50 A	95		124	nC
Q _g	Gate Charge Total (10 V)		192		250	nC
Q _{gd}	Gate Charge Gate-to-Drain		31			nC
Q _{gs}	Gate Charge Gate-to-Source		29			nC
Q _{g(th)}	Gate Charge at V _{th}		15			nC
Q _{oss}	Output Charge	V _{DS} = 12.5 V, V _{GS} = 0 V	35			nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5 V, V _{GS} = 10 V, I _{DS} = 50 A, R _G = 0 Ω	5			ns
t _r	Rise Time		43			ns
t _{d(off)}	Turn Off Delay Time		156			ns
t _f	Fall Time		72			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = 50 A, V _{GS} = 0 V	0.8		1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 12.5 V, I _F = 50 A, di/dt = 300A/μs	34			nC
t _{rr}	Reverse Recovery Time		21			ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

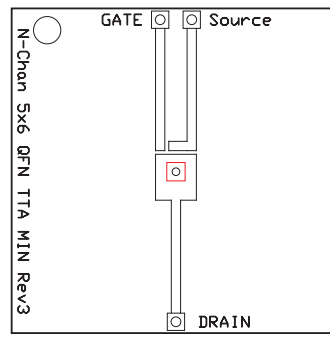
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-Case Thermal Resistance ⁽¹⁾			0.8	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			50	

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

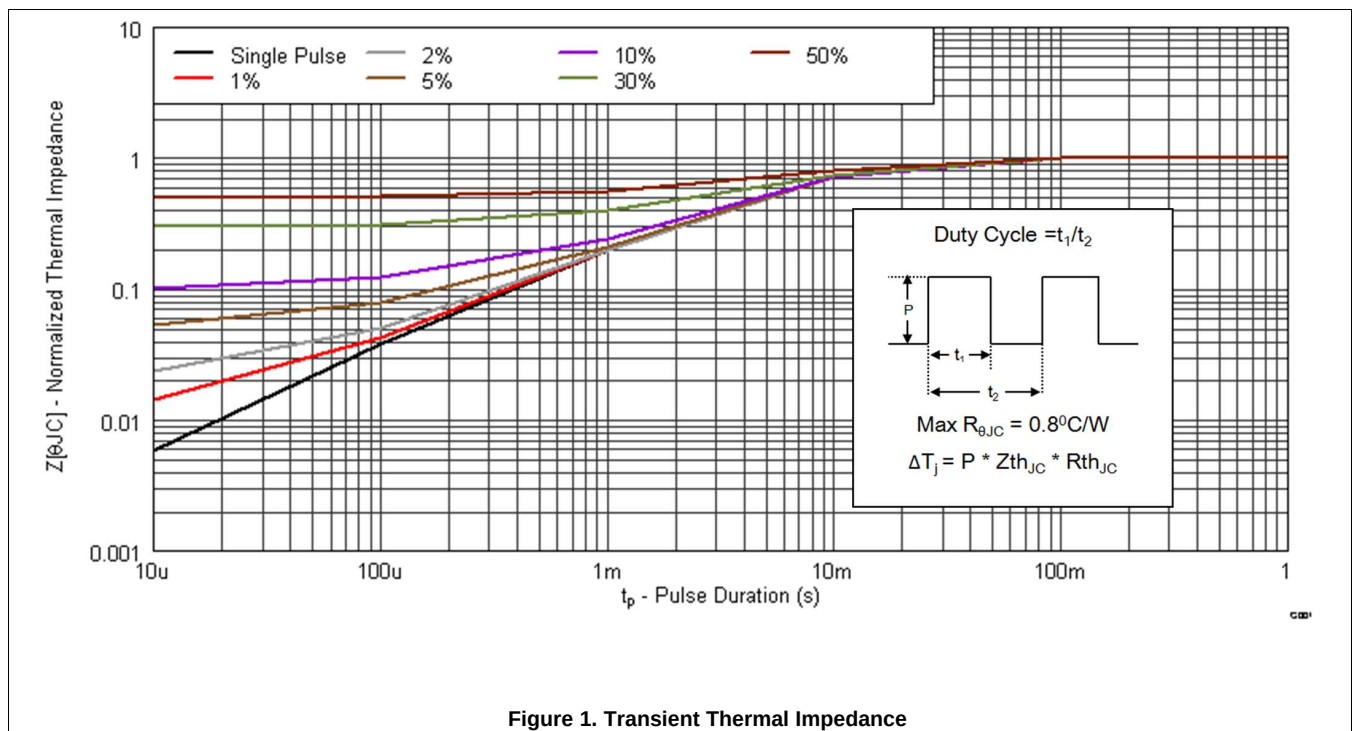


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Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

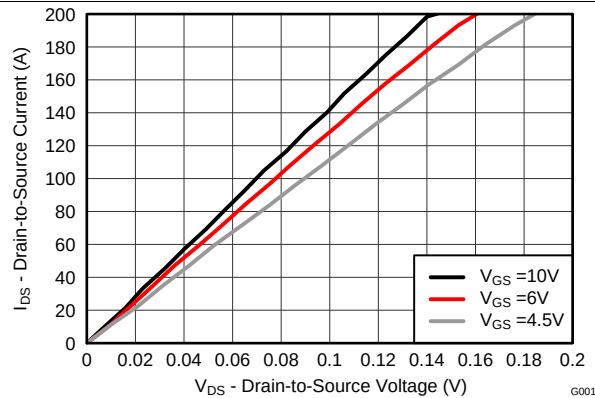


Figure 2. Saturation Characteristics

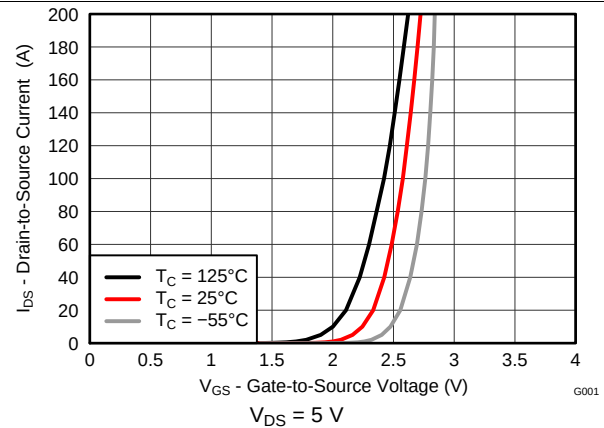


Figure 3. Transfer Characteristics

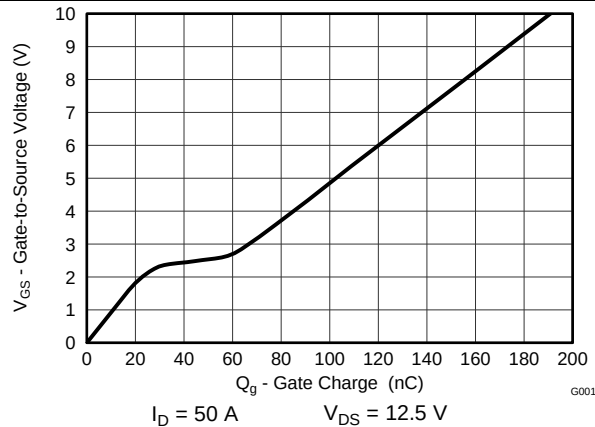


Figure 4. Gate Charge

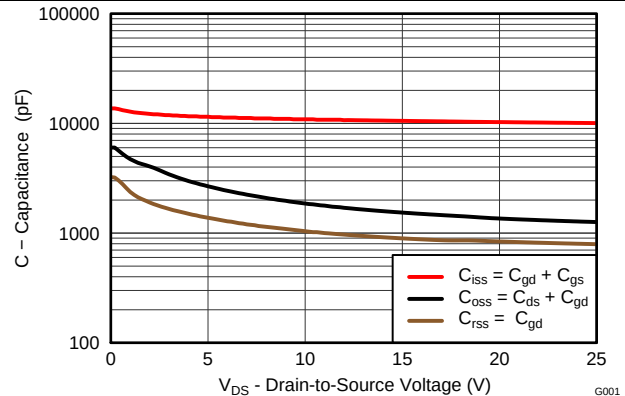


Figure 5. Capacitance

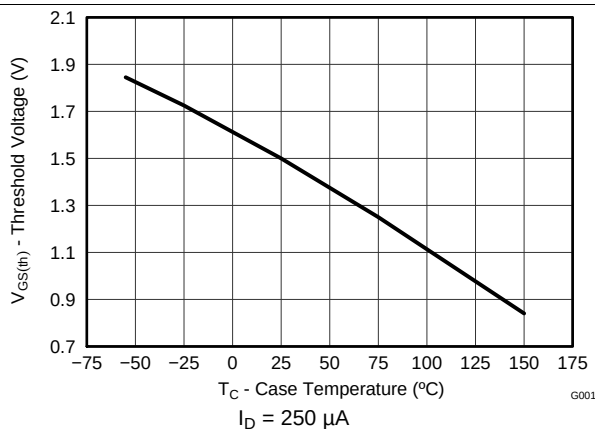


Figure 6. Threshold Voltage vs Temperature

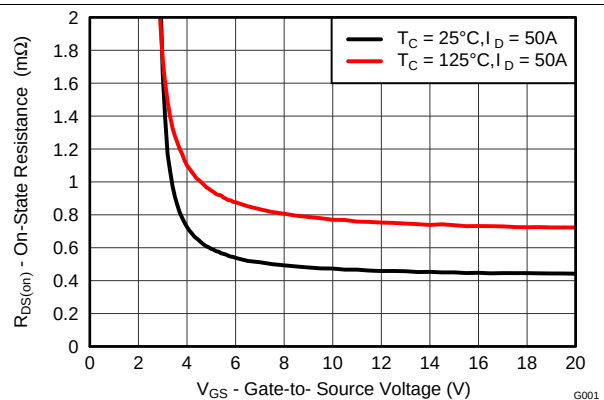


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

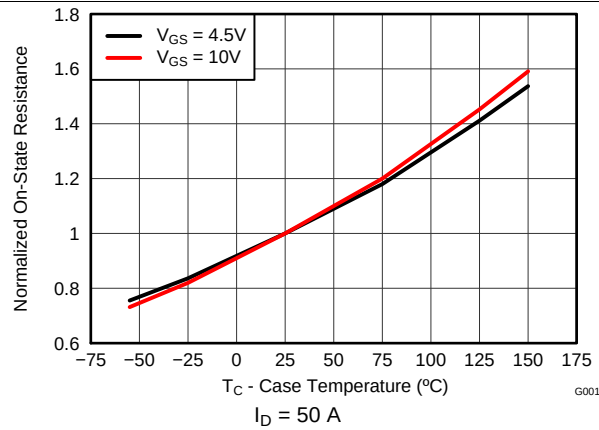


Figure 8. Normalized On-State Resistance vs Temperature

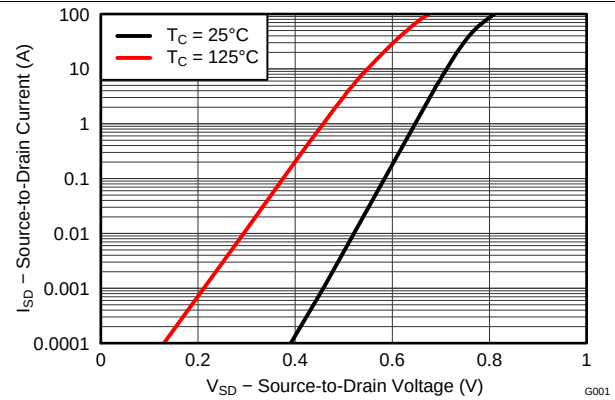


Figure 9. Typical Diode Forward Voltage

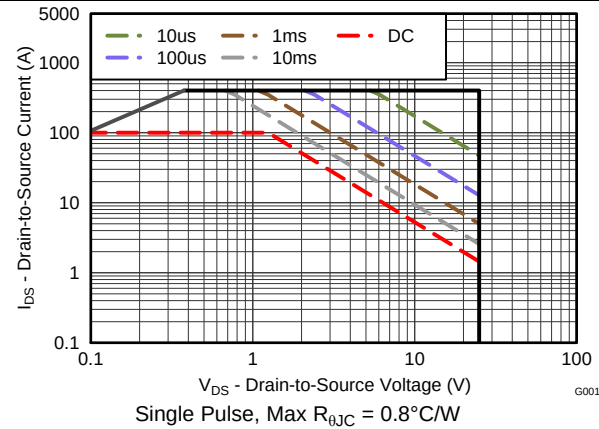


Figure 10. Maximum Safe Operating Area

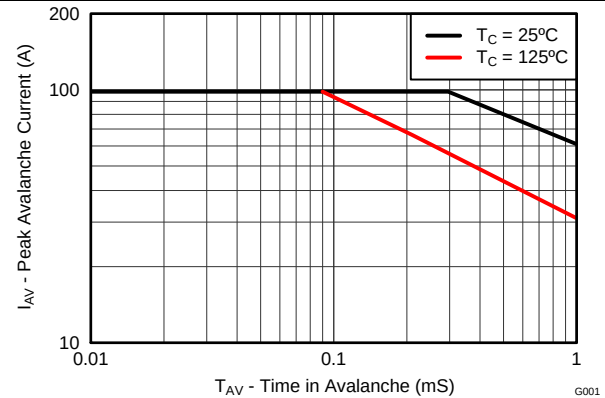


Figure 11. Single Pulse Unclamped Inductive Switching

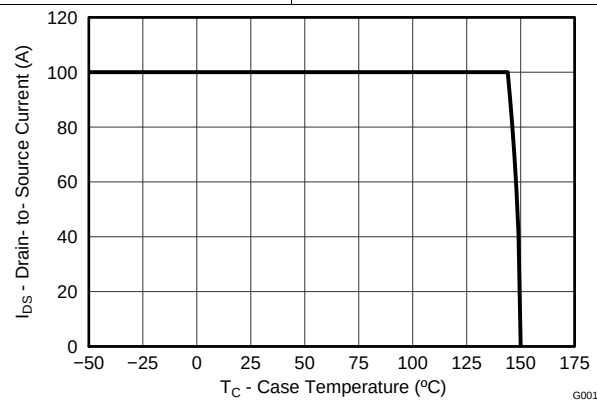


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.

6.4 Electrostatic Discharge Caution



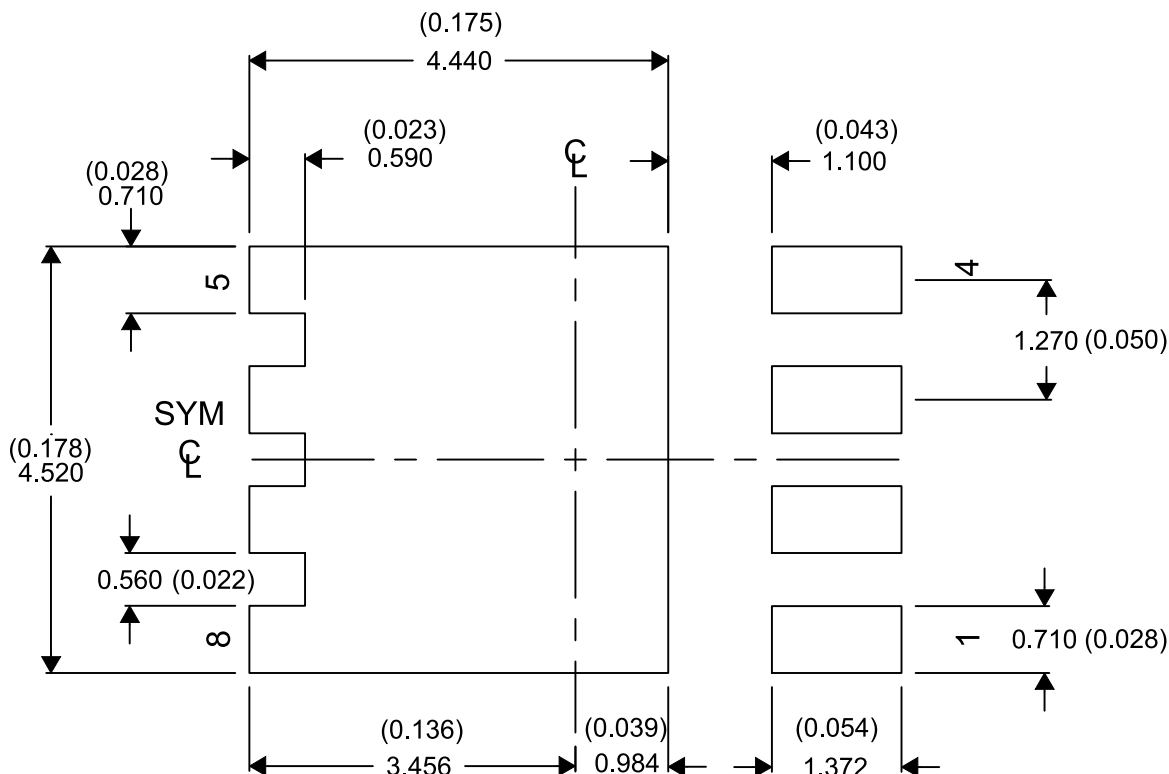
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

[SLYZ022](#) — *TI Glossary*.

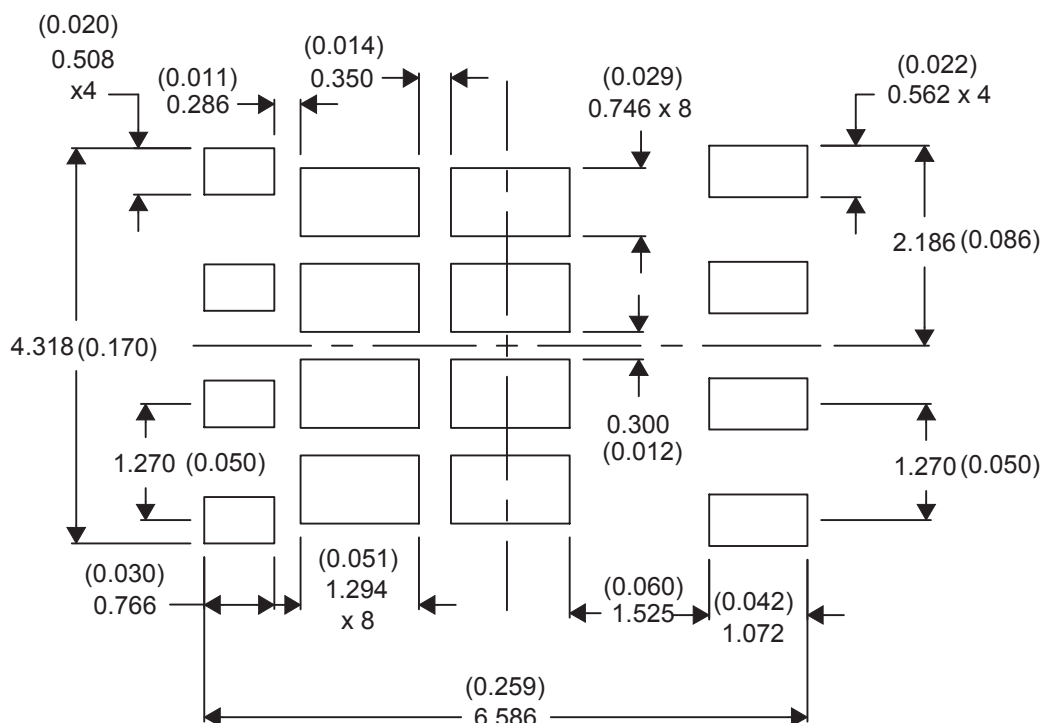
This glossary lists and explains terms, acronyms, and definitions.

7.2 Recommended PCB Pattern

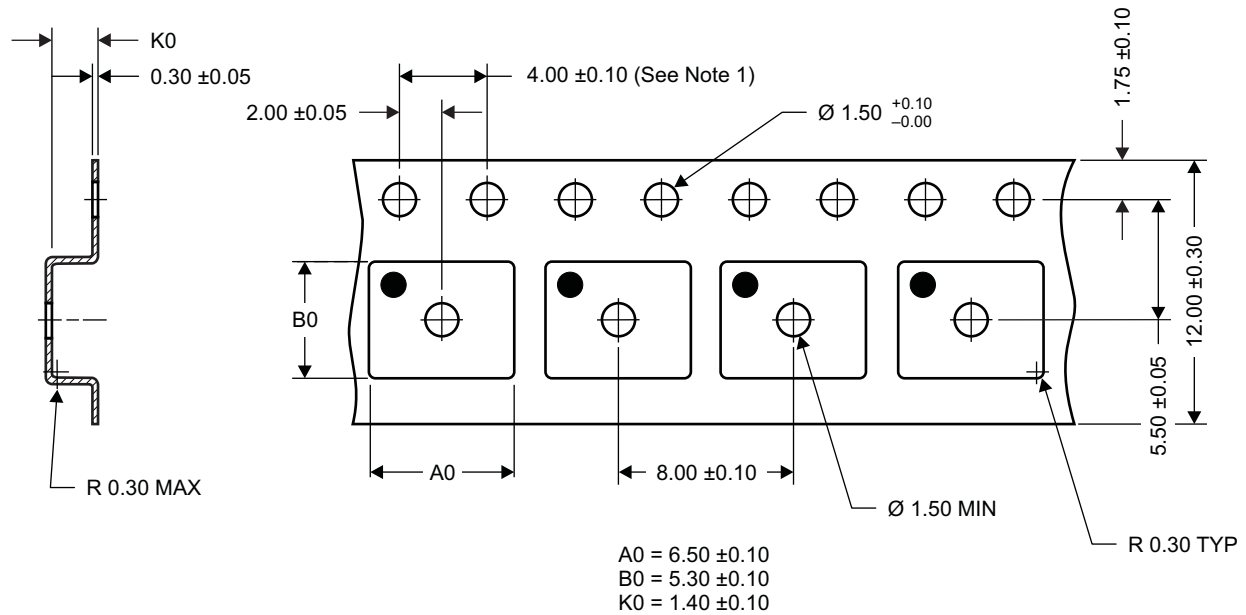


For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

7.3 Recommended Stencil Pattern



7.4 Q5B Tape and Reel Information



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Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified).
- A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16570Q5B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	CSD16570
CSD16570Q5B.B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD16570
CSD16570Q5BG4	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD16570
CSD16570Q5BG4.B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD16570
CSD16570Q5BT	Active	Production	VSON-CLIP (DNK) 8	250 SMALL T&R	ROHS Exempt	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	CSD16570
CSD16570Q5BT.B	Active	Production	VSON-CLIP (DNK) 8	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD16570

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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