TEXAS INSTRUMENTS

CSD16415Q5

SLPS259A – DECEMBER 2011 – REVISED SEPTEMBER 2015

CSD16415Q5 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Ultralow Q_g and Q_{gd}
- Very Low On-Resistance
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen-Free

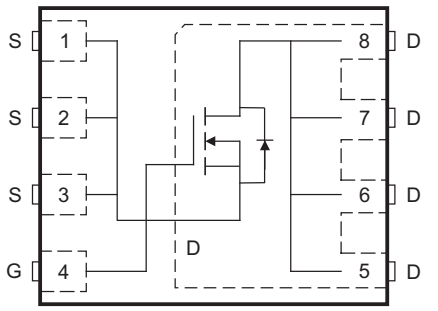
2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

3 Description

This 25 V, 1.3 mΩ, 5 x 6 mm SON NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



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Product Summary

T_A = 25°C		VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge, Total (4.5 V)	21		nC
Q_{gd}	Gate Charge, Gate-to-Drain	5.2		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	1.5	mΩ
		V_{GS} = 10 V	0.99	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

Device Information(1)

DEVICE	PACKAGE	MEDIA	QTY	SHIP
CSD16415Q5	SON 5-mm × 6-mm Plastic Package	13-inch Reel	2500	Tape and Reel

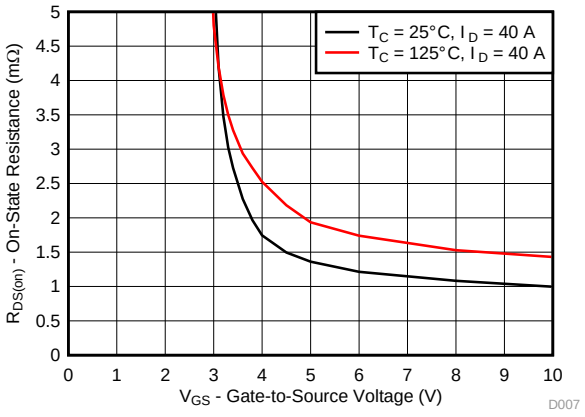
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	–12 to 16	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C(1)	261	
	Continuous Drain Current(1)	38	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	200	A
P_D	Power dissipation(1)	3.2	W
	Power Dissipation, , T_C = 25°C	156	
T_J, T_{stg}	Operating Junction and Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single-Pulse I_D = 100 A, L = 0.1 mH, R_G = 25 Ω	500	mJ

(1) $R_{\theta JA}$ = 40°C/W on 1 in² (6.45 cm²) Cu [2 oz. (0.071 mm thick)] on 0.060 inch (1.52 mm) thick FR4 PCB.
(2) Max $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(ON)}$ vs V_{GS}



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Gate Charge

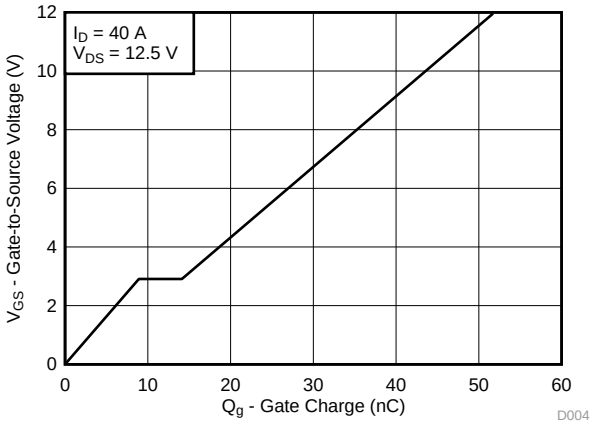

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Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2014) to Revision A	Page
• Added part number to title	1
• Enhanced Description	1
• Added *Device and Documentation Support* section and *Mechanical, Packaging, and Orderable Information* section	1
• Updated pulsed current	1
• Updated Figure 1 to a normalized $R_{\theta JC}$ curve	4
• Updated the SOA in Figure 10	5
• Deleted *Package Marking Information* section at the end of the data sheet	10

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	25			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 20 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –12 V to 16 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.2	1.5	1.9	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V, I_D = 40 A		1.5	1.8	mΩ
		V_{GS} = 10 V, I_D = 40 A		0.99	1.15	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 40 A		168		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		3150	4100	pF
C_{OSS}	Output Capacitance			2530	3300	pF
C_{RSS}	Reverse Transfer Capacitance			175	230	pF
R_g	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 12.5 V, ID = 40 A		21	29	nC
Q_{gd}	Gate Charge, Gate-to-Drain			5.2		nC
Q_{gs}	Gate Charge, Gate-to-Source			8.3		nC
Qg(th)	Gate Charge at Vth			4.8		nC
Q_{OSS}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		55		nC
$t_{d(on)}$	Turnon Delay Time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 40 A, R_G = 2 Ω		16.6		ns
t_r	Rise Time			30		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			12.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = 40 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/µs		72		nC
t_{rr}	Reverse Tecovery Time	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/µs		45		ns

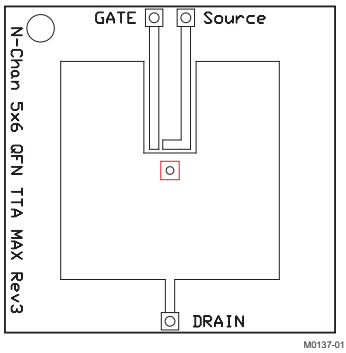
5.2 Thermal Information

T_A = 25°C (unless otherwise noted)

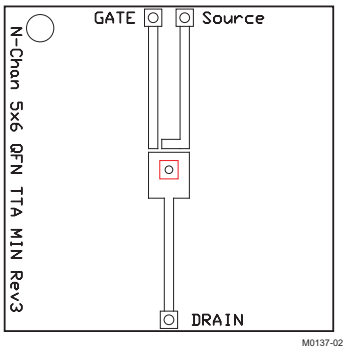
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case(1)			0.8	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch (2.54 cm) square, 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.060 inch (1.52 mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1 $inch^2$ (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

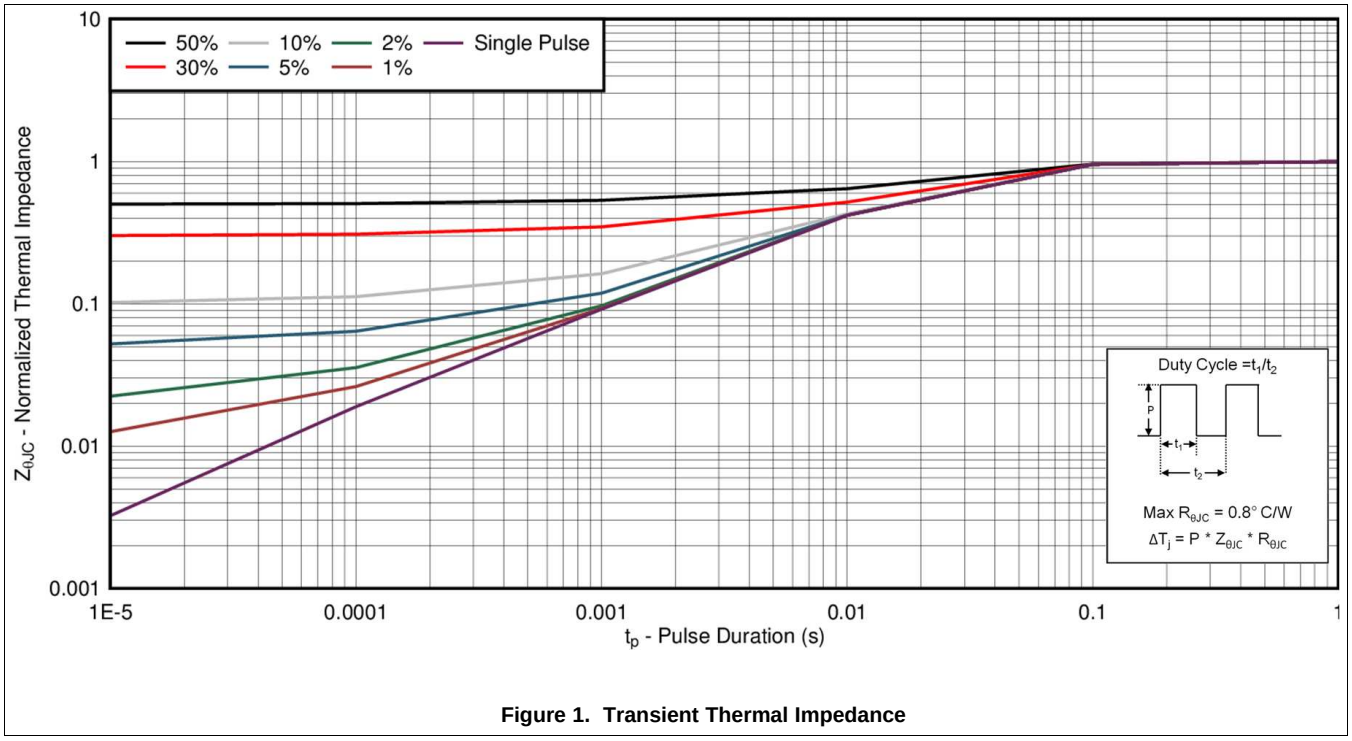


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)

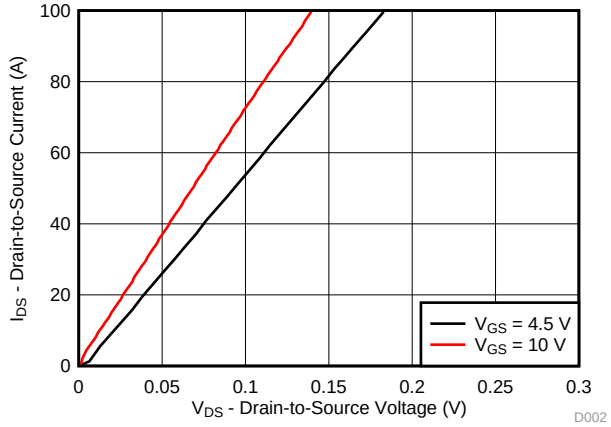


Figure 2. Saturation Characteristics

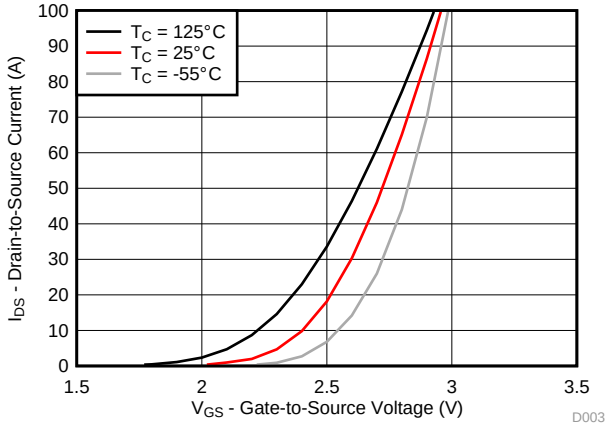


Figure 3. Transfer Characteristics

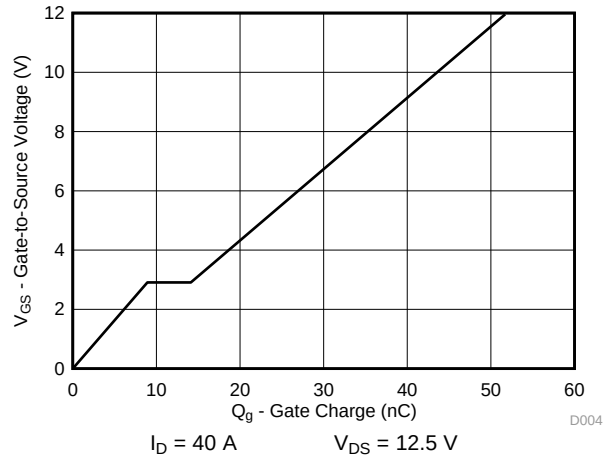


Figure 4. Gate Charge

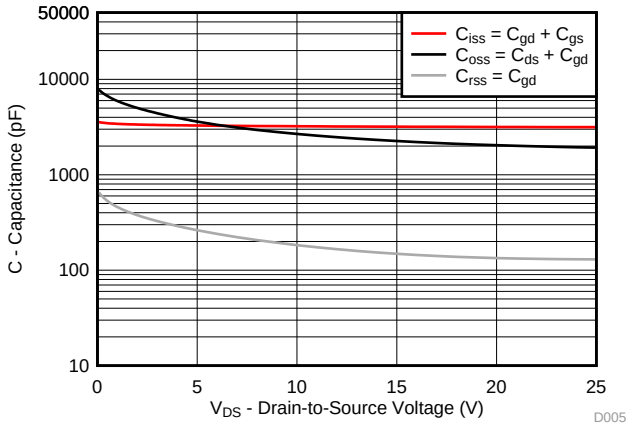


Figure 5. Capacitance

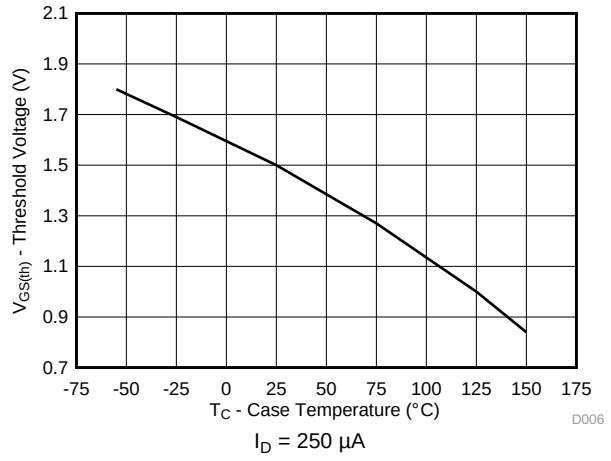


Figure 6. Threshold Voltage vs Temperature

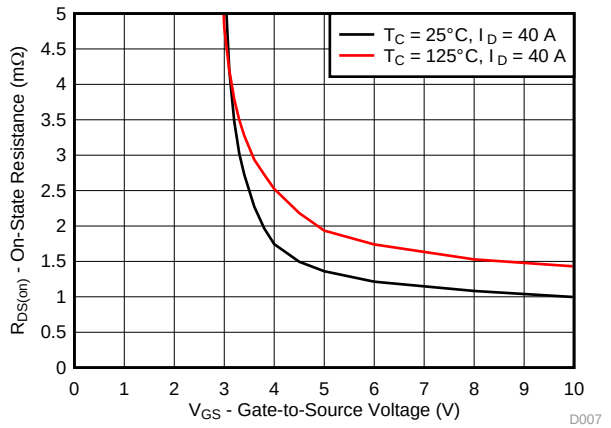
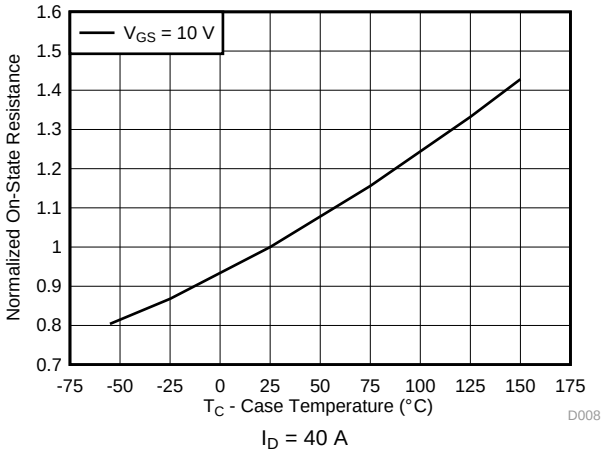


Figure 7. On-Resistance vs Gate Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)



I_D = 40 A

Figure 8. On-Resistance vs Temperature

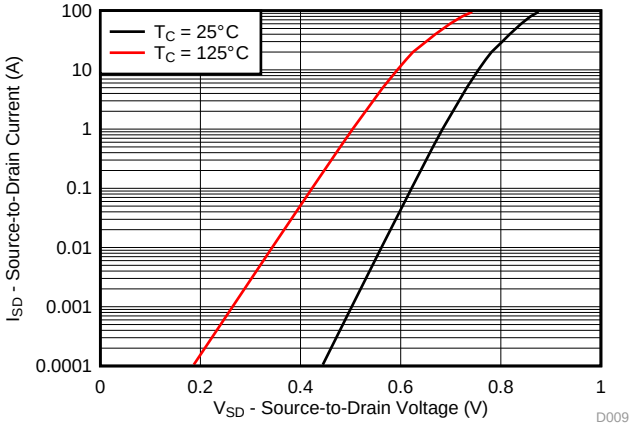
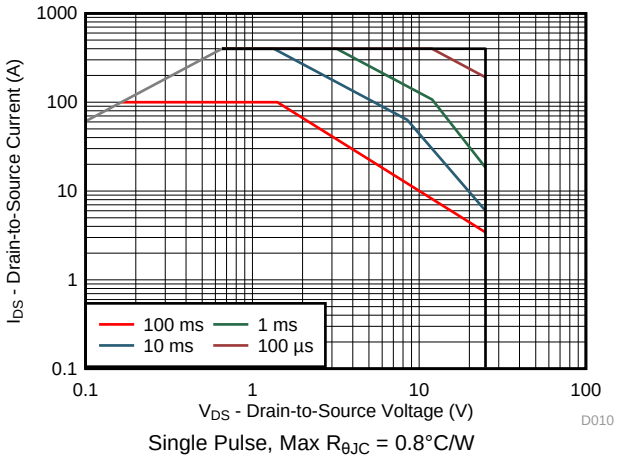


Figure 9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JC}$ = 0.8°C/W

Figure 10. Maximum Safe Operating Area

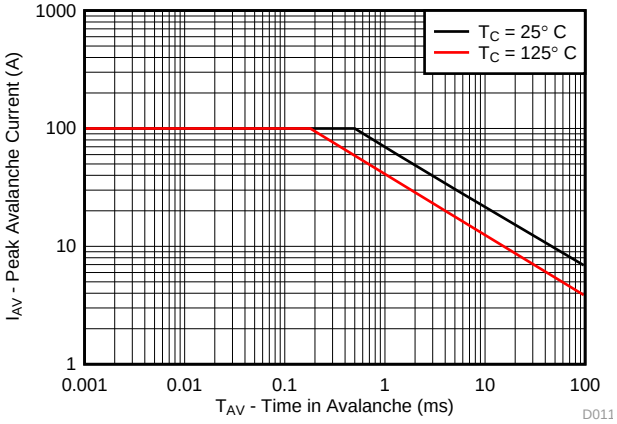


Figure 11. Single-Pulse Unclamped Inductive Switching

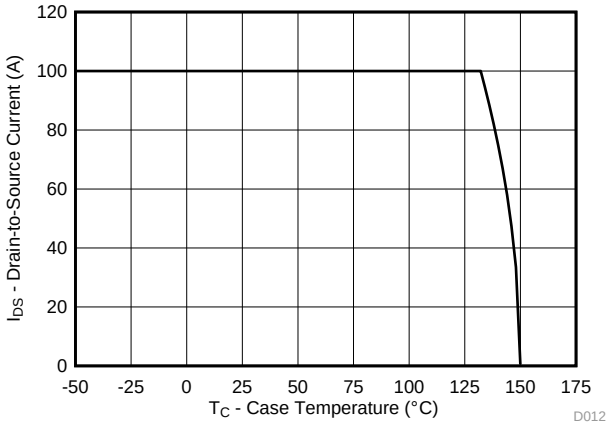


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

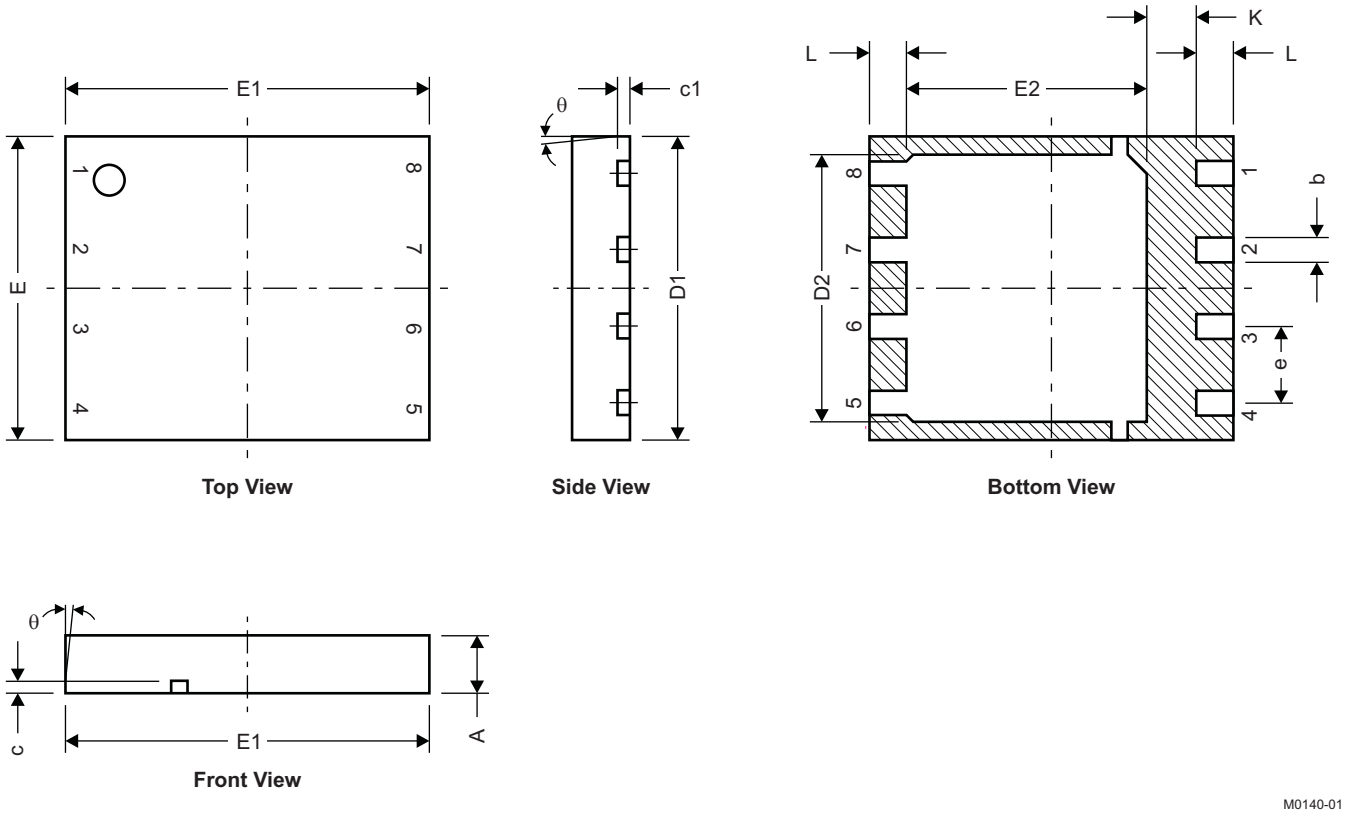
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

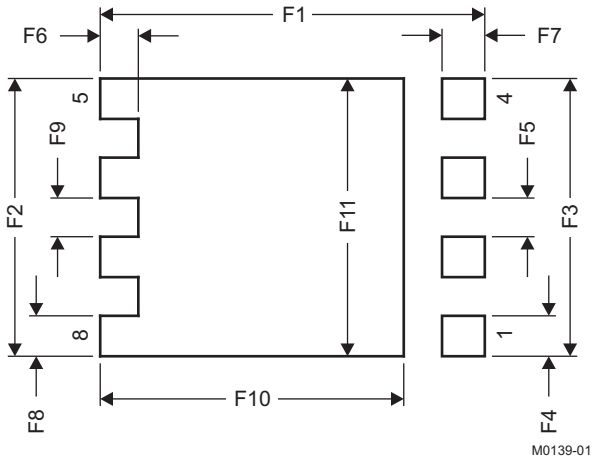
7.1 Q5 Package Dimensions



M0140-01

DIM	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.950		1.050	0.037		0.039
b	0.360		0.460	0.014		0.018
c	0.150		0.250	0.006		0.010
c1	0.150		0.250	0.006		0.010
D1	4.900		5.100	0.193		0.201
D2	4.320		4.520	0.170		0.178
E	4.900		5.100	0.193		0.201
E1	5.900		6.100	0.232		0.240
E2	3.920		4.12	0.154		0.162
e		1.27			0.050	
K	0.760			0.030		
L	0.510		0.710	0.020		0.028
θ	0.00					

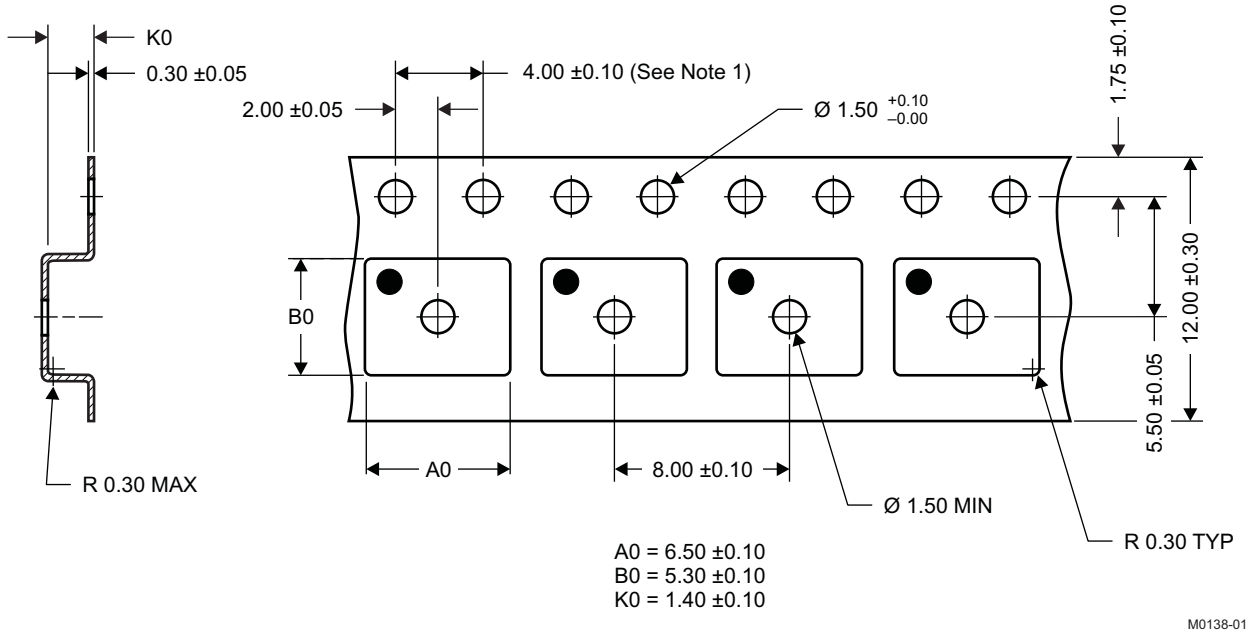
7.2 Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Q5 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black, static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16415Q5	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16415
CSD16415Q5.B	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16415
CSD16415Q5T	Active	Production	VSON-CLIP (DQH) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16415
CSD16415Q5T.B	Active	Production	VSON-CLIP (DQH) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16415

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

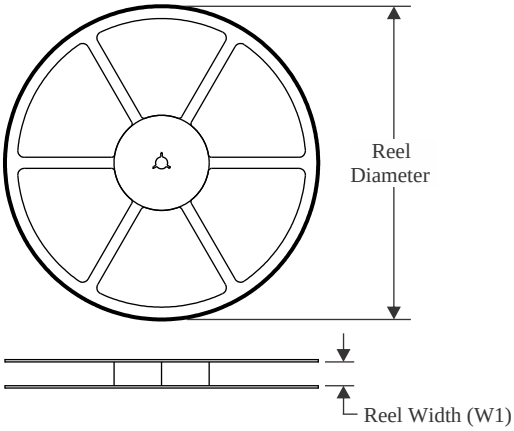
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

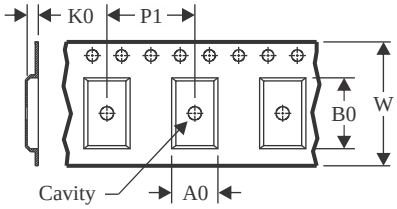
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

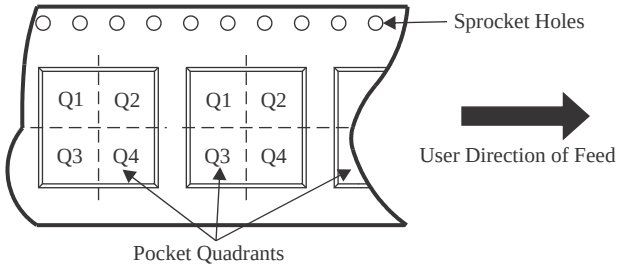


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

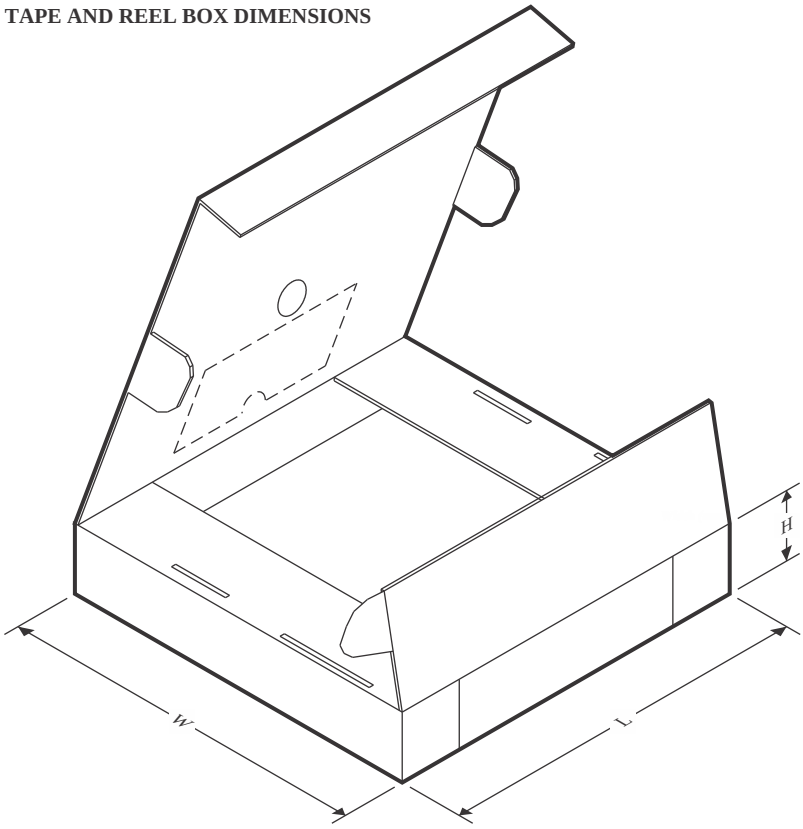
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16415Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

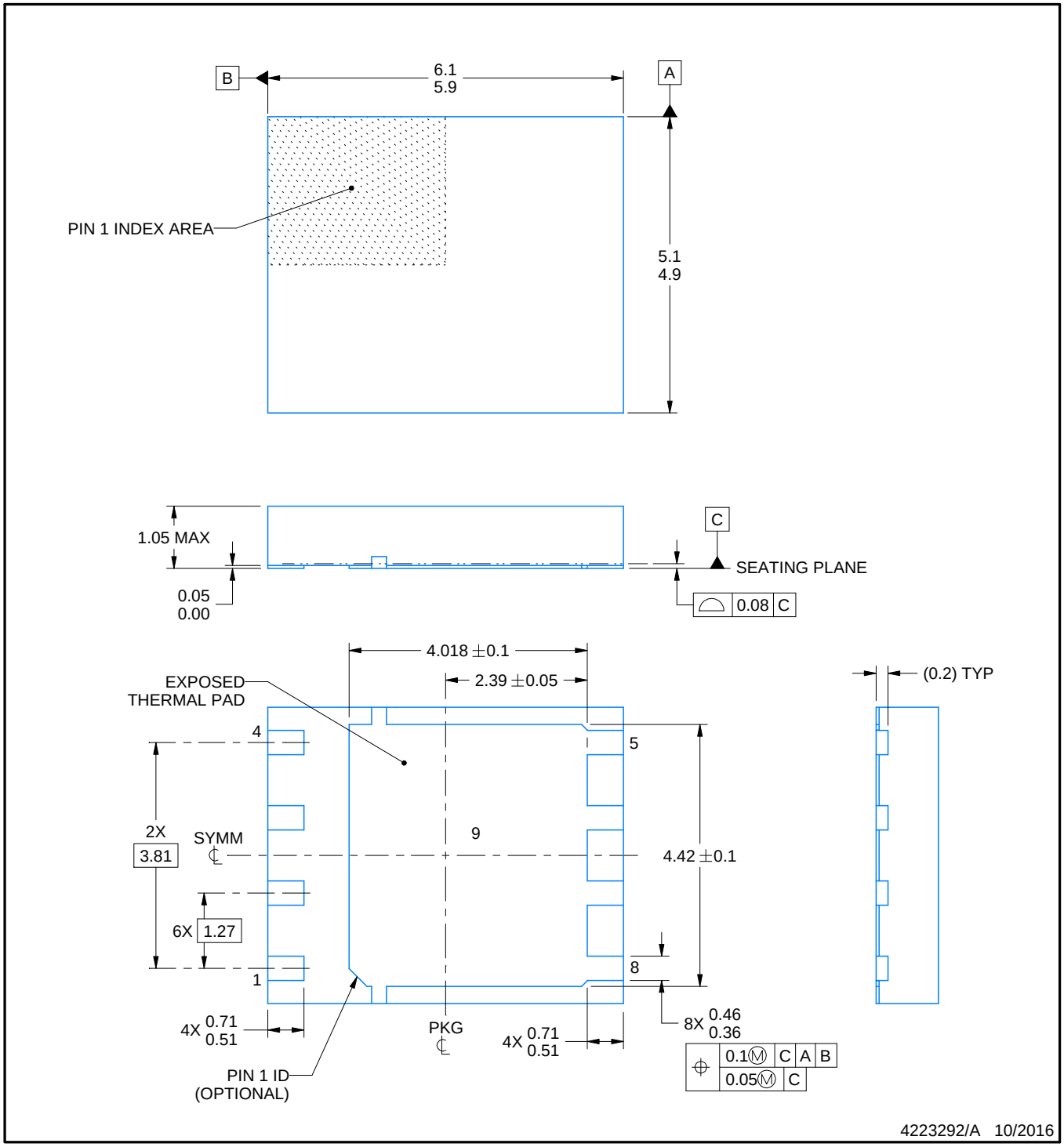
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16415Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

PACKAGE OUTLINE

DQH0008A

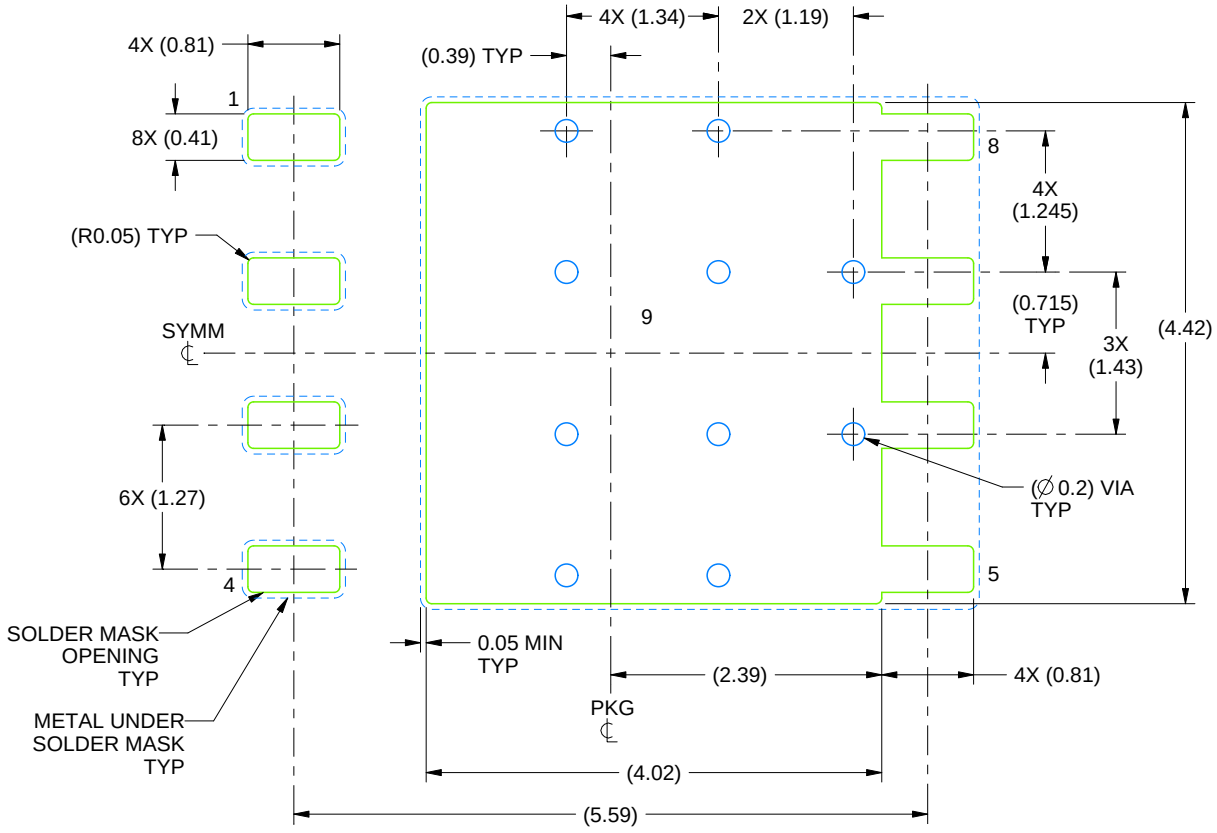
VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

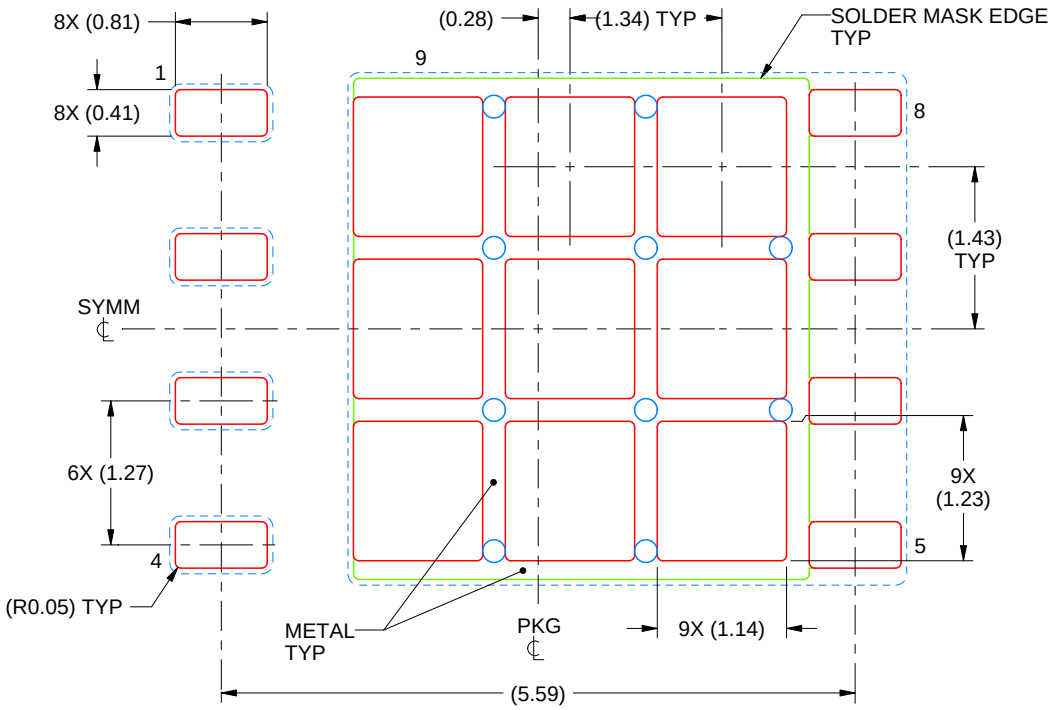


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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