



CSD16340Q3 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Optimized for 5 V Gate Drive
- Resistance Rated at $V_{GS} = 2.5$ V
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

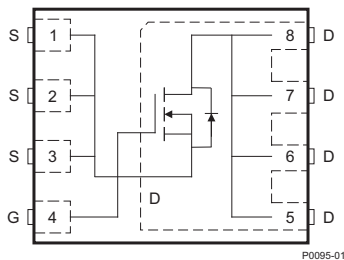
2 Applications

- Point of Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control or Synchronous FET Applications

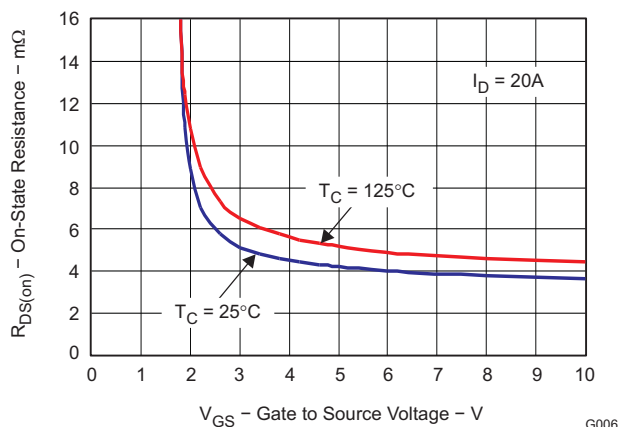
3 Description

This 25 V, 3.8 mΩ, 3.3 × 3.3 mm SON NexFET™ power MOSFET is designed to minimize losses in power conversion and optimized for 5 V gate drive applications.

Top View



$R_{DS(on)}$ vs V_{GS}



Product Summary

$T_A = 25^\circ\text{C}$		VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	6.5		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.2		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5$ V	6.1	mΩ
		$V_{GS} = 4.5$ V	4.3	mΩ
		$V_{GS} = 8$ V	3.8	mΩ
V_{th}	Threshold Voltage	0.85		V

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD16340Q3	13-Inch Reel	2500	SON 3.3 x 3.3 mm Plastic Package	Tape and Reel
CSD16340Q3T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current ⁽¹⁾	21	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	115	A
P_D	Power Dissipation ⁽¹⁾	3	W
T_J , T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 40$ A, $L = 0.1$ mH, $R_G = 25 \Omega$	80	mJ

(1) Typical $R_{\theta JA} = 39^\circ\text{C/W}$ on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

Gate Charge

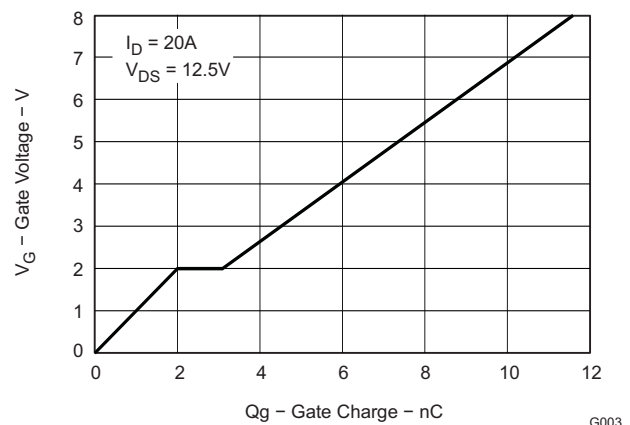


Table of Contents

1 Features	1	6.1 Trademarks	8
2 Applications	1	6.2 Electrostatic Discharge Caution	8
3 Description	1	6.3 Glossary	8
4 Revision History	2	7 Mechanical, Packaging, and Orderable Information	9
5 Specifications	3	7.1 Q3 Package Dimensions	9
5.1 Electrical Characteristics	3	7.2 Recommended PCB Pattern	10
5.2 Thermal Information	4	7.3 Recommended Stencil Opening	10
5.3 Typical MOSFET Characteristics	5	7.4 Q3 Tape and Reel Information	11
6 Device and Documentation Support	8		

4 Revision History

Changes from Revision D (November 2011) to Revision E	Page
• Added 7" reel to Ordering Information	1
• Updated Mechanical Information	9

Changes from Revision C (June 2011) to Revision D	Page
• Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table	4
• Replaced Figure 10 - Maximum Safe Operating Area	6

Changes from Revision B (September 2010) to Revision C	Page
• Deleted the Package Marking Information section	9

Changes from Revision A (January 2010) to Revision B	Page
• Changed Figure 2 , reversed the order of the V_{GS} labels	5

Changes from Original (December 2009) to Revision A	Page
• Changed Q_g in the PRODUCT SUMMARY table from: 6.8 To 6.5 nC	1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	25			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 20 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = +10/–8 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	0.6	0.85	1.1	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 2.5 V, I _{DS} = 20 A	6.1		7.8	mΩ
		V _{GS} = 4.5 V, I _{DS} = 20 A	4.3		5.5	mΩ
		V _{GS} = 8 V, I _{DS} = 20 A	3.8		4.5	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _{DS} = 20 A	121			S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 12.5 V, f = 1 MHz	1050		1350	pF
C _{OSS}	Output Capacitance		730		950	pF
C _{RSS}	Reverse Transfer Capacitance		53		69	pF
R _g	Series Gate Resistance	V _{DS} = 12.5 V, I _D = 20 A	1.5		3	Ω
Q _g	Gate Charge Total (4.5 V)		6.5		9.2	nC
Q _{gd}	Gate Charge Gate-to-Drain		1.2			nC
Q _{gs}	Gate Charge Gate-to-Source		2.1			nC
Q _{g(th)}	Gate Charge at V _{th}		1			nC
Q _{OSS}	Output Charge		15			nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5 V, V _{GS} = 4.5 V, I _D = 20 A R _G = 2 Ω	4.8			ns
t _r	Rise Time		16.1			ns
t _{d(off)}	Turn Off Delay Time		13.8			ns
t _f	Fall Time		5.2			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _S = 20 A, V _{GS} = 0 V	0.8		1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13 V, I _F = 20 A, di/dt = 300 A/μs	14.5			nC
t _{rr}	Reverse Recovery Time		20			ns

CSD16340Q3

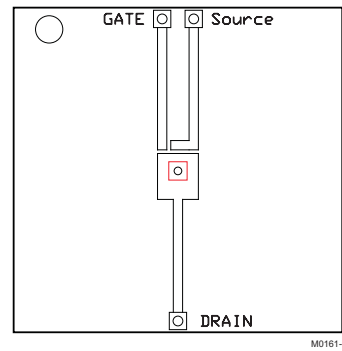
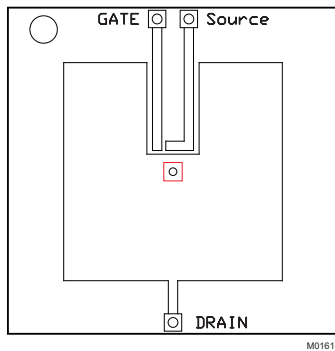
SLPS247E – DECEMBER 2009 – REVISED AUGUST 2014

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5.2 Thermal Information

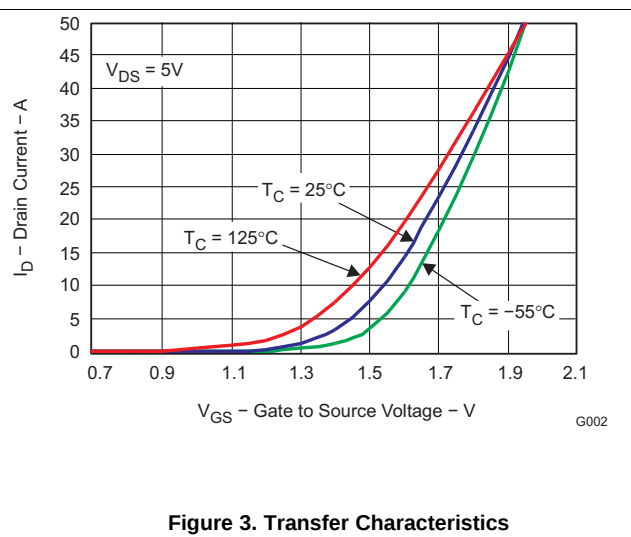
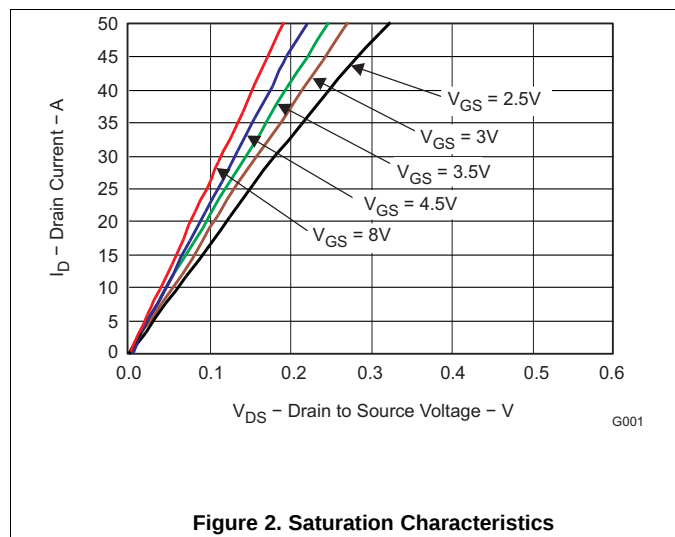
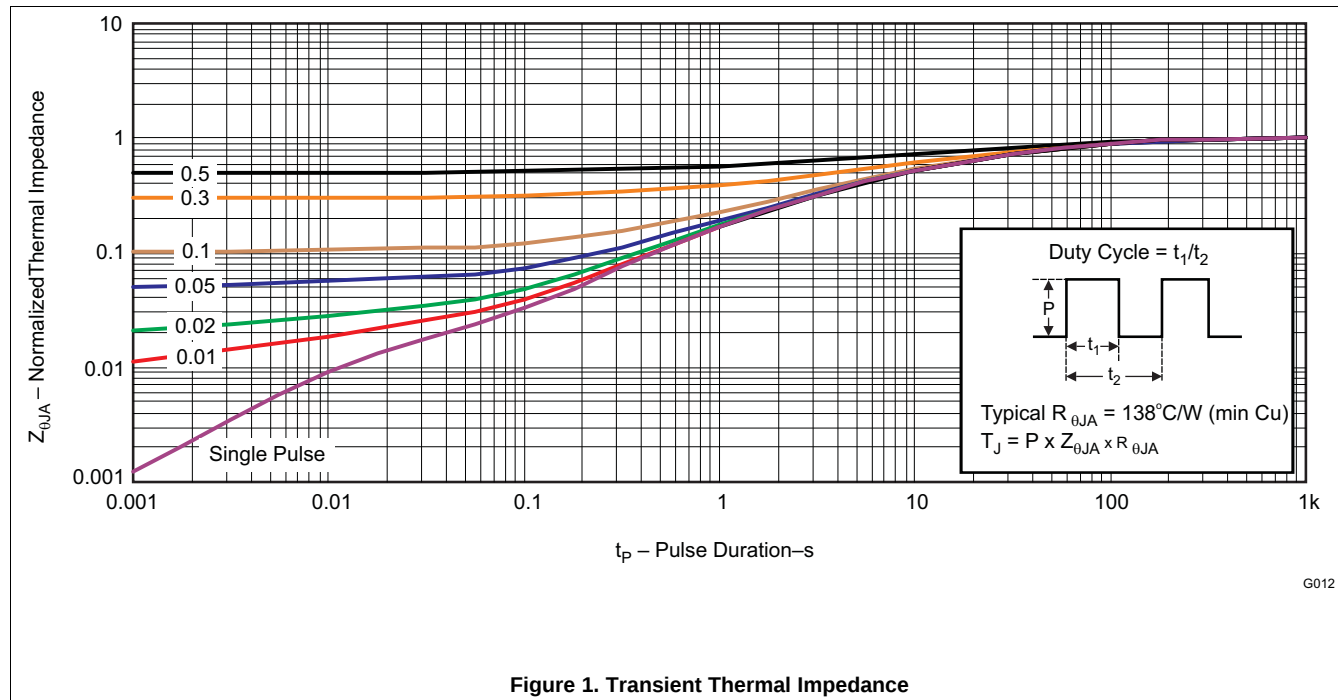
THERMAL METRIC ⁽¹⁾⁽²⁾		CSD16340Q3	UNITS
		Q3 (8 PINS)	
θ_{JA}	Junction-to-Ambient Thermal Resistance	42.0	°C/W
θ_{JCTop}	Junction-to-Case (top) Thermal Resistance	20.6	
θ_{JB}	Junction-to-Board Thermal Resistance	8.8	
Ψ_{JT}	Junction-to-Top Characterization Parameter	0.3	
Ψ_{JB}	Junction-to-Board Characterization Parameter	8.7	
θ_{JCbott}	Junction-to-Case (bottom) Thermal Resistance	0.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).



5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

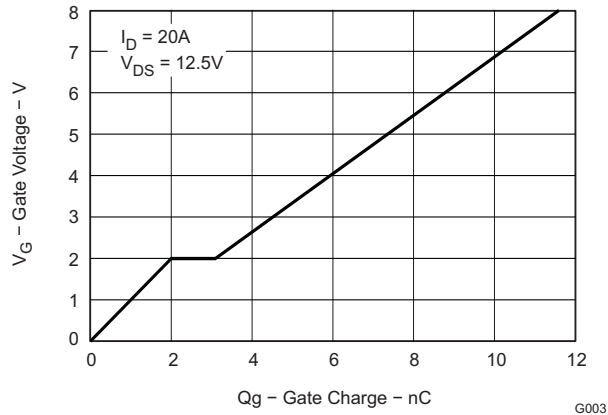


Figure 4. Gate Charge

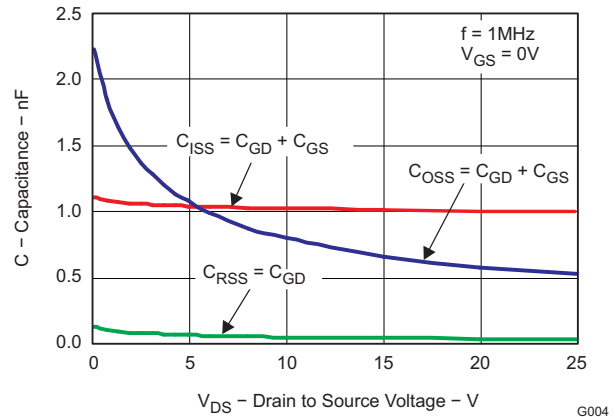


Figure 5. Capacitance

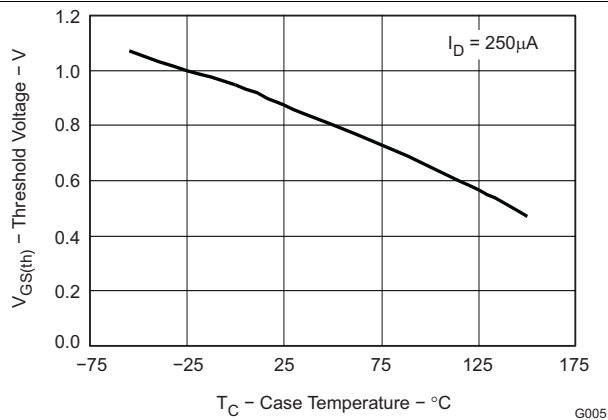


Figure 6. Threshold Voltage vs Temperature

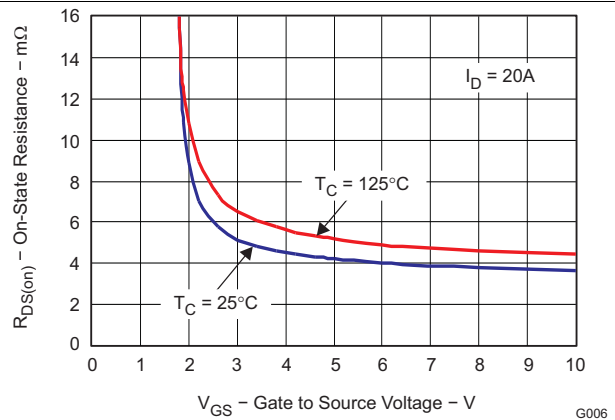


Figure 7. On-Resistance vs Gate Voltage

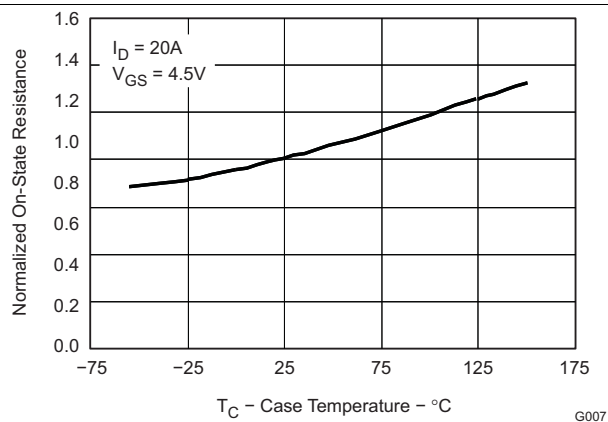


Figure 8. Normalized On Resistance vs Temperature

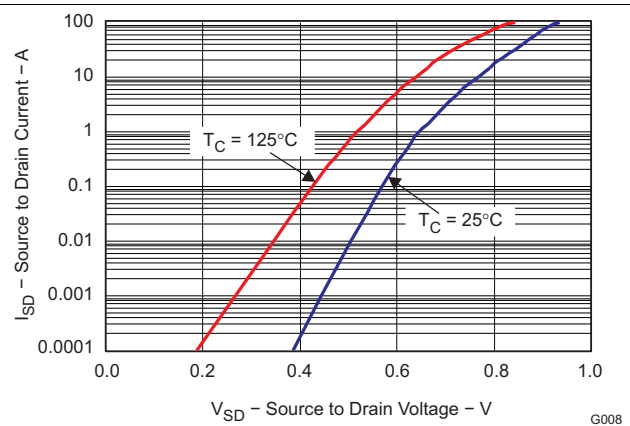


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

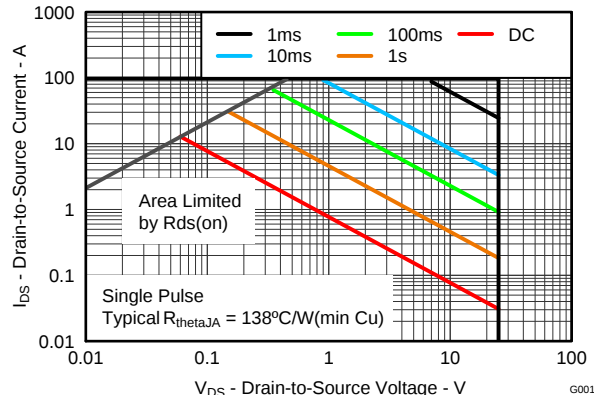


Figure 10. Maximum Safe Operating Area

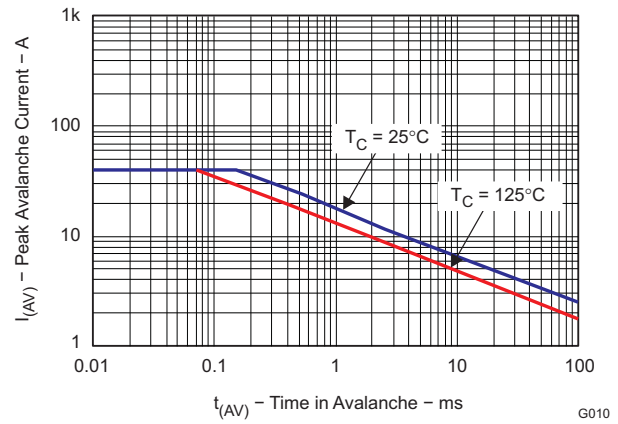


Figure 11. Single Pulse Unclamped Inductive Switching

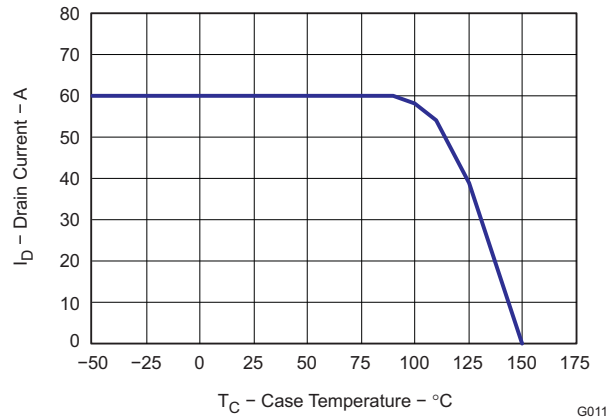


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

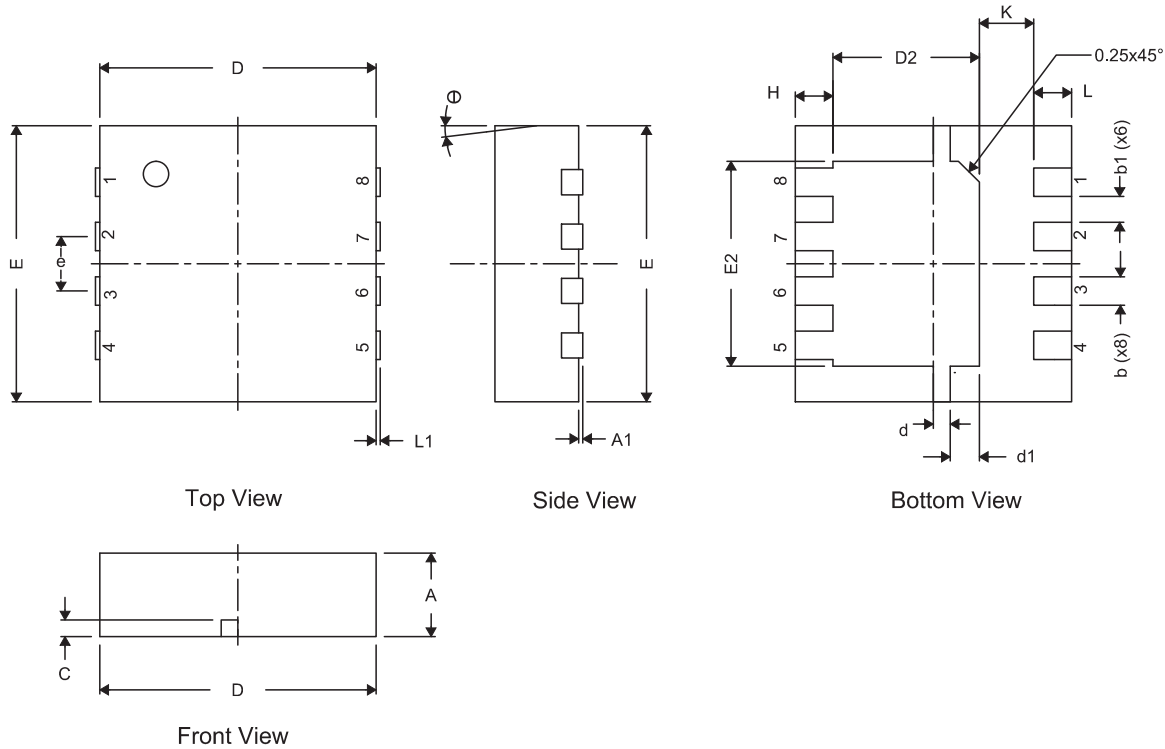
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

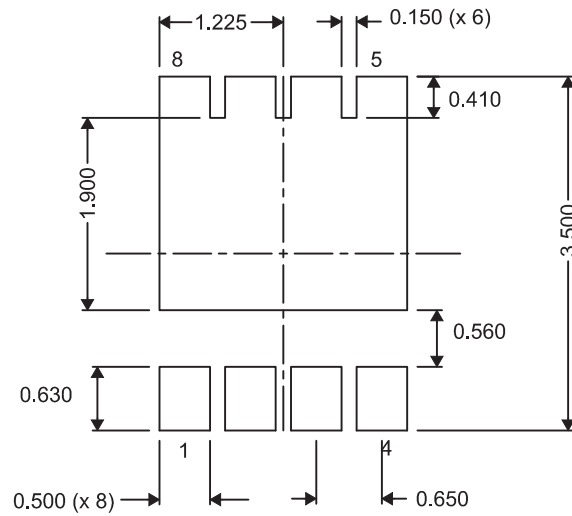
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



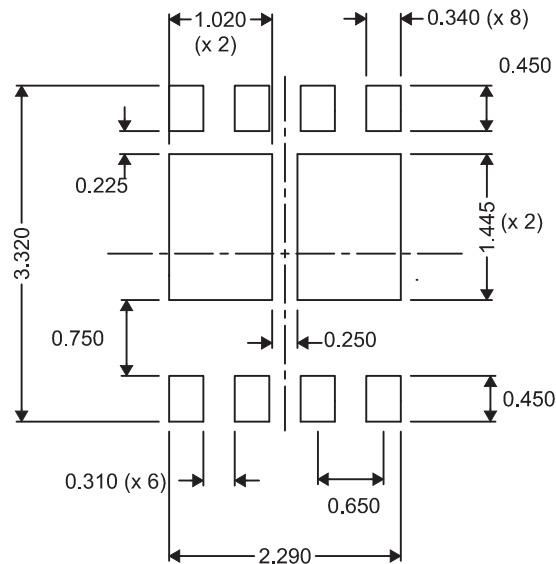
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



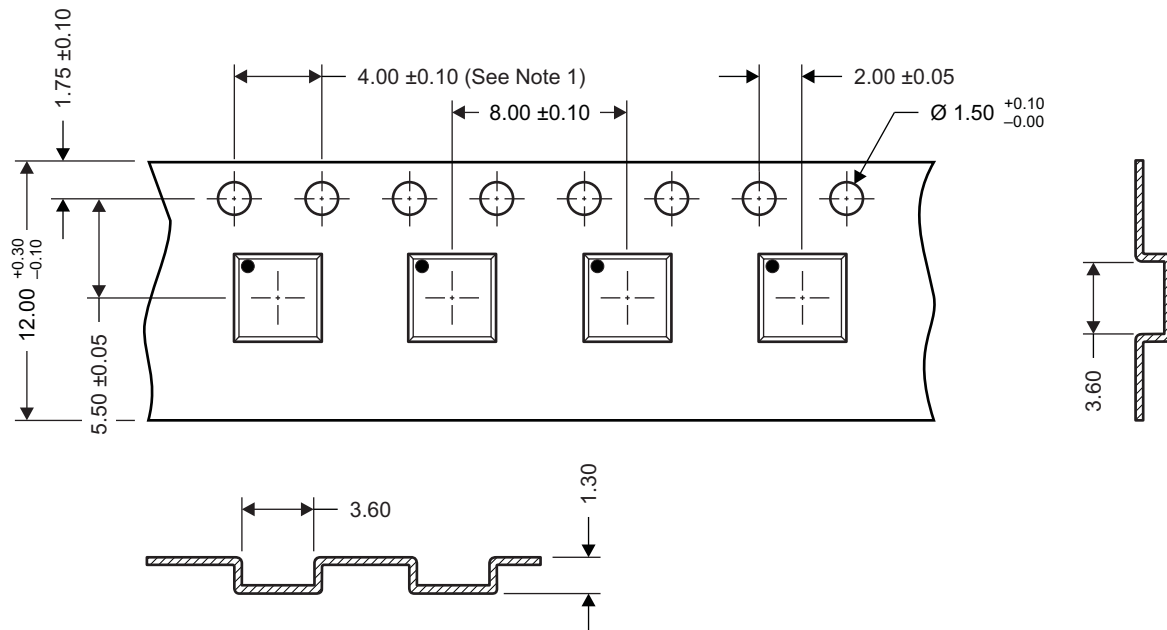
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16340Q3	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16340
CSD16340Q3.B	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16340
CSD16340Q3T	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16340
CSD16340Q3T.B	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16340

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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