

CSD16321Q5 25V、N チャネル NexFET™ パワー MOSFET

1 特長

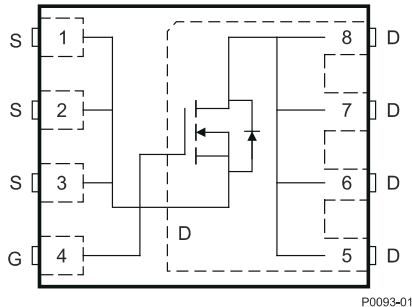
- 5V ゲートの駆動に最適化
- 非常に低い Q_g および Q_{gd}
- 低い熱抵抗
- アバランシェ定格
- 鉛フリーの端子メッキ処理
- RoHS 準拠
- SON 5mm × 6mm プラスチック・パッケージ

2 アプリケーション

- ネットワーク、テレコム、コンピューティング・システム・アプリケーション用のポイント・オブ・ロード(POL)同期整流降圧型コンバータ
- 同期 FET アプリケーション用に最適化

3 概要

この 25V、1.9mΩ、5mm × 6mm の SON NexFET™ パワー MOSFET は、電力変換アプリケーションでの損失を最小限に抑えるように設計されています。



上面図

製品概要

$T_A = 25^\circ\text{C}$		標準値	単位
V_{DS}	ドレイン - ソース間電圧	25	V
Q_g	ゲートの合計電荷 (4.5V)	14	nC
Q_{gd}	ゲート-ドレイン間ゲート電荷	2.5	nC
$R_{DS(on)}$	ドレイン - ソース間オン抵抗	$V_{GS} = 3V$	2.8
		$V_{GS} = 4.5V$	2.1
		$V_{GS} = 8V$	1.9
$V_{GS(th)}$	スレッショルド電圧	1.1	V

製品情報 (1)

デバイス	メディア	数量	パッケージ	出荷形態
CSD16321Q5	13 インチ・リール	2500	SON 5.00mm × 6.00mm プラスチック パッケージ	テープ およびリール
CSD16321Q5T	7 インチ・リール	250		

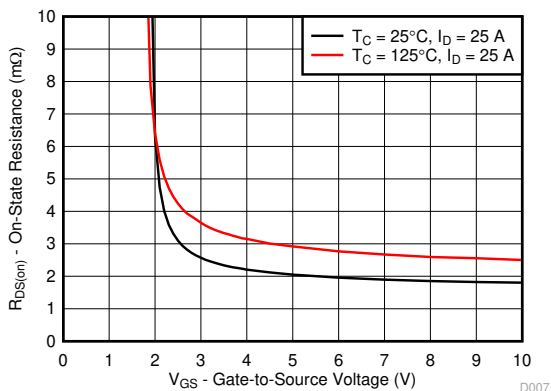
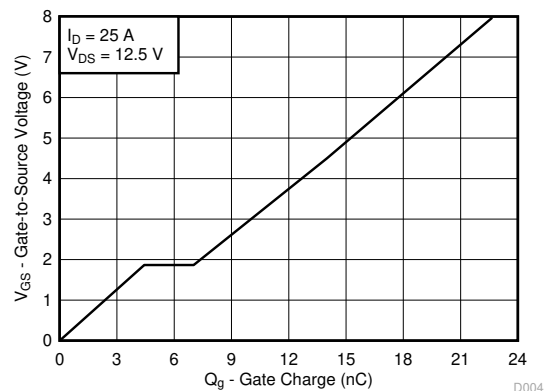
- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

絶対最大定格

$T_A = 25^\circ\text{C}$		値	単位
V_{DS}	ドレイン - ソース間電圧	25	V
V_{GS}	ゲート - ソース間電圧	+10 / -8	V
I_D	連続ドレイン電流 (パッケージ制限)	100	A
	連続ドレイン電流 (シリコン制限)、 $T_C = 25^\circ\text{C}$	177	
	連続ドレイン電流 ⁽¹⁾	29	
I_{DM}	パルス・ドレイン電流 ⁽²⁾	400	A
P_D	消費電力 ⁽¹⁾	3.1	W
	消費電力、 $T_C = 25^\circ\text{C}$	113	
T_J , T_{stg}	動作時の接合部温度、 保存温度	-55~150	$^\circ\text{C}$
E_{AS}	アバランシェ エネルギー、単一パルス $I_D = 66A$, $L = 0.1mH$, $R_G = 25\Omega$	218	mJ

- (1) 厚さ 0.06in の FR4 PCB 上に構築された面積 $1in^2$ 、2 オンスの Cu パッド上で、標準値 $R_{\theta JA} = 40^\circ\text{C/W}$
- (2) 最大 $R_{\theta JC} = 1.1^\circ\text{C/W}$ 、パルス期間 $\leq 100\mu s$ 、デューティ・サイクル $\leq 1\%$



 $R_{DS(on)}$ と V_{GS} との関係

ゲート電荷

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4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC CHARACTERISTICS							
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	25			V	
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 20 V	1			μA	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = +10 / −8 V	100			nA	
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.9	1.1	1.4	V	
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 3 V, I _D = 25 A	2.8			mΩ	
		V _{GS} = 4.5 V, I _D = 25 A	2.1				
		V _{GS} = 8 V, I _D = 25 A	1.9				
g _{fs}	Transconductance	V _{DS} = 12.5 V, I _D = 25 A	150			S	
DYNAMIC CHARACTERISTICS							
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 12.5 V, f = 1 MHz	2360			3100	pF
C _{oss}	Output capacitance		1700			2200	pF
C _{rss}	Reverse transfer capacitance		115			150	pF
R _G	Series gate resistance		1.5			3	Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 12.5 V, I _D = 25 A	14			19	nC
Q _{gd}	Gate charge gate-to-drain		2.5				nC
Q _{gs}	Gate charge gate-to-source		4				nC
Q _{g(th)}	Gate charge at V _{th}		2.1				nC
Q _{oss}	Output charge	V _{DS} = 15 V, V _{GS} = 0 V	36				nC
t _{d(on)}	Turnon delay time	V _{DS} = 12.5 V, V _{GS} = 4.5 V, I _D = 25 A, R _G = 2 Ω	9				ns
t _r	Rise time		15				ns
t _{d(off)}	Turnoff delay time		27				ns
t _f	Fall time		17				ns
DIODE CHARACTERISTICS							
V _{SD}	Diode forward voltage	I _{SD} = 25 A, V _{GS} = 0 V	0.8			1	V
Q _{rr}	Reverse recovery charge	V _{DD} = 13 V, I _F = 25 A, di/dt = 300 A/μs	33				nC
t _{rr}	Reverse recovery time	V _{DD} = 13 V, I _F = 25 A, di/dt = 300 A/μs	32				ns

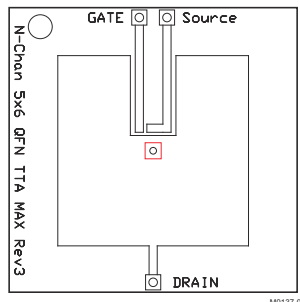
4.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

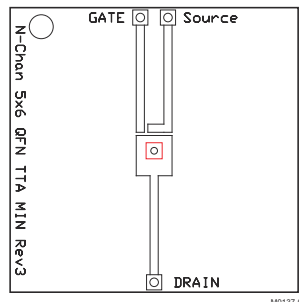
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			1.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ^{(1) (2)}			50	$^\circ\text{C}/\text{W}$

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in², 2-oz Cu pad on a 1.5-in × 1.5-in, 0.06-in thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 Material with 1 in² of 2-oz Cu.



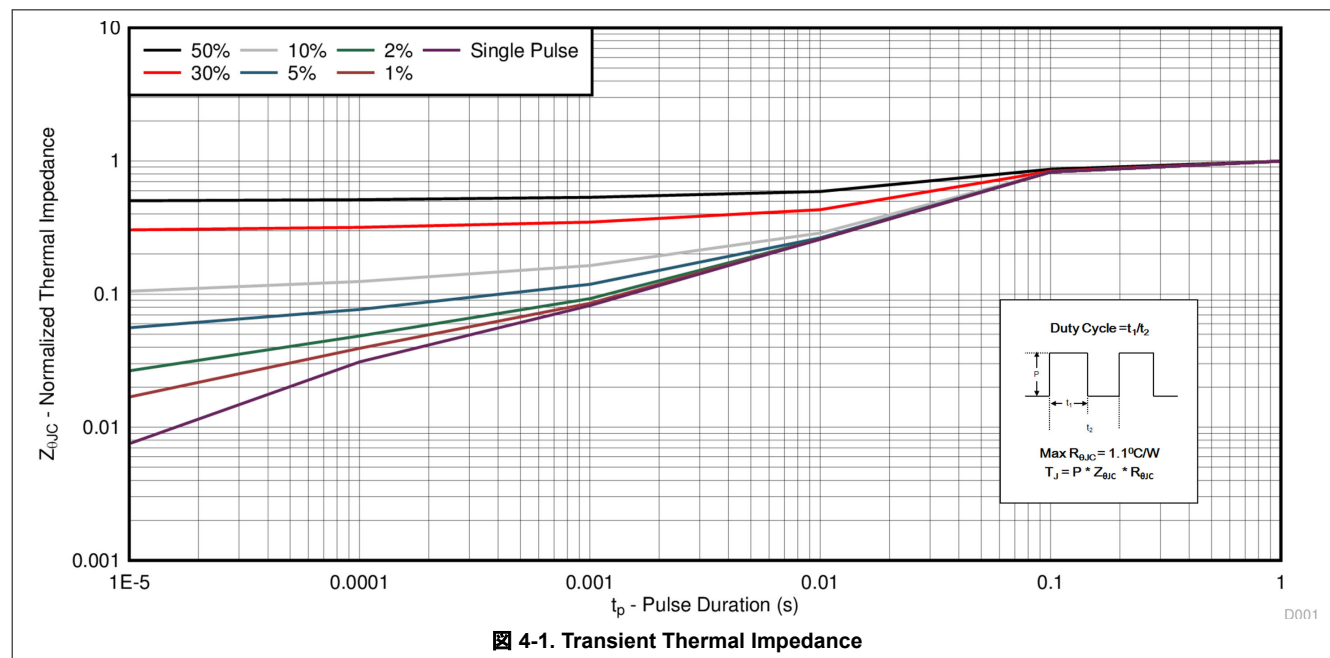
Max $R_{\theta JA} = 50^{\circ}\text{C/W}$ when mounted on 1 in² of 2-oz Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$ when mounted on minimum pad area of 2-oz Cu.

4.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)



4.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

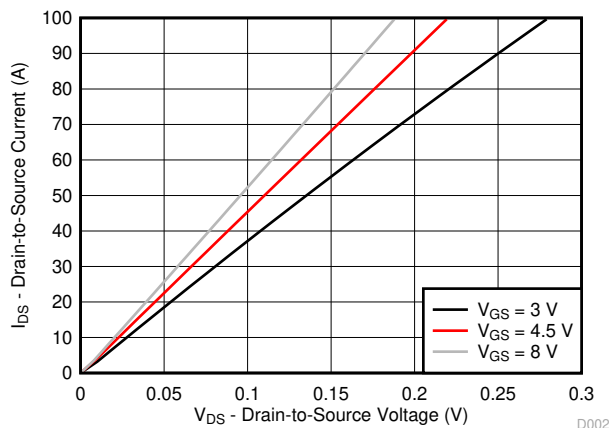


Figure 4-2. Saturation Characteristics

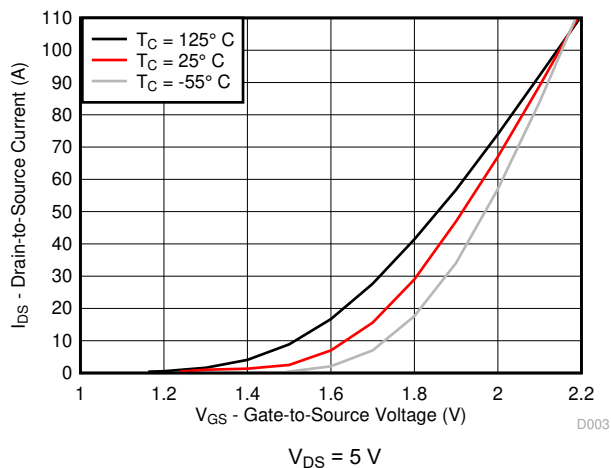


Figure 4-3. Transfer Characteristics

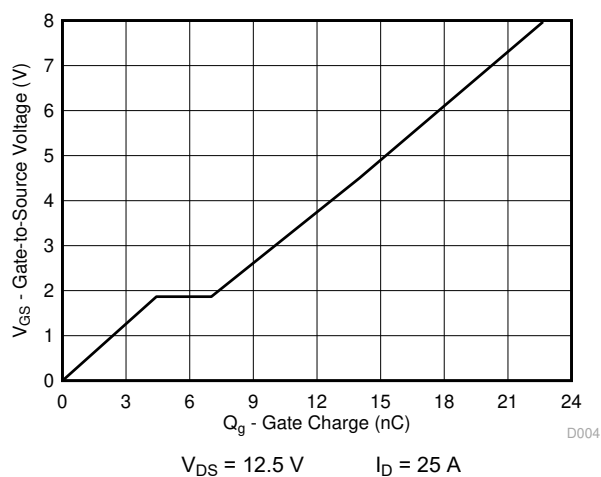


Figure 4-4. Gate Charge

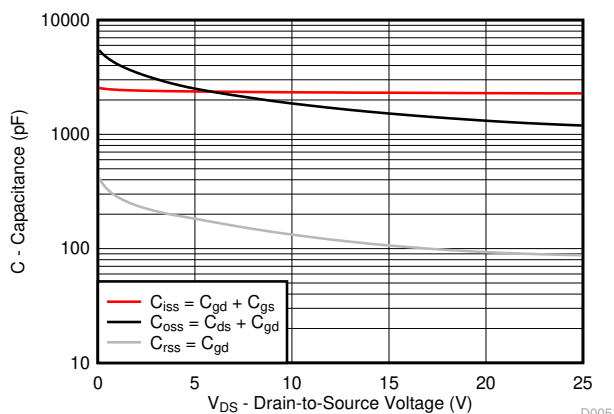


Figure 4-5. Capacitance

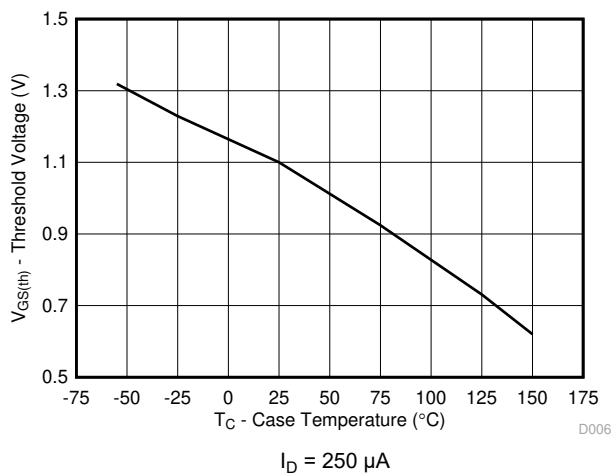


Figure 4-6. Threshold Voltage vs Temperature

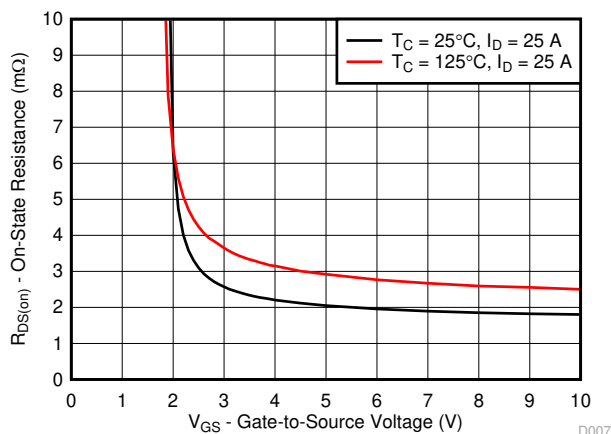


Figure 4-7. On Resistance vs Gate Voltage

4.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

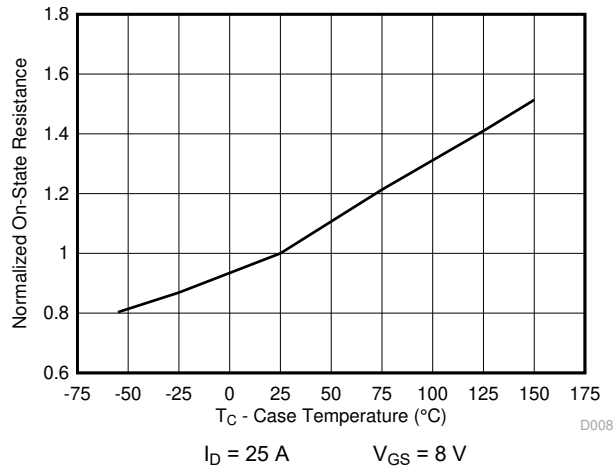


Figure 4-8. On Resistance vs Temperature

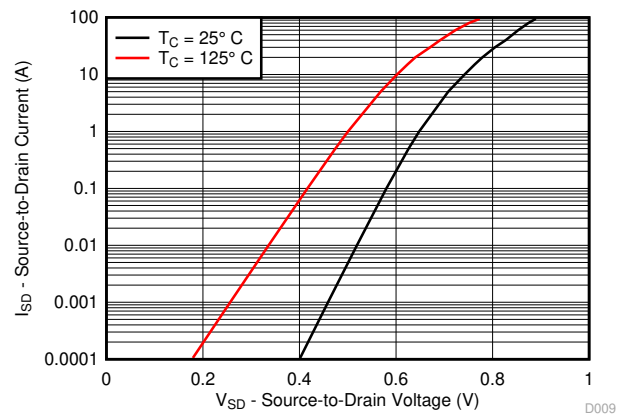


Figure 4-9. Typical Diode Forward Voltage

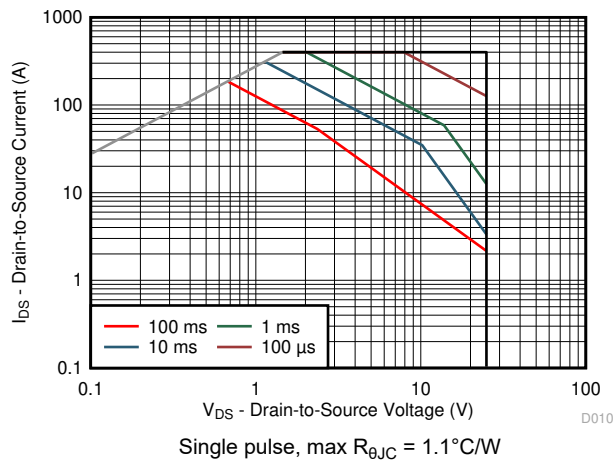


Figure 4-10. Maximum Safe Operating Area

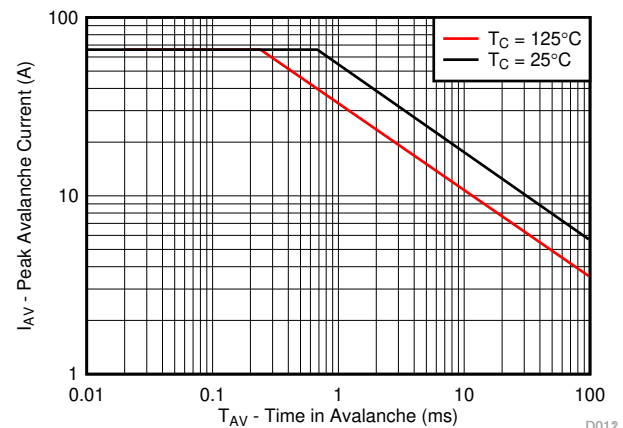


Figure 4-11. Single Pulse Unclamped Inductive Switching

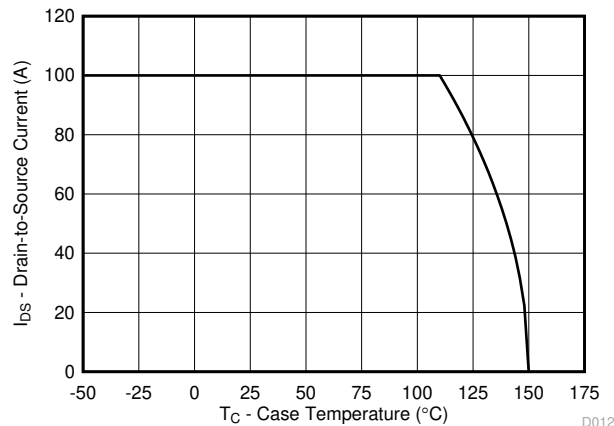


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

5.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

5.3 Trademarks

NexFET™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

5.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

5.5 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

6 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (May 2017) to Revision E (December 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
Changes from Revision C (December 2016) to Revision D (May 2017)	Page
• 3V、4.5V、8V での $R_{DS(on)}$ の値と説明を「電気的特性」の表の値と一致するように変更.....	1
Changes from Revision B (May 2010) to Revision C (December 2016)	Page
• 「概要」の記述を変更	1
• 「絶対最大定格」の表にシリコン制限連続ドレイン電流を追加.....	1
• 「絶対最大定格」の表に $T_C = 25^\circ\text{C}$ での最大消費電力を追加.....	1
• 「絶対最大定格」の表の注 2 を変更.....	1
• Changed $R_{\theta JA}$ max from 48°C/W : to 50°C/W	4
• Changed the SOA in 図 4-10 to reflect measured data.....	5
• Changed MECHANICAL DATA section to Mechanical, Packaging, and Orderable Information section.....	10
Changes from Revision A (January 2010) to Revision B (May 2010)	Page
• Changed $R_{DS(on)} - V_{GS} = 3\text{ V}$, $I_D = 25\text{ A}$ MAX value From: 3.5 To: 3.8.....	4
Changes from Revision * (August 2009) to Revision A (January 2010)	Page
• 上面図のピン配置図のラベルを変更.....	1

• 絶対最大定格 の注 1 を $R_{\theta JA} = 39^{\circ}\text{C/W}$ から $R_{\theta JA} = 39^{\circ}\text{C/W}$ (標準値) に変更.....	1
• Changed 図 4-1 text From: $R_{\theta JA} = 92^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 93^{\circ}\text{C/W}$	5
• Changed 図 4-10 text From: $R_{\theta JA} = 92^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 93^{\circ}\text{C/W}$	5
• Changed 図 4-11 X-axis values.....	5

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Option Addendum

Packaging Information

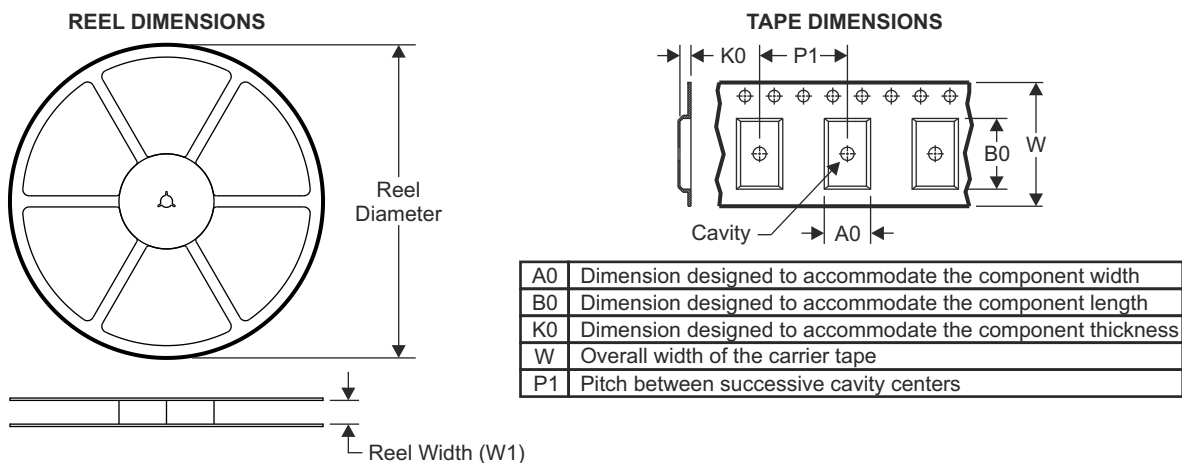
Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
CSD16321Q5	ACTIVE ⁽¹⁾	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

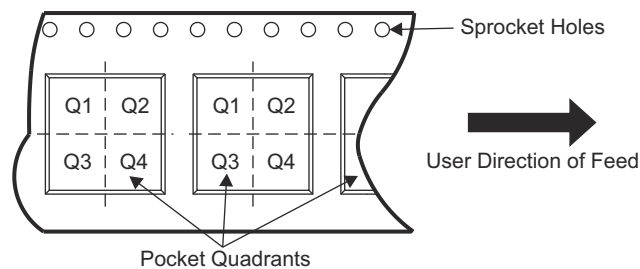
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

7.2 Tape and Reel Information

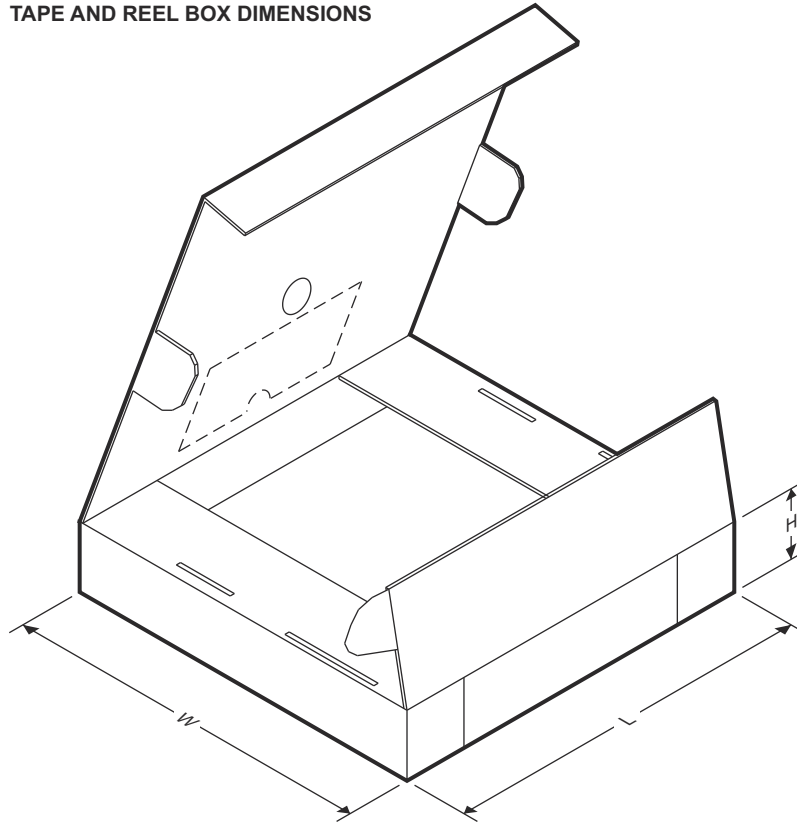


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

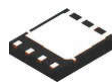


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16321Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16321Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

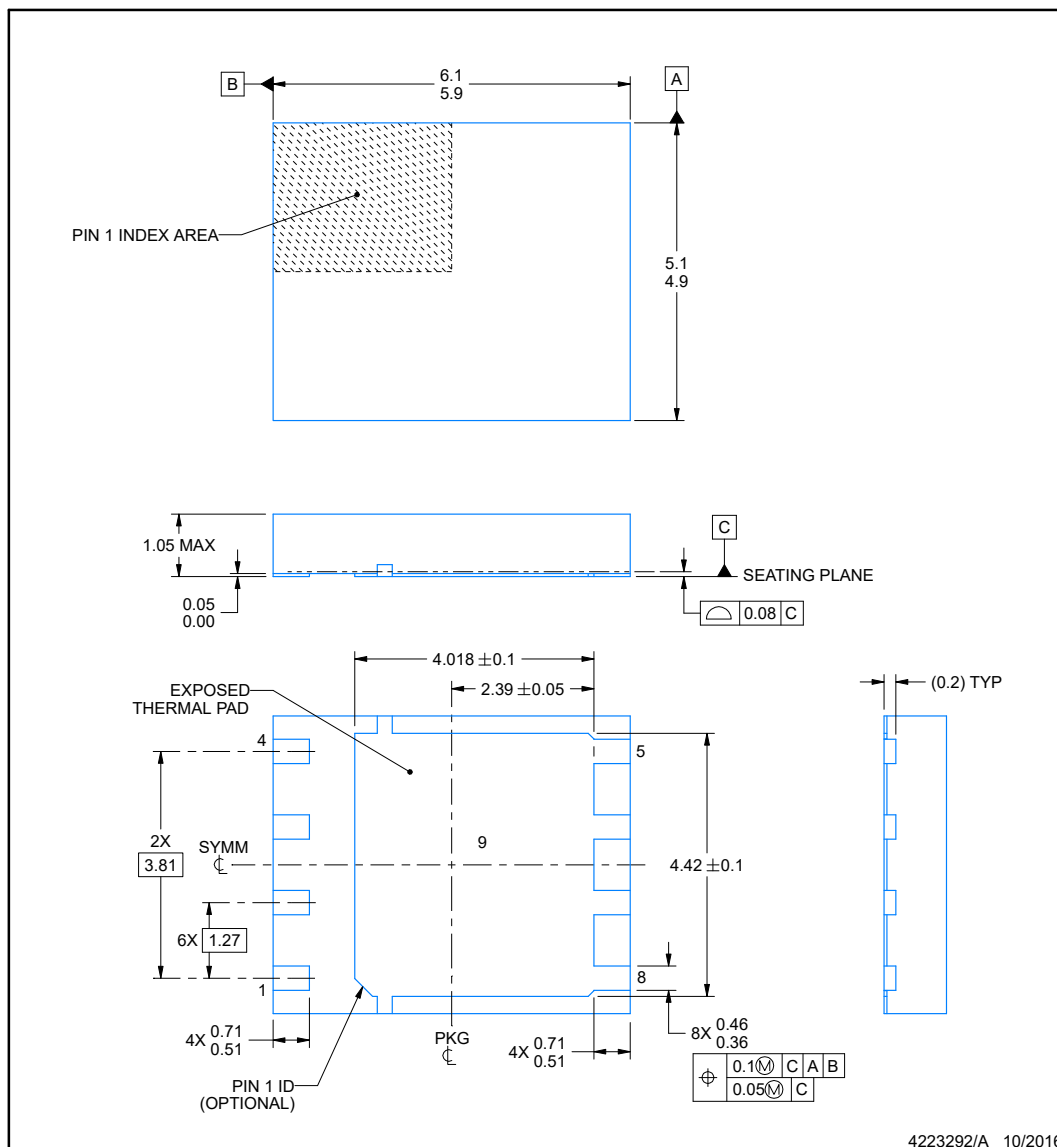


PACKAGE OUTLINE

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

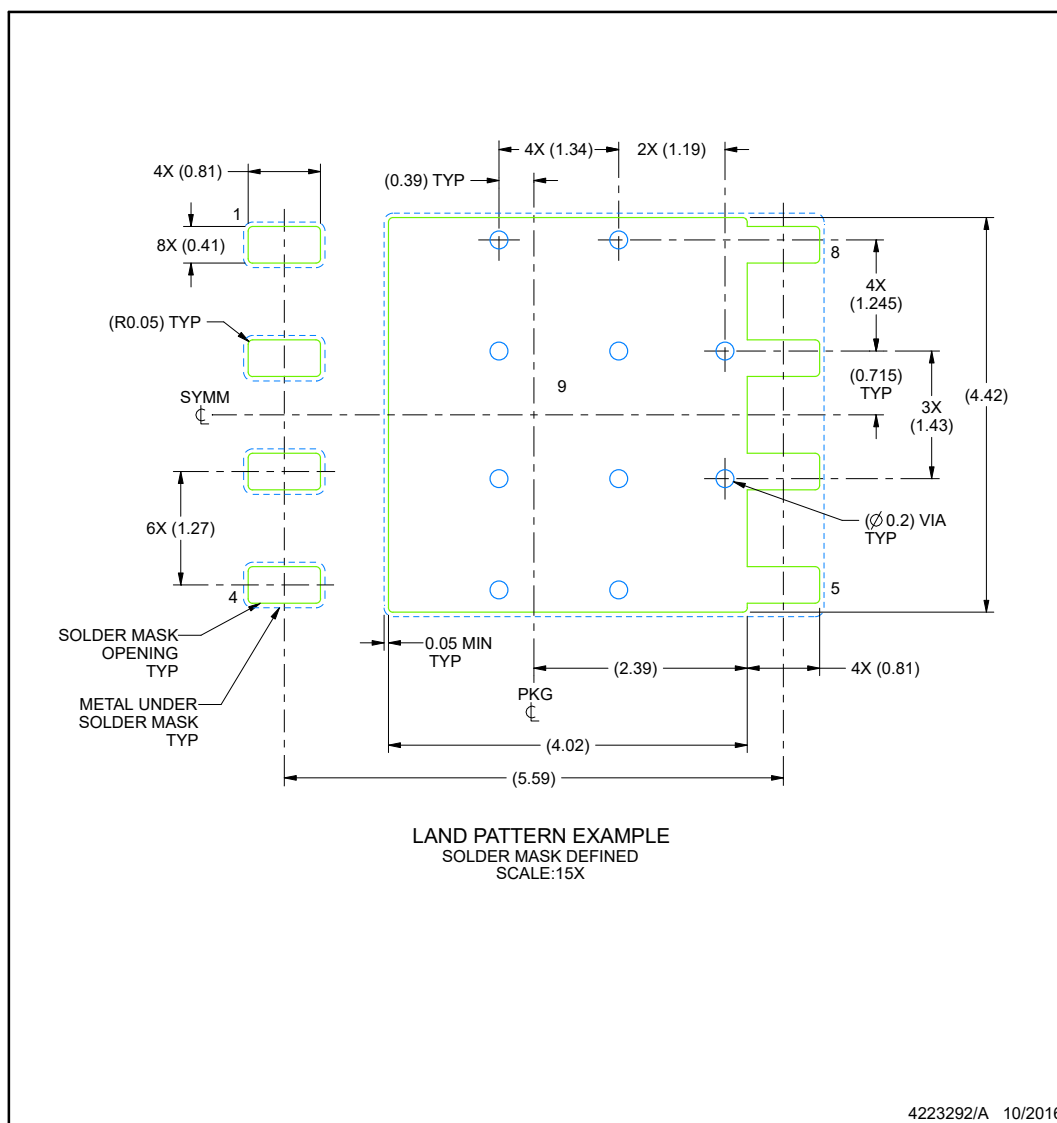
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

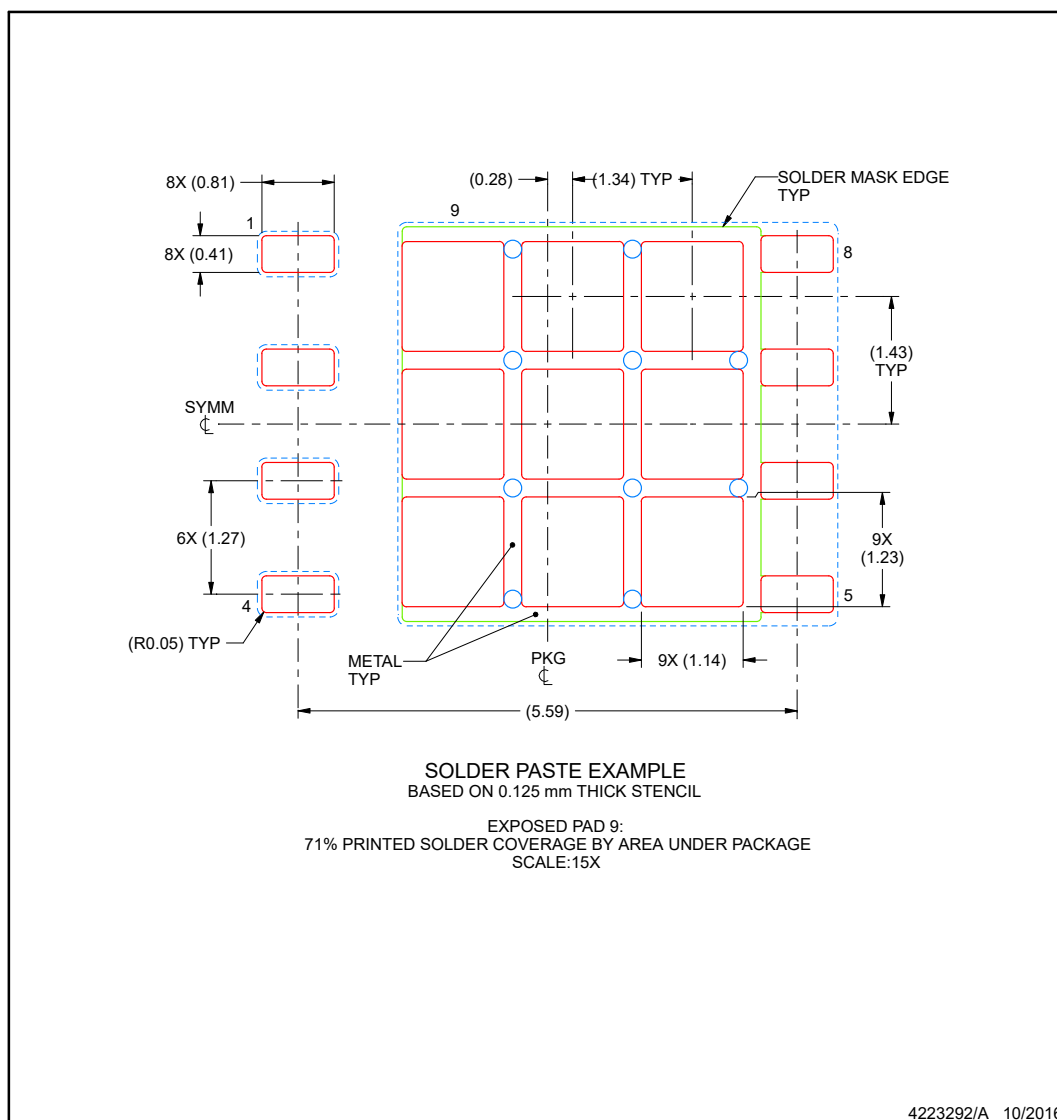


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN**DQH0008A****VSON-CLIP - 1.05 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16321Q5	Active	Production	VSON-CLIP (DQH) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5.B	Active	Production	VSON-CLIP (DQH) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5T	Active	Production	VSON-CLIP (DQH) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5T.B	Active	Production	VSON-CLIP (DQH) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16321Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16321Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0



VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

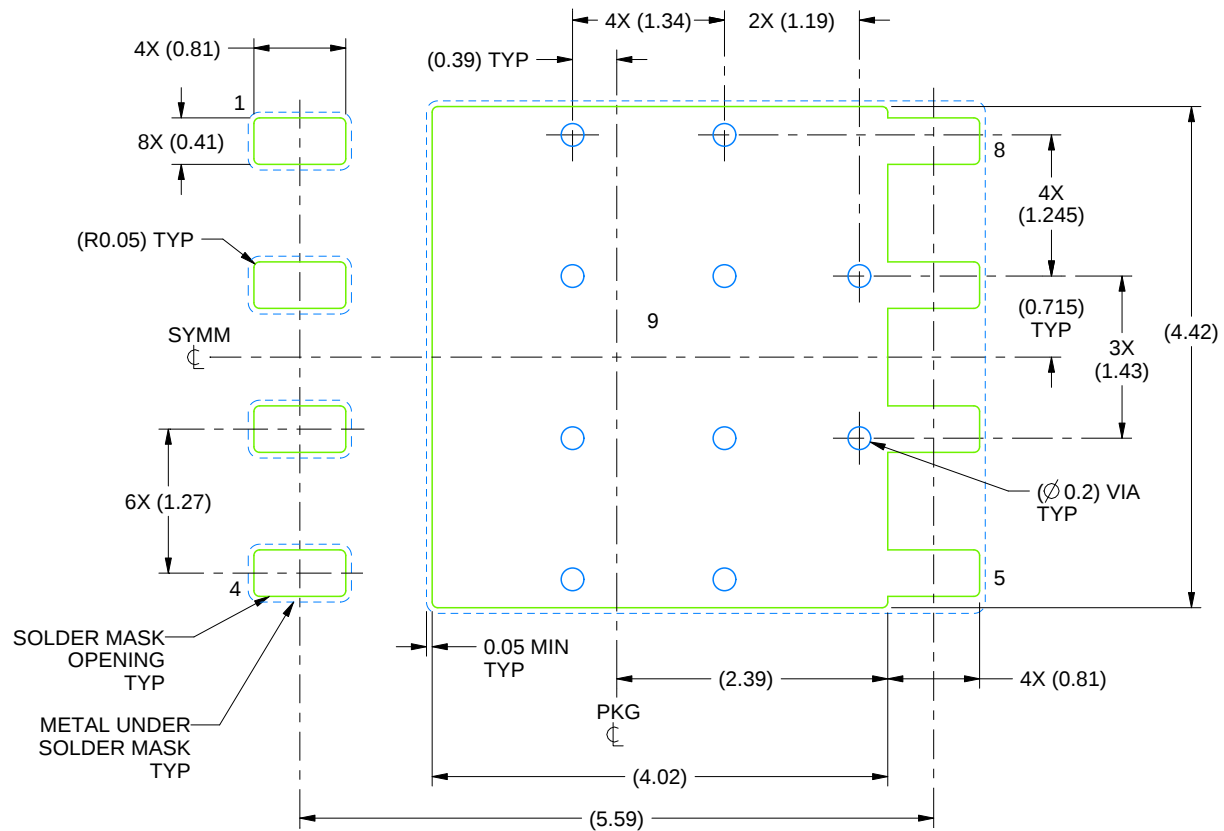


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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NOTES: (continued)

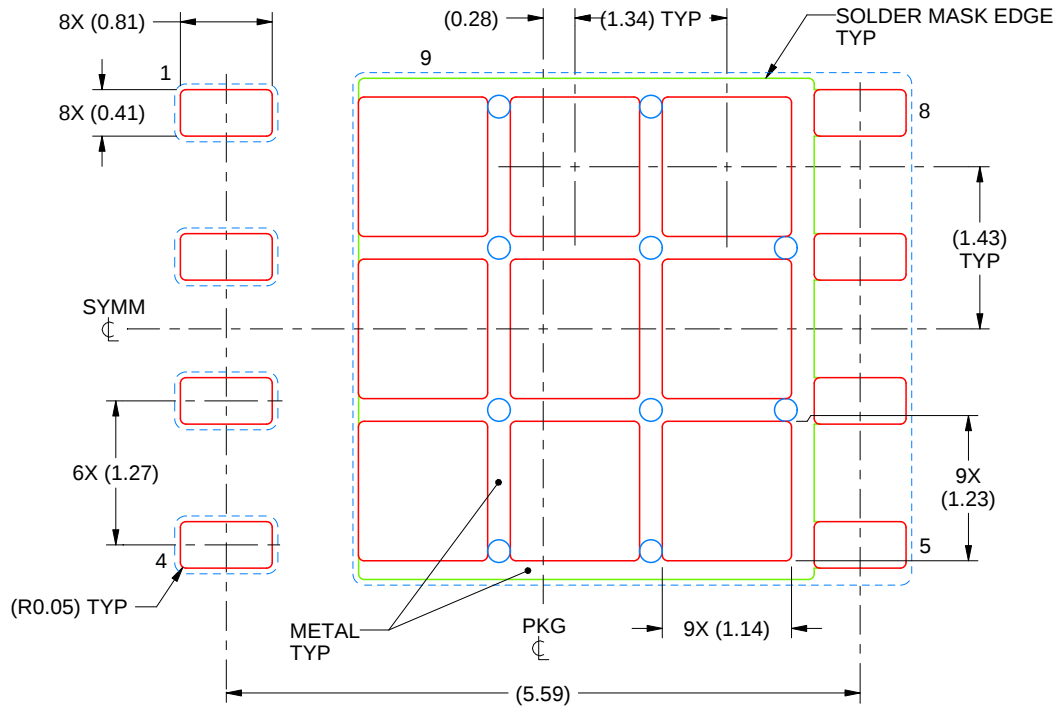
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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