Ten-Output Low-Jitter Low-Power Clock Buffer and Level Translator

Check for Samples: CDCLVC1310

FEATURES

- **High-Performance Crystal Buffer With Ultralow Noise Floor of –169 dBc/Hz**
- **Additive Phase Noise/Jitter Performance Is 25 fs_{RMS} (Typ.)**
- **Level Translation With 3.3-V or 2.5-V Core and 3.3-V, 2.5-V, 1.8-V, or 1.5-V Output Supply**
- **Device inputs consist of primary, secondary, and crystal inputs, and manually selectable (through pins) using the input MUX. The primary and secondary inputs can accept LVPECL, LVDS, HCSL, SSTL or LVCMOS signals and crystal input.**
  - **Crystal Frequencies Supported Are From 8 MHz to 50 MHz**
  - **Differential and Single-Ended Input Frequencies Supported Are up to 200 MHz**
- **10 Single-Ended LVCMOS Outputs. The outputs can operate at 1.5-V, 1.8-V, 2.5-V or 3.3-V Power-Supply Voltage.**
  - **LVCMOS Outputs Operate up to 200 MHz**
  - **Output Skew Is 30 ps (Typical)**
  - **Total Propagation Delay Is 2 ns (Typical)**
  - **Synchronous and Glitch-Free Output Enable Is Available**
- **Offered in QFN-32 5-mm × 5-mm Package With Industrial Temperature Range of –40°C to 85°C**
- **Can Overdrive Crystal Input With LVCMOS Signal up to 50 MHz**

APPLICATIONS

- **Wireless and Wired Infrastructure**
- **Networking and Data Communications**
- **Medical Imaging**
- **Portable Test and Measurement**
- **High-End A/V**

DESCRIPTION

The CDCLVC1310 is a highly versatile, low-jitter, low-power clock fanout buffer which can distribute to ten low-jitter LVCMOS clock outputs from one of three inputs, whose primary and secondary inputs can feature differential or single-ended signals and crystal input. Such a buffer is good for use in a variety of mobile and wired infrastructure, data communication, computing, low-power medical imaging, and portable test and measurement applications. When the input is an illegal level, the output is at a defined state. One can set the core to 2.5 V or 3.3 V, and output to 1.5 V, 1.8 V, 2.5 V or 3.3 V. Pin programming easily configures the CDCLVC1310. The overall additive jitter performance is 25 fs_{RMS} (typical). The CDCLVC1310 comes in a small 32-pin 5-mm × 5-mm QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

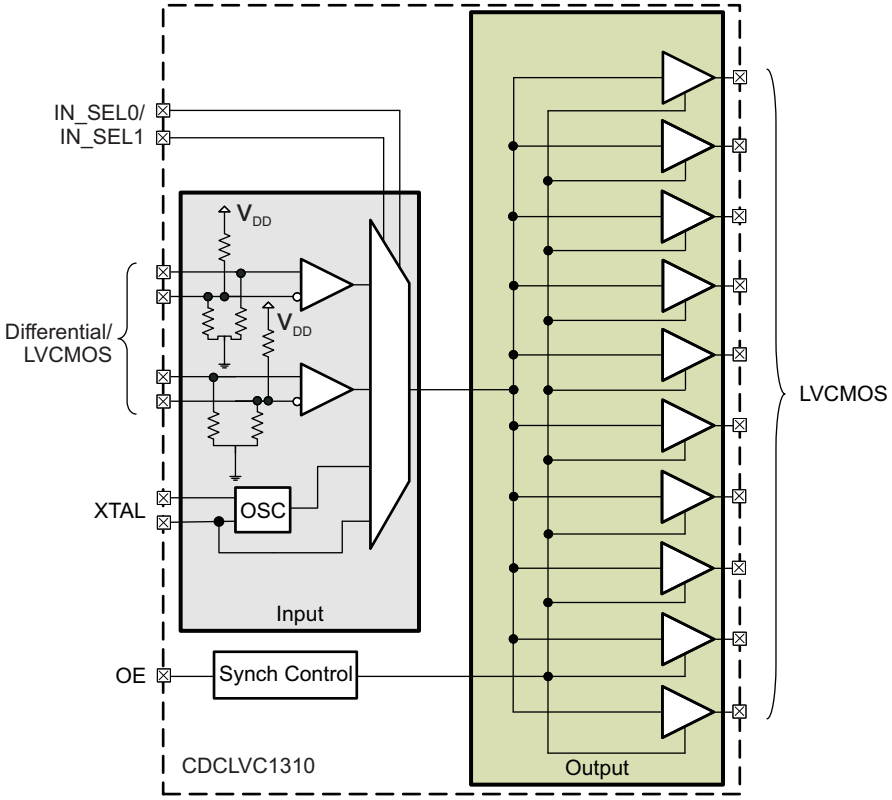
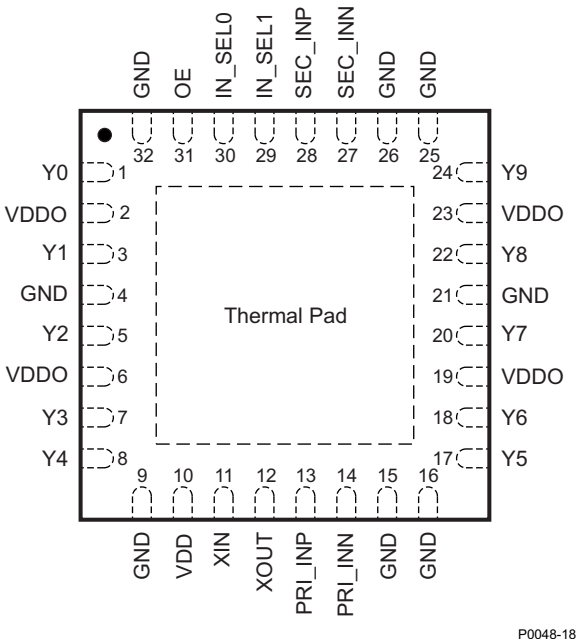


Figure 1. High-Level Block Diagram of CDCLVC1310

PINOUT DIAGRAM

CDCLVC1310
RHB-32 Package
(Top View)



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PIN FUNCTIONS

PIN		I/O	TYPE	DESCRIPTION
NAME	NO(s)			
GND	4, 9, 15, 16, 21, 25, 26, 32	PWR	Analog	Power-supply ground
IN_SEL0, IN_SEL1	30, 29	I	Digital	Input-clock selection (pulldown of 150 kΩ)
OE	31	I	Digital	LVCMOS output enable (pulldown of 150 kΩ)
PRI_INN	14	I	Analog	Inverting differential primary reference input, internally biased to Vdd / 2 (pullup or pulldown of 150 kΩ)
PRI_INP	13	I	Analog	Non-inverting differential or single-ended primary reference input (pulldown of 150 kΩ)
SEC_INN	27	I	Analog	Inverting differential secondary reference input, internally biased to Vdd / 2 (pullup or pulldown of 150 kΩ)
SEC_INP	28	I	Analog	Non-inverting differential or single-ended secondary reference input (pulldown of 150 kΩ)
VDD	10	PWR	Analog	Power-supply pins
VDDO	2, 6, 19, 23	PWR	Analog	I/O power-supply pins
XIN	11	I	Analog	Crystal-oscillator input or XTAL bypass mode
XOUT	12	I	Analog	Crystal-oscillator output
Y0	1	O	Analog	LVCMOS output 0
Y1	3	O	Analog	LVCMOS output 1
Y2	5	O	Analog	LVCMOS output 2
Y3	7	O	Analog	LVCMOS output 3
Y4	8	O	Analog	LVCMOS output 4
Y5	17	O	Analog	LVCMOS output 5
Y6	18	O	Analog	LVCMOS output 6
Y7	20	O	Analog	LVCMOS output 7
Y8	22	O	Analog	LVCMOS output 8
Y9	24	O	Analog	LVCMOS output 9

Table 1. Input Selection

IN_SEL1	IN_SEL0	INPUT CHOSEN
0	0	PRI_IN
0	1	SEC_IN
1	0	XTAL or overdrive (1)
1	1	XTAL bypass (2)

(1) This mode is for XTAL input or overdrive of XTAL oscillator with LVCMOS input. For characteristics; see LVCMOS OUTPUT CHARACTERISTICS.
(2) This mode is only XTAL bypass. For characteristics, see LVCMOS OUTPUT CHARACTERISTICS.

Table 2. INPUT/OUTPUT OPERATION (1)

INPUT STATE	OUTPUT STATE
PRI_INx, SEC_INx open	Logic LOW
PRI_INP, SEC_INP = HIGH, PRI_INN, SEC_INN = LOW	Logic HIGH
PRI_INP, SEC_INP = LOW, PRI_INN, SEC_INN = HIGH	Logic LOW

(1) Device must have switching edge to obtain output states.

Table 3. OE Function

OE	Yx
0	High-impedance
1	Enabled

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDD, VDDO	Supply-voltage range	–0.5 to 4.6	V
V_{IN}	Input-voltage range	–0.5 to VDD + 0.5	V
V_{OUT}	Output-voltage range	–0.5 to VDDO + 0.5	V
I_{IN}	Input current	±20	V
I_{OUT}	Output current	±50	V
T_{stg}	Storage-temperature range	–65 to 150	°C
T_J	Junction temperature	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDO	Output supply voltage	3.135	3.3	3.465	V
		2.375	2.5	2.625	
		1.6	1.8	2	
		1.35	1.5	1.65	
VDD	Core supply voltage	3.135	3.3	3.465	V
		2.375	2.5	2.625	
I_{OH}	High-level output current, LVCMOS			–24	mA
I_{OL}	Low-level output current, LVCMOS			24	mA
T_A	Ambient temperature	–40		85	°C

THERMAL INFORMATION

THERMAL METRIC(1)		CDCLVC1310 RHB 32 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	41.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	34.1	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	14.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

INPUT CHARACTERISTICS

over recommended ranges of supply voltage (VDDO ≤ VDD), load and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristic (OE, IN_SEL0, IN_SEL1, PRI_IN, SEC_IN)						
I_{IH}	Input high current	VDD = 3.465 V, V_{IH} = 3.465 V			40	µA
I_{IL}	Input low current	VDD = 3.465 V, V_{IL}= 0 V			–40	µA
ΔV/ΔT	Input edge rate	20%–80%		2		V/ns
$R_{Pullup/down}$	Pullup or pulldown resistance			150		kΩ
C_{IN}	Input capacitance			2		pF
Single-Ended DC Characteristic (PRI_INP, SEC_INP)(1)						
V_{IH}	Input high voltage	VDD = 3.3 V ±5%	2		VDD + 0.3	V
		VDD = 2.5 V ±5%	1.6		VDD + 0.3	
V_{IL}	Input low voltage	VDD = 3.3 V ±5%	–0.3		1.3	V
		VDD = 2.5 V ±5%	–0.3		0.9	
Single-Ended DC Characteristic (OE, IN_SEL0, IN_SEL1)						
V_{IH}	Input high voltage		0.7 × VDD			V
V_{IL}	Input low voltage				0.3 × VDD	V
Differential DC Characteristic (PRI_IN, SEC_IN)						
$V_{I,DIFF}$	Differential input voltage swing(2)		0.15		1.3	V
V_{ICM}	Input common-mode voltage(3)		0.5		VDD – 0.85	V
AC Characteristic (PRI_IN, SEC_IN)						
f_{IN}	Input frequency		DC		200	MHz
idc	Input duty cycle		40%		60%	

(1) PRI/SEC_INN biased to VDD / 2
(2) V_{IL} should not be less than –0.3 V
(3) Input common-mode voltage is defined as V_{IH} (see Figure 19).

CRYSTAL CHARACTERISTICS

over recommended ranges of supply voltage, load and ambient temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Equivalent series resistance (ESR)			50		Ω
Maximum shunt capacitance			7		pF
Drive level			100		µW

CRYSTAL OSCILLATOR CHARACTERISTICS

over recommended ranges of supply voltage, load and ambient temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mode of oscillation			Fundamental		
Frequency		8		50	MHz
Frequency in overdrive mode(1)				50	MHz
Frequency in bypass mode(2)				50	MHz
On-chip load capacitance			12		pF

(1) Input signal swing (max) = 2 V; input signal t_r (max) = 10 ns; t_f(max) = 10 ns; functional, but device may not meed ac parameters.
(2) Input signal swing (max) = V_{DD}; input signal t_r (max) = 10 ns; t_f(max) = 10 ns; functional, but device may not meed ac parameters.

LVCMOS OUTPUT CHARACTERISTICS

over recommended ranges of supply voltage (VDDO ≤ VDD), load (50 Ω to VDDO/2), and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}					200	MHz
V_{OH}	Output high voltage	VDDO = 3.135 V to 3.465 V	0.8 * VDDO			V
		VDDO = 2.375 V to 2.625 V	0.8 * VDDO			
		VDDO = 1.6 V to 2 V	0.7 * VDDO			
		VDDO = 1.35 V to 1.65 V	0.7 * VDDO			
V_{OL}	Output low voltage	VDDO = 3.135 V to 3.465 V			0.2 * VDDO	V
		VDDO = 2.375 V to 2.625 V			0.2 * VDDO	
		VDDO = 1.6 V to 2 V			0.3 * VDDO	
		VDDO = 1.35 V to 1.65 V			0.3 * VDDO	
R_{OUT}	Output impedance	VDDO = 3.3 V		15		Ω
		VDDO = 2.5 V		20		
		VDDO = 1.8 V		25		
		VDDO = 1.5 V		30		
$t_{SLEW-RATE}$	Output slew rate, rising and falling	VDDO=3.3V +/- 5%, 20% to 80%	5.6	7.3	9.0	V/ns
		VDDO=2.5V +/- 5%, 20% to 80%	3.9	4.8	5.4	
		VDDO=1.8V +/- 200mV, 20% to 80%	1.6	2.1	2.5	
		VDDO=1.5V +/- 150mV, 20% to 80%	0.9	1.2	1.4	
t_{SK}	Output skew			30	50	ps
$t_{SK,PP}$	Part-to-part skew(1)				2	ns

(1) Calculation for part-to-part skew is the difference between the fastest and the slowest t_{pd} across multiple devices.

LVCMOS OUTPUT CHARACTERISTICS (continued)

over recommended ranges of supply voltage (VDDO ≤ VDD), load (50 Ω to VDDO/2), and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DELAY}	Output frequency	VDD = 3.3 V ±5%, VDDO = 1.35 V to VDD	1.5	1.95	4.0	ns
		VDD = 2.5 V ±5%, VDDO = 1.35 V to VDD	1.8	2.4	4.4	
t_{RJIT}	System-level additive jitter(2)	Single-ended input, VDD = 3.3 V, VDDO = 3.3 V		25		f_S, RMS
		Single-ended input, VDD = 2.5 V or 3.3 V, VDDO = 1.5 V, 1.8 V, or 2.5 V, $f_{IN/OUT}$ = 125 MHz		30		
		Differential input, VDD = 3.3 V, VDDO = 3.3 V		30		
		Differential input, VDD = 2.5 V or 3.3 V, VDDO = 1.5 V, 1.8 V, or 2.5 V, $f_{IN/OUT}$ = 125 MHz		30		
NF	Noise floor	10-kHz offset(3)		–145		dBc/Hz
		100-kHz offset(3)		–156		
		1-MHz offset(3)		–163		
		10-MHz offset(3)		–164		
		20-MHz offset(3)		–164		
		10-kHz offset(4)		–145		
		100-kHz offset(4)		–155		
		1-MHz offset(4)		–160		
		10-MHz offset(4)		–161		
		20-MHz offset(4)		–162		
odc	Output duty cycle	$f_{IN/OUT}$ = 125 MHz, idc = 50%(5)	45%		55%	
t_{EN}	Output enable or disable time				2	Cycle
$MUX_{ISOLATION}$	MUX isolation(6)	125 MHz	55			dB

(2) Integration range: 12 kHz–20 MHz; input source see the *System-Level Additive-Jitter Measurement* section
(3) Single-ended input, $f_{IN/OUT}$ = 125 MHz, VDD = VDDO = 3.3 V
(4) Differential input, $f_{IN/OUT}$ = 125 MHz, VDD = VDDO = 3.3 V
(5) Stable V_{IH}, V_{IL}, and V_{CM}
(6) See Figure 18.

PHASE NOISE WITH XTAL[1] SELECTED

VDD = VDDO = 2.5 V or 3.3 V, f_{XTAL} = 25 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Jrms	RMS phase jitter	IB = 12 kHz to 5 MHz, VDD = VDDO = 3.3 V		80		fs rms
		IB = 12 kHz to 5 MHz, VDD = VDDO = 2.5 V		115		
PN	Phase noise (see Figure 15)	f_{offset} = 100 Hz, VDD = VDDO = 3.3 V		–92		dBc/Hz
		f_{offset} = 1 kHz, VDD = VDDO = 3.3 V		–137		
		f_{offset} = 10 kHz, VDD = VDDO = 3.3 V		–163		
		f_{offset} = 100 kHz, VDD = VDDO = 3.3 V		–168		
		f_{offset} = 1 MHz, VDD = VDDO = 3.3 V		–168		
		f_{offset} = 5 MHz, VDD = VDDO = 3.3 V		–169		
		f_{offset} = 100 Hz, VDD = VDDO = 2.5 V		–91		
		f_{offset} = 1 kHz, VDD = VDDO = 2.5 V		–136		
		f_{offset} = 10 kHz, VDD = VDDO = 2.5 V		–159		
		f_{offset} = 100 kHz, VDD = VDDO = 2.5 V		–164		
		f_{offset} = 1 MHz, VDD = VDDO = 2.5 V		–165		
		f_{offset} = 5 MHz, VDD = VDDO = 2.5 V		–165		

(1) Crystal specification: C_L = 18 pF; ESR = 35 Ω (max); C_0 = 7 pF; drive level = 100 µW (max)

DEVICE CURRENT CONSUMPTION

over recommended ranges of supply voltage, load and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL PARAMETERS FOR ALL VERSIONS						
I_{DD}	Static device current[1]	OE = 0 V or V_{DD}; Ref. input (PRI/SEC) = 0 V or V_{DD}; I_O = 0 mA; V_{DD} / V_{DDO} = 3.3 V		14		mA
		OE = 0 V or V_{DD}; Ref. input (PRI/SEC) = 0 V or V_{DD}; I_O = 0 mA; V_{DD} / V_{DDO} = 2.5 V		8		
$I_{DD,XTAL}$	Device current with XTAL input[1]			20		mA
C_{PD}	Power dissipation capacitance per output[2]	VDDO = 3.465 V; f = 100 MHz			8.8	pF
		VDDO = 2.625 V; f = 100 MHz			7.7	
		VDDO = 2 V; f = 100 MHz			7.3	
		VDDO = 1.65 V; f = 100 MHz			6.9	

(1) I_{DD} and $I_{DD,XTAL}$ is the current through V_{DD}; outputs enabled or in the high-impedance state; no load.
(2) This is the formula for the power dissipation calculation (see the *Power Considerations* section)
$I_{DD,Total} = I_{DD} + I_{DD,Cload} + I_{DD,dyn}$ [mA]
$I_{DD,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA]
$I_{DD,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA]
n = Number of switching output pins

TEST CONFIGURATIONS

Figure 2 through Figure 8 illustrate how to set up the device for a variety of test configurations.

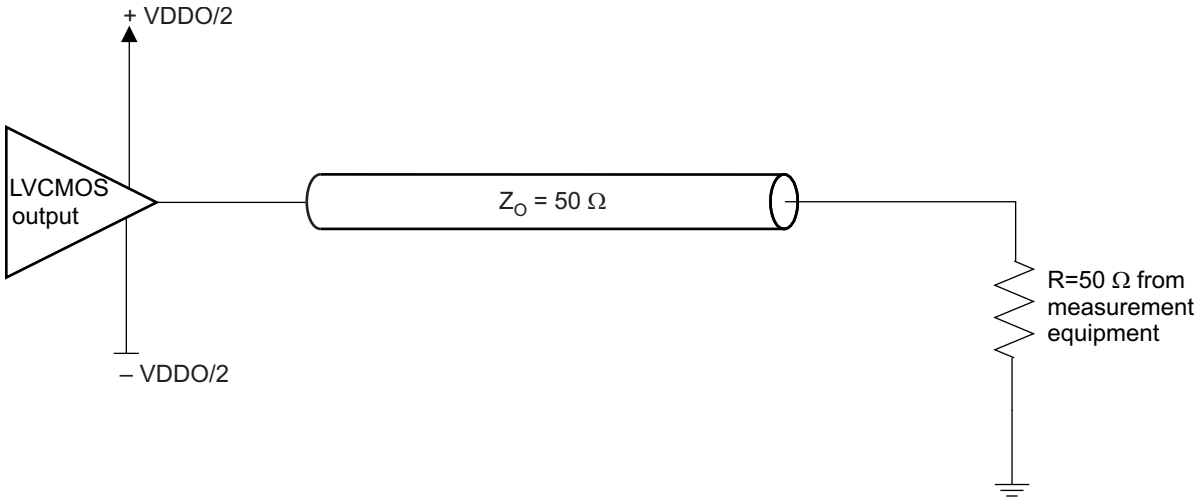


Figure 2. LVCMOS Output DC Configuration; Test Load Circuit

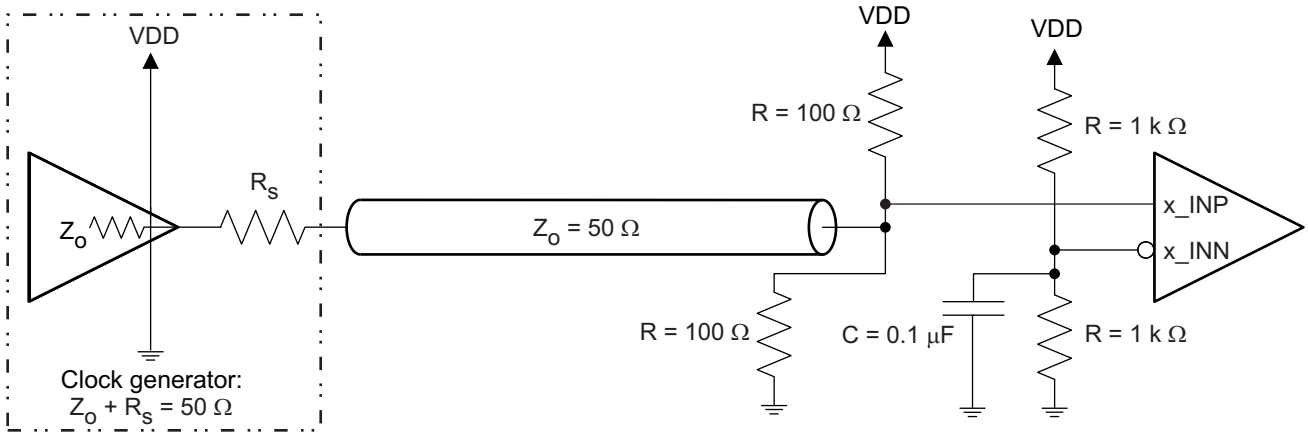


Figure 3. LVCMOS Input DC Configuration During Device Test

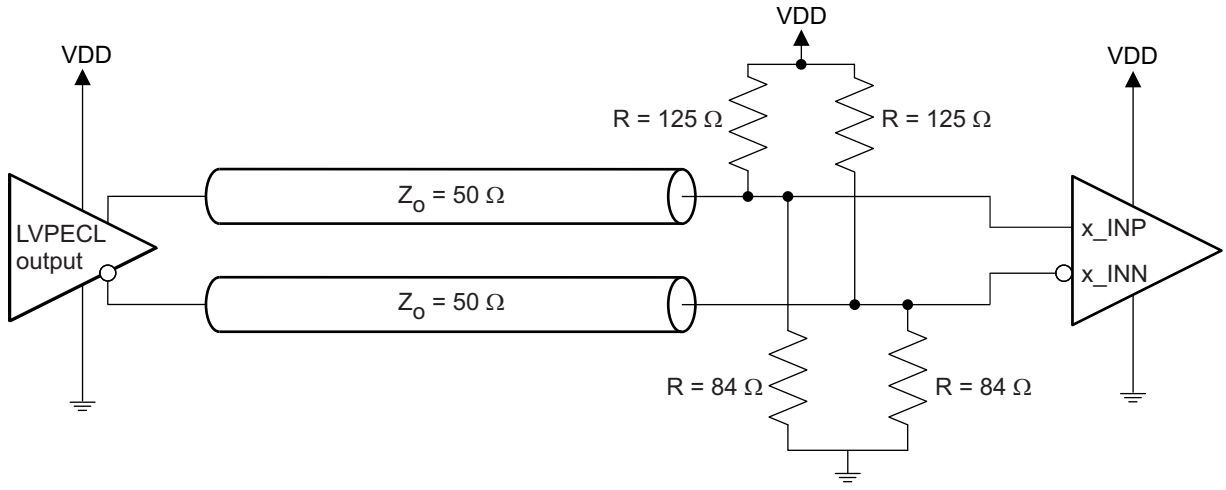


Figure 4. LVPECL Input Configuration During Device Test

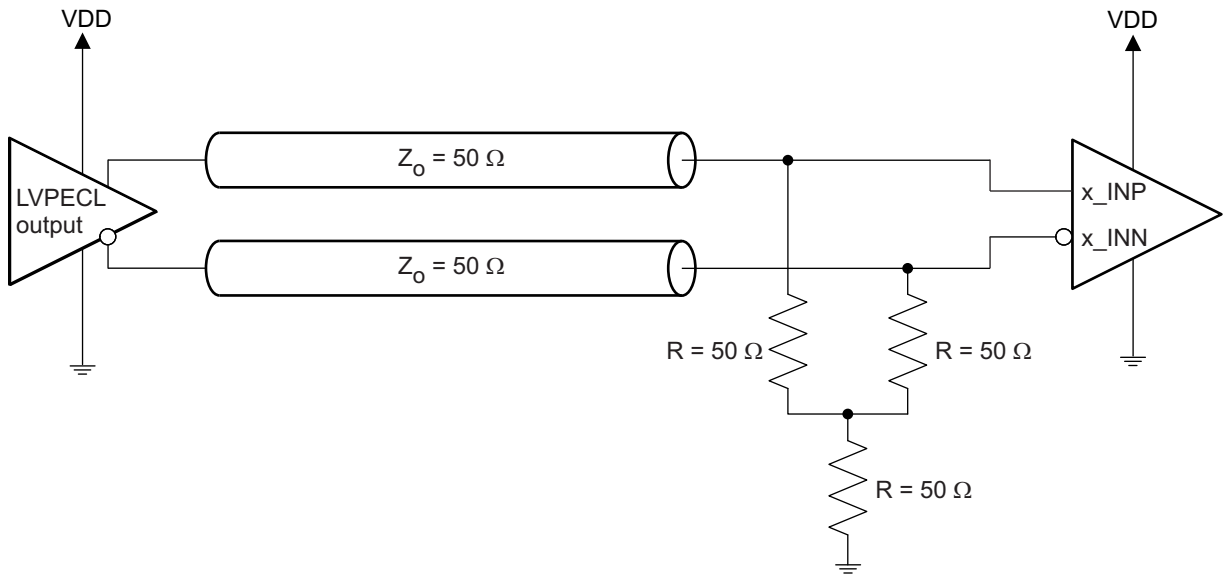


Figure 5. LVPECL Input Configuration During Device Test

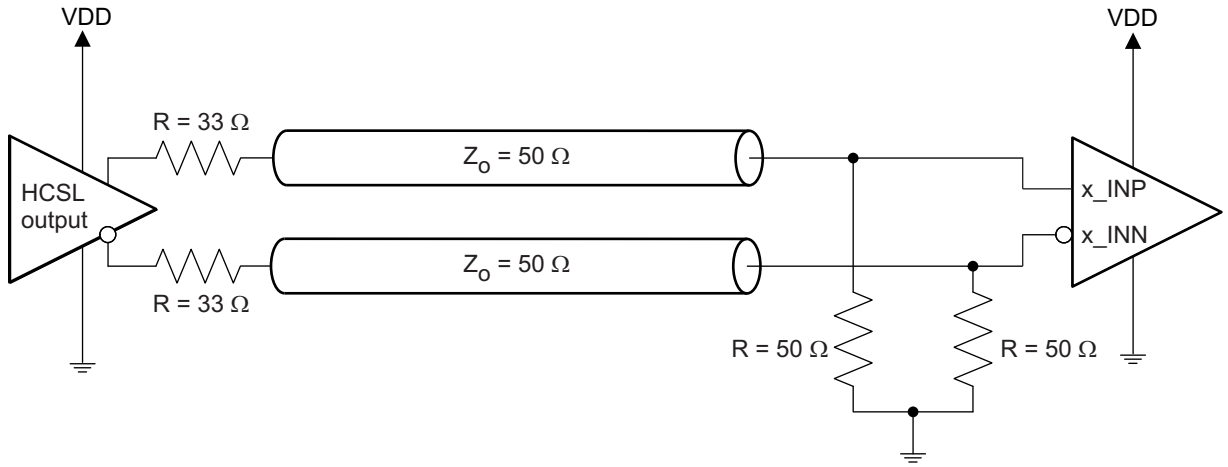


Figure 6. HCSL Input Configuration During Device Test

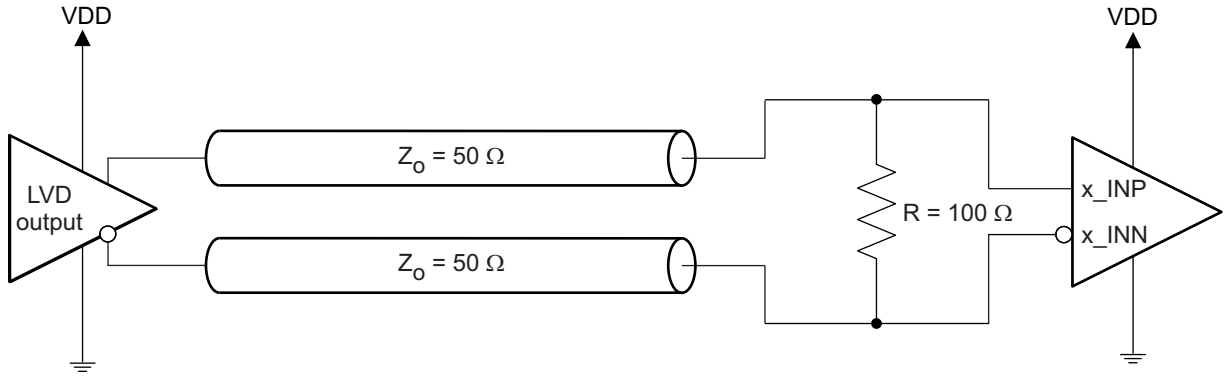


Figure 7. LVDS Input Configuration During Device Test

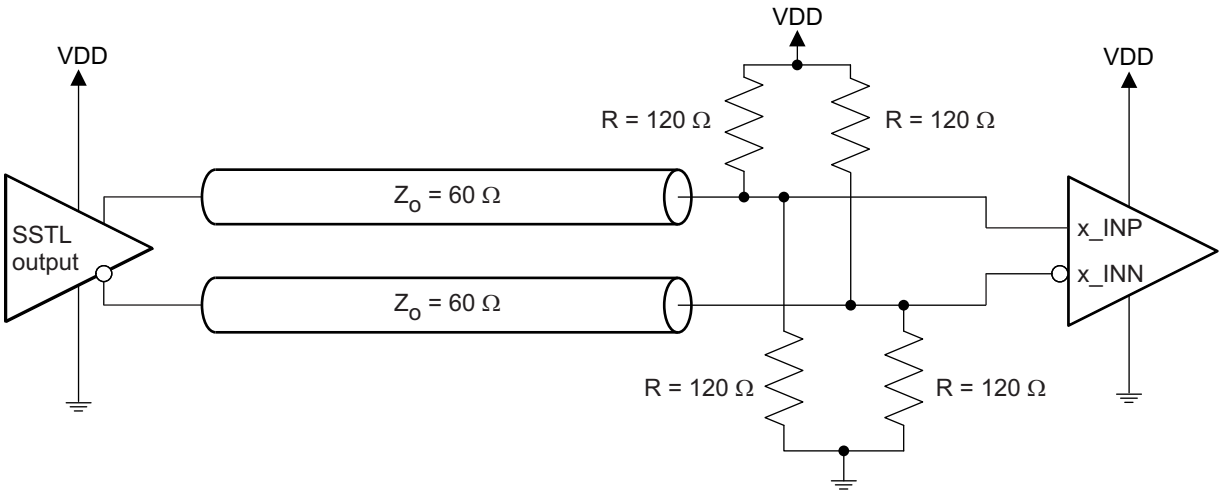


Figure 8. SSTL Input Configuration During Device Test

APPLICATION INFORMATION

Typical Application Load

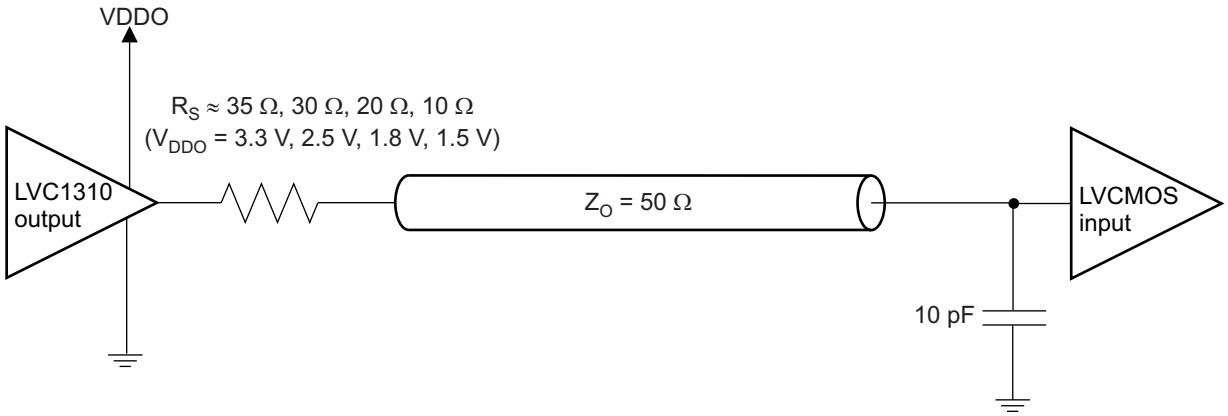


Figure 9. LVCMOS Output DC Configuration: Typical Application Load

Parameter Measurement Information

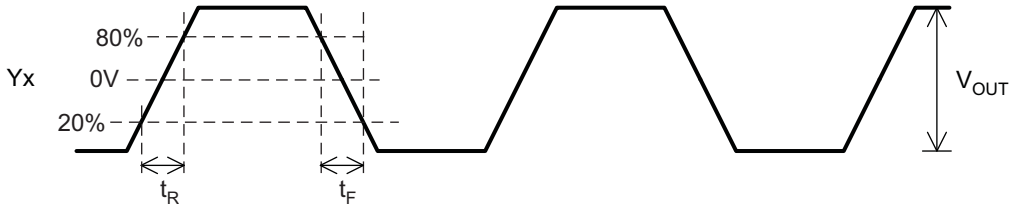


Figure 10. LVCMOS Output Voltage, and Rise and Fall Times

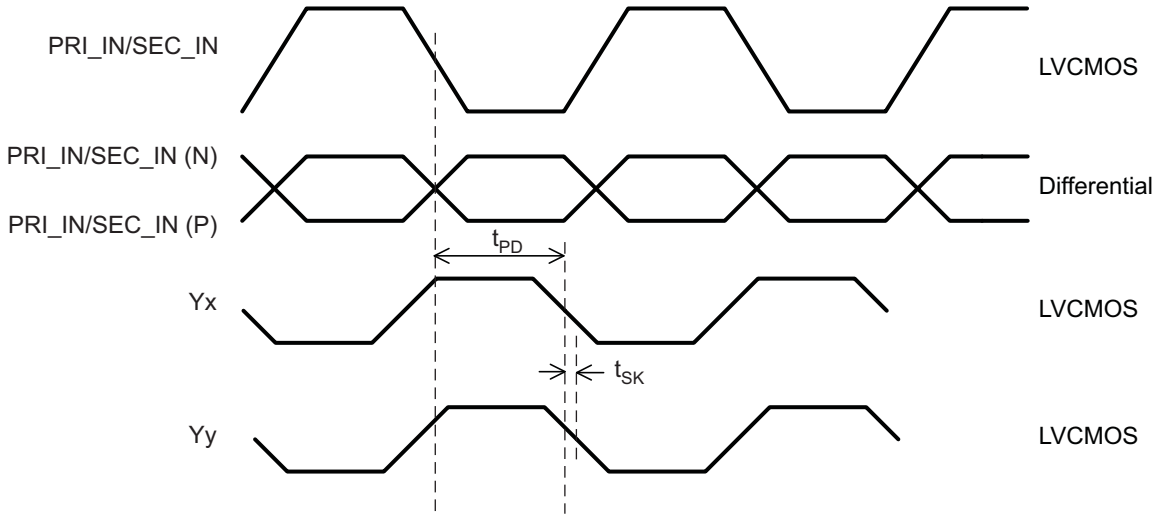


Figure 11. Differential and Single-Ended Output Skew and Propagation Delay

Crystal Oscillator Input

The crystal oscillator circuit is characterized with 18-pF parallel-resonant crystals. Choices of C1 and C2 were to minimize the ppm error. Optional resistor $R_{OPTIONAL}$ limits the drive level of the oscillator circuit.

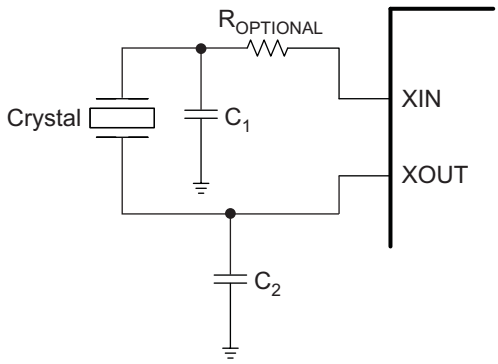


Figure 12. Crystal Reference Input

The input XIN can accept single-ended LVCMOS signals in two configurations. It is possible to overdrive the oscillator stage or to use a pure LVCMOS input (see Table 1). If overdriving the oscillator stage, it is necessary to ac-couple the input with a capacitor (see Figure 13). Otherwise, if selecting the bypass, there is no requirement for a coupling capacitor. Additional measurements and information about crystal oscillator input and limiting the drive level are available in the applications report *Crystal Oscillator Performance of the CDCLVC1310* (SCAA119).

NOTE

If using the overdrive or bypass mode, the device is functional, but may not meet its ac parameters.

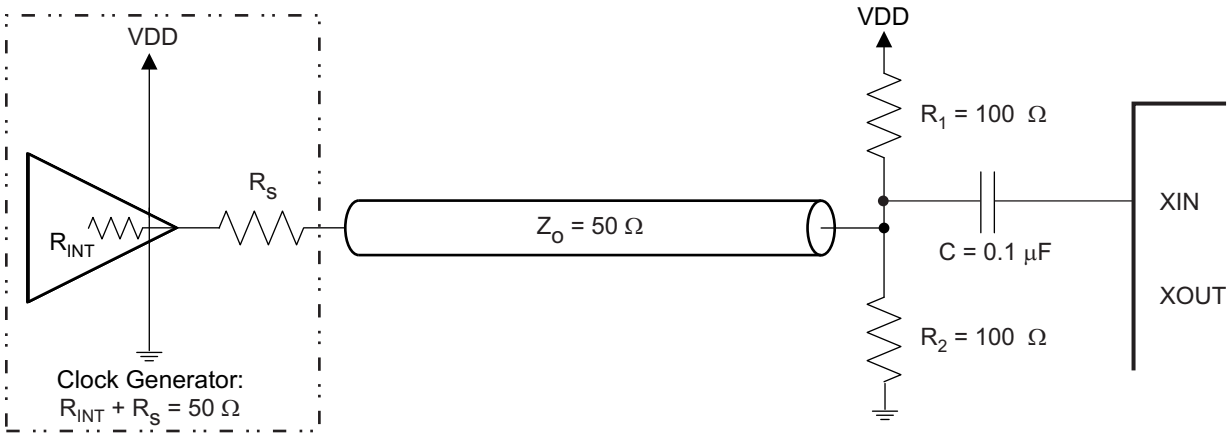


Figure 13. Single-Ended Crystal Input

Phase-Noise Performance

The CDCLVC1310 provides ultralow phase-noise outputs (noise floor = –170 dBc/Hz) if it has an attached crystal. Figure 14 shows the phase-noise plot of the CDCLVC1310 with a 25-MHz crystal at V_{DD} = V_{DDO} = 3.3 V and room temperature.

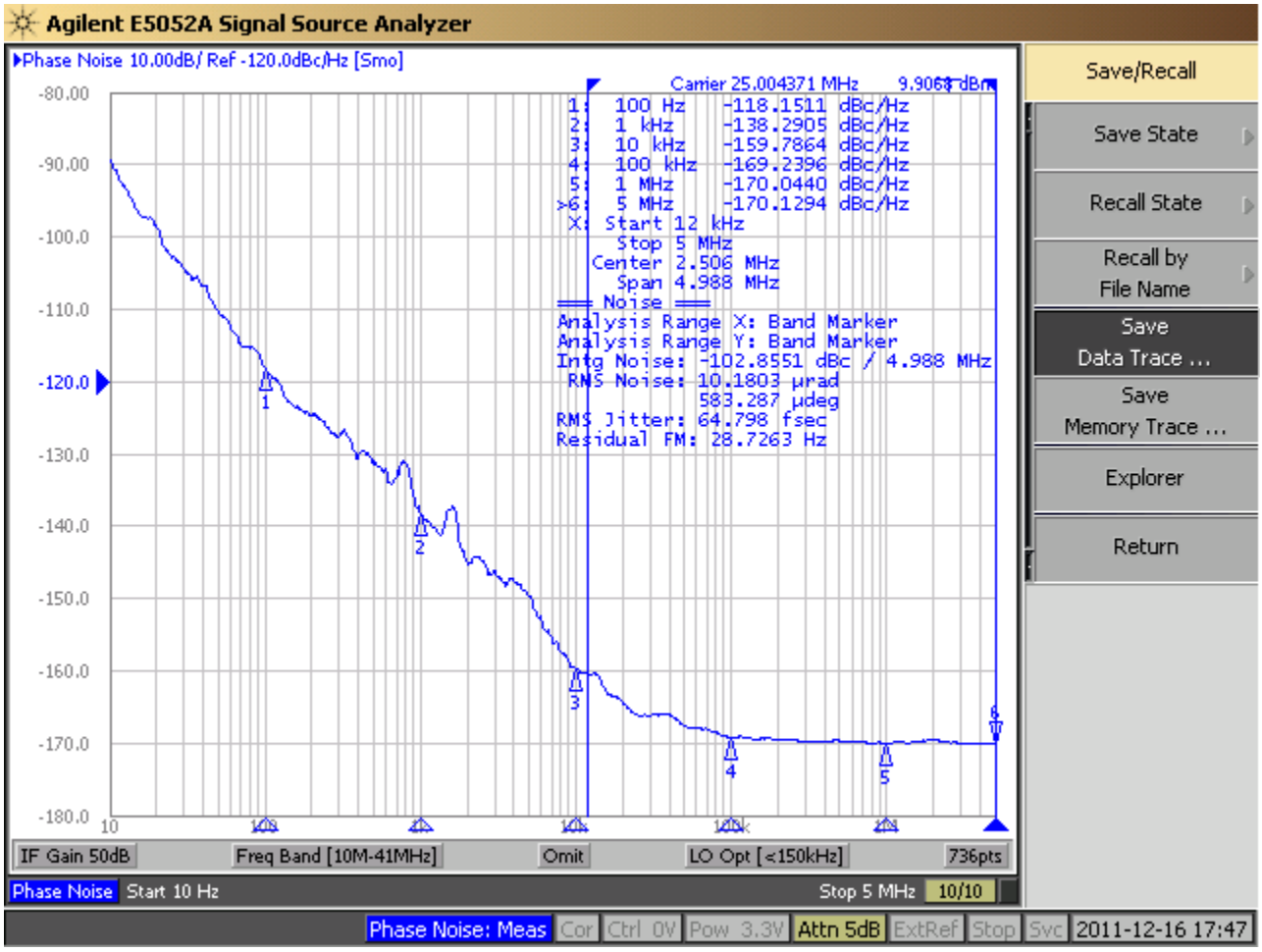


Figure 14. Phase-Noise Profile With 25-MHz Crystal at Nominal Conditions

System-Level Additive-Jitter Measurement

For high-performance devices, limitations of the equipment influence phase-noise measurements. The noise floor of the equipment often exceeds the noise floor of the device. The real noise floor of the device is probably lower (see LVCMOS Output Characteristics). Phase noise is influenced by the input source and the measurement equipment. Additional measurements and information about system-level additive jitter and noise floor are available in the applications report *Phase Noise Performance of CDCLVC1310* (SCAA115).

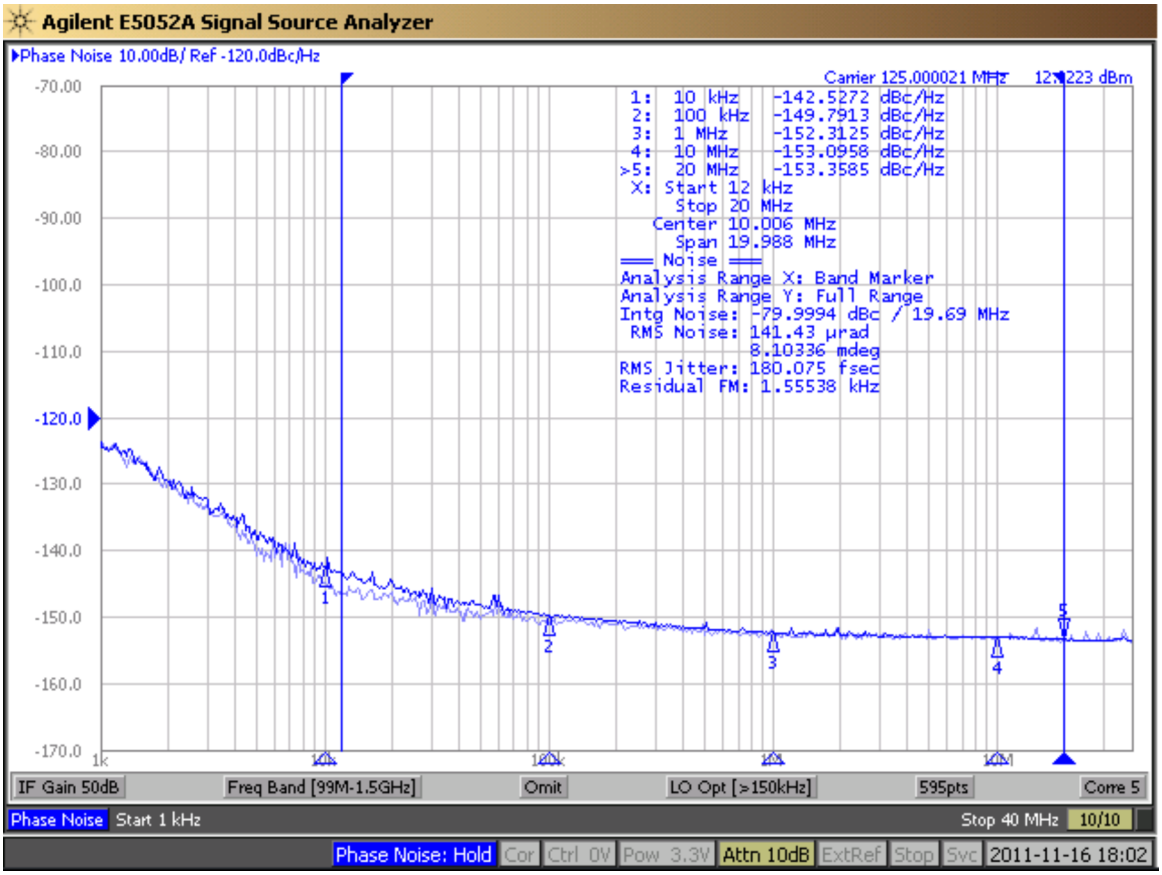


Figure 15. Input Phase Noise (179.4 fs, Light Blue) and Output Phase Noise (180 fs, Dark Blue)

Output Enable

Pulling OE to LOW (t_1), forces the outputs to the high-impedance state after the next falling edge of the input signal (t_2). The outputs remain in the high-impedance state as long as OE is LOW (see Figure 16).

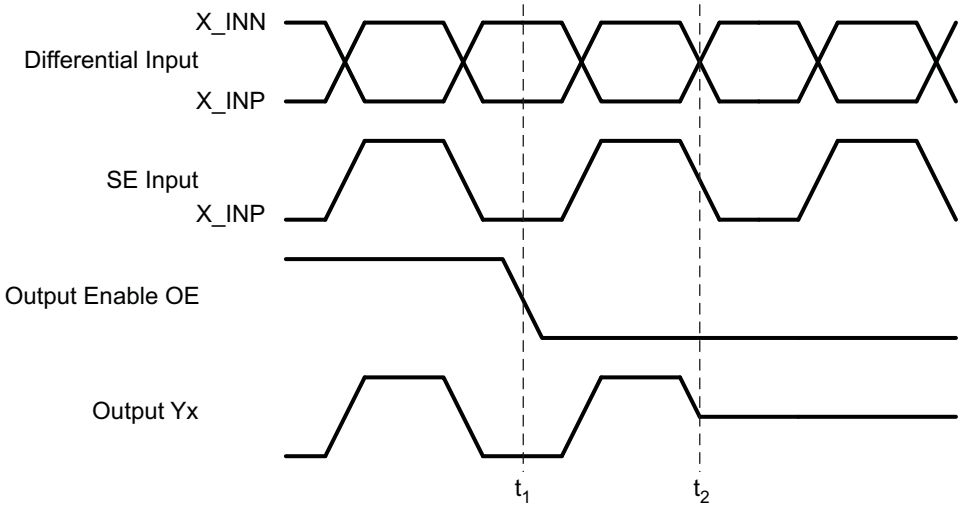


Figure 16. OE: Disable Outputs

If the outputs are in the high-impedance state, pulling OE to HIGH forces all outputs LOW asynchronously (t_3). Within two clock cycles (maximum), the outputs start switching again (t_4), after a falling edge of the input signal (see Figure 17).

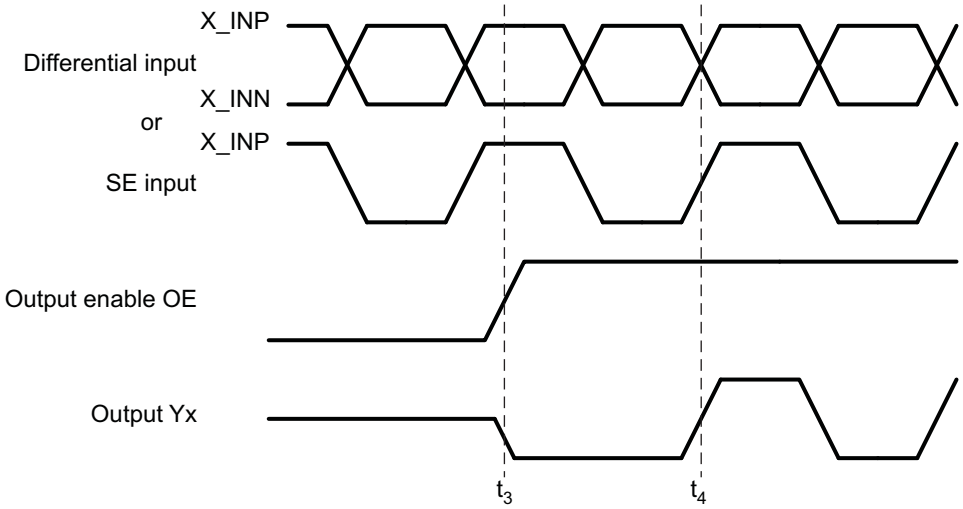


Figure 17. OE: Enable Outputs

If the outputs are in the high-impedance state and the input is static (no clock signal), OE works fully asynchronously. A transition of OE from LOW to HIGH forces the outputs to LOW. A transition from HIGH to LOW does not force to the high-impedance state again. Therefore, a state change requires a falling edge of the input signal (see Figure 16).

MUX Isolation

The definition of MUX isolation is the difference in output amplitude (dB) between an active and a static input signal.

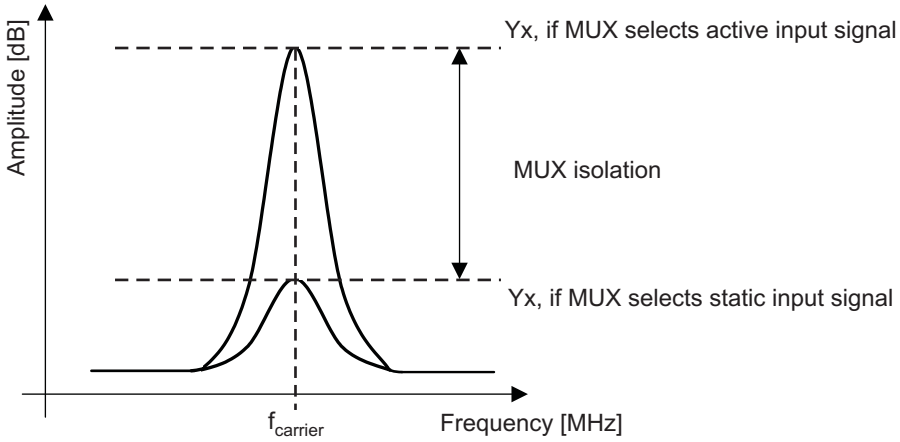
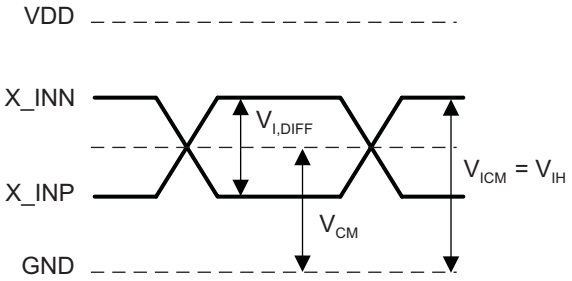


Figure 18. Output Spectrum of an Active and a Static Input Signal

Differential Input Level



NOTE: The calculation for VCM is: $V_{CM} = V_{DD} – V_{ICM} – V_{I,DIFF}/2$

Figure 19. Differential Input Level

Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states
- Power required to charge any output load

The output load can be capacitive-only or capacitive and resistive. Use the following formula to calculate the power consumption of the device:

$P_{Dev} = P_{stat} + P_{dyn} + P_{Cload}$ (see Figure 20 and Figure 21)

$P_{stat} = I_{DD} \times V_{DD}$

$P_{dyn} + P_{Cload} = (I_{DD,dyn} + I_{DD,Cload}) \times V_{DDO}$

where:

$I_{DD,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA] (see Figure 22)

$I_{DD,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA]

Example for power consumption of the CDCLVC1310: 10 outputs are switching, f = 100 MHz, $V_{DD} = V_{DDO}$ = 3.3 V and assuming C_{load} = 2 pF per output:

P_{Dev} = 46.2 mW + 117.5 mW = 163.7 mW

P_{stat} = 14 mA × 3.3 V = 46.2 mW

$P_{dyn} + P_{Cload}$ = (29 mA + 6.6 mA) x 3.3 V = 117.5 mW

$I_{DD,dyn}$ = 8.8 pF × 3.3 V × 100 MHz × 10 = 29 mA

$I_{DD,Cload}$ = 2 pF × 3.3 V x 100 MHz × 10 = 6.6 mA

NOTE

For dimensioning the power supply, consider the total power consumption. The total power consumption is the sum of device power consumption and the power consumption of the load.

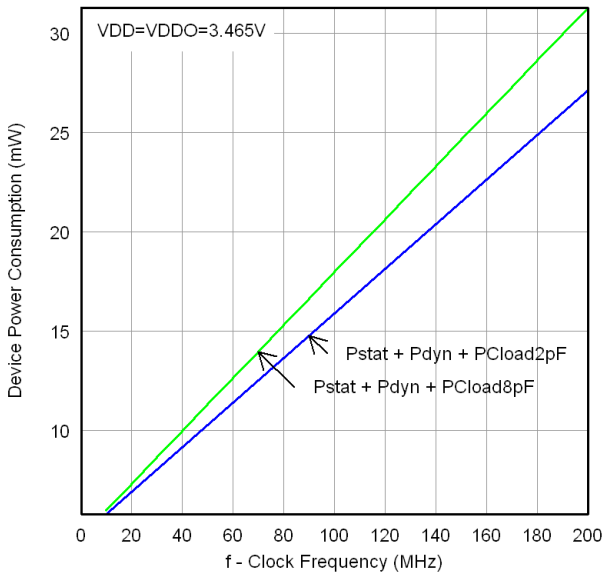


Figure 20. Device Power Consumption versus Clock Frequency (VDD = VDDO = 3.465 V; Load 2 pF, 8 pF; per Output)

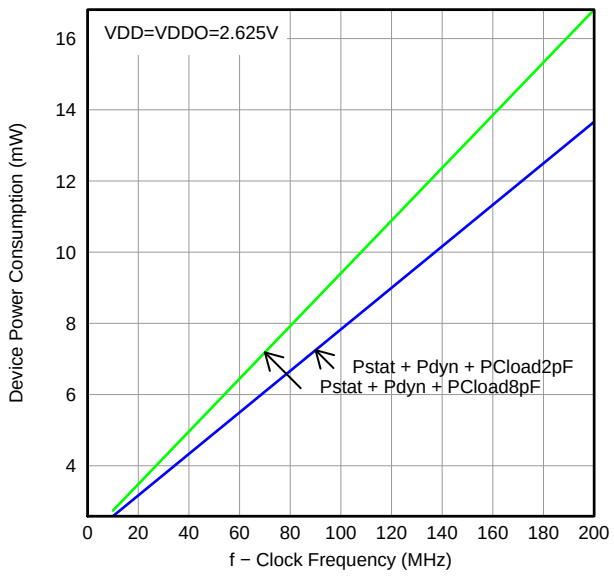


Figure 21. Device Power Consumption versus Clock Frequency (VDD = VDDO = 2.625 V; Load 2 pF, 8 pF; per Output)

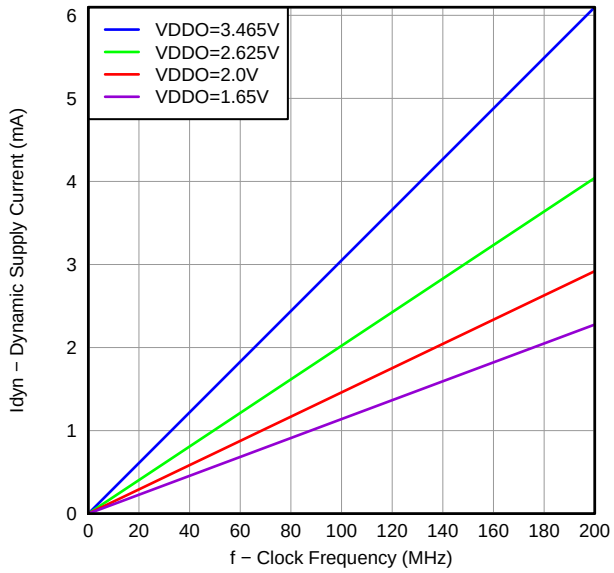


Figure 22. Dynamic Supply Current versus Clock Frequency (per Output)

Thermal Management

Power consumption of the CDCLVC1310 can be high enough to require attention to thermal management. For reliability and performance reasons, limit the die temperature to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125°C.

The device package has an exposed pad that provides the primary heat removal path as well as an electrical grounding to the printed circuit board (PCB). To maximize the removal of heat from the package, incorporate a thermal landing pattern including multiple vias to a ground plane on the PCB within the footprint of the package. Solder the exposed pad down to ensure adequate heat conduction out of the package. Figure 23 shows a recommended land and via pattern.

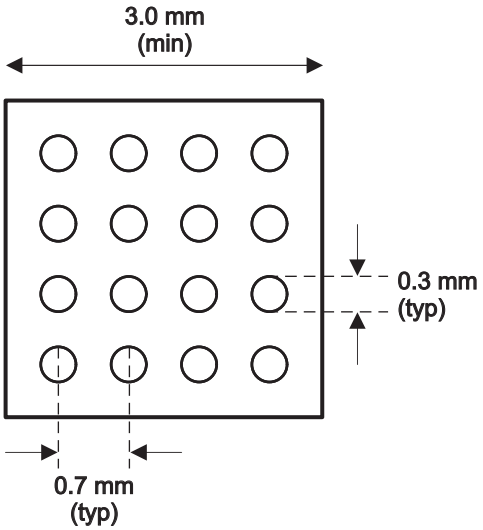


Figure 23. Recommended PCB Layout for CDCLVC1310

Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is very critical to applications.

Use of filter capacitors eliminates the low-frequency noise from power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, place them very close to the power supply pins and lay out traces with short loops to minimize inductance. TI recommends to adding as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package. There is a recommendation, but not a requirement, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low dc resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply, and to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

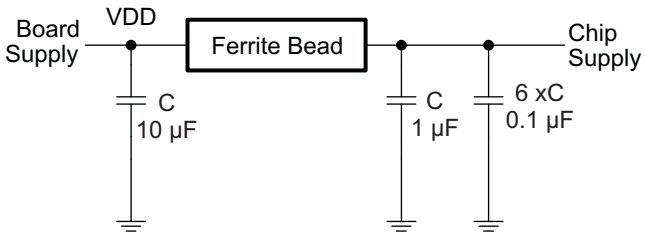


Figure 24. Power-Supply Decoupling

REVISION HISTORY

Changes from Revision D (July 2013) to Revision E **Page**

- Changed V_{OH} in LVCMOS OUTPUT CHARACTERISTICS 7
- Changed V_{OL} in LVCMOS OUTPUT CHARACTERISTICS 7
- Changed $t_{SLEW-RATE}$ in LVCMOS OUTPUT CHARACTERISTICS 7

Changes from Revision C (October 2012) to Revision D **Page**

- Changed t_{DELAY} in LVCMOS OUTPUT CHARACTERISTICS 8

Changes from Revision B (February 2012) to Revision C **Page**

- Changed unit for phase jitter from picosecond to femtosecond 9
- Revised Figure 3 10
- Revised Figure 4 10
- Revised Figure 5 11
- Revised Figure 6 11
- Revised Figure 8 12
- Added reference to application report SCAA119 14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCLVC1310RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVC 1310
CDCLVC1310RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVC 1310
CDCLVC1310RHBRG4.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVC 1310

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

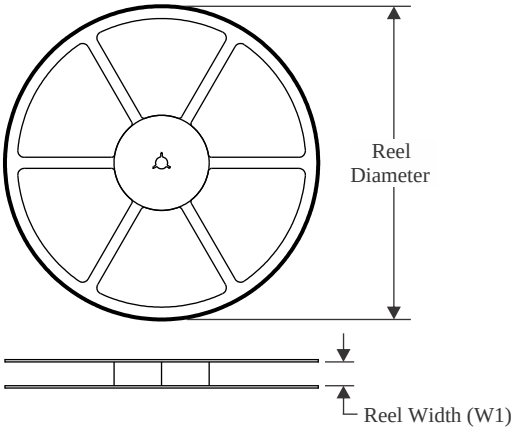
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

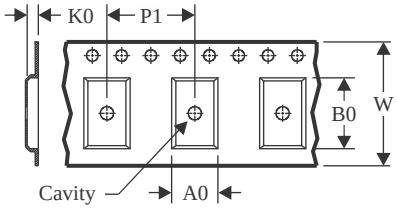
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

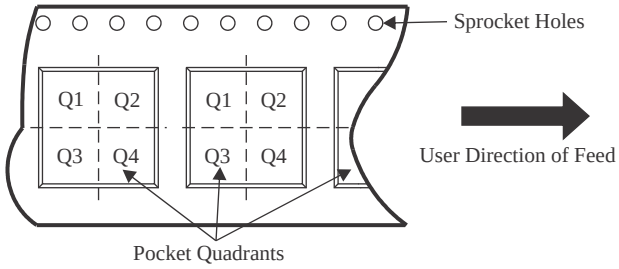


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

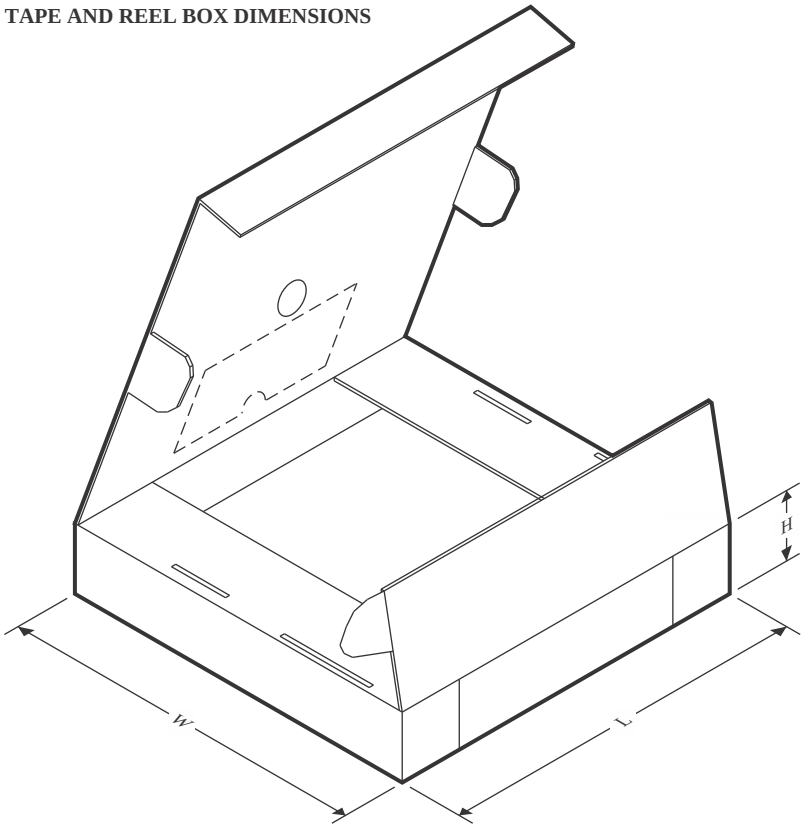
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVC1310RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVC1310RHBR	VQFN	RHB	32	3000	346.0	346.0	33.0

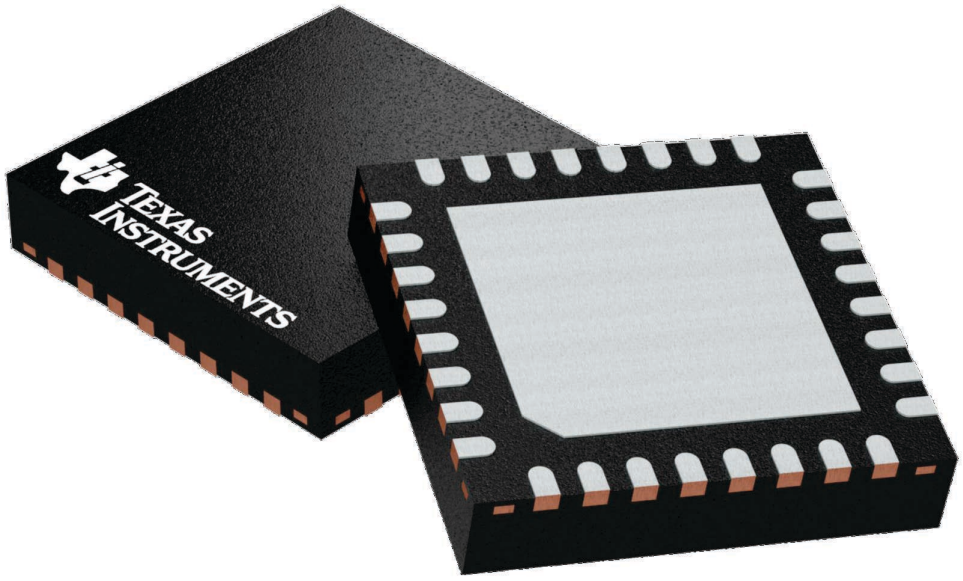
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

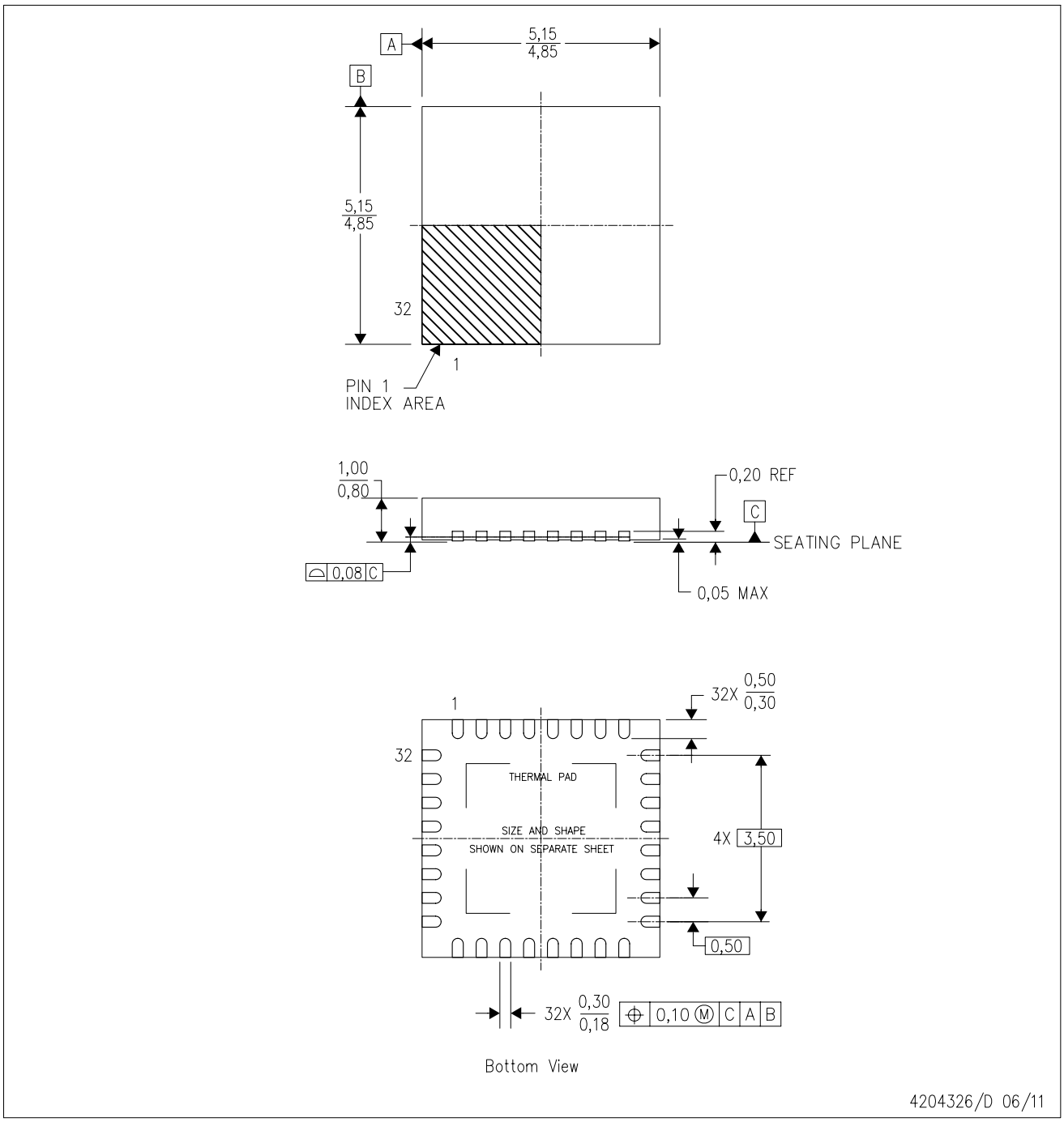
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

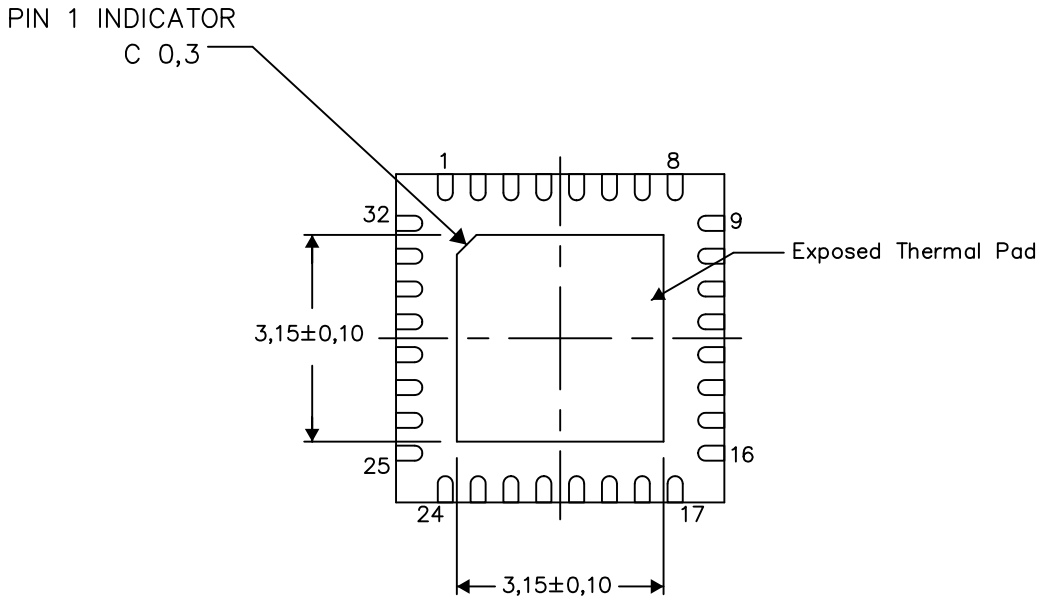
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



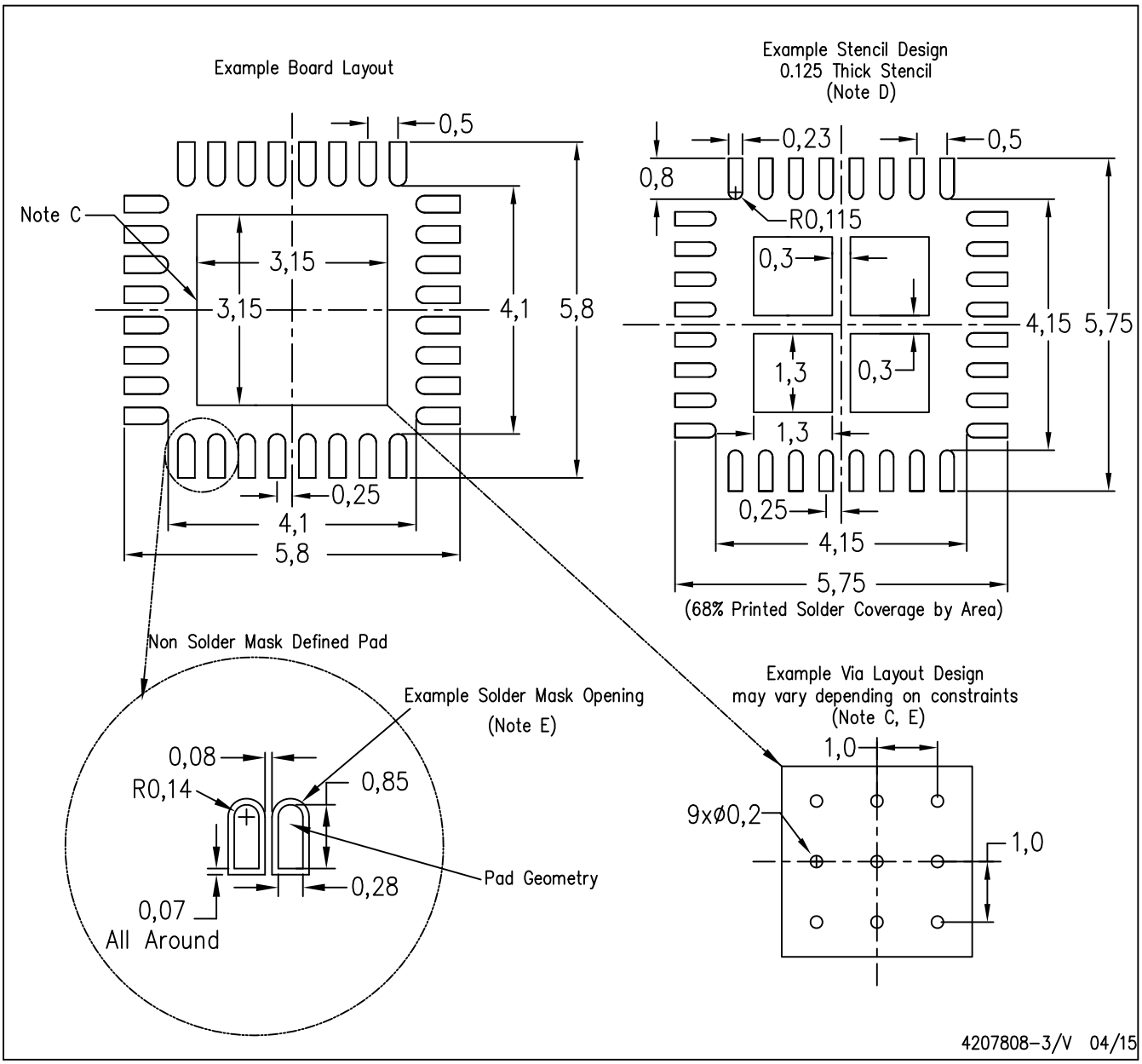
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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