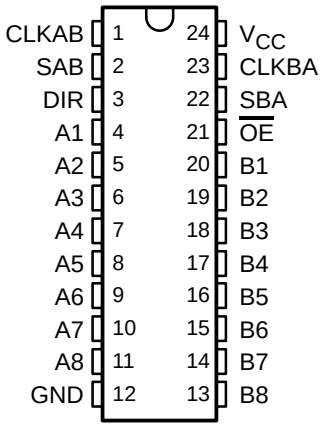
- **2-V to 6-V V_{CC} Operation (CD54HC646)**
- **4.5-V to 5.5-V V_{CC} Operation (CD74HCT646)**
- **Wide Operating Temperature Range of –55°C to 125°C**
- **Balanced Propagation Delays and Transition Times**
- **Standard Outputs Drive Up To 15 LS-TTL Loads**
- **Significant Power Reduction Compared to LS-TTL Logic ICs**
- **Inputs Are TTL-Voltage Compatible (CD74HCT646)**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **True Data Paths**

CD54HC646 . . . F PACKAGE
CD74HCT646 . . . M PACKAGE
(TOP VIEW)



description/ordering information

The CD54HC646 and CD74HCT646 consist of bus-transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with these devices.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either or both registers.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

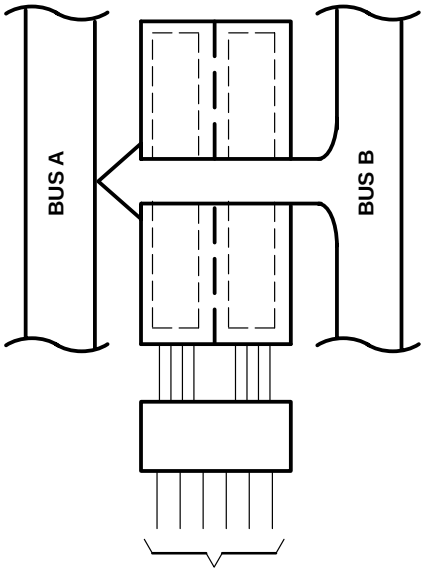
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – M	Tape and reel	CD74HCT646M96	HCT646M
	CDIP – F	Tube	CD54HC646F3A	CD54HC646F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

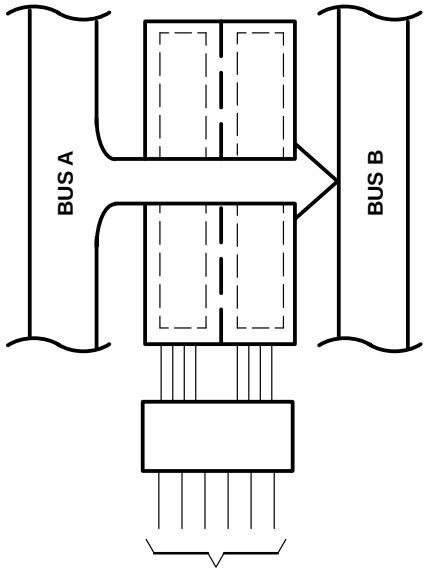
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



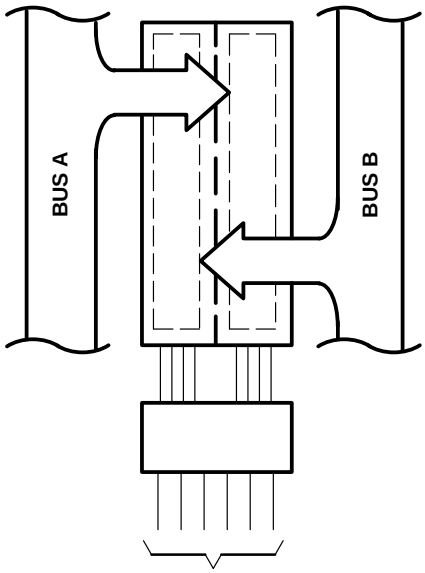
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



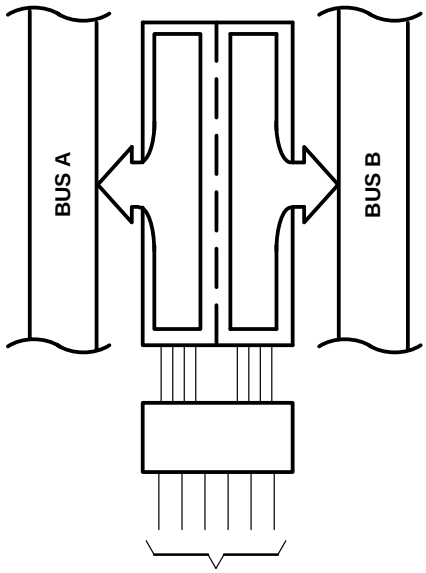
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

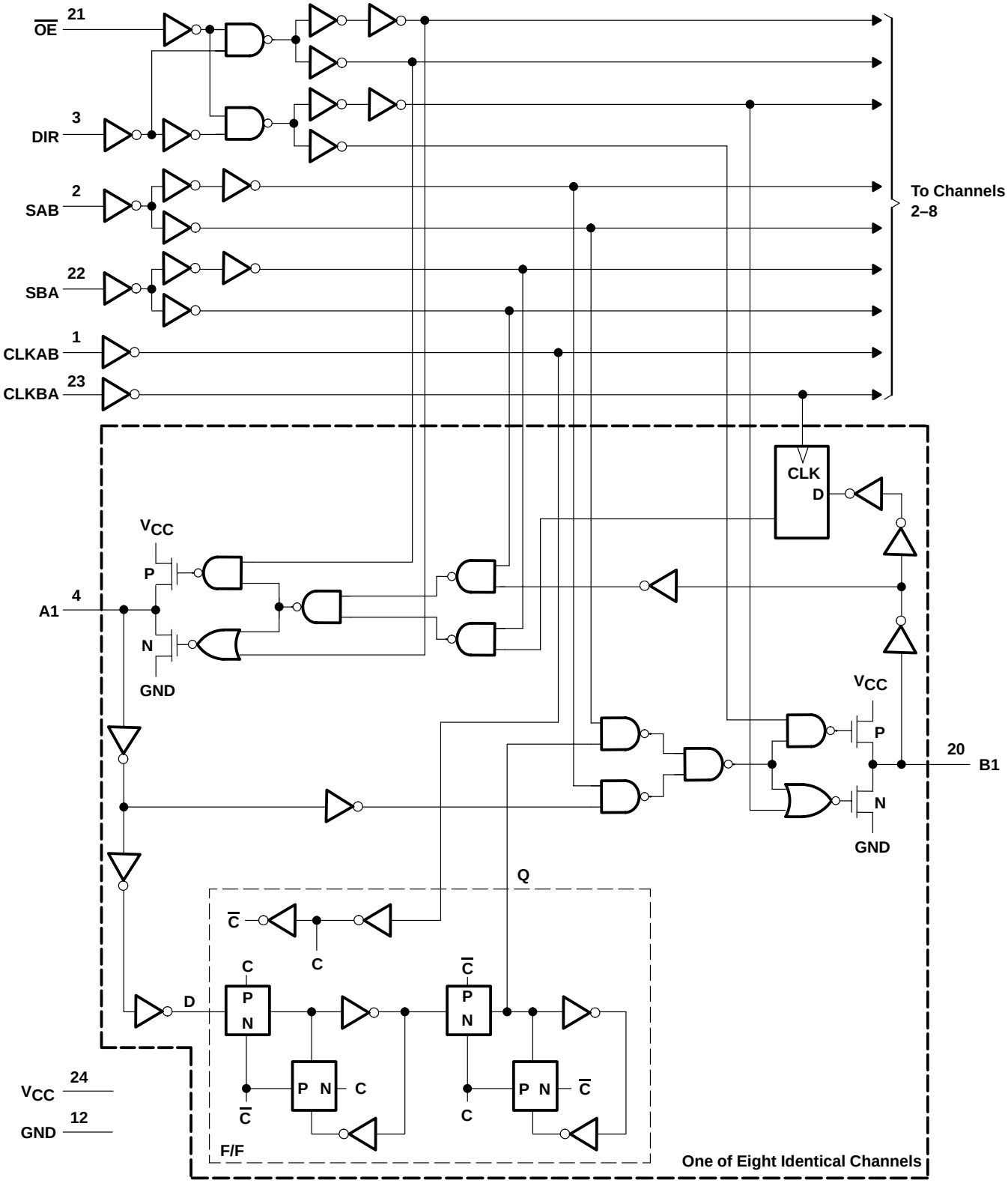


21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output drain current per output, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2) M package . . . . . 46°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions for CD54HC646 (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V		1000	ns
		V_{CC} = 4.5 V		500	
		V_{CC} = 6 V		400	
T_A	Operating free-air temperature		–55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for CD74HCT646 (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage		V_{CC}	V
V_O	Output voltage		V_{CC}	V
t_t	Input transition (rise and fall) time		500	ns
T_A	Operating free-air temperature	–55	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics for CD54HC646 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9		1.9		1.9		V
			4.5 V	4.4		4.4		4.4		
			6 V	5.9		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.1		0.1		0.1	V
			4.5 V		0.1		0.1		0.1	
			6 V		0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V		8		160		80	μA
C_i					10		10		10	pF
C_o					20		20		20	pF

electrical characteristics for CD74HCT646 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4			4.4		4.4		V
		I_{OH} = –6 mA		3.98			3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 6 mA				0.26		0.4		0.33	
I_I	V_I = V_{CC} to GND		5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or 0		5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at V_{CC} – 2.1 V, Other inputs at 0 or V_{CC}		4.5 V to 5.5 V		100	360		490		450	μA
C_i						10		10		10	pF
C_o						20		20		20	pF

† Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD†
$\overline{OE}$	1.3
DIR	0.75
CLKAB or CLKBA	0.6
SAB or SBA	0.45
A or B	0.3

† Unit Load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 360 μA max at 25°C).

timing requirements for CD54HC646 over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		V_{CC}	T_A = 25°C		T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V		6		4		5	MHz
		4.5 V		30		20		25	
		6 V		35		23		29	
t_w	Pulse duration, CLKBA or CLKAB high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	2 V	60		90		75		ns
		4.5 V	12		18		15		
		6 V	10		15		13		
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	2 V	35		55		45		ns
		4.5 V	7		11		9		
		6 V	6		9		8		

timing requirements for CD74HCT646 over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 3)

		T_A = 25°C		T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		25		17		20	MHz
t_w	Pulse duration, CLKBA or CLKAB high or low	25		38		31		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	12		18		15		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	5		5		5		ns

switching characteristics for CD54HC646 over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF	2 V	6			4		5		MHz
				4.5 V	30			20		25		
				6 V	35			23		29		
			C_L = 15 pF	5 V		60						
t_{pd}	CLKBA or CLKAB	A or B	C_L = 50 pF	2 V			220		330		275	ns
				4.5 V			44		66		55	
				6 V			37		56		47	
			C_L = 15 pF	5 V		18						
	A or B	B or A	C_L = 50 pF	2 V			135		205		170	
				4.5 V			27		41		34	
				6 V			23		35		29	
			C_L = 15 pF	5 V		12						
	SBA or SAB†	A or B	C_L = 50 pF	2 V			170		255		215	
				4.5 V			34		51		43	
				6 V			29		43		37	
			C_L = 15 pF	5 V		14						
t_{en}	$\overline{OE}$	A or B	C_L = 50 pF	2 V			175		265		220	ns
				4.5 V			35		53		44	
				6 V			30		45		37	
			C_L = 15 pF	5 V		14						
t_{dis}	$\overline{OE}$	A or B	C_L = 50 pF	2 V			175		265		220	ns
				4.5 V			35		53		44	
				6 V			30		45		37	
			C_L = 15 pF	5 V		14						
t_t		Any	C_L = 50 pF	2 V			60		90		75	ns
				4.5 V			12		18		15	
				6 V			10		15		13	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics for CD74HCT646 over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

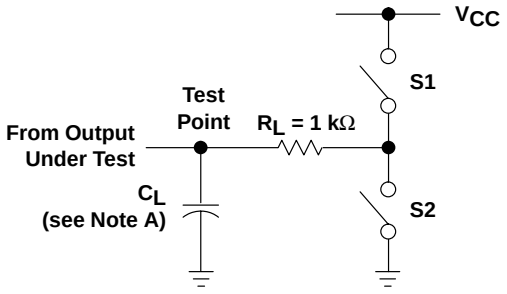
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF	4.5 V	25			17		20		MHz
			C_L = 15 pF	5 V		45						
t_{pd}	CLKBA or CLKAB	A or B	C_L = 50 pF	4.5 V			44		66		55	ns
			C_L = 15 pF	5 V		18						
	A or B	B or A	C_L = 50 pF	4.5 V			37		56		46	
			C_L = 15 pF	5 V		15						
	SBA or SAB†	A or B	C_L = 50 pF	4.5 V			46		69		58	
			C_L = 15 pF	5 V		19						
t_{en}	$\overline{OE}$	A or B	C_L = 50 pF	4.5 V			45		68		56	ns
			C_L = 15 pF	5 V		19						
t_{dis}	$\overline{OE}$	A or B	C_L = 50 pF	4.5 V			35		53		44	ns
			C_L = 15 pF	5 V		14						
t_t			C_L = 50 pF	4.5 V			12		18		15	ns

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

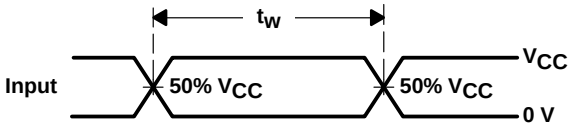
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	52	pF

PARAMETER MEASUREMENT INFORMATION – CD54HC646

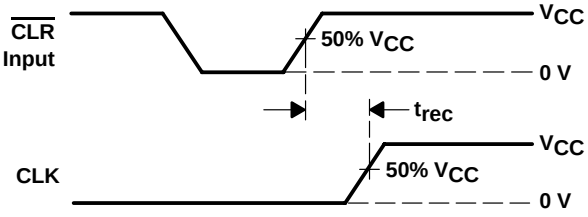


LOAD CIRCUIT

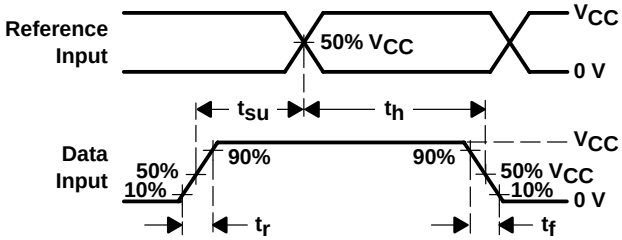
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



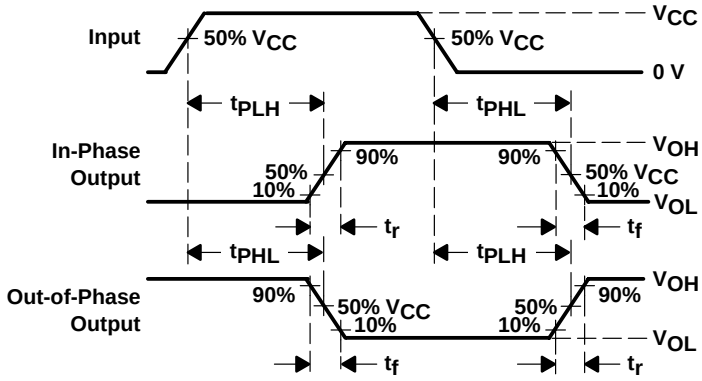
VOLTAGE WAVEFORMS
PULSE DURATION



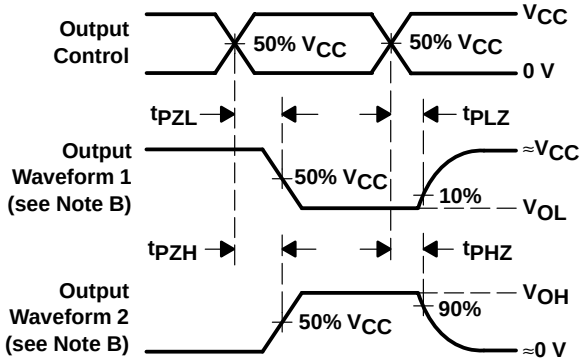
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

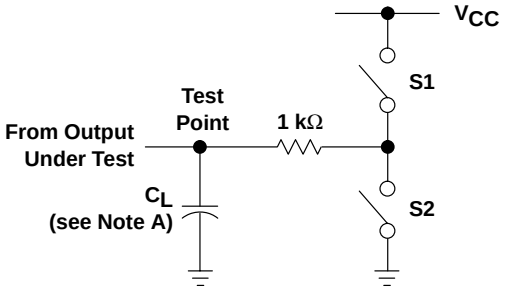


VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

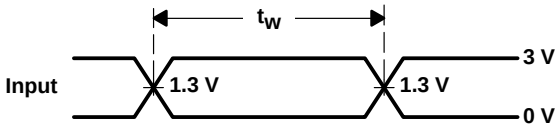
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION – CD74HCT646

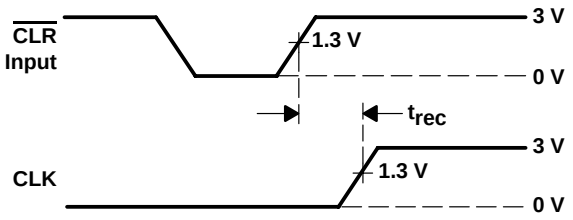


LOAD CIRCUIT

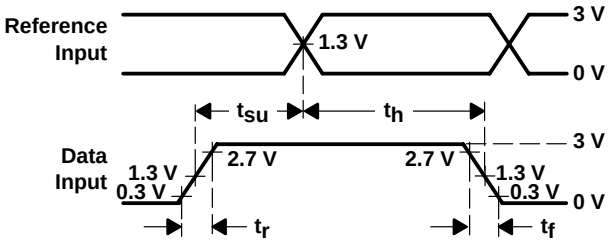
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



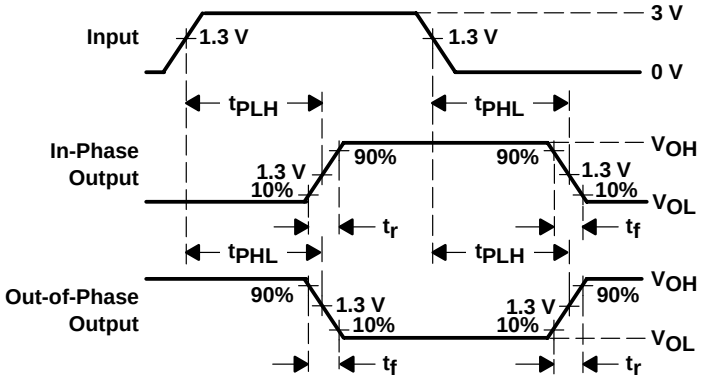
VOLTAGE WAVEFORMS
PULSE DURATION



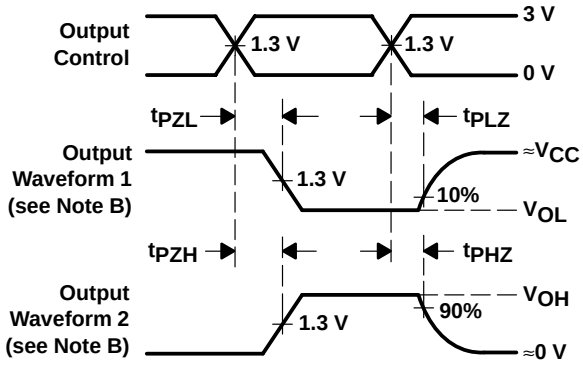
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8688501JA	Active	Production	CDIP (J) | 24	15 | TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8688501JA CD54HC646F3A
CD54HC646F3A	Active	Production	CDIP (J) | 24	15 | TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8688501JA CD54HC646F3A
CD54HC646F3A.A	Active	Production	CDIP (J) | 24	15 | TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8688501JA CD54HC646F3A
CD74HCT646M96	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT646M
CD74HCT646M96.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT646M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

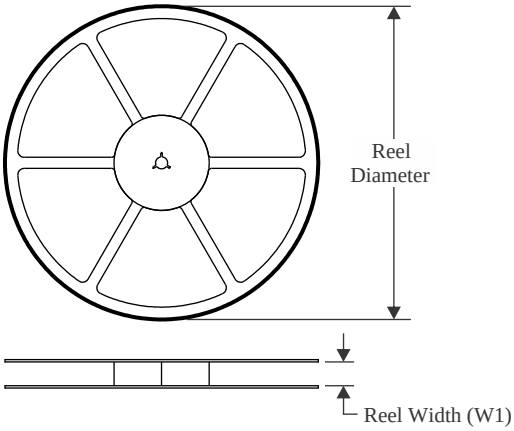
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

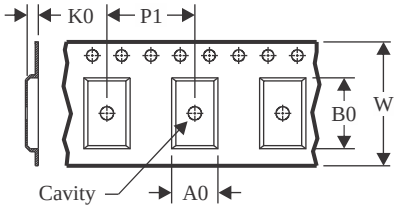
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

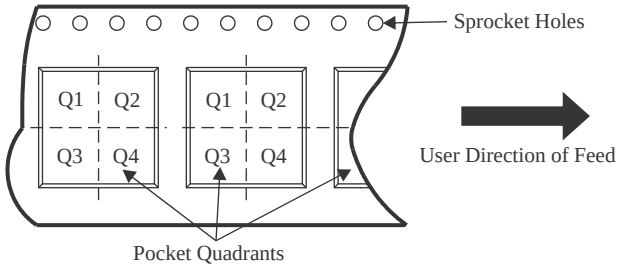


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

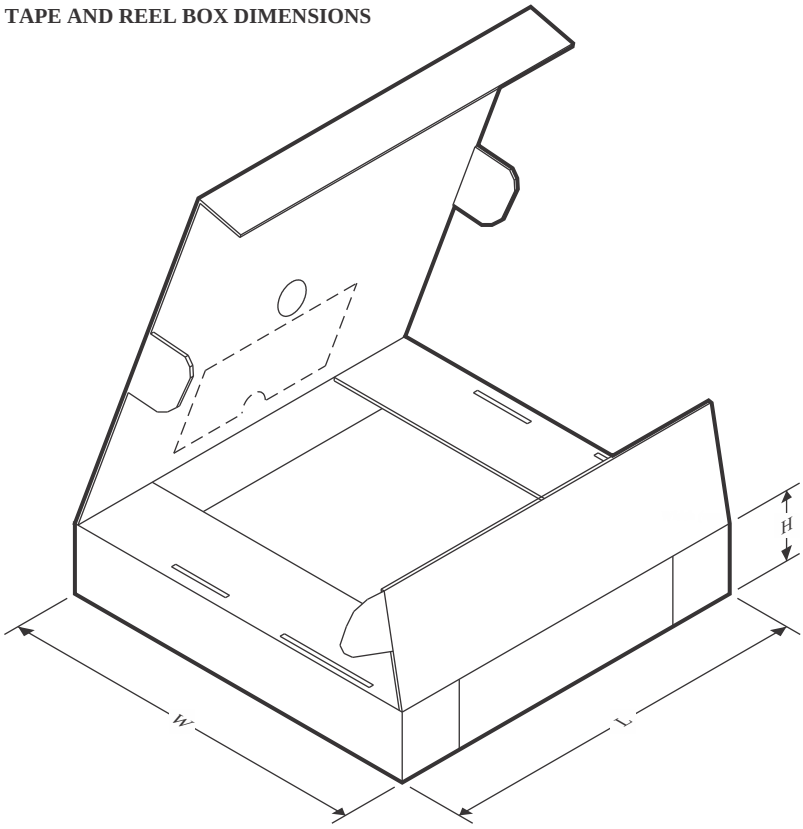
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT646M96	SOIC	DW	24	2000	350.0	350.0	43.0

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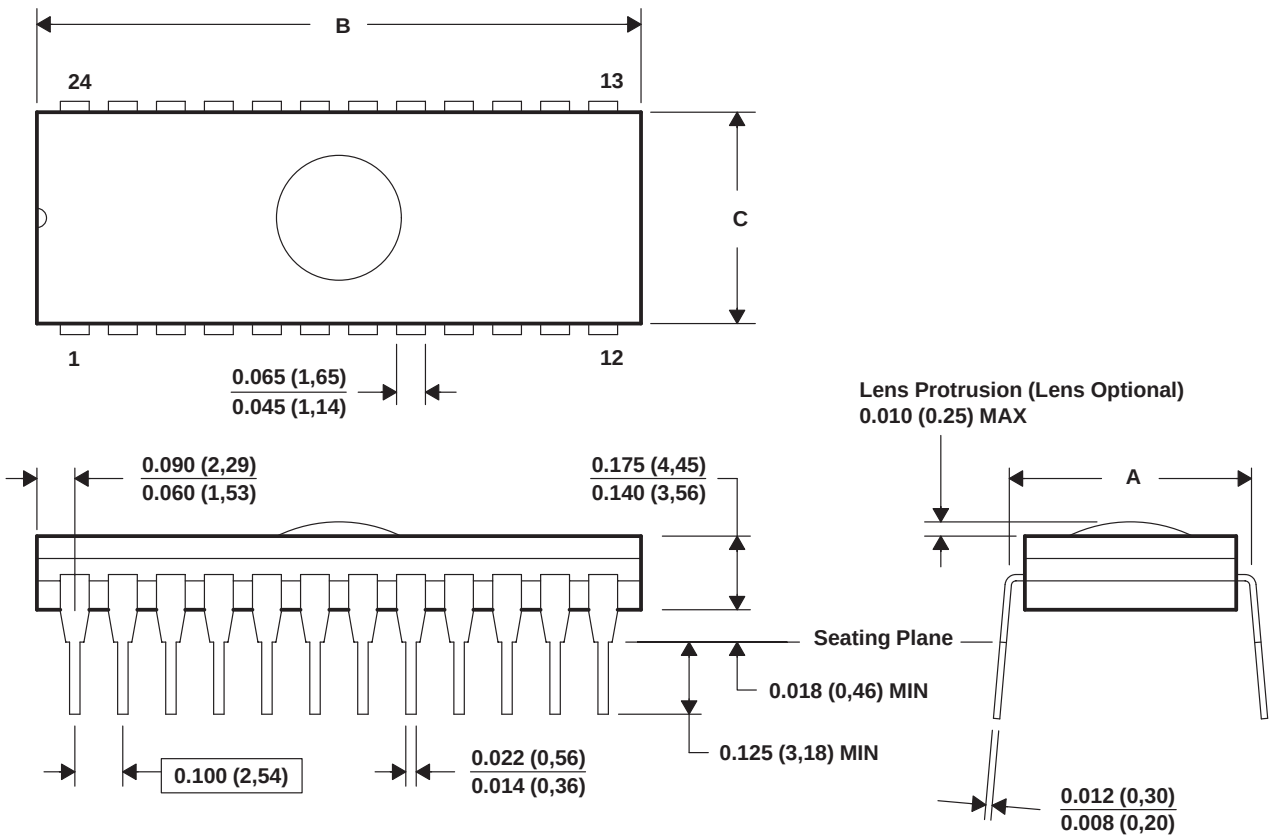
J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



DIM \ PINS **		24		28		32		40	
		NARR	WIDE	NARR	WIDE	NARR	WIDE	NARR	WIDE
"A"	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
"B"	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
"C"	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

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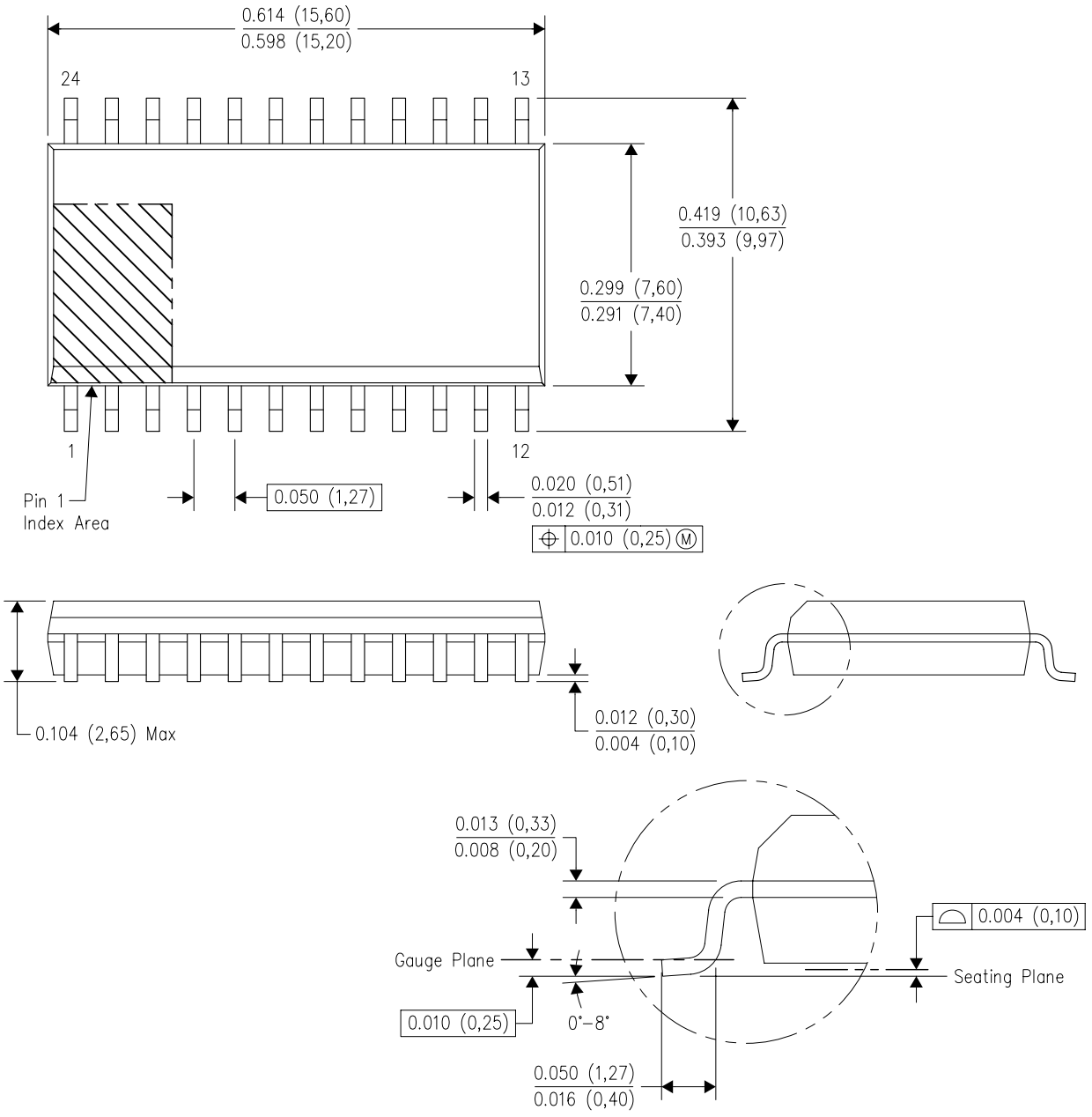
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
D. This package can be hermetically sealed with a ceramic lid using glass frit.
E. Index point is provided on cap for terminal identification.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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