TEXAS INSTRUMENTS
CD54HC4511, CD74HC4511, CD74HCT4511
JAJSOZ9E – DECEMBER 1998 – REVISED AUGUST 2022

CDx4HC4511、CD74HCT4511 BCD から 7 セグメントへのラッチ / デコーダ / ドライバ

1 特長

- 2V～6V の V_{CC} で動作 ('HC4511)
- 4.5V～5.5V の V_{CC} で動作 (CD74HCT4511)
- 高い出力ソース能力
  - 4.5V で 7.5mA (CD74HCT4511)
  - 6V で 10mA ('HC4511)
- BCD コード・ストレージ用の入力ラッチ
- ランプ・テストおよびブランキング機能
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC と比べて消費電力を大幅に削減
- 'HC4511
  - 高いノイズ耐性、V_{CC} = 5V 時に V_{CC} に対して N_{IL} または N_{IH} = 30%
- CD74HCT4511
  - LSTTL 入力ロジックと直接互換、V_{IL} = 0.8V (最大値)、V_{IH} = 2V (最小値)
  - CMOS 入力互換、V_{OL}、V_{OH} で $I_I \leqq 1_{\mu A}$

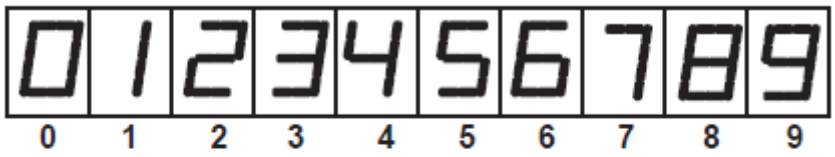
2 概要

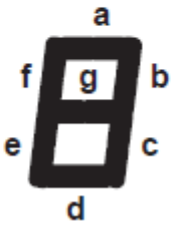
CD54HC4511 、CD74HC4511 、CD74HCT4511 は、BCD から 7 セグメントへのラッチ / デコーダ / ドライバで、4 つのアドレス入力 (D_0～D_3) と、アクティブ Low のブランキング ($\overline{BL}$) 入力、ランプ・テスト ($\overline{LT}$) 入力、ラッチ・イネーブル ($\overline{LE}$) 入力を搭載しており、ラッチ・イネーブル入力が High のときは BCD 入力をラッチに保存できます。$\overline{LE}$ が Low のときはラッチがディセーブルで、出力が BCD 入力に対して透過的になります。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
CD54HC4511	J (CDIP、16)	24.38mm × 6.92mm
CD74HC4511	N (PDIP、16)	19.31mm × 6.35mm
	D (SOIC、16)	9.90mm × 3.90mm
	PW (TSSOP、16)	5.00mm × 4.40mm
CD74HCT4511	N (PDIP、16)	19.31mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。





ディスプレイ

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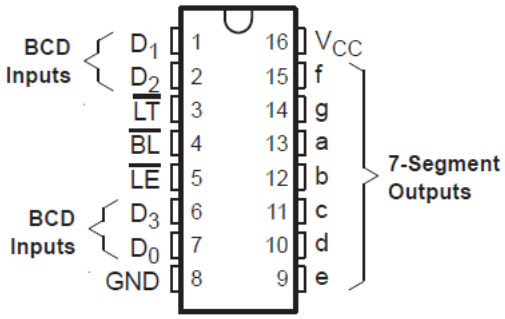
3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2003) to Revision E (August 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新	1

4 Pin Configuration and Functions



J, N, D, PW package
16-Pin CDIP, PDIP, SOIC, TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
I_{IK}	Input diode current	V_I < – 0.5 V or V_I > V_{CC} + 0.5 V (1)		±20	mA
I_{OK}	Output diode current	V_O < – 0.5 V or V_O > V_{CC} + 0.5 V (1)		±20	mA
I_O	Output source or sink current per output pin	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (During Soldering)	At distance 1/16 ± 1/32 in (1.59 ± 0.79 mm) from case for 10 s maximum		265	°C
		Unit inserted into a PC board (minimum thickness 1/16 in, 1.59 mm) (with solder contacting lead tips only)		300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

5.2 Recommended Operating Conditions for 'HC4511(1)

			T_A = 25°C		T_A = – 55°C to 125°C		T_A = – 40°C to 85°C		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	6	2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		1.5		V
		V_{CC} = 4.5 V	3.15		3.15		3.15		
		V_{CC} = 6 V	4.2		4.2		4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5		0.5	V
		V_{CC} = 4.5 V		1.35		1.35		1.35	
		V_{CC} = 6 V		1.8		1.8		1.8	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
t_t	Input transition rise/fall time	V_{CC} = 2 V		1000		1000		1000	ns
		V_{CC} = 4.5 V		500		500		500	
		V_{CC} = 6 V		400		400		400	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.3 Recommended Operating Conditions for CD74HCT4511(1)

		T_A = – 55°C to 125°C		T_A = – 55°C to 125°C		T_A = – 40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	
V_I	Input voltage		V_{CC}		V_{CC}		V_{CC}	V
V_O	Output voltage		V_{CC}		V_{CC}		V_{CC}	V

5.3 Recommended Operating Conditions for CD74HCT4511(1) (continued)

		T_A = – 55°C to 125°C		T_A = – 55°C to 125°C		T_A = – 40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_t	Input transition (rise and fall) time		500		500		500	ns

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	N (PDIP) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Package thermal impedance	67	73	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 'HC4511 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		T_A = – 55°C to 125°C		T_A = – 40°C to 85°C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = −20 µA	2 V	1.9		1.9		1.9		V
				4.5 V	4.4		4.4		4.4		
				6 V	5.9		5.9		5.9		
			I_{OH} = −4 mA	4.5 V	3.98		3.7		3.84		
			I_{OH} = −5.2 mA	6 V	5.48		5.2		5.34		
V_{OL}	Low level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.1		0.1		0.1	V
				4.5 V		0.1		0.1		0.1	
				6 V		0.1		0.1		0.1	
			I_{OL} = 4 mA	4.5 V		0.26		0.4		0.33	
			I_{OL} = 5.2 mA	6 V		0.26		0.4		0.33	
I_I	Input leakage current V	V_I = V_{CC} or 0		6 V		±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or 0,	I_O = 0	6 V		8		160		80	µA
C_i	Input Capacitance			2 V to 6 V		10		10		10	pF

5.6 CD74HCT4511 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			T_A = −55°C to 125°C		T_A= – 40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = −20 µA	4.5 V	4.4			4.4		4.4		V
			I_{OH} = −4 mA		3.98			3.7		3.84		
V_{OL}	Low level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	4.5 V			0.1		0.1		0.1	
			I_{OL} = 4 mA				0.26		0.4		0.33	
I_I	Input leakage current V	V_I = V_{CC} to GND		5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC} (1)	Supply-Current Change	$\overline{LT}$, $\overline{LE}$ inputs held at V_{CC} – 2.1 V		4.5 V to 5.5 V		100	540		735		675	µA
		$\overline{BL}$, Dn inputs held at V_{CC} – 2.1 V				100	108		147		135	

5.6 CD74HCT4511 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = −55°C to 125°C		T_A = – 40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_i	Input Capacitance					10		10		10	pF

(1) Additional supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

5.7 'HC4511 Timing Requirements

		V_{CC}	T_A = 25°C		T_A = – 55°C to 125°C		T_A = – 40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, $\overline{LE}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, BCD inputs before $\overline{LE}$ ↑	2 V	60		90		75		ns
		4.5 V	12		18		15		
		6 V	10		15		13		
t_h	Hold time, BCD inputs before $\overline{LE}$ ↑	2 V	3		3		3		ns
		4.5 V	3		3		3		
		6 V	3		3		3		

5.8 Switching Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = – 55°C TO 125°C		T_A = – 40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D_n	Output	C_L = 50 pF	2 V			300		450		375	ns
				4.5 V			60		90		75	
				6 V			51		77		64	
			C_L = 15 pF	5 V		25						
	$\overline{LE}$	Output	C_L = 50 pF	2 V			270		405		340	
				4.5 V			54		81		68	
				6 V			46		69		58	
			C_L = 15 pF	5 V		23						
	$\overline{BL}$	Output	C_L = 50 pF	2 V			220		330		275	
				4.5 V			44		66		55	
				6 V			37		56		47	
			C_L = 15 pF	5 V		18						
	$\overline{LT}$	Output	C_L = 50 pF	2 V			160		240		200	
				4.5 V			32		48		40	
				6 V			27		41		34	
			C_L = 15 pF	5 V		13						
t_t		Any	C_L = 50 pF	2 V			75		110		95	ns
				4.5 V			15		22		19	
				6 V			13		19		16	

5.9 CD74HCT4511 Timing Requirements

		T_A = 25°C		T_A = – 55°C TO 125 °C		T_A = – 40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ low	16		24		20		ns
t_{su}	Setup time, BCD inputs before $\overline{LE}$ ↑	16		24		20		ns
t_h	Hold time, BCD inputs before $\overline{LE}$ ↑	5		5		5		ns

over operating free-air temperature range (unless otherwise noted)

5.10 CD74HCT4511 Switching Characteristics

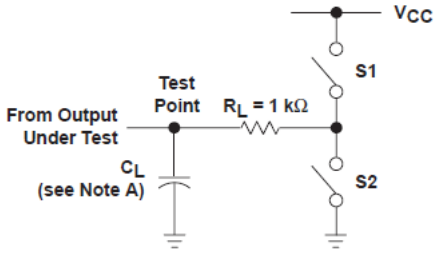
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = – 55°C to 125°C		T_A = – 40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D_n	Output	C_L = 50 pF	4.5 V			60		90		75	ns
			C_L = 15 pF	5 V		25						
	$\overline{LE}$	Output	C_L = 50 pF	4.5 V			54		81		68	
			C_L = 15 pF	5 V		23						
	$\overline{BL}$	Output	C_L = 50 pF	4.5 V			44		66		55	
			C_L = 15 pF	5 V		18						
	$\overline{LT}$	Output	C_L = 50 pF	4.5 V			33		50		41	
			C_L = 15 pF	5 V		13						
t_t		Any	C_L = 50 pF	4.5 V			15		22		19	ns

5.11 Operating Characteristics

PARAMETER[1]			TYP	UNIT
C_{pd}	Power dissipation capacitance	'HC4511	114	pF
		CD74HCT4511	110	

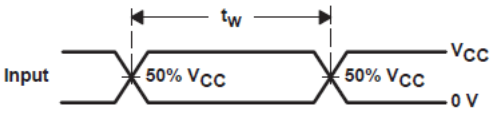
(1) C_{pd} is used to determine the dynamic power consumption, per package.
$P_D = C_{pd} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where:
f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

6 Parameter Measurement Information

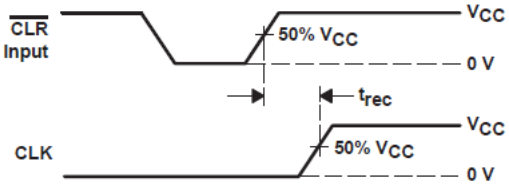


LOAD CIRCUIT

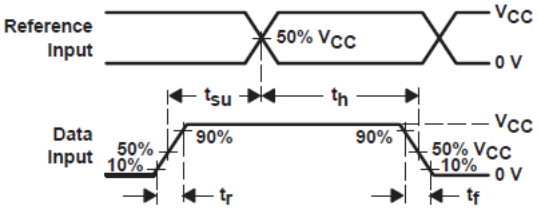
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



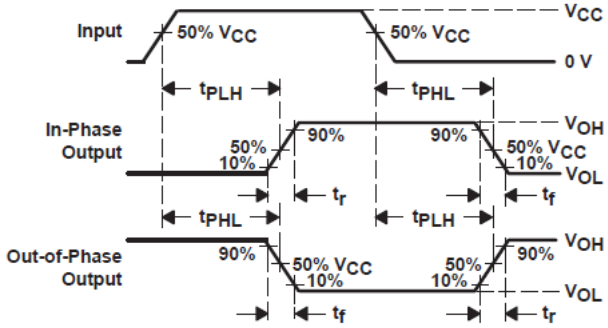
VOLTAGE WAVEFORMS
PULSE DURATION



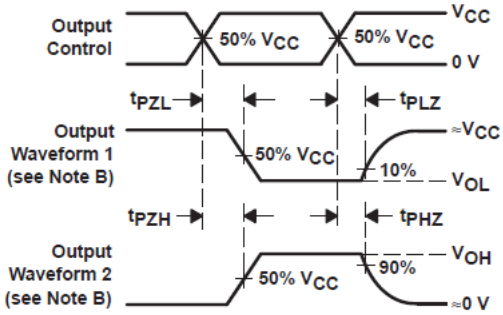
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



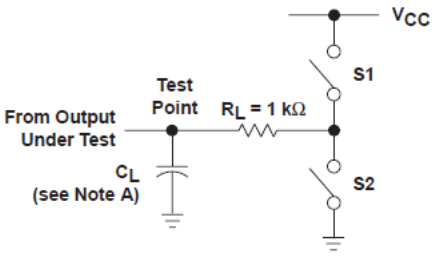
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

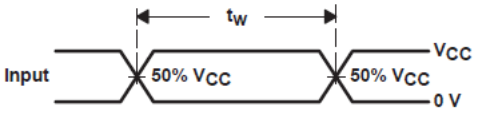
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

図 6-1. 'HC4511

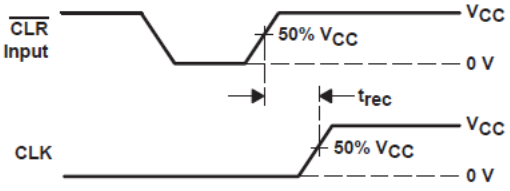


LOAD CIRCUIT

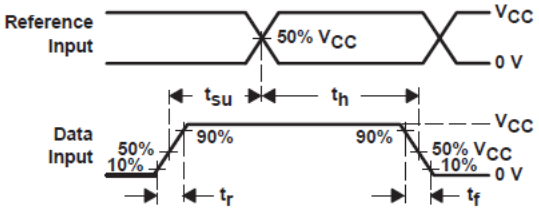
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



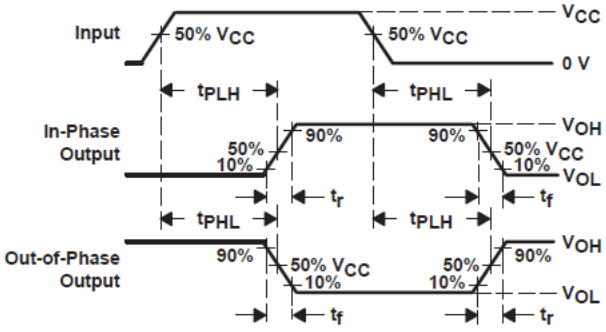
VOLTAGE WAVEFORMS
PULSE DURATION



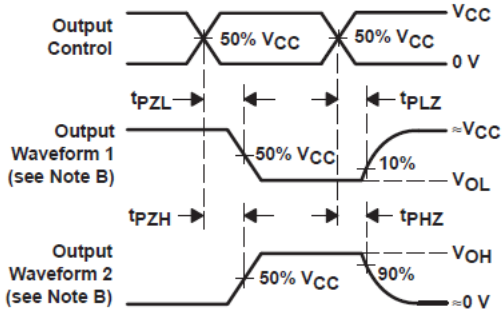
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

図 6-2. CD74HCT4511

7 Detailed Description

7.1 Overview

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs (D_0–D_3), an active-low blanking ($\overline{BL}$) input, lamp-test ($\overline{LT}$) input, and a latch-enable ($\overline{LE}$) input that, when high, enables the latches to store the BCD inputs. When $\overline{LE}$ is low, the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors, but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

7.2 Functional Block Diagram

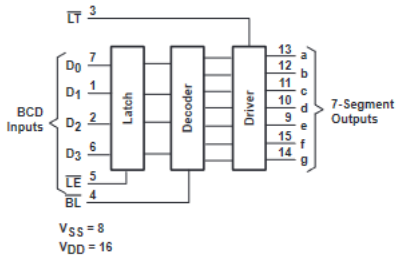


図 7-1. Function Diagram

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS(1)							OUTPUTS(2)							
$\overline{LE}$	$\overline{BL}$	$\overline{LT}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	t	t	t	t	t	t	t	t

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't caret = Depends on BCD code previously applied when $\overline{LE}$ = LNOTE: Display is blank for all illegal input codes (BCD > HLLH).
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

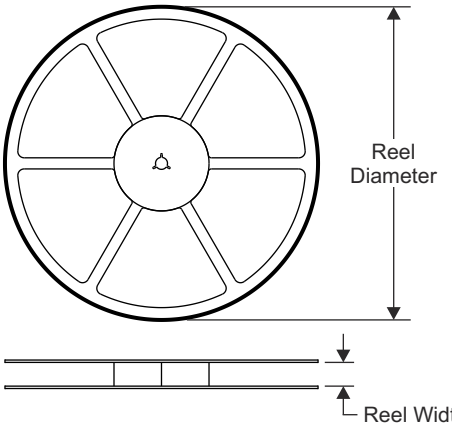
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

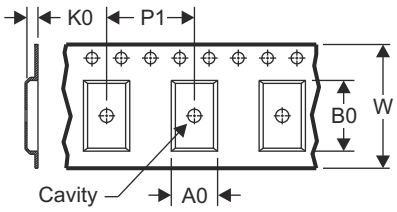
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

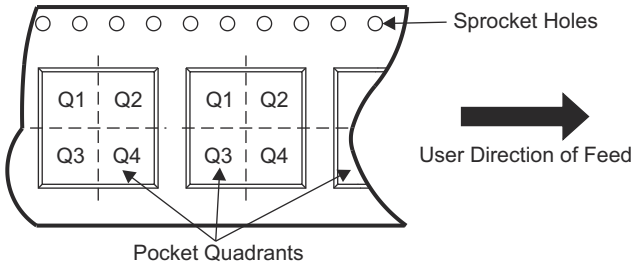


TAPE DIMENSIONS



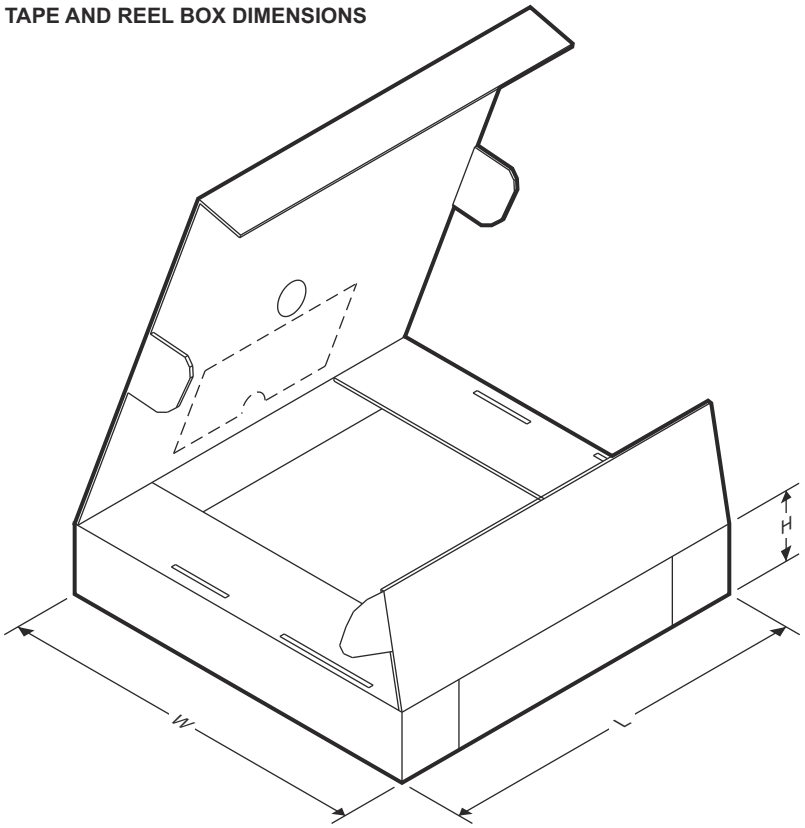
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



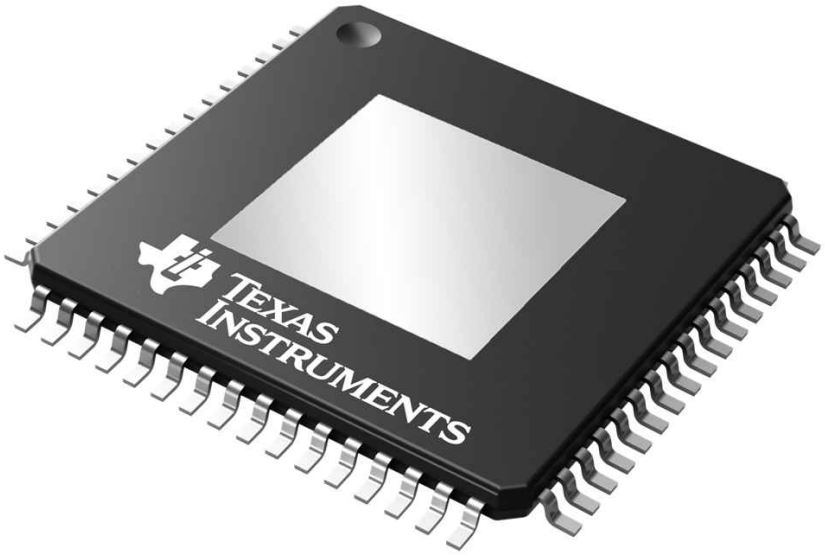
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTAS6584QDKQQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTAS6584QPHDRQ1	HTQFP	PHD	64	1000	350.0	350.0	43.0

11.2 Mechanical Data

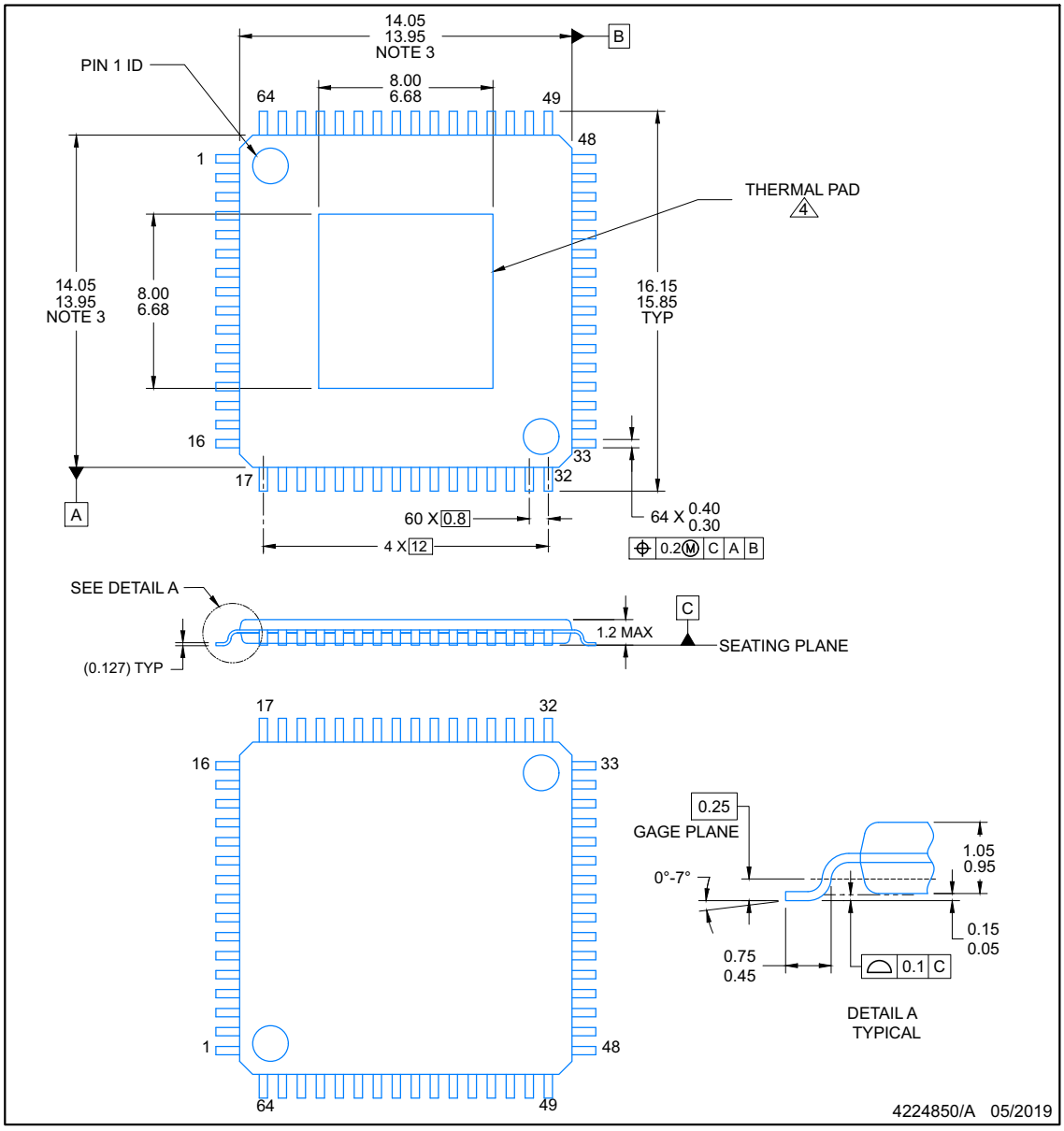


PACKAGE OUTLINE

PHD0064B

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



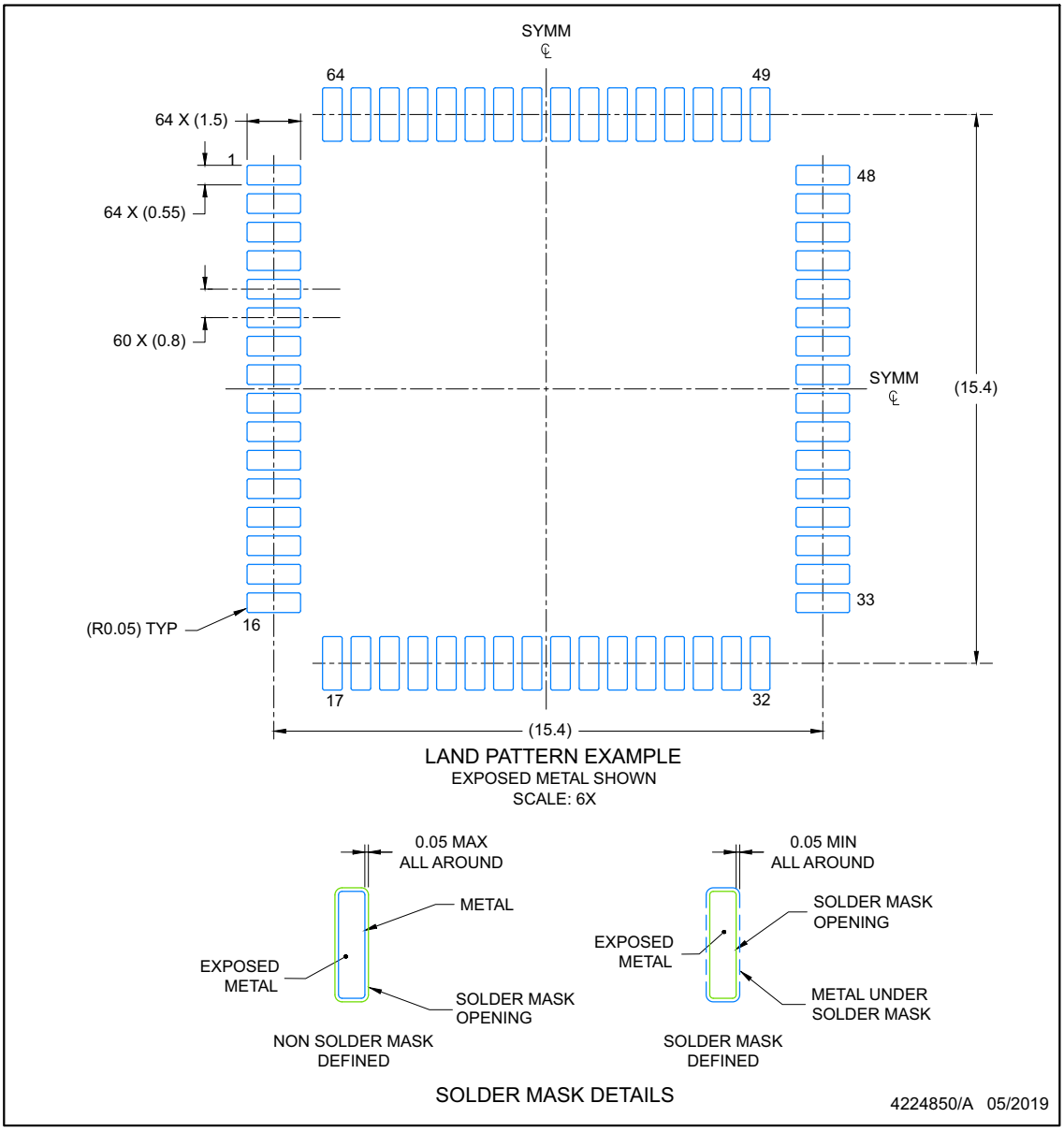
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.

EXAMPLE BOARD LAYOUT

PHD0064B — **HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



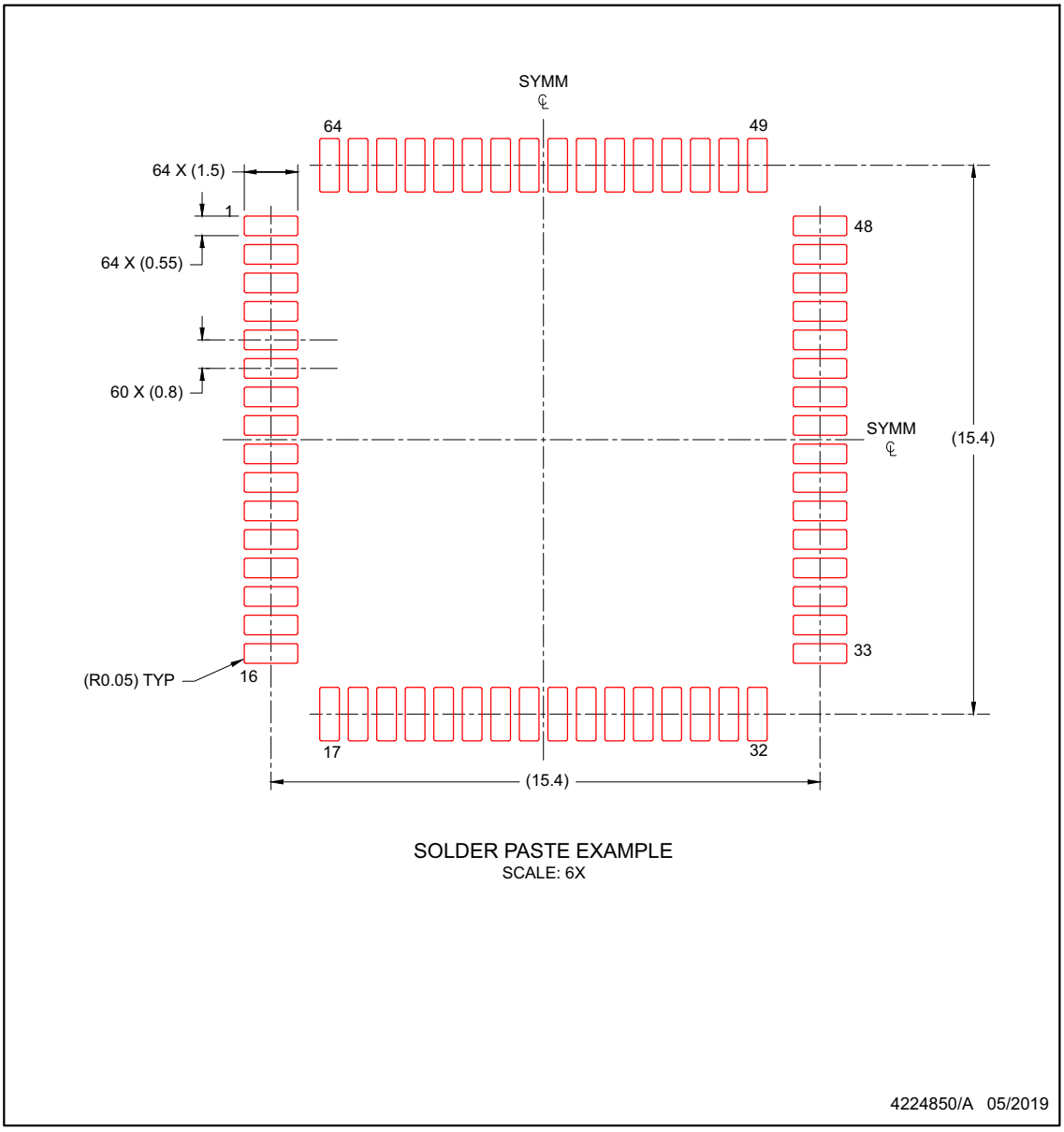
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PHD0064B — **HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE: 6X

4224850/A 05/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8773301EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A
CD54HC4511F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A
CD54HC4511F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A
CD74HC4511E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4511E
CD74HC4511E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4511E
CD74HC4511EE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4511E
CD74HC4511M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4511M
CD74HC4511M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC4511M
CD74HC4511M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M
CD74HC4511M96G4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M
CD74HC4511PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWRE4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4511
CD74HCT4511E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4511E
CD74HCT4511E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4511E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4511, CD74HC4511 :

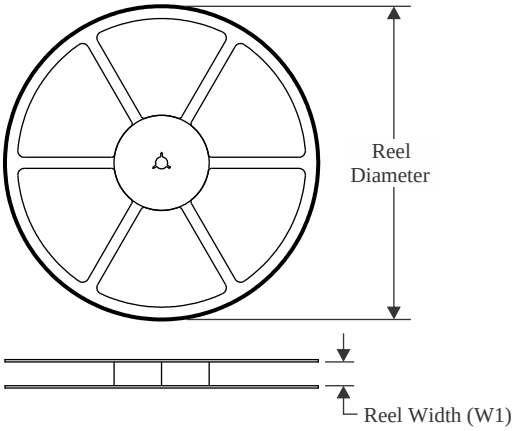
- Catalog : CD74HC4511
- Military : CD54HC4511

NOTE: Qualified Version Definitions:

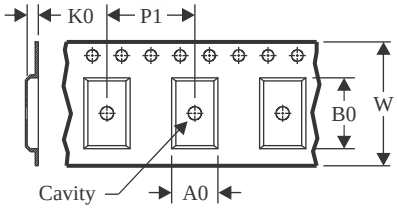
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

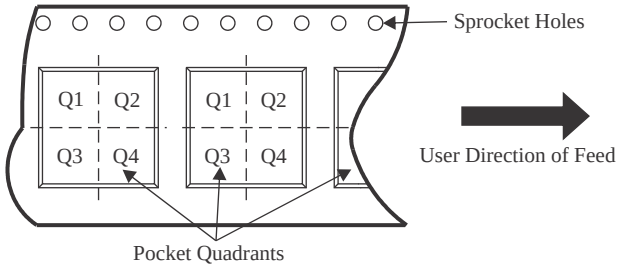


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

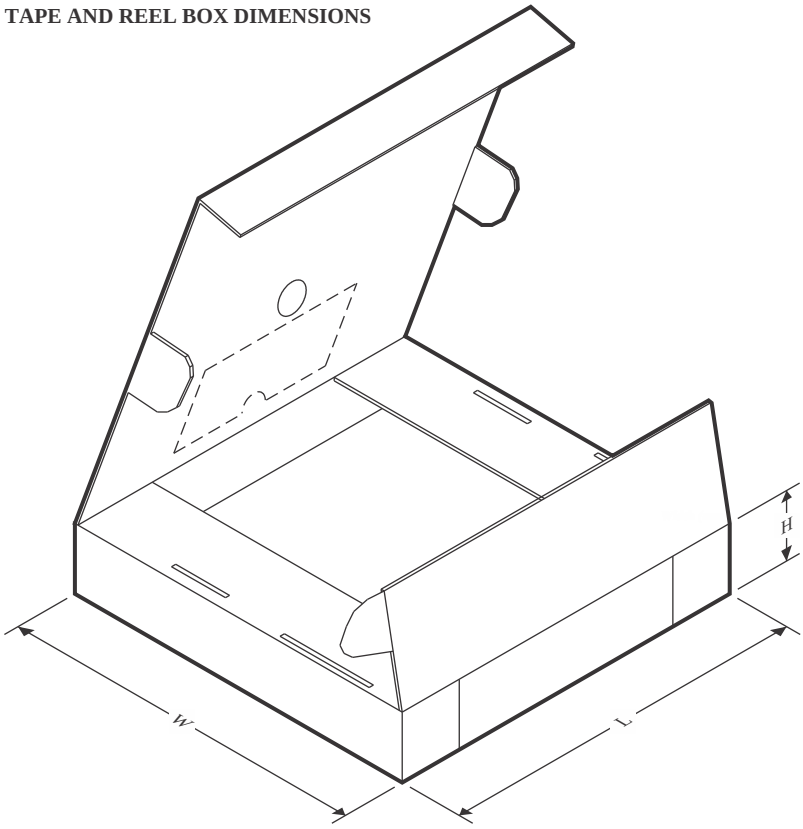
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4511M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4511M96	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC4511PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

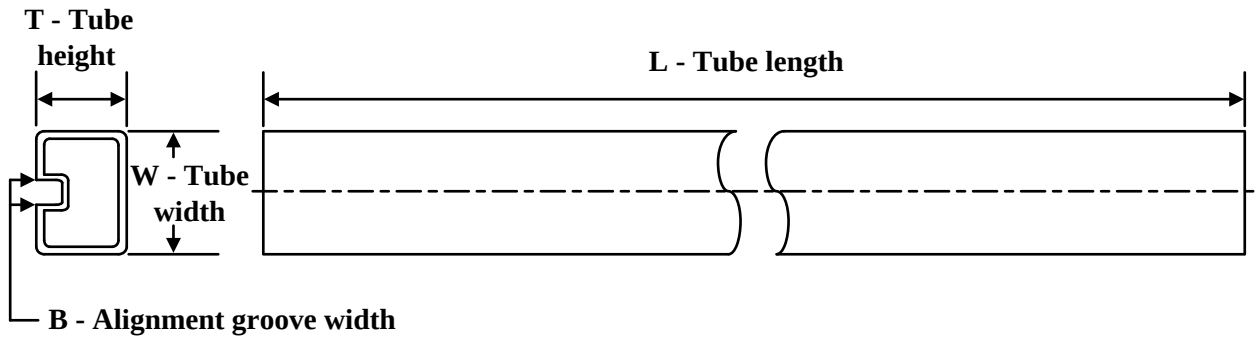
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4511M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC4511M96	SOIC	D	16	2500	366.0	364.0	50.0
CD74HC4511PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

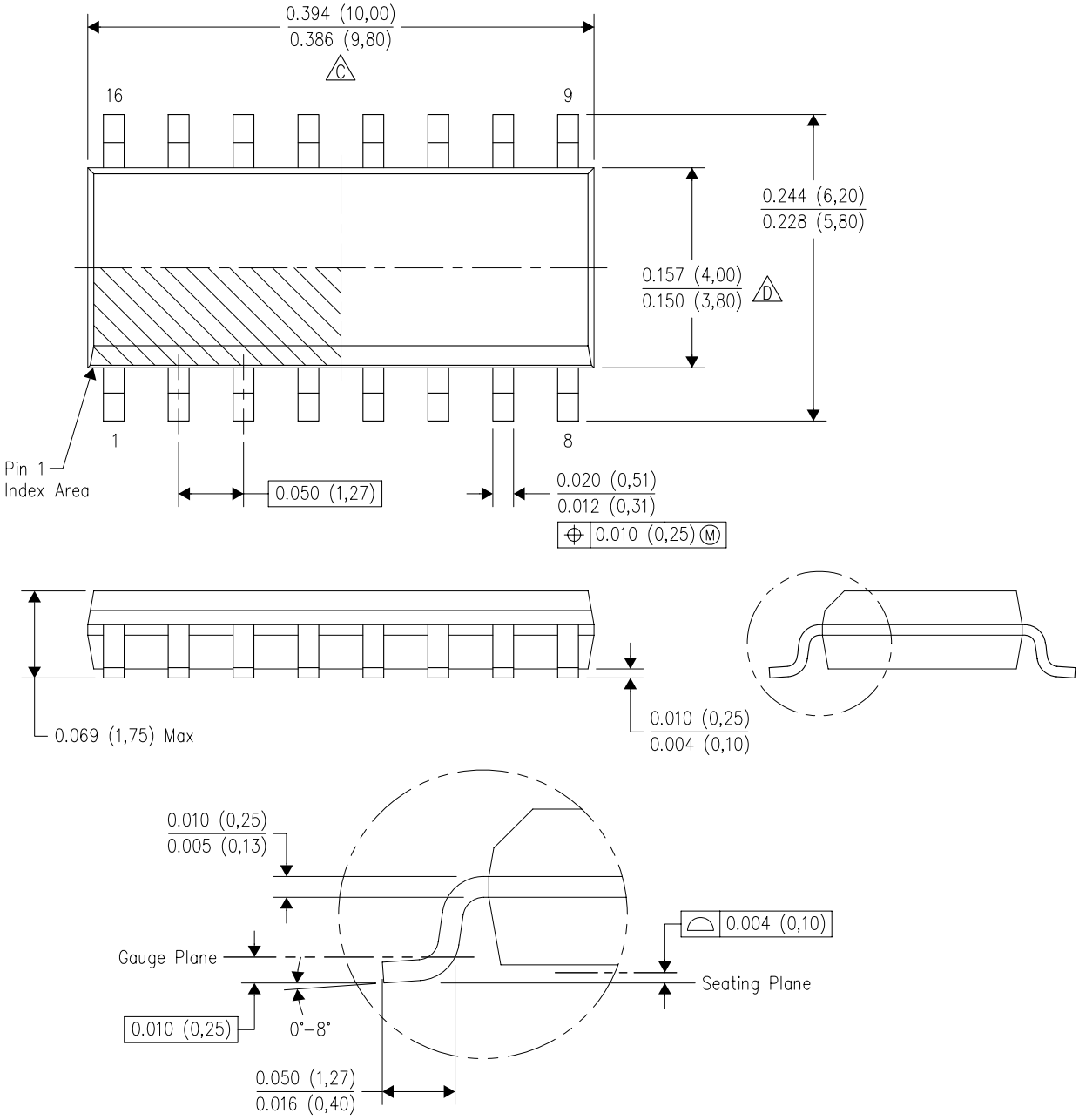
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



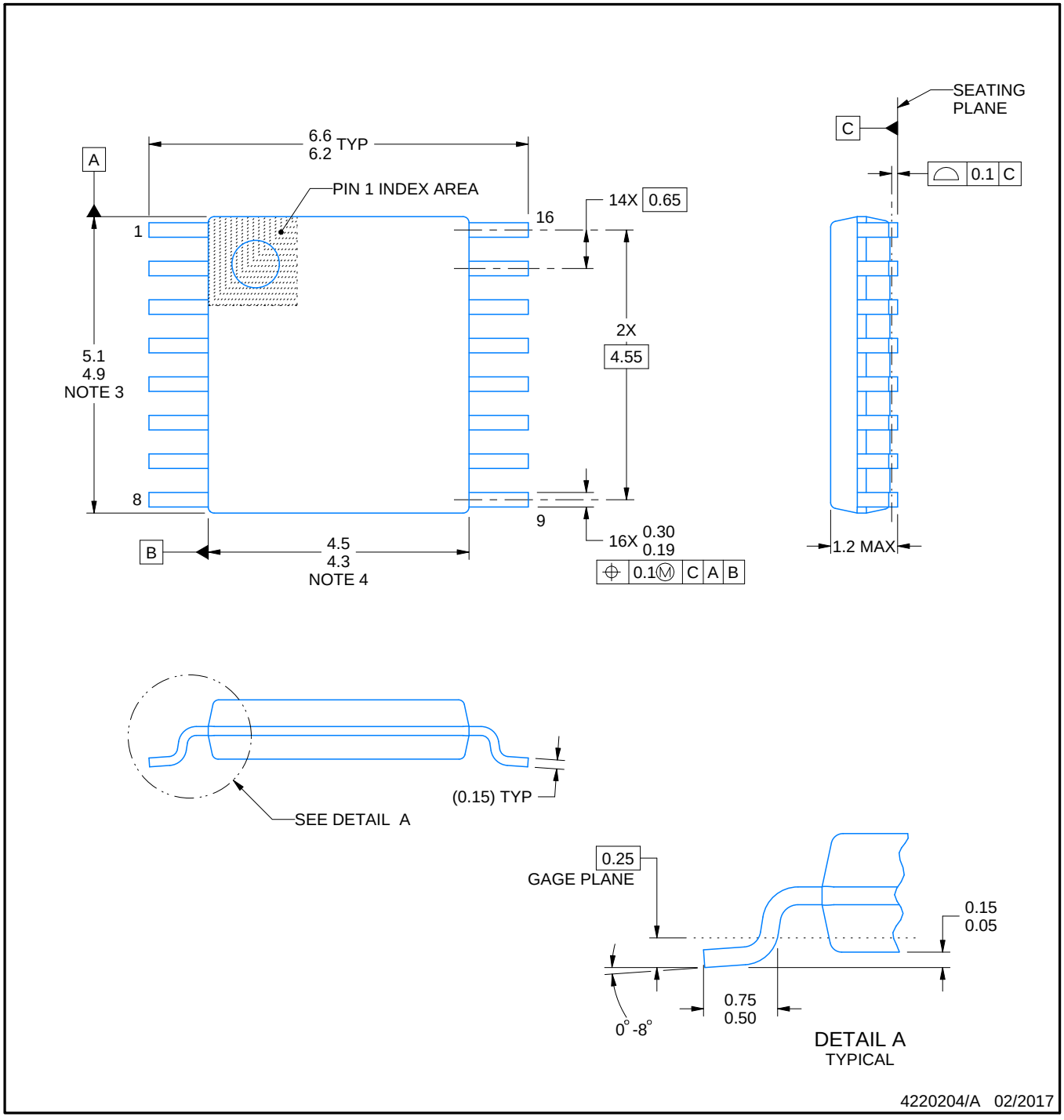
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

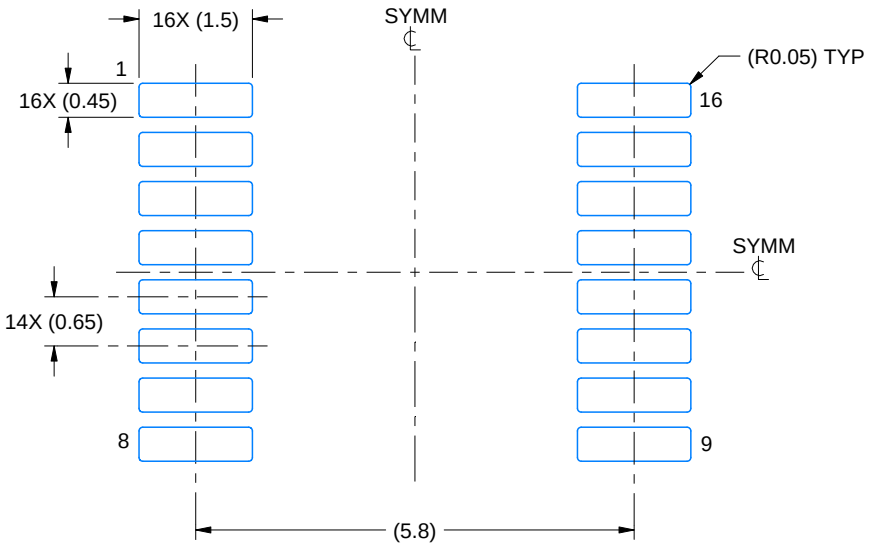
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

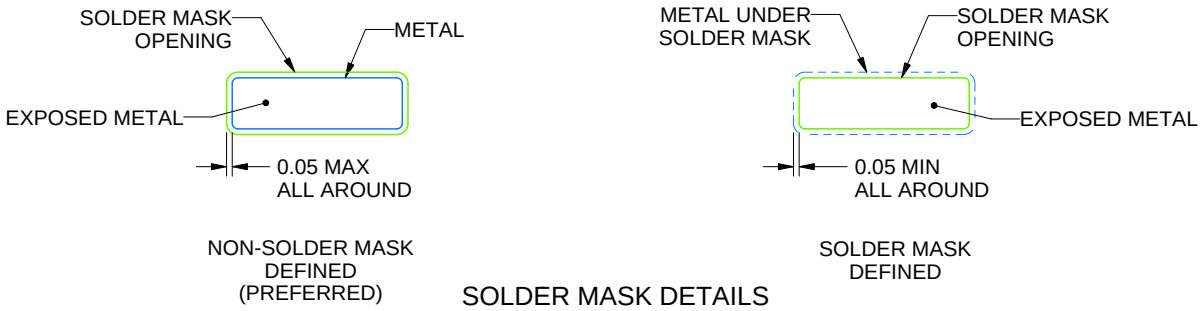


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

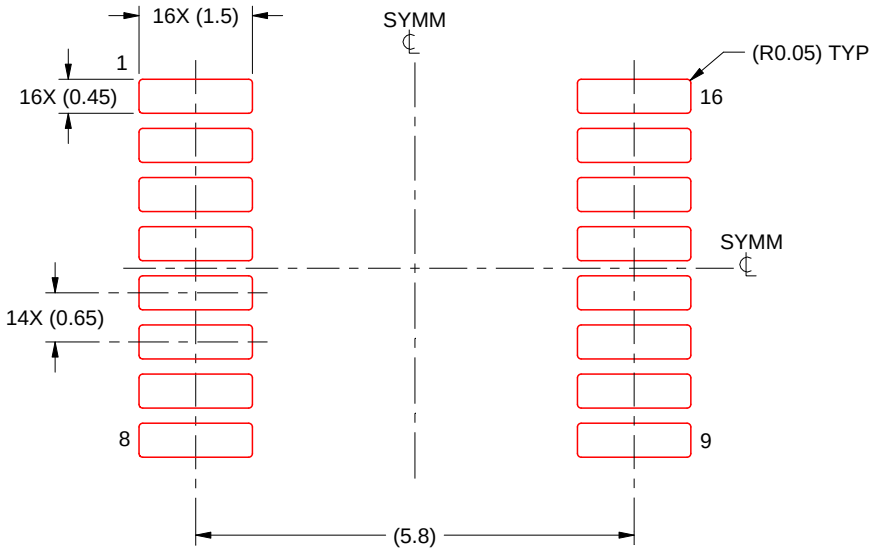


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

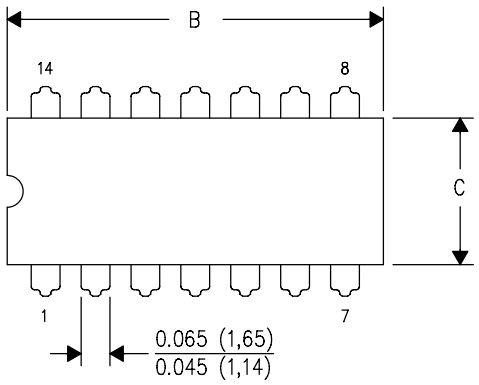
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

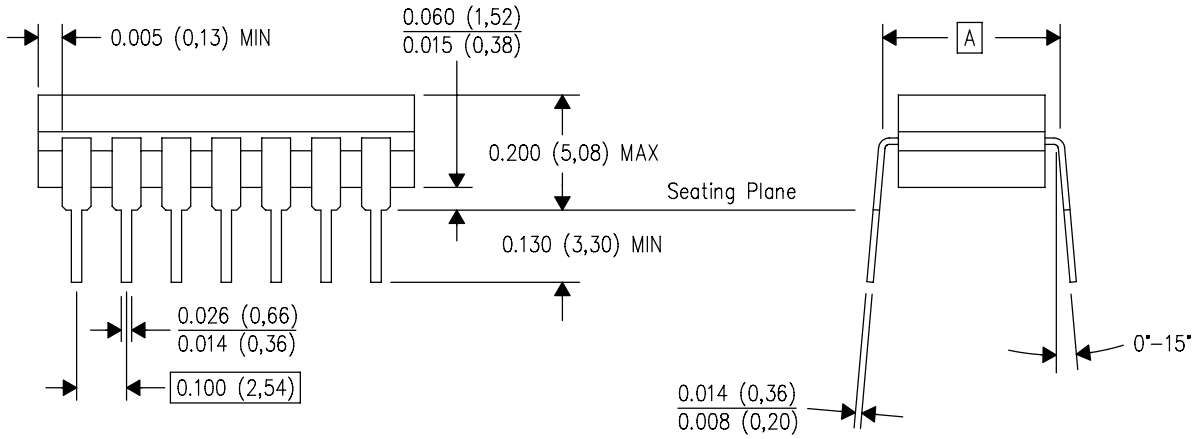
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



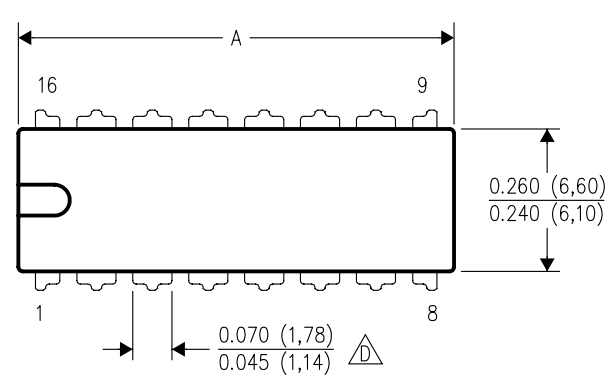
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

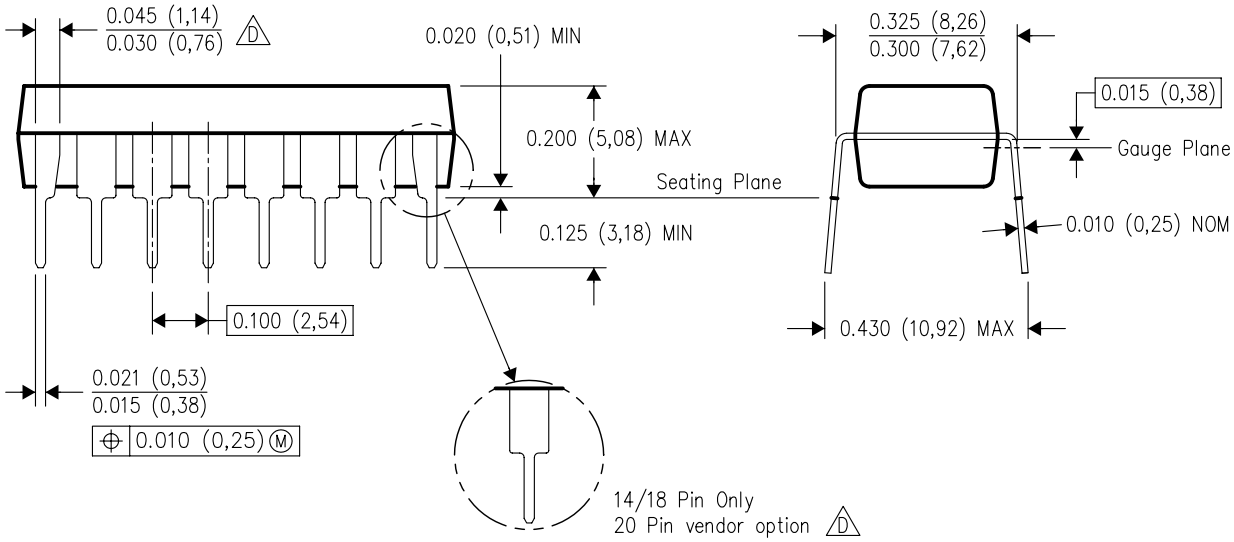
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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