



CD54HC240, CD74HC240, CD74HC241, CD54HC244  
 CD74HC244, CD54HCT240, CD74HCT240, CD54HCT241  
 CD74HCT241, CD54HCT244, CD74HCT244

JAJSNX1G – NOVEMBER 1998 – REVISED OCTOBER 2022

# CDx4HC240、CDx4HCT240、CD74HC241、CDx4HCT241、CDx4HC244、CDx4HCT244 ハイスピード CMOS ロジック・オクタール・バッファ/ライン・ドライバ、3 ステート

## 1 特長

- HC/HCT240 反転
- HC/HCT241 非反転
- HC/HCT244 非反転
- 8ns の伝搬遅延 (標準値、 $V_{CC} = 5V$ 、 $C_L = 15pF$ 、 $T_A = 25^\circ C$ 、HC240 の場合)
- 3 ステート出力
- バッファ付き入力
- 大電流バス・ドライバ出力
- ファンアウト (全温度範囲にわたって)
  - 標準出力: 10 個の LSTTL 負荷
  - バス・ドライバ出力: 15 個の LSTTL 負荷
- 広い動作温度範囲:  $-55^\circ C \sim 125^\circ C$
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ:
  - 2V~6V で動作
  - 優れたノイズ耐性:  $V_{CC}$  に対して  $N_{IL} = 30\%$ 、 $N_{IH} = 30\%$  ( $V_{CC} = 5V$  時)
- HCT タイプ:
  - 4.5V~5.5V で動作
  - LSTTL 入力ロジックと直接互換、 $V_{IL} = 0.8V$  (最大値)、 $V_{IH} = 2V$  (最小値)
  - CMOS 入力互換、 $V_{OL}$ 、 $V_{OH}$  で  $I_L \leq 1\mu A$

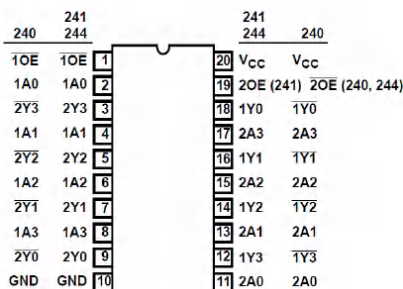
## 2 概要

'HC240 と 'HCT240 は、2 つのアクティブ Low 出力イネーブルを備えた反転 3 ステート・バッファです。CD74HC241、'HCT241、'HC244、'HCT244 は、非反転 3 ステート・バッファです。241 は 1 つのアクティブ High 出力イネーブルと 1 つのアクティブ Low 出力イネーブルを備えており、244 は 2 つのアクティブ Low 出力イネーブルを備えていることが異なります。3 つのタイプはすべて同じピン配置です。

### パッケージ情報

| 部品番号       | パッケージ <sup>(1)</sup> | 本体サイズ (公称)       |
|------------|----------------------|------------------|
| CD74HC240  | M (SOIC, 20)         | 12.80mm × 7.50mm |
|            | E (PDIP, 20)         | 25.40mm × 6.35mm |
| CD54HC240  | F (CDIP, 20)         | 26.92mm × 6.92mm |
| CD74HCT240 | M (SOIC, 20)         | 12.80mm × 7.50mm |
|            | E (PDIP, 20)         | 25.40mm × 6.35mm |
|            | PW (TSSOP, 20)       | 6.50mm × 4.40mm  |
| CD54HCT240 | F (CDIP, 20)         | 26.92mm × 6.92mm |
| CD74HC241  | M (SOIC, 20)         | 12.80mm × 7.50mm |
|            | E (PDIP, 20)         | 25.40mm × 6.35mm |
| CD74HCT241 | M (SOIC, 20)         | 12.80mm × 7.50mm |
|            | E (PDIP, 20)         | 25.40mm × 6.35mm |
| CD54HCT241 | F (CDIP, 20)         | 26.92mm × 6.92mm |
| CD74HC244  | M (SOIC, 20)         | 12.80mm × 7.50mm |
|            | E (PDIP, 20)         | 25.40mm × 6.35mm |
| CD54HC244  | F (CDIP, 20)         | 26.92mm × 6.92mm |
| CD74HCT244 | M (SOIC, 20)         | 12.80mm × 7.50mm |
|            | E (PDIP, 20)         | 25.40mm × 6.35mm |
| CD54HCT244 | F (CDIP, 20)         | 26.92mm × 6.92mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ピン配置図



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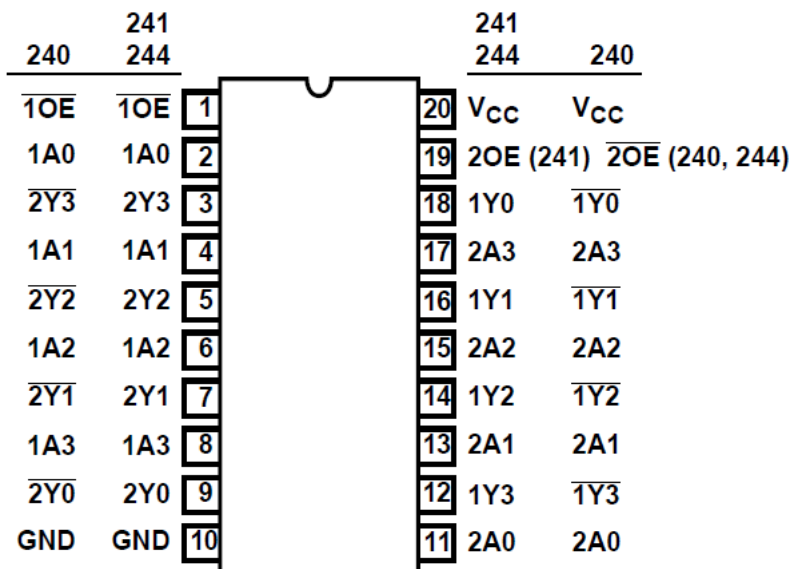
## 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| <b>Changes from Revision E (October 2004) to Revision F (February 2022)</b> | <b>Page</b> |
|-----------------------------------------------------------------------------|-------------|
| • 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新.....                         | 1           |

| <b>Changes from Revision F (February 2022) to Revision G (October 2022)</b>                                                 | <b>Page</b> |
|-----------------------------------------------------------------------------------------------------------------------------|-------------|
| • Increased RθJA for packages: DW (73 to 109.1); DB (82 to 122.7); N (67 to 84.6); NS (64 to 113.4); PW (108 to 131.8)..... | 4           |

## 4 Pin Configuration and Functions



J, N, DW, or PW package  
20-Pin CDIP, PDIP, SOIC, or TSSOP  
Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

|                  |                                                          |                                                                         | MIN  | MAX | UNIT |
|------------------|----------------------------------------------------------|-------------------------------------------------------------------------|------|-----|------|
| V <sub>CC</sub>  | Supply voltage                                           |                                                                         | –0.5 | 7   | V    |
| I <sub>IK</sub>  | Input clamp diode current                                | For V <sub>I</sub> < –0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V |      | ±20 | mA   |
| I <sub>OK</sub>  | Output clamp diode current                               | For V <sub>O</sub> < –0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V |      | ±20 | mA   |
| I <sub>O</sub>   | Drain current, per output                                | For –0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V                   |      | ±35 | mA   |
| I <sub>O</sub>   | Output source or sink current per output pin             | For V <sub>O</sub> > –0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V |      | ±25 | mA   |
| I <sub>CC</sub>  | Continuous current through V <sub>CC</sub> or GND        |                                                                         |      | ±70 | mA   |
| T <sub>J</sub>   | Junction temperature                                     |                                                                         |      | 150 | °C   |
| T <sub>stg</sub> | Storage temperature range                                |                                                                         | –65  | 150 | °C   |
|                  | Lead temperature (Soldering 10s) (SOIC - lead tips only) |                                                                         |      | 300 | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

|                                 |                          |           | MIN | MAX             | UNIT |
|---------------------------------|--------------------------|-----------|-----|-----------------|------|
| V <sub>CC</sub>                 | Supply voltage range     | HC types  | 2   | 6               | V    |
|                                 |                          | HCT types | 4.5 | 5.5             |      |
| V <sub>I</sub> , V <sub>O</sub> | Input or output voltage  |           | 0   | V <sub>CC</sub> | V    |
| t <sub>t</sub>                  | Input rise and fall time | 2 V       |     | 1000            | ns   |
|                                 |                          | 4.5 V     |     | 500             |      |
|                                 |                          | 6 V       |     | 400             |      |
| T <sub>A</sub>                  | Temperature range        |           | –55 | 125             | °C   |

### 5.3 Thermal Information

| THERMAL METRIC         |                                                       | DW (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|------------------------|-------------------------------------------------------|-----------|-----------|----------|---------|------------|------|
|                        |                                                       | 20 PINS   | 20 PINS   | 20 PINS  | 20 PINS | 20 PINS    |      |
| R <sub>θJA</sub>       | Junction-to-ambient thermal resistance <sup>(1)</sup> | 109.1     | 122.7     | 84.6     | 113.4   | 131.8      | °C/W |
| R <sub>θJC (top)</sub> | Junction-to-case (top) thermal resistance             | 76        | 81.6      | 72.5     | 78.6    | 72.2       | °C/W |
| R <sub>θJB</sub>       | Junction-to-board thermal resistance                  | 77.6      | 77.5      | 65.3     | 78.4    | 82.8       | °C/W |
| Ψ <sub>JT</sub>        | Junction-to-top characterization parameter            | 51.5      | 46.1      | 55.3     | 47.1    | 21.5       | °C/W |
| Ψ <sub>JB</sub>        | Junction-to-board characterization parameter          | 77.1      | 77.1      | 65.2     | 78.1    | 82.4       | °C/W |
| R <sub>θJC (bot)</sub> | Junction-to-case (bottom) thermal resistance          | N/A       | N/A       | N/A      | N/A     | N/A        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics '240

| PARAMETER                       |                                         | TEST CONDITIONS <sup>(2)</sup>                         | V <sub>CC</sub> (V) | 25°C |     |      | –40°C to 85°C |     | –55°C to 125°C |     | UNIT |
|---------------------------------|-----------------------------------------|--------------------------------------------------------|---------------------|------|-----|------|---------------|-----|----------------|-----|------|
|                                 |                                         |                                                        |                     | MIN  | TYP | MAX  | MIN           | MAX | MIN            | MAX |      |
| HC TYPES                        |                                         |                                                        |                     |      |     |      |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |                                                        | 2                   | 1.5  |     | 1.5  |               | 1.5 |                | V   |      |
|                                 |                                         |                                                        | 4.5                 | 3.15 |     | 3.15 |               |     |                |     |      |
|                                 |                                         |                                                        | 6                   | 4.2  |     | 4.2  |               |     |                |     |      |
| V <sub>IL</sub>                 | Low level input voltage                 |                                                        | 2                   | 0.5  |     | 0.5  |               | 0.5 |                | V   |      |
|                                 |                                         |                                                        | 4.5                 | 1.35 |     | 1.35 |               |     |                |     |      |
|                                 |                                         |                                                        | 6                   | 1.8  |     | 1.8  |               |     |                |     |      |
| V <sub>OH</sub>                 | High level output voltage               | I <sub>OH</sub> = – 20 µA                              | 2                   | 1.9  |     | 1.9  |               | 1.9 |                | V   |      |
|                                 |                                         | I <sub>OH</sub> = – 20 µA                              | 4.5                 | 4.4  |     | 4.4  |               |     |                |     |      |
|                                 |                                         | I <sub>OH</sub> = – 20 µA                              | 6                   | 5.9  |     | 5.9  |               |     |                |     |      |
|                                 | High level output voltage               | I <sub>OH</sub> = – 6 mA                               | 4.5                 | 3.98 |     | 3.84 |               | 3.7 |                |     |      |
|                                 |                                         | I <sub>OH</sub> = – 7.8 mA                             | 6                   | 5.48 |     | 5.34 |               | 5.2 |                |     |      |
| V <sub>OL</sub>                 | Low level output voltage                | I <sub>OL</sub> = 20 µA                                | 2                   | 0.1  |     | 0.1  |               | 0.1 |                | V   |      |
|                                 |                                         | I <sub>OL</sub> = 20 µA                                | 4.5                 | 0.1  |     | 0.1  |               | 0.1 |                |     |      |
|                                 |                                         | I <sub>OL</sub> = 20 µA                                | 6                   | 0.1  |     | 0.1  |               | 0.1 |                |     |      |
|                                 | Low level output voltage                | I <sub>OL</sub> = 6 mA                                 | 4.5                 | 0.26 |     | 0.33 |               | 0.4 |                |     |      |
|                                 |                                         | I <sub>OL</sub> = 7.8 mA                               | 6                   | 0.26 |     | 0.33 |               | 0.4 |                |     |      |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND                | 6                   | ±0.1 |     | ±1   |               | ±1  |                | µA  |      |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND                | 6                   | 8    |     | 80   |               | 160 |                | µA  |      |
| I <sub>OZ</sub>                 | Three-state leakage current             |                                                        | 6                   | ±0.5 |     | ±0.5 |               | ±10 |                | µA  |      |
| HCT TYPES                       |                                         |                                                        |                     |      |     |      |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |                                                        | 4.5 to 5.5          | 2    |     | 2    |               | 2   |                | V   |      |
| V <sub>IL</sub>                 | Low level input voltage                 |                                                        | 4.5 to 5.5          | 0.8  |     | 0.8  |               | 0.8 |                | V   |      |
| V <sub>OH</sub>                 | High level output voltage               | V <sub>OH</sub> = – 20 µA                              | 4.5                 | 4.4  |     | 4.4  |               | 4.4 |                | V   |      |
|                                 | High level output voltage               | V <sub>OH</sub> = – 6 mA                               | 4.5                 | 3.98 |     | 3.84 |               | 3.7 |                |     |      |
| V <sub>OL</sub>                 | Low level output voltage                | V <sub>OL</sub> = 20 µA                                | 4.5                 | 0.1  |     | 0.1  |               | 0.1 |                | V   |      |
|                                 | Low level output voltage                | V <sub>OL</sub> = 6 mA                                 | 4.5                 | 0.26 |     | 0.33 |               | 0.4 |                |     |      |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND                | 5.5                 | ±0.1 |     | ±1   |               | ±1  |                | µA  |      |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND                | 5.5                 | 8    |     | 80   |               | 160 |                | µA  |      |
| I <sub>OZ</sub>                 | Three-state leakage current             |                                                        | 5.5                 | ±0.5 |     | ±5   |               | ±10 |                | µA  |      |
| ΔI <sub>CC</sub> <sup>(1)</sup> | Additional supply current per input pin | nA0 - A3 inputs held at V <sub>CC</sub> – 2.1          | 4.5 to 5.5          | 100  | 540 | 675  |               | 735 |                | µA  |      |
|                                 |                                         | 1 $\overline{O}E$ inputs held at V <sub>CC</sub> – 2.1 | 4.5 to 5.5          | 100  | 252 | 315  |               | 343 |                | µA  |      |
|                                 |                                         | 2 $\overline{O}E$ inputs held at V <sub>CC</sub> – 2.1 | 4.5 to 5.5          | 100  | 252 | 315  |               | 343 |                | µA  |      |

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.5 Electrical Characteristics '241

| PARAMETER                       |                                         | TEST CONDITIONS <sup>(2)</sup>                | V <sub>CC</sub> (V) | 25°C    |     |     | –40°C to 85°C |     | –55°C to 125°C |     | UNIT |
|---------------------------------|-----------------------------------------|-----------------------------------------------|---------------------|---------|-----|-----|---------------|-----|----------------|-----|------|
|                                 |                                         |                                               |                     | MIN     | TYP | MAX | MIN           | MAX | MIN            | MAX |      |
| HC TYPES                        |                                         |                                               |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |                                               | 2                   | 1.5     |     |     | 1.5           |     | 1.5            |     | V    |
|                                 |                                         |                                               | 4.5                 | 3.15    |     |     | 3.15          |     | 3.15           |     |      |
|                                 |                                         |                                               | 6                   | 4.2     |     |     | 4.2           |     | 4.2            |     |      |
| V <sub>IL</sub>                 | Low level input voltage                 |                                               | 2                   | 0.5     |     |     | 0.5           |     | 0.5            |     | V    |
|                                 |                                         |                                               | 4.5                 | 1.35    |     |     | 1.35          |     | 1.35           |     |      |
|                                 |                                         |                                               | 6                   | 1.8     |     |     | 1.8           |     | 1.8            |     |      |
| V <sub>OH</sub>                 | High level output voltage               | I <sub>OH</sub> = – 20 μA                     | 2                   | 1.9     |     |     | 1.9           |     | 1.9            |     | V    |
|                                 |                                         | I <sub>OH</sub> = – 20 μA                     | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     |      |
|                                 |                                         | I <sub>OH</sub> = – 20 μA                     | 6                   | 5.9     |     |     | 5.9           |     | 5.9            |     |      |
|                                 | High level output voltage               | I <sub>OH</sub> = – 6 mA                      | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     |      |
|                                 |                                         | I <sub>OH</sub> = – 7.8 mA                    | 6                   | 5.48    |     |     | 5.34          |     | 5.2            |     |      |
| V <sub>OL</sub>                 | Low level output voltage                | I <sub>OL</sub> = 20 μA                       | 2                   | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 |                                         | I <sub>OL</sub> = 20 μA                       | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     |      |
|                                 |                                         | I <sub>OL</sub> = 20 μA                       | 6                   | 0.1     |     |     | 0.1           |     | 0.1            |     |      |
|                                 | Low level output voltage                | I <sub>OL</sub> = 6 mA                        | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     |      |
|                                 |                                         | I <sub>OL</sub> = 7.8 mA                      | 6                   | 0.26    |     |     | 0.33          |     | 0.4            |     |      |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND       | 6                   | ±0.1    |     |     | ±1            |     | ±1             |     | μA   |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND       | 6                   | 8       |     |     | 80            |     | 160            |     | μA   |
| I <sub>OZ</sub>                 | Three-state leakage current             |                                               | 6                   | ±0.5    |     |     | ±0.5          |     | ±10            |     | μA   |
| HCT TYPES                       |                                         |                                               |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |                                               | 4.5 to 5.5          | 2       |     |     | 2             |     | 2              |     | V    |
| V <sub>IL</sub>                 | Low level input voltage                 |                                               | 4.5 to 5.5          | 0.8     |     |     | 0.8           |     | 0.8            |     | V    |
| V <sub>OH</sub>                 | High level output voltage               | V <sub>OH</sub> = – 20 μA                     | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     | V    |
|                                 | High level output voltage               | V <sub>OH</sub> = – 6 mA                      | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     |      |
| V <sub>OL</sub>                 | Low level output voltage                | V <sub>OL</sub> = 20 μA                       | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 | Low level output voltage                | V <sub>OL</sub> = 6 mA                        | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     |      |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND       | 5.5                 | ±0.1    |     |     | ±1            |     | ±1             |     | μA   |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND       | 5.5                 | 8       |     |     | 80            |     | 160            |     | μA   |
| I <sub>OZ</sub>                 | Three-state leakage current             |                                               | 5.5                 | ±0.5    |     |     | ±5            |     | ±10            |     | μA   |
| ΔI <sub>CC</sub> <sup>(1)</sup> | Additional supply current per input pin | nA0 - A3 inputs held at V <sub>CC</sub> – 2.1 | 4.5 to 5.5          | 100 252 |     |     | 315           |     | 343            |     | μA   |
|                                 |                                         | 1OE inputs held at V <sub>CC</sub> – 2.1      | 4.5 to 5.5          | 100 252 |     |     | 315           |     | 343            |     | μA   |
|                                 |                                         | 2OE inputs held at V <sub>CC</sub> – 2.1      | 4.5 to 5.5          | 100 540 |     |     | 675           |     | 735            |     | μA   |

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.6 Electrical Characteristics '244

| PARAMETER                       |                                         | TEST CONDITIONS <sup>(2)</sup>                         | V <sub>CC</sub> (V) | 25°C    |     |     | –40°C to 85°C |     | –55°C to 125°C |     | UNIT |
|---------------------------------|-----------------------------------------|--------------------------------------------------------|---------------------|---------|-----|-----|---------------|-----|----------------|-----|------|
|                                 |                                         |                                                        |                     | MIN     | TYP | MAX | MIN           | MAX | MIN            | MAX |      |
| HC TYPES                        |                                         |                                                        |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |                                                        | 2                   | 1.5     |     |     | 1.5           |     | 1.5            |     | V    |
|                                 |                                         |                                                        | 4.5                 | 3.15    |     |     | 3.15          |     | 3.15           |     |      |
|                                 |                                         |                                                        | 6                   | 4.2     |     |     | 4.2           |     | 4.2            |     |      |
| V <sub>IL</sub>                 | Low level input voltage                 |                                                        | 2                   | 0.5     |     |     | 0.5           |     | 0.5            |     | V    |
|                                 |                                         |                                                        | 4.5                 | 1.35    |     |     | 1.35          |     | 1.35           |     |      |
|                                 |                                         |                                                        | 6                   | 1.8     |     |     | 1.8           |     | 1.8            |     |      |
| V <sub>OH</sub>                 | High level output voltage               | I <sub>OH</sub> = – 20 µA                              | 2                   | 1.9     |     |     | 1.9           |     | 1.9            |     | V    |
|                                 |                                         | I <sub>OH</sub> = – 20 µA                              | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     |      |
|                                 |                                         | I <sub>OH</sub> = – 20 µA                              | 6                   | 5.9     |     |     | 5.9           |     | 5.9            |     |      |
|                                 | High level output voltage               | I <sub>OH</sub> = – 6 mA                               | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     |      |
|                                 |                                         | I <sub>OH</sub> = – 7.8 mA                             | 6                   | 5.48    |     |     | 5.34          |     | 5.2            |     |      |
| V <sub>OL</sub>                 | Low level output voltage                | I <sub>OL</sub> = 20 µA                                | 2                   | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 |                                         | I <sub>OL</sub> = 20 µA                                | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     |      |
|                                 |                                         | I <sub>OL</sub> = 20 µA                                | 6                   | 0.1     |     |     | 0.1           |     | 0.1            |     |      |
|                                 | Low level output voltage                | I <sub>OL</sub> = 6 mA                                 | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     |      |
|                                 |                                         | I <sub>OL</sub> = 7.8 mA                               | 6                   | 0.26    |     |     | 0.33          |     | 0.4            |     |      |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND                | 6                   | ±0.1    |     |     | ±1            |     | ±1             |     | µA   |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND                | 6                   | 8       |     |     | 80            |     | 160            |     | µA   |
| I <sub>OZ</sub>                 | Three-state leakage current             |                                                        | 6                   | ±0.5    |     |     | ±0.5          |     | ±10            |     | µA   |
| HCT TYPES                       |                                         |                                                        |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |                                                        | 4.5 to 5.5          | 2       |     |     | 2             |     | 2              |     | V    |
| V <sub>IL</sub>                 | Low level input voltage                 |                                                        | 4.5 to 5.5          | 0.8     |     |     | 0.8           |     | 0.8            |     | V    |
| V <sub>OH</sub>                 | High level output voltage               | V <sub>OH</sub> = – 20 µA                              | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     | V    |
|                                 | High level output voltage               | V <sub>OH</sub> = – 6 mA                               | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     |      |
| V <sub>OL</sub>                 | Low level output voltage                | V <sub>OL</sub> = 20 µA                                | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 | Low level output voltage                | V <sub>OL</sub> = 6 mA                                 | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     |      |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND                | 5.5                 | ±0.1    |     |     | ±1            |     | ±1             |     | µA   |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND                | 5.5                 | 8       |     |     | 80            |     | 160            |     | µA   |
| I <sub>OZ</sub>                 | Three-state leakage current             |                                                        | 5.5                 | ±0.5    |     |     | ±5            |     | ±10            |     | µA   |
| ΔI <sub>CC</sub> <sup>(1)</sup> | Additional supply current per input pin | nA0 - A3 inputs held at V <sub>CC</sub> – 2.1          | 4.5 to 5.5          | 100 252 |     |     | 315           |     | 343            |     | µA   |
|                                 |                                         | 1 $\overline{O}E$ inputs held at V <sub>CC</sub> – 2.1 | 4.5 to 5.5          | 100 252 |     |     | 315           |     | 343            |     | µA   |
|                                 |                                         | 2 $\overline{O}E$ inputs held at V <sub>CC</sub> – 2.1 | 4.5 to 5.5          | 100 252 |     |     | 315           |     | 343            |     | µA   |

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.7 Switching Characteristics '240

$C_L = 50 \text{ pF}$ , Input  $t_r$ ,  $t_f = 6 \text{ ns}$

| PARAMETER                              |                                                     | V <sub>CC</sub> (V) | 25°C                |     |     | –40°C to 85°C |     |     | –55°C to 125°C |     |     | UNIT |
|----------------------------------------|-----------------------------------------------------|---------------------|---------------------|-----|-----|---------------|-----|-----|----------------|-----|-----|------|
|                                        |                                                     |                     | MIN                 | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |      |
| HC TYPES                               |                                                     |                     |                     |     |     |               |     |     |                |     |     |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation delay<br>Data to outputs                | 2                   | 100                 |     |     | 125           |     |     | 150            |     |     | ns   |
|                                        |                                                     | 4.5                 | 8 <sup>(3)</sup> 20 |     |     | 25            |     |     | 30             |     |     |      |
|                                        |                                                     | 6                   | 17                  |     |     | 21            |     |     | 26             |     |     |      |
| t <sub>THL</sub> ,<br>t <sub>TLH</sub> | Output enable and disable<br>time                   | 2                   | 150                 |     |     | 190           |     |     | 225            |     |     | ns   |
|                                        |                                                     | 4.5                 | 30                  |     |     | 38            |     |     | 45             |     |     |      |
|                                        |                                                     | 5                   | 12                  |     |     |               |     |     |                |     |     |      |
|                                        |                                                     | 6                   | 26                  |     |     | 33            |     |     | 38             |     |     |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Output transition time                              | 2                   | 60                  |     |     | 75            |     |     | 90             |     |     | ns   |
|                                        |                                                     | 4.5                 | 12                  |     |     | 15            |     |     | 18             |     |     |      |
|                                        |                                                     | 6                   | 10                  |     |     | 13            |     |     | 15             |     |     |      |
| C <sub>I</sub>                         | Input capacitance                                   |                     | 10                  |     |     | 10            |     |     | 10             |     |     | pF   |
| C <sub>O</sub>                         | Three-state output<br>capacitance                   |                     | 20                  |     |     | 20            |     |     | 20             |     |     | pF   |
| C <sub>PD</sub>                        | Power dissipation<br>capacitance <sup>(1) (2)</sup> | 5                   | 38 <sup>(3)</sup>   |     |     |               |     |     |                |     |     | pF   |
| HCT TYPES                              |                                                     |                     |                     |     |     |               |     |     |                |     |     |      |
| t <sub>PHL</sub> ,<br>t <sub>PLH</sub> | Data to outputs                                     | 4.5                 | 9 <sup>(3)</sup> 22 |     |     | 28            |     |     | 33             |     |     | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Output enable and disable<br>times                  | 4.5                 | 30                  |     |     | 38            |     |     | 45             |     |     | ns   |
| t <sub>THL</sub> ,<br>t <sub>TLH</sub> | Output transition time                              | 4.5                 | 12                  |     |     | 15            |     |     | 18             |     |     | ns   |
| C <sub>I</sub>                         | Input capacitance                                   |                     | 10                  |     |     | 10            |     |     | 10             |     |     | pF   |
| C <sub>PD</sub>                        | Power dissipation<br>capacitance <sup>(1) (2)</sup> | 5                   | 40                  |     |     |               |     |     |                |     |     | pF   |

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per channel.

(2)  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

(3)  $C_L = 15 \text{ pF}$  and  $V_{CC} = 5 \text{ V}$ .

## 5.8 Switching Characteristics '241

 $C_L = 50 \text{ pF}$ , Input  $t_r$ ,  $t_f = 6 \text{ ns}$ 

| PARAMETER                              |                                                     | V <sub>CC</sub> (V) | 25°C                 |     |     | –40°C to 85°C |     |     | –55°C to 125°C |     |     | UNIT |
|----------------------------------------|-----------------------------------------------------|---------------------|----------------------|-----|-----|---------------|-----|-----|----------------|-----|-----|------|
|                                        |                                                     |                     | MIN                  | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |      |
| HC TYPES                               |                                                     |                     |                      |     |     |               |     |     |                |     |     |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation delay<br>Data to outputs                | 2                   | 110                  |     |     | 140           |     |     | 165            |     |     | ns   |
|                                        |                                                     | 4.5                 | 9 <sup>(3)</sup> 22  |     |     | 28            |     |     | 33             |     |     |      |
|                                        |                                                     | 6                   | 19                   |     |     | 24            |     |     | 28             |     |     |      |
| t <sub>THL</sub> ,<br>t <sub>TLH</sub> | Output enable and disable<br>time                   | 2                   | 150                  |     |     | 190           |     |     | 225            |     |     | ns   |
|                                        |                                                     | 4.5                 | 30                   |     |     | 38            |     |     | 45             |     |     |      |
|                                        |                                                     | 5                   | 12                   |     |     |               |     |     |                |     |     |      |
|                                        |                                                     | 6                   | 26                   |     |     | 33            |     |     | 38             |     |     |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Output transition time                              | 2                   | 60                   |     |     | 75            |     |     | 90             |     |     | ns   |
|                                        |                                                     | 4.5                 | 12                   |     |     | 15            |     |     | 18             |     |     |      |
|                                        |                                                     | 6                   | 10                   |     |     | 13            |     |     | 15             |     |     |      |
| C <sub>I</sub>                         | Input capacitance                                   |                     | 10                   |     |     | 10            |     |     | 10             |     |     | pF   |
| C <sub>O</sub>                         | Three-state output<br>capacitance                   |                     | 20                   |     |     | 20            |     |     | 20             |     |     | pF   |
| C <sub>PD</sub>                        | Power dissipation<br>capacitance <sup>(1) (2)</sup> | 5                   | 34 <sup>(3)</sup>    |     |     |               |     |     |                |     |     | pF   |
| HCT TYPES                              |                                                     |                     |                      |     |     |               |     |     |                |     |     |      |
| t <sub>PHL</sub> ,<br>t <sub>PLH</sub> | Data to outputs                                     | 4.5                 | 10 <sup>(3)</sup> 25 |     |     | 31            |     |     | 38             |     |     | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Output enable and disable<br>times                  | 4.5                 | 30                   |     |     | 38            |     |     | 45             |     |     | ns   |
| t <sub>THL</sub> ,<br>t <sub>TLH</sub> | Output transition time                              | 4.5                 | 12                   |     |     | 15            |     |     | 18             |     |     | ns   |
| C <sub>I</sub>                         | Input capacitance                                   |                     | 10                   |     |     | 10            |     |     | 10             |     |     | pF   |
| C <sub>PD</sub>                        | Power dissipation<br>capacitance <sup>(1) (2)</sup> | 5                   | 38                   |     |     |               |     |     |                |     |     | pF   |

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per channel.

(2)  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $f_O$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

(3)  $C_L = 15 \text{ pF}$  and  $V_{CC} = 5 \text{ V}$ .

## 5.9 Switching Characteristics '244

$C_L = 50$  pF, Input  $t_r$ ,  $t_f = 6$  ns

| PARAMETER                              |                                                     | V <sub>CC</sub> (V) | 25°C                 |     |     | −40°C to 85°C |     |     | −55°C to 125°C |     |     | UNIT |
|----------------------------------------|-----------------------------------------------------|---------------------|----------------------|-----|-----|---------------|-----|-----|----------------|-----|-----|------|
|                                        |                                                     |                     | MIN                  | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |      |
| HC TYPES                               |                                                     |                     |                      |     |     |               |     |     |                |     |     |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation delay<br>Data to outputs                | 2                   | 110                  |     |     | 140           |     |     | 165            |     |     | ns   |
|                                        |                                                     | 4.5                 | 9 <sup>(3)</sup> 22  |     |     | 28            |     |     | 33             |     |     |      |
|                                        |                                                     | 6                   | 19                   |     |     | 24            |     |     | 28             |     |     |      |
| t <sub>THL</sub> ,<br>t <sub>TLH</sub> | Output enable and disable<br>time                   | 2                   | 150                  |     |     | 190           |     |     | 225            |     |     | ns   |
|                                        |                                                     | 4.5                 | 30                   |     |     | 38            |     |     | 45             |     |     |      |
|                                        |                                                     | 5                   | 12                   |     |     |               |     |     |                |     |     |      |
|                                        |                                                     | 6                   | 26                   |     |     | 33            |     |     | 38             |     |     |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Output transition time                              | 2                   | 60                   |     |     | 75            |     |     | 90             |     |     | ns   |
|                                        |                                                     | 4.5                 | 12                   |     |     | 15            |     |     | 18             |     |     |      |
|                                        |                                                     | 6                   | 10                   |     |     | 13            |     |     | 15             |     |     |      |
| C <sub>I</sub>                         | Input capacitance                                   |                     | 10                   |     |     | 10            |     |     | 10             |     |     | pF   |
| C <sub>O</sub>                         | Three-state output<br>capacitance                   |                     | 20                   |     |     | 20            |     |     | 20             |     |     | pF   |
| C <sub>PD</sub>                        | Power dissipation<br>capacitance <sup>(1) (2)</sup> | 5                   | 46 <sup>(3)</sup>    |     |     |               |     |     |                |     |     | pF   |
| HCT TYPES                              |                                                     |                     |                      |     |     |               |     |     |                |     |     |      |
| t <sub>PHL</sub> ,<br>t <sub>PLH</sub> | Data to outputs                                     | 4.5                 | 10 <sup>(3)</sup> 25 |     |     | 31            |     |     | 38             |     |     | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Output enable and disable<br>times                  | 4.5                 | 30                   |     |     | 38            |     |     | 45             |     |     | ns   |
| t <sub>THL</sub> ,<br>t <sub>TLH</sub> | Output transition time                              | 4.5                 | 12                   |     |     | 15            |     |     | 18             |     |     | ns   |
| C <sub>I</sub>                         | Input capacitance                                   |                     | 10                   |     |     | 10            |     |     | 10             |     |     | pF   |
| C <sub>PD</sub>                        | Power dissipation<br>capacitance <sup>(1) (2)</sup> | 5                   | 40                   |     |     |               |     |     |                |     |     | pF   |

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per channel.

(2)  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

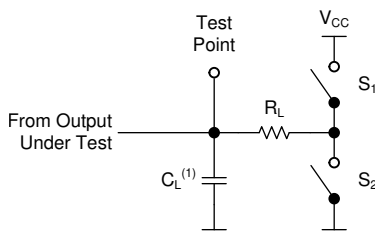
(3)  $C_L = 15$  pF and  $V_{CC} = 5$  V.

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .

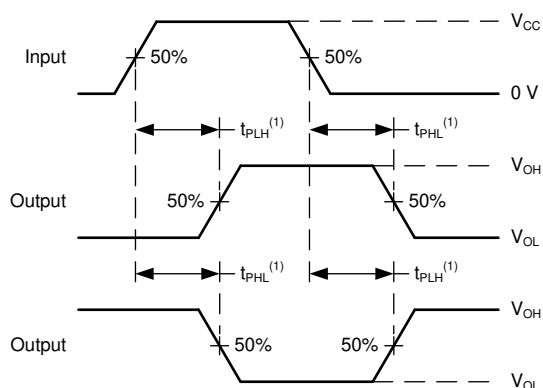
For clock inputs,  $f_{\max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



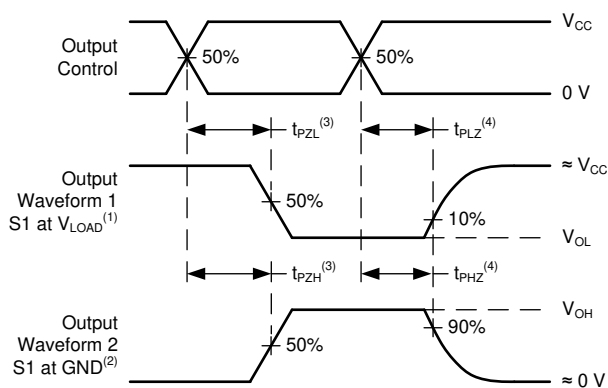
(1)  $C_L$  includes probe and test-fixture capacitance.

**FIG 6-1. Load Circuit for 3-State Outputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**FIG 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**



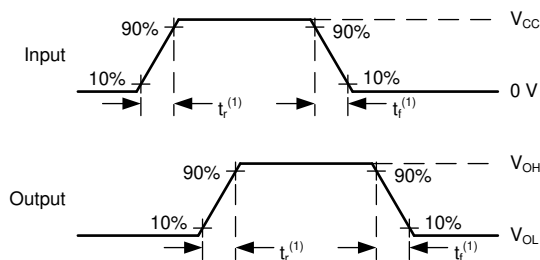
(1) S1 = CLOSED; S2 = OPEN.

(2) S1 = OPEN; S2 = CLOSED.

(3)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

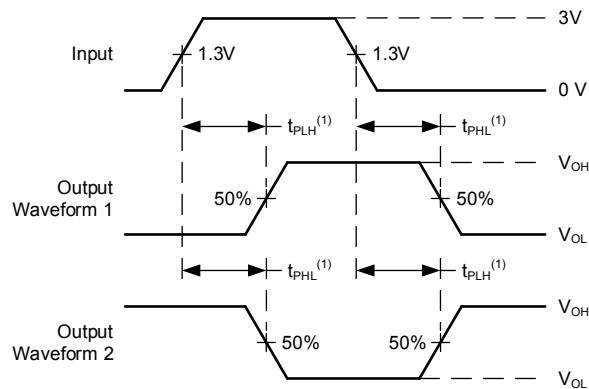
(4)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**FIG 6-3. Voltage Waveforms, Standard CMOS Inputs Propagation Delays**



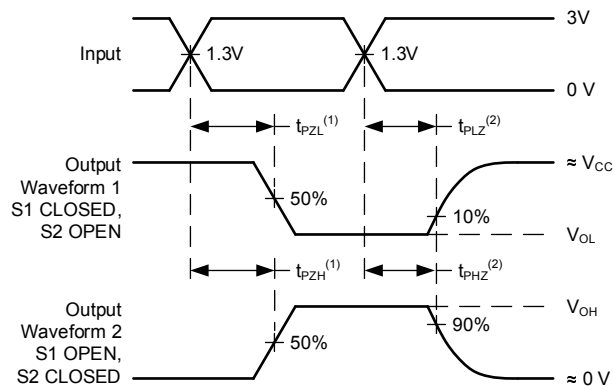
(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**FIG 6-4. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**6-5. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**



(1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

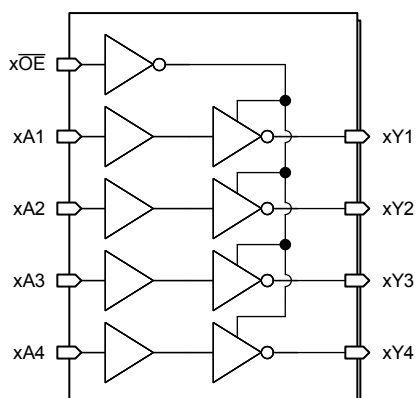
**6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays**

## 7 Detailed Description

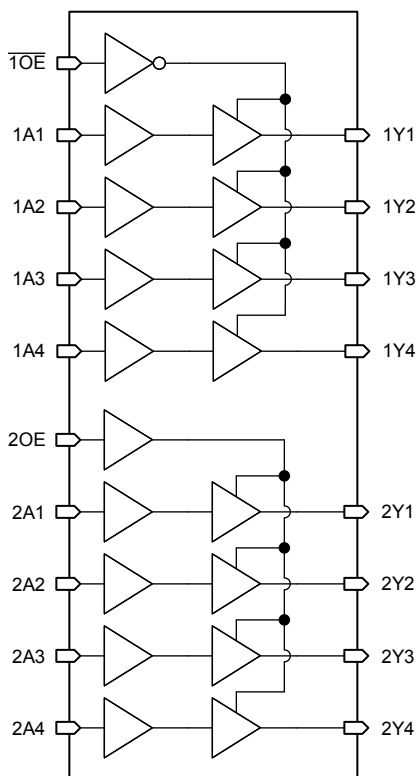
### 7.1 Overview

The 'HC240 and 'HCT240 are inverting three-state buffers having two active-low output enables. The CD74HC241, 'HCT241, 'HC244 and 'HCT244 are non-inverting threestate buffers that differ only in that the 241 has one activehigh and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

### 7.2 Functional Block Diagram



7-1. Functional Block Diagram '240



7-2. Functional Block Diagram '241

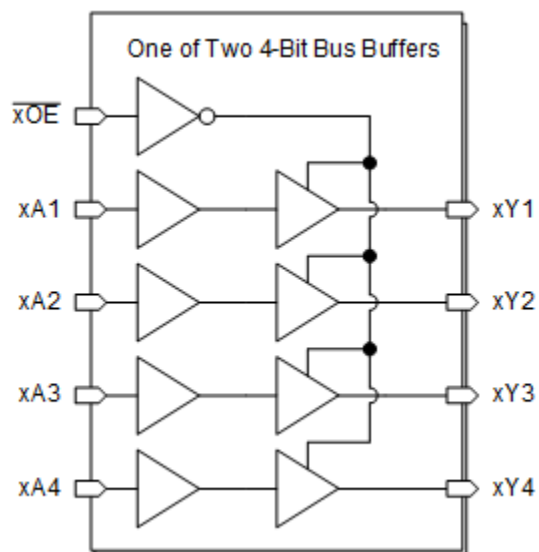


图 7-3. Functional Block Diagram '244

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| <a href="#">CD54HC240F3A</a>  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8407401RA<br>CD54HC240F3A  |
| CD54HC240F3A.A                | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8407401RA<br>CD54HC240F3A  |
| <a href="#">CD54HC244F</a>    | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HC244F                 |
| CD54HC244F.A                  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HC244F                 |
| <a href="#">CD54HC244F3A</a>  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8409601RA<br>CD54HC244F3A  |
| CD54HC244F3A.A                | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8409601RA<br>CD54HC244F3A  |
| <a href="#">CD54HCT240F3A</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8550501RA<br>CD54HCT240F3A |
| CD54HCT240F3A.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8550501RA<br>CD54HCT240F3A |
| <a href="#">CD54HCT241F3A</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT241F3A              |
| CD54HCT241F3A.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT241F3A              |
| <a href="#">CD54HCT244F</a>   | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT244F                |
| CD54HCT244F.A                 | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT244F                |
| <a href="#">CD54HCT244F3A</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8513001RA<br>CD54HCT244F3A |
| CD54HCT244F3A.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8513001RA<br>CD54HCT244F3A |
| <a href="#">CD74HC240E</a>    | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC240E                 |
| CD74HC240E.A                  | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC240E                 |
| <a href="#">CD74HC240M</a>    | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC240M                     |
| <a href="#">CD74HC240M96</a>  | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC240M                     |
| CD74HC240M96.A                | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC240M                     |
| <a href="#">CD74HC241E</a>    | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC241E                 |
| CD74HC241E.A                  | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC241E                 |
| <a href="#">CD74HC241M</a>    | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC241M                     |
| <a href="#">CD74HC241M96</a>  | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC241M                     |

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CD74HC241M96.A                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC241M              |
| <a href="#">CD74HC244E</a>    | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC244E          |
| CD74HC244E.A                  | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC244E          |
| CD74HC244E.B                  | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC244E          |
| CD74HC244EE4                  | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC244E          |
| <a href="#">CD74HC244M</a>    | Obsolete      | Production           | SOIC (DW)   20  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC244M              |
| CD74HC244M.B                  | Obsolete      | Production           | SOIC (DW)   20  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC244M              |
| <a href="#">CD74HC244M96</a>  | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC244M              |
| CD74HC244M96.A                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC244M              |
| CD74HC244M96.B                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC244M              |
| CD74HC244M96E4                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC244M              |
| CD74HC244M96G4                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC244M              |
| <a href="#">CD74HCT240E</a>   | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT240E         |
| CD74HCT240E.A                 | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT240E         |
| CD74HCT240EE4                 | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT240E         |
| <a href="#">CD74HCT240M</a>   | Obsolete      | Production           | SOIC (DW)   20  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HCT240M             |
| <a href="#">CD74HCT240M96</a> | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT240M             |
| CD74HCT240M96.A               | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT240M             |
| CD74HCT240M96.B               | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT240M             |
| <a href="#">CD74HCT240PW</a>  | Obsolete      | Production           | TSSOP (PW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HK240               |
| <a href="#">CD74HCT240PWR</a> | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HK240               |
| CD74HCT240PWR.A               | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HK240               |
| <a href="#">CD74HCT240PWT</a> | Obsolete      | Production           | TSSOP (PW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HK240               |
| <a href="#">CD74HCT241E</a>   | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT241E         |
| CD74HCT241E.A                 | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT241E         |
| <a href="#">CD74HCT241M96</a> | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT241M             |
| CD74HCT241M96.A               | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT241M             |
| CD74HCT241M96.B               | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT241M             |
| <a href="#">CD74HCT244E</a>   | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU   NIPDAU                      | N/A for Pkg Type                  | -55 to 125   | CD74HCT244E         |
| CD74HCT244E.A                 | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT244E         |
| CD74HCT244E.B                 | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT244E         |

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD74HCT244M</a>   | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HCT244M             |
| <a href="#">CD74HCT244M96</a> | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT244M             |
| CD74HCT244M96.A               | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT244M             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC240, CD54HC244, CD54HCT240, CD54HCT241, CD54HCT244, CD74HC240, CD74HC244, CD74HCT240, CD74HCT241, CD74HCT244 :**

● Catalog : [CD74HC240](#), [CD74HC244](#), [CD74HCT240](#), [CD74HCT241](#), [CD74HCT244](#)

● Military : [CD54HC240](#), [CD54HC244](#), [CD54HCT240](#), [CD54HCT241](#), [CD54HCT244](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

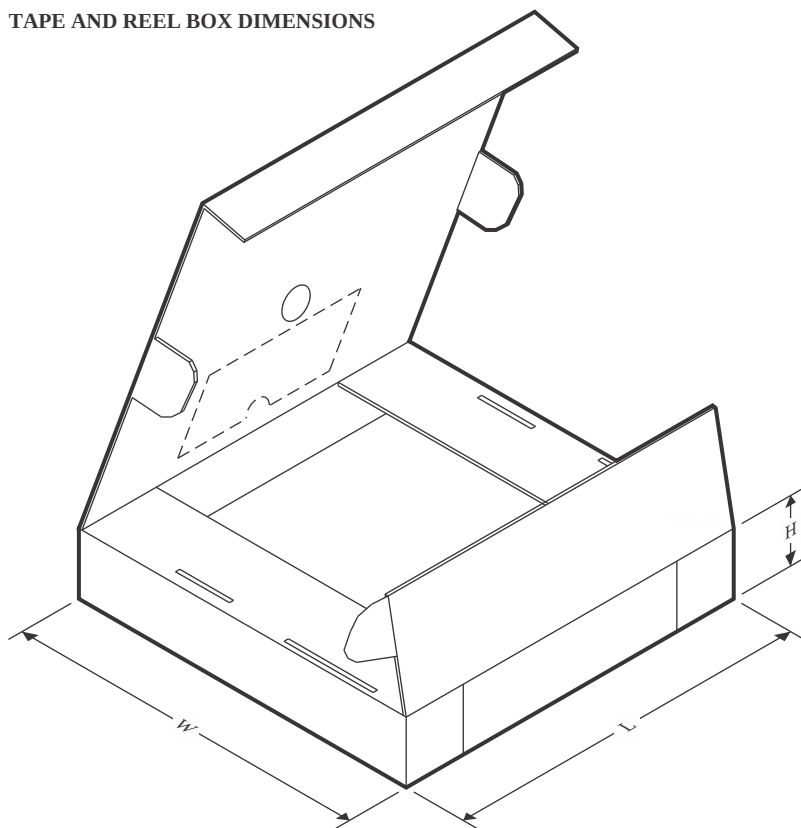
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC240M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HC241M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HC244M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT240M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT240PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| CD74HCT241M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT241M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT244M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT244M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC240M96  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HC241M96  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HC244M96  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HCT240M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HCT240PWR | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| CD74HCT241M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HCT241M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HCT244M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74HCT244M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |

**TUBE**

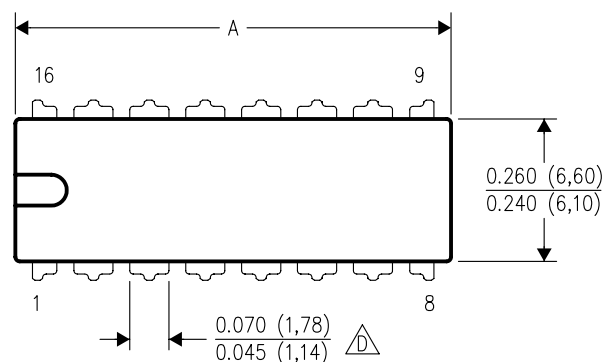

\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC240E    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC240E.A  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC241E    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC241E.A  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC244E    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC244E.A  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC244E.B  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC244EE4  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT240E   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT240E.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT240EE4 | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT241E   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT241E.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT244E   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT244E.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT244E.B | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |

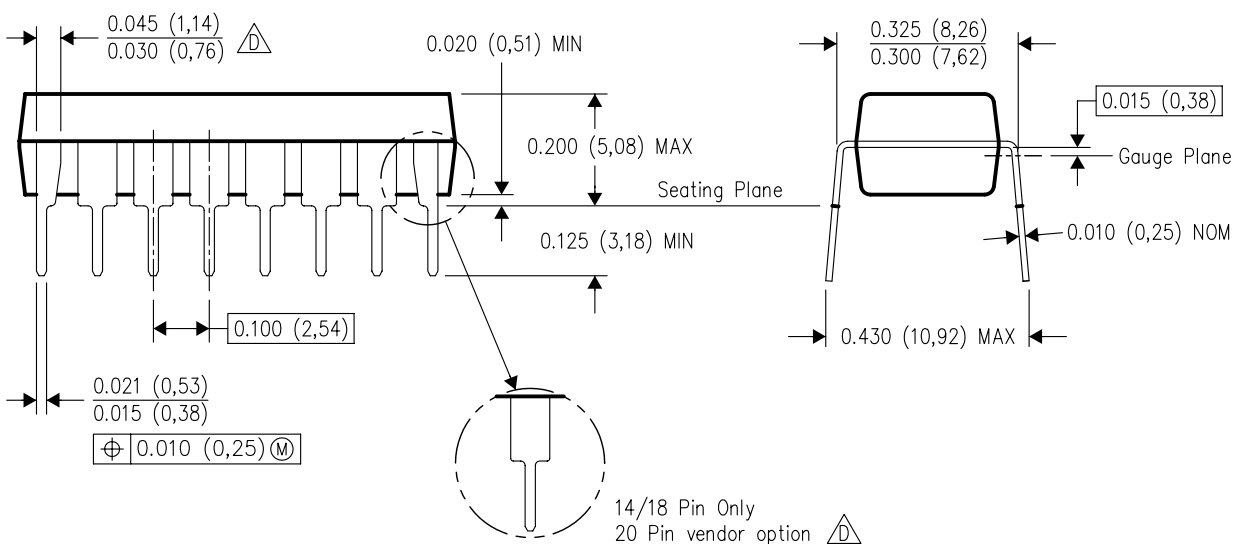
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



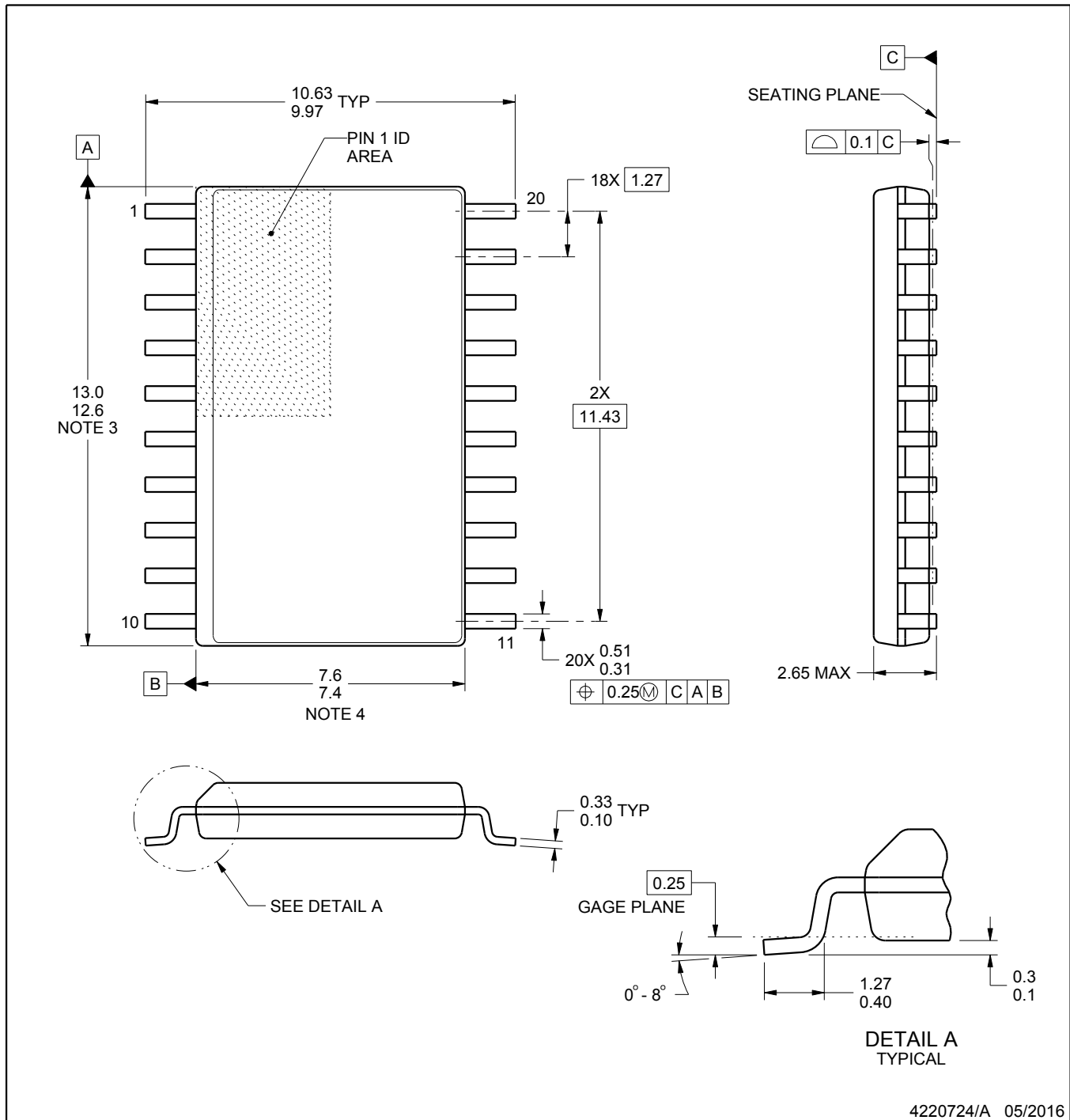
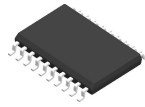
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

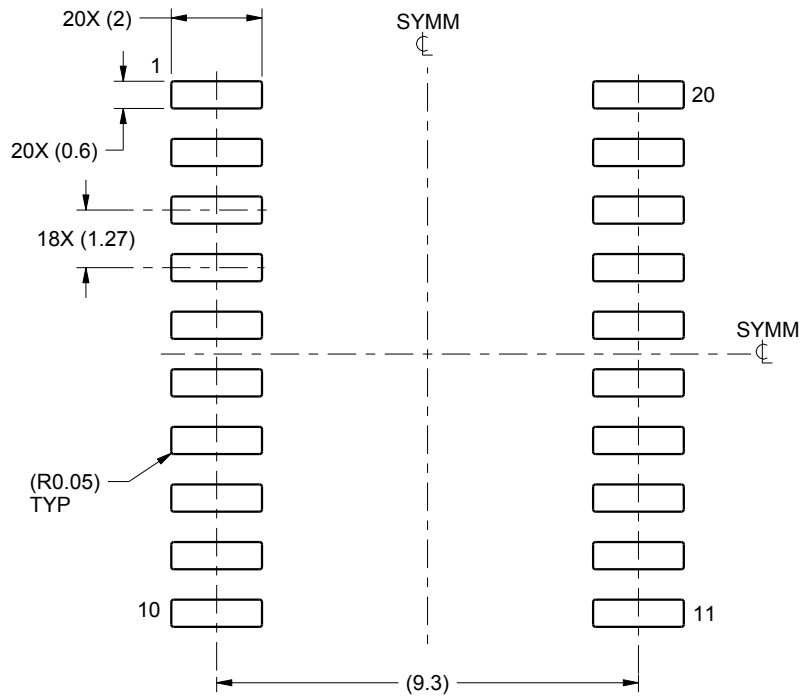
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

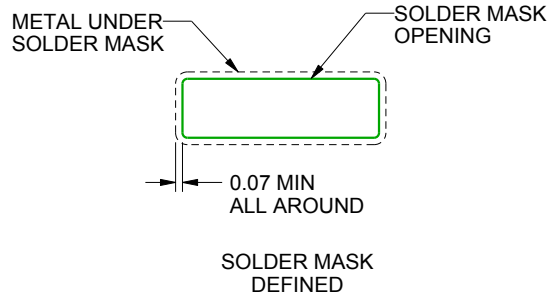
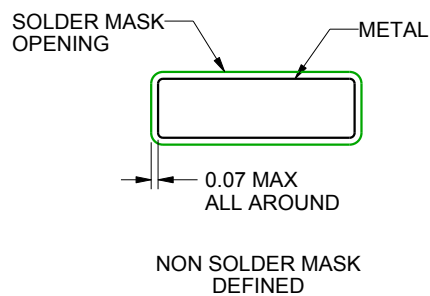
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

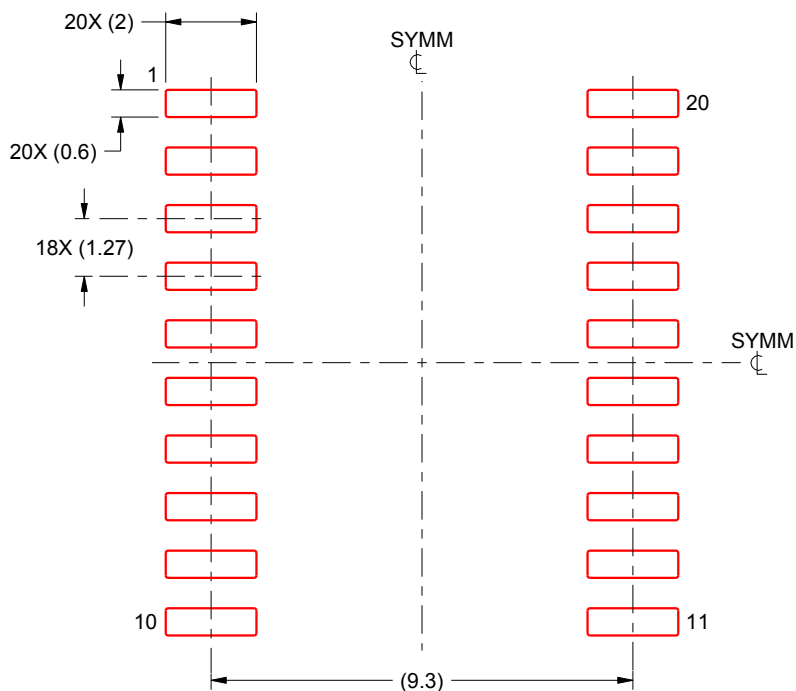
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

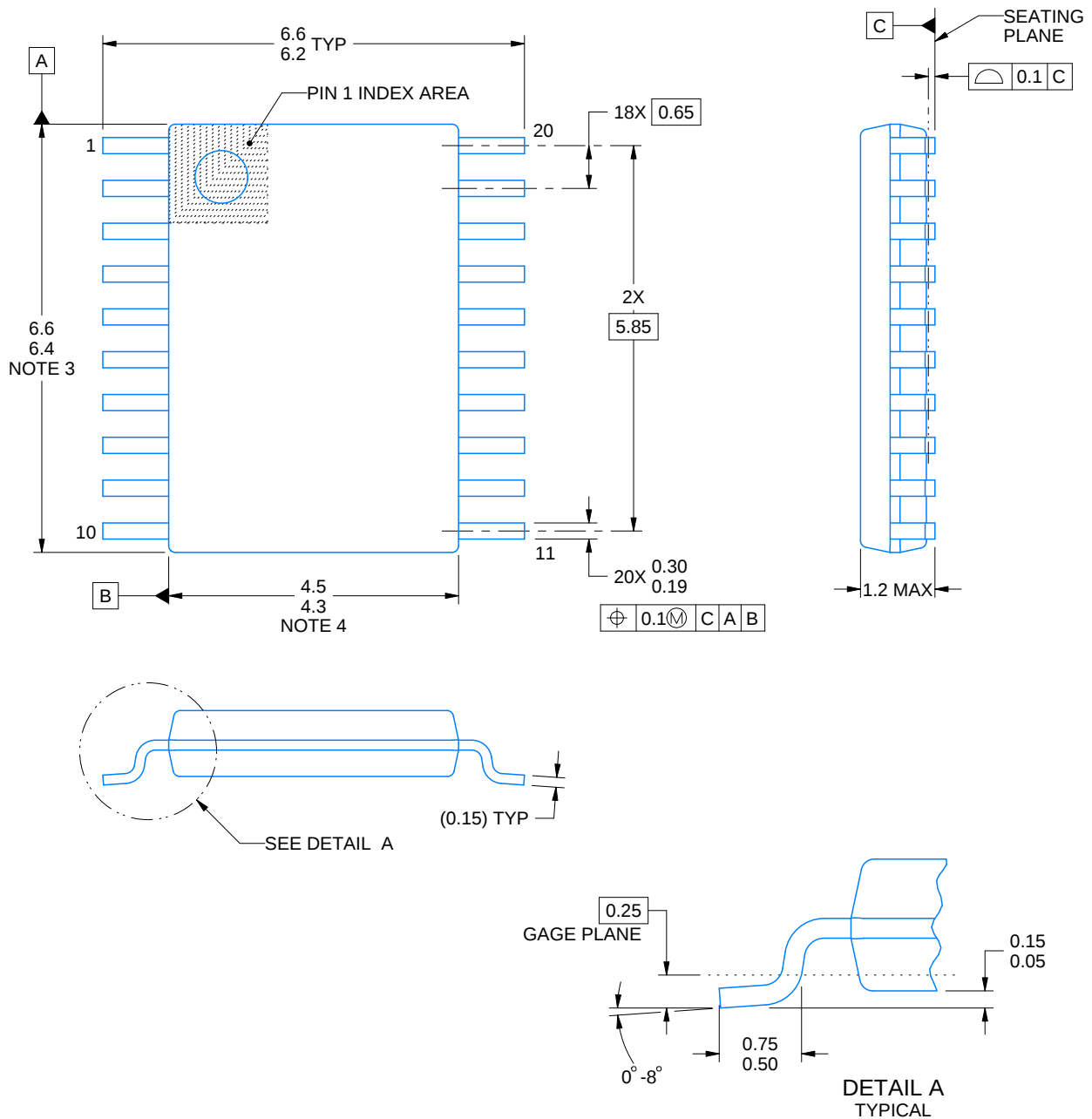
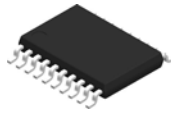


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

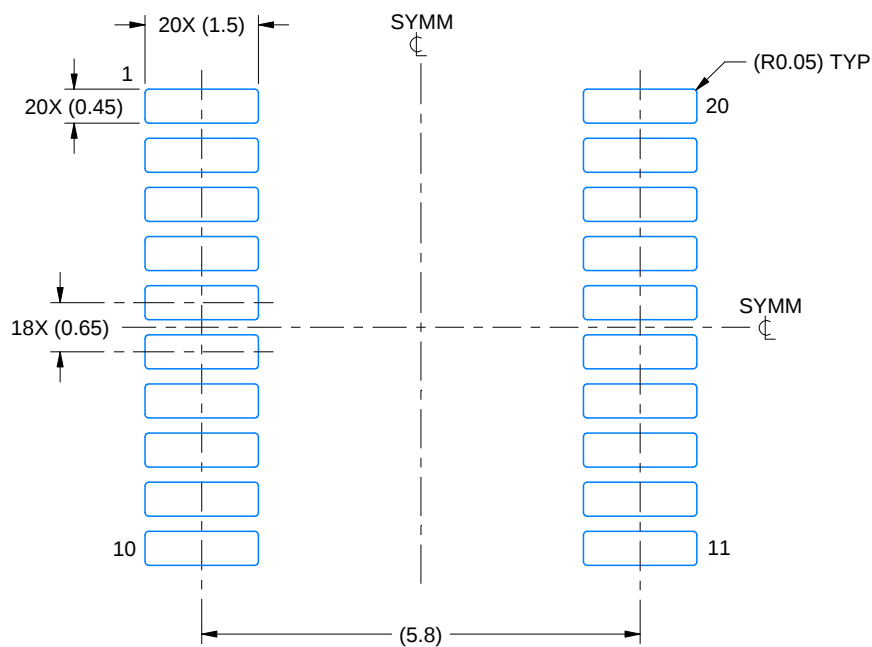
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

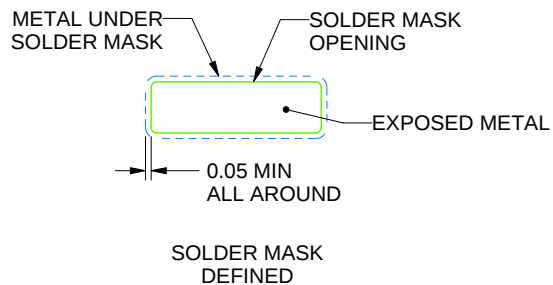
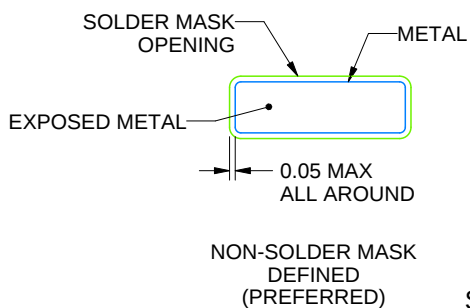
**PW0020A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

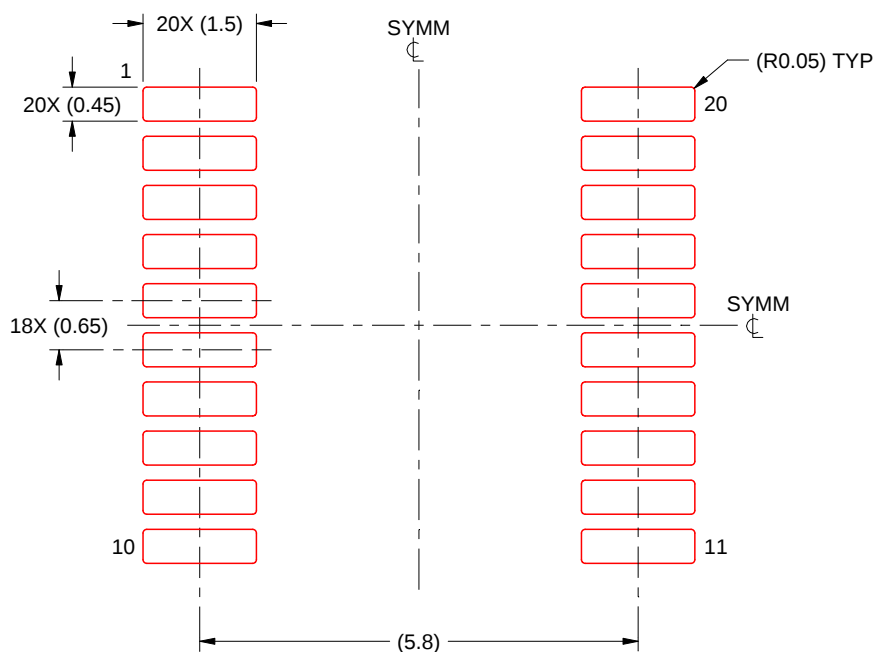
6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

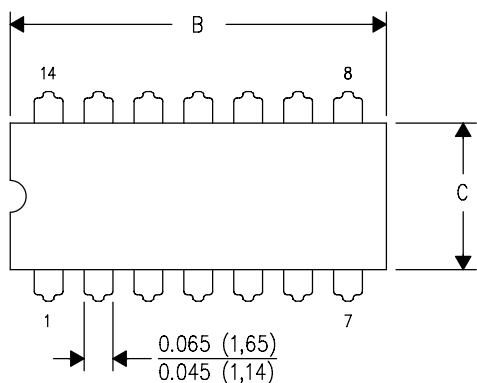
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

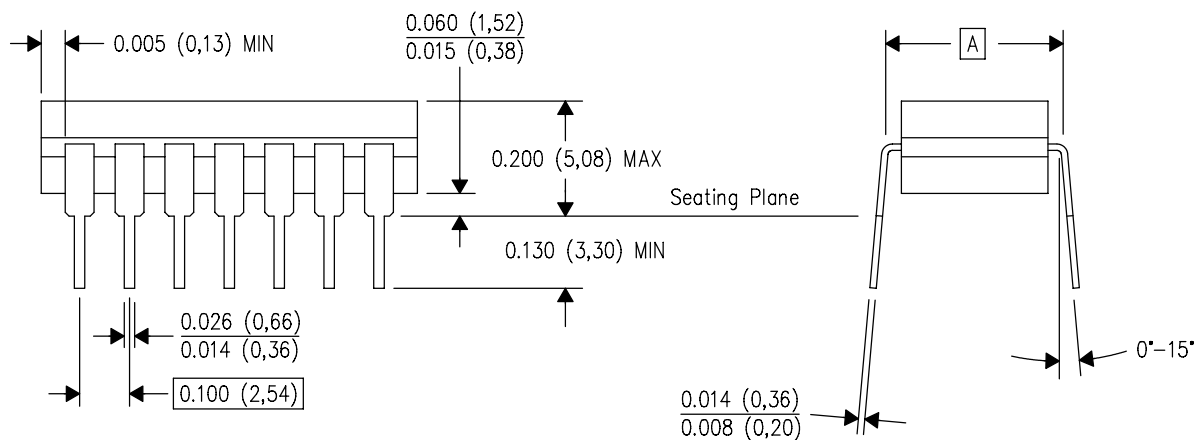
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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