

## CDx4HCT14 ヘキサ・インバータ、シュミット・トリガ入力

### 1 特長

- LSTTL 入力ロジック互換
  - $V_{IL(max)} = 0.8V, V_{IH(min)} = 2V$
- CMOS 入力ロジック互換
  - $I_I \leq 1\mu A (V_{OL}, V_{OH})$
- バッファ付き入力
- 4.5V~5.5V で動作
- 広い動作温度範囲: -55°C ~ +125°C
- 最大 10 個の LSTTL 負荷ファンアウトに対応
- LSTTL ロジック IC に比べて消費電力を大幅削減

### 2 アプリケーション

- 反転クロック入力の同期
- スイッチのデバウンス
- デジタル信号の反転

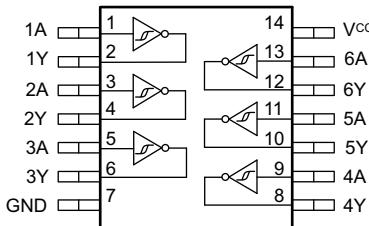
### 3 概要

このデバイスには、シュミット・トリガ入力の 6 つの独立したインバータが内蔵されています。各ゲートはブール関数  $Y = \bar{A}$  を正論理で実行します。

#### 製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
CD74HCT14M	SOIC (14)	8.70mm × 3.90mm
CD74HCT14E	PDIP (14)	19.30mm × 6.40mm
CD74HCT14PW	TSSOP (14)	5.00mm × 4.40mm
CD54HCT14F	CDIP (14)	21.30mm × 7.60mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能とピン配置



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## 4 Revision History

DATE	REVISION	NOTES
June 2020	*	Initial release. Moved the HCT devices from the SCHS129 to a standalone data sheet.

## 5 Pin Configuration and Functions

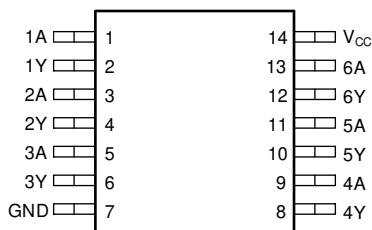


图 5-1. D, N, PW, or J Package 14-Pin SOIC, PDIP, TSSOP, or CDIP Top View

## Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	—	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V <sub>cc</sub>	14	—	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>	Plastic package	150		°C
		Hermetic package or die	175		°C
	Lead temperature (soldering 10s)	SOIC - lead tips only	300		°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

### 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5.5	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2		V	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		0.8	V	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V	
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V	
t <sub>t</sub>	Input transition time	V <sub>CC</sub> = 4.5 V		500		ns
		V <sub>CC</sub> = 5.5 V		400		
T <sub>A</sub>	Operating free-air temperature		-55	125	°C	

### 6.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD74HCT14			UNIT
		N (PDIP)	D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	62.9	95.5	119.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.7	49.9	42.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	42.7	51.7	64.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	30.3	12.8	4.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	42.4	51.3	63.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.4 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT	
			25°C			−40°C to 85°C			−55°C to 125°C				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$V_{T+}$	Positive switching threshold		4.5 V	1.2	1.9	1.2	1.9	1.9	1.2	1.9	1.9	V	
			5.5 V	1.4	2.1	1.4	2.1	2.1	1.4	2.1	2.1		
$V_{T-}$	Negative switching threshold		4.5 V	0.5	1.2	0.5	1.2	0.5	0.5	1.2	1.2	V	
			5.5 V	0.6	1.4	0.6	1.4	1.4	0.6	1.4	1.4		
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ )		4.5 V	0.4	1.4	0.4	1.4	0.4	0.4	1.4	1.4	V	
			5.5 V	0.4	1.5	0.4	1.5	0.4	0.4	1.5	1.5		
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5 V	4.4		4.4		4.4		4.4	V	
			$I_{OH} = -4 \text{ mA}$	4.5 V	3.98		3.84		3.7				
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5 V		0.1		0.1		0.1		V	
			$I_{OL} = 4 \text{ mA}$	4.5 V		0.26		0.33		0.4			
$I_I$	Input leakage current	$V_I = V_{CC}$ and GND	$I_O = 0$	5.5 V		±0.1		±1		±1		µA	
$I_{CC}$	Supply current	$V_I = V_{CC}$ or GND	$I_O = 0$	5.5 V		2		20		40		µA	
$\Delta I_{CC}$ (1)	Additional Quiescent Device Current Per Input Pin.	$V_I = V_{CC} - 2.1$		4.5 V to 5.5 V		360		450		490		µA	
$C_i$	Input capacitance		5 V		10		10		10		10	pF	

(1) For dual-supply systems theoretical worst case ( $V_I = 2.4 \text{ V}$ ,  $V_{CC} = 5.5 \text{ V}$ ) specification is 1.8 mA.

## 6.5 Switching Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT	
					25°C			−40°C to 85°C			−55°C to 125°C				
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{pd}$	Propagation delay	A	Y	$C_L = 50 \text{ pF}$	4.5 V		38		48		57		ns		
				$C_L = 15 \text{ pF}$	5 V		16								
$t_t$	Transition-time		Y	$C_L = 50 \text{ pF}$	4.5 V		15		19		22		ns		

## 6.6 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS			$V_{CC}$	MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance per gate	No load			5 V		20		pF

## 6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$

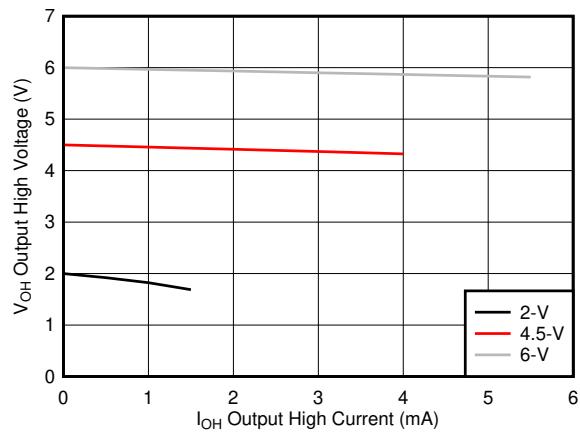


图 6-1. Typical output voltage in the high state ( $V_{OH}$ )

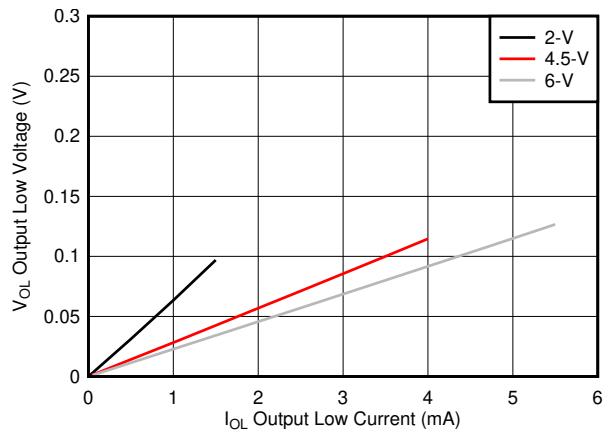
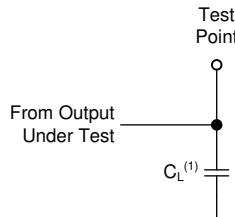


图 6-2. Typical output voltage in the low state ( $V_{OL}$ )

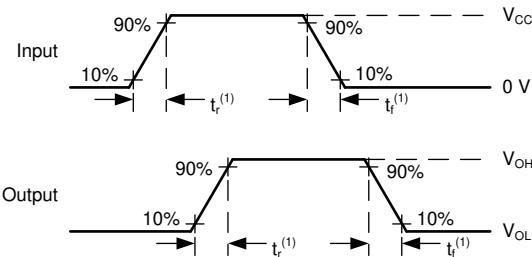
## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f < 6$  ns.
- The outputs are measured one at a time, with one input transition per measurement.



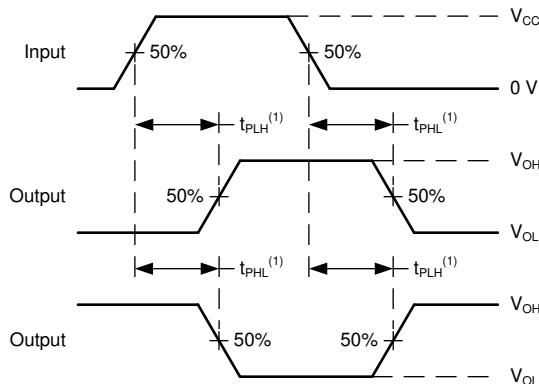
A.  $C_L = 50$  pF and includes probe and jig capacitance.

**图 7-1. Load Circuit**



A.  $t_t$  is the greater of  $t_r$  and  $t_f$ .

**图 7-2. Voltage Waveforms Transition Times**



A. The maximum between  $t_{PLH}$  and  $t_{PHL}$  is used for  $t_{pd}$ .

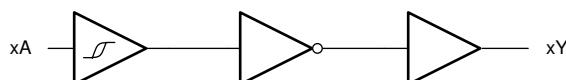
**图 7-3. Voltage Waveforms Propagation Delays**

## 8 Detailed Description

### 8.1 Overview

This device contains six independent inverters with Schmitt-trigger inputs. Each gate performs the Boolean function  $Y = \overline{A}$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [セクション 6.1](#) must be followed at all times.

The CD74HCT14 can drive a load with a total capacitance less than or equal to the maximum load listed in the [セクション 6.5](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [セクション 6.1](#).

#### 8.3.2 TTL-Compatible Schmitt-Trigger CMOS Inputs

TTL-Compatible Schmitt-trigger CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [セクション 6.4](#). The worst case resistance is calculated with the maximum input voltage, given in the [セクション 6.1](#), and the maximum input leakage current, given in the [セクション 6.4](#), using ohm's law ( $R = V / I$ ).

The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the [セクション 6.4](#), which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

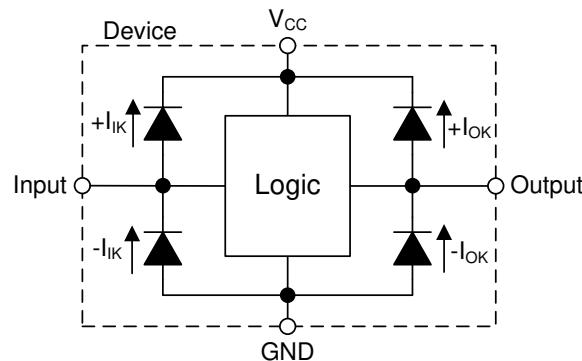
TTL-Compatible CMOS inputs have a lower threshold voltage than standard CMOS inputs to allow for compatibility with older bipolar logic devices. See the [セクション 6.2](#) for the valid input voltages for the CD74HCT14.

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [図 8-1](#).

#### 注意

Voltages beyond the values specified in the [セクション 6.1](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.4 Device Functional Modes

**表 8-1. Function Table**

INPUT	OUTPUT
A	Y
L	H
H	L

## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

This device can be used to add an additional stage to a counter with an external flip-flop. Because counters use a negative edge trigger, the flip-flop's clock input must be inverted to provide this function. This function only requires one of the six available inverters in the device, so the remaining channels can be used for other applications needing an inverted signal or improved signal integrity. Unused inputs must be terminated at V<sub>CC</sub> or GND. Unused outputs can be left floating.

### 9.2 Typical Application

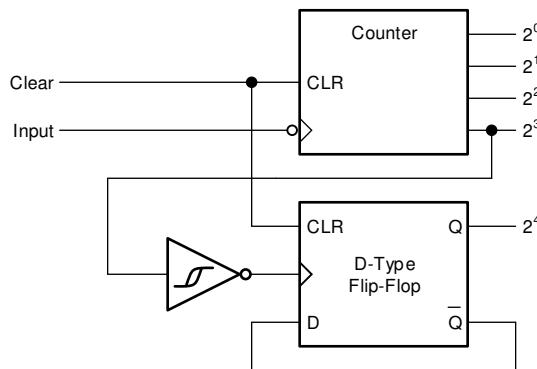


図 9-1. Typical application schematic

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [セクション 6.2](#). The supply voltage sets the device's electrical characteristics as described in the [セクション 6.4](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HCT14 plus the maximum supply current, I<sub>CC</sub>, listed in the [セクション 6.4](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V<sub>CC</sub> listed in the [セクション 6.1](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and C<sub>pd</sub> Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

### 注意

The maximum junction temperature, T<sub>J(max)</sub> listed in the [セクション 6.1](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [セクション 6.1](#). These limits are provided to prevent damage to the device.

### 9.2.1.2 Input Considerations

Input signals must cross  $V_{t-}(\text{min})$  to be considered a logic LOW, and  $V_{t+}(\text{max})$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the [セクション 6.1](#).

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HCT14, as specified in the [セクション 6.4](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The CD74HCT14 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the  $\Delta V_T(\text{min})$  in the [セクション 6.4](#). This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than  $V_{CC}$  or ground is plotted in the [セクション 6.7](#).

Refer to the [セクション 8.3](#) for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the [セクション 6.4](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [セクション 6.4](#).

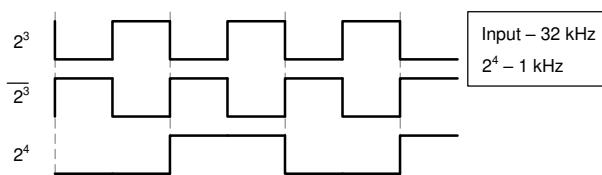
Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to [セクション 8.3](#) for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the [セクション 11](#).
2. Ensure the capacitive load at the output is  $\leq 70 \text{ pF}$ . This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HCT14 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_o(\text{max})) \Omega$ . This will ensure that the maximum output current from the [セクション 6.1](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

### 9.2.3 Application Curves



**図 9-2. Typical application timing diagram**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [セクション 6.2](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu F$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu F$  and 1- $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [図 11-1](#).

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V<sub>CC</sub>, whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

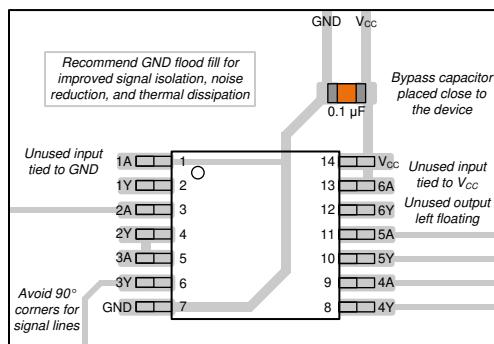


图 11-1. Example layout for the CD74HCT14

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

### 12.2 サポート・リソース

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すべての商標は、それぞれの所有者に帰属します。

### 12.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インストルメンツは、IC を取り扱う際には常に適切な注意を払うことをお勧めします。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.5 用語集

#### TI 用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD54HCT14F</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT14F
CD54HCT14F.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT14F
<a href="#">CD54HCT14F3A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8689001CA CD54HCT14F3A
CD54HCT14F3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8689001CA CD54HCT14F3A
<a href="#">CD74HCT14E</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT14E
CD74HCT14E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT14E
<a href="#">CD74HCT14M</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HCT14M
<a href="#">CD74HCT14M96</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT14M
CD74HCT14M96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT14M
<a href="#">CD74HCT14MT</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HCT14M
<a href="#">CD74HCT14PWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HK14
CD74HCT14PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK14
<a href="#">CD74HCT14PWR1G4</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK14

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HCT14, CD74HCT14 :**

- Catalog : [CD74HCT14](#)
- Military : [CD54HCT14](#)

NOTE: Qualified Version Definitions:

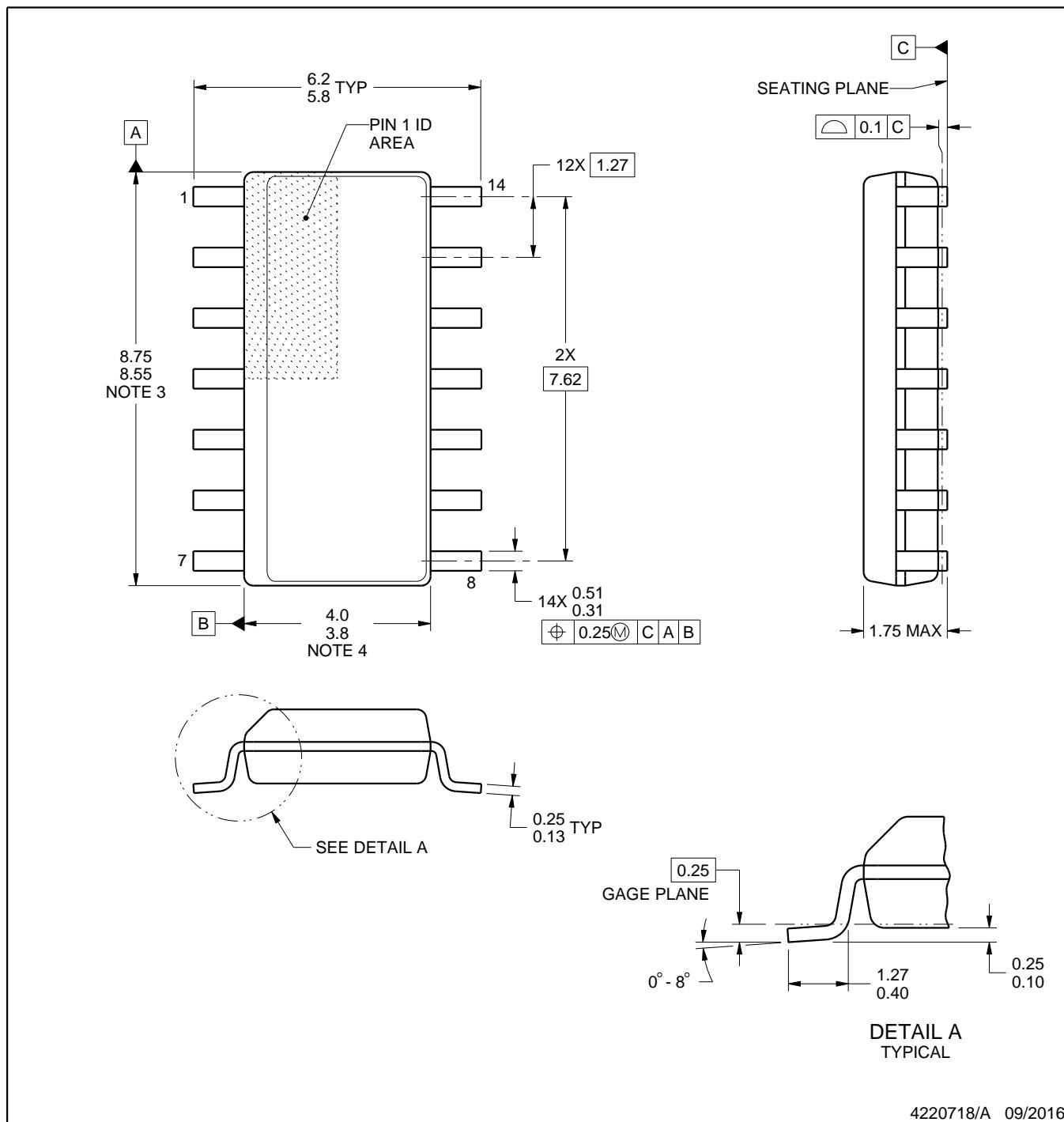
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

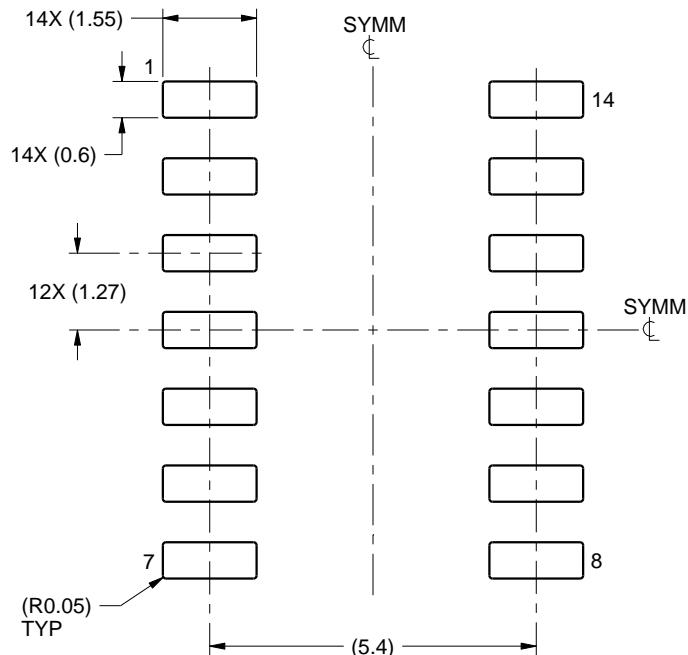
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

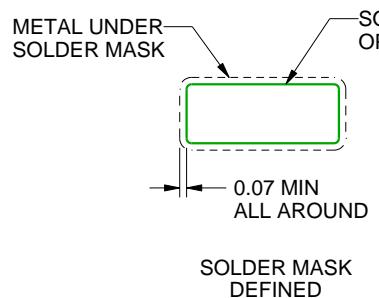
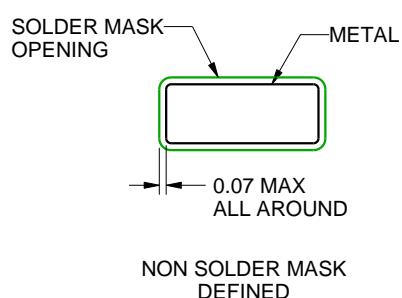
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

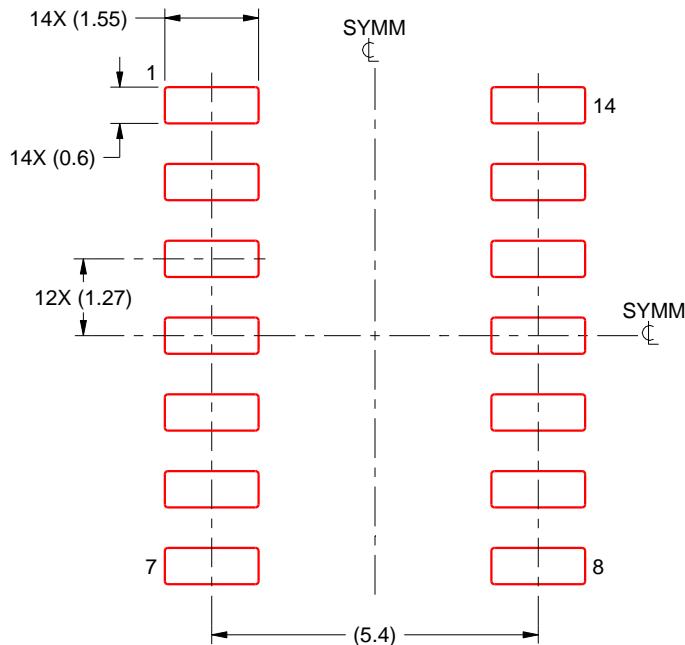
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

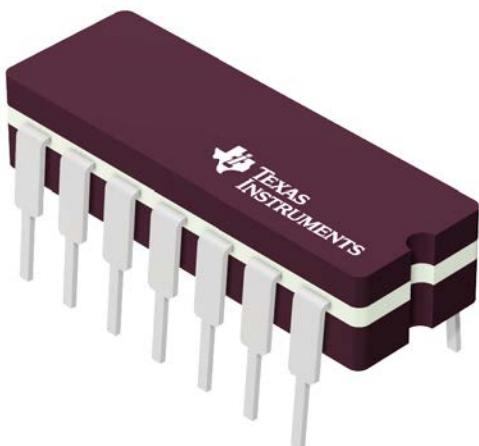
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

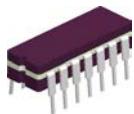
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

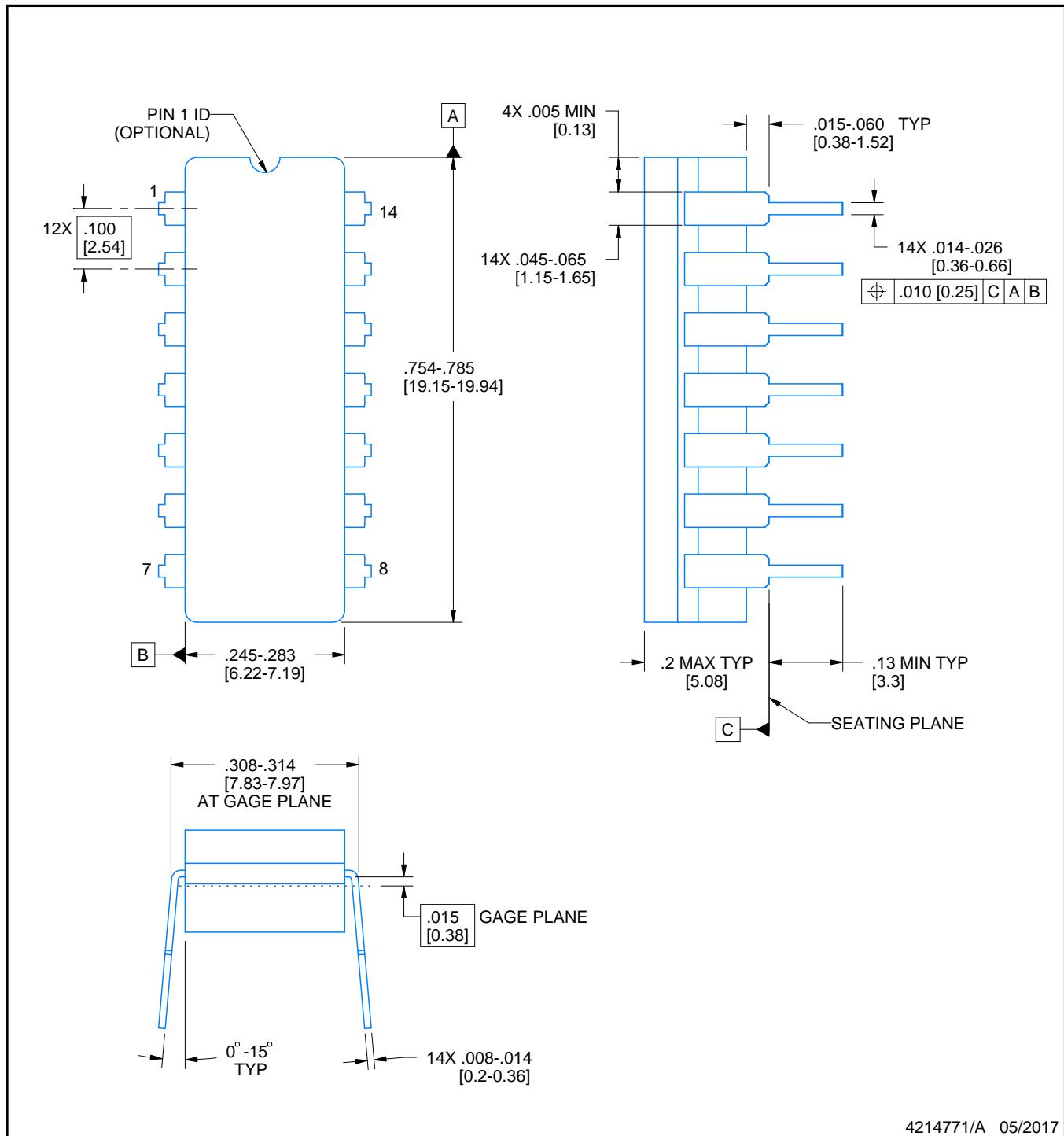
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

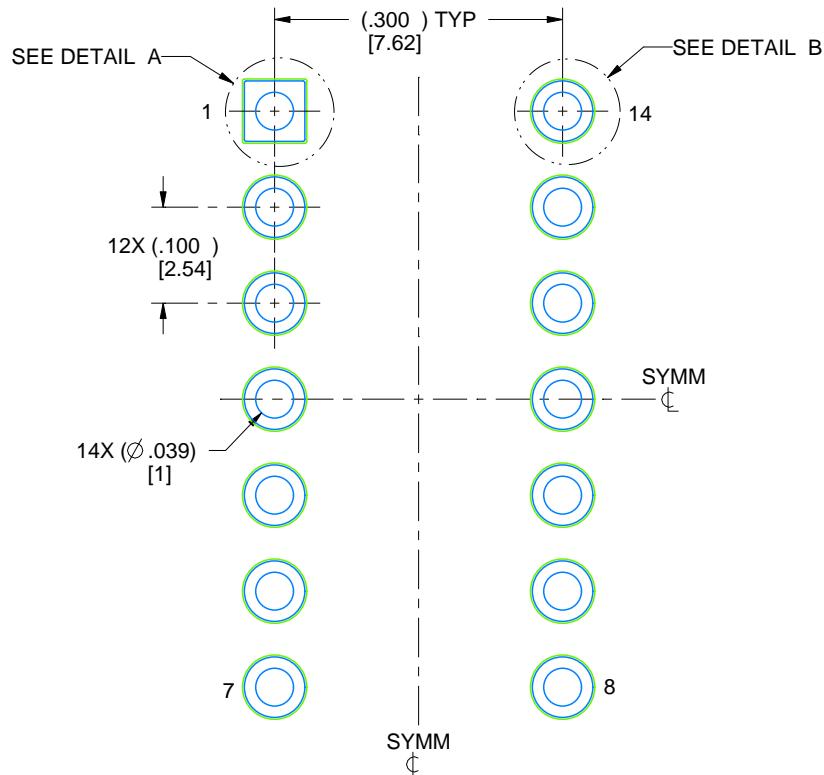
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

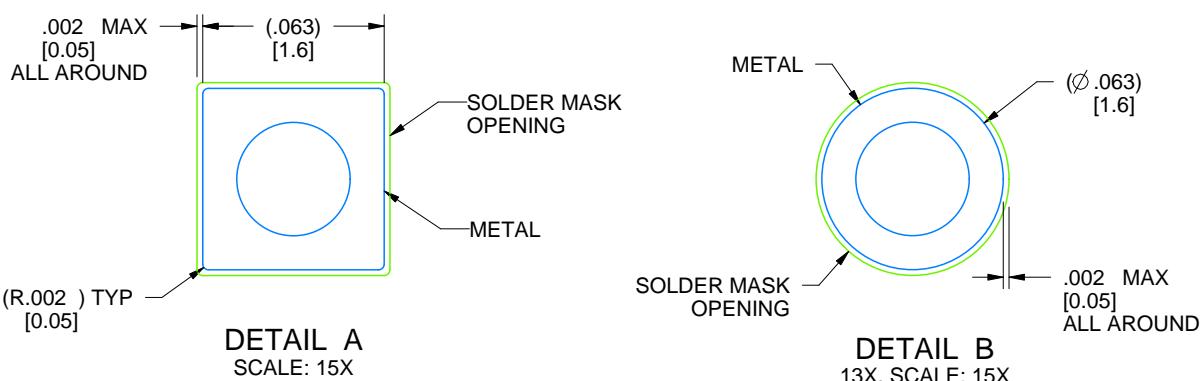
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

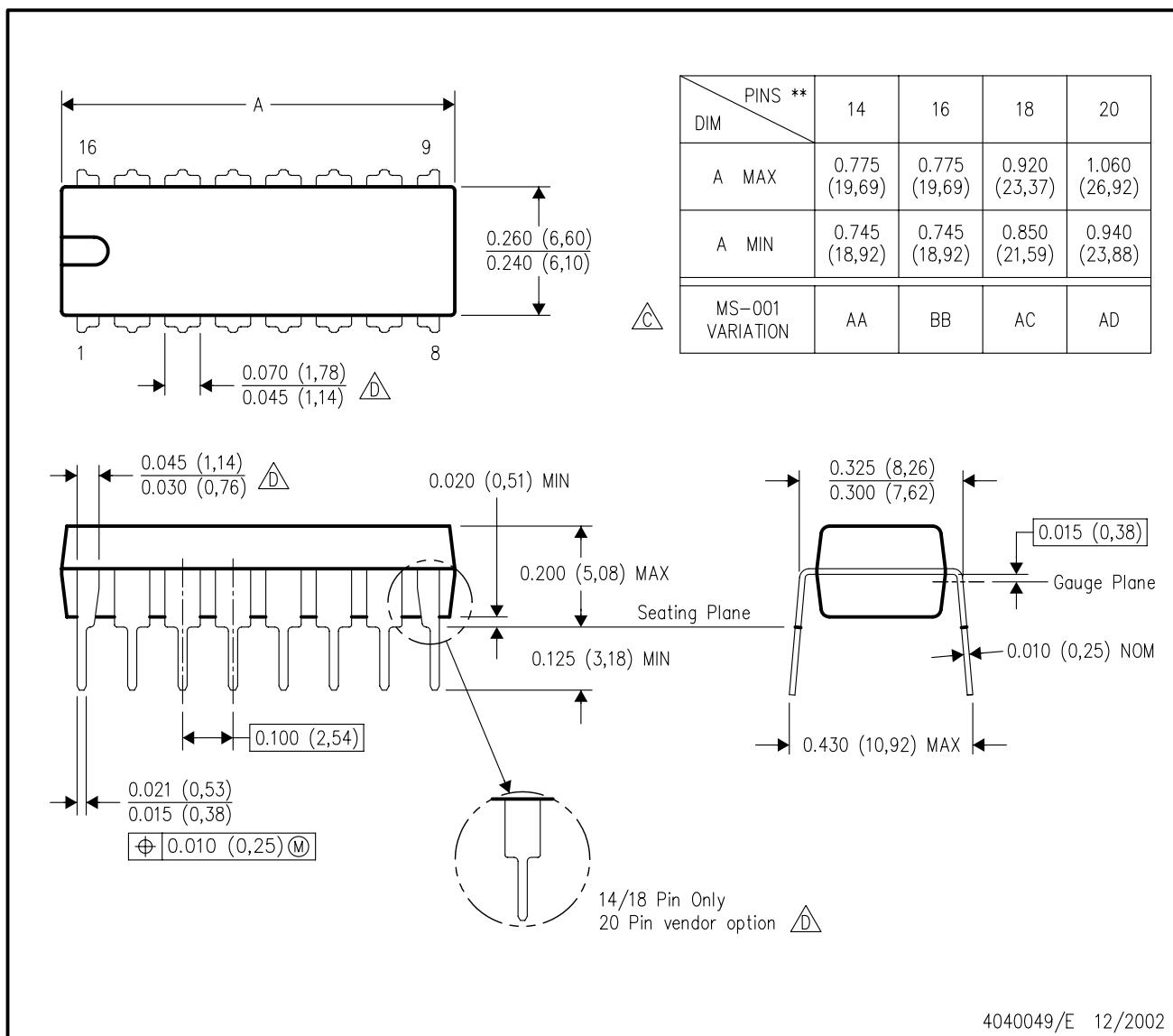


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



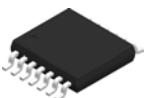
NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

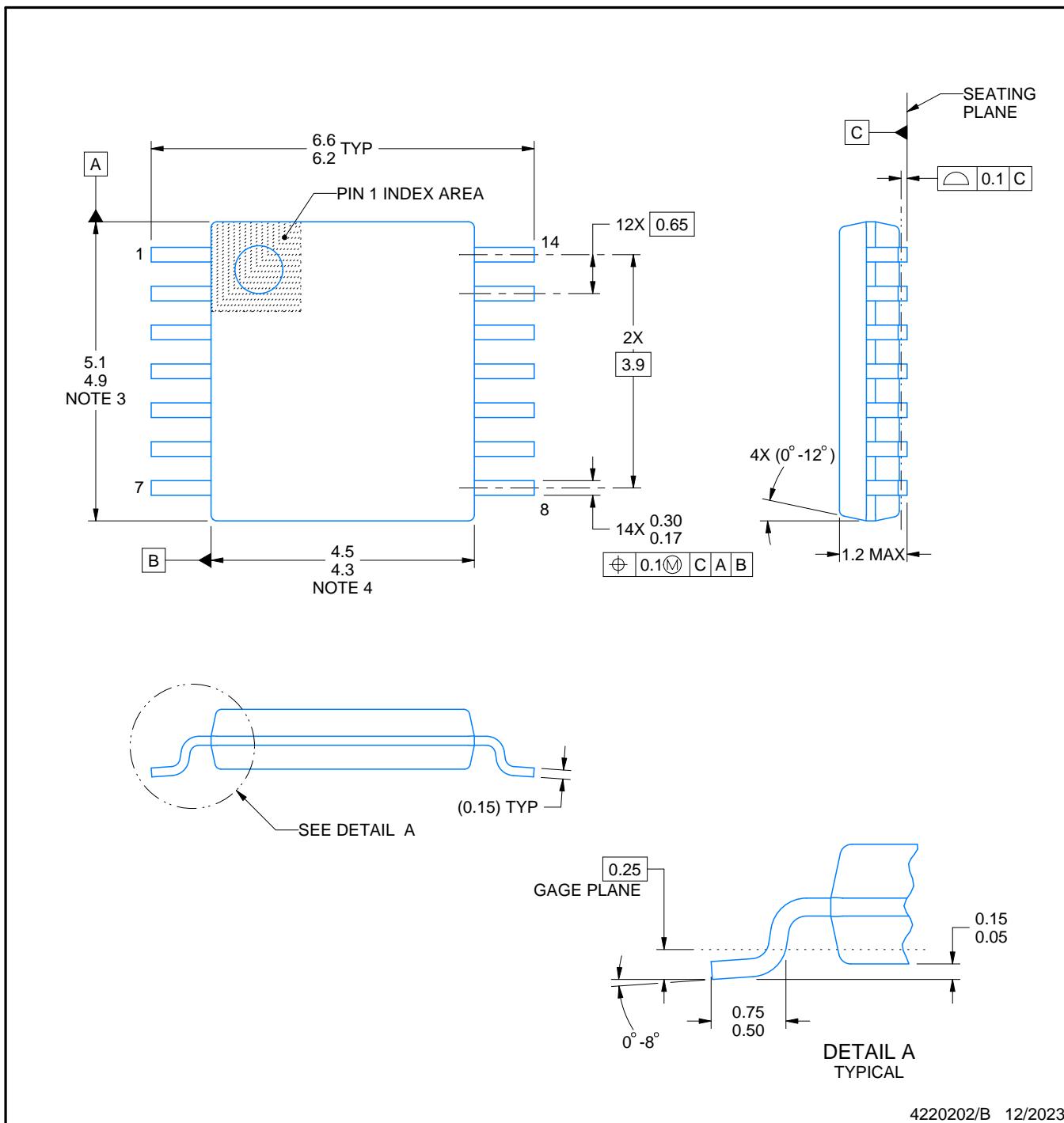
# PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

## NOTES:

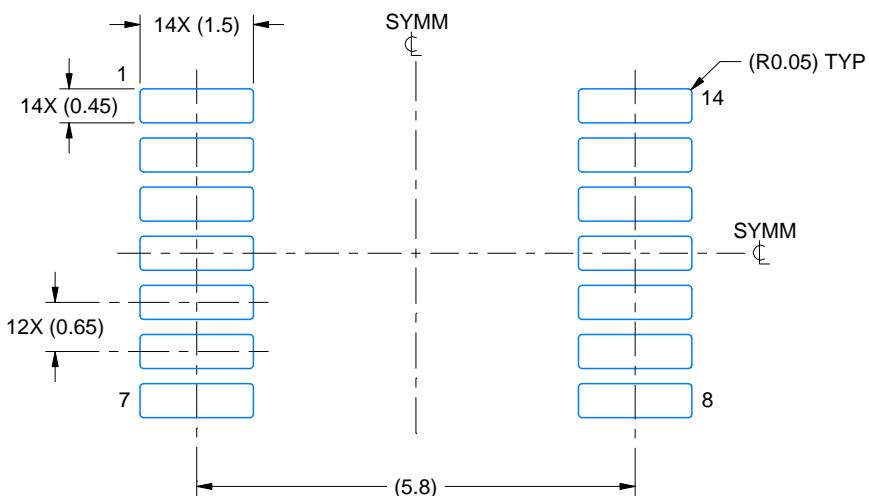
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

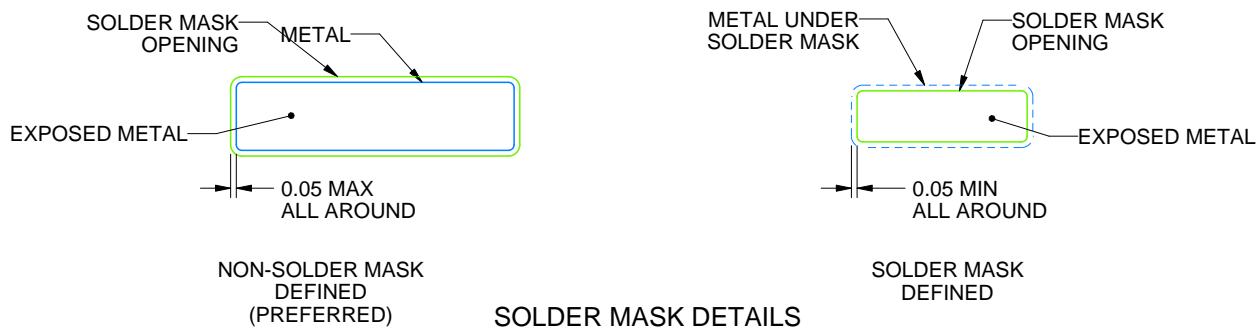
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

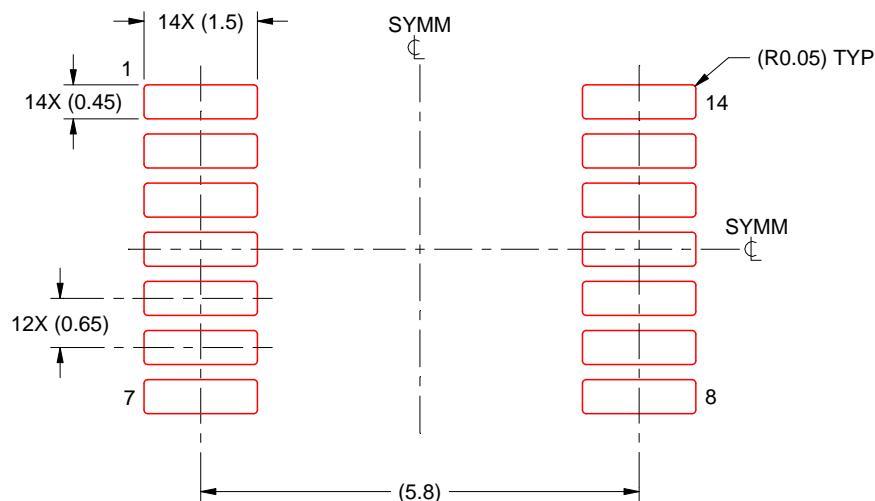
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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