# CD4085B Types

## CMOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (20-Volt Rating)

■ CD4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

The CD4085B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

*Features:*

■ Medium-speed operation — $t_{PHL}$ = 90 ns; $t_{PLH}$ = 125 ns (typ.) at 10 V
■ Individual inhibit controls
■ Standardized symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 $\mu$A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (over full package-temperature range):
   1 V at $V_{DD}$ = 5 V
   2 V at $V_{DD}$ = 10 V
   2.5 V at $V_{DD}$ = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



E = $\overline{INHIBIT + AB + CD}$
LOGIC I = HIGH
LOGIC 0 = LOW

$V_{DD}$ = 14
$V_{SS}$ = 7

92CS-23690R2

**FUNCTIONAL DIAGRAM**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*
DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
Voltages referenced to $V_{SS}$ Terminal) ................................................ -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ................................................ -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ................................................ ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
   For $T_A$ = -55°C to +100°C ................................................ 500mW
   For $T_A$ = +100°C to +125°C ................................................ Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
   FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ................................................ 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ................................................ -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ................................................ -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
   At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ................................................ +265°C
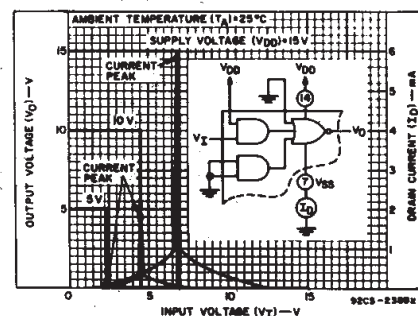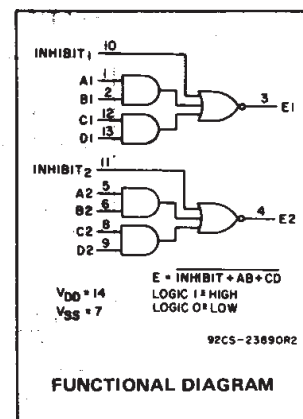


*Fig. 1 — Typical voltage and current transfer characteristics.*
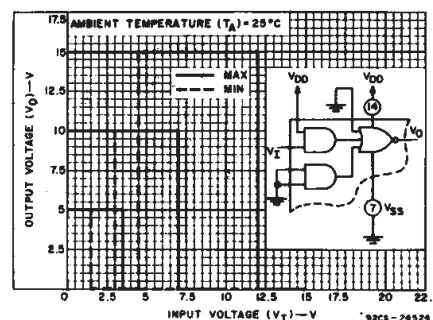


*Fig. 2 — Min. and max. voltage transfer characteristics.*

**RECOMMENDED OPERATING CONDITIONS**
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

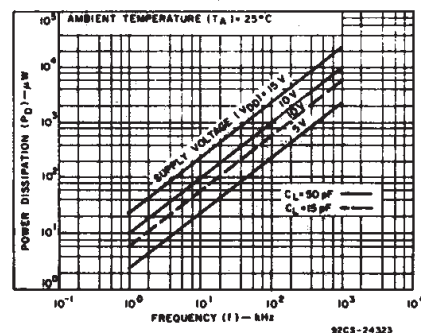| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | 3 | 18 | V |



| | |
|---|---|
| A1 | 1 • 14 | $V_{DD}$ |
| B1 | 2 • 13 | D1 |
| E1 = $\overline{INH1 + A1B1 + C1D1}$ | 3 • 12 | C1 |
| E2 = $\overline{INH2 + A2B2 + C2D2}$ | 4 • 11 | INHIBIT 2 |
| A2 | 5 • 10 | INHIBIT 1 |
| B2 | 6 • 9 | D2 |
| $V_{SS}$ | 7 • 8 | C2 |

TOP VIEW
92CS-23889R1

**Terminal Assignment**



*Fig. 3 — Typical power dissipation vs. frequency.*

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

## STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-TERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current $I_{DD}$ Max. | − | 0,5 | 5 | 1 | 1 | 30 | 30 | − | 0.02 | 1 | μA |
| | − | 0,10 | 10 | 2 | 2 | 60 | 60 | − | 0.02 | 2 | |
| | − | 0,15 | 15 | 4 | 4 | 120 | 120 | − | 0.02 | 4 | |
| | − | 0,20 | 20 | 20 | 20 | 600 | 600 | − | 0.04 | 20 | |
| Output Low (Sink) Current, $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | − | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | − | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | − | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | − | |
| | 2.5 | 0,5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | − | |
| | 9.5 | 0,10 | 10 | −1.6 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | − | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | − | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | − | 0,5 | 5 | 0.05 | | | | − | 0 | 0.05 | V |
| | − | 0,10 | 10 | 0.05 | | | | − | 0 | 0.05 | |
| | − | 0,15 | 15 | 0.05 | | | | − | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | − | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | − | |
| | − | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | − | |
| | − | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | − | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5,4.5 | − | 5 | 1.5 | | | | − | − | 1.5 | V |
| | 1,9 | − | 10 | 3 | | | | − | − | 3 | |
| | 1.5,13.5 | − | 15 | 4 | | | | − | − | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5,4.5 | − | 5 | 3.5 | | | | 3.5 | − | − | |
| | 1,9 | − | 10 | 7 | | | | 7 | − | − | |
| | 1.5,13.5 | − | 15 | 11 | | | | 11 | − | − | |
| Input Current, $I_{IN}$ Max. | − | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | − | $±10^{-5}$ | ±0.1 | μA |
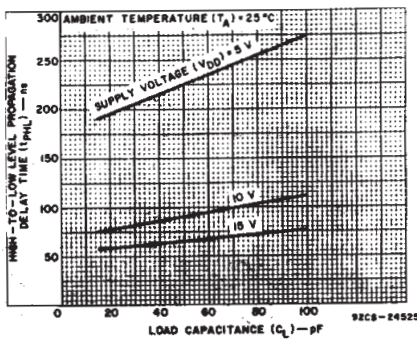


Fig. 4 – Typical data high-to-low level propagation delay time vs. load capacitance.
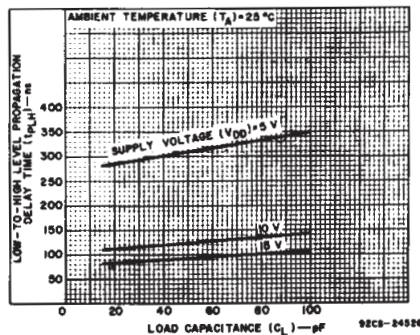


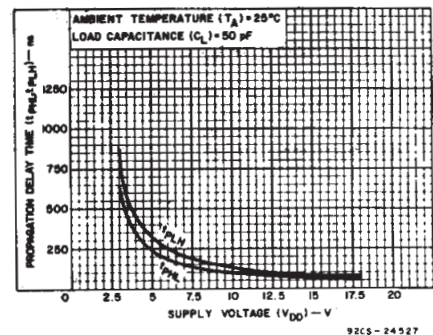Fig. 5 – Typical data low-to-high level propagation delay time vs. load capacitance.



Fig. 6 – Typical data propagation delay time vs. supply voltage.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at $T_A$ = 25°C; Input $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 K$\Omega$

| CHARACTERISTIC | | CONDITIONS $V_{DD}$ V | LIMITS | | UNITS |
|---|---|---|---|---|---|
| | | | Typ. | Max. | |
| Propagation Delay Time (Data): | | 5 | 225 | 450 | |
| High-to-Low Level, | $t_{PHL}$ | 10 | 90 | 180 | ns |
| | | 15 | 65 | 130 | |
| Low-to-High Level, | $t_{PLH}$ | 5 | 310 | 620 | |
| | | 10 | 125 | 250 | ns |
| | | 15 | 90 | 180 | |
| Propagation Delay Time (Inhibit): | | 5 | 150 | 300 | |
| High-to-Low Level, | $t_{PHL}$ | 10 | 60 | 120 | ns |
| | | 15 | 40 | 80 | |
| Low-to-High Level, | $t_{PLH}$ | 5 | 250 | 500 | |
| | | 10 | 100 | 200 | ns |
| | | 15 | 70 | 140 | |
| Transition Time, | $t_{THL}$, $t_{TLH}$ | 5 | 100 | 200 | |
| | | 10 | 50 | 100 | ns |
| | | 15 | 40 | 80 | |
| Input Capacitance, | $C_{IN}$ | Any Input | 5 | 7.5 | pF |
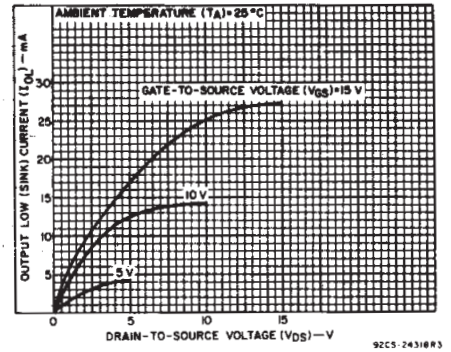


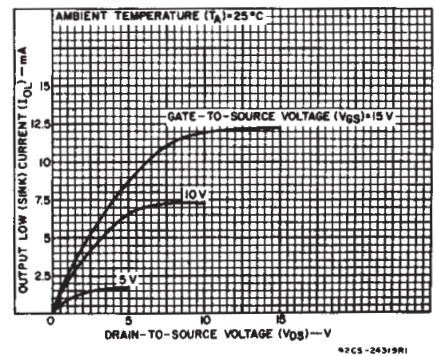Fig. 7 — Typical output low (sink) current characteristics.



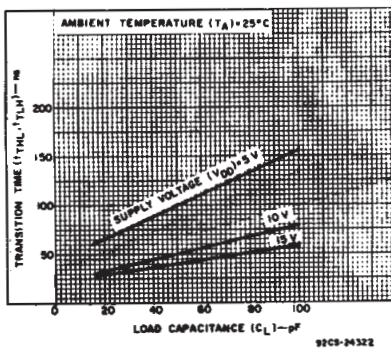Fig. 8 — Minimum output low (sink) current characteristics.



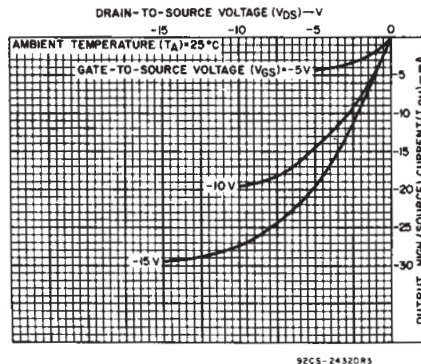Fig. 9 — Typical transition time vs. load capacitance.



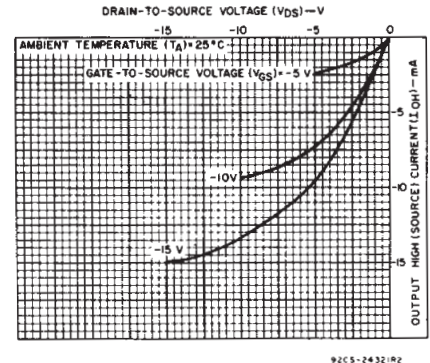Fig. 10 — Typical output high (source) current characteristics.



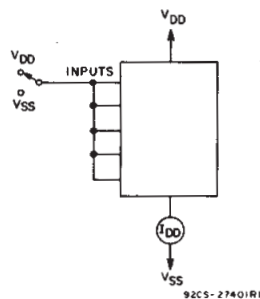Fig. 11 — Minimum output high (source) current characteristics.



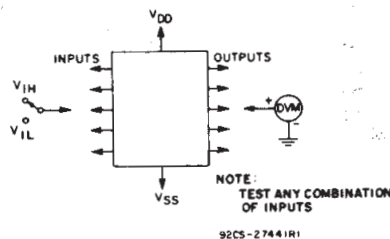Fig. 12 — Quiescent device current test circuit.



Fig. 13 — Input voltage test circuit.
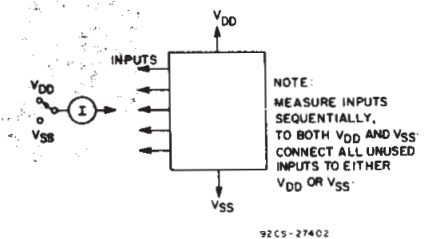


Fig. 14 — Input current test circuit.

3

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Fig. 15 — CD4085 schematic diagram.

* ALL INPUTS PROTECTED BY STANDARD CMOS PROTECTION NETWORK

TERM.14 = $V_{DD}$
TERM. 7 = $V_{SS}$

92CL-23891R1



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).

48 – 56
(1.219 – 1.422)

4 – 10
(0.102 – 0.254)

46 – 54
(1.168 – 1.372)

92CS-32204

Dimensions and Pad Layout for CD4085BH.

## PACKAGING INFORMATION

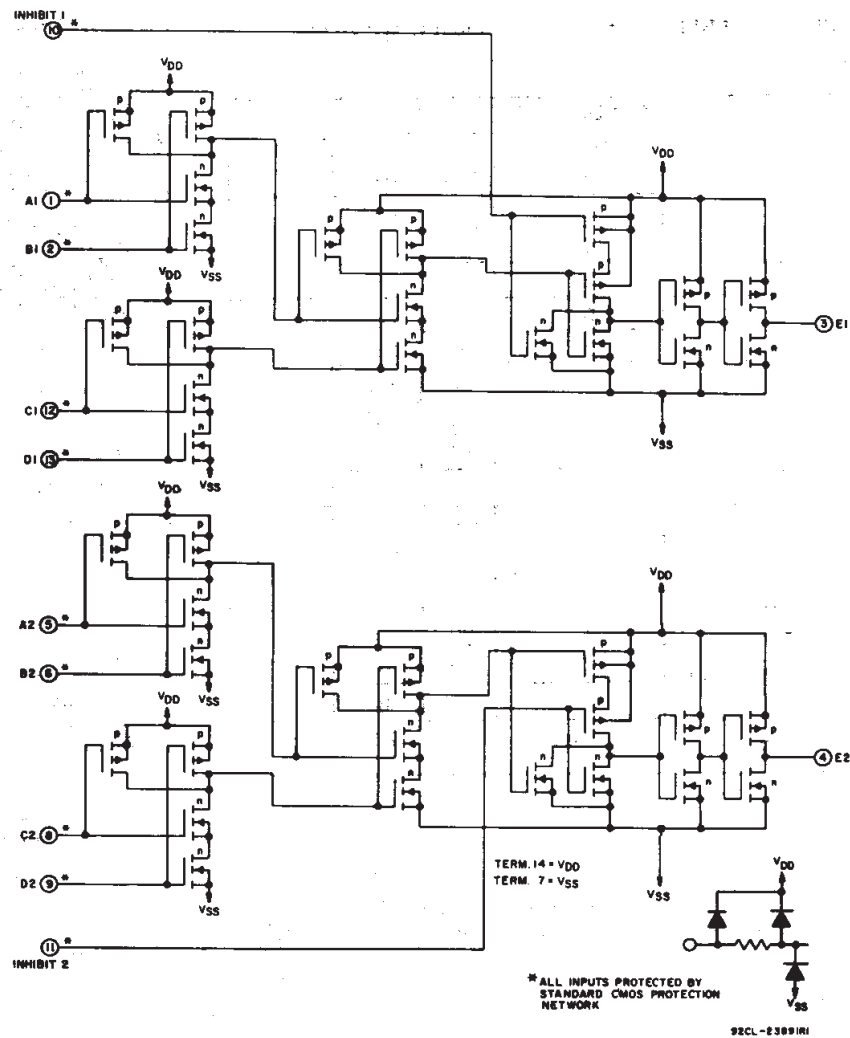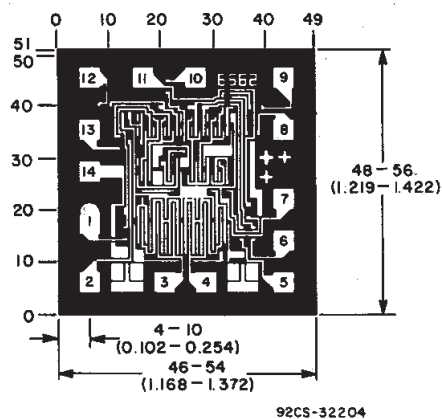| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CD4085BE | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4085BE |
| CD4085BE.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4085BE |
| CD4085BF | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4085BF |
| CD4085BF.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4085BF |
| CD4085BF3A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4085BF3A |
| CD4085BF3A.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4085BF3A |
| CD4085BM | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4085BM |
| CD4085BM.A | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4085BM |
| CD4085BPWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM085B |
| CD4085BPWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM085B |

**(1)** **Status:** For more details on status, see our product life cycle.

**(2)** **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3)** **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4)** **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5)** **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6)** **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD4085B, CD4085B-MIL :**

● Catalog : CD4085B

● Military : CD4085B-MIL

NOTE: Qualified Version Definitions:

 ● Catalog - TI's standard catalog product

 ● Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**

Cavity

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Sprocket Holes

| Q1 | Q2 |   | Q1 | Q2 |
| Q3 | Q4 |   | Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4085BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| CD4085BPWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

## TUBE



T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

\*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD4085BE | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4085BE | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4085BE.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4085BE.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4085BM | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| CD4085BM.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

6.2
5.8 TYP

A

PIN 1 ID
AREA

1

14

12X 1.27

8.75
8.55
NOTE 3

2X
7.62

7

8

14X 0.51
0.31

B

4.0
3.8
NOTE 4

⊕ 0.25Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

1.75 MAX

SEE DETAIL A

0.25
0.13 TYP

0.25
GAGE PLANE

0° - 8°

1.27
0.40

0.25
0.10

**DETAIL A**
TYPICAL

4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

14

SYMM

7

8

(R0.05)
TYP

(5.4)

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## D0014A

14X (1.55)

SYMM

1

14X (0.6)

14

12X (1.27)

SYMM

7

8

(5.4)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

TEXAS
INSTRUMENTS

PIN 1 ID
(OPTIONAL)

A

1

12X | .100
[2.54]

14

7

8

B

.245-.283
[6.22-7.19]

.754-.785
[19.15-19.94]

4X .005 MIN
[0.13]

.015-.060  TYP
[0.38-1.52]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ | .010 [0.25] | C | A | B

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015
[0.38]

GAGE PLANE

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A   05/2017

NOTES:

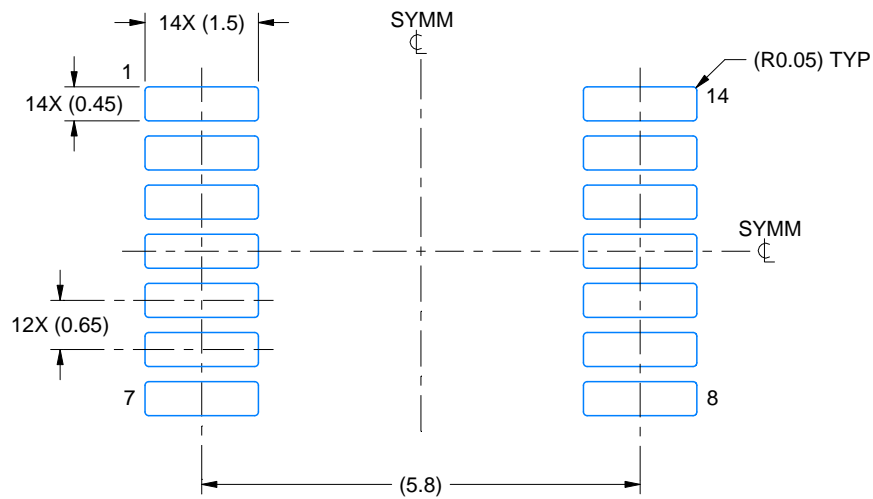1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

**TEXAS INSTRUMENTS**
www.ti.com

(.300 ) TYP
[7.62]

SEE DETAIL  A

SEE DETAIL  B

1

14

12X (.100 )
[2.54]

14X (Ø .039)
[1]

SYMM
℄

7

8

SYMM
℄

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002  MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002 ) TYP
[0.05]

DETAIL  A
SCALE: 15X

METAL

(Ø .063)
[1.6]

SOLDER MASK
OPENING

.002  MAX
[0.05]
ALL AROUND

DETAIL  B
13X, SCALE: 15X

4214771/A   05/2017

TEXAS
INSTRUMENTS
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## N (R−PDIP−T**)　　　　　PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN



| PINS **<br>DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS−001<br>VARIATION | AA | BB | AC | AD |

0.260 (6,60)/0.240 (6,10)

0.070 (1,78)/0.045 (1,14)

0.045 (1,14)/0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)/0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)/0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
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**PW0014A**

SMALL OUTLINE PACKAGE



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

14X (1.5)

14X (0.45)

1

SYMM

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.5)

1

14X (0.45)

SYMM

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER