

## CD40x7B CMOS アナログ マルチプレクサ / デマルチプレクサ

### 1 特長

- 高電圧タイプ (20V 定格)
  - CD4067B – シングル 16 チャンネル マルチプレクサ / デマルチプレクサ
- 低いオン抵抗: 15V<sub>P-P</sub> 信号入力範囲で、V<sub>DD</sub> - V<sub>SS</sub> = 15V において 125Ω (代表値)
- 高いオフ抵抗: V<sub>DD</sub> - V<sub>SS</sub> = 10V でチャンネル リーク ±10pA (代表値)
- マッチングされたスイッチ特性: V<sub>DD</sub> - V<sub>SS</sub> = 15V において R<sub>ON</sub> = 5Ω (代表値)
- あらゆるデジタル制御入力および電源条件で非常に低い静止消費電力: V<sub>DD</sub> - V<sub>SS</sub> = 10V において 0.2μW (代表値)
- オンチップでバイナリ アドレスをデコード
- 5V、10V、15V のパラメータ定格
- 20V で静止電流を 100% テスト済み
- 標準化された対称出力特性
- パッケージの温度範囲全体にわたって 18V 時に最大入力電流 1μA: 25°C で 18V 時に 100nA
- JEDEC 暫定標準 No. 13-B 『Standard Specifications for Description of "B" Series CMOS Devices』のすべての要件に適合

### 2 アプリケーション

- アナログ信号とデジタル多重化
- 伝送ゲート ロジックの実装
- A/D 変換と D/A 変換
- 信号ゲーティング

### 3 概要

CD40x7B CMOS アナログ マルチプレクサ / デマルチプレクサは、オン状態のインピーダンスとオフ状態のリーク電流が低く、内部アドレス デコード機能を備えたデジタル制御のアナログ スイッチです。これらのデバイスをデマルチプレクサとして使用する場合は、チャンネルの IN 端子または OUT 端子が出力となり、共通 OUT 端子または IN 端子が入力となります。また、オン抵抗は入力範囲全体にわたって比較的一定です。

CD4067B は、4 つのバイナリ制御入力 A、B、C、D と 1 つの禁止入力を備えた 16 チャンネル マルチプレクサで、どの入力の組み合わせでも 1 つのスイッチが選択されるように構成されています。

禁止入力にロジック 1 が印加されると、すべてのチャンネルがオフになります。

CD40x7B タイプは、24 リードのハーメチック デュアル インライン セラミック パッケージ (F3A サフィックス)、24 リードのデュアル インライン プラスチック パッケージ (E サフィックス)、24 リードのスマール アウトライン パッケージ (M、M96、NSR サフィックス)、24 リードのシン シュリンク スモール アウトライン パッケージ (P および PWR サフィックス) で供給されます。

#### 製品情報

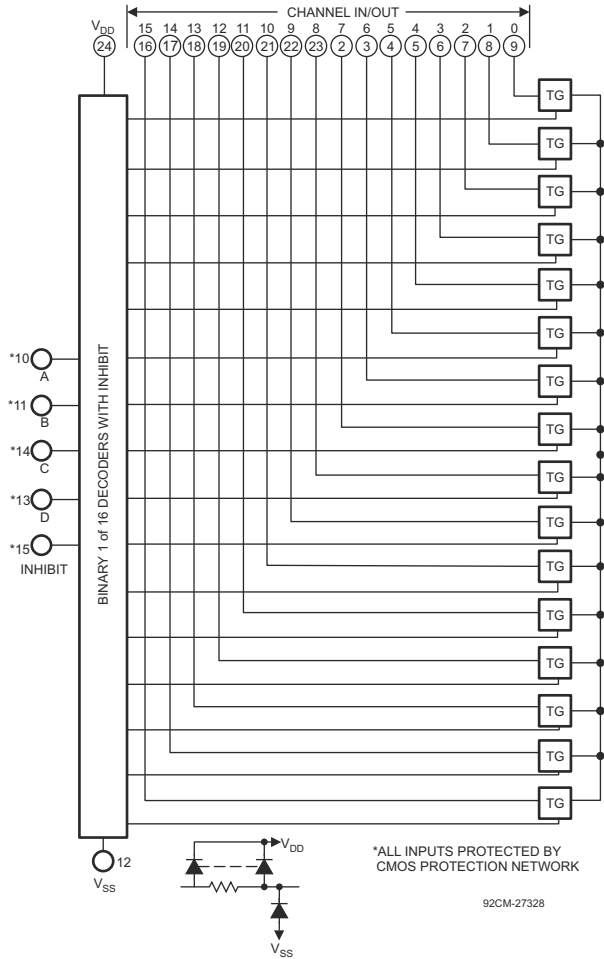
部品番号	チャンネル	パッケージ <sup>(1)</sup>
CD4067B	2 チャンネル 8:1 差動 マルチプレクサ	PW (TSSOP, 24)
		DW (SOIC, 24)

(1) 詳細については、[セクション 11](#) を参照してください。

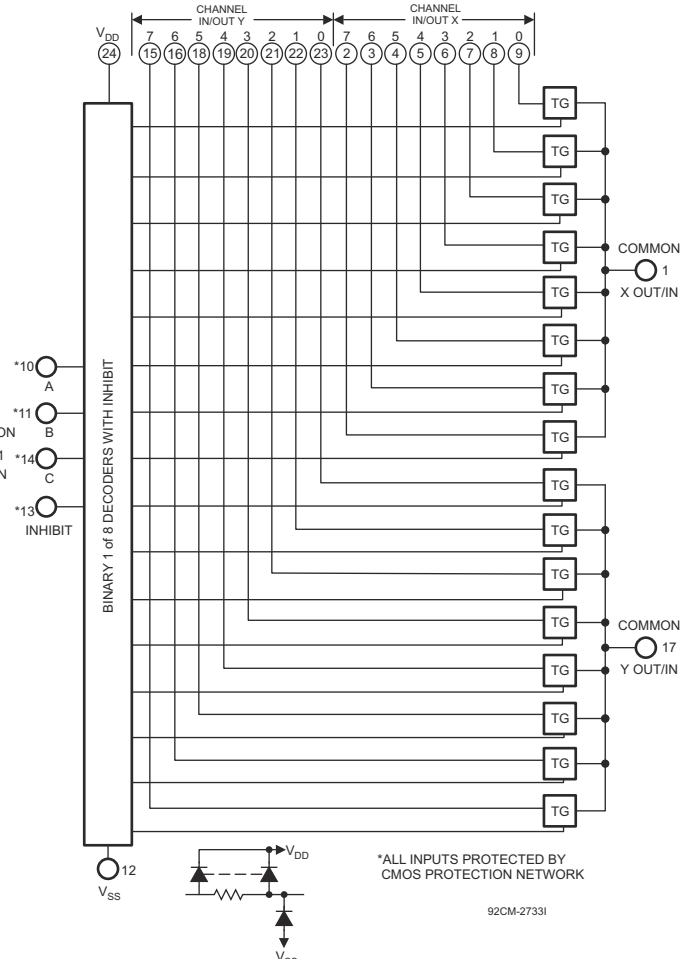


**CD4067B, CD4097B**

JAJSUX9D – JUNE 2003 – REVISED AUGUST 2024



**CD4067 の論理図**



**CD4097 の論理図**

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## 4 Pin Configuration and Functions

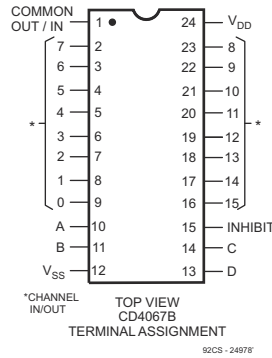


図 4-1. CD4067B 24 Pins (Top View)

表 4-1. Function Table

CD4067 TRUTH TABLE					
A	B	C	D	inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

表 4-2. Function Table

CD4097 TRUTH TABLE				
A	B	C	inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		20	V
$V_{DD}$		-0.5	20	V
$V_{SS}$		-20	0.5	V
$I_{SEL}$ or $I_{EN}$	Logic control input pin current ( $\overline{EN}$ , Ax, SELx)	-30	30	mA
$V_S$ or $V_D$	Source or drain voltage (Sx, D)	$V_{SS}-0.5$	$V_{DD}+0.5$	V
$I_S$ or $I_D$ (CONT)	Source or drain continuous current (Sx, D)	-20	20	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±200	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ <sup>(1)</sup>	Power supply voltage differential	3		18	V
$V_{DD}$	Positive power supply voltage	3		18	V
$V_S$ or $V_D$	Signal path input/output voltage (source or drain pin) (Sx, D)	$V_{SS}$		$V_{DD}$	V
$V_{SEL}$ or $V_{EN}$	Address or enable pin voltage	0		$V_{DD}$	V
$I_S$ or $I_D$ (CONT)	Source or drain continuous current (Sx, D)	-10		10	mA
$T_A$	Ambient temperature	-55		125	°C

- (1)  $V_{DD}$  and  $V_{SS}$  can be any value as long as  $3V \leq (V_{DD} - V_{SS}) \leq 24V$ , and the minimum  $V_{DD}$  is met.

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD406x	CD406x	UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	109.7	101.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	69.4	44.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.9	68.2	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	25.8	3.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	67.1	67.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.5 Electrical Characteristics

Over operating free-air temperature range, V<sub>SUPPLY</sub> = ±5V, and R<sub>L</sub> = 100Ω, (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
<b>SIGNAL INPUTS (V<sub>IS</sub>) AND OUTPUTS (V<sub>OS</sub>)</b>											
I <sub>DD</sub>	Quiescent Device Current	V <sub>IS</sub> = 0 to 5V V <sub>DD</sub> = 5V	T <sub>A</sub> = -55°C					13	μA		
			T <sub>A</sub> = -40°C					13			
			T <sub>A</sub> = 25°C			5	14.5				
			T <sub>A</sub> = 85°C				150				
			T <sub>A</sub> = 125°C				150				
		V <sub>IS</sub> = 0 to 5V V <sub>DD</sub> = 10V	T <sub>A</sub> = -55°C							14	
			T <sub>A</sub> = -40°C							14	
			T <sub>A</sub> = 25°C			6	15.5				
			T <sub>A</sub> = 85°C				300				
			T <sub>A</sub> = 125°C				300				
		V <sub>IS</sub> = 0 to 5V V <sub>DD</sub> = 15V	T <sub>A</sub> = -55°C							20	
			T <sub>A</sub> = -40°C							20	
			T <sub>A</sub> = 25°C			6	20				
			T <sub>A</sub> = 85°C				600				
			T <sub>A</sub> = 125°C				600				
		V <sub>IS</sub> = 0 to 5V V <sub>DD</sub> = 20V	T <sub>A</sub> = -55°C							100	
			T <sub>A</sub> = -40°C							100	
			T <sub>A</sub> = 25°C			7	100				
			T <sub>A</sub> = 85°C				3000				
			T <sub>A</sub> = 125°C				3000				
r <sub>ON</sub>	ON Resistance r <sub>ON</sub> Max	to (V <sub>DD</sub> -V <sub>SS</sub> )/2, V <sub>C</sub> = V <sub>DD</sub> , R <sub>L</sub> = 10kΩ returned V <sub>IS</sub> = V <sub>SS</sub> to V <sub>DD</sub>	V <sub>DD</sub> = 5V	T <sub>A</sub> = -55°C				800	Ω		
				T <sub>A</sub> = -40°C				850			
				T <sub>A</sub> = 25°C			470	1050			
				T <sub>A</sub> = 85°C				1200			
				T <sub>A</sub> = 125°C				1300			
			V <sub>DD</sub> = 10V	T <sub>A</sub> = -55°C							310
				T <sub>A</sub> = -40°C							330
				T <sub>A</sub> = 25°C			180	400			
				T <sub>A</sub> = 85°C				520			
				T <sub>A</sub> = 125°C				550			
			V <sub>DD</sub> = 15V	T <sub>A</sub> = -55°C							200
				T <sub>A</sub> = -40°C							210
T <sub>A</sub> = 25°C				125	240						
T <sub>A</sub> = 85°C					300						
V <sub>DD</sub> = 15V	T <sub>A</sub> = 125°C						320				

## 5.5 Electrical Characteristics (続き)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100\Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER			TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$\Delta R_{ON}$	On-state resistance difference between any two switches		$R_L = 10k\Omega, V_C = V_{DD}$	$V_{DD} = 5V$				15		$\Omega$	
	On-state resistance difference between any two switches	On-state resistance difference between any two switches		$V_{DD} = 10V$				10			
	On-state resistance difference between any two switches	On-state resistance difference between any two switches		$V_{DD} = 15V$				5			
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)				$V_{DD} - V_{SS} = 18V$	$T_A = -55^\circ C$			$\pm 100$	$nA$		
				$T_A = -40^\circ C$			$\pm 100$				
				$T_A = 25^\circ C$		$\pm 0.1$	$\pm 100^{(2)}$				
				$T_A = 85^\circ C$			$\pm 1000^{(2)}$				
				$T_A = 125^\circ C$			$\pm 1000^{(2)}$				
$C_{IS}$	Input capacitance	$V_S = 0V$ $f = 1MHz$ CD4067	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$		5		pF	
$C_{OS}$	Output capacitance	$V_S = 0V$ $f = 1MHz$ CD4067	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$		55		pF	
$C_{OS}$	Output capacitance	$V_S = 0V$ $f = 1MHz$ CD4097	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$		35		pF	
$C_{IOS}$	Feed through	$V_S = 0V$ $f = 1MHz$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$	$V_{DD} = 5V, V_C = V_{SS} = -5V$		0.2		pF	
$V_{IHC}$	Control input, high voltage		See Figure 6-1	$V_{DD} = 5V$					3.5		V
				$V_{DD} = 10V$					7		V
				$V_{DD} = 15V$					11		V
$V_{ILC}$	Control input, low voltage (max)			$V_{DD} = 5V$				1			V
				$V_{DD} = 10V$				1			V
				$V_{DD} = 15V$				1			V
$I_{IN}$	Input current (max)		$V_{IS} \leq V_{DD}, V_{DD} - V_{SS} = 18V, V_{CC} \leq V_{DD} - V_{SS}, V_{DD} = 18V$	$T_A = -55^\circ C$				-0.1	1	$\mu A$	
				$T_A = -40^\circ C$				-0.1	1		
	$T_A = 25^\circ C$				-0.1	0.0001	1				
	$T_A = 85^\circ C$				-1	1					
	Input current (max)	Input current (max)		$T_A = 125^\circ C$				-1	1		
$C_{IN}$	Input Capacitance						5	7.5		pF	
BW	-3dB cutoff frequency (switch on)	CD4067	$V_C = V_{DD} = 5V, V_{SS} = -5V, V_{IS(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$ Common Out/In				14		$MHz$		
		CD4097					20				
	-3dB cutoff frequency (switch on)		$V_C = V_{DD} = 5V, V_{SS} = -5V, V_{IS(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$ Any channel				60				
THD	Total Harmonic Distortion	Total Harmonic Distortion	$V_C = V_{DD} = 5V, V_{SS} = 0V, V_{IS(p-p)} = 2V$ (sine wave centered on 0V), $R_L = 10k\Omega, f_{IS} = 1-kHz$ sine wave				0.3		$\%$		
			$V_C = V_{DD} = 10V, V_{SS} = 0V, V_{IS(p-p)} = 3V$ (sine wave centered on 0V), $R_L = 10k\Omega, f_{IS} = 1-kHz$ sine wave				0.2				
			$V_C = V_{DD} = 15V, V_{SS} = 0V, V_{IS(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 10k\Omega, f_{IS} = 1-kHz$ sine wave				0.12				
OISO	-40dB feed through frequency (switch off)	CD4067	$V_C = V_{DD} = 5V, V_{SS} = -5V, V_{IS(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$ Common Out/In				20		$MHz$		
		CD4097					12				
	-40dB feed through frequency (switch off)		$V_C = V_{DD} = 5V, V_{SS} = -5V, V_{IS(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$ Any channel				8				
XTALK	-40dB crosstalk frequency	Any 2 Channels					1		$MHz$		
		CD4097 on Common	$V_C = V_{DD} = 5V, V_{SS} = -5V, V_{IS(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$				10				
		CD4097 on Any					18				

### 5.5 Electrical Characteristics (続き)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100\Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crosstalk (control input to signal output)	$V_C = 10V$ (square wave), $R_L = 10k\Omega$ , $V_{DD} = 10V$					75		mV

- (1) Peak-to-Peak voltage symmetrical about  $(V_{DD} - V_{EE}) / 2$ .
- (2) Determined by minimum feasible leakage measurement for automatic testing.

### 5.6 AC Performance Characteristics

$V_{DD} = +15V$ ,  $V_{SS} = V_{EE} = 0V$ ,

$T_A = 25^\circ C$  (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$t_{pd}$	Signal Input	Signal Output	$V_{IN} = V_{DD}$ , $C_L = 50$ pF, $R_L = 1k\Omega$	5V		30	60	ns
				10V		15	30	
				15V		7	20	
$t_{ph}$	Signal Input	Signal Output	$V_{IN} = V_{DD}$ , $C_L = 50$ pF, $R_L = 1k\Omega$	5V		325	650	ns
				10V		135	270	
				15V		95	190	
$t_{phi}$	Signal Input	Signal Output	$V_{IN} = V_{DD}$ , $C_L = 50$ pF, $R_L = 1k\Omega$	5V		220	440	ns
				10V		90	180	
				15V		65	130	

### 5.7 Typical Characteristics

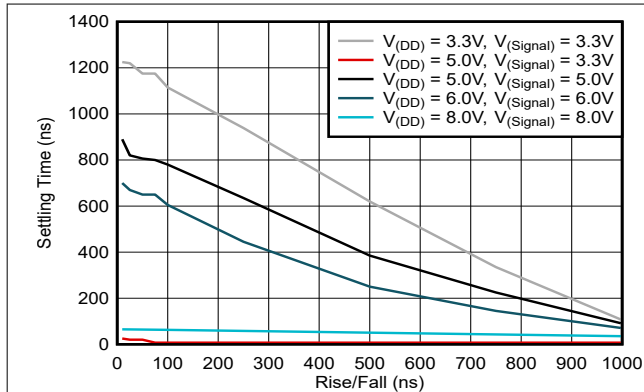


図 5-1. System Settling Time vs Signal Rise/Fall Time

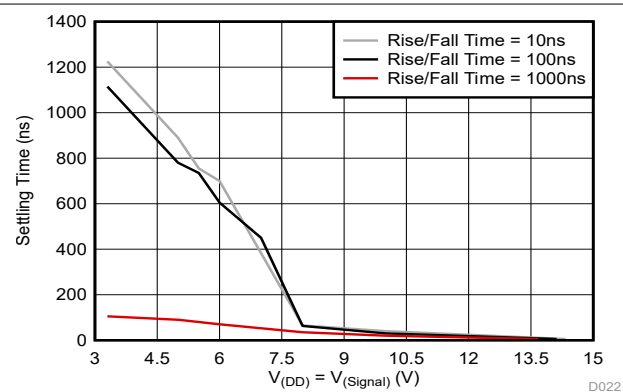


図 5-2. System Settling Time vs Signal Voltage

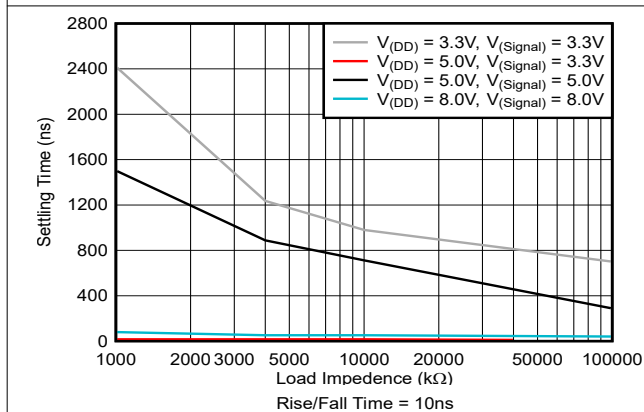


図 5-3. System Settling Time vs Signal Voltage

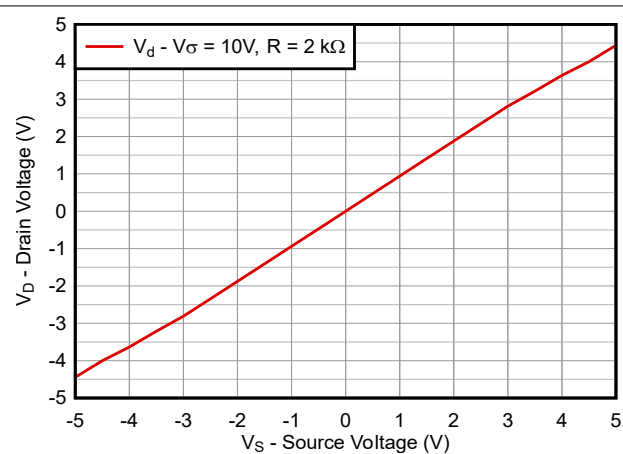
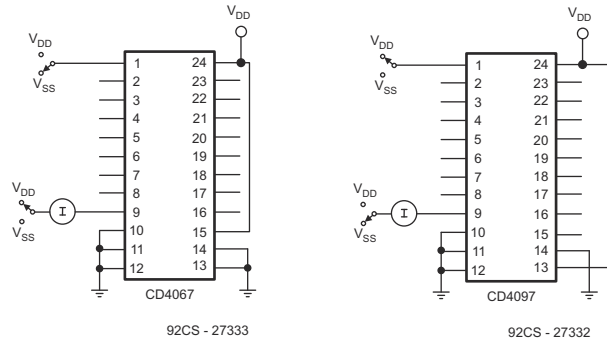


図 5-4. Source Voltage Input vs Drain Voltage Output

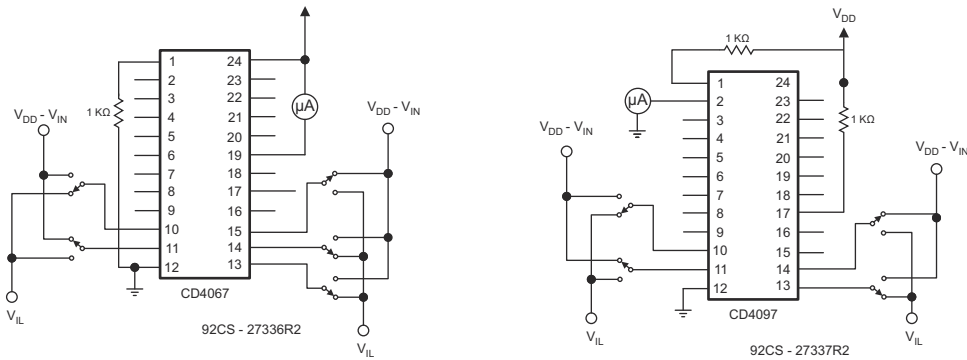


## 6 Parameter Measurement Information

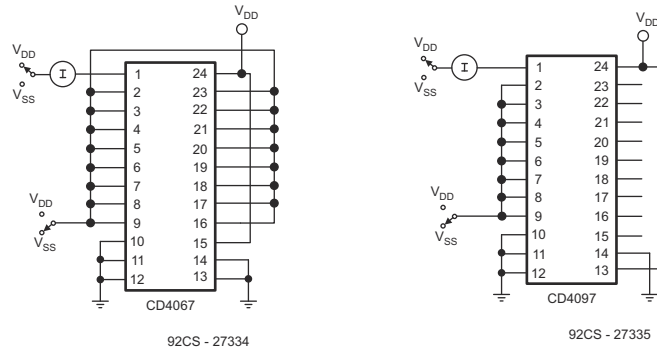
### 6.1 Test Circuits



**図 6-1. OFF Channel Leakage Current – Any Channel OFF**



**図 6-2. Input Voltage – Measure <2μA on all OFF Channels (For Example, Channel 12)**



**図 6-3. OFF Channel Leakage Current – All Channels OFF**

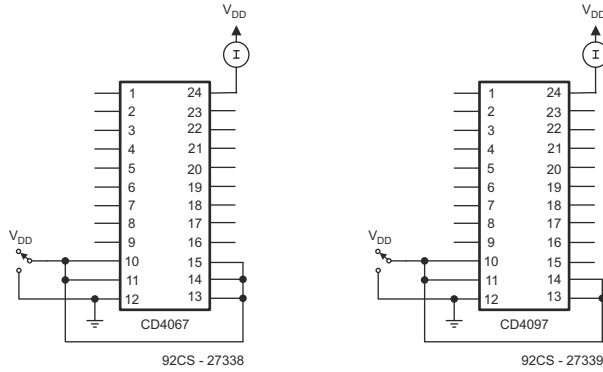


图 6-4. Quiescent Device Current

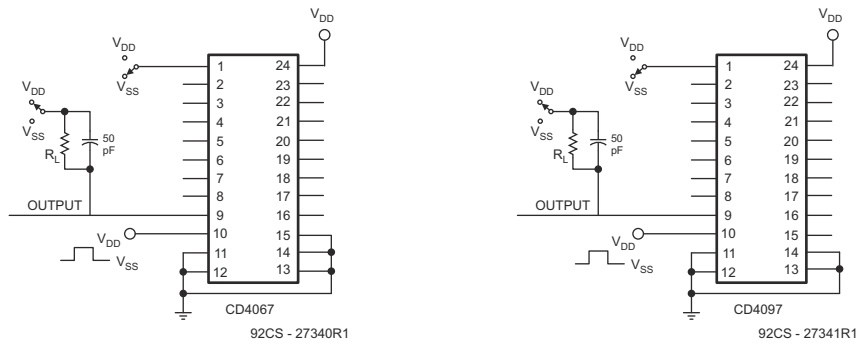


图 6-5. Turn-on and Turn-off Propagation Delay – Address Select Input to Signal Output (For Example,, Measured on Channel 0)

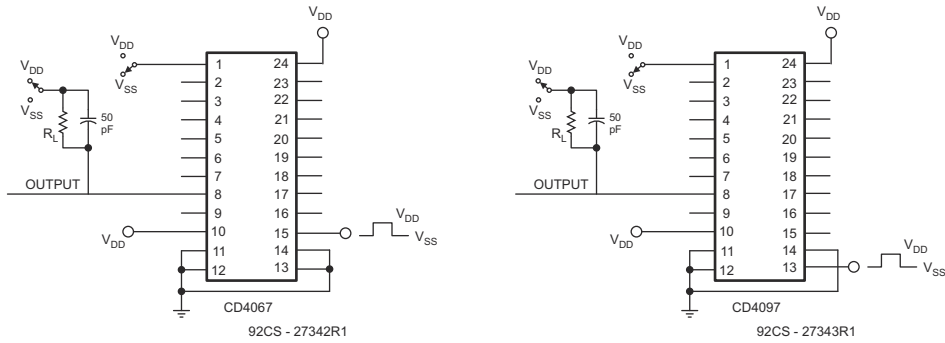


图 6-6. Turn-on and Turn-off Propagation Delay – Inhibit Input to Signal Output (For Example,, Measured on Channel 1)

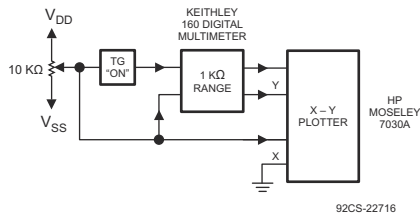


图 6-7. Channel ON Resistance Measurement Circuit

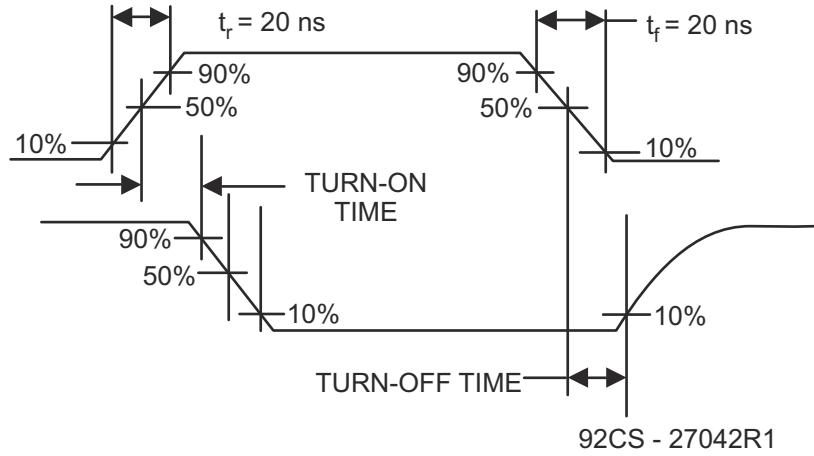


図 6-8. Propagation Delay Waveform Channel Being turned ON ( $R_L = 10k\Omega$ ,  $C_L = 50$  pF)

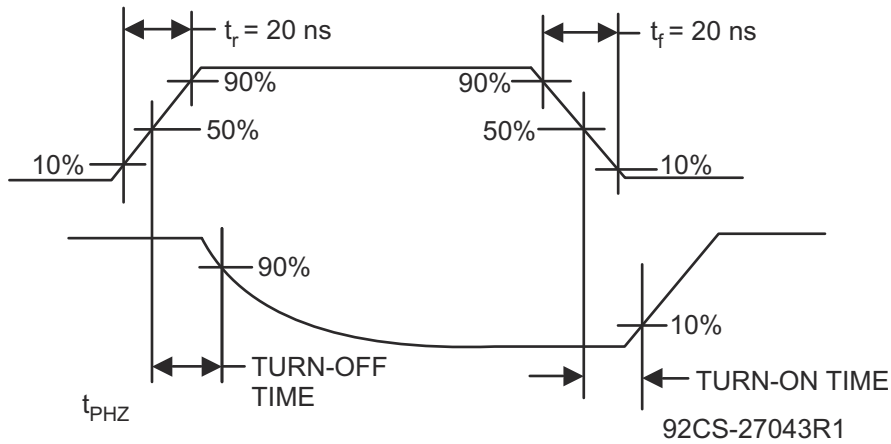


図 6-9. Propagation Delay Waveform Channel Being turned OFF ( $R_L = 300\Omega$ ,  $C_L = 50$  pF)

## 7 Detailed Description

### 7.1 Functional Block Diagram

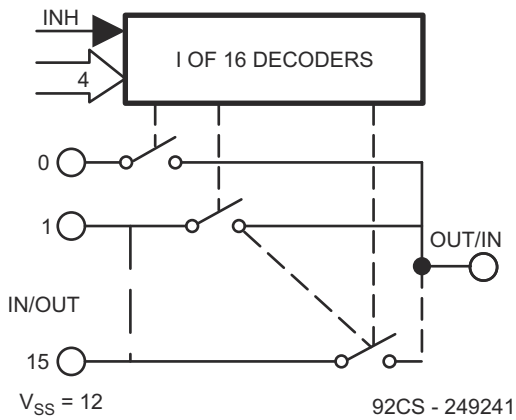


図 7-1. CD4067

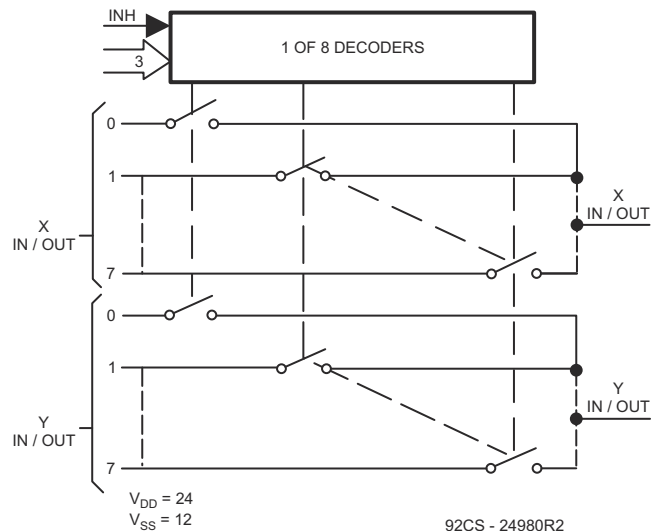


図 7-2. CD4097

### 7.2 Device Functional Modes

表 7-1. Function Table

CD4067 TRUTH TABLE					
A	B	C	D	inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

**表 7-2. Function Table**

CD4097 TRUTH TABLE				
A	B	C	inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

## 8 Application and Implementation

### 注

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### 8.1 Application Information

#### 8.1.1 Special Considerations

In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD40x7B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also, when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to  $V_{SS}$ , which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to  $V_{SS}$ .

The amount of charge dumped is mostly a function of the signal level above  $V_{SS}$ . Typically, at  $V_{DD}-V_{SS} = 10V$ , a 100pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 $\mu$ s. When the inhibit signal turns a channel off, there is no charge dumping to  $V_{SS}$ . Rather, there is a slight rise in the channel voltage level (65mV typical) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8V (calculated from  $R_{TON}$  values shown in *Electrical Characteristics* tables). No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.

### 8.2 Typical Application

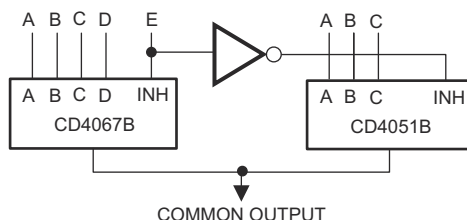


図 8-1. 18-24-to-1 MUX Addressing

## 9 Device and Documentation Support

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (July 2024) to Revision D (August 2024)	Page
• Added Settling Time plots.....	8

Changes from Revision B (June 2003) to Revision C (July 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• Changed max and typ IDD for lower supply voltages.....	6
• Changed max IIN at low temperature.....	6

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD4067BF</a>	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4067BF
CD4067BF.A	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4067BF
<a href="#">CD4067BF3A</a>	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4067BF3A
CD4067BF3A.A	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4067BF3A
<a href="#">CD4067BM</a>	Obsolete	Production	SOIC (DW)   24	-	-	Call TI	Call TI	-55 to 125	CD4067BM
<a href="#">CD4067BM96</a>	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM
CD4067BM96.A	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM
<a href="#">CD4067BM96G4</a>	Obsolete	Production	SOIC (DW)   24	-	-	Call TI	Call TI	-55 to 125	CD4067BM
<a href="#">CD4067BPW</a>	Obsolete	Production	TSSOP (PW)   24	-	-	Call TI	Call TI	-55 to 125	CM067B
<a href="#">CD4067BPWR</a>	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B
CD4067BPWR.A	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B
<a href="#">CD4097BF</a>	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4097BF
CD4097BF.A	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4097BF
<a href="#">CD4097BM</a>	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM
CD4097BM.A	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM
CD4097BME4	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM
CD4097BMG4	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM
<a href="#">CD4097BPW</a>	NRND	Production	TSSOP (PW)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B
CD4097BPW.A	NRND	Production	TSSOP (PW)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B
<a href="#">CD4097BPWR</a>	NRND	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B
CD4097BPWR.A	NRND	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B
CD4097BPWRE4	NRND	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.



(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD4067B, CD4067B-MIL, CD4097B, CD4097B-MIL :**

● Catalog : [CD4067B](#), [CD4097B](#)

● Military : [CD4067B-MIL](#), [CD4097B-MIL](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4067BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4067BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CD4097BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4067BM96	SOIC	DW	24	2000	350.0	350.0	43.0
CD4067BPWR	TSSOP	PW	24	2000	353.0	353.0	32.0
CD4097BPWR	TSSOP	PW	24	2000	353.0	353.0	32.0

**TUBE**

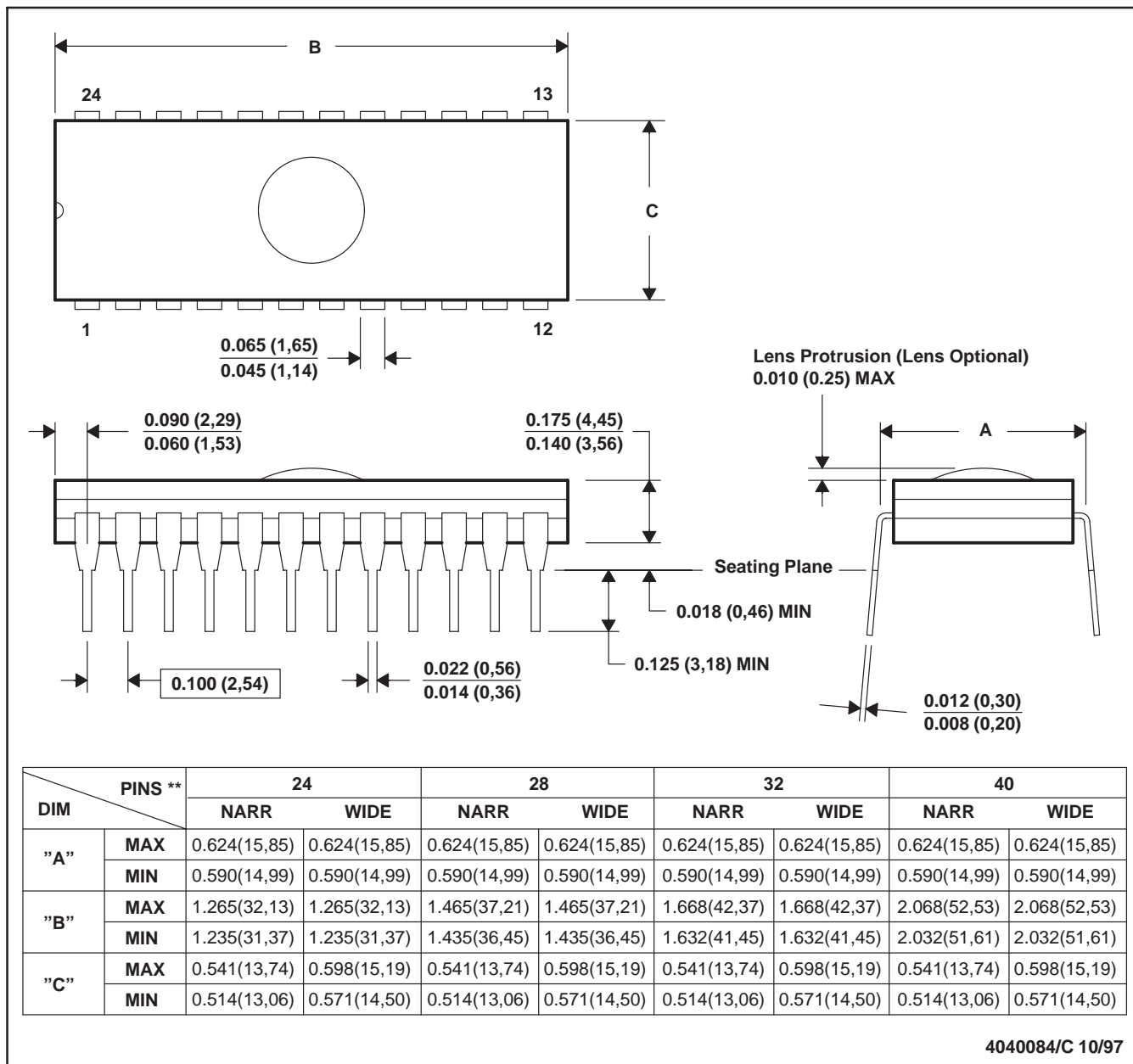

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4097BM	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4097BM.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4097BME4	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4097BMG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4097BPW	PW	TSSOP	24	60	530	10.2	3600	3.5
CD4097BPW.A	PW	TSSOP	24	60	530	10.2	3600	3.5

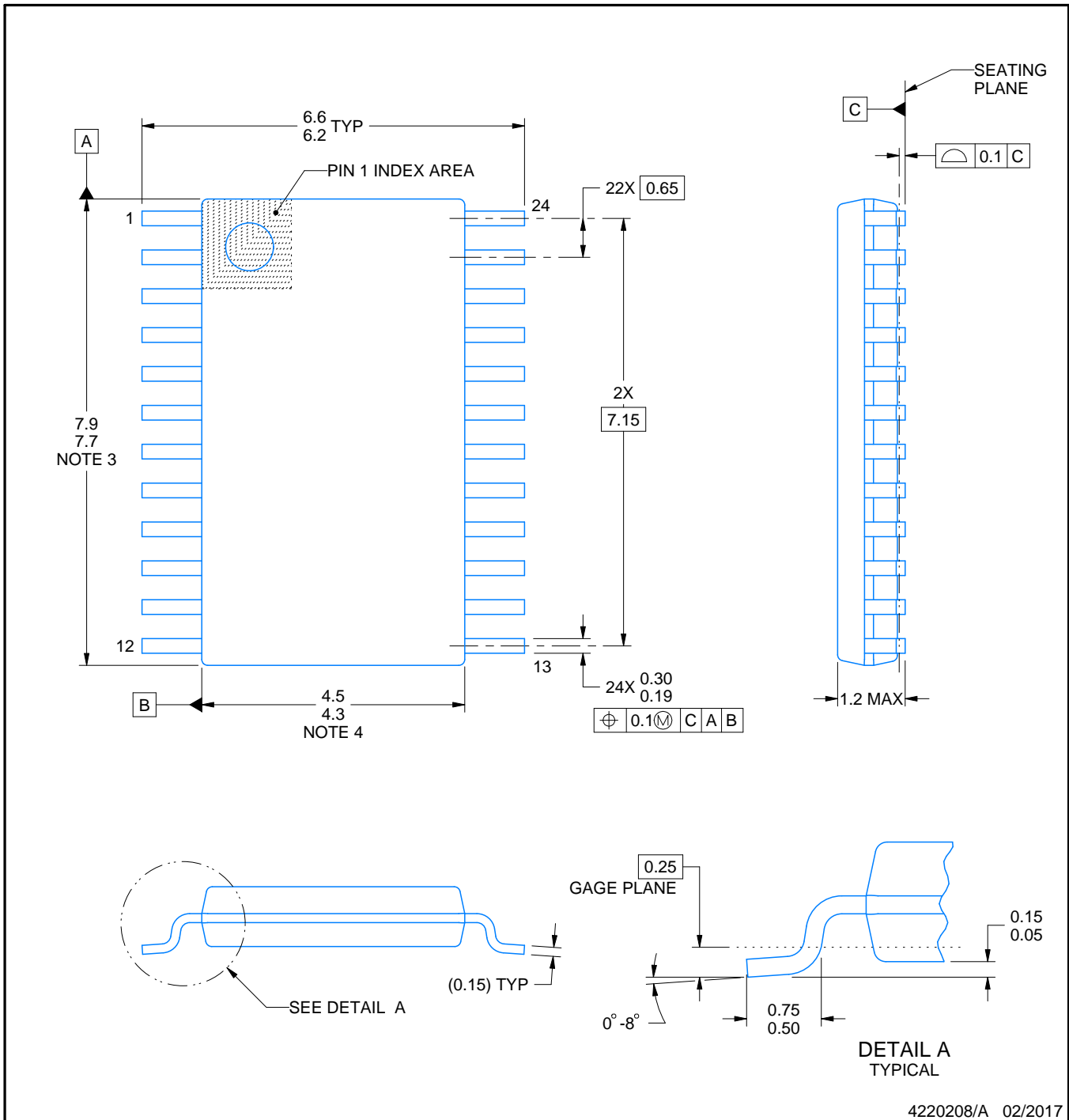
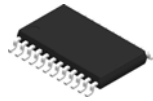
J (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).  
 D. This package can be hermetically sealed with a ceramic lid using glass frit.  
 E. Index point is provided on cap for terminal identification.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



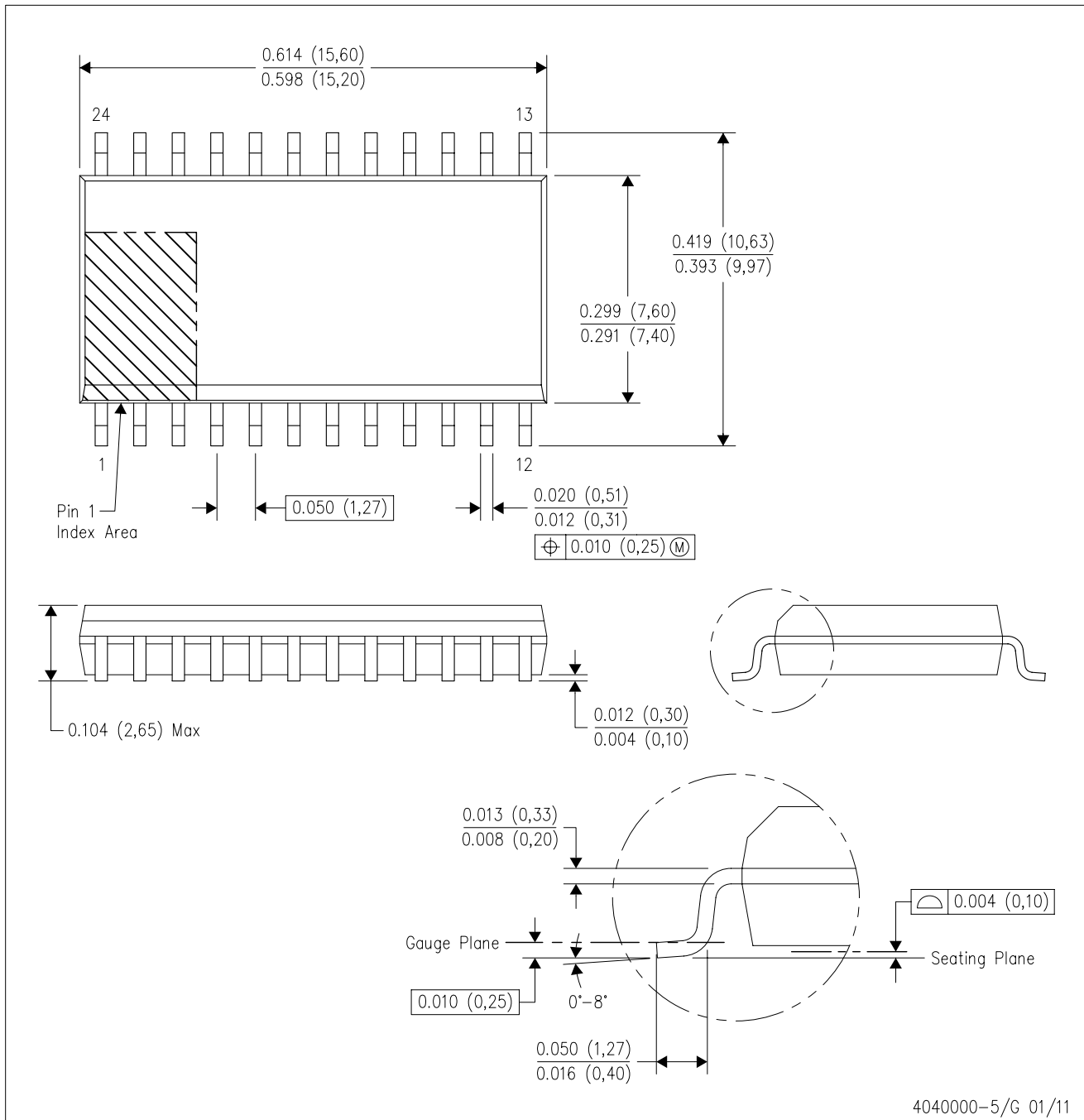
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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最終更新日：2025 年 10 月