CC2640R2L SimpleLink™ Bluetooth® 5.1 Low Energy ワイヤレス・マイコン

1 特長

- マイコン
  - 高性能な Arm® Cortex®-M3
  - EEMBC CoreMark® スコア:142
  - クロック速度:最大 48MHz
  - 275KB 不揮発性メモリ (128KB のイン・システム・プログラマブル・フラッシュを含む)
  - 最大 28KB のシステム SRAM、そのうち 20KB は超低リークの SRAM
  - キャッシュまたはシステム RAM として使用可能な 8KB の SRAM
  - 2 ピン cJTAG および JTAG デバッグ
  - OTA (Over-The-Air) アップグレードに対応
- 高効率のコード・サイズ・アーキテクチャ:ドライバ、TI-RTOS、および Bluetooth® ソフトウェアを ROM に格納することで、アプリケーションで利用可能なフラッシュが増加
- RoHS 準拠のパッケージ
  - 5mm×5mm RHB VQFN32 (15GPIO)
  - 7mm × 7mm RGZ VQFN48 (31GPIO)
- ペリフェラル
  - すべてのデジタル・ペリフェラル・ピンを任意の GPIO に配線可能
  - 4 個の汎用タイマ・モジュール (8 個の 16 ビットまたは 4 個の 32 ビット・タイマ、それぞれ PWM)
  - 12 ビット ADC、200k サンプル/秒、8 チャネルのアナログ・マルチプレクサ
  - UART、I^2C、および I2S
  - SSI×2 (SPI、MICROWIRE、TI)
  - リアルタイム・クロック (RTC)
  - AES-128 セキュリティ・モジュール
  - TRNG (True Random Number Generator)
  - 温度センサ内蔵
- 外部システム
  - オンチップの内蔵 DC/DC コンバータ
  - CC2590 および CC2592 レンジ・エクステンダとのシームレスな統合
  - 必要な外部部品はごくわずか
  - 5mm × 5mm および 7mm × 7mm の VQFN パッケージで、SimpleLink™ CC2640, CC2640R2F および CC2650 デバイスとピン互換
  - 7mm x 7mm の VQFN パッケージで、SimpleLink™ CC2642R および CC2652R デバイスとピン互換
  - 5mm×5mm VQFN パッケージで、SimpleLink™ CC1350 デバイスとピン互換
- 低消費電力
  - 広い電源電圧範囲
    - 通常動作の場合:1.8～3.8V
    - 外部レギュレータ・モード:1.7～1.95V
  - アクティブ・モード RX:5.9mA
  - アクティブ・モード TX (0dBm):6.1mA
  - アクティブ・モード TX (+5dBm):9.1mA
  - アクティブ・モード MCU:61µA/MHz
  - アクティブ・モード MCU:48.5CoreMark/mA
  - スタンバイ:1.5µA (RTC 動作、RAM/CPU 保持)
  - シャットダウン:100nA (外部イベントによるウェークアップ)
- RF 部
  - Bluetooth Low Energy 5.1 およびそれ以前の LE 仕様と互換性のある 2.4GHz RF トランシーバ
  - 優れたレシーバ感度 (BLE で -97dBm)、選択性、ブロッキング性能
  - BLE のリンク・バジェットは 102dB
  - 最大 +5dBm のプログラム可能な出力電力
  - シングルエンドまたは差動 RF インターフェイス
  - 国際的な無線周波数規制への準拠を目標としたシステムに最適
    - ETSI EN 300 328 (ヨーロッパ)
    - EN 300 440 Class 2 (ヨーロッパ)
    - FCC CFR47 Part 15 (米国)
    - ARIB STD-T66 (日本)
- 開発ツールとソフトウェア
  - フル機能の開発キット
  - 複数のリファレンス・デザイン
  - SmartRF™ Studio
  - IAR Embedded Workbench®® for Arm®
  - Code Composer Studio™ 統合開発環境 (IDE)
  - Code Composer Studio™ Cloud IDE

2 アプリケーション

- ホーム / ビル・オートメーション
  - ネットワーク接続された家電製品
  - 照明器具
  - スマート・ロック
  - ゲートウェイ
  - セキュリティ・システム
- 産業用
  - ファクトリ・オートメーション
  - アセット・トラッキングおよび管理
  - HMI
  - アクセス制御
- 電子 POS (EPOS)
  - 電子棚札 (ESL)
- 健康と医療
  - 電子温度計
  - SpO2
  - 血糖値測定器と血圧測定器
  - 計量器
  - 補聴器
- スポーツとフィットネス
  - ウェアラブル・フィットネスおよびアクティビティ・モニタ
  - スマート追跡機能
  - 患者モニタ
  - フィットネス機器
- HID
  - ゲーム
  - ポインティング・デバイス (ワイヤレス・キーボードおよびマウス)

3 概要

この CC2640R2L デバイスは、Bluetooth® 5.1 Low Energy と独自の 2.4GHz アプリケーションをサポートする 2.4GHz ワイヤレス・マイクロコントローラ (MCU) です。このデバイスは、医療、アセット・トラッキング、パーソナル・エレクトロニクス、リテール・オートメーション、ビル・オートメーションの各市場、および産業用の性能が必要なアプリケーションで、低消費電力のワイヤレス通信と高度なセンシングに最適化されています。このデバイスの主な特長としては、以下に示すものがあります。

- 以下の Bluetooth® 5.1 機能に対応:LE Coded PHY (長距離)、LE 2Mbit PHY (高速)、アドバタイズ拡張機能、複数アドバタイズメント・セット、さらに、Bluetooth® 5.0 とそれ以前の Low Energy 仕様の主な機能の後方互換性およびサポート。
- 強力な Arm® Cortex®-M3 プロセッサ上でアプリケーションを開発するための SimpleLink™ CC2640R2 ソフトウェア開発キット (SDK) に含まれる、認定済みの Bluetooth® 5.1 ソフトウェア・プロトコル・スタック。
- 暗号化アクセラレータを搭載したフラッシュ・ベースのアーキテクチャであり、オンチップおよびオフチップの OAD をサポートしています。
- 柔軟性の高い低消費電力 RF トランシーバ機能を備えた専用のソフトウェア制御無線コントローラ (Arm® Cortex®-M0) により、複数の物理層および RF 規格をサポート
- Bluetooth® Low Energy (1Mbps の PHY で -97dBm) に対応する優れた無線感度および堅牢 (選択度、ブロッキング) 性能。

CC2640R2L デバイスは、SimpleLink™ マイコン (MCU) プラットフォームの一部です。本プラットフォームは、シングル・コア SDK (ソフトウェア開発キット) と豊富なツール・セットを備えた使いやすい共通の開発環境を共有する Wi-Fi®、Bluetooth Low Energy、Thread、ZigBee®、Sub-1GHz MCU、およびホスト MCU で構成されています。SimpleLink™ プラットフォームは一度で統合を実現でき、製品ラインアップのどのデバイスの組み合わせでも設計に追加できるので、設計要件変更の際もコードの 100% 再利用が可能です。詳細については、SimpleLink™ MCU プラットフォームを参照してください。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
CC2640R2LRGZ	VQFN (48)	7.00mm × 7.00mm
CC2640R2LRHB	VQFN (32)	5.00mm × 5.00mm

(1) 詳細については、セクション 12 を参照してください。

4 Functional Block Diagram

図 4-1 shows a block diagram for the CC2640R2L device.

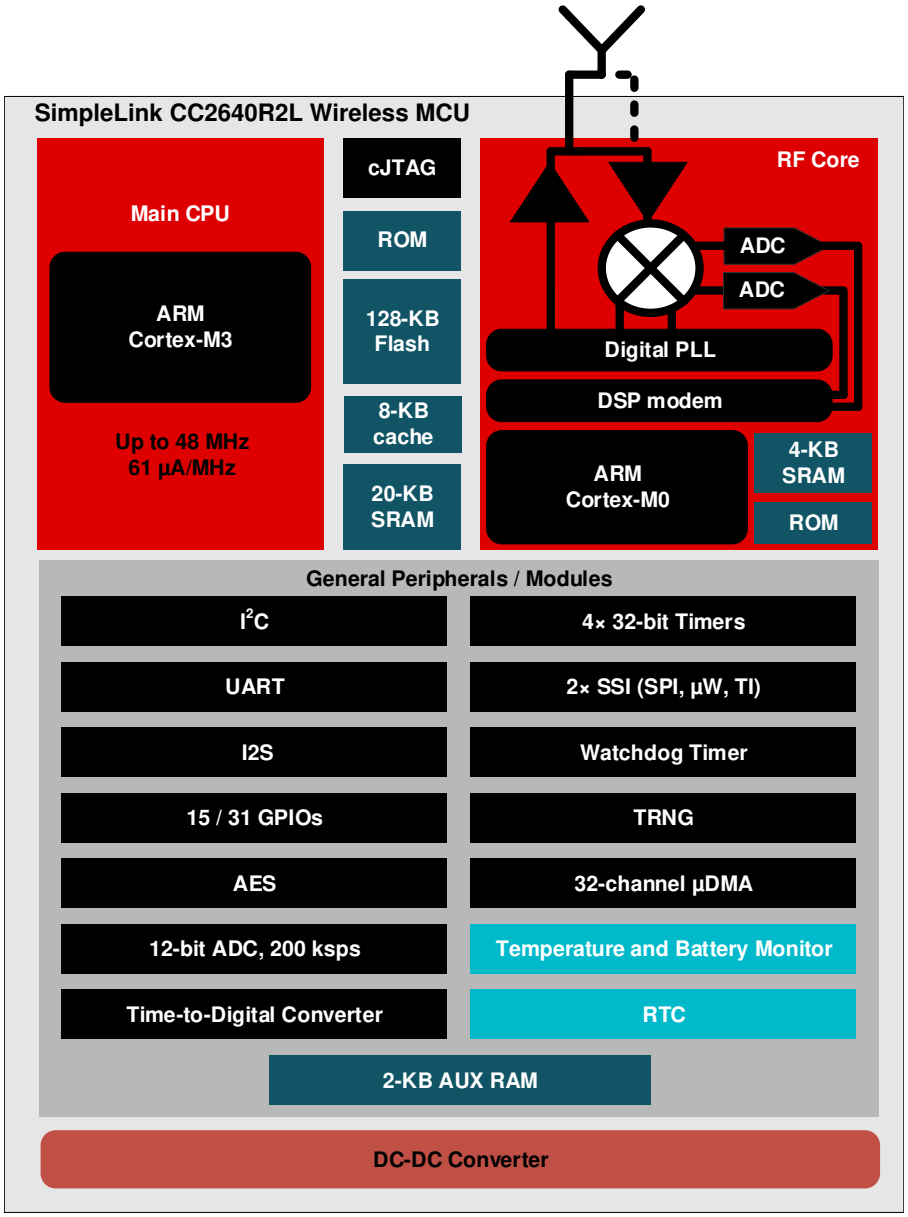

図 4-1. Block Diagram

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5 Revision History

Changes from May 22, 2020 to September 22, 2020 (from Revision * (June 2020) to Revision A (September 2020)) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 1
- セクション 3 を更新 2
- Changed 図 8-20 in セクション 8.26 25

6 Device Comparison

表 6-1. Device Family Overview

Device	PHY Support	Flash (KB)	RAM (KB)	GPIO	Package(1)
CC2640R2Lxxx(2)	Bluetooth low energy (Normal, High Speed, Long Range)	128	20	31, 15	RGZ, RHB
CC2640R2Fxxx(2)	Bluetooth low energy (Normal, High Speed, Long Range)	128	20	31, 15, 14, 10	RGZ, RHB, YFV, RSM
CC2640F128xxx	Bluetooth low energy (Normal)	128	20	31, 15, 10	RGZ, RHB, RSM
CC2650F128xxx	Multi-Protocol(3)	128	20	31, 15, 10	RGZ, RHB, RSM
CC2630F128xxx	IEEE 802.15.4 (ZigBee/6LoWPAN)	128	20	31, 15, 10	RGZ, RHB, RSM
CC2620F128xxx	IEEE 802.15.4 (RF4CE)	128	20	31, 10	RGZ, RSM

(1) The package designator replaces the xxx in device name to form a complete device name, RGZ is 7-mm × 7-mm VQFN48, RHB is 5-mm × 5-mm VQFN32, RSM is 4-mm × 4-mm VQFN32, and YFV is 2.7-mm × 2.7-mm DSBGA.
(2) CC2640R2L devices contain Bluetooth Low Energy Host and Controller libraries in ROM, leaving more of the 128KB Flash memory available for the customer application when used with supported BLE-Stack software protocol stack releases. Actual use of ROM and Flash memory by the protocol stack may vary depending on device software configuration. See www.ti.com for more details.
(3) The CC2650 device supports all PHYs and can be reflashed to run all the supported standards.

6.1 Related Products

TI's Wireless Connectivity	The wireless connectivity portfolio offers a wide selection of low-power RF solutions suitable for a broad range of applications. The offerings range from fully customized solutions to turn key offerings with pre-certified hardware and software (protocol).
TI's SimpleLink™ Sub-1 GHz Wireless MCUs	Long-range, low-power wireless connectivity solutions are offered in a wide range of Sub-1 GHz ISM bands.
Companion Products	Review products that are frequently purchased or used in conjunction with this product.
SimpleLink™ CC2640R2 Wireless MCU LaunchPad™ Development Kit	The CC2640R2 LaunchPad™ development kit brings easy Bluetooth® low energy (BLE) connection to the LaunchPad ecosystem with the SimpleLink ultra-low power CC26xx family of devices. Compared to the CC2650 LaunchPad, the CC2640R2 LaunchPad provides the following: • More free flash memory for the user application in the CC2640R2 wireless MCU • Out-of-the-box support for Bluetooth 4.2 specification • 4× faster Over-the-Air download speed compared to Bluetooth 4.1
SimpleLink™ Bluetooth low energy/Multi-standard SensorTag	The new SensorTag IoT kit invites you to realize your cloud-connected product idea. The new SensorTag now includes 10 low-power MEMS sensors in a tiny red package. And it is expandable with DevPacks to make it easy to add your own sensors or actuators.
Reference Designs	Find reference designs leveraging the best in TI technology to solve your system-level challenges

7 Terminal Configuration and Functions

7.1 Pin Diagram – RGZ Package

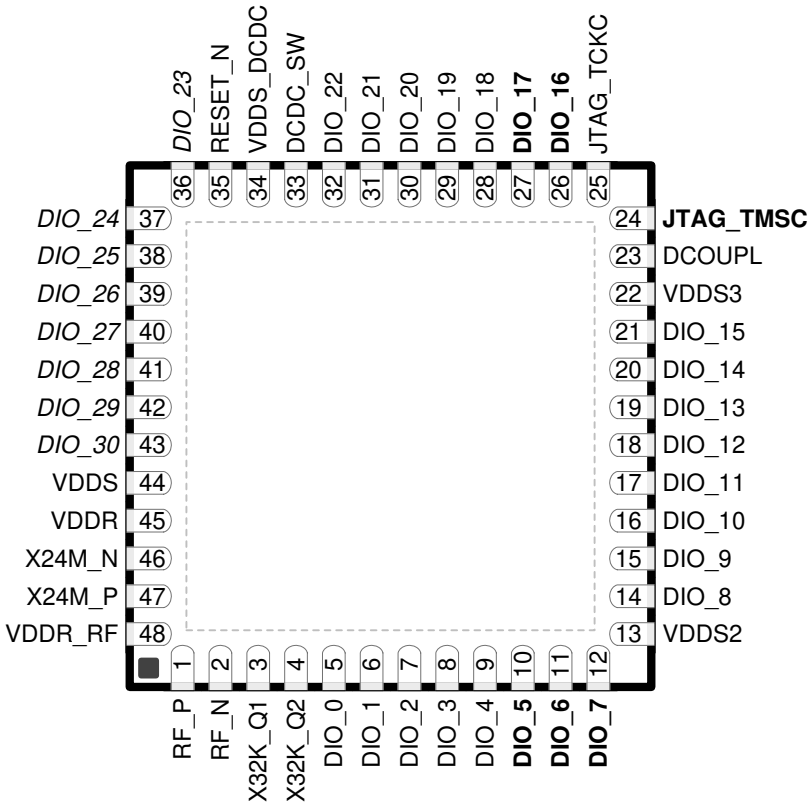


図 7-1. RGZ Package 48-Pin VQFN (7-mm × 7-mm) Pinout, 0.5-mm Pitch

I/O pins marked in 図 7-1 in **bold** have high-drive capabilities; they are the following:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

I/O pins marked in 図 7-1 in *italics* have analog capabilities; they are the following:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

7.2 Signal Descriptions – RGZ Package

表 7-1. Signal Descriptions – RGZ Package

NAME	NO.	TYPE	DESCRIPTION
DCDC_SW	33	Power	Output from internal DC/DC(1)
DCOUPL	23	Power	1.27-V regulated digital-supply decoupling capacitor(2)
DIO_0	5	Digital I/O	GPIO
DIO_1	6	Digital I/O	GPIO
DIO_2	7	Digital I/O	GPIO
DIO_3	8	Digital I/O	GPIO
DIO_4	9	Digital I/O	GPIO
DIO_5	10	Digital I/O	GPIO, high-drive capability
DIO_6	11	Digital I/O	GPIO, high-drive capability
DIO_7	12	Digital I/O	GPIO, high-drive capability
DIO_8	14	Digital I/O	GPIO
DIO_9	15	Digital I/O	GPIO
DIO_10	16	Digital I/O	GPIO
DIO_11	17	Digital I/O	GPIO
DIO_12	18	Digital I/O	GPIO
DIO_13	19	Digital I/O	GPIO
DIO_14	20	Digital I/O	GPIO
DIO_15	21	Digital I/O	GPIO
DIO_16	26	Digital I/O	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	Digital I/O	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	Digital I/O	GPIO
DIO_19	29	Digital I/O	GPIO
DIO_20	30	Digital I/O	GPIO
DIO_21	31	Digital I/O	GPIO
DIO_22	32	Digital I/O	GPIO
DIO_23	36	Digital/Analog I/O	GPIO, Analog
DIO_24	37	Digital/Analog I/O	GPIO, Analog
DIO_25	38	Digital/Analog I/O	GPIO, Analog
DIO_26	39	Digital/Analog I/O	GPIO, Analog
DIO_27	40	Digital/Analog I/O	GPIO, Analog
DIO_28	41	Digital/Analog I/O	GPIO, Analog
DIO_29	42	Digital/Analog I/O	GPIO, Analog
DIO_30	43	Digital/Analog I/O	GPIO, Analog
JTAG_TMSC	24	Digital I/O	JTAG TMSC, high-drive capability
JTAG_TCKC	25	Digital I/O	JTAG TCKC(3)
RESET_N	35	Digital input	Reset, active-low. No internal pullup.
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
VDDR	45	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC/DC(2) (4)
VDDR_RF	48	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC/DC(2) (5)

表 7-1. Signal Descriptions – RGZ Package (continued)

NAME	NO.	TYPE	DESCRIPTION
VDDS	44	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	13	Power	1.8-V to 3.8-V DIO supply(1)
VDDS3	22	Power	1.8-V to 3.8-V DIO supply(1)
VDDS_DCDC	34	Power	1.8-V to 3.8-V DC/DC supply
X32K_Q1	3	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	4	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	46	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	47	Analog I/O	24-MHz crystal oscillator pin 2
EGP		Power	Ground – Exposed Ground Pad

(1) For more details, see the technical reference manual (listed in セクション 11.3).
(2) Do not supply external circuitry from this pin.
(3) For design consideration regarding noise immunity for this pin, see the JTAG Interface chapter in the *CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual*
(4) If internal DC/DC is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

7.3 Pin Diagram – RHB Package

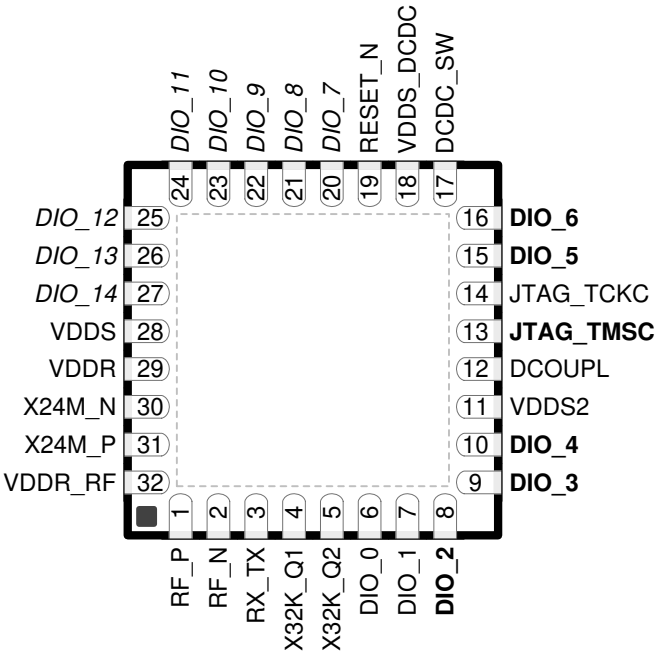


図 7-2. RHB Package 32-Pin VQFN (5-mm × 5-mm) Pinout, 0.5-mm Pitch

I/O pins marked in 図 7-2 in **bold** have high-drive capabilities; they are the following:

- Pin 8, DIO_2
- Pin 9, DIO_3
- Pin 10, DIO_4
- Pin 13, JTAG_TMSC
- Pin 15, DIO_5
- Pin 16, DIO_6

I/O pins marked in 図 7-2 in *italics* have analog capabilities; they are the following:

- Pin 20, DIO_7
- Pin 21, DIO_8
- Pin 22, DIO_9
- Pin 23, DIO_10
- Pin 24, DIO_11
- Pin 25, DIO_12
- Pin 26, DIO_13
- Pin 27, DIO_14

7.4 Signal Descriptions – RHB Package

表 7-2. Signal Descriptions – RHB Package

NAME	NO.	TYPE	DESCRIPTION
DCDC_SW	17	Power	Output from internal DC/DC(1)
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling(2)
DIO_0	6	Digital I/O	GPIO
DIO_1	7	Digital I/O	GPIO
DIO_2	8	Digital I/O	GPIO, high-drive capability
DIO_3	9	Digital I/O	GPIO, high-drive capability
DIO_4	10	Digital I/O	GPIO, high-drive capability
DIO_5	15	Digital I/O	GPIO, High drive capability, JTAG_TDO
DIO_6	16	Digital I/O	GPIO, High drive capability, JTAG_TDI
DIO_7	20	Digital/Analog I/O	GPIO, Analog
DIO_8	21	Digital/Analog I/O	GPIO, Analog
DIO_9	22	Digital/Analog I/O	GPIO, Analog
DIO_10	23	Digital/Analog I/O	GPIO, Analog
DIO_11	24	Digital/Analog I/O	GPIO, Analog
DIO_12	25	Digital/Analog I/O	GPIO, Analog
DIO_13	26	Digital/Analog I/O	GPIO, Analog
DIO_14	27	Digital/Analog I/O	GPIO, Analog
JTAG_TMSC	13	Digital I/O	JTAG TMSC, high-drive capability
JTAG_TCKC	14	Digital I/O	JTAG TCKC(3)
RESET_N	19	Digital input	Reset, active-low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX, Negative RF output signal to PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX, Positive RF output signal to PA during TX
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
VDDR	29	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC/DC(4) (2)
VDDR_RF	32	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC/DC(2) (5)
VDDS	28	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply(1)
VDDS_DCDC	18	Power	1.8-V to 3.8-V DC/DC supply
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2
EGP		Power	Ground – exposed ground pad

(1) See technical reference manual (listed in セクション 11.3) for more details.
(2) Do not supply external circuitry from this pin.
(3) For design consideration regarding noise immunity for this pin, see the JTAG Interface chapter in the *CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual*
(4) If internal DC/DC is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage (VDDS, VDDS2, and VDDS3)	VDDR supplied by internal DC/DC regulator or internal GLDO. VDDS_DCDC connected to VDDS on PCB	–0.3	4.1	V
Supply voltage (VDDS(3) and VDDR)	External regulator mode (VDDS and VDDR pins connected on PCB)	–0.3	2.25	V
Voltage on any digital pin(4) (5)		–0.3	VDDSx + 0.3, max 4.1	V
Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P		–0.3	VDDR + 0.3, max 2.25	V
Voltage on ADC input (V_{in})	Voltage scaling enabled	–0.3	VDDS	V
	Voltage scaling disabled, internal reference	–0.3	1.49	
	Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
Input RF level			5	dBm
T_{stg}	Storage temperature	–40	150	°C

(1) All voltage values are with respect to ground, unless otherwise noted.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) In external regulator mode, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog-capable DIO.
(5) Each pin is referenced to a specific VDDSx (VDDS, VDDS2 or VDDS3). For a pin-to-VDDS mapping table, see 表 9-2.

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge (RHB and RGZ packages)	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	All pins	±2500	V
		Charged device model (CDM), per JESD22-C101(2)	RF pins	±500	
			Non-RF pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Ambient temperature			–40	85	°C
Operating supply voltage (VDDS and VDDR), external regulator mode	For operation in 1.8-V systems (VDDS and VDDR pins connected on PCB, internal DC/DC cannot be used)		1.7	1.95	V
Operating supply voltage VDDS	For operation in battery-powered and 3.3-V systems (internal DC/DC can be used to minimize power consumption)		1.8	3.8	V
Operating supply voltages VDDS2 and VDDS3		VDDS < 2.7 V	1.8	3.8	V
Operating supply voltages VDDS2 and VDDS3		VDDS ≥ 2.7 V	1.9	3.8	V

8.4 Power Consumption Summary

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V with internal DC/DC converter, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	Reset. RESET_N pin asserted or VDDS below Power-on-Reset threshold		100		nA
		Shutdown. No clocks running, no retention		150		
		Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF		1.5		µA
		Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF		1.7		
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF		6		
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF		6.2		
		Idle. Supply Systems and RAM powered.		650		
		Active. Core running CoreMark		1.45 mA + 31 µA/MHz		
		Radio RX (1)		5.9		mA
		Radio RX(2)		6.1		
		Radio TX, 0-dBm output power(1)		6.1		
		Radio TX, 0-dBm output power(2)		7.0		
		Radio TX, 5-dBm output power(2)		9.1		
Peripheral Current Consumption (Adds to core current I_{core} for each peripheral unit activated) (3)						
I_{peri}	Peripheral power domain	Delta current with domain enabled		50		µA
	Serial power domain	Delta current with domain enabled		13		µA
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle		237		µA
	µDMA	Delta current with clock enabled, module idle		165		µA
	Timers	Delta current with clock enabled, module idle		113		µA
	I^2C	Delta current with clock enabled, module idle		12		µA
	I2S	Delta current with clock enabled, module idle		36		µA
	SSI	Delta current with clock enabled, module idle		93		µA
	UART	Delta current with clock enabled, module idle		164		µA

(1) Single-ended RF mode is optimized for size and power consumption. Measured on CC2650EM-4XS.
(2) Differential RF mode is optimized for RF performance. Measured on CC2650EM-5XD.
(3) I_{peri} is not supported in Standby or Shutdown.

8.5 General Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLASH MEMORY					
Supported flash erase cycles before failure(1)		100			k Cycles
Maximum number of write operations per row before erase(2)				83	write operations
Flash retention	105°C	11.4			Years at 105°C
Flash page/sector erase current	Average delta current		12.6		mA
Flash page/sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash page/sector erase time(3)			8		ms
Flash write time(3)	4 bytes at a time		8		µs

(1) Aborting flash during erase or program modes is not a safe operation.
(2) Each row is 2048 bits (or 256 Bytes) wide.
(3) This number is dependent on Flash aging and will increase over time and erase cycles.

8.6 125-kbps Coded (Bluetooth 5) – RX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		–103		dBm
Receiver saturation	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–260		310	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)	–260		260	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)	–140		140	ppm
Co-channel rejection (1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–3		dB
Selectivity, ±1 MHz (1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5(2)		dB
Selectivity, ±2 MHz (1)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = 10^{-3}		43 / 32(2)		dB
Selectivity, ±3 MHz (1)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		47 / 42(2)		dB
Selectivity, ±4 MHz (1)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		46 / 47(2)		dB
Selectivity, ±6 MHz (1)	Wanted signal at –79 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		49 / 46(2)		dB
Alternate channel rejection, ±7 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		50 / 47(2)		dB
Selectivity, image frequency(1)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		32		dB
Selectivity, image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 32(2)		dB

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Blocker rejection, ±8 MHz and above(1)	Wanted signal at –79 dBm, modulated interferer at ±8 MHz and above, BER = 10^{-3}		>46		dB
Out-of-band blocking (3)	30 MHz to 2000 MHz		–40		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–19		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–22		dBm
Intermodulation	Wanted signal at 2402 MHz, –76 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–42		dBm

(1) Numbers given as I/C dB.
(2) X / Y, where X is +N MHz and Y is –N MHz.
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification.

8.7 125-kbps Coded (Bluetooth 5) – TX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Differential mode, delivered to a single-ended 50-Ω load through a balun		5		dBm
Output power, highest setting	Measured on CC2650EM-4XS, delivered to a single-ended 50-Ω load		2		dBm
Output power, lowest setting	Delivered to a single-ended 50-Ω load through a balun		–21		dBm
Spurious emission conducted measurement(1)	f < 1 GHz, outside restricted bands		–43		dBm
	f < 1 GHz, restricted bands ETSI		–65		dBm
	f < 1 GHz, restricted bands FCC		–71		dBm
	f > 1 GHz, including harmonics		–46		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

8.8 500-kbps Coded (Bluetooth 5) – RX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		–101		dBm
Receiver saturation	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–240		240	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)	–500		500	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)	–310		330	ppm
Co-channel rejection (1)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}		–5		dB
Selectivity, ±1 MHz (1)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5(2)		dB
Selectivity, ±2 MHz (1)	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = 10^{-3}		41 / 31(2)		dB
Selectivity, ±3 MHz (1)	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		44 / 41(2)		dB

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±4 MHz (1)	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		44 / 44(2)		dB
Selectivity, ±6 MHz (1)	Wanted signal at –72 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		44 / 44(2)		dB
Alternate channel rejection, ±7 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		44 / 44(2)		dB
Selectivity, image frequency(1)	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB
Selectivity, image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 41(2)		dB
Blocker rejection, ±8 MHz and above(1)	Wanted signal at –72 dBm, modulated interferer at ±8 MHz and above, BER = 10^{-3}		44		dB
Out-of-band blocking (3)	30 MHz to 2000 MHz		–35		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–19		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–19		dBm
Intermodulation	Wanted signal at 2402 MHz, –69 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–37		dBm

(1) Numbers given as I/C dB.
(2) X / Y, where X is +N MHz and Y is –N MHz.
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification.

8.9 500-kbps Coded (Bluetooth 5) – TX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Differential mode, delivered to a single-ended 50-Ω load through a balun		5		dBm
Output power, highest setting	Measured on CC2650EM-4XS, delivered to a single-ended 50-Ω load		2		dBm
Output power, lowest setting	Delivered to a single-ended 50-Ω load through a balun		–21		dBm
Spurious emission conducted measurement(1)	f < 1 GHz, outside restricted bands		–43		dBm
	f < 1 GHz, restricted bands ETSI		–65		dBm
	f < 1 GHz, restricted bands FCC		–71		dBm
	f > 1 GHz, including harmonics		–46		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

8.10 1-Mbps GFSK (Bluetooth low energy) – RX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		–97		dBm
Receiver sensitivity	Single-ended mode. Measured on CC2650EM-4XS, at the SMA connector, BER = 10^{-3}		–96		dBm
Receiver saturation	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		4		dBm
Receiver saturation	Single-ended mode. Measured on CC2650EM-4XS, at the SMA connector, BER = 10^{-3}		0		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–350		350	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	–750		750	ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 3(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		34 / 25(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		38 / 26(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		42 / 29(2)		dB
Selectivity, ±5 MHz or more(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = 10^{-3}		32		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		25		dB
Selectivity, image frequency ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		3 / 26(2)		dB
Out-of-band blocking (3)	30 MHz to 2000 MHz		–20		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–5		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–8		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–10		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–34		dBm
Spurious emissions, 30 to 1000 MHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–71		dBm
Spurious emissions, 1 to 12.75 GHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–62		dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB

(1) Numbers given as I/C dB.
(2) X / Y, where X is +N MHz and Y is –N MHz.
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification.

8.11 1-Mbps GFSK (Bluetooth low energy) – TX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Differential mode, delivered to a single-ended 50-Ω load through a balun		5		dBm
Output power, highest setting	Measured on CC2650EM-4XS, delivered to a single-ended 50-Ω load		2		dBm
Output power, lowest setting	Delivered to a single-ended 50-Ω load through a balun		–21		dBm
Spurious emission conducted measurement(1)	f < 1 GHz, outside restricted bands		–43		dBm
	f < 1 GHz, restricted bands ETSI		–65		dBm
	f < 1 GHz, restricted bands FCC		–71		dBm
	f > 1 GHz, including harmonics		–46		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

8.12 2-Mbps GFSK (Bluetooth 5) – RX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		–90		dBm
Receiver saturation	Differential mode. Measured at the CC2650EM-5XD SMA connector, BER = 10^{-3}		3		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–300		500	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	–1000		1000	ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–7		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		31 / 26(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		37 / 38(2)		dB
Alternate channel rejection, ±7 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		37 / 36(2)		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		4		dB
Selectivity, image frequency ±2 MHz(1)	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–7 / 26(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–33		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–15		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–10		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level		–45		dBm

(1) Numbers given as I/C dB.
(2) X / Y, where X is +N MHz and Y is –N MHz.
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification.

8.13 2-Mbps GFSK (Bluetooth 5) – TX

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Differential mode, delivered to a single-ended 50-Ω load through a balun		5		dBm
Output power, highest setting	Measured on CC2650EM-4XS, delivered to a single-ended 50-Ω load		2		dBm
Output power, lowest setting	Delivered to a single-ended 50-Ω load through a balun		–21		dBm
Spurious emission conducted measurement(1)	f < 1 GHz, outside restricted bands		–43		dBm
	f < 1 GHz, restricted bands ETSI		–65		dBm
	f < 1 GHz, restricted bands FCC		–71		dBm
	f > 1 GHz, including harmonics		–46		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

8.14 24-MHz Crystal Oscillator (XOSC_HF)

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR, Equivalent series resistance(2)	6 pF < C_L ≤ 9 pF		20	60	Ω
ESR, Equivalent series resistance(2)	5 pF < C_L ≤ 6 pF			80	Ω
L_M, Motional inductance(2)	Relates to load capacitance (C_L in Farads)		< 1.6 × 10^{-24} / C_L ^{2}		H
C_L, Crystal load capacitance(2) (3)		5		9	pF
Crystal frequency(2) (4)			24		MHz
Crystal frequency tolerance(2) (5)		–40		40	ppm
Start-up time(4) (6)			150		µs

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) The crystal manufacturer's specification must satisfy this requirement
(3) Adjustable load capacitance is integrated into the device. External load capacitors are not required
(4) Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V
(5) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance. As per Bluetooth specification.
(6) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection.

8.15 32.768-kHz Crystal Oscillator (XOSC_LF)

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency(1)			32.768		kHz
Crystal frequency tolerance, Bluetooth low-energy applications(1) (2)		–500		500	ppm
ESR Equivalent series resistance(1)			30	100	kΩ
C_L Crystal load capacitance(1)		6		12	pF

(1) The crystal manufacturer's specification must satisfy this requirement
(2) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance. As per Bluetooth specification.

8.16 48-MHz RC Oscillator (RCOSC_HF)

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			48		MHz

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Uncalibrated frequency accuracy			±1%		
Calibrated frequency accuracy(1)			±0.25%		
Start-up time			5		µs

(1) Accuracy relative to the calibration source (XOSC_HF).

8.17 32-kHz RC Oscillator (RCOSC_LF)

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency(1)			32.8		kHz
Temperature coefficient			80		ppm/°C

(1) The frequency accuracy of the Real Time Clock (RTC) is not directly dependent on the frequency accuracy of the 32-kHz RC Oscillator. The RTC can be calibrated to an accuracy within ±500 ppm of 32.768 kHz by measuring the frequency error of RCOSC_LF relative to XOSC_HF and compensating the RTC tick speed. The procedure is explained in *Running Bluetooth® Low Energy on CC2640 Without 32 kHz Crystal*.

8.18 ADC Characteristics

T_c = 25°C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		VDDS	V
	Resolution			12		Bits
	Sample rate				200	ksps
	Offset	Internal 4.3-V equivalent reference(2)		2		LSB
	Gain error	Internal 4.3-V equivalent reference(2)		2.4		LSB
DNL(3)	Differential nonlinearity			>–1		LSB
INL(4)	Integral nonlinearity			±3		LSB
ENOB	Effective number of bits	Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone		9.8		Bits
		VDDS as reference, 200 ksps, 9.6-kHz input tone		10		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		11.1		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone		–65		dB
		VDDS as reference, 200 ksps, 9.6-kHz input tone		–69		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		–71		
SINAD, SNDR	Signal-to-noise and Distortion ratio	Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone		60		dB
		VDDS as reference, 200 ksps, 9.6-kHz input tone		63		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		69		
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone		67		dB
		VDDS as reference, 200 ksps, 9.6-kHz input tone		68		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		73		
	Conversion time	Serial conversion, time-to-output, 24-MHz clock		50		clock-cycles
	Current consumption	Internal 4.3-V equivalent reference(2)		0.66		mA
	Current consumption	VDDS as reference		0.75		mA

T_c = 25°C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TIRTOS API in order to include the gain/offset compensation factors stored in FCFG1.		4.3(2) (5)		V
Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TIRTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: Vref = 4.3 V × 1408 / 4095		1.48		V
Reference voltage	VDDS as reference (Also known as *RELATIVE*) (input voltage scaling enabled)		VDDS		V
Reference voltage	VDDS as reference (Also known as *RELATIVE*) (input voltage scaling disabled)		VDDS / 2.82(5)		V
Input impedance	200 ksps, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241™-2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.
(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on device (see 図 8-21).
(4) For a typical example, see 図 8-22.
(5) Applied voltage must be within absolute maximum ratings (セクション 8.1) at all times.

8.19 Temperature Sensor

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		°C
Range		–40		85	°C
Accuracy			±5		°C
Supply voltage coefficient(1)			3.2		°C/V

(1) Automatically compensated when using supplied driver libraries.

8.20 Battery Monitor

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV
Range		1.8		3.8	V
Accuracy			13		mV

8.21 Synchronous Serial Interface (SSI)

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
S1(1) t_{clk_per} (SSIClk period)	Device operating as slave	12		65024	system clocks
S2(1) t_{clk_high} (SSIClk high time)	Device operating as slave		0.5		t_{clk_per}
S3(1) t_{clk_low} (SSIClk low time)	Device operating as slave		0.5		t_{clk_per}
S1 (TX only)(1) t_{clk_per} (SSIClk period)	One-way communication to slave, device operating as master	4		65024	system clocks
S1 (TX and RX)(1) t_{clk_per} (SSIClk period)	Normal duplex operation, device operating as master	8		65024	system clocks
S2(1) t_{clk_high} (SSIClk high time)	Device operating as master		0.5		t_{clk_per}
S3(1) t_{clk_low} (SSIClk low time)	Device operating as master		0.5		t_{clk_per}

(1) Refer to SSI timing diagrams 図 8-1, 図 8-2, and 図 8-3.

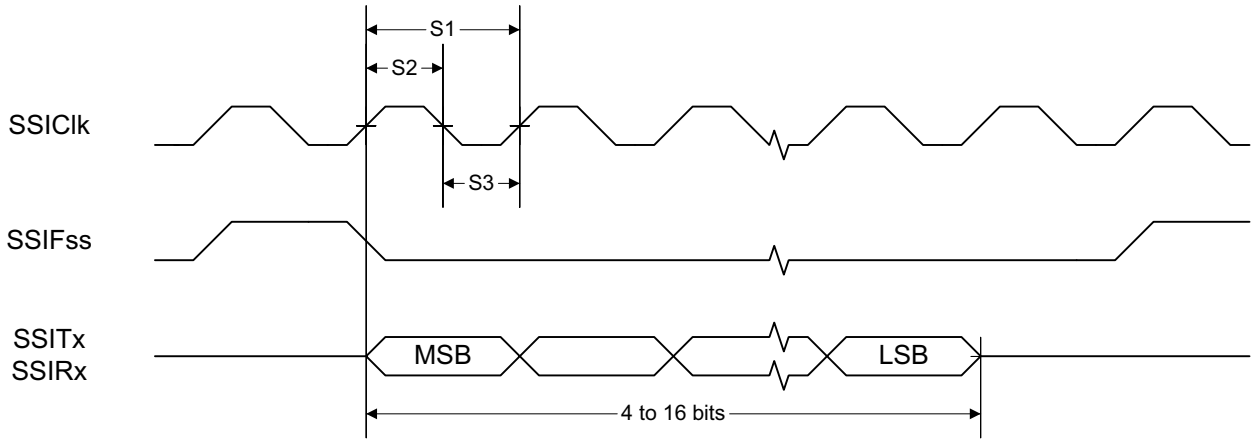


図 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

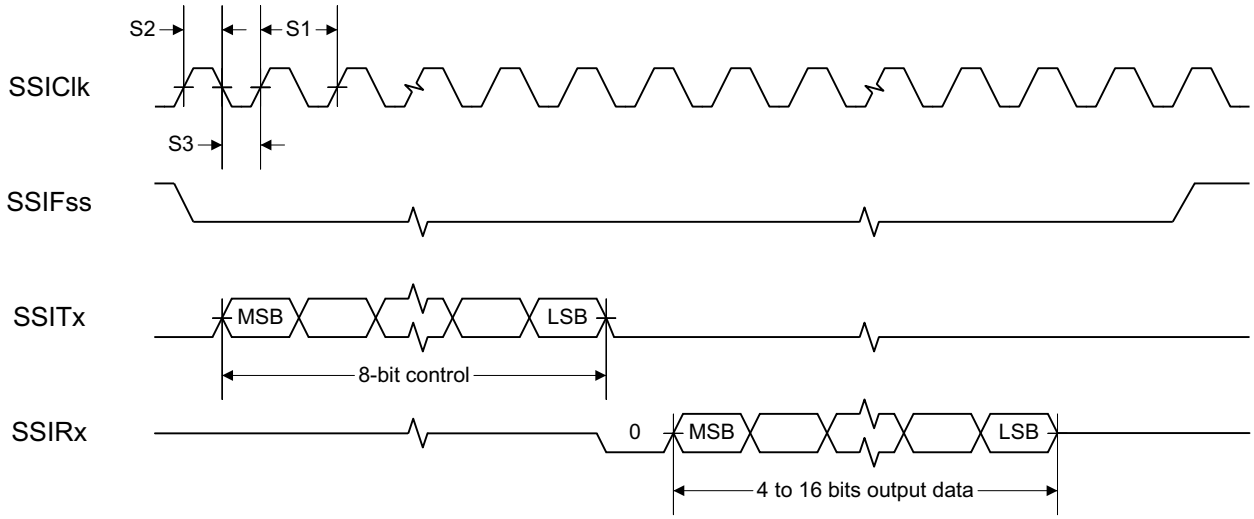


図 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

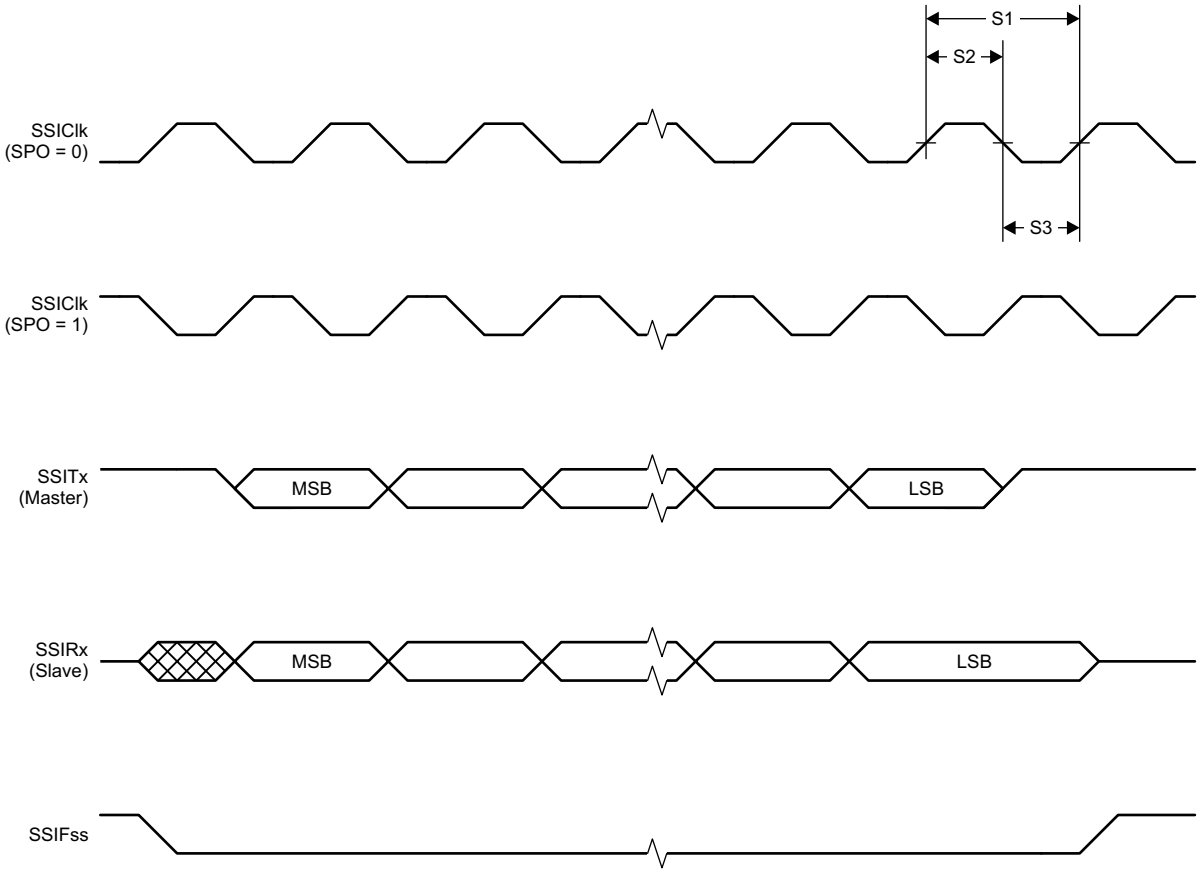


図 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

8.22 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 1.8 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only	1.32	1.54		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.26	0.32	V
GPIO VOH at 4-mA load	IOCURR = 1	1.32	1.58		V
GPIO VOL at 4-mA load	IOCURR = 1		0.21	0.32	V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		71.7		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		21.1		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.07		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.74		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.33		V
T_A = 25°C, V_{DDS} = 3.0 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.68		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.33		V
GPIO VOH at 4-mA load	IOCURR = 1		2.72		V
GPIO VOL at 4-mA load	IOCURR = 1		0.28		V
T_A = 25°C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		277		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		113		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.94		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.54		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.4		V
T_A = 25°C					
VIH	Lowest GPIO input voltage reliably interpreted as a «High»			0.8	VDDS(1)
VIL	Highest GPIO input voltage reliably interpreted as a «Low»	0.2			VDDS(1)

(1) Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in セクション 11.3 for more details.

8.23 Thermal Resistance Characteristics

NAME	DESCRIPTION	RHB (°C/W)(1) (2)	RGZ (°C/W)(1) (2)
$R\theta_{JA}$	Junction-to-ambient thermal resistance	32.8	29.6
$R\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	24.0	15.7
$R\theta_{JB}$	Junction-to-board thermal resistance	6.8	6.2
Psi_{JT}	Junction-to-top characterization parameter	0.3	0.3
Psi_{JB}	Junction-to-board characterization parameter	6.8	6.2
$R\theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	1.9

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*.
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*.

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

8.24 Timing Requirements

		MIN	NOM	MAX	UNIT
Rising supply-voltage slew rate		0		100	mV/µs
Falling supply-voltage slew rate		0		20	mV/µs
Falling supply-voltage slew rate, with low-power flash settings(1)				3	mV/µs
Positive temperature gradient in standby(2)	No limitation for negative temperature gradient, or outside standby mode			5	°C/s
CONTROL INPUT AC CHARACTERISTICS(3)					
RESET_N low duration		1			µs

(1) For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor (see 図 10-1) must be used to ensure compliance with this slew rate.
(2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see セクション 8.17).
(3) T_A = –40°C to +85°C, V_{DDS} = 1.7 V to 3.8 V, unless otherwise noted.

8.25 Switching Characteristics

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKEUP AND TIMING					
Idle → Active			14		µs
Standby → Active			151		µs
Shutdown → Active			1015		µs

8.26 Typical Characteristics

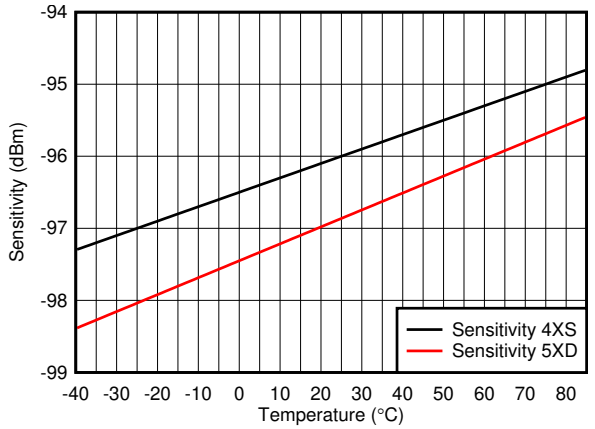


図 8-4. BLE Sensitivity vs Temperature

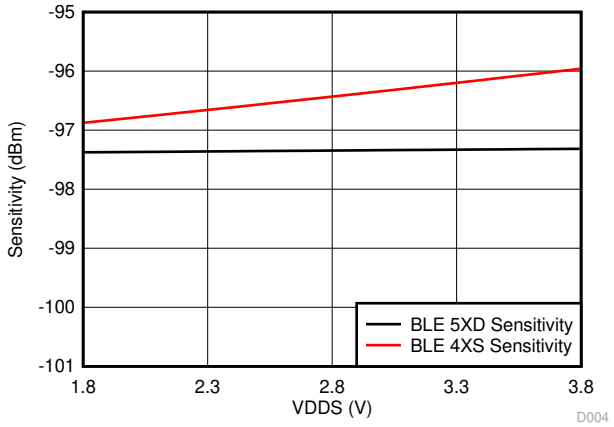


図 8-5. BLE Sensitivity vs Supply Voltage (VDDS)

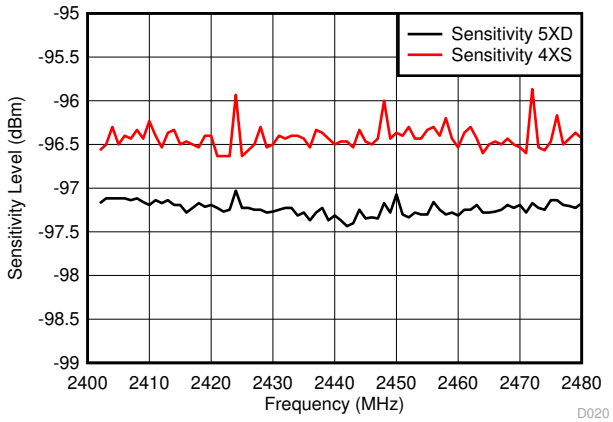


図 8-6. BLE Sensitivity vs Channel Frequency

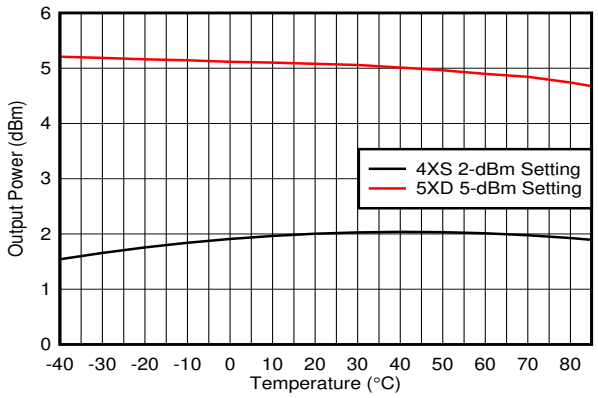


図 8-7. TX Output Power vs Temperature

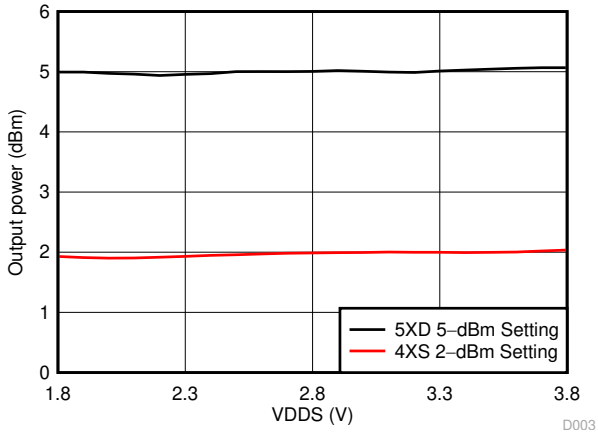


図 8-8. TX Output Power vs Supply Voltage (VDDS)

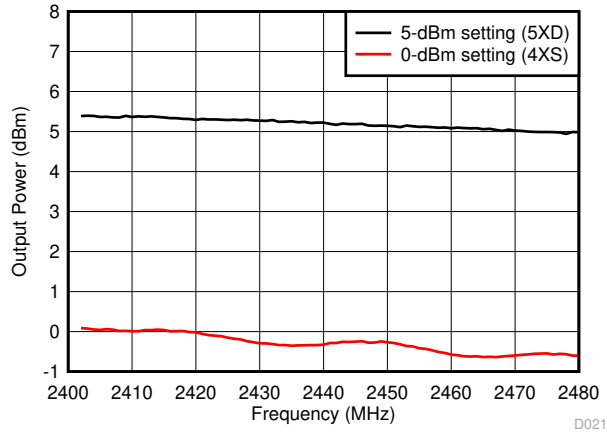


図 8-9. TX Output Power vs Channel Frequency

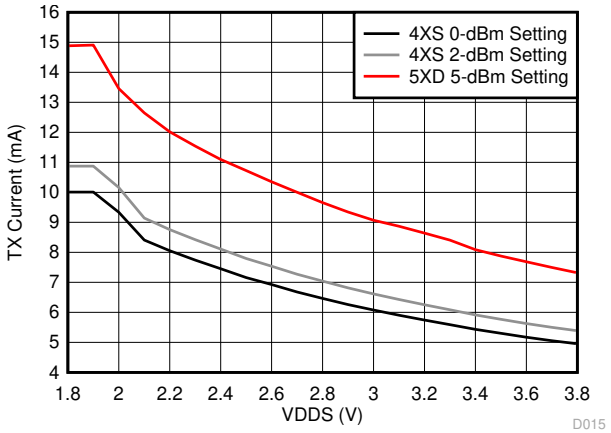


図 8-10. TX Current Consumption vs Supply Voltage (VDDS)

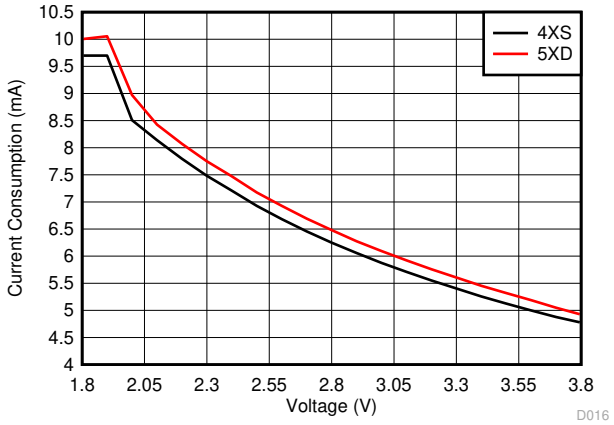


図 8-11. RX Mode Current vs Supply Voltage (VDDS)

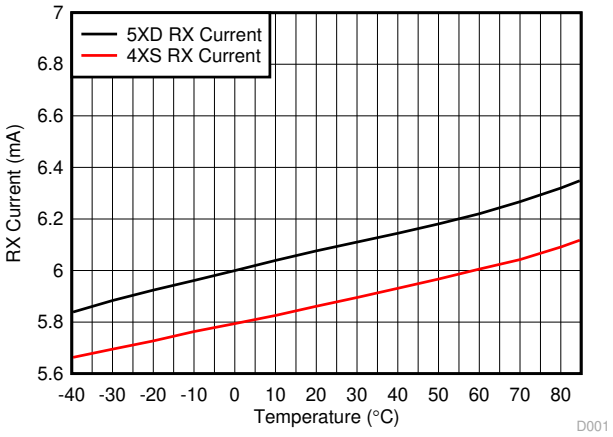


図 8-12. RX Mode Current Consumption vs Temperature

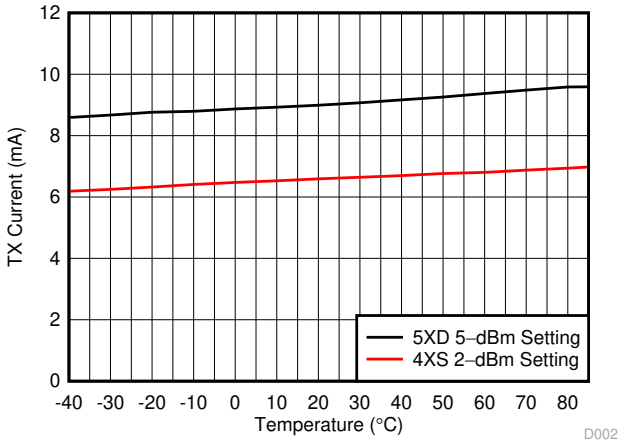


図 8-13. TX Mode Current Consumption vs Temperature

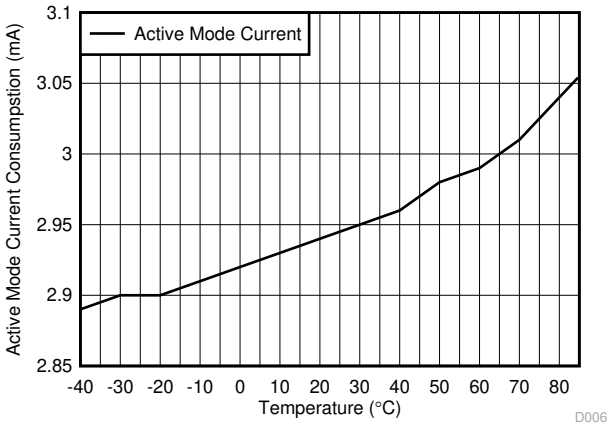


図 8-14. Active Mode (MCU Running, No Peripherals) Current Consumption vs Temperature

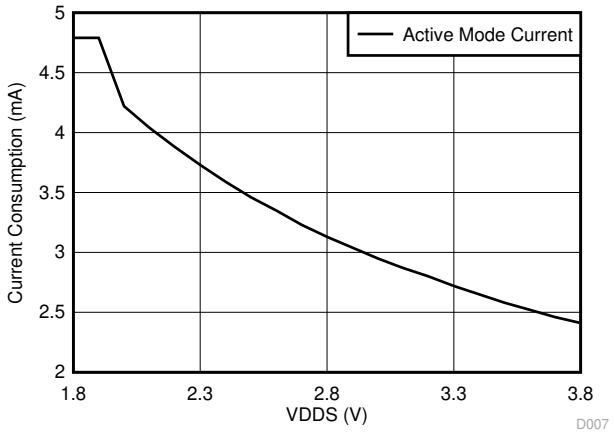


図 8-15. Active Mode (MCU Running, No Peripherals) Current Consumption vs Supply Voltage (VDDS)

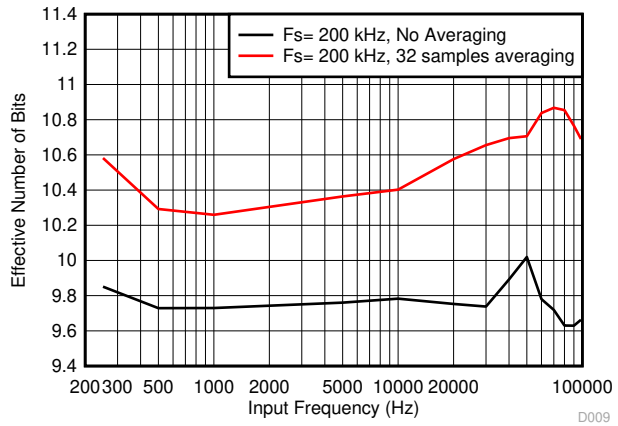


図 8-16. SoC ADC Effective Number of Bits vs Input Frequency (Internal Reference, Scaling Enabled)

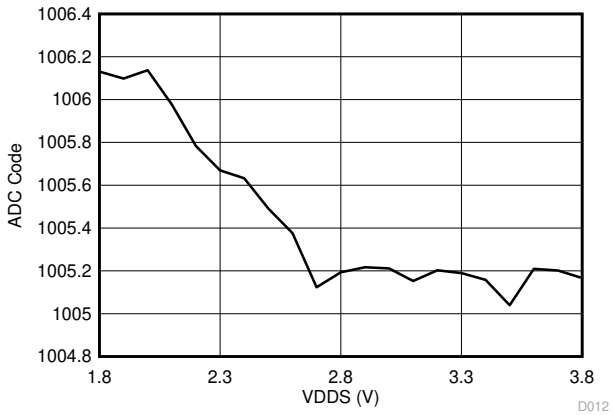


図 8-17. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference)

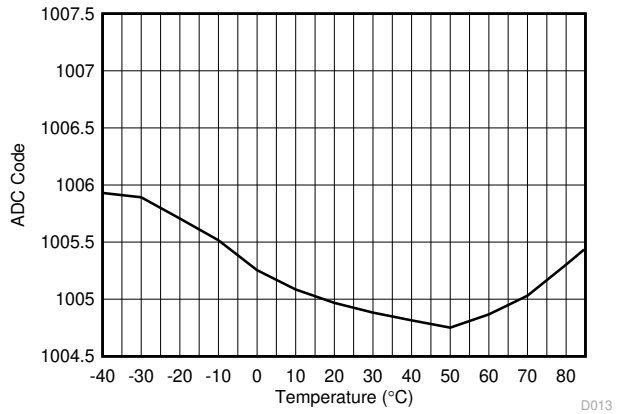


図 8-18. SoC ADC Output vs Temperature (Fixed Input, Internal Reference)

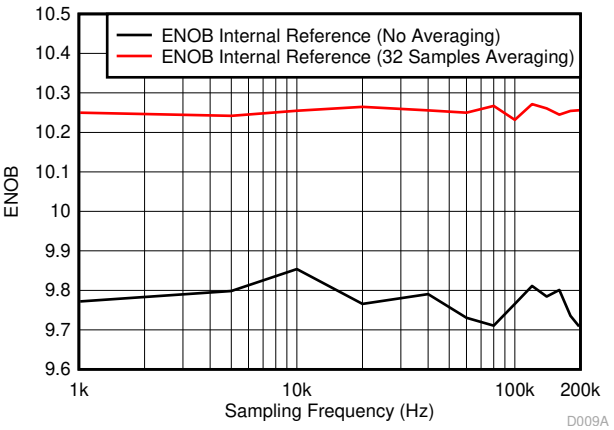


図 8-19. SoC ADC ENOB vs Sampling Frequency (Scaling Enabled, Input Frequency = FS / 10)

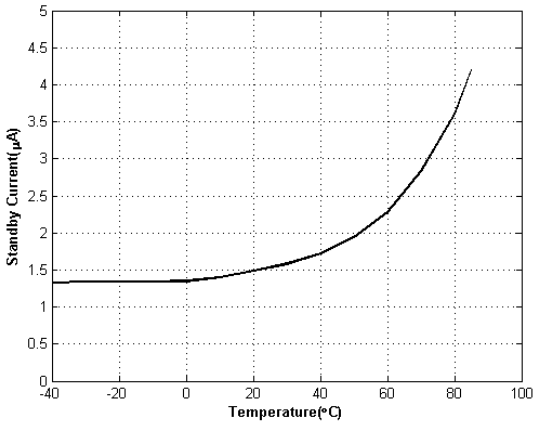


図 8-20. Standby Mode Supply Current vs Temperature

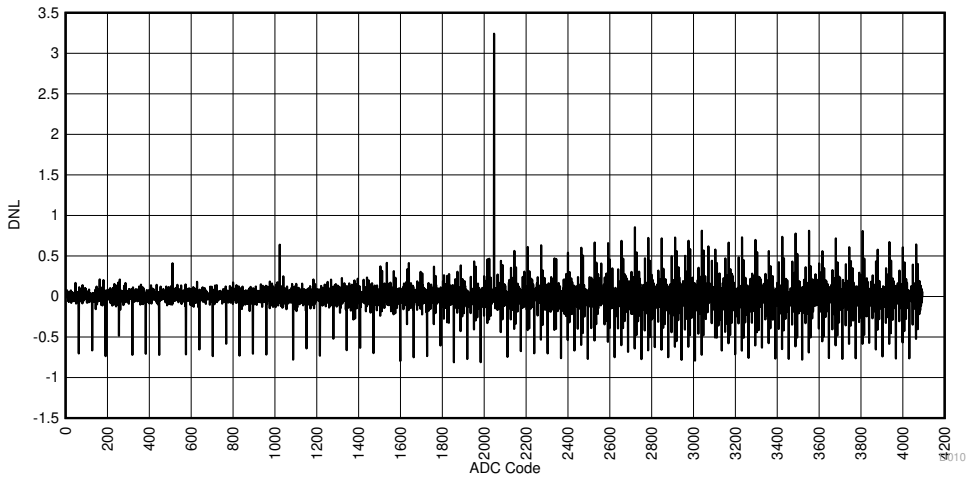


図 8-21. SoC ADC DNL vs ADC Code (Internal Reference)

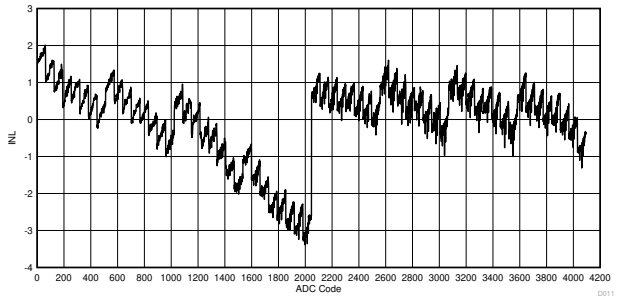


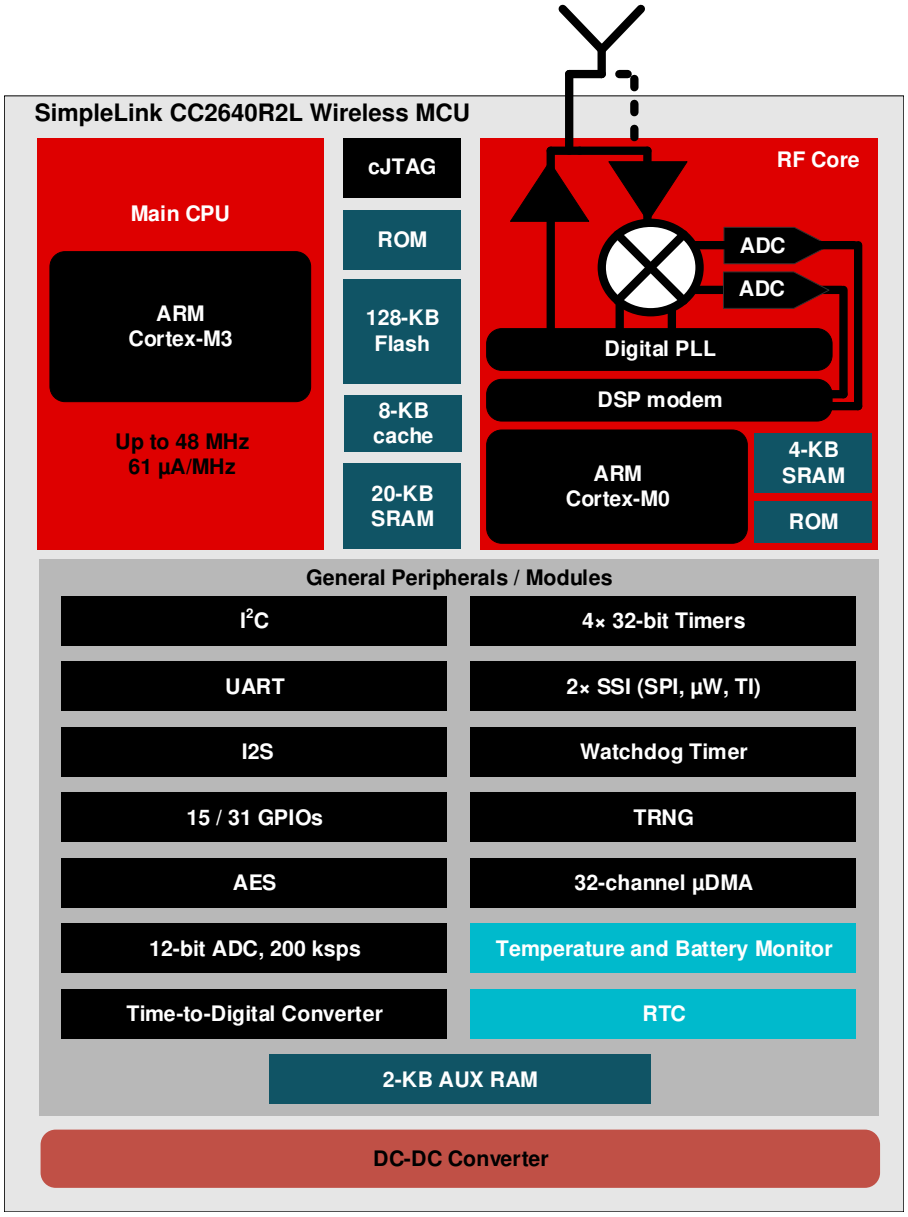
図 8-22. SoC ADC INL vs ADC Code (Internal Reference)

9 Detailed Description

9.1 Overview

The core modules of the CC2640R2L MCU are shown in セクション 9.2.

9.2 Functional Block Diagram



9.3 Main CPU

The SimpleLink™ CC2640R2L Wireless MCU contains an Arm Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The CM3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Arm Cortex-M3 features include:

- 32-bit Arm Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultra-low-power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

9.4 RF Core

The RF Core contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuits, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU.

The RF core is capable of autonomously handling the time-critical aspects of the radio protocols (Bluetooth low energy) thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4-KB SRAM block and runs initially from separate ROM memory. The Arm Cortex-M0 processor is not programmable by customers.

9.5 Memory

The Flash memory provides nonvolatile storage for code and data. The Flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI-RTOS kernel, Driverlib, and lower layer protocol stack software (Bluetooth low energy controller). It also contains a bootloader that can be used to reprogram the device using SPI or UART. For CC2640R2Lxxx devices, the ROM contains Bluetooth 4.2 low energy host- and controller software libraries, leaving more of the flash memory available for the customer application.

9.6 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

9.7 Power Management

To minimize power consumption, the CC2640R2L MCU supports a number of power modes and power management features (see 表 9-1).

表 9-1. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.45 mA + 31 µA/MHz	650 µA	1.5 µA	0.15 µA	0.1 µA
Wake-up Time to CPU Active(1)	–	14 µs	151 µs	1015 µs	1015 µs
Register Retention	Full	Full	Partial	No	No
SRAM Retention	Full	Full	Full	No	No
High-Speed Clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-Speed Clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Wake up on RTC	Available	Available	Available	Off	Off
Wake up on Pin Edge	Available	Available	Available	Available	Off
Wake up on Reset Pin	Available	Available	Available	Available	Available
Brown Out Detector (BOD)	Active	Active	Duty Cycled	Off	N/A
Power On Reset (POR)	Active	Active	Active	Active	N/A

(1) Not including RTOS overhead

In active mode, the application CM3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see 表 9-1).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into active mode.

In standby mode, only the always-on domain (AON) is active. An external wake-up event or RTC event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is turned off entirely, including the AON domain. The I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake-up from Shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way, a reset-by-reset pin, or a power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the Flash memory contents.

9.8 Clock Systems

The CC2640R2L supports two external and two internal clock sources.

A 24-MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32-kHz crystal is optional. *Bluetooth* low energy requires a slow-speed clock with better than ±500 ppm accuracy if the device is to enter any sleep mode while maintaining a connection. The internal 32-kHz RC oscillator can in some use cases be compensated to meet the requirements. The low-speed crystal oscillator is designed for use with a 32-kHz watch-type crystal.

The internal high-speed oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

9.9 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high drive capabilities (marked in **bold** in セクション 7).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps .

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The I^2C interface is used to communicate with devices compatible with the I^2C standard. The I^2C interface supports 100-kHz and 400-kHz operation, and can serve as both I^2C master and I^2C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data transfer tasks from the CM3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except for in Shutdown (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

The ADC is a 12-bit, 200 ksamples per second (ksps) ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, and the RTC.

9.10 Voltage Supply Domains

The CC2640R2L device can interface to two or three different voltage domains depending on the package type. On-chip level converters ensure correct operation as long as the signal voltage on each input/output pin is set with respect to the corresponding supply pin (VDDS, VDDS2 or VDDS3). 表 9-2 lists the pin-to-VDDS mapping.

表 9-2. Pin Function to VDDS Mapping Table

	Package	
	VQFN 7 × 7 (RGZ)	**VQFN 5 × 5 (RHB)**
VDDS(1)	DIO 23–30 Reset_N	DIO 7–14 Reset_N
VDDS2	DIO 0–11	DIO 0–6 JTAG
VDDS3	DIO 12–22 JTAG	N/A

(1) VDDS_DCDC must be connected to VDDS on the PCB.

9.11 System Architecture

Depending on the product configuration, CC26xx can function either as a Wireless Network Processor (WNP—an IC running the wireless protocol stack, with the application running on a separate MCU), or as a System-on-Chip (SoC), with the application and protocol stack running on the Arm Cortex-M3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

10 Application, Implementation, and Layout

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Very few external components are required for the operation of the CC2640R2L device. This section provides some general information about the various configuration options when using the CC2640R2L in an application, and then shows two examples of application circuits with schematics and layout. This is only a small selection of the many application circuit examples available as complete reference designs from the product folder on www.ti.com.

図 10-1 shows the various RF front-end configuration options. The RF front end can be used in differential- or single-ended configurations with the options of having internal or external biasing. These options allow for various trade-offs between cost, board space, and RF performance. Differential operation with external bias gives the best performance while single-ended operation with internal bias gives the least amount of external components and the lowest power consumption. Reference designs exist for each of these options.

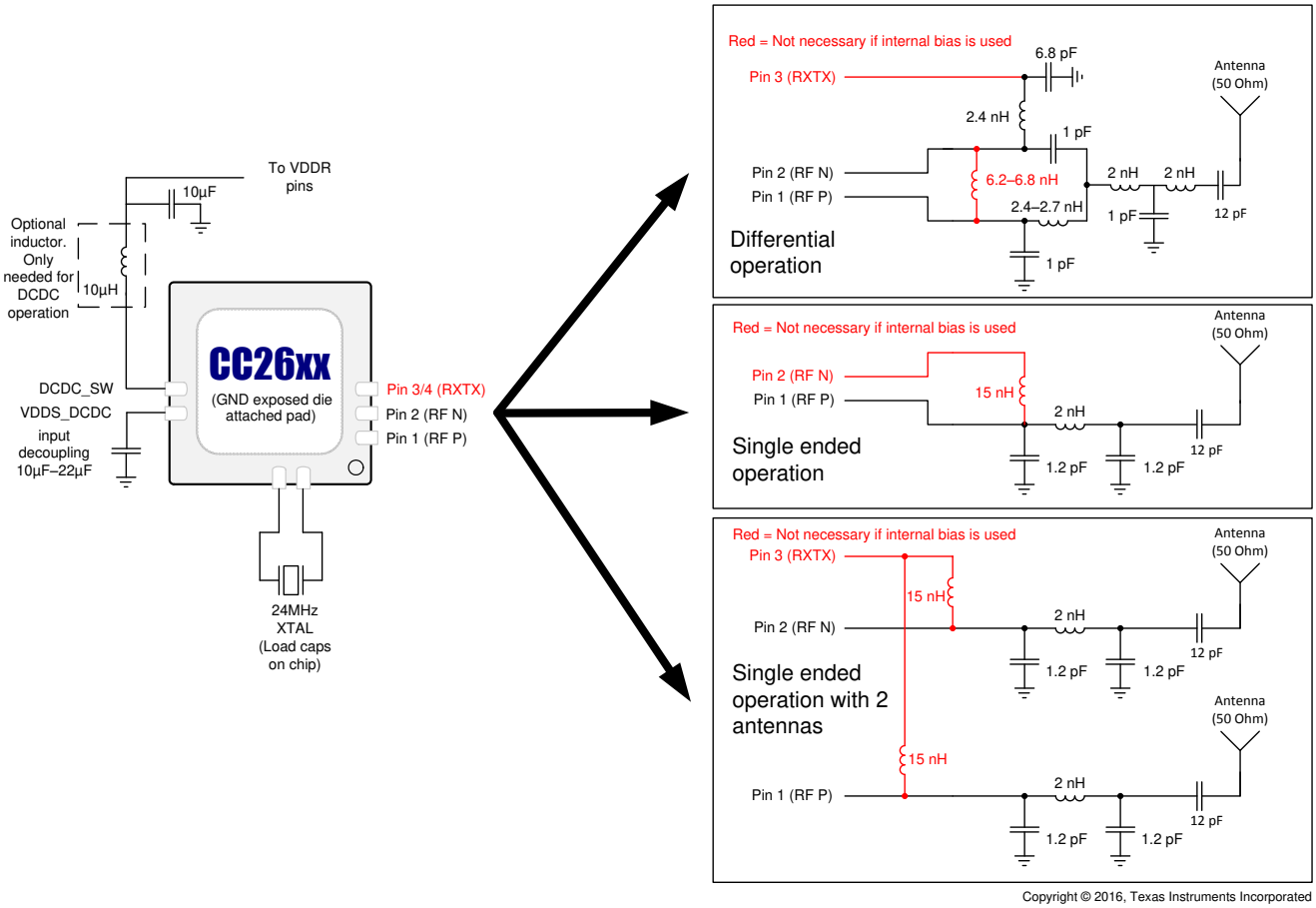


図 10-1. CC2640R2L Application Circuit

図 10-2 shows the various supply voltage configuration options. Not all power supply decoupling capacitors or digital I/Os are shown. Exact pin positions will vary between the different package options. For a detailed overview of power supply decoupling and wiring, see the TI reference designs and the CC26xx technical reference manual ().

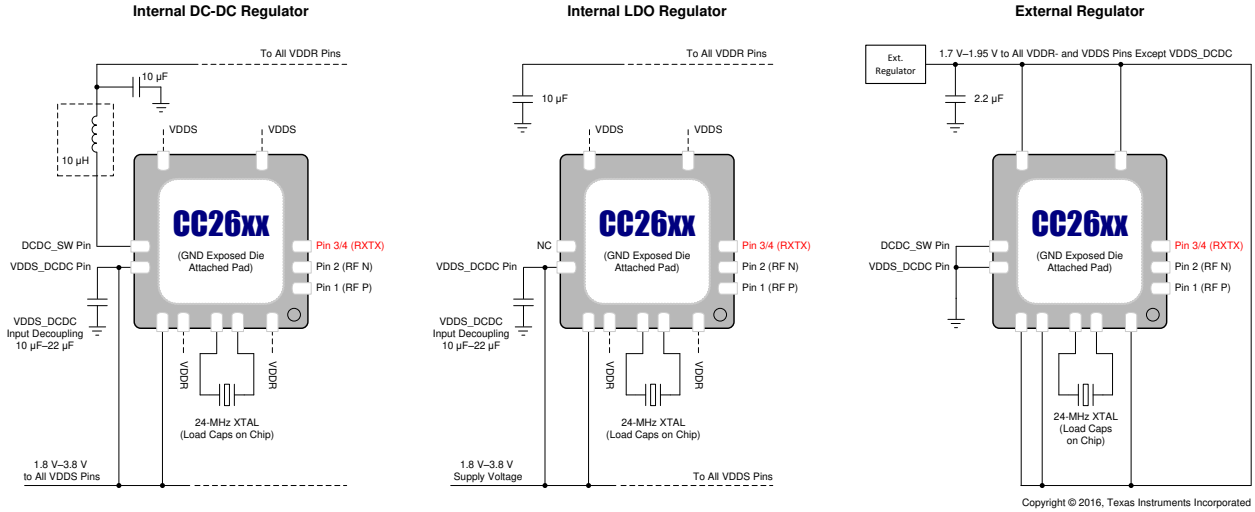


図 10-2. Supply Voltage Configurations

10.2 5 × 5 External Differential (5XD) Application Circuit

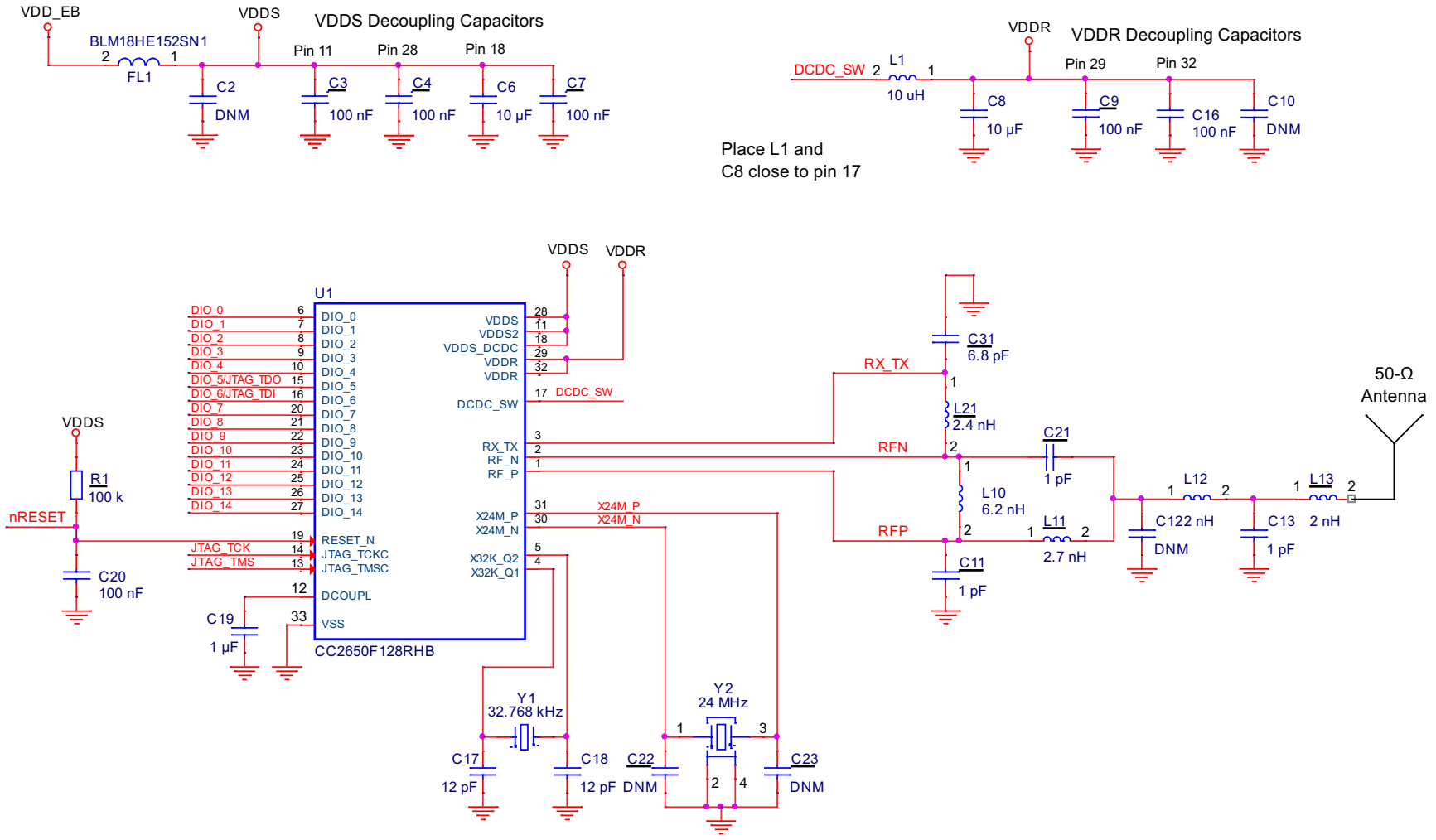


図 10-3. 5 × 5 External Differential (5XD) Application Circuit

10.2.1 Layout

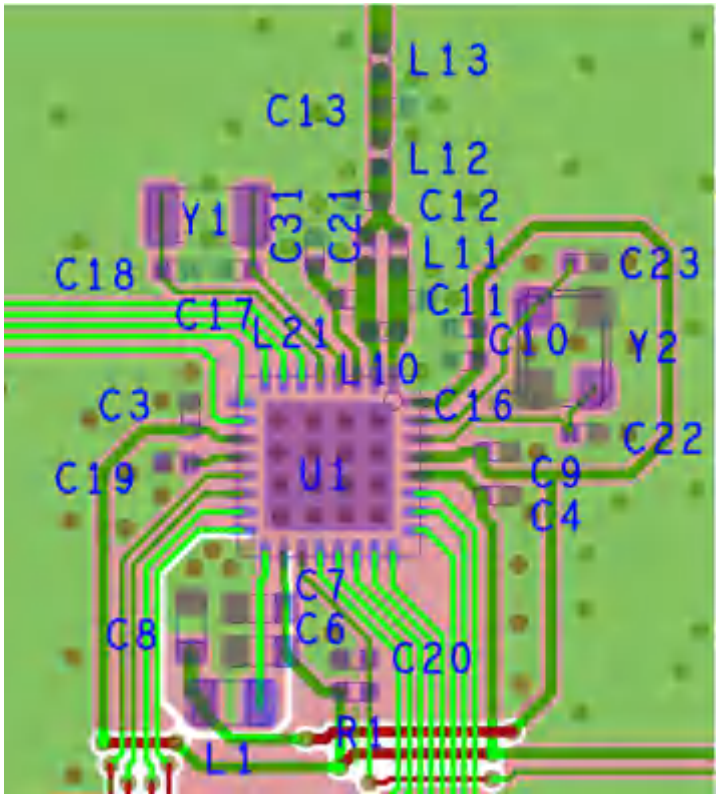


図 10-4. 5 × 5 External Differential (5XD) Layout

11 Device and Documentation Support

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all pre-production part numbers or date-code markings. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, CC2640R2L is in production; therefore, no prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGZ).

For orderable part numbers of the CC2640R2L device in the RHB and RGZ package types, see the *Package Option Addendum* of this document, the TI website (www.ti.com), or contact your TI sales representative.

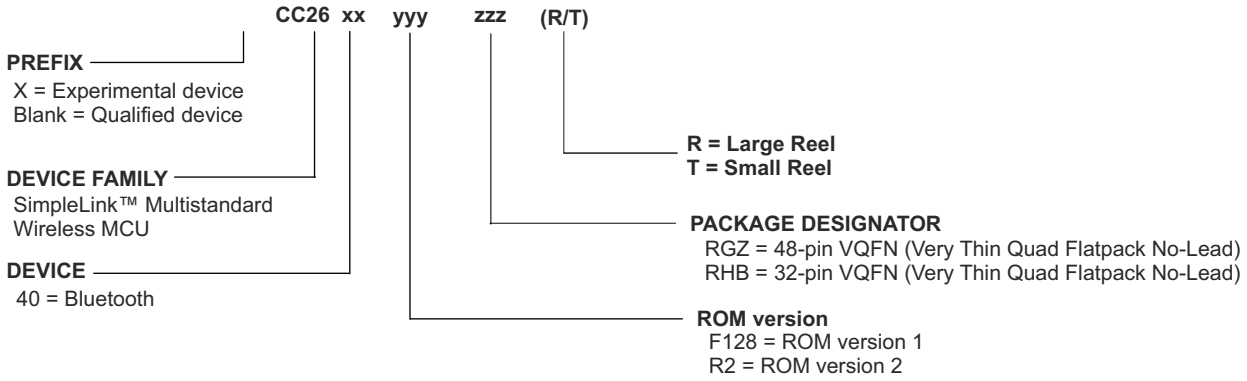


図 11-1. Device Nomenclature

11.2 Tools and Software

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of the CC2640R2L device applications:

Software Tools:

SmartRF Studio 7 is a PC application that helps designers of radio systems to easily evaluate the RF-IC at an early stage in the design process.

- Test functions for sending and receiving radio packets, continuous wave transmit and receive
- Evaluate RF performance on custom boards by wiring it to a supported evaluation board or debugger
- Can also be used without any hardware, but then only to generate, edit and export radio configuration settings
- Can be used in combination with several development kits for Texas Instruments' CCxxxx RF-ICs

IDEs and Compilers:

Code Composer Studio™ Integrated Development Environment (IDE):

- Integrated development environment with project management tools and editor
- Code Composer Studio (CCS) 7.0 and later has built-in support for the CC26xx device family
- Best support for XDS debuggers; XDS100v3, XDS110 and XDS200
- High integration with TI-RTOS with support for TI-RTOS Object View

IAR Embedded Workbench® for Arm®:

- Integrated development environment with project management tools and editor
- IAR EWARM 7.80.1 and later has built-in support for the CC26xx device family
- Broad debugger support, supporting XDS100v3, XDS200, IAR I-Jet and Segger J-Link
- Integrated development environment with project management tools and editor
- RTOS plugin available for TI-RTOS

For a complete listing of development-support tools for the CC2640R2L platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

11.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com (CC2640R2L). In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the CC2640R2L devices, related peripherals, and other technical collateral is listed in the following.

Technical Reference Manual

CC13xx, CC26xx SimpleLink™ Wireless MCU Technical Reference Manual

Errata

CC2640R2L SimpleLink™ Wireless MCU Errata

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.5 Texas Instruments Low-Power RF Website

Texas Instruments' Low-Power RF website has all the latest products, application and design notes, FAQ section, news and events updates. Go to www.ti.com/lprf.

11.6 Low-Power RF eNewsletter

The Low-Power RF eNewsletter is up-to-date on new products, news releases, developers' news, and other news and events associated with low-power RF products from TI. The Low-Power RF eNewsletter articles include links to get more online information.

Sign up at: www.ti.com/lprfnewsletter

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11.8 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.9 Export Control Notice

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11.10 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC2640R2LRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2640 R2L
CC2640R2LRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2640 R2L
CC2640R2LRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2640 R2L
CC2640R2LRHBR	Active	Production	VQFN (RHB) | 32	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2640 R2L
CC2640R2LRHBR.A	Active	Production	VQFN (RHB) | 32	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2640 R2L
CC2640R2LRHBR.B	Active	Production	VQFN (RHB) | 32	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2640 R2L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

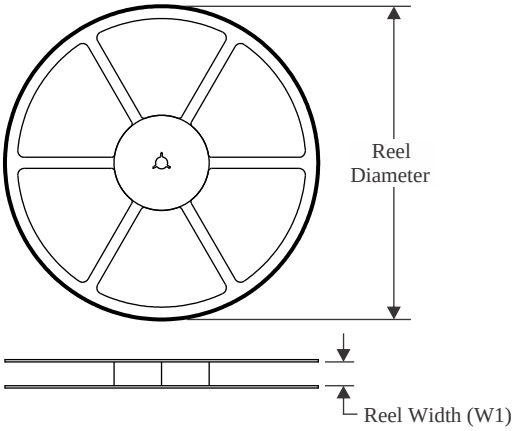
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

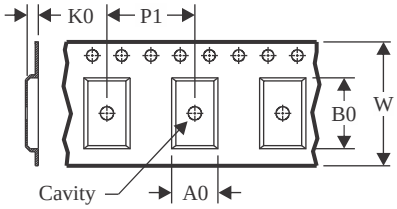
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

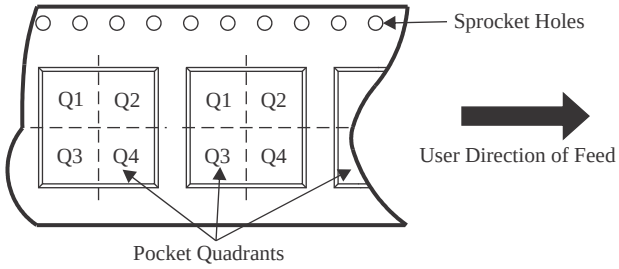


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

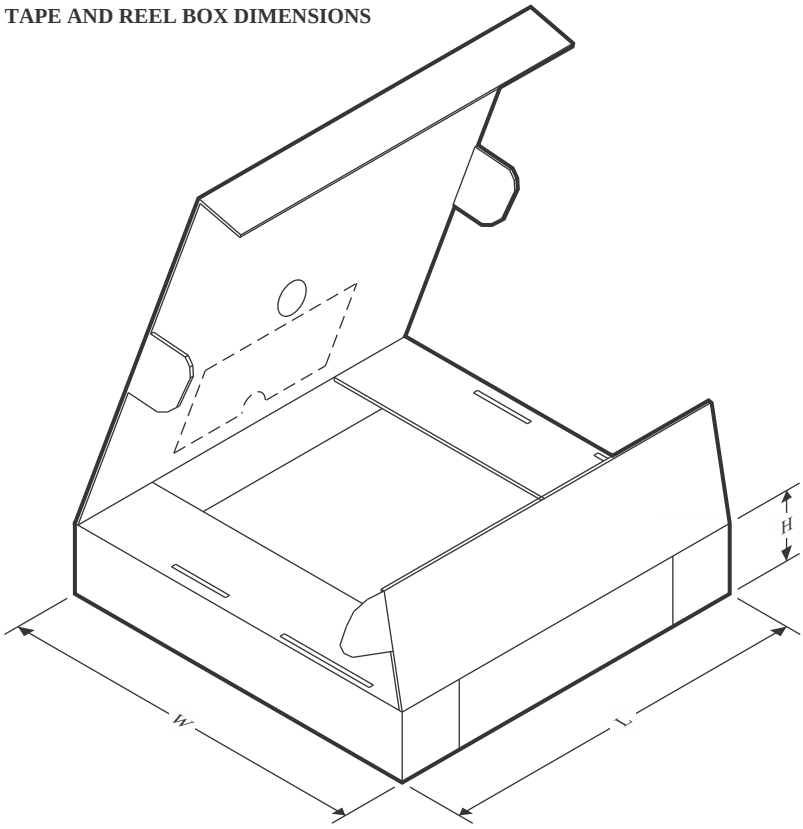
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2640R2LRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC2640R2LRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC2640R2LRHBR	VQFN	RHB	32	2500	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC2640R2LRHBR	VQFN	RHB	32	2500	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2640R2LRGZR	VQFN	RGZ	48	2500	336.6	336.6	31.8
CC2640R2LRGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
CC2640R2LRHBR	VQFN	RHB	32	2500	367.0	367.0	35.0
CC2640R2LRHBR	VQFN	RHB	32	2500	336.6	336.6	31.8

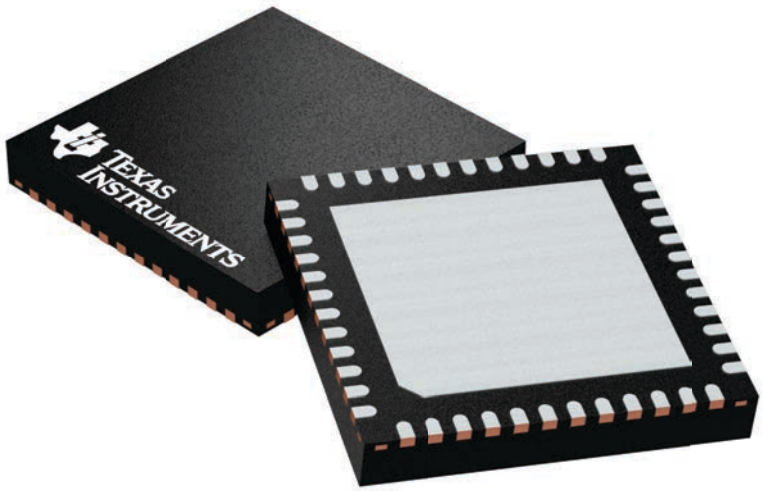
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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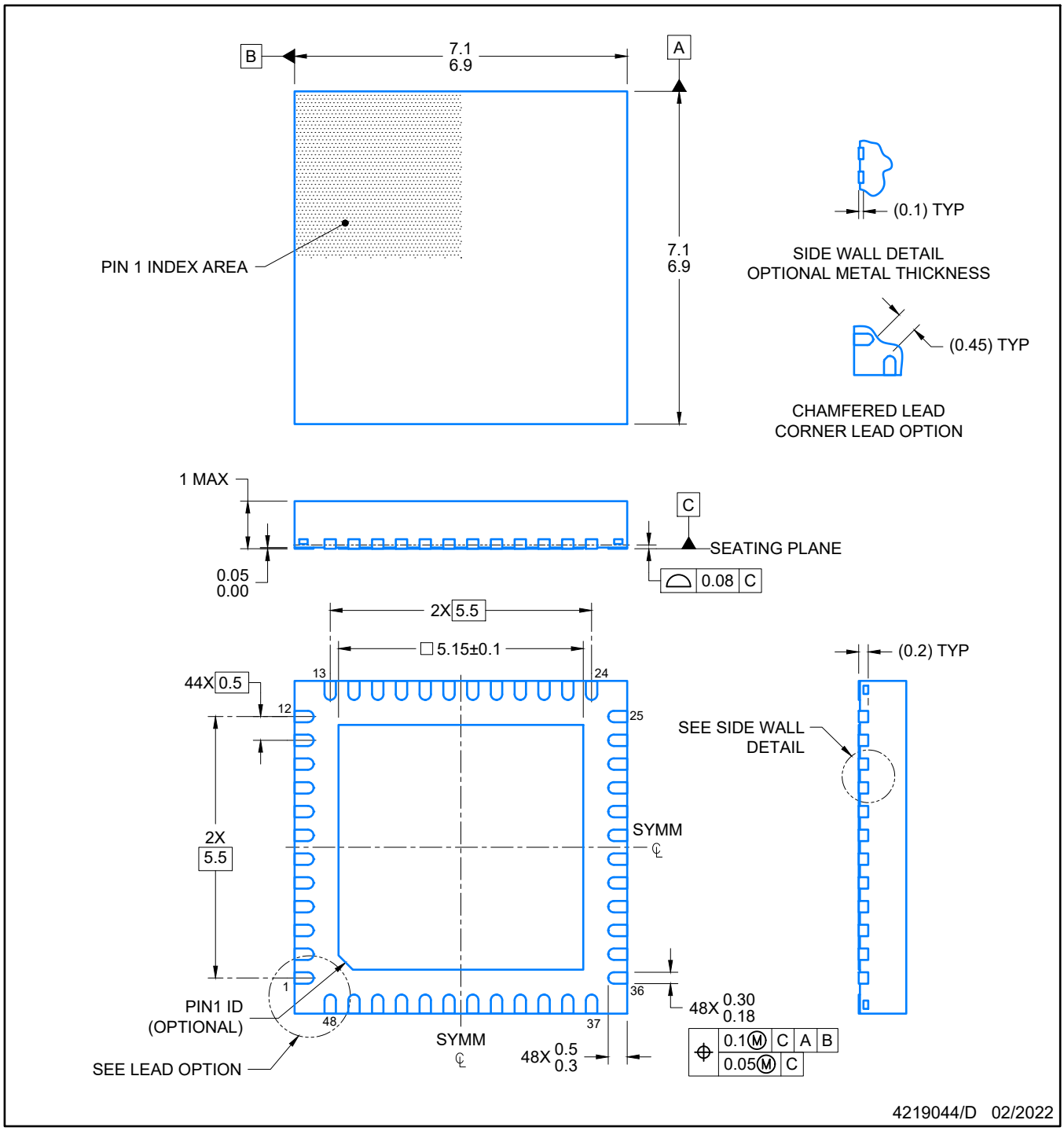
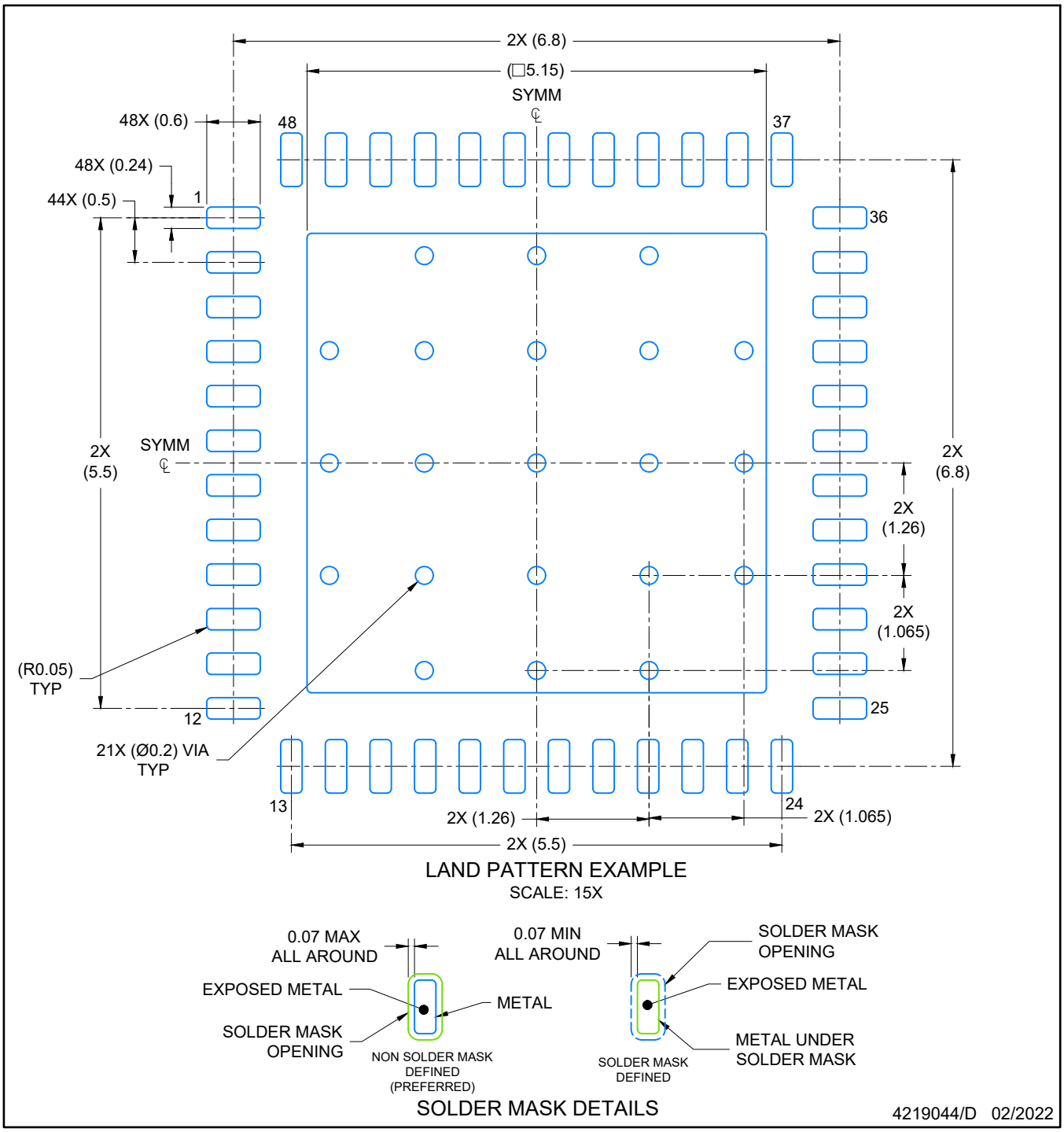
PLASTIC QUADFLAT PACK- NO LEAD



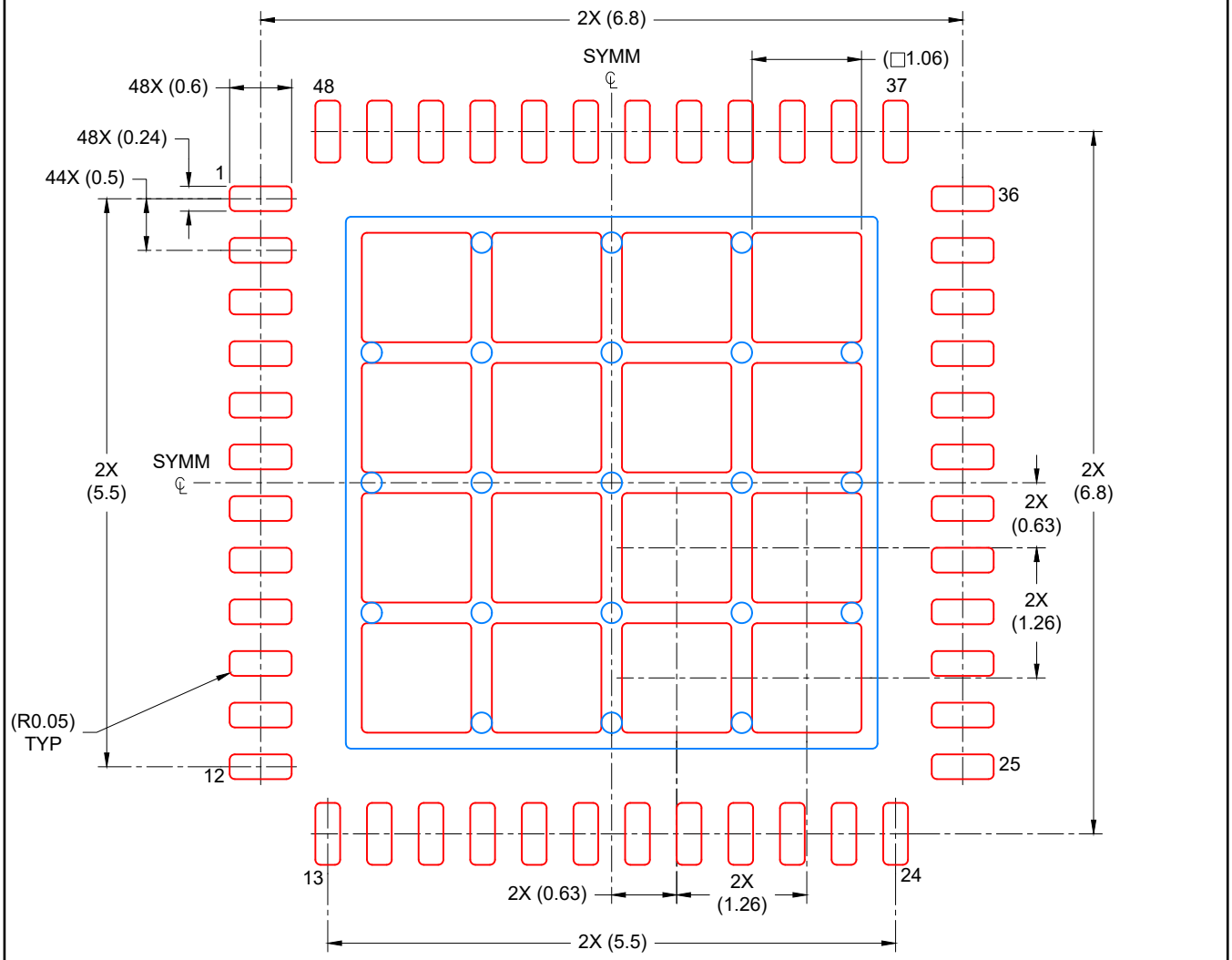
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

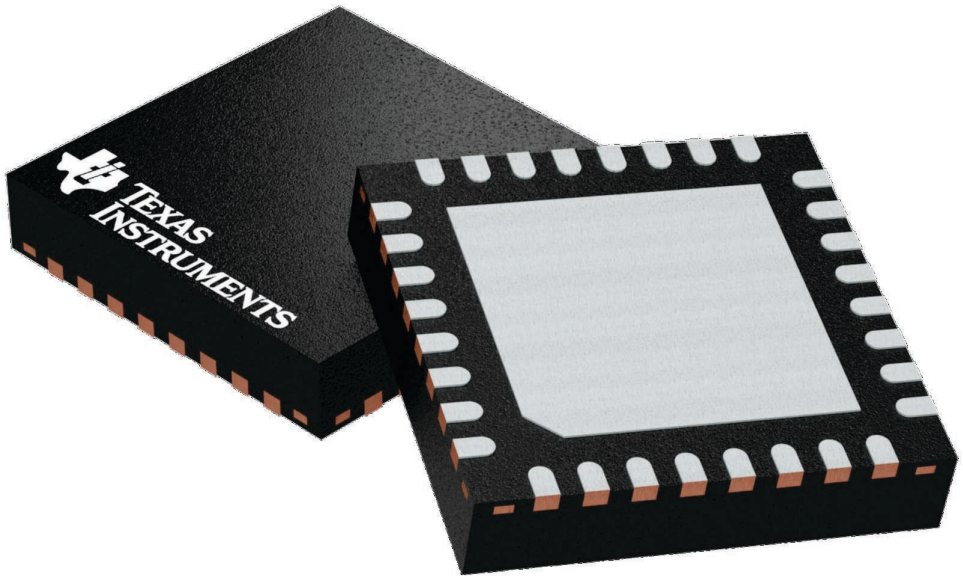
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

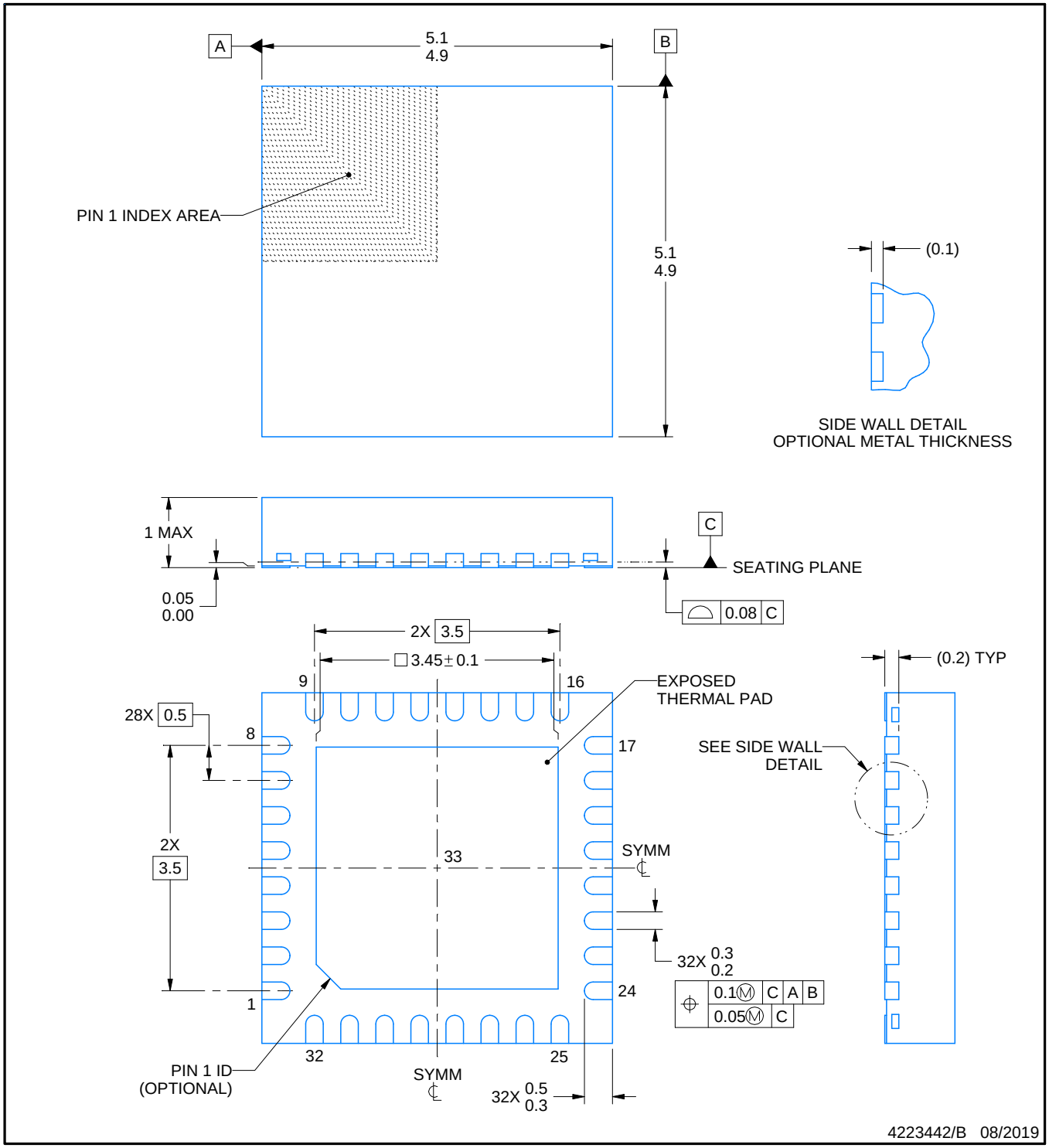
4224745/A

RHB0032E

PACKAGE OUTLINE

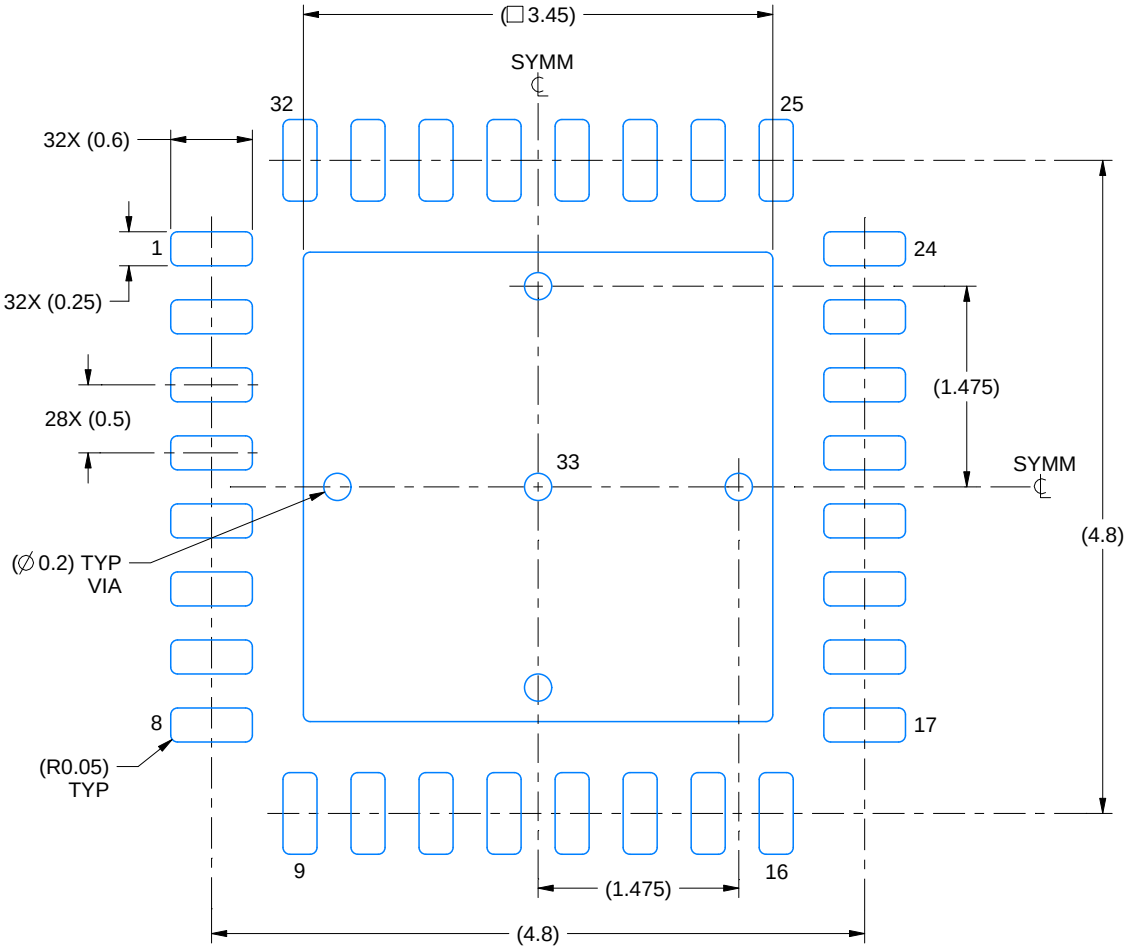
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

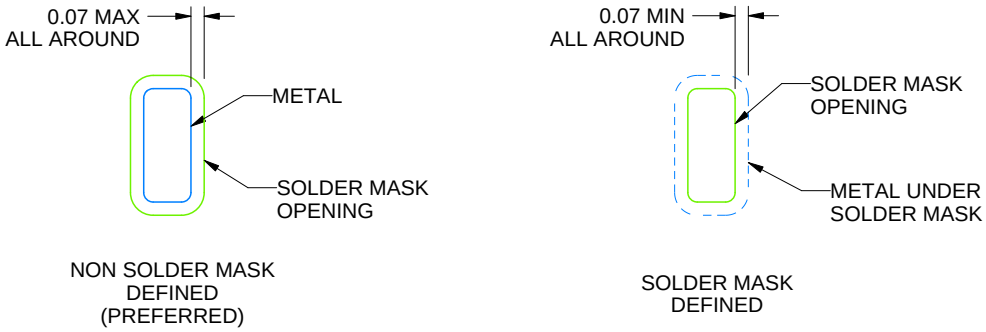


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

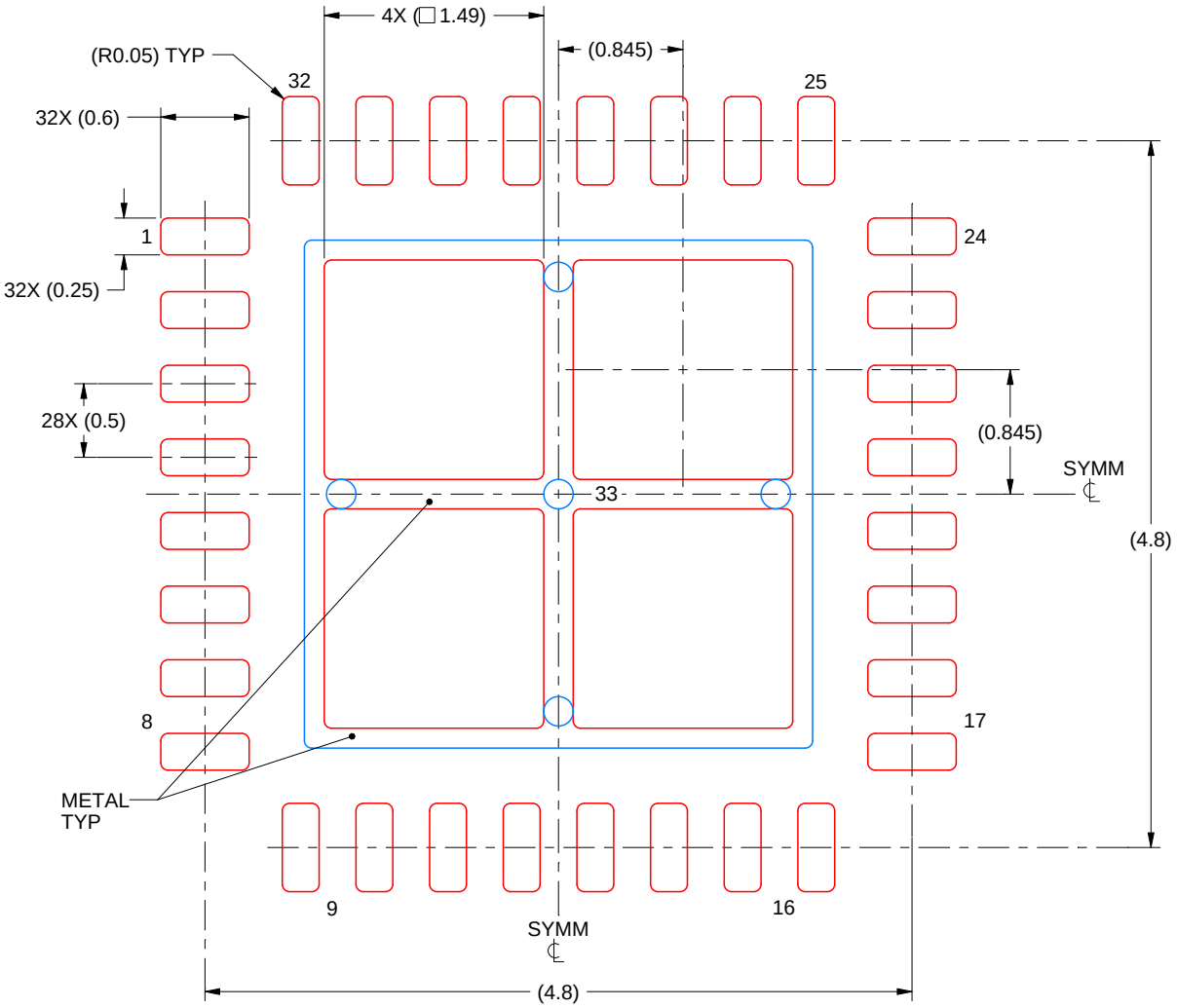


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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