TEXAS INSTRUMENTS
BUF20800-Q1
JAJSEK1C – AUGUST 2011 – REVISED AUGUST 2018

BUF20800-Q1 2つのプログラム可能なVCOMチャネル搭載の18チャネル ガンマ補正用プログラム可能電圧ジェネレータ

1 特長

- **車載アプリケーションに対応**
- **下記内容でAEC-Q100認定済み：**
  - デバイス温度グレード1
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC4
- **低い消費電流**: 900µA/ch
- **アナログ電源電圧**: 7V～18V
- **デジタル電源電圧**: 2V～5.5V
- 18チャネルのガンマ補正
- 2チャネルのプログラム可能なV_{COM}: 50mAのI_{OUT}
- 10ビット分解能
- **レール・ツー・レール出力**
- I^2Cインターフェイス
  - 3.4MHzの高速モード
- **デモ用基板とソフトウェアを利用可能**

2 アプリケーション

- **抵抗ベースのガンマ・ソリューションの代替品**
- TFT-LCDリファレンス・ドライバ
- **動的なガンマ制御**

3 概要

BUF20800-Q1はプログラム可能な電圧リファレンス・ジェネレータで、TFT-LCDパネルのガンマ補正用に設計されています。ガンマ補正用に18のプログラム可能な出力を持ち、V_{COM}調整用に2つのチャネルがあり、それぞれが10ビット分解能です。

すべてのチャネルはI^2Cインターフェイスによりプログラム可能で、最高3.4MHzの高速データ転送に対応しています。

プログラムが可能なため、従来のように各種のガンマ電圧を最適化するため抵抗の値を変更するといった時間を要するプロセスが不要になり、設計者はパネルに適したガンマ電圧を非常に短時間で判定できます。必要な変更は、ハードウェアの変更なしに簡単に実装できます。

BUF20800-Q1はTIの最先端の、ジオメトリが小さいアナログCMOSプロセスを使用しているため、評価のみでなく完全な量産においても非常に有力な選択肢となります。

必要なチャネル数が少ない場合は、お近くの販売またはマーケティング代理店にお問い合わせください。

BUF20800-Q1は、PowerPAD™付きのHTSSOP-38パッケージで供給され、-40℃～+105℃で動作が規定されています。

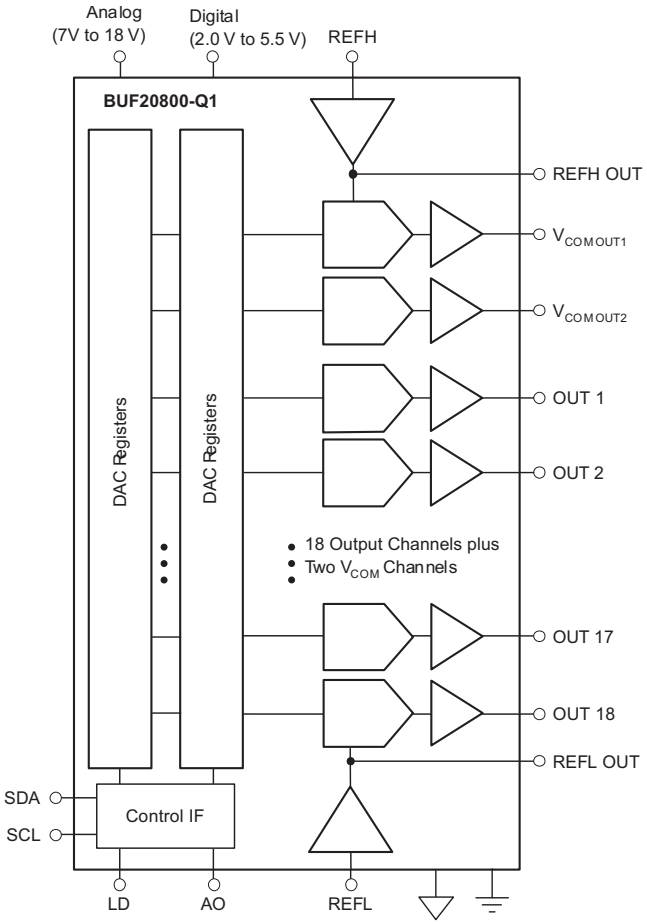
製品情報 (1)

型番	パッケージ	本体サイズ(公称)
BUF20800-Q1	HTSSOP (38)	9.80mm×9.60mm

関連製品

特長	製品名
12チャネルのプログラム可能なバッファ、10ビット	BUF12800
プログラム可能なV_{COM}	BUF01900
11、6、4チャネルのガンマ補正バッファ、18V電源	BUFxx704
高速V_{COM}、1および2チャネル	SN10501
完全なLCD DC/DCソリューション	TPS65100

ブロック概略図



(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (January 2018) から **Revision C** に変更 **Page**

- Changed OUT1-9 high output swing MIN number from "17.7" to "17.6" ... 6
- Added OUT1-9 high output swing for T_A = +25°C" ... 6

Revision A (November 2017) から **Revision B** に変更 **Page**

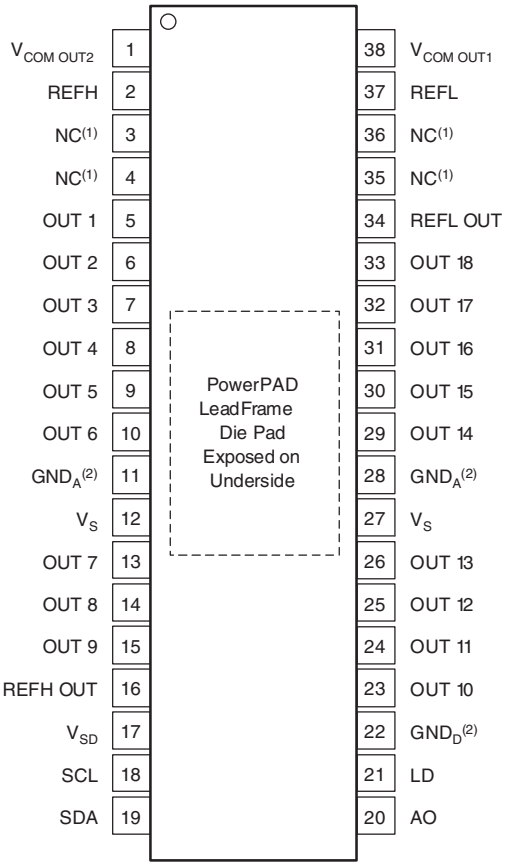
- Added INL spec over temperature ... 6
- Added R1 and R2 callouts and corrected capacitor '10mF' value to '10µF' in Typical Application Configuration ... 22

2011年8月発行のものから更新 **Page**

- 新しいTI標準にフォーマットを変更: 「*製品情報*」表、「*ピン構成および機能*」セクション、「*仕様*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Changed to "Code 978" from "Code 1023" ... 6
- Changed to "Code 32" from "Code 00" ... 6
- Added MAX value for "OUT 10-18 output swing : low " parameter ... 6

5 Pin Configuration and Functions

DCP Package
38-Pin HTSSOP
TOP VIEW



(1) NC denotes no connection

(2) GND_D and GND_A are internally connected and must be at the same voltage potential.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	20	I	Two-wire serial interface address select pin
GND_A	28	—	Analog ground. Must be connected to digital ground GND_D.
	11		
GND_D	22	—	Digital ground. Must be connected to analog ground GND_A.
LD	21		Output latch pin
NC	3	—	No connection. Leave this pin floating.
	4		
	35		
	36		
OUT1	5	O	DAC output 1
OUT2	6	O	DAC output 2
OUT3	7	O	DAC output 3
OUT4	8	O	DAC output 4
OUT5	9	O	DAC output 5

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT6	10	O	DAC output 6
OUT7	13	O	DAC output 7
OUT8	14	O	DAC output 8
OUT9	15	O	DAC output 9
OUT10	23	O	DAC output 10
OUT11	24	O	DAC output 11
OUT12	25	O	DAC output 12
OUT13	26	O	DAC output 13
OUT14	29	O	DAC output 14
OUT15	30	O	DAC output 15
OUT16	31	O	DAC output 16
OUT17	32	O	DAC output 17
OUT18	33	O	DAC output 18
REFH	2	I	Reference voltage REFH input
REFH OUT	16	O	Reference voltage REFH output
REFL	37	I	Reference voltage REFL input
REFL OUT	34	O	Reference voltage REFL output
SCL	18	I	Serial clock input; open drain.
SDA	19	I/O	Serial data I/O; open drain.
VCOMOUT1	38	O	VCOM channel 1
VCOMOUT2	1	O	VCOM channel 2
VS	12	I	Analog supply
	27		
VSD	17	I	Digital supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1).

PARAMETER			MINIMUM	MAXIMUM	UNIT
V_S	Supply voltage			19	V
V_{SD}	Supply voltage			6	V
	Signal input terminals, SCL, SDA, AO, LD	Voltage	–0.5	6	V
		Current	±10		mA
	Output Short-Circuit (2)		Continuous		
T_A	Operating temperature		–40	+105	°C
T_{stg}	Storage temperature		–65	+150	°C
T_J	Junction temperature			125	°C
	Latch-up per JESD78B		Class 1		

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one channel at a time.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VS	Analog supply	7		18	V
VSD	Digital supply	2		5.5	V
REFH	Reference high	4		VS – 0.2	V
REFL	Reference low	GND + 0.2		VS – 4	V
T_A	Operating ambient temperature	–40		105	°C
T_J	Operating junction temperature			125	°C

6.4 Thermal Information

THERMAL METRIC (1)		BUF20800-Q1 DCP Package (HTSSOP Family) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At T_A = 25°C, V_S = 18 V, V_{SD} = 5 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF20800-Q1 MIN	TYP	MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
	OUT 1−9 output swing: high	Sourcing 10 mA, V_{REFH} = 17.8 V, Code 1023, T_A = –40°C to +105°C	17.6			V
		Sourcing 10 mA, V_{REFH} = 17.8 V, Code 1023, T_A = +25°C	17.7	17.8		
	OUT 10−18 output swing: high	Sourcing 10 mA, V_{REFH} = 17.8 V, Code 978, T_A = –40°C to +105°C	16.8	17.2		
	OUT 1−9 output swing: low	Sinking 10 mA, V_{REFL} = 0.2 V, Code 32, T_A = –40°C to +105°C		0.6	1.0	V
	OUT 10−18 output swing: low	Sinking 10 mA, V_{REFL} = 0.2 V, Code 00, T_A = –40°C to +105°C		0.2	0.4	
	VCOM buffer output swing: high	Sourcing 50 mA, V_{REFH} =17.8 V, T_A = –40°C to +105°C	13	15.5		V
	VCOM buffer output swing: low	Sinking 50 mA, V_{REFL} = 0.2 V, T_A = –40°C to +105°C		1	2.0	V
I_O	Output current (1)	All Channels, Code 512, Sinking/Sourcing	40	45		mA
INL	Integral nonlinearity	No Load, V_{REFH} = 17 V, V_{REFL} = 1 V		0.3	1.5	Bits
		No Load, V_{REFH} = 17 V, V_{REFL} = 1 V, T_A = –40°C to 105°C			2.5	
DNL	Differential nonlinearity	No Load, V_{REFH} = 17 V, V_{REFL} = 1 V		0.3	1	Bits
	Gain error			0.12		%
t_D	Program to out delay			5		µs
	Output accuracy	No Load, V_{REFH} = 17 V, V_{REFL} = 1 V		±20	±50	mV
		No Load, V_{REFH} = 17 V, V_{REFL} = 1 V, T_A = –40°C to +105°C		±25		mV
RI_{NH}	Input resistance at V_{REFH} and V_{REFL}			100		MΩ
REG	Load regulation, All References	V_{OUT} = V_S/2, I_{OUT} = 5 mA to –5 mA Step		0.5	1.5	mV/mA
	40 mA, All Channels	V_{OUT} = V_S/2, $I_{SINKING}$ = 40 mA, $I_{SOURCING}$ = 40 mA		0.5	1.5	mV/mA
ANALOG POWER SUPPLY						
V_S	Operating range		7		18	V
I_S	Total analog supply current	No Load		18	28	mA
		Outputs at Reset Values, No Load, Two-Wire Bus Inactive, T_A = –40°C to +105°C			28	mA
DIGITAL						
V_{IH}	Logic 1 input voltage		0.7 × V_{SD}			V
V_{IL}	Logic 0 input voltage				0.3 × V_{SD}	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 3 mA		0.15	0.4	V
	Input leakage			±0.01	±10	µA
f_{CLK}	Clock frequency	Standard/Fast Mode, T_A = –40°C to +105°C			400	kHz
		High-Speed Mode, T_A = –40°C to +105°C			3.4	MHz

(1) See typical characteristic graph Output Voltage vs Output Current

Electrical Characteristics (continued)

At T_A = 25°C, V_S = 18 V, V_{SD} = 5 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF20800-Q1			UNIT
			MIN	TYP	MAX	
DIGITAL POWER SUPPLY						
V_{SD}	Operating range		2.0		5.5	V
I_{SD}	Digital supply current (2)	Outputs at Reset Values, No Load, Two-Wire Bus Inactive		25	50	µA
		Outputs at Reset Values, No Load, Two-Wire Bus Inactive, T_A = –40°C to +105°C		100		µA
TEMPERATURE RANGE						
	Operating temperature range	Junction Temperature < +125°C	–40		+105	°C
	Storage temperature range		–65		+150	°C
θ_{JA}	Thermal resistance, HTSSOP-38: Junction-to-Ambient			30		°C/W
θ_{JC}	Thermal resistance, HTSSOP-38: Junction-to-Case			15		°C/W

(2) See typical characteristic graph Digital Supply Current vs Temperature

6.6 Typical Characteristics

At T_A = 25°C, V_S = 18 V, V_{SD} = 5 V, V_{REFH} = 17 V, V_{REFL} = 1 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.

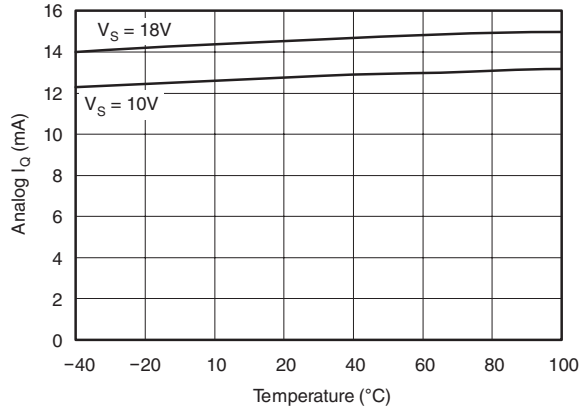


Figure 1. Analog Supply Current vs Temperature

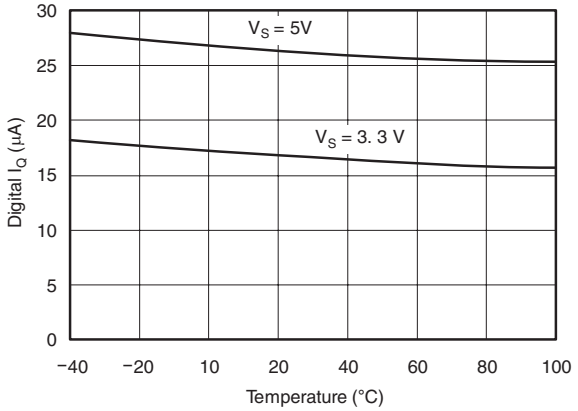


Figure 2. Digital Supply Current vs Temperature

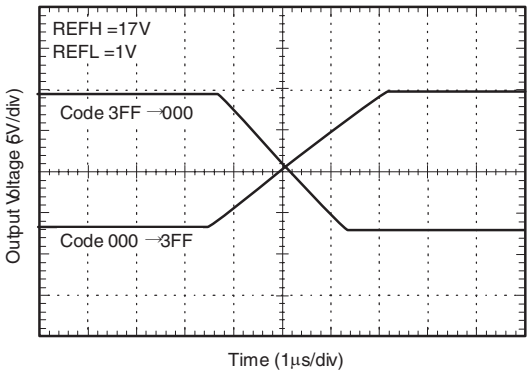


Figure 3. Full−scale Output Swing

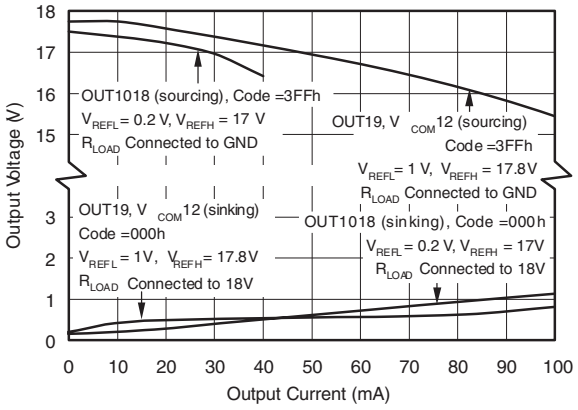


Figure 4. Output Voltage vs Output Current

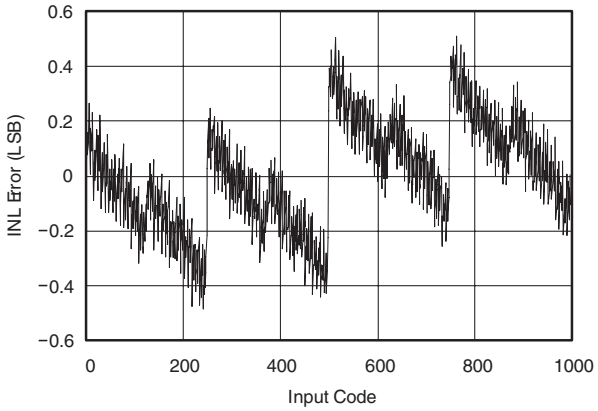


Figure 5. Integral Nonlinearity Error vs Input Code

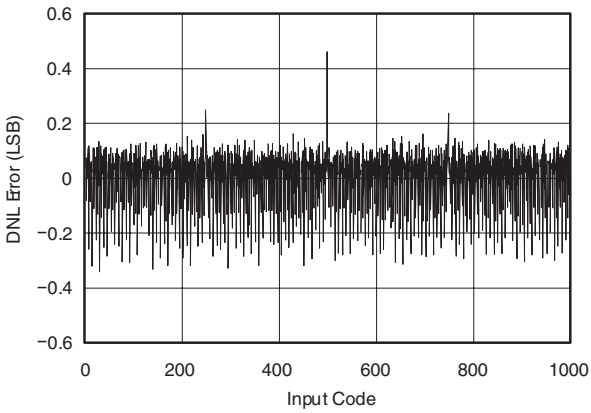


Figure 6. Differential Nonlinearity Error vs Input Code

7 Detailed Description

7.1 Overview

The BUF20800-Q1 programmable voltage reference allows fast, easy adjustment of 18 programmable reference outputs and two channels for V_{COM} adjustment, each with 10-bit resolution. It offers very simple, time-efficient adjustment of the gamma reference and V_{COM} voltages. The BUF20800-Q1 is programmed through a high-speed, standard, two-wire interface. The BUF20800-Q1 features a double-register structure for each DAC channel to simplify the implementation of dynamic gamma control. This structure allows pre-loading of register data and rapid updating of all channels simultaneously.

Buffers 1−9 are able to swing to within 200mV of the positive supply rail, and to within 0.6V of the negative supply rail. Buffers 10−18 are able to swing to within 0.8V of the positive supply rail and to within 200mV of the negative supply rail.

The BUF20800-Q1 can be powered using an analog supply voltage from 7V to 18V, and a digital supply from 2V to 5.5V. The digital supply must be applied prior to or simultaneously with the analog supply to avoid excessive current and power consumption; damage to the device may occur if it is left connected only to the analog supply for extended periods of time. Figure 7 shows the power supply timing requirements.

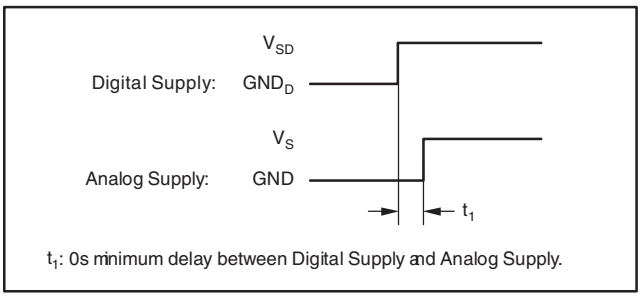
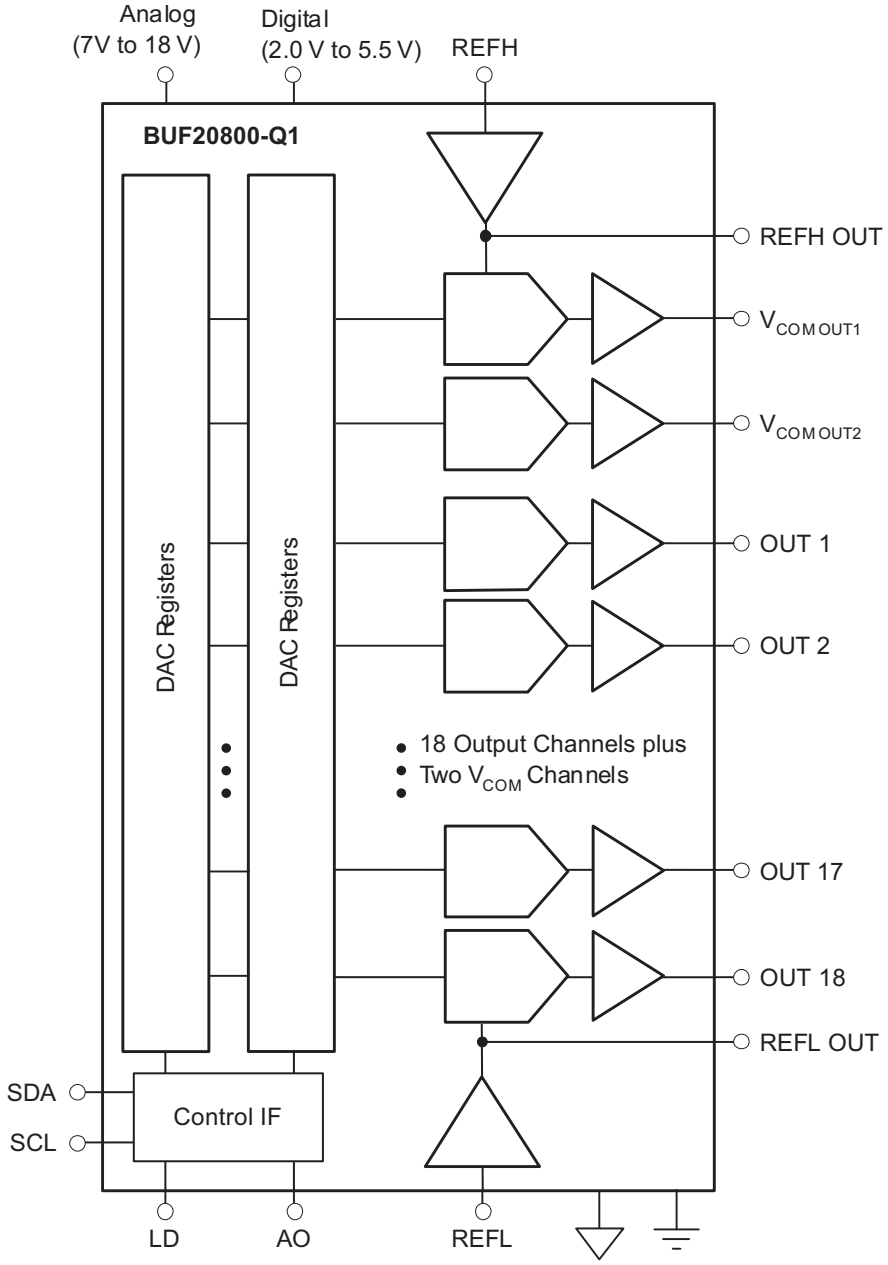


Figure 7. Power Supply Timing Requirements

Figure 14 shows the BUF20800-Q1 in a typical configuration. In this configuration, the BUF20800-Q1 device address is 74h. The output of each digital-to-analog converter (DAC) is immediately updated as soon as data are received in the corresponding register (LD = 0).

For maximum dynamic range, set $V_{REFH} = V_S - 0.2$ V and $V_{REFL} = GND + 0.2$ V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 General-call Reset and Power-up

The BUF20800-Q1 responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF20800-Q1 acknowledges both bytes. Upon receiving a General Call Reset, the BUF20800-Q1 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

Feature Description (continued)

The BUF20800-Q1 automatically performs a reset upon power up. As part of the reset, all outputs are set to $(V_{REFH} - V_{REFL})/2$. Other reset values are available as a custom modification—contact your TI representative for details.

The BUF20800-Q1 resets all outputs to $(V_{REFH} - V_{REFL})/2$ after sending the device address, if a valid DAC address is sent with bits D7 to D5 set to '100'. If these bits are set to '010', only the DAC being addressed in this most significant byte (MSB) and the following least significant byte (LSB) will be reset.

7.3.2 Output Voltage

Buffer output values are determined by the reference voltages (VREFH and VREFL) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = \left[\frac{V_{REFH} - V_{REFL}}{1024} \times \text{Decimal Value of Code}\right] + V_{REFL} \quad (1)$$

The valid voltage ranges for the reference voltages are:

$$4V \le V_{REFH} - V_S \le 0.2\ V \text{ and } 0.2\ V \le V_{REFL} \le V_S - 4\ V \quad (2)$$

The BUF20800-Q1 outputs are capable of a full-scale voltage output change in typically 5 μs—no intermediate steps are required.

7.3.3 Output Latch

Updating the DAC register is not the same as updating the DAC output voltage, because the BUF20800-Q1 features a double-buffered register structure. There are three methods for latching transferred data from the storage registers into the DACs to update the DAC output voltages.

Method 1 requires externally setting the latch pin (LD) LOW, LD = LOW, which will update each DAC output voltage whenever its corresponding register is updated.

Method 2 externally sets LD = HIGH to allow all DAC output voltages to retain their values during data transfer and until LD = LOW, which will then simultaneously update the output voltages of all DACs to the new register values. Use this method to transfer a future data set in advance to prepare for a very fast output voltage update.

Method 3 uses software control. LD is maintained HIGH, and all DACs are updated when the master writes a 1 in bit 15 of any DAC register. The update will occur after receiving the 16-bit data for the currently-written register.

The General Call Reset and the power-up reset will update the DAC regardless of the state of the latch pin.

7.3.4 Programmable VCOM

The V_{COM} channels of the BUF20800-Q1 can swing to 2V from the positive supply rail while sourcing 50 mA and to 1 V above the negative rail while sinking 50 mA (see Figure 4, typical characteristic *Output Voltage vs Output Current*). To store the gamma and the V_{COM} values, an external EEPROM is required. During power-up of the LCD panel, the timing controller can then read the EEPROM and load the values into the BUF20800-Q1 to generate the desired V_{COM} voltages, as illustrated in Figure 10 and Figure 8. The V_{COM} channels can be programmed independently from the gamma channels.

Feature Description (continued)

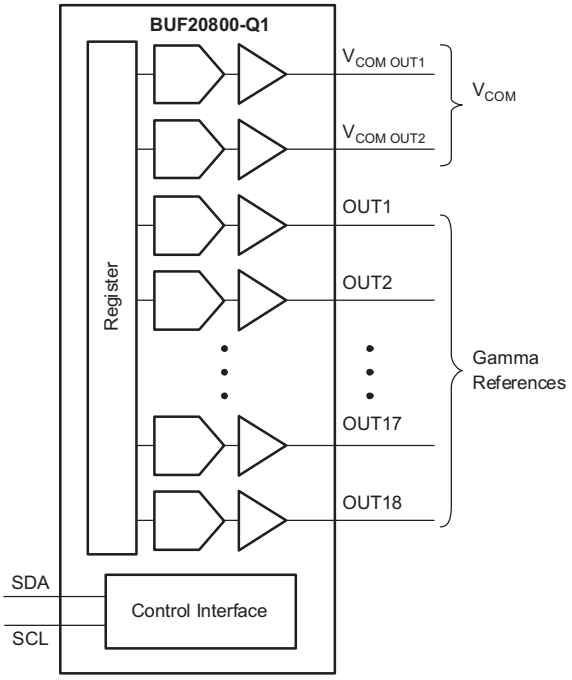


Figure 8. BUF20800-Q1 Used for Programmable V_{COM}

7.3.5 REFH and REFL Input range

Best performance and output swing range of the BUF20800-Q1 are achieved by applying REFH and REFL voltages that are slightly below the power-supply voltages. Most specifications have been tested at REFH = V_S − 200mV and REFL = GND + 200mV. The REFH internal buffer is designed to swing very closely to V_S and the REFL internal buffer to GND. However, there is a finite limit on how close they can swing before saturating. To avoid saturation of the internal REFH and REFL buffers, the REFH voltage should not be greater than V_S −100mV and REFL voltage should not be lower than GND + 100mV. Figure 9 shows the swing capability of the REFH and REFL buffers.

The other consideration when trying to maximize the output swing capability of the gamma buffers is the limitation in the swing range of output buffers (OUT1−18, V_{COM1}, and V_{COM2}), which depends on the load current. A typical load in the LCD application is 5−10mA. For example, if OUT1 is sourcing 10mA, the swing is typically limited to about V_S − 200mV. The same applies to OUT18, which typically limits at GND + 200mV when sinking 10mA. An increase in output swing can only be achieved for much lighter loads. For example, a 3mA load typically allows the swing to be increased to approximately V_S − 100mV and GND + 100mV.

Connecting REFH directly to V_S and REFL directly to GND does not damage the BUF20800-Q1. As discussed above however, the output stages of the REFH and REFL buffers will saturate. This condition is not desirable and can result in a small error in the measured output voltages of OUT1−18, V_{COM1}, and V_{COM2}. As described above, this method of connecting REFH and REL does not help to maximize the output swing capability.

Feature Description (continued)

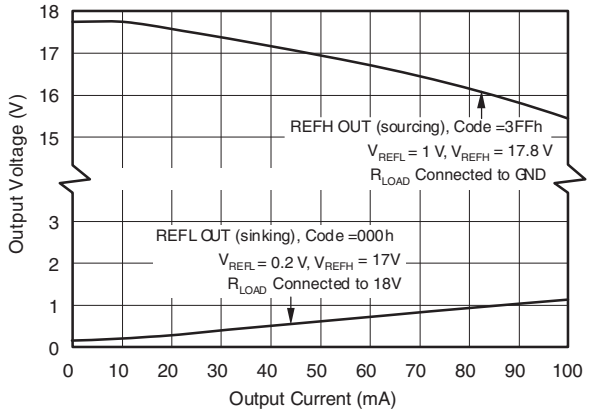


Figure 9. Reference Buffer Output Voltage vs Output Current

7.4 Device Functional Modes

7.4.1 Replacement of Traditional Gamma Buffer

Traditional gamma buffers rely on a resistor string (often using expensive 0.1% resistors) to set the gamma voltages. During development, the optimization of these gamma voltages can be time-consuming. Programming these gamma voltages with the BUF20800-Q1 can significantly reduce the time required for gamma voltage optimization. The final gamma values can be written into an external EEPROM to replace a traditional gamma buffer solution. During power-up of the LCD panel, the timing controller reads the EEPROM and loads the values into the BUF20800-Q1 to generate the desired gamma voltages. Figure 10a shows the traditional resistor string; Figure 10b shows the more efficient alternative method using the BUF20800-Q1.

BUF20800-Q1 uses the most advanced high-voltage CMOS process available today, which allows it to be competitive with traditional gamma buffers.

This technique offers significant advantages:

- It shortens development time significantly.
- It allows demonstration of various gamma curves to LCD monitor makers by simply uploading a different set of gamma values.
- It allows simple adjustment of gamma curves during production to accommodate changes in the panel manufacturing process or end-customer requirements.
- It decreases cost and space.

Device Functional Modes (continued)

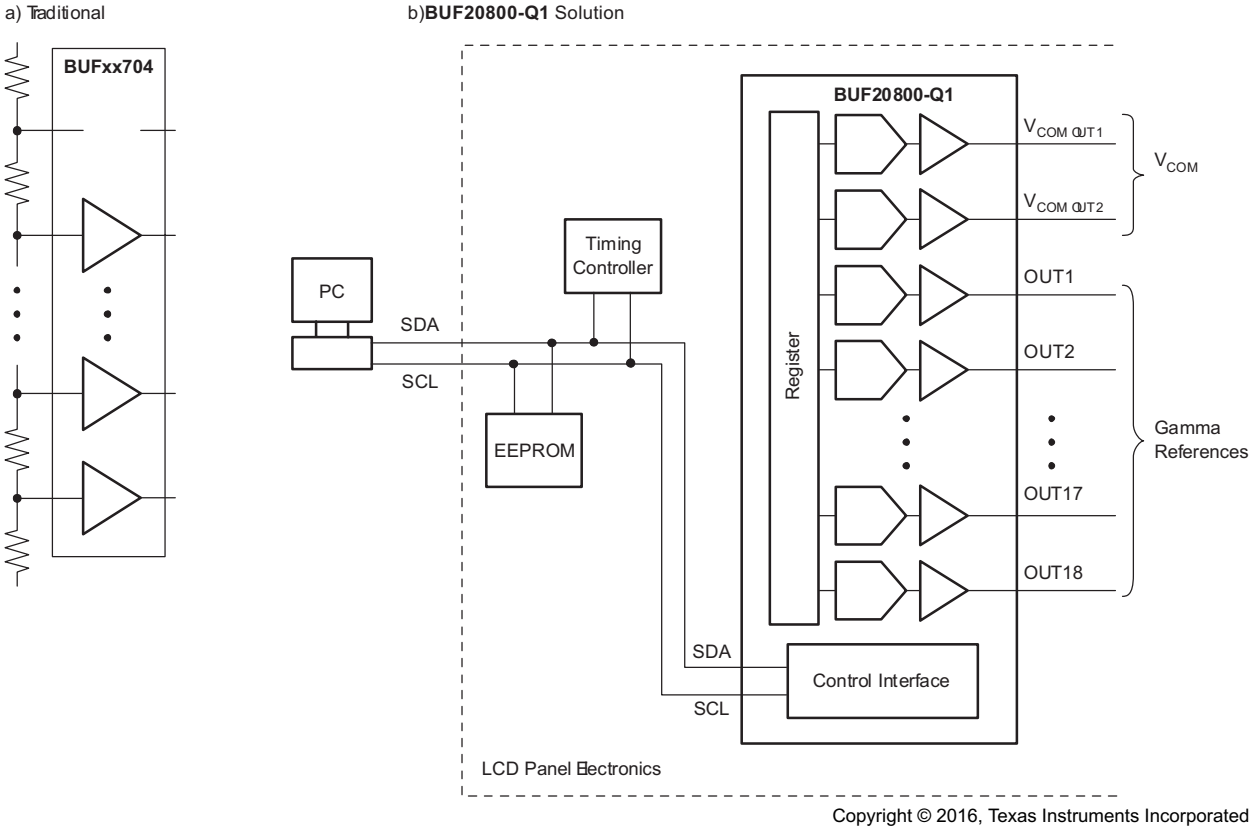


Figure 10. Replacement of the Traditional Gamma Buffer

7.4.2 Dynamic Gamma Control

Dynamic gamma control is a technique used to improve the picture quality in LCD TV applications. The brightness in each picture frame is analyzed and the gamma curves are adjusted on a frame-by-frame basis. The gamma curves are typically updated during the short vertical blanking period in the video signal. Figure 11 shows a block diagram using the BUF20800-Q1 for dynamic gamma control and V_{COM} output.

The BUF20800-Q1 is ideally suited for rapidly changing the gamma curves because of its unique topology:

- double register input structure to the DAC;
- fast serial interface;
- simultaneous updating of all DACs by software. See the Read/Write Operations to write to all registers and the Output Latch sections.

The double register input structure saves programming time by allowing updated DAC values to be pre-loaded into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC output values remain unchanged—the display is unaffected. During the vertical sync period, the DAC outputs (and therefore, the gamma voltages) can be quickly updated either by using an additional control line connected to the LD pin, or through software—writing a '1' in bit 15 of any DAC register. For the details on the operation of the double register input structure, see the Output Latch section.

Example: Update all 18 gamma registers simultaneously via software.

Step 1: Check if LD pin is placed in HIGH state.

Step 2: Write DAC Registers 1−18 with bit 15 always '0'.

Device Functional Modes (continued)

Step 3: Write any DAC register a second time with identical data. Make sure that bit 15 is '1'. All DAC channels will be updated simultaneously after receiving the last bit of data. (Note: this step may be eliminated by setting bit 15 of DAC 18 to '1' in the previous step.)

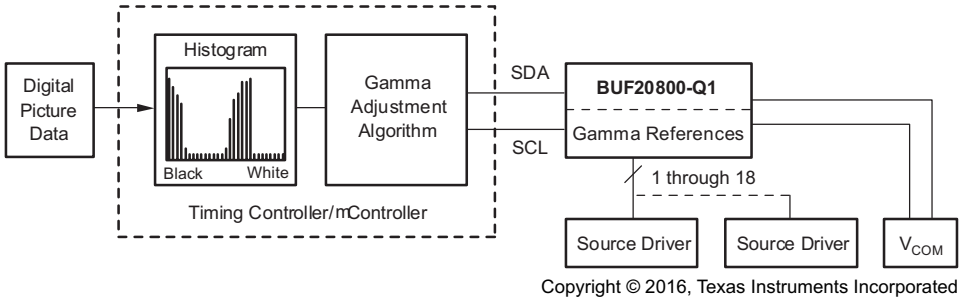


Figure 11. Dynamic Gamma Control

7.5 Programming

7.5.1 Two-wire Bus Overview

The BUF20800-Q1 communicates through an industry standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the 9th clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF20800-Q1 can act only as a slave device; therefore, it never drives SCL. SCL is only an input for the BUF20800-Q1. Table 1 and Table 2 summarize the address and command codes, respectively, for the BUF20800-Q1.

7.5.2 Data Rates

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF20800-Q1 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001xxx, with SCL = 400kHz, following the START condition; xxx are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF20800-Q1 will respond to the High-speed command regardless of the value of these last three bits. The BUF20800-Q1 will not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. On receiving a master code, the BUF20800-Q1 will switch on its Hs mode filters, and communicate at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF20800-Q1 will switch out of Hs mode with the next STOP condition.

Programming (continued)

7.5.3 Read/Write Operations

The BUF20800-Q1 is able to read from a single DAC, or multiple DACs, or write to the register of a single DAC, or multiple DACs in a single communication transaction. DAC addresses begin with 0000 0000, which corresponds to DAC_1, through 0001 0011, which corresponds to V_{COM} OUT2.

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH will perform a read transaction.

7.5.3.1 Writing

To write to a single DAC register

1. 1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send a DAC address byte. Bits D7−D5 must be set to 0. Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10011 are valid and will be acknowledged. Table 3 shows the DAC addresses.
4. Send two bytes of data for the specified DAC register. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 are used, and bits D15−D14 must not be 01), followed by the least significant byte (bits D7−D0). The register is updated after receiving the second byte.
5. Send a STOP condition on the bus

The BUF20800-Q1 will acknowledge each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register will not be updated. Updating the DAC register is not the same as updating the DAC output voltage. See the Output Latch section.

The process of updating multiple DAC registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF20800-Q1 automatically and sequentially steps through subsequent registers as additional data is sent. The process continues until all desired registers have been updated or a STOP condition is sent.

To write to multiple DAC registers:

1. 1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be updated. The BUF20800-Q1 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning), followed by the least significant byte (bits D7−D0). The first two bytes are for the DAC addressed in step 3 above. Its register is automatically updated after receiving the second byte. The next two bytes are for the following DAC. That DAC register is updated after receiving the fourth byte. This process continues until the registers of all following DACs have been updated.
5. Send a STOP condition on the bus.

The BUF20800-Q1 will acknowledge each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data will be updated.

Programming (continued)

7.5.3.2 Reading

Reading a DAC register will return the data stored in the DAC. This data can differ from the data stored in the DAC register. See the Output Latch section.

To read the DAC value:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send the DAC address byte. Bits D7−D5 must be set to 0; Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10011 are valid and will be acknowledged.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF20800-Q1 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8; only bits D9 and D8 have meaning); the next byte is the least significant byte (bits D7−D0).
7. Acknowledge after receiving the first byte.
8. Do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

To Read Multiple DACs:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be read. The BUF20800-Q1 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF20800-Q1 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, only bits D9 and D8 have meaning); the next byte is the least significant byte (bits D7−D0).
7. Acknowledge after receiving each byte of data except for the last byte. The acknowledge bit of the last byte should be HIGH to end the read operation.
8. When all desired DACs have been read, send a STOP or repeated START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

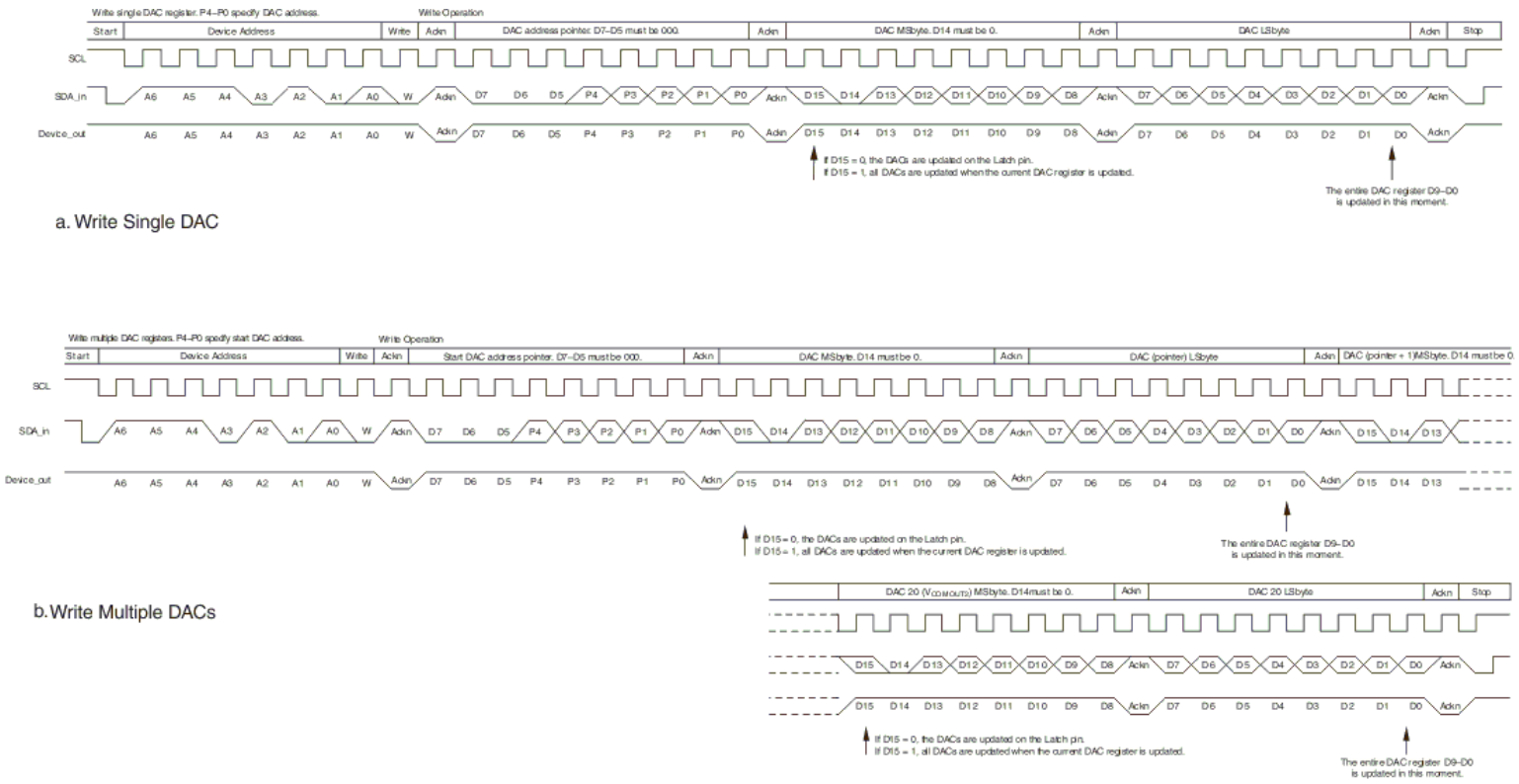


Figure 12. Timing Diagram for Write DAC Register

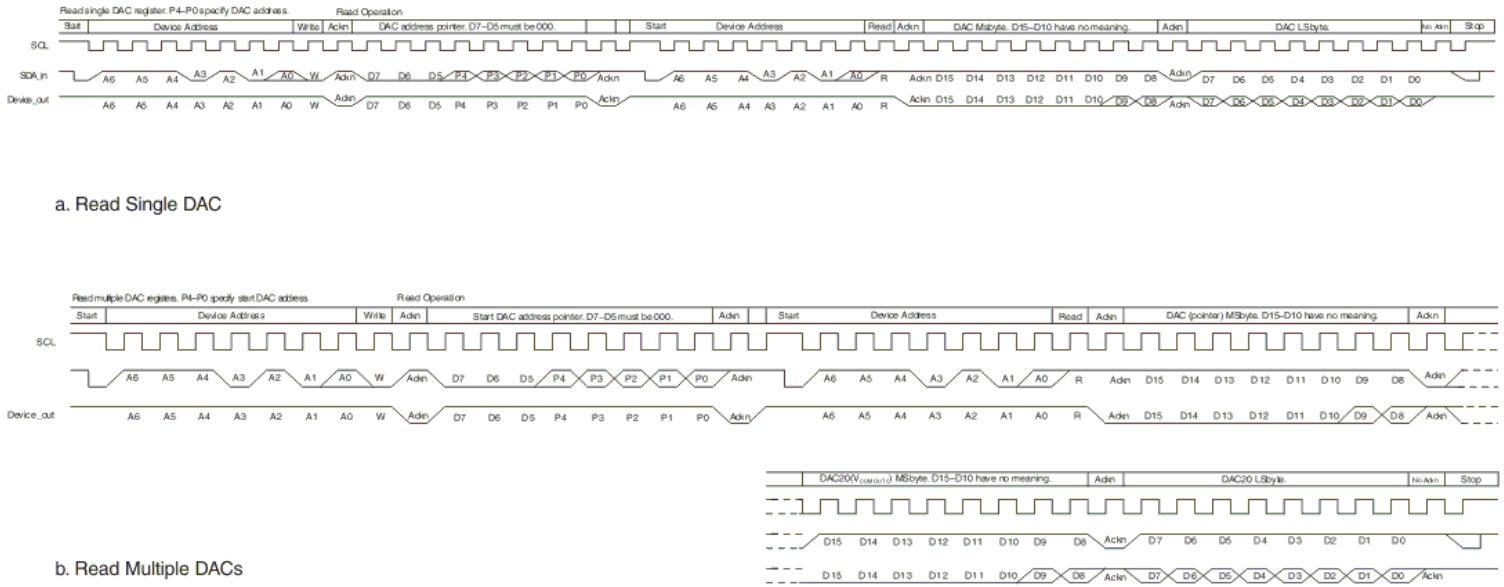


Figure 13. Timing Diagram for Read DAC Register

7.5.4 Register Maps

7.5.4.1 Addressing the BUF20800-Q1

The address of the BUF20800-Q1 is 111010x, where x is the state of the A0 pin. When the A0 pin is LOW, the device will acknowledge on address 74h (1110100). If the A0 pin is HIGH, the device will acknowledge on address 75h (1110101).

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick-Reference Table of BUF20800-Q1 Addresses

DEVICE/COMPONENT	
BUF20800-Q1 Address:	**ADDRESS**
A0 pin is LOW (device acknowledges on address 74h)	1110100
A0 pin is HIGH (device acknowledges on address 75h)	1110101

Table 2. Quick-Reference Table of Command Codes

COMMAND	CODE
General Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

7.5.5 Registers

Table 3. DAC Addresses

DAC	ADDRESS
DAC_1	0000 0000
DAC_2	0000 0001
DAC_3	0000 0010
DAC_4	0000 0011
DAC_5	0000 0100
DAC_6	0000 0101
DAC_7	0000 0110
DAC_8	0000 0111
DAC_9	0000 1000
DAC_10	0000 1001
DAC_11	0000 1010
DAC_12	0000 1011
DAC_13	0000 1100
DAC_14	0000 1101
DAC_15	0000 1110
DAC_16	0000 1111
DAC_17	0001 0000
DAC_18	0001 0001
V_{COM} OUT1	0001 0010
V_{COM} OUT2	0001 0011

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

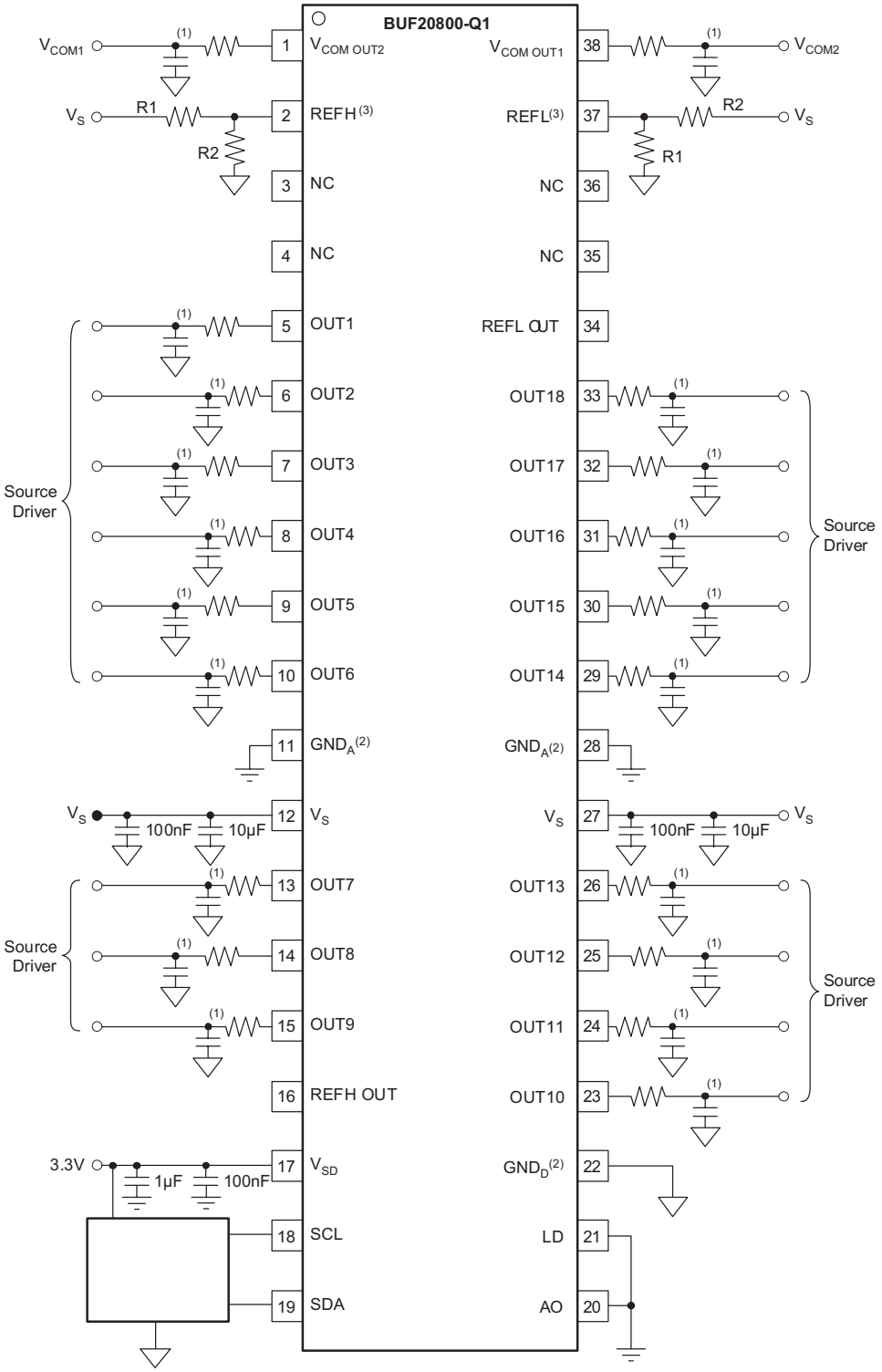
8.1 Application Information

The BUF20800-Q1 device was designed to provide 18 programmable outputs for gamma correction for the source driver IC and two VCOM channels for the common plane in LCD display applications.

8.2 Typical Application

Figure 14 shows a typical application circuit for the BUF20800-Q1 device.

Typical Application (continued)



(1) RC combination optional.
(2) GND_A and GND_D must be connected together.
(3) Connecting a capacitor to this node is not recommended.

Figure 14. Typical Application Configuration

Typical Application (continued)

8.2.1 Design Requirements

Table 4 shows the design parameters for this design.

Table 4. Design Requirements

PARAMETER	SYMBOL	VALUE
Analog Input Supply Voltage	V_S	18 V
Digital Input Supply Voltage	V_{SD}	5 V
REFH Input Voltage	V_{REFH}	17.8 V
REFL Input Voltage	V_{REFL}	0.2 V

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. Connect a 10-µF capacitor in parallel to a 100-nF capacitor to all the analog input supply pins as shown in Figure 14. Connecting a 1-µF capacitor in parallel to a 100-nF capacitor is as well recommended at the digital input supply pin.

8.2.2.2 REFH and REFL Voltage Settings

The resistors R1 and R2 in Figure 14 shall be selected such as the ratio R2/(R1+R2) is close to 17/18. Use for instance R1 = 1 kΩ and R2 = 75 kΩ.

8.2.3 Application Curves

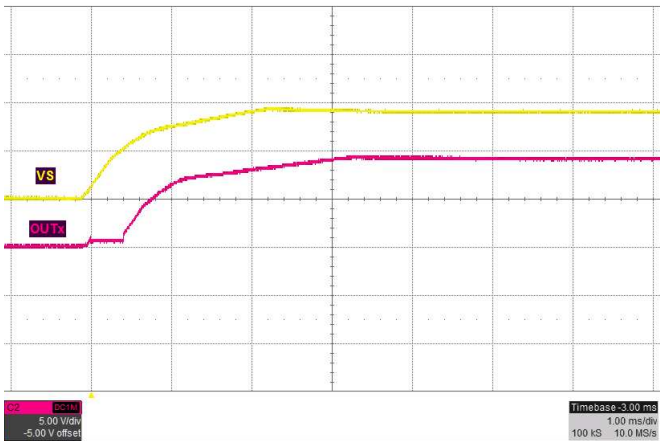


Figure 15. Power-Up Response

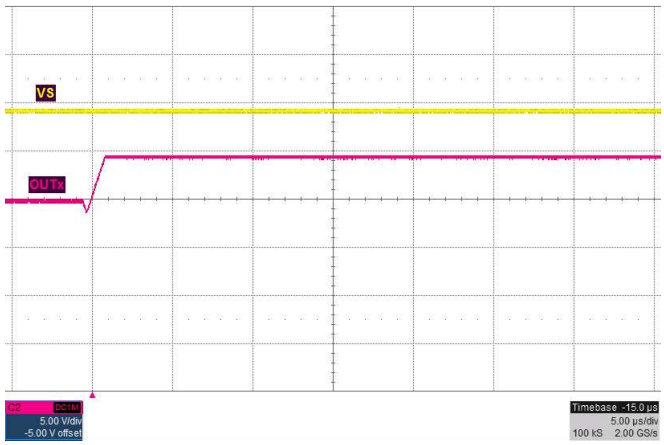


Figure 16. Output Response to a General-Call Reset

8.2.4 Configuration for 20 Gamma Channels

The VCOM outputs can be used as additional gamma references in order to achieve two additional gamma channels (20 total). The VCOM outputs will behave the same as the OUT1−9 outputs when sourcing or sinking smaller currents (see Figure 4). The VCOM outputs are better able to swing to the positive rail than to the negative rail. Therefore, it is better to use the VCOM outputs for higher reference voltages, as shown in Figure 17.

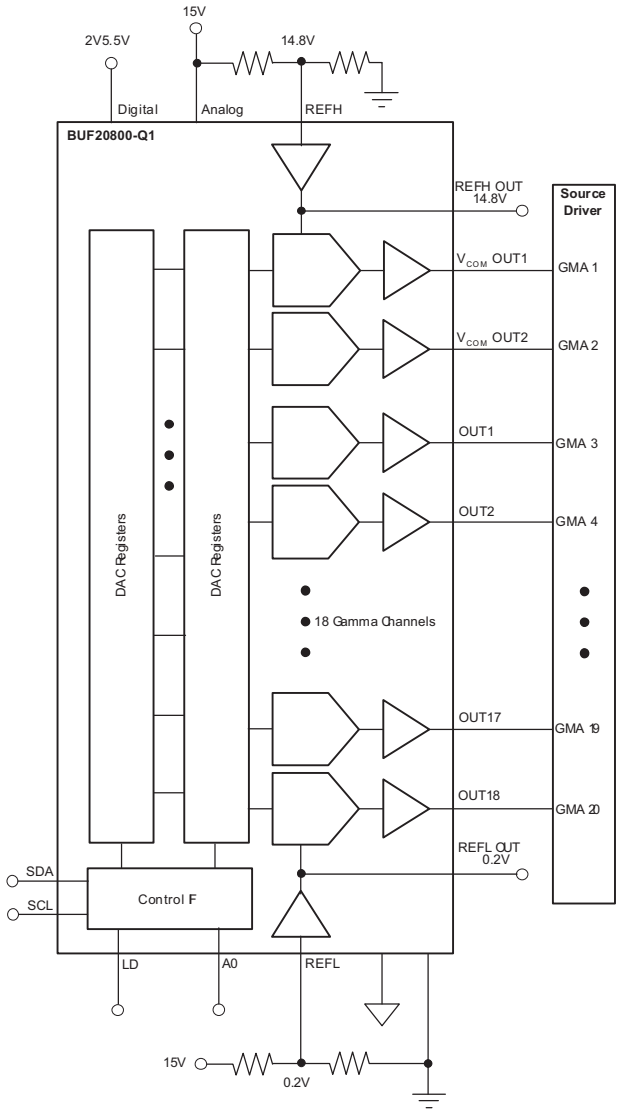


Figure 17. 20 Gamma Channel Solution − Two V_{COM} Channels Used as Additional Gamma Channels

8.2.5 Configuration for 22 Gamma Channels

In addition to the V_{COM} outputs, the REFH and REFL OUT outputs can also be used as fixed gamma references. The output voltage will be set by the REFH and REFL input voltages, respectively. Therefore, REFH OUT should be used for the highest voltage gamma reference, and REFL OUT for the lowest voltage gamma reference. A 22-channel solution can be created by using all 18 outputs, the two V_{COM} outputs, and both REFH/L OUT outputs for gamma references—see Figure 15. However, the REFH and REFL OUT buffers were designed to only drive light loads on the order of 5−10mA. Driving capacitive loads is not recommended with these buffers. In addition, the REFH and REFL buffers must not be allowed to saturate from sourcing/sinking too much current from REFH OUT or REFL OUT. Saturation of the REFH and REFL buffers results in errors in the voltages of OUT1−18 and V_{COM} OUT1−2. The BUF01900 can be used to provide a programmable V_{COM} output.

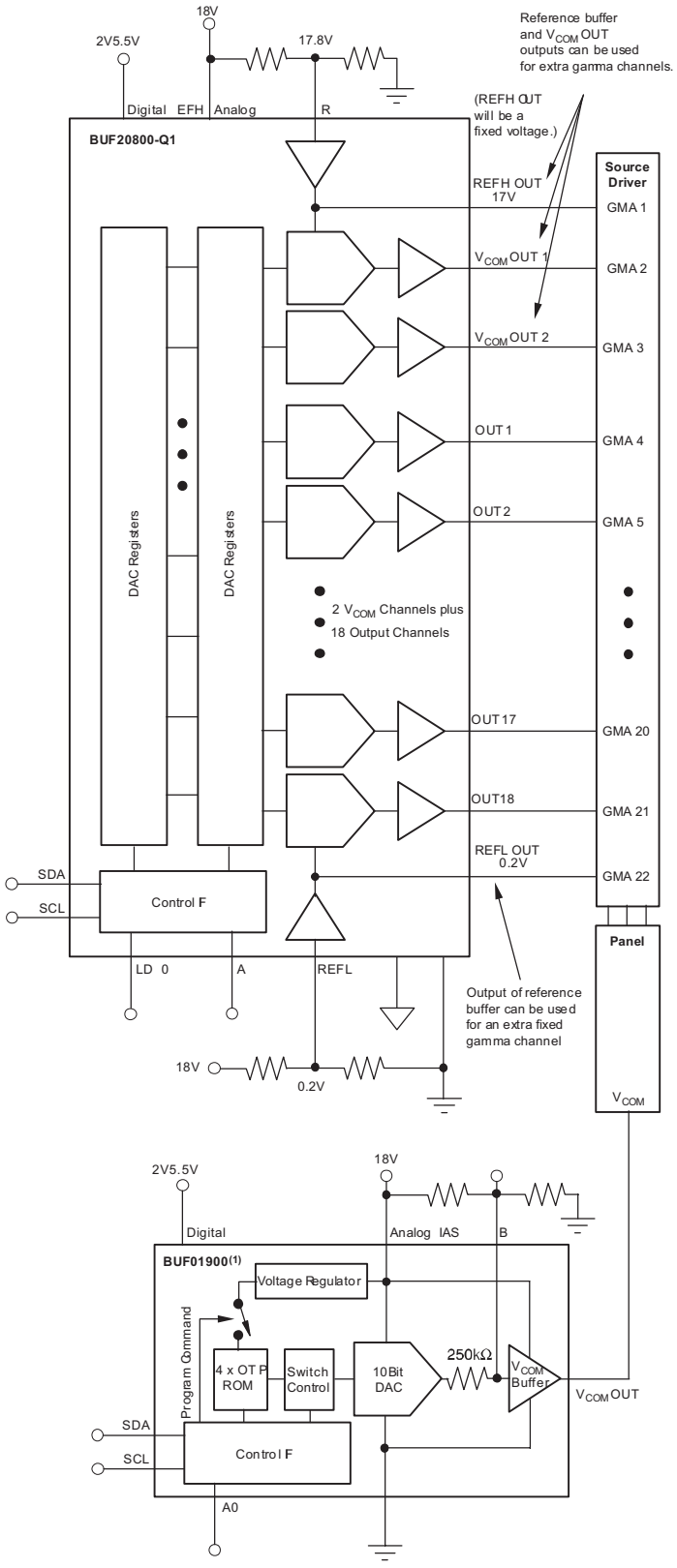


Figure 18. 22-Channel Gamma Solution

8.2.6 The BUF20800-Q1 in Industrial Applications

The wide supply range, high output current, and very low cost make the BUF20800-Q1 attractive for a range of medium accuracy industrial applications such as programmable power supplies, multi-channel data-acquisition systems, data loggers, sensor excitation and linearization, power-supply generation, and other uses. Each DAC channel features 1LSB DNL and INL.

Many systems require different levels of biasing and power supply for various components as well as sensor excitation, control-loop set-points, voltage outputs, current outputs, and other functions. The BUF20800-Q1, with its 20 total programmable DAC channels, provides great flexibility to the entire system by allowing the designer to change all these parameters via software.

Figure 19 provides various ideas on how the BUF20800-Q1 can be used in applications. A micro-controller with two-wire serial interface controls the various DACs of the BUF20800-Q1. The BUF20800-Q1 can be used for:

- sensor excitation
- programmable bias/reference voltages
- variable power-supplies
- high-current voltage output
- 4-20mA output
- set-point generators for control loops

NOTE: The output voltages of the BUF20800-Q1 DACs will be set to $(V_{REFH} - V_{REFL})/2$ at power-up or reset.

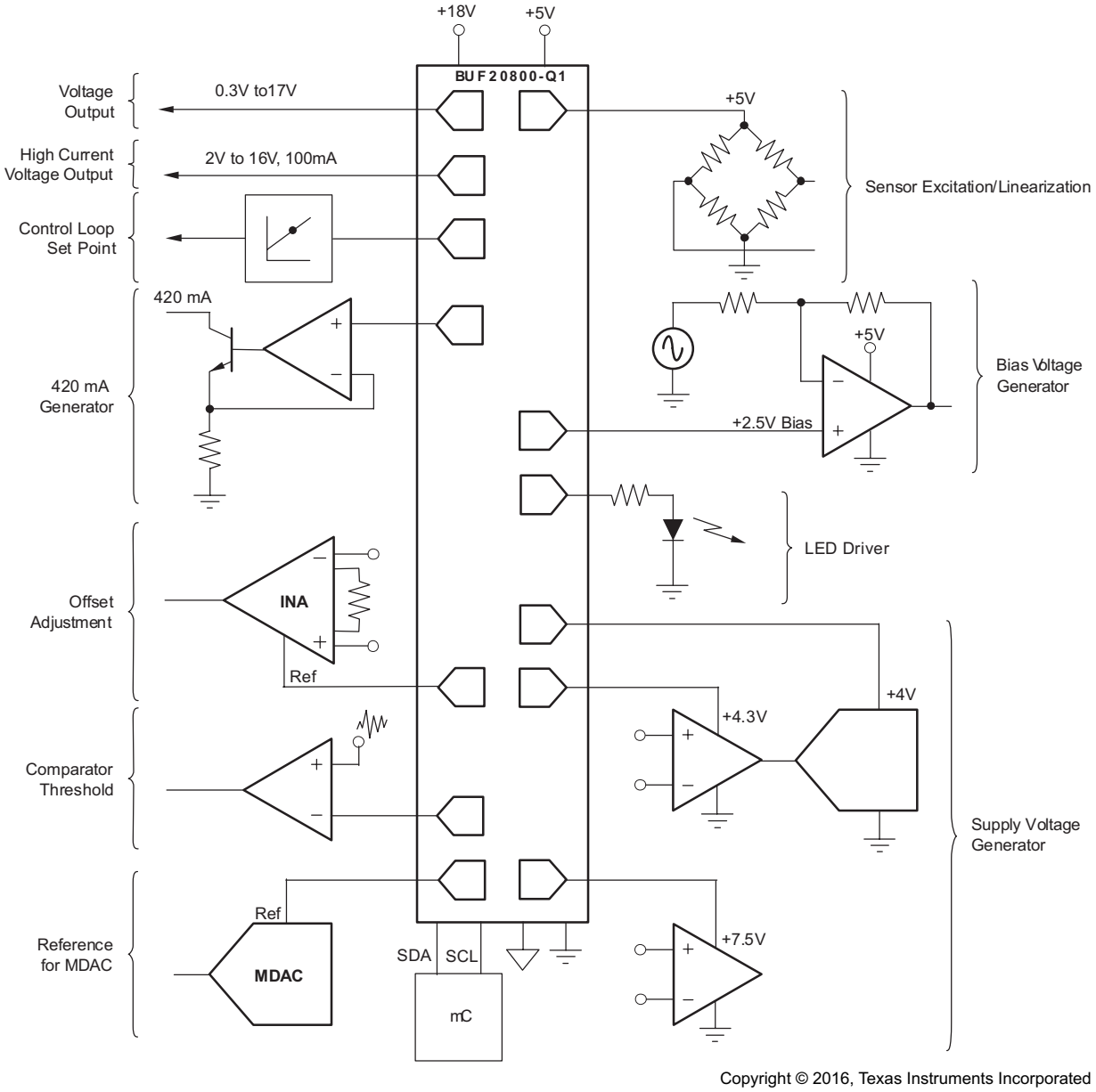


Figure 19. Industrial Applications for the BUF20800-Q1

8.2.7 Total TI Panel Solution

In addition to the BUF20800-Q1 programmable voltage reference, TI offers a complete set of ICs for the LCD panel market, including gamma correction buffers, various power-supply solutions, and audio power solutions. See Figure 20 for the total IC solution from TI.

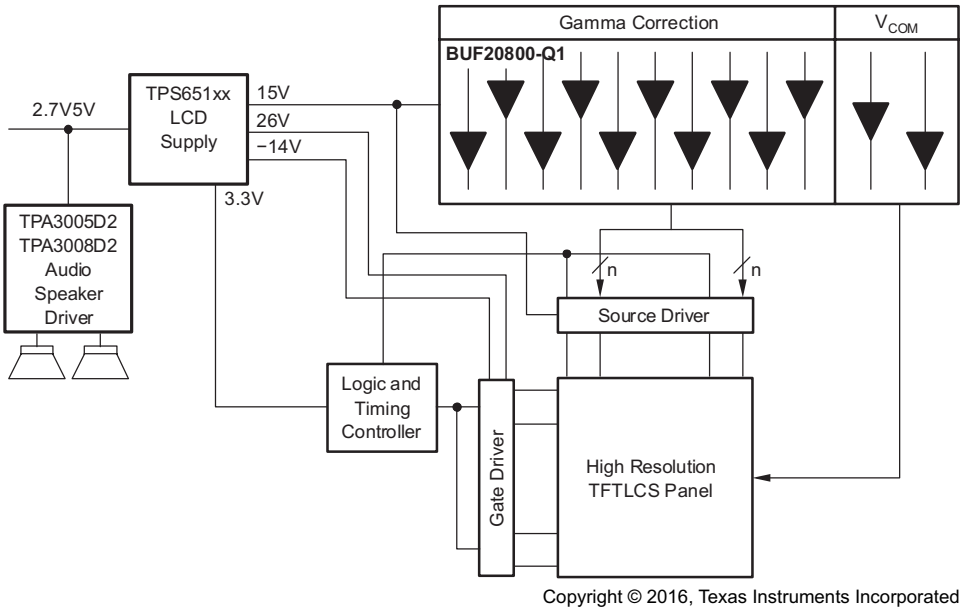


Figure 20. TI LCD Solution

9 Power Supply Recommendations

The device is designed to operate with an analog supply voltage from 7 V to 18 V, and a digital supply from 2 V to 5.5 V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time.
The analog and digital supplies must be well regulated and the input capacitances shown in the application circuit in Figure 14 are recommended for typical applications.

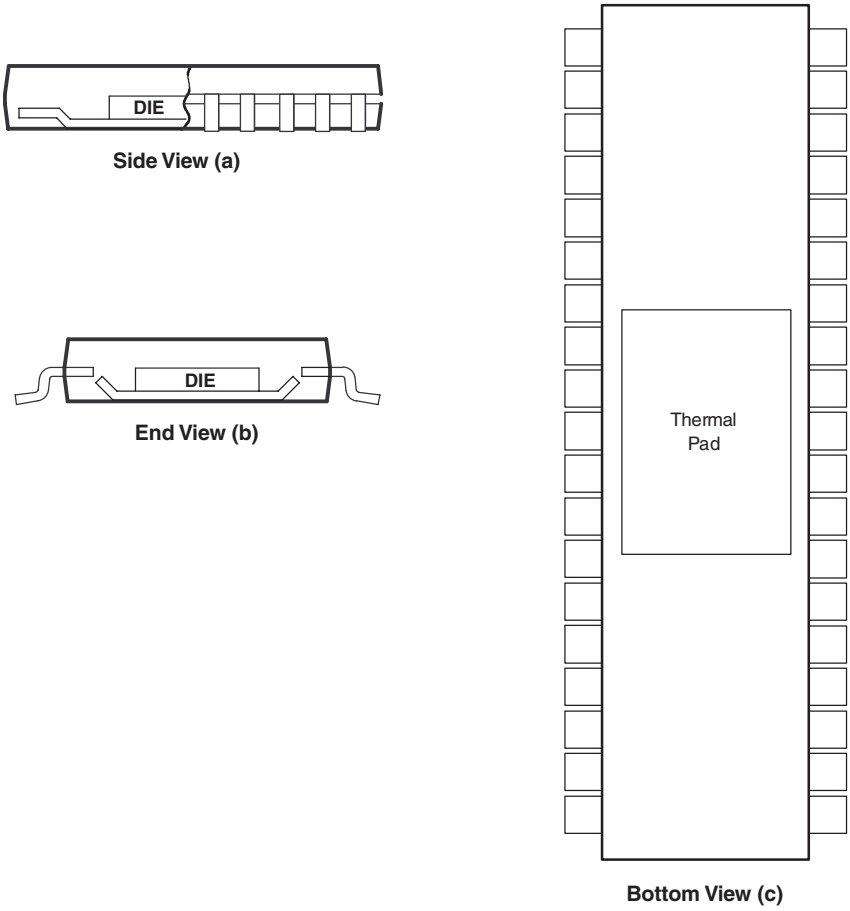
10 Layout

10.1 Layout Guidelines

10.1.1 General PowerPAD Design Considerations

The BUF20800-Q1 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, see Figure 21(a) and Figure 21(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 21(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

Layout Guidelines (continued)



The thermal pad is electrically isolated from all terminals in the package.

Figure 21. Views of Thermally-Enhanced DCP Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. **Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation.** This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the HTSSOP-38 DCP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. An example thermal land pattern mechanical drawing is attached to the end of this data sheet.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF20800-Q1 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.

Layout Guidelines (continued)

5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF20800-Q1 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its twelve holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF20800-Q1 IC is simply placed in position and run through the solder reflow operation as any standard surface mount component. This preparation results in a properly installed part.

For a given θ_{JA} (listed in the Electrical Characteristics table), the maximum power dissipation is shown in Figure 22, and is calculated by Equation 3:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (3)$$

where

- P_D = maximum power dissipation (W)
- T_{MAX} = absolute maximum junction temperature (+125°C)
- T_A = free-ambient air temperature (°C)

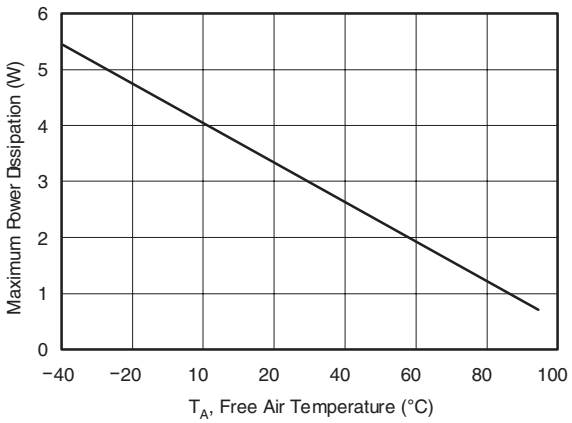


Figure 22. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

10.2 Layout Example

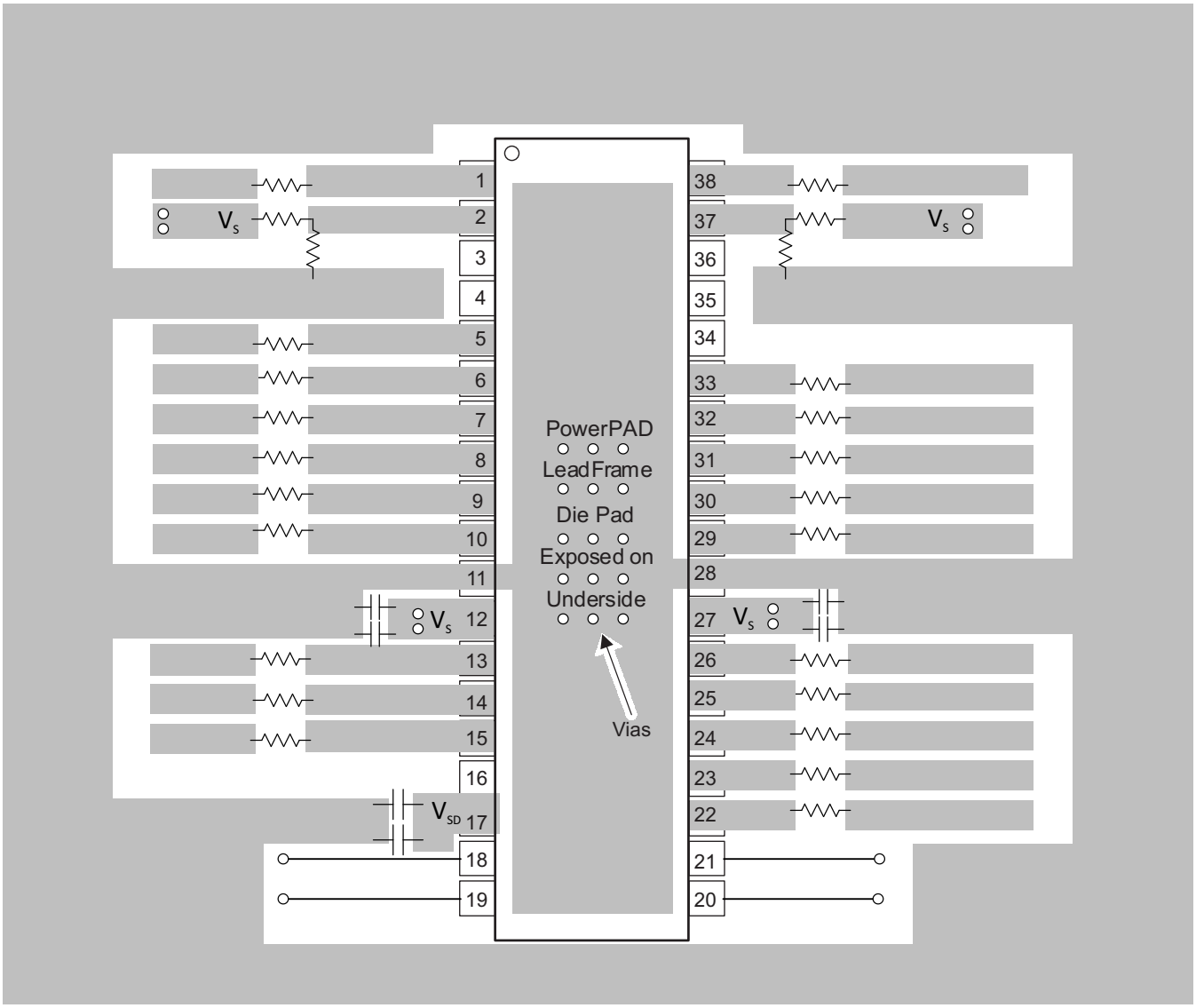


Figure 23. PCB Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『熱特性が強化されたPowerPADパッケージ』、SLMA002
- 『ガンマ・バッファ付きの容量性負荷の駆動』、SBOA134

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

PowerPAD, E2E are trademarks of Texas Instruments.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BUF20800ATDCPRQ1	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	BUF20800Q
BUF20800ATDCPRQ1.A	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	BUF20800Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF BUF20800-Q1 :

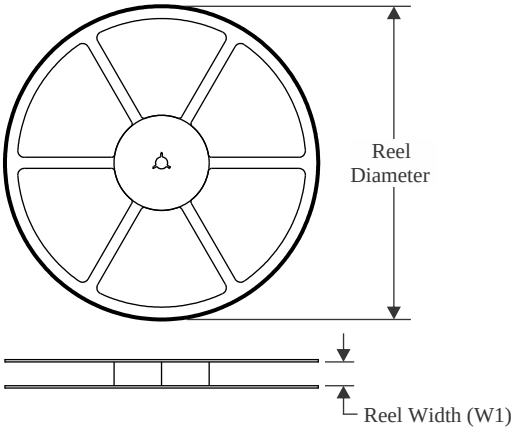
- Catalog : BUF20800

NOTE: Qualified Version Definitions:

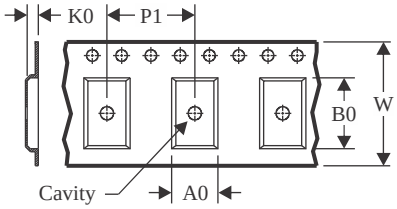
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

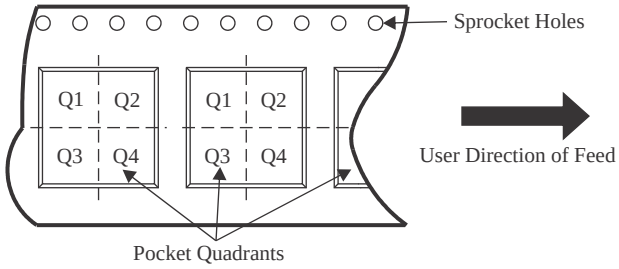


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

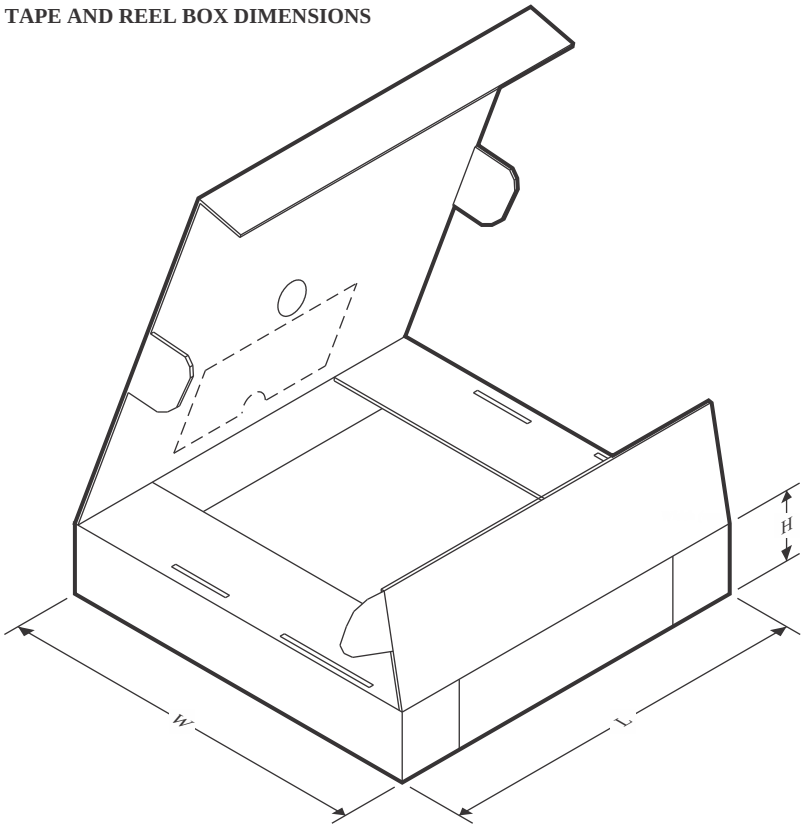
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF20800ATDCPRQ1	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF20800ATDCPRQ1	HTSSOP	DCP	38	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

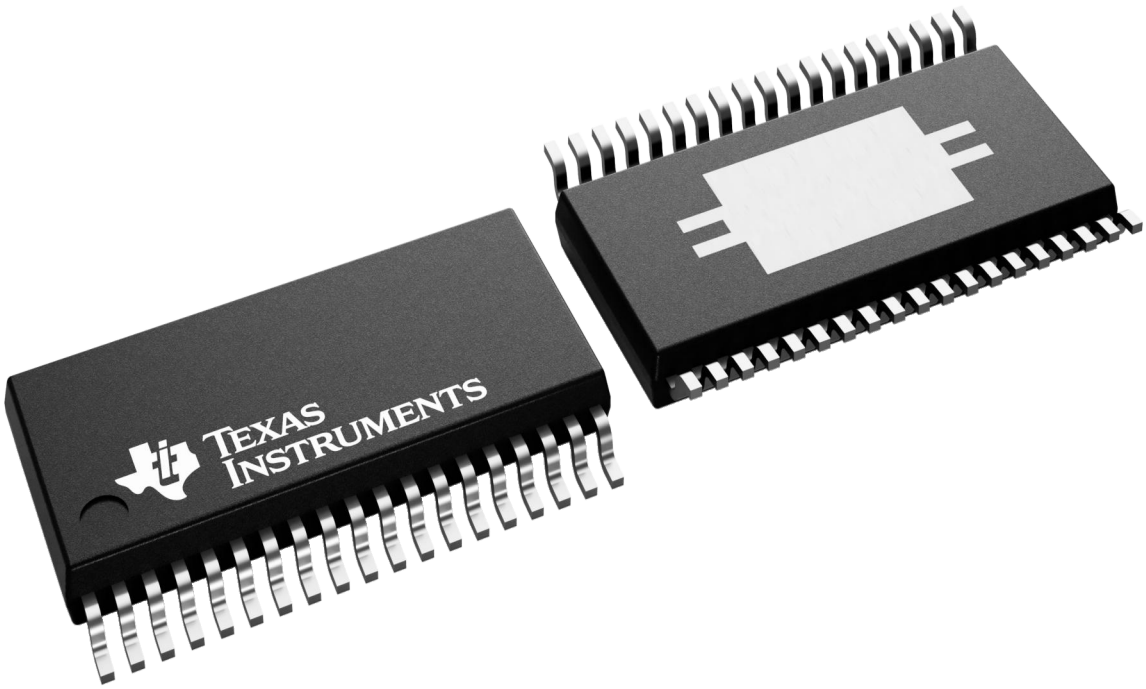
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

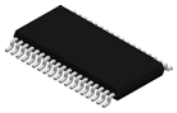
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

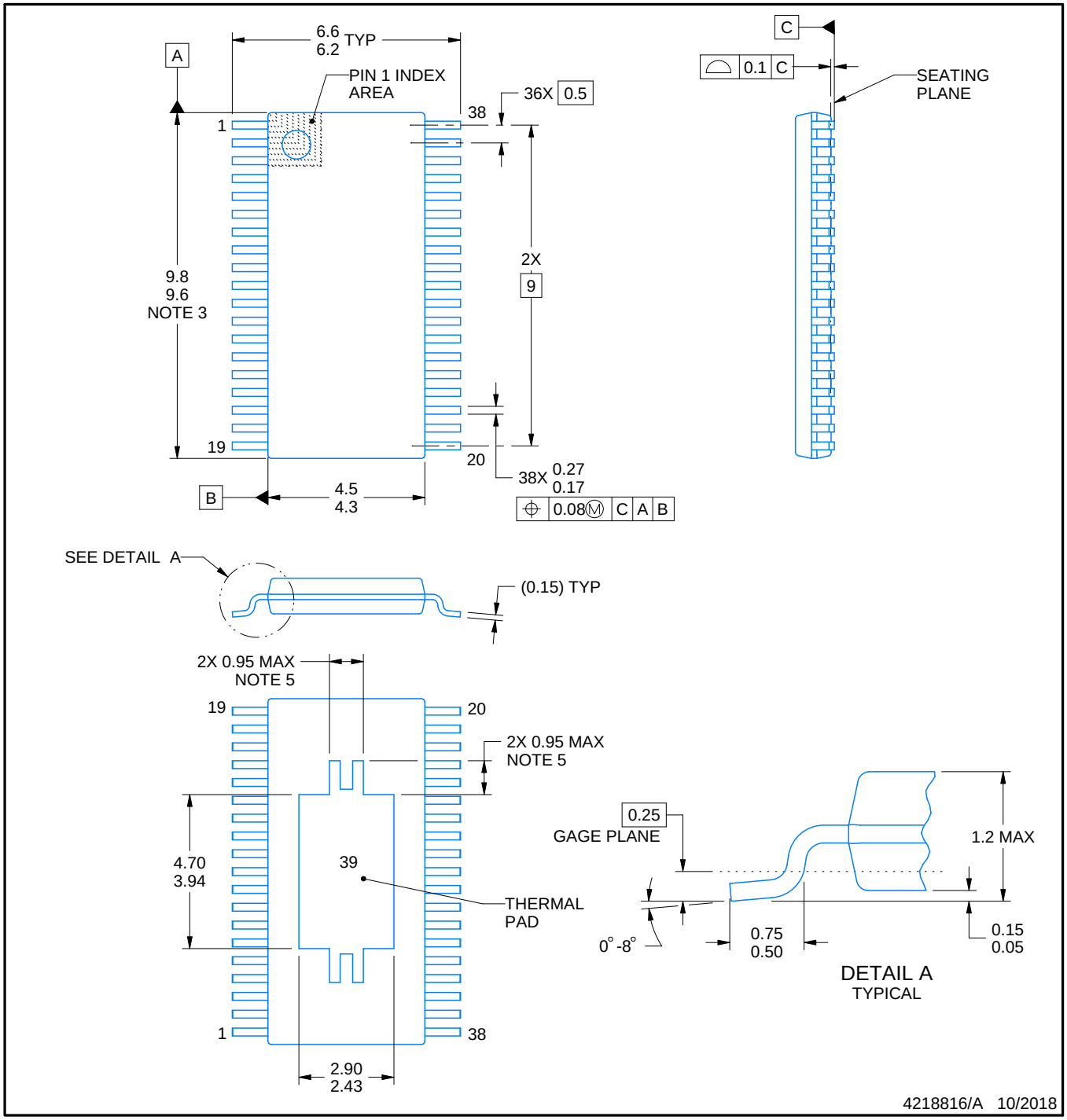
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

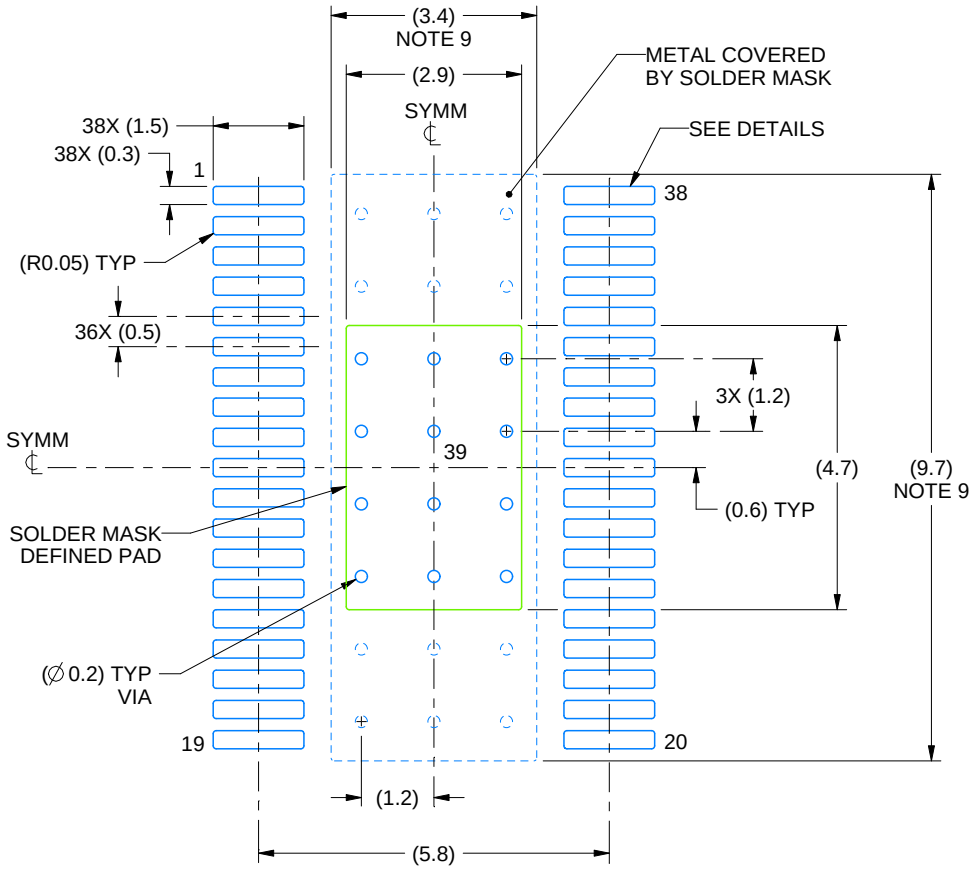
SMALL OUTLINE PACKAGE



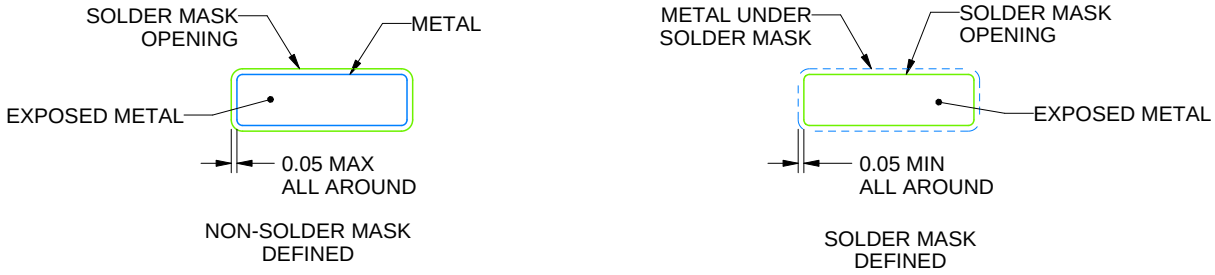
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

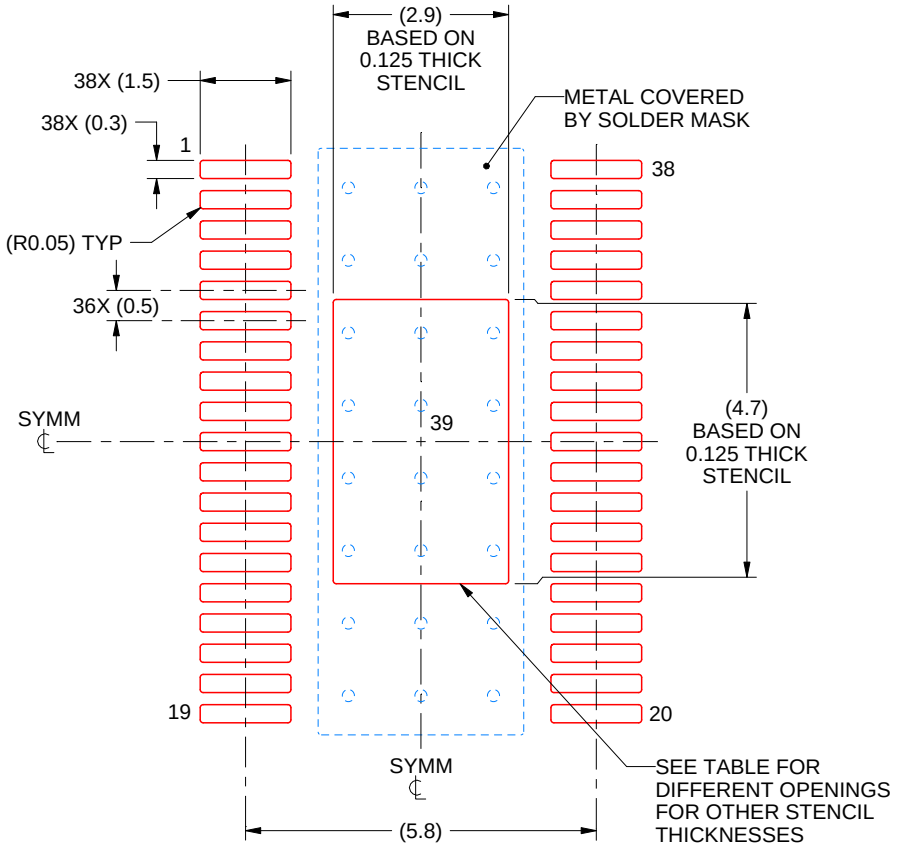


SOLDER MASK DETAILS

4218816/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

4218816/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月