TEXAS INSTRUMENTS
BQ769142
JAJSKT5B – SEPTEMBER 2020 – REVISED JANUARY 2022

BQ769142 3 直列～14 直列リチウムイオン、リチウムポリマ、LiFePO$_4$ バッテリ・パック用高精度バッテリ・モニタおよびプロテクタ

1 特長

- 3 直列～14 直列セルのバッテリ監視が可能
- ハイサイド保護 NFET 用チャージ・ポンプを内蔵 (オプションの自律的回復機能付き)
- 電圧、温度、電流、内部診断を含む包括的な保護スイート
- 2 つの独立した ADC
  - 電流と電圧の同時サンプリングに対応
  - 入力オフセット誤差 1μV 未満 (標準値) の高精度クーロン・カウンタ
  - 高精度のセル電圧測定:誤差 10mV 未満 (標準値)
- 広範囲電流アプリケーション (検出抵抗の両端で ±200mV の測定範囲)
- セカンダリ化学ヒューズ・ドライブ保護を内蔵
- 自律制御またはホスト制御のセル・バランシング
- 複数の電力モード (一般的なバッテリ・パックの動作範囲の条件)
  - 通常モード:286μA
  - 複数のスリープ・モード・オプション:24μA～41μA
  - 複数のディープスリープ・モード・オプション:9μA～10μA
  - シャットダウン・モード:1μA
- 85V の高電圧耐性 (セル接続および他の一部のピン)
- 製造ラインでのランダム・セル取付シーケンスの許容
- 内部センサと最大 9 つの外部サーミスタによる温度センシングをサポート
- 内蔵ワンタイム・プログラマブル (OTP) メモリ、生産ラインで顧客によりプログラム可能
- 400kHz I^{2}C、SPI、HDQ 1 線式インターフェイスを含む通信オプション
- 外部システム用のプログラム可能なデュアル LDO
- 48 ピン TQFP パッケージ (PFB)

2 アプリケーション

- バッテリ・バックアップ・ユニット (BBU)
- 電動自転車 / 電動スクーター / 軽電気自動車 (LEV)
- コードレス電動工具および園芸用具
- 非軍事用ドローン
- その他の産業用バッテリ・パック (10S 以上)

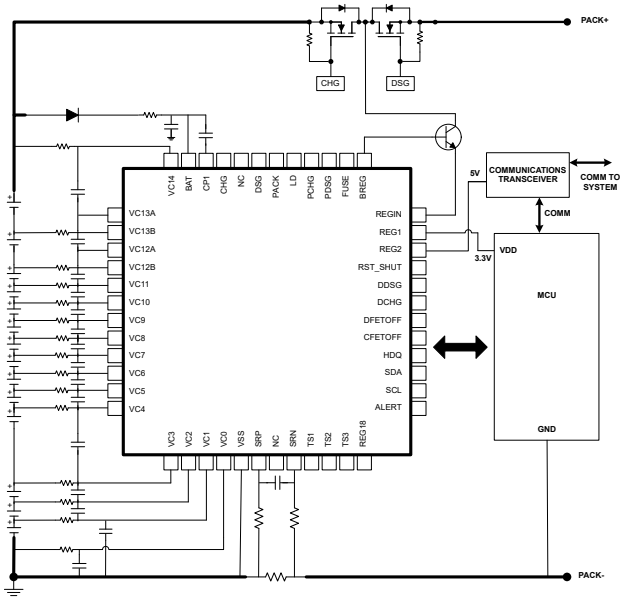
3 概要

テキサス・インスツルメンツの BQ769142 デバイスは、3 直列～14 直列リチウムイオン、リチウムポリマ、LiFePO$_4$ バッテリ・パック用の高集積高精度バッテリ・モニタおよびプロテクタです。このデバイスは高精度の監視システム、高度に構成可能な保護サブシステム、自律制御またはホスト制御のセル・バランシング機能を内蔵しています。ハイサイド・チャージ・ポンプ NFET ドライバ、外部システム用のプログラム可能なデュアル LDO、400kHz I^{2}C、SPI、HDQ 1 線式規格をサポートするホスト通信ペリフェラルも統合されています。BQ769142 デバイスは、48 ピンの TQFP パッケージで供給されます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
BQ769142xx	PFB (48 ピン)	7mm × 7mm

(1) デバイス・ファミリの詳細については、「デバイス比較表」を参照してください。利用可能なデバイスについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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• Updated the *Absolute Maximum Ratings*, *Recommended Operating Conditions*, *ESD Ratings*, and *Analog-to-Digital Converter* tables	7
• Added Cell 1 Voltage Validation During SLEEP Mode	37
• Updated the voltage in General Purpose ADCIN Functionality	38
• Updated the nominal value of VREF1 and the ADC counts calculations based on that value	40
• Updated the simplified schematic. Denoted capacitors on sense resistor inputs to VSS as optional	65
• Updated Documentation Support	80

Changes from Revision * (December 2020) to Revision A (February 2021)	Page
• Updated the short circuit in discharge voltage threshold detection accuracy characteristics in the *Comparator-Based Protection Subsystem* section (page 21) of the *Specifications*	7

5 Device Comparison Table

BQ769142 Device Family			
PART NUMBER	Communications Interface	CRC Enabled	REG1 LDO Default
BQ769142	I^2C	Y	Disabled
BQ769142xx(1)	Contact TI for more information.		

(1) Future options

6 Pin Configuration and Functions

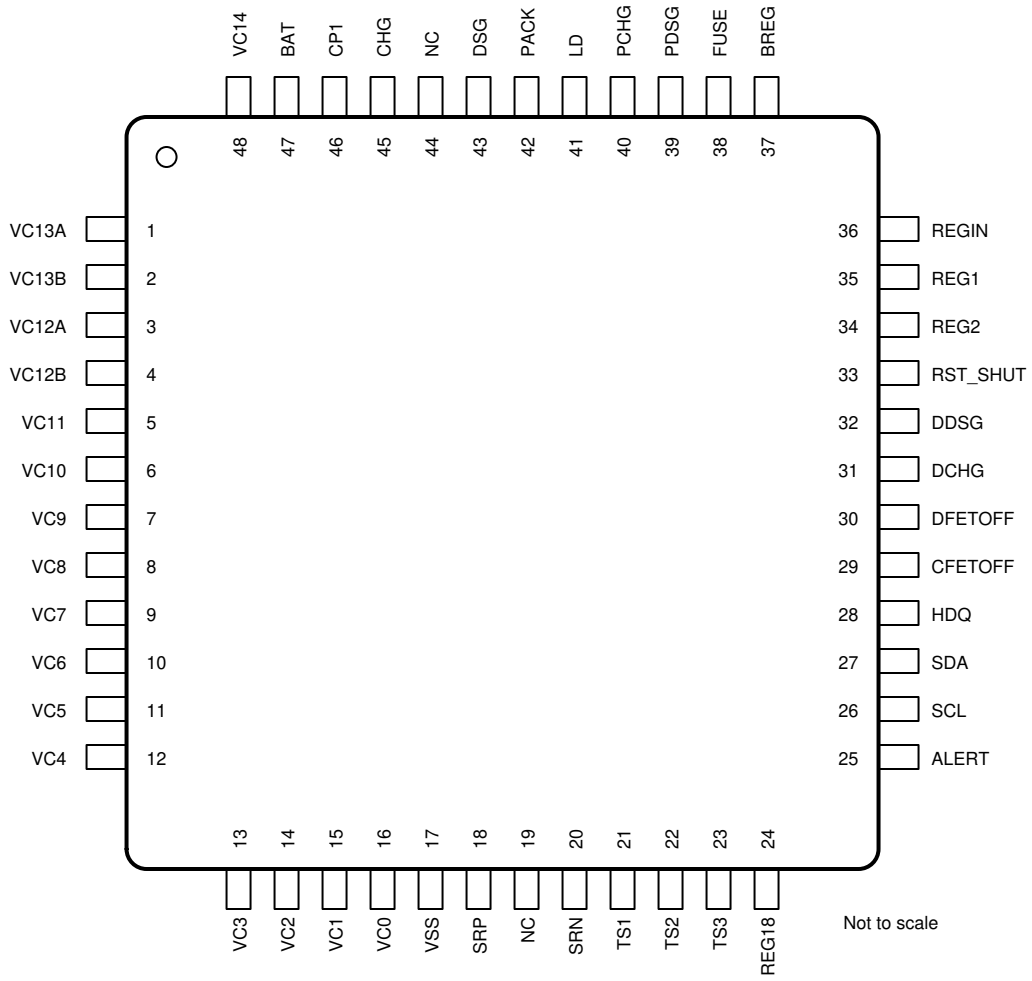


表 6-1. BQ769142 TQFP Package (PFB) Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	VC13A	I	IA	Return balance current for the fourteenth cell from bottom of the stack. This pin should be shorted to VC13B on the PCB.
2	VC13B	I	IA	Sense voltage input pin for the thirteenth cell from the bottom of the stack; balance current input for the thirteenth cell from the bottom of the stack
3	VC12A	I	IA	Return balance current for the thirteenth cell from bottom of stack. This pin should be shorted to VC12B on the PCB.
4	VC12B	I	IA	Sense voltage input pin for the twelfth cell from the bottom of the stack; balance current input for the twelfth cell from the bottom of the stack
5	VC11	I	IA	Sense voltage input pin for the eleventh cell from the bottom of the stack, balance current input for the eleventh cell from the bottom of the stack, and return balance current for the twelfth cell from the bottom of the stack

表 6-1. BQ769142 TQFP Package (PFB) Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
6	VC10	I	IA	Sense voltage input pin for the tenth cell from the bottom of the stack, balance current input for the tenth cell from the bottom of the stack, and return balance current for the eleventh cell from the bottom of the stack
7	VC9	I	IA	Sense voltage input pin for the ninth cell from the bottom of the stack, balance current input for the ninth cell from the bottom of the stack, and return balance current for the tenth cell from the bottom of the stack
8	VC8	I	IA	Sense voltage input pin for the eighth cell from the bottom of the stack, balance current input for the eighth cell from the bottom of the stack, and return balance current for the ninth cell from the bottom of the stack
9	VC7	I	IA	Sense voltage input pin for the seventh cell from the bottom of the stack, balance current input for the seventh cell from the bottom of the stack, and return balance current for the eighth cell from the bottom of the stack
10	VC6	I	IA	Sense voltage input pin for the sixth cell from the bottom of the stack, balance current input for the sixth cell from the bottom of the stack, and return balance current for the seventh cell from the bottom of the stack
11	VC5	I	IA	Sense voltage input pin for the fifth cell from the bottom of the stack, balance current input for the fifth cell from the bottom of the stack, and return balance current for the sixth cell from the bottom of the stack
12	VC4	I	IA	Sense voltage input pin for the fourth cell from the bottom of the stack, balance current input for the fourth cell from the bottom of the stack, and return balance current for the fifth cell from the bottom of the stack
13	VC3	I	IA	Sense voltage input pin for the third cell from the bottom of the stack, balance current input for the third cell from the bottom of the stack, and return balance current for the fourth cell from the bottom of the stack
14	VC2	I	IA	Sense voltage input pin for the second cell from the bottom of the stack, balance current input for the second cell from the bottom of the stack, and return balance current for the third cell from the bottom of the stack
15	VC1	I	IA	Sense voltage input pin for the first cell from the bottom of the stack, balance current input for the first cell from the bottom of the stack, and return balance current for the second cell from the bottom of the stack
16	VC0	I	IA	Sense voltage input pin for the negative terminal of the first cell from the bottom of the stack, and return balance current for the first cell from the bottom of the stack
17	VSS	—	P	Device ground
18	SRP	I	IA	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
19	NC	—	—	This pin is not connected to silicon.
20	SRN	I	IA	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
21	TS1	I/O	OD, I/OA	Thermistor input, or general purpose ADC input
22	TS2	I/O	OD, I/OA	Thermistor input and functions as wakeup from SHUTDOWN, or general purpose ADC input
23	TS3	I/O	OD, I/OA	Thermistor input, or general purpose ADC input
24	REG18	O	P	Internal 1.8-V LDO output (only for internal use)
25	ALERT	I/O	I/OD, I/OA	Multifunction pin, can be ALERT output, or HDQ I/O, or thermistor input, or general purpose ADC input, or general purpose digital output
26	SCL	I/O	I/OD	Multifunction pin, can be SCL or SPI_SCLK
27	SDA	I/O	I/OD	Multifunction pin, can be SDA or SPI_MISO
28	HDQ	I/O	I/OD, I/OA	Multifunction pin, can be HDQ I/O, SPI_MOSI, thermistor input, general purpose ADC input, or general purpose digital output
29	CFETOFF	I/O	I/OD, I/OA	Multifunction pin, can be CFETOFF, SPI_CS, thermistor input, general purpose ADC input, or general purpose digital output

表 6-1. BQ769142 TQFP Package (PFB) Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
30	DFETOFF	I/O	I/OD, I/OA	Multifunction pin, can be DFETOFF, BOTHOFF, thermistor input, general purpose ADC input, or general purpose digital output
31	DCHG	I/O	OD, I/OA	Multifunction pin, can be DCHG, thermistor input, general purpose ADC input, or general purpose digital output
32	DDSG	I/O	OD, I/OA	Multifunction pin, can be DDSG, thermistor input, general purpose ADC input, or general purpose digital output
33	RST_SHUT	I	ID	Digital input pin for reset or shutdown
34	REG2	O	P	Second LDO (REG2) output, which can be programmed for 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V
35	REG1	O	P	First LDO (REG1) output, which can be programmed for 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V
36	REGIN	I	IA	Input pin for REG1 and REG2 LDOs
37	BREG	O	OA	Base control signal for external preregulator transistor
38	FUSE	I/O	I/OA	Fuse sense and drive
39	PDSG	O	OA	Predischarge PFET control
40	PCHG	O	OA	Precharge PFET control
41	LD	I/O	I/OA	Load detect pin
42	PACK	I	IA	Pack sense input pin
43	DSG	O	OA	NMOS Discharge FET drive output pin
44	NC	—	—	This pin is not connected to silicon.
45	CHG	O	OA	NMOS Charge FET drive output pin
46	CP1	I/O	I/OA	Charge pump capacitor
47	BAT	I	P	Primary power supply input pin
48	VC14	I	IA	Sense voltage input pin for the fourteenth cell from the bottom of the stack, balance current input for the fourteenth cell from the bottom of the stack, and top-of-stack measurement point
P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output				

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION	PINS	MIN	MAX	UNIT
Supply voltage range	BAT	VSS–0.3	VSS+85	V
Input voltage range, V_{IN}	PACK, LD	VSS–0.3	VSS+85	V
Input voltage range, V_{IN}	PCHG, PDSG	the maximum of V_{BAT}-10 or V_{LD}-10	VSS+85	V
Input voltage range, V_{IN}	REGIN	the maximum of VSS–0.3 or V_{BREG}-5.5	the minimum of VSS+6 or V_{BAT}+0.3 or V_{BREG}+0.3	V
Input voltage range, V_{IN}	FUSE(2)	VSS–0.3	the minimum of VSS+20 or V_{BAT}+0.3	V
Input voltage range, V_{IN}	BREG	the maximum of VSS–0.3 or V_{REGIN}-0.3	V_{REGIN}+5.5	V
Input voltage range, V_{IN}	REG1, REG2	VSS–0.3	minimum of VSS+6 or V_{REGIN}+0.3	V
Input voltage range, V_{IN}	ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, RST_SHUT (3)	VSS–0.3	VSS+6	V
Input voltage range, V_{IN}	TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, DDSG (when used as thermistor or general purpose ADC input)	VSS–0.3	V_{REG18} + 0.3	V
Input voltage range, V_{IN}	SRP, SRN	VSS–0.3	V_{REG18} + 0.3	V
Input voltage range, V_{IN}	VC14	maximum of VSS-0.3 and VC13A–0.3	VSS+85	V
Input voltage range, V_{IN}	VC13A	maximum of VSS-0.3 and VC13B–0.3	VSS+85	V
Input voltage range, V_{IN}	VC13B	maximum of VSS-0.3 and VC12A–0.3	VSS+85	V
Input voltage range, V_{IN}	VC12A	maximum of VSS-0.3 and VC12B–0.3	VSS+85	V
Input voltage range, V_{IN}	VC12B	maximum of VSS-0.3 and VC11–0.3	VSS+85	V
Input voltage range, V_{IN}	VC11	maximum of VSS-0.3 and VC10–0.3	VSS+85	V
Input voltage range, V_{IN}	VC10	maximum of VSS-0.3 and VC9–0.3	VSS+85	V
Input voltage range, V_{IN}	VC9	maximum of VSS-0.3 and VC8–0.3	VSS+85	V
Input voltage range, V_{IN}	VC8	maximum of VSS-0.3 and VC7–0.3	VSS+85	V

7.1 Absolute Maximum Ratings (continued)

over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION	PINS	MIN	MAX	UNIT
Input voltage range, V_{IN}	VC7	maximum of VSS-0.3 and VC6–0.3	VSS+85	V
Input voltage range, V_{IN}	VC6	maximum of VSS-0.3 and VC5–0.3	VSS+85	V
Input voltage range, V_{IN}	VC5	maximum of VSS-0.3 and VC4–0.3	VSS+85	V
Input voltage range, V_{IN}	VC4	maximum of VSS-0.3 and VC3–0.3	VSS+85	V
Input voltage range, V_{IN}	VC3	maximum of VSS-0.3 and VC2–0.3	VSS+85	V
Input voltage range, V_{IN}	VC2	maximum of VSS-0.3 and VC1–0.3	VSS+85	V
Input voltage range, V_{IN}	VC1	maximum of VSS-0.3 and VC0–0.3	VSS+85	V
Input voltage range, V_{IN}	VC0	VSS–0.3	VSS+6	V
Output voltage range, V_O	CP1	V_{BAT}–0.3	the minimum of VSS+85 or V_{BAT}+15	V
Output voltage range, V_O	CHG	VSS–0.3	VSS+85	V
Output voltage range, V_O	DSG	VSS–0.3	VSS+85	V
Output voltage range, V_O	REG1, REG2, TS2 (for wakeup function), ALERT, CFETOFF, DFETOFF, HDQ, DCHG, DDSG, when configured to drive a digital output	VSS–0.3	VSS+6	V
Output voltage range, V_O	REG18	VSS–0.3	VSS+2	V
Maximum cell balancing current through a single cell	VC0 – VC14		100	mA
Maximum VSS current, I_{SS}			75	mA
Functional temperature, T_{FUNC}		–40	85	°C
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{STG}		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The current allowed to flow into the FUSE pin must be limited (such as by using external series resistance) to 2 mA or less.
(3) When the ALERT, HDQ, CFETOFF, DFETOFF, DCHG, or DDSG pins are selected for thermistor input or general purpose ADC–input, their voltage is limited to V_{REG18} + 0.3 V. These pins can accept up to 6 V when configured for other uses, such as a digital input.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	Supply voltage	Voltage on BAT pin (normal operation)	4.7		80	V
V_{BAT}	Supply voltage(4)	Voltage on BAT pin (OTP programming)	10		12	V
T_{OTP}	OTP programming temperature(4)		-40		45	°C
V_{PORA}	Power-on reset	Rising threshold on BAT	3		4	V
V_{PORA_HYS}	Power-on reset hysteresis	Device shuts down when BAT < V_{PORA} - V_{PORA_HYS}		180		mV
$V_{WAKEONLD}$	Wake on LD voltage	Rising edge on LD, with BAT already in valid range	0.8	1.45	2.25	V
$V_{WAKEONTS2}$	Wake on TS2 voltage	Falling edge on TS2, with BAT already in valid range. TS2 will be weakly driven with a ≈ 5 V level during shutdown.	0.7		1.1	V
V_{IN}	Input voltage range(4)	PACK, LD	0		80	V
V_{IN}	Input voltage range(4)	PCHG, PDSG	the maximum of V_{BAT}-9 or V_{LD}-19		80	V
V_{IN}	Input voltage range(4)	REG1, REG2, RST_SHUT, ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, except when the pin is being used for general purpose ADC input or thermistor measurement.	0		5.5	V
V_{IN}	Input voltage range(4)	TS1, TS2, TS3, CFETOFF, DFETOFF, DCHG, DDSG, ALERT, HDQ, when the pin is configured for general purpose ADC input or thermistor measurement.	0		V_{REG18}	V
V_{IN}	Input voltage range(4)	SRP, SRN, SRP-SRN (while measuring current)	–0.2		0.2	V
V_{IN}	Input voltage range(4)	SRP, SRN (without measuring current)	–0.2		0.75	V
V_{IN}	Input voltage range(4) (5)	$V_{VC(0)}$	–0.2		0.5	V
V_{IN}	Input voltage range(4)	$V_{VC(x)}$, 1 ≤ x ≤ 4	maximum of $V_{VC(x–1)}$ – 0.2 or VSS–0.2		minimum of $V_{VC(x–1)}$+5.5 or VSS+80	V
V_{IN}	Input voltage range(4)	$V_{VC(x)}$, x ≥ 5	maximum of $V_{VC(x–1)}$ – 0.2 or VSS + 2.0		minimum of $V_{VC(x–1)}$ + 5.5 or VSS + 80	V
R_C	External cell input resistance(4) (7)		20		100	Ω
C_C	External cell input capacitance(4) (7)		0.1	0.22	1	µF
V_O	Output voltage range	LD			80	V
V_O	Output voltage range(6)	CHG, DSG, CP1			85	V
T_{OPR}	Operating temperature(6)		–40		85	°C

7.3 Recommended Operating Conditions (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CELL(ACC)}$	Cell voltage measurement accuracy	2 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 5 V, T_A = 25°C, 1 ≤ x ≤ 14(2) (3)	–5		5	mV
$V_{CELL(ACC)}$	Cell voltage measurement accuracy(6)	2 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 5 V, T_A = 0°C to 60°C, 1 ≤ x ≤ 14(2) (3)	–10		10	mV
$V_{CELL(ACC)}$	Cell voltage measurement accuracy(6)	–0.2 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 5.5 V, T_A = -40°C to 85°C, 1 ≤ x ≤ 14(2) (3)	–15		15	mV
$V_{STACK(ACC)}$	Stack voltage (VC14 - VSS) measurement accuracy(6)	0 V < V_{VC14} - V_{VSS} < 80 V, T_A = -40°C to 85°C(2)	–0.5		0.5	V
$V_{PACK(ACC)}$	PACK pin voltage measurement accuracy(6)	0 V < V_{PACK} < 80 V, T_A = -40°C to 85°C(2)	–0.5		0.5	V
$V_{LD(ACC)}$	LD pin voltage measurement accuracy(6)	0 V < V_{LD} < 80 V, T_A = -40°C to 85°C(2)	–0.5		0.5	V

(1) Operation with VBAT up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on VBAT should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Cell voltage accuracy is specified after completion of board offset calibration
(3) While in SLEEP mode, it is important that the cell 1 voltage measurement be validated before being considered valid. For further information and details, see **Cell 1 Voltage Validation during SLEEP Mode**.
(4) Specified by design
(5) Voltage on VC0 can extend higher (limited by absolute maximum specification) during cell balancing.
(6) Specified by characterization
(7) Values may need to be optimized during system design and evaluation for best performance

7.4 Thermal Information BQ769142

THERMAL METRIC(1)		BQ769142 PFB (TQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Supply Current

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{NORMAL}	Normal Mode	Regular measurements and protections active, REG1 = 3.3 V with no load, REG2 = OFF, CHG = ON in 11V overdrive mode, DSG = ON in 11V overdrive mode, **Settings:Configuration:Power Config[FASTADC]** = 0, no communication		286		µA
I_{SLEEP_1}	SLEEP Mode	Periodic protections and monitoring, no pack current, REG1 = OFF, REG2 = OFF, CHG = OFF, DSG = ON in 11V overdrive mode, no communication, **Power:Sleep:Voltage Time** = 5 s		41		µA

7.5 Supply Current (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SLEEP_2}	SLEEP Mode	Periodic protections and monitoring, no pack current, REG1 = OFF, REG2 = OFF, CHG = OFF, DSG = source follower mode, no communication, **Power:Sleep:Voltage Time** = 5 s		24		µA
$I_{DEEPSLEEP\_1}$	DEEPSLEEP Mode	No monitoring or protections, REG1 = 3.3 V with no load, REG2 = OFF, LFO = ON, no communication		10.7		µA
$I_{DEEPSLEEP\_2}$	DEEPSLEEP Mode	No monitoring or protections, REG1 = 3.3 V with no load, REG2 = OFF, LFO = OFF, no communication		9.2		µA
$I_{SHUTDOWN}$	SHUTDOWN Mode	All blocks powered down, with the exception of the TS2 wakeup circuit, no monitoring or protections, no communication		1	3.1	µA

(1) Operation with VBAT up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on VBAT should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.

7.6 Digital I/O

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input	ALERT (configured as HDQ), SCL, SDA, HDQ, CFETOFF, DFETOFF, RST_SHUT	0.66 x V_{REG18}		5.5	V
V_{IL}	Low-level input	ALERT (configured as HDQ), SCL, SDA, HDQ, CFETOFF, DFETOFF, RST_SHUT			0.33 x V_{REG18}	V
V_{OH}	Output voltage high, TS2	TS2 during SHUTDOWN mode, V_{BAT} > 6 V	4.5		6	V
V_{OH}	Output voltage high, TS2 low voltage	TS2 during SHUTDOWN mode, 4.7 V ≤ V_{BAT} ≤ 6 V	3		6	V
V_{OH}	Output voltage high, 5 V case	ALERT, SDA (configured as SPI_MISO), SCL (configured as SPI_SCLK), CFETOFF (configured as GPO), DFETOFF (configured as GPO), DCHG, DDSG, pins driving from REG1, V_{REG1} set to 5 V nominal setting, V_{BAT} > 8 V, I_{OH} = -5.0 mA, 10 pF load	0.9 x V_{REG1}		V_{REG1}	V
V_{OL}	Output voltage low, 5 V case	ALERT, SCL, SDA, HDQ, DCHG, DDSG, CFETOFF (configured as GPO), DFETOFF (configured as GPO), pins driving from REG1, V_{REG1} set to 5 V nominal setting, V_{BAT} > 8 V, I_{OL} = 5 mA, 10 pF load			0.77	V
R_{OH}	Output weak high resistance	TS2 during SHUTDOWN mode		4600		kΩ
C_{IN}	Input capacitance(2)	ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, REGIN, TS1, TS2, TS3		2		pF
I_{LKG}	Input leakage current	ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, REGIN, device in SHUTDOWN mode			1	µA

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.

(2) Specified by design

7.7 LD Pin

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(PULLUP)}$	Internal pullup current from BAT pin to LD pin, used for load detect functionality	V_{BAT} ≥ 4.7 V, V_{LD} = VSS	35	100	172	µA
R_{PD}	Internal pulldown resistance on LD pin in SHUTDOWN mode	V_{BAT} ≥ 4.7 V		80		kΩ

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.

7.8 Precharge (PCHG) and Predischarge (PDSG) FET Drive

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PCHG\_ON)}$	Output voltage, PCHG on	max(V_{PACK}, V_{BAT}) - V_{PCHG}, V_{PACK} ≥ 8 V, V_{BAT} ≥ 4.7 V	7.5	8.4	9.7	V
$V_{(PCHG\_ON)}$	Output voltage, PCHG on	V_{PACK} - V_{PCHG}, 4.7 V ≤ V_{PACK} < 8 V, V_{BAT} ≥ 4.7 V, V_{PACK} > V_{BAT}	V_{PACK} – 0.5 V		V_{PACK}	V
$V_{(PDSG\_ON)}$	Output voltage, PDSG on	max(V_{LD}, V_{BAT}) - V_{PDSG}, V_{BAT} ≥ 8 V	7.47	8.4	9.7	V
$V_{(PDSG\_ON)}$	Output voltage, PDSG on	V_{BAT} - V_{PDSG}, 4.7 V ≤ V_{BAT} < 8 V, V_{BAT} ≥ V_{LD}	V_{BAT} – 0.5 V		V_{BAT}	V
$I_{(PULLDOWN)}$	Current sink capability, PCHG and PDSG	PCHG and PDSG enabled, V_{BAT} = 59.2 V		30		µA

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.

7.9 FUSE Pin Functionality

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OH)}$	Output voltage high (when driving fuse)	V_{BAT} ≥ 8 V, C_L = 1 nF, 5 kΩ load.	6	7	9	V
$V_{(OH)}$	Output voltage high (when driving fuse)	4.7 V ≤ V_{BAT} < 8 V, C_L = 1 nF, 5 kΩ load.	V_{BAT} – 1.75			V
$V_{(IH)}$	High-level input (for fuse detection)	Current into device pin must be limited to maximum 2 mA	2		12	V
$V_{(IL)}$	Low-level input (for fuse detection)				0.7	V
$t_{(RISE)}$	Output rise time (when driving fuse)	V_{BAT} ≥ 8 V, C_L = 1 nF, R_{LOAD} = 5 kΩ, $V_{(OH)}$ = 10% to 90% of final settled voltage		0.5		µs

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.

7.10 REG18 LDO

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{REG18}	External capacitor, REG18 to VSS(2)		1.8	2.2	22	µF

7.10 REG18 LDO (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG18}	Regulator voltage		1.6	1.8	2	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	ΔV_{REG18} vs (V_{REG18} at 25°C), I_{REG18} = 1 mA, V_{BAT} = 55 V		±0.15		%
$\Delta V_{O(LINE)}$	Line regulation	ΔV_{REG18} vs (V_{REG18} at 25°C, V_{BAT} = 55 V), I_{REG18} = 1 mA, as V_{BAT} varies across specified range	–0.6		0.5	%
$\Delta V_{O(LOAD)}$	Load regulation	ΔV_{REG18} vs (V_{REG18}, V_{BAT} = 55 V), I_{REG18} = 0 mA to 1 mA, at 25°C	–1.5		1.5	%
I_{SC}	Regulator short-circuit current limit	V_{REG18} = 0 V	3		14	mA

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design

7.11 REG0 Pre-regulator

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BREG_HDRM}	Pre-regulator control voltage headroom (min(V_{BAT} - V_{BREG}))(4)	V_{BAT} ≥ 4.7 V		1.5	1.91	V
V_{REGIN_INT}	Pre-regulator voltage, when generated using BREG	V_{BAT} > 8 V, although specific requirement depends on external device selected	5	5.5	5.8	V
V_{REGIN_EXT}	Pre-regulator voltage when using externally supplied REGIN(4)	See requirements based on settings of REG1 and REG2			5.5	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	ΔV_{REGIN} vs V_{REGIN} at 25°C, I_{REGIN} = 50 mA, V_{BAT} > 8 V		±0.05		%
I_{Max}	Maximum current driven out from BREG(4)	Under short circuit conditions (V_{REGIN} = 0 V)	2.5	3.33		mA
C_{EXT}	External capacitor REGIN to VSS(3) (4)		15	22	27	nF
C_{BREG}	External capacitor BREG to VSS(4)				150	pF

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Supported output current is limited for V_{STACK} < 5.5 V. V_{REGIN} limited to ~2.5 V below V_{BAT}.
(3) Capacitance should be above 7 nF after consideration for aging and derating.
(4) Specified by design

7.12 REG1 LDO

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG1\_1.8}$	Regulator voltage (nominal 1.8V setting)	V_{REGIN} ≥ 3.0 V, I_{REG1} = 0 mA to 45 mA	1.6	1.84	2	V
$V_{REG1\_2.5}$	Regulator voltage (nominal 2.5V setting)	V_{REGIN} ≥ 3.5 V, I_{REG1} = 0 mA to 45 mA	2.25	2.55	2.75	V
$V_{REG1\_3.0}$	Regulator voltage (nominal 3.0V setting)	V_{REGIN} ≥ 3.8 V, I_{REG1} = 0 mA to 45 mA	2.7	3.05	3.3	V
$V_{REG1\_3.3}$	Regulator voltage (nominal 3.3V setting)	V_{REGIN} ≥ 4.1 V, I_{REG1} = 0 mA to 45 mA	3	3.36	3.6	V
$V_{REG1\_5.0}$	Regulator voltage (nominal 5.0V setting)	V_{REGIN} ≥ 5.0 V, I_{REG1} = 0 mA to 45 mA	4.5	5.19	5.5	V

7.12 REG1 LDO (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{O(TEMP)}$	Regulator output over temperature	ΔV_{REG1} vs (V_{REG1} at 25°C, I_{REG1} = 20 mA, V_{REGIN} = 5.5 V, V_{REG1} set to nominal 3.3 V setting)		±0.25		%
$\Delta V_{O(LINE)}$	Line regulation	ΔV_{REG1} vs (V_{REG1} at 25°C, V_{REGIN} = 5.5 V, I_{REG1} = 20 mA), as V_{REGIN} varies from 5 V to 6 V, V_{REG1} set to nominal 3.3 V setting	–1		1	%
I_{SC}	Regulator short-circuit current limit	V_{REG1} = 0 V	47		80	mA
C_{EXT}	External capacitor REG1 to VSS(2)		1			µF

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design

7.13 REG2 LDO

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG2\_1.8}$	Regulator voltage (nominal 1.8V setting)	V_{REGIN} ≥ 3.0 V, I_{REG2} = 0 mA to 45 mA	1.6	1.84	2	V
$V_{REG2\_2.5}$	Regulator voltage (nominal 2.5V setting)	V_{REGIN} ≥ 3.5 V, I_{REG2} = 0 mA to 45 mA	2.25	2.55	2.75	V
$V_{REG2\_3.0}$	Regulator voltage (nominal 3.0V setting)	V_{REGIN} ≥ 3.8 V, I_{REG2} = 0 mA to 45 mA	2.7	3.06	3.3	V
$V_{REG2\_3.3}$	Regulator voltage (nominal 3.3V setting)	V_{REGIN} ≥ 4.1 V, I_{REG2} = 0 mA to 45 mA	3.0	3.38	3.6	V
$V_{REG2\_5.0}$	Regulator voltage (nominal 5.0V setting)	V_{REGIN} ≥ 5.0 V, I_{REG2} = 0 mA to 45 mA	4.5	5.23	5.5	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	ΔV_{REG2} vs (V_{REG2} at 25°C, I_{REG2} = 20 mA, V_{REGIN} = 5.5 V, V_{REG2} set to nominal 3.3 V setting)		±0.25		%
$\Delta V_{O(LINE)}$	Line regulation	ΔV_{REG2} vs (V_{REG2} at 25°C, V_{REGIN} = 5.5 V, I_{REG2} = 20 mA), as V_{REGIN} varies from 5 V to 6 V, V_{REG2} set to nominal 3.3 V setting	–1		1	%
I_{SC}	Regulator short-circuit current limit	V_{REG2} = 0 V	47		80	mA
C_{EXT}	External capacitor REG2 to VSS(2)		1			µF

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design

7.14 Voltage References

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE 1						
$V_{(REF1)}$	Internal reference voltage (2)	T_A = 25°C	1.210	1.212	1.214	V
$V_{(REF1DRIFT)}$	Internal reference voltage drift (2) (4)	T_A = -10°C to 60°C		±10		PPM/°C
$V_{(REF1DRIFT)}$	Internal reference voltage drift (2) (4)	T_A = -40°C to 85°C		±10		PPM/°C
VOLTAGE REFERENCE 2						
$V_{(REF2)}$	Internal reference voltage (3)	T_A = 25°C	1.23	1.24	1.25	V
$V_{(REF2DRIFT)}$	Internal reference voltage drift(3) (4)	T_A = -10°C to 60°C		±20		PPM/°C

7.14 Voltage References (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(REF2DRIFT)}$	Internal reference voltage drift(3) (4)	T_A = -40°C to 85°C		±50		PPM/°C

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) $V_{(REF1)}$ is used for the ADC reference. Its effective value is determined through indirect measurement using the ADC and measuring the differential voltage on VC1 - VC0.
(3) $V_{(REF2)}$ is used for the LDO, coulomb counter, and current measurement
(4) Specified by characterization

7.15 Coulomb Counter

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(CC\_IN)}$	Input voltage range for measurements(4)	V_{SRP} - V_{SRN}	–0.2		0.2	V
$V_{(CC\_IN)}$	Input voltage range for measurements(4)	V_{SRP}, V_{SRN}	–0.2		0.2	V
$B_{(CC\_INL)}$	Integral nonlinearity(3)	16-bit, best fit over input voltage range, using 0 V common mode voltage.		±5.2	±22.3	LSB(2)
$B_{(CC\_DNL)}$	Differential nonlinearity	16-bit, no missing codes		±0.1		LSB(2)
$V_{(CC\_OFF)}$	Offset error(3)	16-bit, uncalibrated	-1		1	LSB(2)
$V_{(CC\_OFF\_DRIFT)}$	Offset error drift(3)	16-bit, post-calibration	–0.03		0.03	LSB/°C(2)
$B_{(CC\_GAIN)}$	Gain(3)	16-bit, over ideal input voltage range	130845	131454	132335	LSB/V(2)
$R_{(CC\_IN)}$	Effective input resistance(4)			2		MΩ

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) 1 LSB (16-bit mode, using CC1 filter) = V_{REF2} / (5 x 2^{N-1}) ≈ 1.24 / (5 x 2^{15}) = 7.6µV
(3) Specified by characterization
(4) Specified by design

7.16 Coulomb Counter Digital Filter (CC1)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CC1\_CONV\_FAST)}$	Conversion-time	Single conversion (when operating from LFO in 262.144kHz mode)		250		ms
$t_{(CC1\_CONV\_SLOW)}$	Conversion-time	Single conversion (when operating from LFO in 32.768kHz mode)		4		s
$B_{(CC1\_RSL)}$	Code stability(2) (3)	Single conversion	14.3			bits

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Code stability is defined as the resolution such that the data exhibits 3-sigma variation within ±1-LSB.
(3) Specified by a combination of design and production test

7.17 Current Measurement Digital Filter (CC2)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CC2\_CONV)}$	Conversion-time	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 0		2.93		ms
$t_{(CC2\_CONV\_FAST)}$	Conversion-time in fast mode	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 1		1.46		ms
$B_{(CC2\_RES)}$	Code stability(2) (3)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 0	14	15		bits
$B_{(CC2\_RES\_FAST)}$	Code stability in fast mode(2)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 1		13.5		bits

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Code stability is defined as the resolution such that the data exhibits 3-sigma variation within ±1-LSB.
(3) Specified by characterization

7.18 Current Wake Detector

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE_THR}	Wakeup voltage threshold error(2)	T_A = 25°C, V_{WAKE} = V_{SRP} – V_{SRN}, setting between ±0.5 mV and ±5 mV. Measured using averaged data to remove effects of noise.	-200		200	µV
V_{WAKE_THR}	Wakeup voltage threshold error(2)	T_A = 25°C, V_{WAKE} = V_{SRP} – V_{SRN}, setting beyond ±5 mV. Measured using averaged data to remove effects of noise.	-5		5	% of setting
t_{WAKE}	Measurement interval(2)			12		ms

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design

7.19 Analog-to-Digital Converter

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(ADC\_IN\_CELLS)}$	Input voltage range (differential cell input mode)(5)	Internal reference (Vref = V_{REF1})	–0.2		5.5	V
$V_{(ADC\_IN)}$	Input voltage range (ADCIN measurement mode)(6)	Internal reference (Vref = V_{REF1}), applicable to ADCIN measurements using the TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins	–0.2		V_{REG18}	V
$V_{(ADC\_IN\_TS)}$	Input voltage range (external thermistor measurement mode)(7)	Regulator reference (Vref = V_{REG18}), applicable to external thermistor measurements using the TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins	–0.2		V_{REG18}	V

7.19 Analog-to-Digital Converter (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(ADC\_IN\_DIV)}$	Input voltage range (divider measurement mode)(8)	Internal reference (Vref = V_{REF1}), applicable to divider measurements using the VC14, PACK, and LD pins relative to VSS.	–0.2		80	V
$B_{(ADC\_INL)}$	Integral nonlinearity (when using V_{REF1} and differential cell voltage measurement mode at VC14 - VC13A)(4)	16-bit, best fit over -0.1 V to 5.5 V	–6.6		6.6	LSB(5)
		16-bit, best fit over -0.2 V to 0.2 V	–4		4	LSB(5)
$B_{(ADC\_DNL)}$	Differential nonlinearity	16-bit, no missing codes, using differential cell voltage measurement at VC14-VC13A		±0.12		LSB(5)
$B_{(ADC\_OFF\_CELL)}$	Differential cell offset error	16-bit, uncalibrated, using VC14 - VC13A	–2.75		3.5	LSB(5)
$B_{(ADC\_OFF)}$	ADCIN offset error	16-bit, uncalibrated, using ADCIN mode on TS1 pin		0.53		LSB(6)
$B_{(ADC\_OFF\_DIV)}$	Divider offset error	16-bit, uncalibrated, using divider mode on PACK pin		0.17		LSB(8)
$B_{(ADC\_OFF\_DRIFT\_CELL)}$	Differential cell offset error drift(4)	Offset error measured 16-bit, post calibration, using VC14 - VC13A. Drift measured as change in offset over operating temperature range as compared to offset at 30°C.		0.004	0.07	LSB/°C(5)
$B_{(ADC\_GAIN)}$	Gain	Gain measured 16-bit, over ideal input voltage range, differential cell input mode on VC14-VC13A, uncalibrated.	5385	5406	5427	LSB/V(5)
$B_{(ADC\_GAIN\_DRIFT)}$	Gain drift(4)	Gain measured 16-bit, over ideal input voltage range, differential cell input mode on VC14-VC13A, uncalibrated. Drift value measured as change in gain over operating temperature range, compared to gain at 30°C.	-0.25	0.025	0.25	LSB/V/°C(5)
$R_{(ADC\_IN\_CELL)}$	Effective input resistance(3)	Differential cell input mode on VC14-VC13A(9)	2.1			MΩ
$R_{(ADC\_IN\_LD)}$	Effective input resistance	Divider measurement on LD pin (only active while the LD pin is being measured)		2		MΩ
$R_{(ADC\_IN\_DIV)}$	Effective input resistance	Divider measurement on VC14 and PACK pins (only active while the pin is being measured)		600		kΩ
$B_{(ADC\_RES)}$	Code stability(2) (4)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 0	13.5	15		bits
$B_{(ADC\_RES\_FAST)}$	Code stability in fast mode(2)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 1		14		bits
$t_{(ADC\_CONV)}$	Conversion-time	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 0		2.93		ms
$t_{(ADC\_CONV\_FAST)}$	Conversion-time in fast mode	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[FASTADC]** = 1		1.46		ms

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Code stability is defined as the resolution such that the data exhibits 3-sigma variation within ±1-LSB.
(3) Specified by design
(4) Specified by characterization

(5) The 16-bit LSB size of the differential cell voltage measurement is given by 1 LSB = 5 x V_{REF1} / 2^{N-1} ≈ 5 x 1.212 V / 2^{15} = 185 µV
(6) The 16-bit LSB size of the ADCIN voltage measurement is given by 1 LSB = 5 / 3 x V_{REF1} / 2^{N-1} ≈ 5 / 3 x 1.212 V / 2^{15} = 62 µV
(7) The LSB size of the external thermistor voltage measurement when reported in 32-bit format is given by 1 LSB = 5 / 3 x V_{REG18} / 2^{N-1} ≈ 5 / 3 x 1.8 V / 2^{23} = 358 nV
(8) The 16-bit LSB size of the divider voltage measurement is given by 1 LSB = 425 / 3 x V_{REF1} / 2^{N-1} ≈ 425 / 3 x 1.212 / 2^{15} = 5.24 mV
(9) Average effective differential input resistance with device operating in NORMAL mode, cell balancing disabled, three or more thermistors in use, and a 5 V differential voltage applied.

7.20 Cell Balancing

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(CB)}$	Internal cell balancing resistance(2)	$R_{DS(ON)}$ for internal FET switch at $V_{VC(n)}$ - $V_{VC(n-1)}$ = 1.5V, 1 ≤ n ≤ 14, V_{BAT} ≥ 4.7 V	15	28	46	Ω

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Cell balancing must be controlled to limit the current based on the absolute maximum allowed current, and to avoid exceeding the recommended device operating temperature. This can be accomplished by appropriate sizing of the offchip cell input resistors and limiting the number of cells that can be balanced simultaneously.

7.21 Cell Open Wire Detector

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(OW)}$	Internal cell open wire check current from VCx pin to VSS, 1 ≤ x ≤ 14	VCx > VSS + 0.8 V, 1 ≤ x ≤ 4; VCx > VSS + 2.8 V, 5 ≤ x ≤ 14	22	54	95	µA

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.

7.22 Internal Temperature Sensor

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Internal temperature sensor voltage drift	ΔV_{BE} measurement		0.410		mV/°C

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.

7.23 Thermistor Measurement

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(TS\_PU)}$	Internal pullup resistance(2)	Setting for nominal 18-kΩ	14.4	18.3	21.6	kΩ
		Setting for nominal 180-kΩ	140	178	216	kΩ
$R_{(TS\_PAD)}$	Internal pad resistance(3)			526		Ω

7.23 Thermistor Measurement (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(TS\_PU\_DRIFT)}$	Internal pullup resistance change over temperature	Change over -40°C/+85°C vs value at 25°C for nominal 18-kΩ		±200		Ω
		Change over -40°C/+85°C vs value at 25°C for nominal 180-kΩ		±2000		Ω

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) The internal pullup resistance includes only the resistance between the REG18 pin and the point where the voltage is sensed by the ADC.
(3) The internal pad resistance includes the resistance between the point where the voltage is sensed by the ADC and the pin where an external thermistor is attached (which includes the TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins)

7.24 Internal Oscillators

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-frequency Oscillator						
f_{HFO}	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error(3)	T_A = -40°C to +85°C, includes frequency drift	–4.0	±0.25	4.0	%
$f_{HFO(SU)}$	Start-up time(2)	T_A = -40°C to +85°C, at power-up from SHUTDOWN or exiting DEEPSLEEP mode, oscillator frequency within ±3% of nominal			4.3	ms
		T_A = -40°C to +85°C, cases other than power-up from SHUTDOWN or exiting DEEPSLEEP mode, oscillator frequency within ±3% of nominal			135	µs
Low-frequency Oscillator						
f_{LFO}	Operating frequency	Full-speed setting		262.144		kHz
		Low speed setting		32.768		kHz
$f_{LFO(ERR)}$	Frequency error(3)	Full-speed setting, T_A = -10°C to +60°C, includes frequency drift	–1.5	±0.25	1.5	%
		Full-speed setting, T_A = -40°C to +85°C, includes frequency drift	–2.5	±0.25	2.5	%
$f_{LFO(FAIL)}$	Failure detection frequency	Detects oscillator failure if the LFO frequency falls below this level.	8.5	12	18	kHz

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design
(3) Specified by a combination of design and production test

7.25 High-side NFET Drivers

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON\_HI)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to BAT, 8 V ≤ V_{BAT} ≤ 80 V, V_{LD} ≤ V_{DSG} (2)	CHG/DSG C_L = 20 nF, charge pump high overdrive setting	10	11	13	V
$V_{(FETON\_HI\_LOBAT)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to BAT, 4.7 V ≤ V_{BAT} < 8 V, V_{LD} ≤ V_{DSG} (2)	CHG/DSG C_L = 20 nF, charge pump high overdrive setting	8	11	13	V
$V_{(FETON\_LO)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to BAT, 8 V ≤ V_{BAT} ≤ 80 V, V_{LD} ≤ V_{DSG} (2)	CHG/DSG C_L = 20 nF, charge pump low overdrive setting	4.5	5.7	7	V
$V_{(FETON\_LO\_LOBAT)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to BAT, 4.7 V ≤ V_{BAT} < 8 V, V_{LD} ≤ V_{DSG} (2)	CHG/DSG C_L = 20 nF, charge pump low overdrive setting	3.5	5	7	V
$V_{(SRCFOL\_FETON)}$	DSG on voltage with respect to BAT	CHG/DSG C_L = 20 nF, source follower mode		0		V
$V_{(CHGFETOFF)}$	CHG off voltage with respect to BAT	CHG/DSG C_L = 20 nF, steady state value			0.4	V
$V_{(DSGFETOFF)}$	DSG off voltage with respect to LD	CHG/DSG C_L = 20 nF, steady state value			0.7	V
$t_{(FET\_ON)}$	CHG and DSG rise time	CHG/DSG C_L = 20 nF, R_{GATE} = 100 Ω, 0.5 V to 4 V gate-source overdrive, charge pump high overdrive setting(4) (5)		21	40	µs
$t_{(CHGFETOFF)}$	CHG fall time to BAT	CHG C_L = 20 nF, R_{GATE} = 100 Ω, 90% to 10% of $V_{(FETON)}$ (5)		46	65	µs
$t_{(DSGFETOFF)}$	DSG fall time to LD	DSG C_L = 20 nF, R_{GATE} = 100 Ω, 90% to 10% of $V_{(FETON)}$ (5)		2	20	µs
$t_{(CP\_START)}$	Charge pump start up time	C_L = 20 nF, $C_{(CP1)}$ = 470 nF, 10% to 90% of $V_{(FETON)}$			100	ms
$C_{(CP1)}$	Charge pump capacitor(3)		100	470	2200	nF

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) When the DSG driver is enabled, the CHG driver is disabled, and a voltage is applied at the LD pin such that V_{LD} > V_{DSG}, the voltage at DSG will rise to ≈ V_{LD} - 0.7 V
(3) Specified by design
(4) Specified by characterization
(5) R_{GATE} can be optimized during design and system evaluation for best performance. A larger value may be desired to avoid an overly fast FET turn off, which can result in a large voltage transient due to cell and harness inductance.

7.26 Comparator-Based Protection Subsystem

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OVP)}$	Overvoltage detection range	Nominal setting (50.6 mV steps)		1.012 V to 5.566 V in 50.6 mV steps		V
$V_{(OVP\_ACC)}$	Overvoltage detection voltage threshold accuracy(4)	T_A = +25°C, nominal setting between 1.012 V and 5.566 V(2)		±2		mV
		T_A = +25°C, nominal setting between 3.036 V and 5.06 V(2)	–10		10	mV
		T_A = -10°C to +60°C, nominal setting between 1.012 V and 5.566 V(2)		±3		mV
		T_A = -10°C to +60°C, nominal setting between 3.036 V and 5.06 V(2)	–15		15	mV
		T_A = -40°C to +85°C, nominal setting between 1.012 V and 5.566 V(2)		±5		mV
		T_A = -40°C to +85°C, nominal setting between 3.036 V and 5.06 V(2)	–25		25	mV
$V_{(OVP\_DLY)}$	Overvoltage detection delay(3)	Nominal setting (3.3 ms steps)		10 ms to 6753 ms in 3.3 ms steps		ms
$V_{(UVP)}$	Undervoltage detection range	Nominal setting (50.6 mV steps)		1.012 V to 4.048 V in 50.6 mV steps		V
$V_{(UVP\_ACC)}$	Undervoltage detection voltage threshold accuracy(4)	T_A = +25°C, nominal setting between 1.012 V and 4.048 V(2)		±1.3		mV
		T_A = +25°C, nominal setting between 1.518 V and 3.542 V(2)	–10		10	mV
		T_A = -10°C to +60°C, nominal setting between 1.012 V and 4.048 V(2)		±1.4		mV
		T_A = -10°C to +60°C, nominal setting between 1.518 V and 3.542 V(2)	–15		15	mV
		T_A = -40°C to +85°C, nominal setting between 1.012 V and 4.048 V(2)		±1.6		mV
		T_A = -40°C to +85°C, nominal setting between 1.518 V and 3.542 V(2)	–25		25	mV
$V_{(UVP\_DLY)}$	Undervoltage detection delay(3)	Nominal setting (3.3 ms steps)		10 ms to 6753 ms in 3.3 ms steps		ms

7.26 Comparator-Based Protection Subsystem (continued)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCD)}$	Short circuit in discharge voltage threshold range	Nominal settings, threshold based on V_{SRP} - V_{SRN}		–10, –20, –40, –60, –80, –100, –125, –150, –175, –200, –250, –300, –350, –400, –450, –500		mV
$V_{(SCD\_ACC)}$	Short circuit in discharge voltage threshold detection accuracy(4)	T_A = -40°C to +85°C, $V_{(SCD)}$ settings ≤ -20 mV	–15		15	% of nominal threshold
		T_A = -40°C to +85°C, $V_{(SCD)}$ settings > -20 mV	–35		35	% of nominal threshold
$V_{(SCD\_DLY)}$	Short circuit in discharge detection delay	Fastest setting (with 3 mV on V_{SRN} - V_{SRP})		8		µs
		Fastest setting (with 25 mV on V_{SRN} - V_{SRP})		600		ns
		Nominal setting (15 µs steps)		15 µs to 450 µs in 15 µs steps		µs
$V_{(OCC)}$	Overcurrent in charge (OCC) voltage threshold range	Nominal settings, threshold based on V_{SRP} - V_{SRN}		4 mV to 124 mV in 2 mV steps		mV
$V_{(OCD)}$	Overcurrent in discharge (OCD1, OCD2) voltage threshold ranges	Nominal settings, thresholds based on V_{SRP} - V_{SRN}		–4 mV to –200 mV in 2 mV steps		mV
$V_{(OC\_ACC)}$	Overcurrent (OCC, OCD1, OCD2) detection voltage threshold accuracy(4)	|Setting| < 20 mV	–2		2.65	mV
		|Setting| = 20 mV ~ 56 mV	–4		4	mV
		|Setting| = 56 mV ~ 100 mV	–5		5	mV
		|Setting| > 100 mV	–7		5	mV
$V_{(OC\_DLY)}$	Overcurrent (OCC, OCD1, OCD2) detection delay (independent delay setting for each protection)	Nominal setting (3.3 ms steps)		10 ms to 425 ms in 3.3 ms steps		ms

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Measured by fault triggered using 100 ms detection delay.
(3) Cell balancing not active. Timing of overvoltage and undervoltage protection checks is modified when cell balancing is in progress.
(4) Specified by a combination of characterization and production test

7.27 Timing Requirements - I²C Interface, 100kHz Mode

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock operating frequency(2)	SCL duty cycle = 50%			100	kHz
$t_{HD:STA}$	START condition hold time(2)		4.0			µs
t_{LOW}	Low period of the SCL clock(2)		4.7			µs
t_{HIGH}	High period of the SCL clock(2)		4.0			µs
$t_{SU:STA}$	Setup repeated START(2)		4.7			µs
$t_{HD:DAT}$	Data hold time (SDA input)(2)		0			ns
$t_{SU:DAT}$	Data setup time (SDA input)(2)		250			ns
t_r	Clock rise time(2)	10% to 90%			1000	ns
t_f	Clock fall time(2)	90% to 10%			300	ns
$t_{SU:STO}$	Setup time STOP condition(2)		4.0			µs
t_{BUF}	Bus free time STOP to START(2)		4.7			µs
t_{RST}	I²C bus reset(2)	Bus interface is reset if SCL is detected low for this duration	1.9		2.1	s
R_{PULLUP}	Pullup resistor(3)	Pullup voltage rail ≤ 5 V	1.5			kΩ

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design
(3) Specified by characterization

7.28 Timing Requirements - I²C Interface, 400kHz Mode

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock operating frequency(2)	SCL duty cycle = 50%			400	kHz
$t_{HD:STA}$	START condition hold time(2)		0.6			µs
t_{LOW}	Low period of the SCL clock(2)		1.3			µs
t_{HIGH}	High period of the SCL clock(2)		600			ns
$t_{SU:STA}$	Setup repeated START(2)		600			ns
$t_{HD:DAT}$	Data hold time (SDA input)(2)		0			ns
$t_{SU:DAT}$	Data setup time (SDA input)(2)		100			ns
t_r	Clock rise time(2)	10% to 90%			300	ns
t_f	Clock fall time(2)	90% to 10%			300	ns
$t_{SU:STO}$	Setup time STOP condition(2)		0.6			µs
t_{BUF}	Bus free time STOP to START(2)		1.3			µs
t_{RST}	I²C bus reset(2)	Bus interface is reset if SCL is detected low for this duration	1.9		2.1	s
R_{PULLUP}	Pullup resistor(3)	Pullup voltage rail ≤ 5 V	1.5			kΩ

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design
(3) Specified by characterization

7.29 Timing Requirements - HDQ Interface

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_B	Break Time(2)		190			µs
t_{BR}	Break Recovery Time(2)		40			µs
t_{HW1}	Host Write 1 Time(2)	Host drives HDQ	0.5		50	µs
t_{HW0}	Host Write 0 Time(2)	Host drives HDQ	86		145	µs
t_{CYCH}	Cycle Time, Host to device(2)	Device drives HDQ	190			µs
t_{CYCD}	Cycle Time, device to Host(2)	Device drives HDQ	190	205	250	µs
t_{DW1}	Device Write 1 Time(2)	Device drives HDQ	32		50	µs
t_{DW0}	Device Write 0 Time(2)	Device drives HDQ	80		145	µs
t_{RSPS}	Device Response Time(2) (4)	Device drives HDQ	190			µs
t_{TRND}	Host Turn Around Time(2)	Host drives HDQ after device drives HDQ	210			µs
t_{RISE}	HDQ Line Rising Time to Logic 1(2)				1.8	µs
t_{RST}	HDQ Bus Reset(2)	Host holds bus low to initiate device interface reset	1.9		2.1	s
R_{PULLUP}	Pullup Resistor(3)	Pullup voltage rail ≤ 5 V	1.5			kΩ

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design
(3) Specified by characterization
(4) Response time will vary depending on the internal device processing

7.30 Timing Requirements - SPI Interface

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 4.7 V to 80 V (unless otherwise noted). All values specified with SPI pin filtering enabled.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SCK}	SPI clock period(2)		500(5)			ns
t_{LEAD}	Enable lead-time(2)		625			ns
t_{LAG}	Enable lag time(2)		50			ns
t_{TD}	Sequential transfer delay(3)			50		µs
t_{SU}	Data setup time(2) (6)		50			ns
t_{HI}	Data hold time (inputs)(2) (6)		50			ns
t_{HO}	Data hold time (outputs)(2)		0			ns
t_A	Slave access time(2)				500	ns
t_{DIS}	Slave DOUT disable time(2)				450	ns
t_V	Data valid(2)				235(5)	ns
t_R	Rise time(2)	Up to 25pF load			30	ns
t_F	Fall time(2)	Up to 25pF load			30	ns
t_{RST}	SPI bus reset(2)	Bus interface is reset if SPI_CS is low and SPI_SCLK is detected unchanged for this duration	1.9		2.1	s

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Specified by design
(3) See later discussion in datasheet for more details
(4) Specified by characterization

(5) This assumes 15 ns setup time on the SPI master for MISO. If additional setup time is required, the clock period should be extended accordingly.
(6) When SPI pin filtering is enabled, pulses on input pins of duration below 200 ns may be filtered out.

7.31 Interface Timing Diagrams

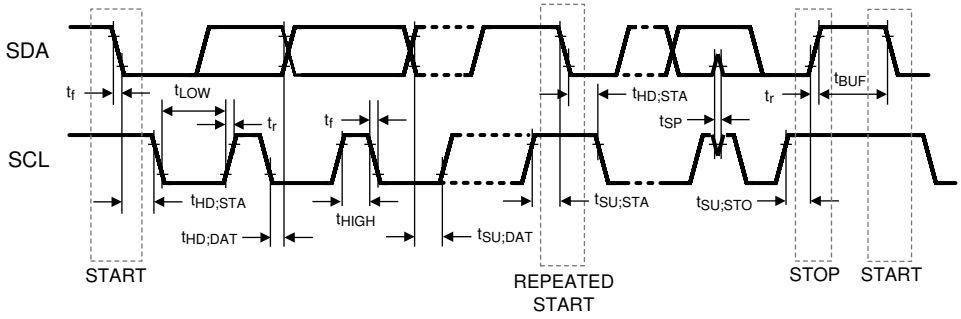


図 7-1. I²C Communications Interface Timing

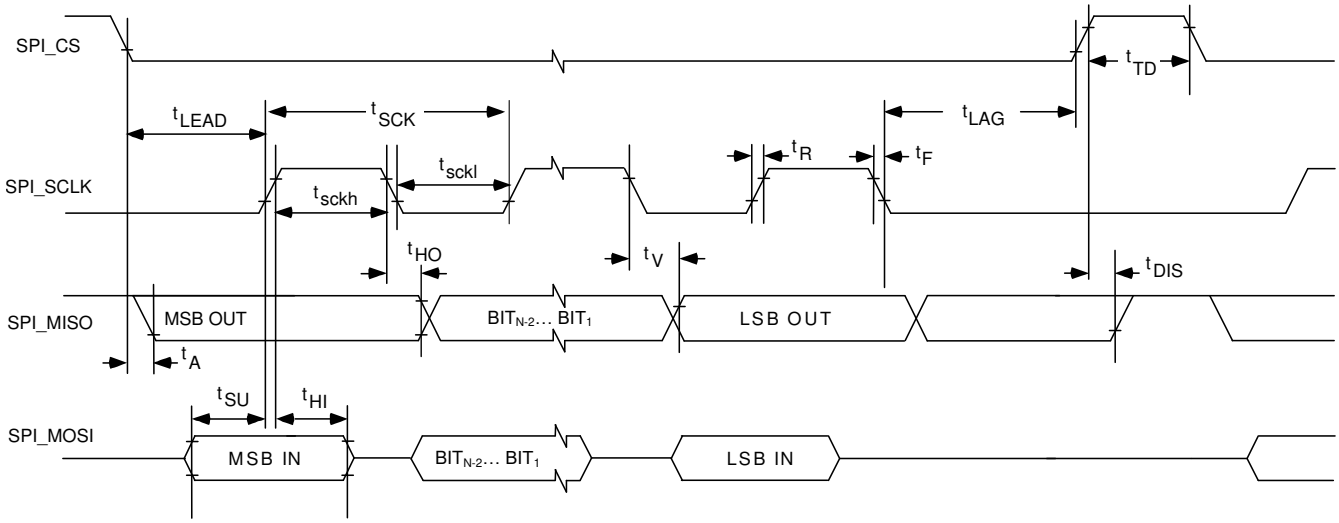
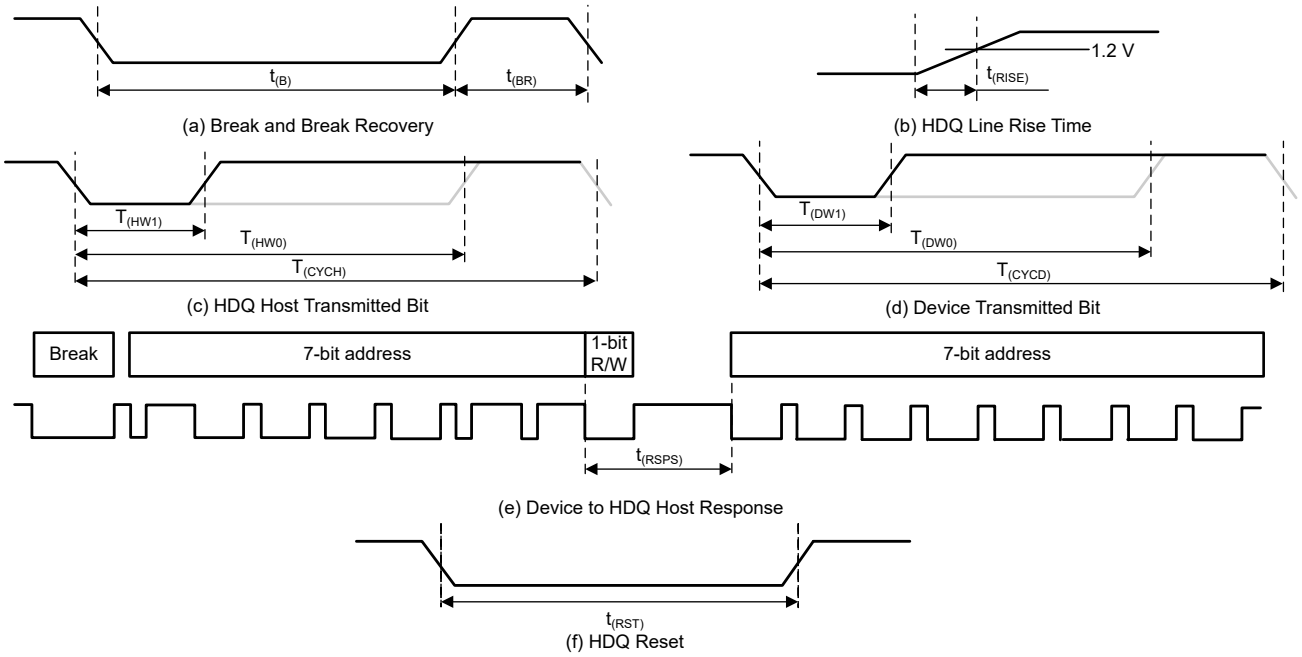


図 7-2. SPI Communications Interface Timing



a. HDQ Breaking
b. Rise time of HDQ line
c. HDQ Host to Device communication
d. Device to HDQ Host communication
e. Device to HDQ Host response format
f. HDQ Host to Device

図 7-3. HDQ Communications Interface Timing

7.32 Typical Characteristics

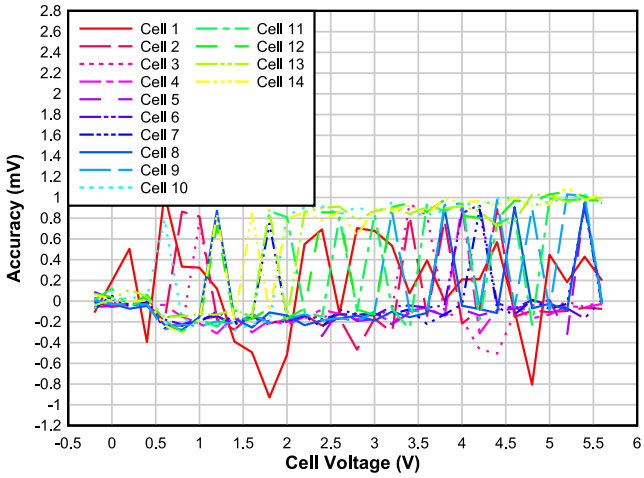


図 7-4. Cell Voltage Measurement Error at 25°C Across Input Range

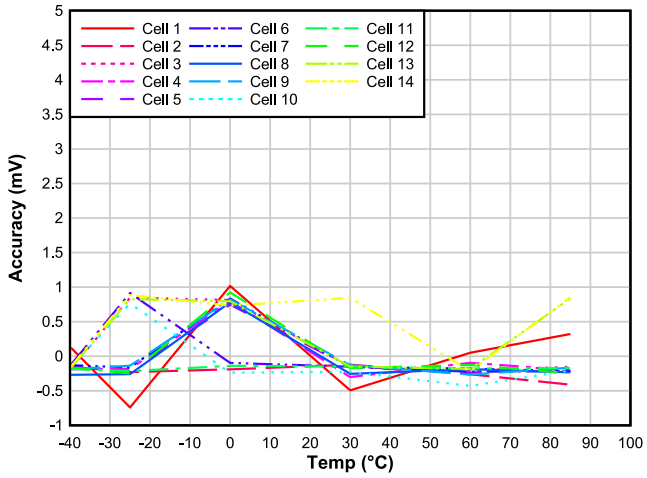


図 7-5. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 1.5 V

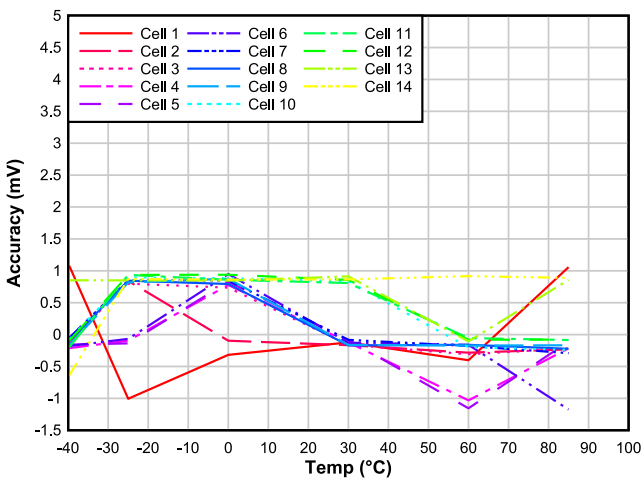


図 7-6. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 2.5 V

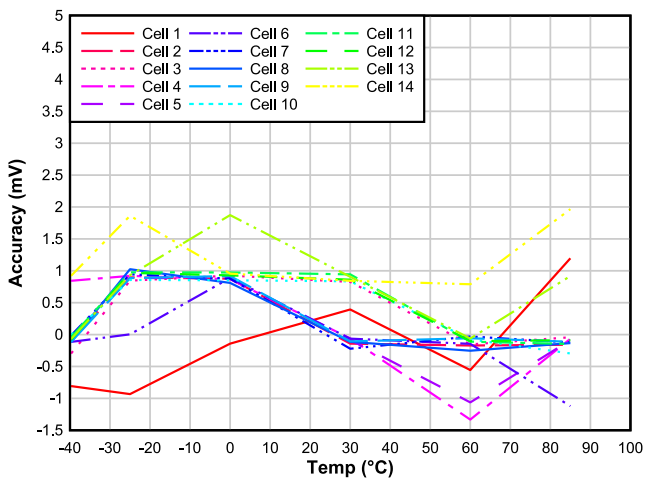


図 7-7. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 3.5 V

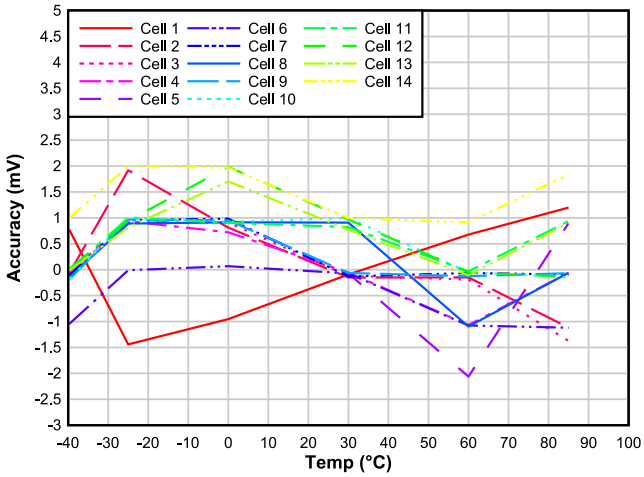


図 7-8. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 4.5 V

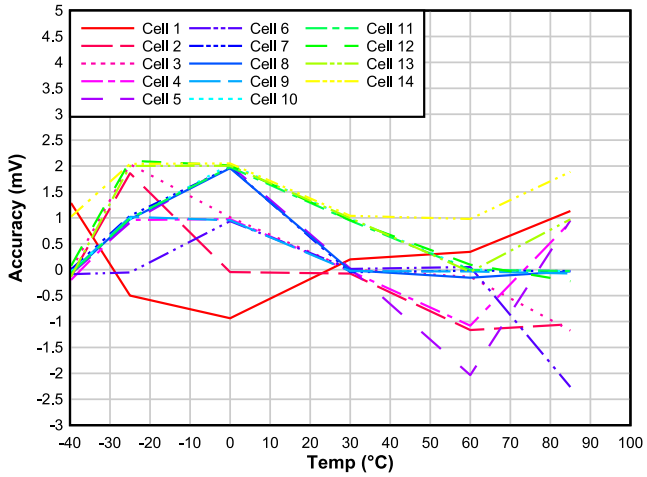
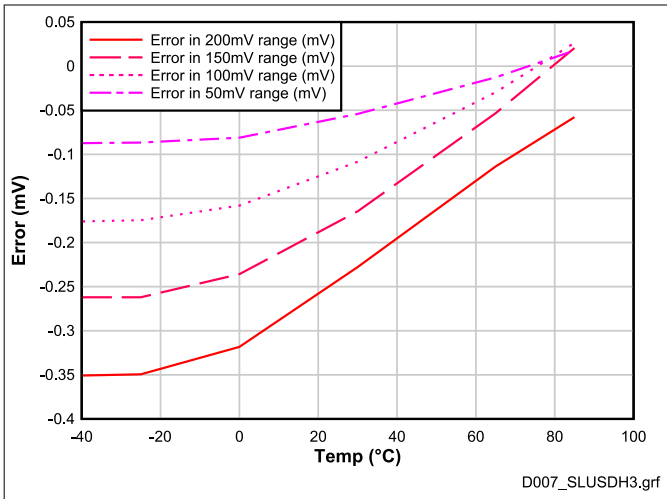


図 7-9. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 5.5 V



Error in measurement of differential voltage between SRP and SRN pins.

図 7-10. Current Measurement Error vs. Temperature

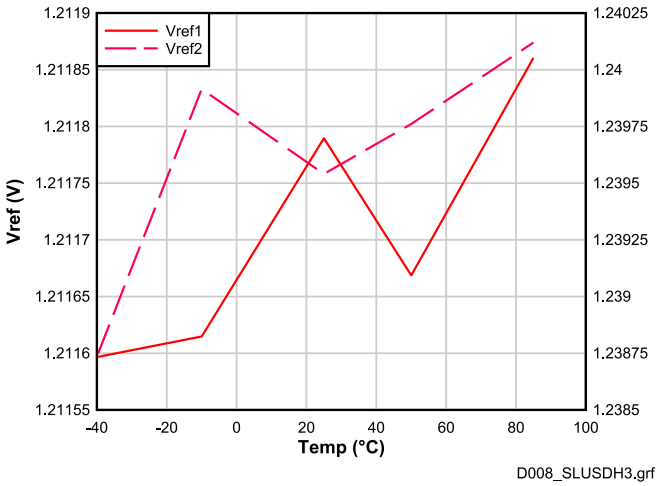


図 7-11. Internal Voltage References vs. Temperature (VREF1 and VREF2)

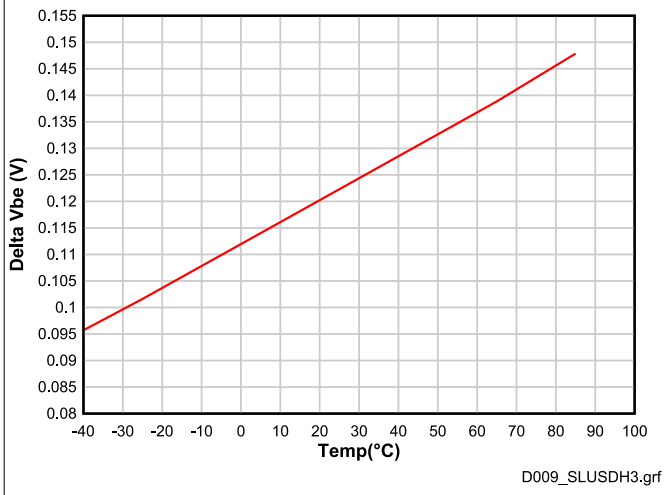
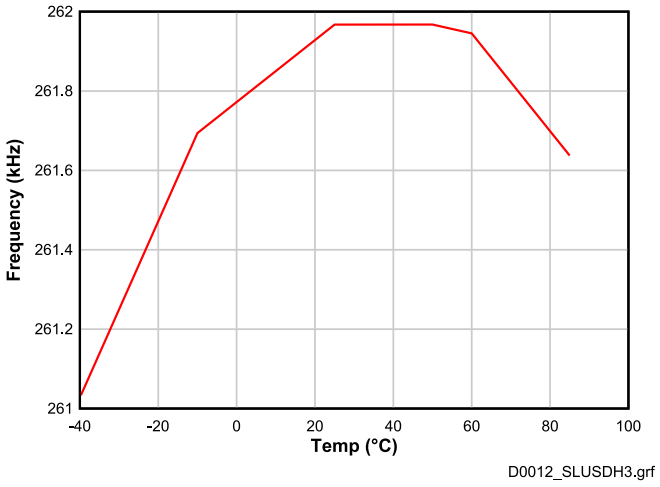


図 7-12. Internal Temperature Sensor (Delta V_{BE}) Voltage vs. Temperature



LFO measured in full speed mode (262 kHz)

図 7-13. Low Frequency Oscillator (LFO) Accuracy vs. Temperature

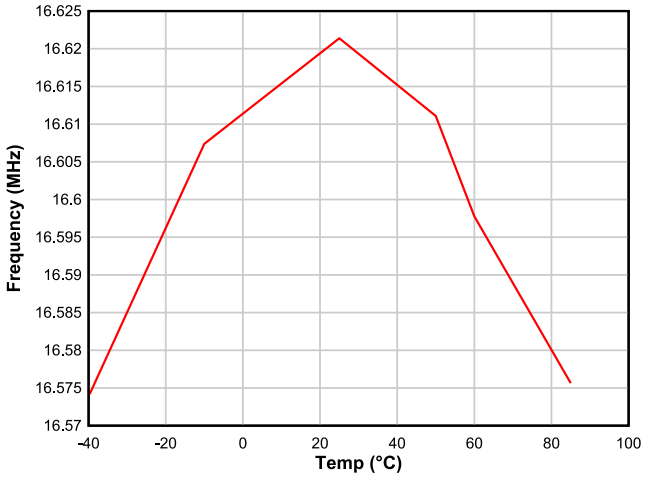


図 7-14. High Frequency Oscillator (HFO) Accuracy vs. Temperature

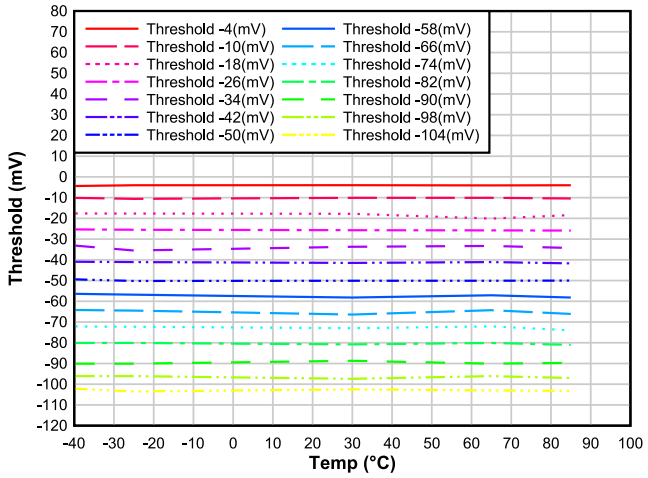


図 7-15. Overcurrent in Discharge Protection 1 (OCD1) Threshold vs. Temperature

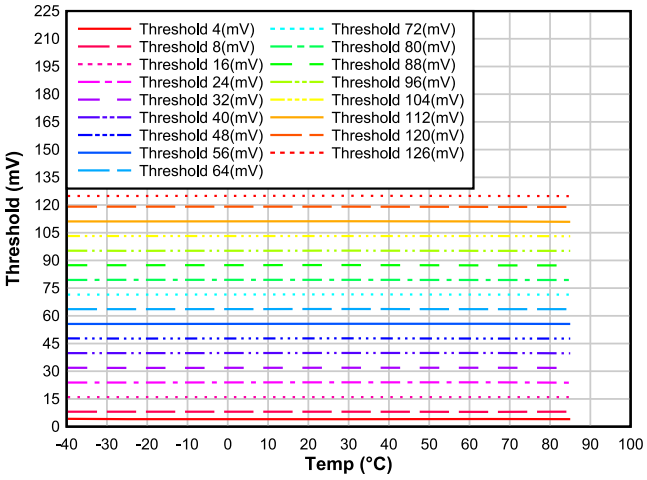


図 7-16. Overcurrent in Charge Protection (OCC) Threshold vs. Temperature

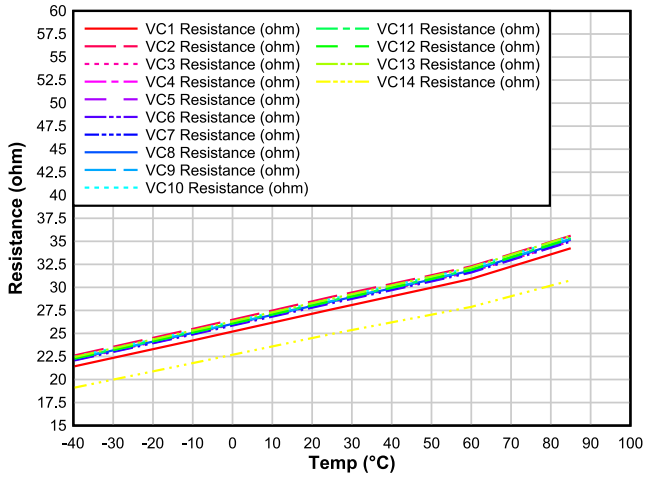
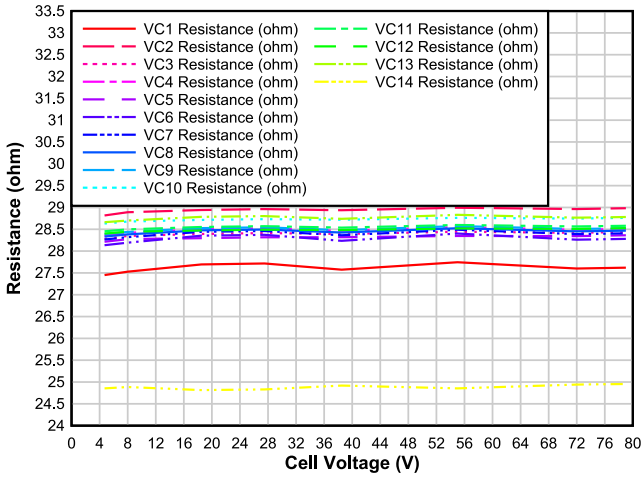


図 7-17. Cell Balancing Resistance vs. Temperature



This test uses a resistor divider across the VCx pins to allow for one common voltage to be scaled across the cell inputs. The top of the string is swept and captured as the Cell Voltage.

図 7-18. Cell Balancing Resistance vs. Cell Common-mode Voltage at 25°C

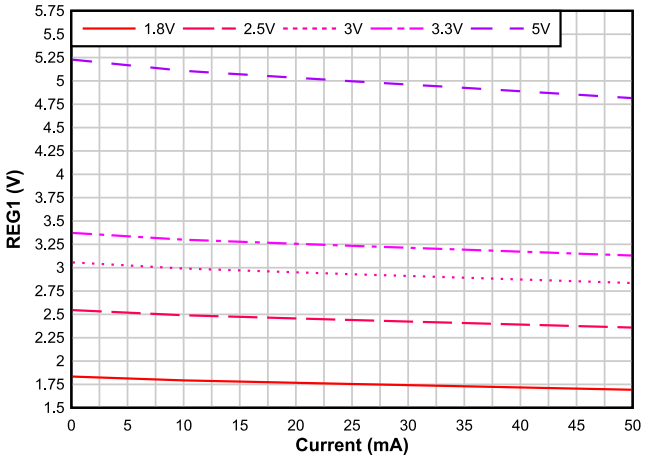


図 7-19. REG1 Voltage vs. Load at 25°C

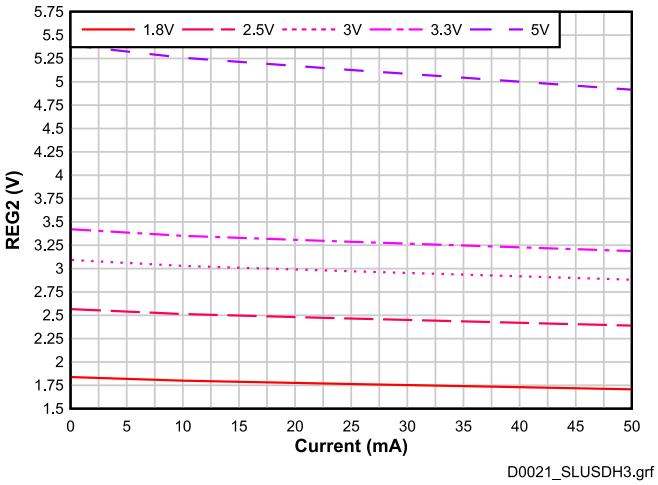


図 7-20. REG2 Voltage vs. Load at 25°C

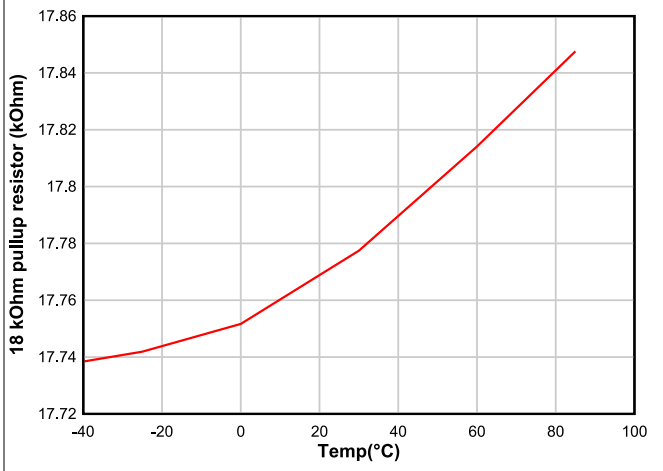


図 7-21. Thermistor Pullup Resistance vs. Temperature (18-kΩ setting)

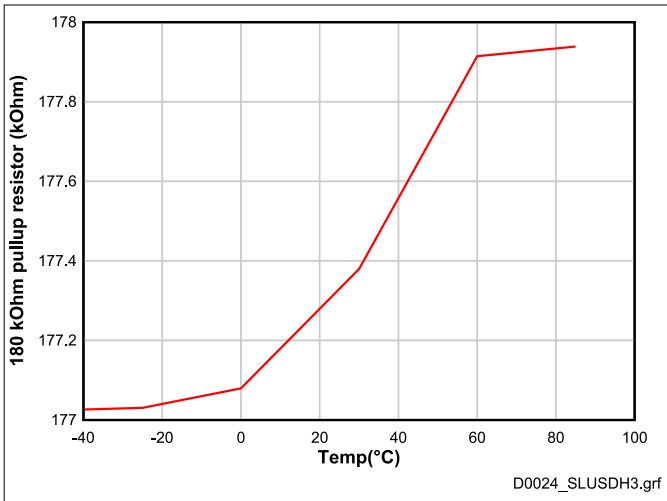
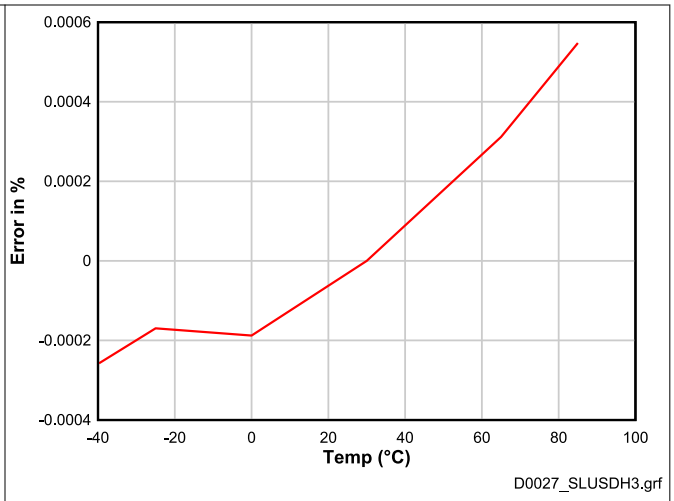


図 7-22. Thermistor Pullup Resistance vs. Temperature (180-kΩ setting)



Error calculated as percentage of nominal gain across ±200-mV input range

図 7-23. Coulomb Counter Gain Error vs. Temperature

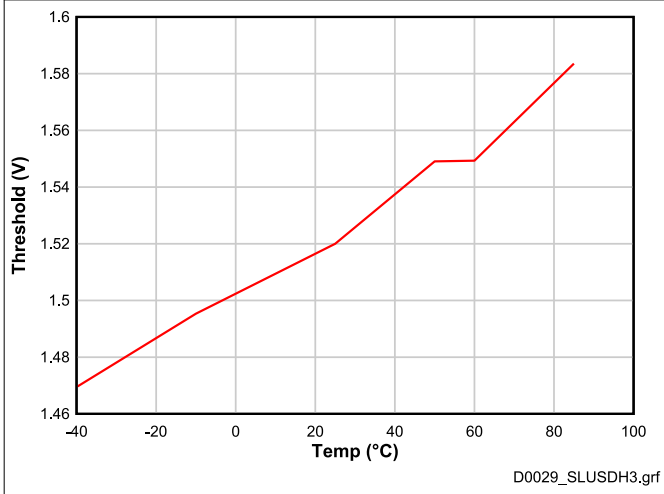


図 7-24. LD Wake Voltage vs. Temperature

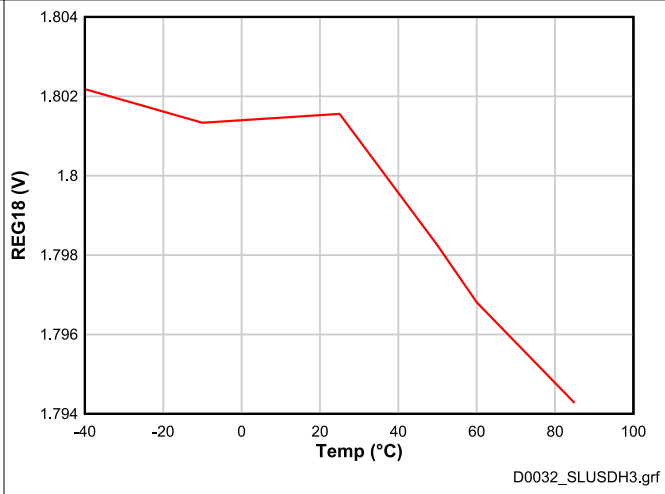


図 7-25. REG18 Voltage vs. Temperature, with No Load

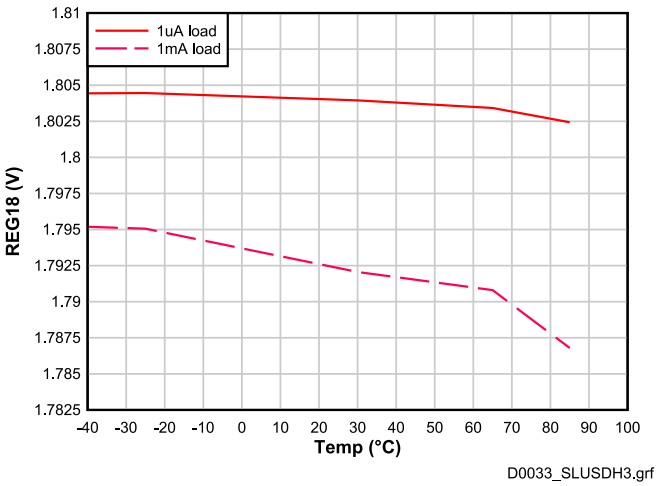
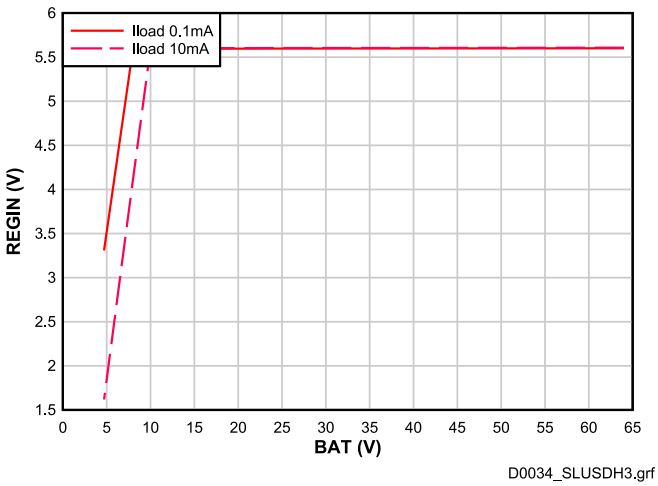


図 7-26. REG18 Voltage vs. Load Current, at 25°C



Measurements taken using external BJT

図 7-27. REGIN Voltage vs. BAT Voltage

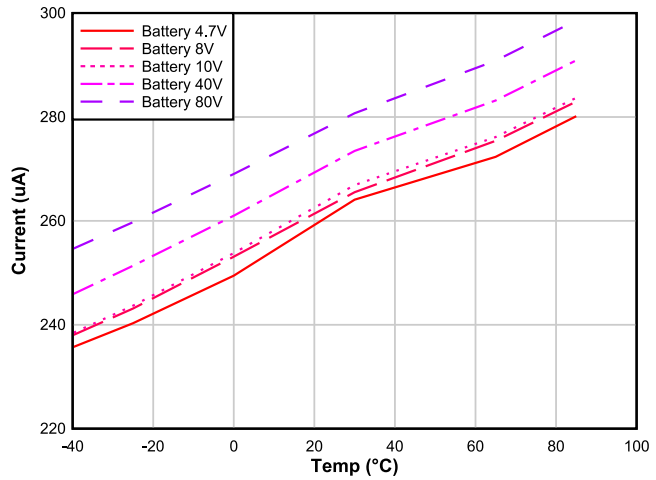


図 7-28. BAT Current in NORMAL Mode vs. Temperature

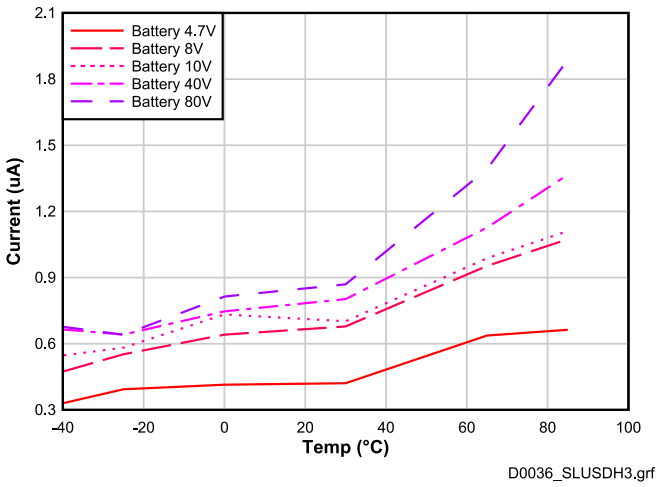


図 7-29. BAT Current in SHUTDOWN Mode vs. Temperature

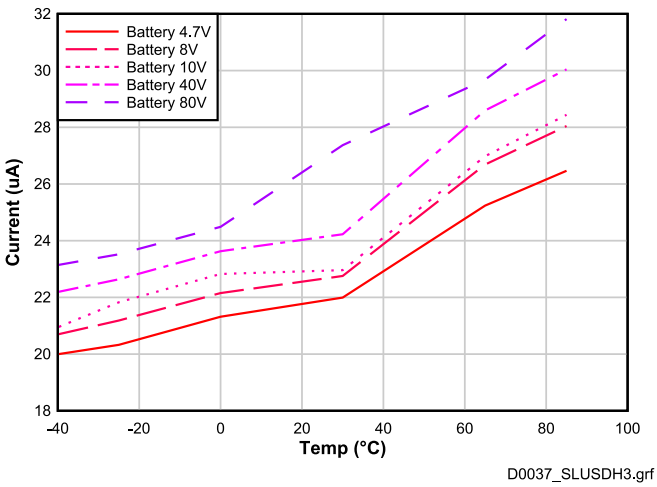


図 7-30. BAT Current in SLEEP2 (SRC Follower) Mode vs. Temperature

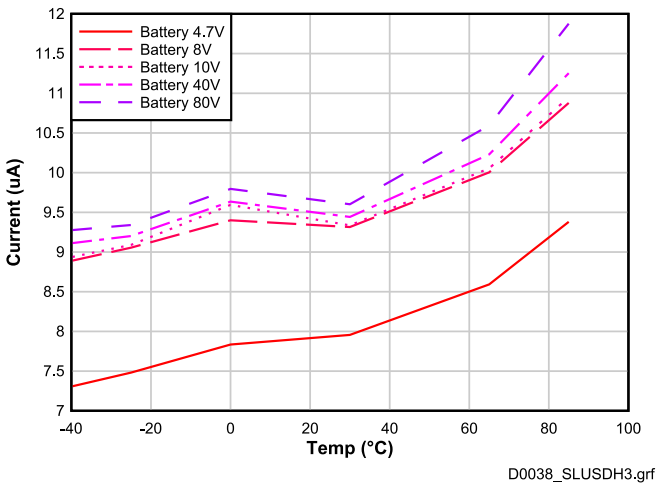


図 7-31. BAT Current in DEEPSLEEP2 (No LFO) Mode vs. Temperature

8 Device Description

8.1 Overview

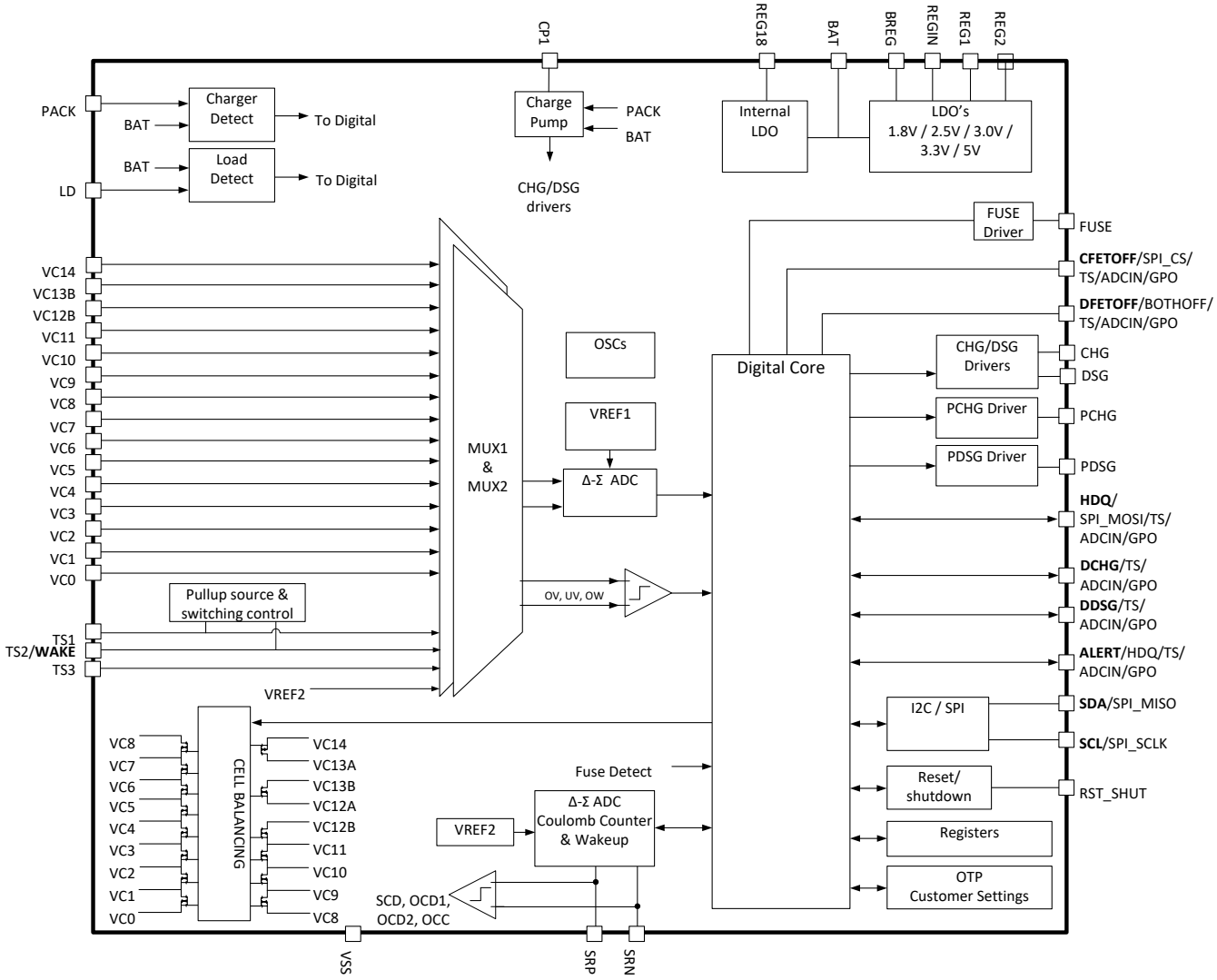
The BQ769142 device is a highly integrated, accurate battery monitor and protector for 3-series to 14-series Li-ion, Li-polymer, and $LiFePO_4$ battery packs. A high accuracy voltage, current, and temperature measurement accuracy provides data for host-based algorithms and control. A feature-rich and highly configurable protection subsystem provides a wide set of protections that can be triggered and recovered completely autonomously by the device or under full control of a host processor. The integrated charge pump with high-side protection NFET drivers enables host communication with the device even when FETs are off by preserving the ground connection to the pack. Dual-programmable LDOs are included for external system use, with each independently programmable to voltages of 1.8 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V, capable of providing up to 45 mA each.

The BQ769142 device includes one-time-programmable (OTP) memory for customers to setup device operation on their own production line. Multiple communications interfaces are supported, including 400-kHz I^2C, SPI, and HDQ one-wire standards. Multiple digital control and status data are available through several multifunction pins on the device, including an interrupt to the host processor, and independent controls for host override of each high-side protection NFET. Three dedicated pins are provided for temperature measurement using external thermistors, and multifunction pins can be programmed to use for additional thermistors, supporting a total of up to nine thermistors, in addition to an internal die temperature measurement.

8.2 BQ769142 Device Versions

The BQ769142 device family may include versions with differing default settings programmed during factory test. These different settings, which may include having a different default communications interface or a different setting for the REG1 LDO, will be described in the *Device Comparison Table*.

8.3 Functional Block Diagram



8.4 Diagnostics

The BQ769142 device includes a suite of diagnostic tests the system can use to increase operational robustness. These tests include comparisons between the two voltage references integrated within the device, a hardware monitor of the LFO frequency, memory checks at power-up or reset, an internal watchdog on the embedded processor, and more. These are described in detail in the *BQ769142 Technical Reference Manual*.

9 Device Configuration

9.1 Commands and Subcommands

The BQ769142 device includes support for direct commands and subcommands. The direct commands are accessed using a 7-bit command address that is sent from a host through the device serial communications interface and either triggers an action, provides a data value to be written to the device, or instructs the device to report data back to the host. Subcommands are additional commands that are accessed indirectly using the 7-bit command address space and provide the capability for block data transfers. For more information on the commands and subcommands supported by the device, refer to the *BQ769142 Technical Reference Manual*.

9.2 Configuration Using OTP or Registers

The BQ769142 device includes registers with values that are stored in the RAM and can be loaded automatically from one-time programmable (OTP) memory. At initial power-up, the device loads OTP settings into registers that are used by the device firmware during operation. The recommended procedure is for the customer to write settings into OTP on the manufacturing line in which case the device will use these settings whenever it is powered up. Alternatively, the host processor can initialize registers after power-up without using the OTP memory, but the registers need to be reinitialized after each power cycle of the device. Register values are preserved while the device is in NORMAL, SLEEP, or DEEPSLEEP modes. If the device enters SHUTDOWN mode, all register memory is cleared, and the device will return to the default parameters (or the OTP configuration if that has been programmed) when powered again. See the *BQ769142 Technical Reference Manual* for more details.

9.3 Device Security

The BQ769142 device includes three security modes—SEALED, UNSEALED, and FULLACCESS—that can be used to limit the ability to view or change settings.

- In SEALED mode, most data and status can be read using commands and subcommands, but only selected settings can be changed. Data memory settings cannot be changed directly.
- UNSEALED mode includes SEALED functionality, and also adds the ability to execute additional subcommands, and read and write data memory.
- FULLACCESS mode allows capability to read and modify all device settings, including writing OTP memory.

Selected settings in the device can be modified while the device is in operation through supported commands and subcommands, but in order to modify all settings, the device must enter CONFIG_UPDATE mode (see セクション 13.6), which stops device operation while settings are being updated. After the update is completed, the operation is restarted using the new settings. CONFIG_UPDATE mode is only available in FULLACCESS mode.

The BQ769142 device implements a key-access scheme to transition among SEALED, UNSEALED, and FULLACCESS modes. Each transition requires that a unique set of keys be sent to the device through subcommands. Refer to the *BQ769142 Technical Reference Manual* for more details.

The device provides additional checks which can be used to optimize system robustness, including subcommands that calculate the digital signature of the integrated instruction ROM and data ROM. These signatures should never change for a particular product. If these were to change, it would indicate an error: either that the ROM had been corrupted or the readback of the ROM or calculation of the signature experienced an error. An additional subcommand calculates a digital signature for the static configuration data (which excludes calibration values) and compares it to a stored value, returning a flag if the result does not match.

9.4 Scratchpad Memory

The BQ769142 device integrates a 32-byte scratchpad memory for the customer to use to store manufacturing data, such as serial numbers, production or test dates, and so forth. The scratchpad data can be written into OTP memory on the customer production line. This data can only be written while in FULLACCESS mode, although it can be read in all modes.

10 Measurement Subsystem

10.1 Voltage Measurement

The BQ769142 device integrates a voltage ADC, which is multiplexed between measurements of cell voltages, an internal temperature sensor, and up to nine external thermistors, and also performs measurements of the voltage at the VC14 pin, the PACK pin, the LD pin, the internal REG18 LDO voltage, and the VSS rail (for diagnostic purposes). The BQ769142 device supports measuring individual differential cell voltages in a series configuration, ranging from 3-series cells to 14-series cells. Each cell voltage measurement is a differential measurement of the voltage between two adjacent cell input pins, such as VC1-VC0, VC2-VC1, and so forth. The cell voltage measurements are processed based on trim and calibration corrections, and then reported in 16-bit resolution using units of 1 mV. The raw 24-bit digital output of the ADC is also available for readout using 32-bit subcommands. The cell voltage measurements can support a recommended voltage range from –0.2 V to 5.5 V. The voltage ADC saturates at a level of 5 × VREF1 (approximately 6.25 V) when measuring cell voltages, although for best performance, it is recommended to stay at a maximum input of 5.5 V.

10.1.1 Voltage Measurement Schedule

The BQ769142 voltage measurements are taken in a measurement loop that consists of multiple measurement slots. All 14-cell voltages are measured on each loop, then one slot is used for one of the VC14 or PACK or LD pin voltages, one slot is used for internal temperature or Vref or VSS measurement, then up to three slots are used to measure thermistors or multifunction pin voltages (ADCIN functionality). Over the course of three loops, a full set of measurements is completed. One measurement loop consists of either 18 (if no thermistors or ADCIN are enabled), 19 (if one thermistor or ADCIN is enabled), 20 (if two thermistors or ADCIN are enabled), or 21 (if three or more thermistors or ADCIN are enabled) measurement slots.

The speed of a measurement loop can be controlled by settings. Each voltage measurement (slot) takes 3 ms (or 1.5 ms depending on setting), so a typical measurement loop with 21 slots per loop takes 63 ms (or 31.5 ms depending on setting). If measurement data is not required as quickly, the timing for the measurement loop can be programmed to slower speeds, which injects idle slots in each loop after the measurement slots. Using slower loop cycle time will reduce the power dissipation of the device when in NORMAL mode.

10.1.2 Using VC Pins for Cells Versus Interconnect

If the BQ769142 device is used in a system with fewer than 14-series cells, the additional cell inputs can be utilized to improve measurement performance. For example, a long connection may exist between two cells in a pack, such that there may be significant interconnect resistance between the cells, as shown in Using Cell Input Pins for Interconnect Measurement, between CELL-A and CELL-B. By connecting VC10 close to the positive terminal of CELL-B, and connecting VC11 close to the negative terminal of CELL-A, more accurate cell voltage measurements are obtained for CELL-A and CELL-B, since the I·R voltage across the interconnect resistance between the cells is not included in either cell voltage measurement. Since the device reports the voltage across the interconnect resistance and the synchronized current, the resistance of the interconnect between CELL-A and CELL-B can also be calculated and monitored during operation. It is recommended to include the series resistance and bypass capacitor on cell inputs connected in this manner, as shown below.

Note

It is important that the differential input for each cell input not fall below –0.3 V (the Absolute Maximum data sheet limit), with the recommended minimum voltage of –0.2 V. Therefore, it is important that the I·R voltage drop across the interconnect resistance does not cause a violation of this requirement.

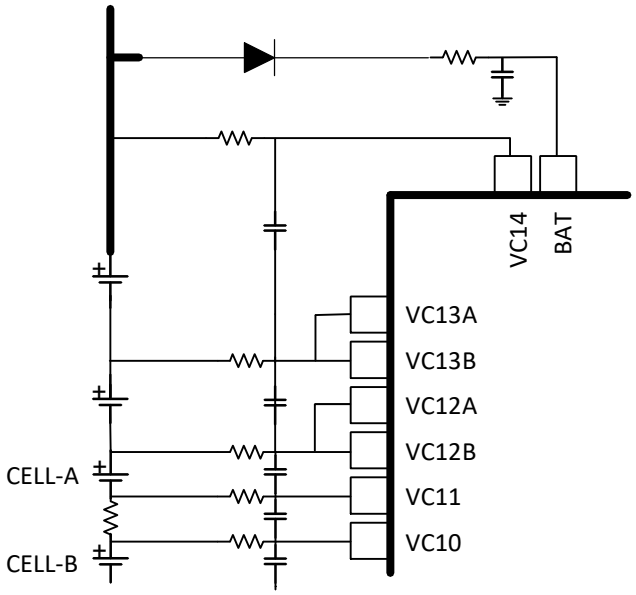


図 10-1. Using Cell Input Pins for Interconnect Measurement

If this connection across an interconnect is not needed (or it is preferred to avoid the extra resistor and capacitor), then the unused cell input pins should be shorted to adjacent cell input pins, as shown in 図 10-2 for VC11.

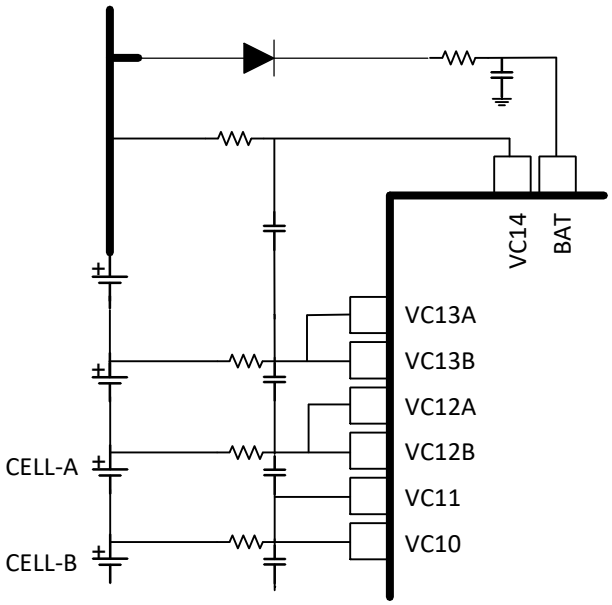


図 10-2. Terminating an Unused Cell Input Pin

A configuration register is used to specify which cell inputs are used for actual cells. The device uses this information to disable cell voltage protections associated with inputs which are used to measure interconnect or are not used at all. Voltage measurements for all inputs are reported in 16-bit format (in units of mV) as well as 32-bit format (in units of raw ADC counts), irrespective of whether they are used for cells or not.

10.1.3 Cell 1 Voltage Validation During SLEEP Mode

In rare cases, an invalid *Cell 1 Voltage()* reading has been observed to occur in some devices taken during SLEEP mode.

While the device is in SLEEP mode, each result obtained from reading the *Cell 1 Voltage()* must be validated before it can be considered valid. During SLEEP mode, current is below programmable thresholds, so the pack is typically not being charged or discharged with any significant level of current. Thus, the cell voltages will generally not be changing significantly.

In order to determine if a measurement of *Cell 1 Voltage()* taken during SLEEP mode is valid, it is necessary to compare each measurement to measurements taken before and after the particular measurement. It is important that these three readings represent three ***separate measurements*** for the *Cell 1 Voltage()*. If the reading is significantly different from the separate readings taken before and after, then that reading is considered invalid and should be discarded.

In order to ensure the three measurements read from the device are truly ***separate measurements***, the host can read the measurements at intervals exceeding ***Power:Sleep:Voltage Time*** while the device is in SLEEP mode. This is necessary to avoid the host reading an existing measurement multiple times, before a new measurement has been taken and is available for readout.

An invalid *Cell 1 Voltage()* reading may result in an SUV PF Alert being set but does not result in an SUV PF status fault if the SUV Delay is set to 1 second or longer. It also does not trigger a Cell Undervoltage (CUV) Protection alert or status fault, since this protection uses a comparator for its detection. If a reading reported by *Cell 1 Voltage()* is below the ***Protections:CUV:Threshold*** level and the CUV protection is enabled, but the CUV Alert is not triggered, this also can be used as an indication the reading is invalid.

This validation process is necessary to ensure that valid *Cell 1 Voltage()* results are measured.

10.2 General Purpose ADCIN Functionality

Several multifunction pins on the BQ769142 device can be used for general purpose ADC input (ADCIN) measurement, if not being used for other purposes. This includes the TS1, TS2, TS3, CFETOFF, DFETOFF, HDQ, DCHG, DDSG, and ALERT pins. When used for ADCIN functionality, the internal bandgap reference is used by the ADC, and the input range of the ADC is limited to the REG18 pin voltage. The digital fullscale range of the ADC is effectively 1.6667 × VREF1, which is approximately 2.02 V during normal operation.

The BQ769142 device also reports the raw ADC counts when a measurement is taken using the TS1 pin. This data can be used during manufacturing to better calibrate the ADCIN functionality.

10.3 Coulomb Counter and Digital Filters

The BQ769142 device monitors pack current using a low-side sense resistor that connects to the SRP and SRN pins through an external RC filter, which should be connected such that a charging current creates a positive voltage on SRP relative to SRN. The differential voltage between SRP and SRN is digitized by an integrated coulomb counter ADC, which can digitize voltages over a ±200-mV range, and uses multiple digital filters to provide optimized measurement of the instantaneous, averaged, and integrated current. The device supports a wide range of sense resistor values, with a larger value providing better resolution for the digitized result. The maximum value of the sense resistor should be limited to ensure the differential voltage remains within the ±200-mV range for system operation when current measurement is desired. For example, a system with maximum discharge current of 200 A during normal operation (not a fault condition) should limit the sense resistor to 1 mΩ or below.

The SRP and SRN pins can also support higher positive voltages relative to VSS, such as may occur during overcurrent or short circuit in discharge conditions without damage to the device, although the current is not accurately digitized in this case. For example, a system with a 1 mΩ sense resistor and the short circuit in discharge protection threshold programmed to a 500-mV level would trigger an SCD protection fault when a discharge current of 500 A was detected.

Multiple digitized current values are available for readout over the serial communications interface, including two using separate hardware digital filters, CC1 and CC2, as well as a firmware filter, CC3.

- The CC1 filter generates a 16-bit current measurement that is used for charge integration and other decision purposes, with one output generated every 250 ms when the device is operating in NORMAL mode.
- The CC2 filter generates a 24-bit current measurement that is used for current reporting, with one output every 3 ms when the device is operating in NORMAL mode (which can be reduced to one output every 1.5

ms based on setting, with reduced measurement resolution). It is reported in 16-bit format, and the 24-bit CC2 data is also available as raw coulomb counter ADC counts, provided in a 32-bit format (with the data contained in the lower 24-bits and the upper 8-bits sign-extended).

- The CC3 filter output is an average of a programmable number of CC2 current samples (up to 255), based on the configuration setting. The CC3 output is reported in 32-bit format.

The integrated passed charge is available as a 64-bit value, which includes the upper 32 bits of accumulated charge as the integer portion, the lower 32 bits of accumulated charge as the fractional portion, and a 32-bit accumulated time over which the charge has been integrated in units of seconds. The accumulated charge integration and timer can be reset by a command from the host over the digital communications interface.

10.4 Synchronized Voltage and Current Measurement

While the cell voltages are digitized sequentially using a single muxed ADC during normal operation, the current is digitized continuously by the dedicated coulomb counter ADC. The current is measured synchronously with each cell voltage measurement, and can be used for individual cell impedance analysis. The ongoing periodic current measurements can be read out through the digital communication interface, while the measurements taken that were synchronized with particular cell voltage measurements are stored paired with the associated cell voltage measurement for separate readout. These values can be read using a block subcommand, which ensures the synchronously aligned voltage and current data are read out together.

10.5 Internal Temperature Measurement

The BQ769142 device integrates the capability to measure its internal die temperature by digitizing the difference in internal transistor base-emitter voltages (delta-V_{BE}). This voltage is measured periodically as part of the measurement loop and is processed to provide a reported temperature value available through the digital communications interface. This internal temperature measurement can be used for cell or FET temperature protections and logic based on configuration settings.

10.6 Thermistor Temperature Measurement

The BQ769142 device includes an on-chip temperature measurement and can also support up to nine external thermistors on multifunction pins (TS1, TS2, TS3, CFETOFF, DFETOFF, ALERT, HDQ, DCHG, and DDSG). The device includes an internal pullup resistor to bias a thermistor during measurement.

The internal pullup resistor has two options that can set the pullup resistor to either 18 kΩ or 180 kΩ (or none at all). The 18-kΩ option is intended for use with thermistors such as the Semitec 103-AT, which has 10-kΩ resistance at room temperature. The 180-kΩ option is intended for use with higher resistance thermistors such as the Semitec 204AP-2, which has 200-kΩ resistance at room temperature. The resistor values are measured during factory production and stored within the device for use during temperature calculation. The individual pin configuration registers determine which pin is used for a thermistor measurement, what value of pullup resistor is used, as well as whether the thermistor measurement is used for a cell or FET temperature reading.

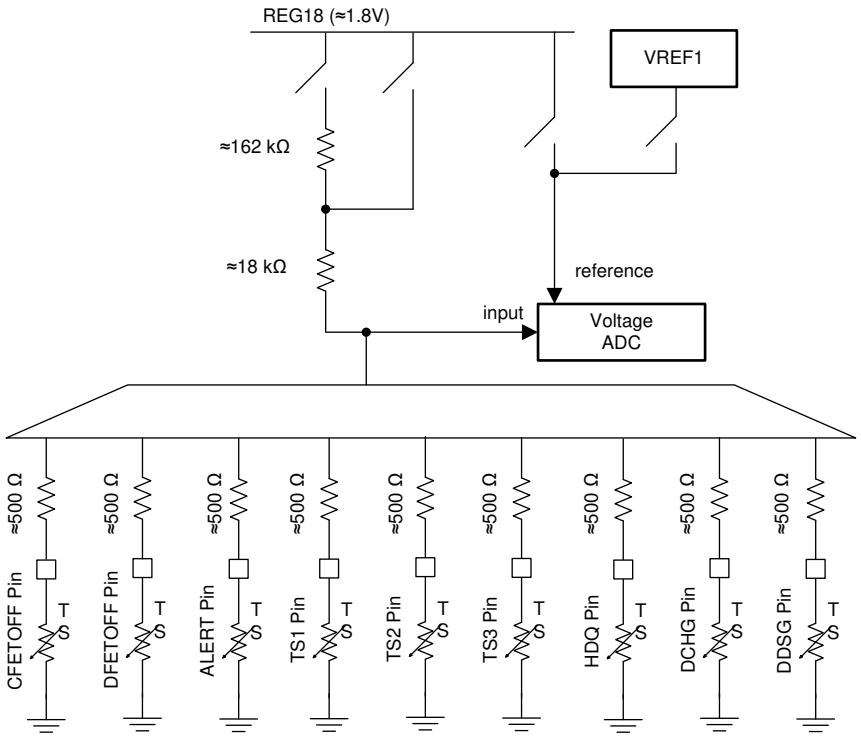


図 10-3. External Thermistor Biasing

To provide a high precision temperature result, the device uses the same 1.8-V LDO voltage for the ADC reference as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric measurement that removes the error contribution from the LDO voltage level. The device processes the digitized thermistor voltage to calculate the temperature based on multiorder polynomials, which the user can be program, based on the specific thermistor selected.

10.7 Factory Trim of Voltage ADC

The BQ769142 device includes factory trim for the cell voltage ADC measurements to optimize the voltage measurement performance even if the customer does no further calibration. The customer can perform calibration on the production line to further optimize the performance in the system. The trim information is used to correct the raw ADC readings before they are reported as 16-bit voltage values. The 32-bit ADC voltage data, which is generated in units of ADC counts, is modified before reporting by subtracting a stored offset trim value. The resulting reported data does not include any further correction (such as for gain), therefore the customer will need to process them before use.

The device includes a factory gain trim for the voltage measurements performed using the general purpose ADC input capability on the multifunction pins as well as the TS1, TS2, and TS3 pins. It also includes factory gain trim on the voltage measurements of the PACK pin, the LD pin, and the top-of-stack (VC14) pin.

10.8 Voltage Calibration (ADC Measurements)

The BQ769142 device includes an optional capability for the customer to calibrate each cell voltage gain and the gain for the stack voltage, the PACK pin voltage, and the LD pin voltage individually, and multifunction pin general ADC measurements. An offset calibration value ***Calibration:Vcell Offset:Vcell Offset*** is included for use with the cell voltage measurements, and ***Calibration:Vdiv Offset:Vdiv Offset*** is used with the TOS (stack), PACK, and LD voltage measurements. The cell voltage gains determined during calibration are written in ***Calibration:Voltage:Cell 1 Gain – Cell 14 Gain***, where ***Cell 1 Gain*** is used for the measurement of VC1–VC0, ***Cell 2 Gain*** is used for the measurement of VC2–VC1, and so forth. Similarly, the calibration voltage gain for the TOS voltage should be written in ***Calibration:Voltage:TOS Gain***, the PACK pin voltage gain in ***Calibration:Voltage:Pack Gain***, the LD pin voltage gain in ***Calibration:Voltage:LD Gain***, and multifunction pin general purpose ADCIN measurement gain in ***Calibration:Voltage:ADC Gain***.

If values for the calibration gain configuration are not written, the BQ769142 device uses a factory trim or default values for the respective gain values. When a calibration gain configuration value is written, the device will use that in place of any factory trim or default gain. The raw ADC measurement data (in units of counts) is corrected by first subtracting a stored offset trim value, then the gain is applied, then the ***Calibration:Vcell Offset:Vcell Offset*** (for cell voltage measurements) or the ***Calibration:Vdiv Offset:Vdiv Offset*** (for TOS, PACK, or LD voltage measurements) is subtracted, before the final voltage value is reported.

The factory trim values for the Cell Gain parameters can be read from the Cell Gain data memory registers while in FULLACCESS mode but not in CONFIG_UPDATE mode, if the data memory values have not been overwritten. While in CONFIG_UPDATE mode, the Cell Gain values will read back either with all zeros, if they have not been overwritten, or whatever values have been written to these registers. Upon exiting CONFIG_UPDATE mode, readback of the Cell Gain parameters will provide the values presently used in operation.

Further details on calibration procedures can be found in the *BQ769142 Technical Reference Manual*.

The effective fullscale digital range of the cell measurement is 5 × VREF1, and the effective fullscale digital range of the ADCIN measurement is 1.667 × VREF1, although the voltages applied for these measurements should be limited based on the specifications in セクション 7. Using a value for VREF1 of 1.212 V, the nominal gain for the cell measurements is 12120, while the nominal gain for the ADCIN measurements is 4040. The reported voltages are calculated as:

Cell # Voltage() = ***Calibration:Voltage:Cell # Gain*** × (16-bit ADC counts) / 65536 – ***Calibration:Vcell Offset:Vcell Offset***

Stack Voltage() = ***Calibration:Voltage:TOS Gain*** × (16-bit ADC counts) / 65536 – ***Calibration:Vdiv Offset:Vdiv Offset***

PACK Pin Voltage() = ***Calibration:Voltage:Pack Gain*** × (16-bit ADC counts) / 65536 – ***Calibration:Vdiv Offset:Vdiv Offset***

LD Pin Voltage() = ***Calibration:Voltage:LD Gain*** × (16-bit ADC counts) / 65536 – ***Calibration:Vdiv Offset:Vdiv Offset***

ADCIN Voltage = ***Calibration:Voltage:ADC Gain*** × (16-bit ADC counts) / 65536

Note

Cell # Voltage() and ***Calibration:Vcell Offset:Vcell Offset*** have units of mV. The divider voltages (*Stack Voltage()*, *PACK Pin Voltage()*, *LD Pin Voltage()*), and ***Calibration:Vdiv Offset:Vdiv Offset*** all have units of userV.

10.9 Voltage Calibration (COV and CUV Protections)

The BQ769142 device includes optional capabilities for the customer to calibrate the COV (cell overvoltage) and CUV (cell undervoltage) protection thresholds on the production line to improve threshold accuracy in the system, or to realize a threshold between the preset thresholds available from the device.

This calibration is performed while the device is in CONFIG_UPDATE mode. To calibrate the COV threshold, an external voltage is first applied between VC14 and VC13A that is equal to the desired COV threshold. Next, the host sends the *CAL_COV()* subcommand, which causes the BQ769142 device to perform a search for the appropriate calibration coefficients to realize a COV threshold at or close to the applied voltage level. When this search is completed, the resulting calibration coefficient is returned by the subcommand and automatically written into the ***Protections:COV:COV Threshold Override*** configuration parameter. If this parameter is nonzero, the device does not use its factory trim settings, but instead uses this value.

The CUV threshold is calibrated similarly; an external voltage is applied between VC14 and VC13A equal to the desired CUV threshold. Next, while in CONFIG_UPDATE mode, the *CAL_CUV()* subcommand is sent by the host, which causes the BQ769142 device to perform a search for the appropriate calibration coefficients to realize a CUV threshold at or close to the applied voltage level. When this search is completed, the resulting calibration coefficient is returned by the subcommand and automatically written into the ***Protections:CUV:CUV Threshold Override*** configuration parameter.

10.10 Current Calibration

The BQ769142 device coulomb counter ADC measures the differential voltage between the SRP and SRN pins to calculate the system current. The device includes the optional capability for the customer to calibrate the coulomb counter offset and current gain on the production line.

The ***Calibration:Current Offset:CC Offset*** configuration register contains an offset value in units of 32-bit coulomb counter ADC counts / ***Calibration:Current Offset:Coulomb Counter Offset Samples***. The value of ***Calibration:Current Offset:CC Offset*** / ***Calibration:Current Offset:Coulomb Counter Offset Samples*** is subtracted from the raw coulomb counter ADC counts, then the result is multiplied by ***Calibration:Current:CC Gain*** and scaled to provide the final result in units of userA.

The BQ769142 device uses the ***Calibration:Current:CC Gain*** and ***Calibration:Current:Capacity Gain*** configuration values to convert from the ADC value to current. The ***CC Gain*** reflects the value of the sense resistor used in the system, while the ***Capacity Gain*** is simply the ***CC Gain*** multiplied by 298261.6178.

Both the ***CC Gain*** and ***Capacity Gain*** are encoded using a 32-bit IEEE-754 floating point format. The effective value of the sense resistor is given by:

CC Gain = 7.4768 / (Rsense in mΩ)

10.11 Temperature Calibration

The BQ769142 device enables the customer to calibrate the internal as well as external temperature measurements on the production line, by storing an offset value which is added to the calculated measurement before reporting. A separate offset for each temperature measurement can be stored in the configuration registers shown below.

表 10-1. Temperature Calibration Settings

Section	Subsection	Register Description	Comment	Units
Calibration	Temperature	Internal Temp Offset		0.1 K
Calibration	Temperature	CFETOFF Temp Offset	CFETOFF pin thermistor	0.1 K
Calibration	Temperature	DFETOFF Temp Offset	DFETOFF pin thermistor	0.1 K
Calibration	Temperature	ALERT Temp Offset	ALERT pin thermistor	0.1 K
Calibration	Temperature	TS1 Temp Offset	TS1 pin thermistor	0.1 K
Calibration	Temperature	TS2 Temp Offset	TS2 pin thermistor	0.1 K
Calibration	Temperature	TS3 Temp Offset	TS3 pin thermistor	0.1 K
Calibration	Temperature	HDQ Temp Offset	HDQ pin thermistor	0.1 K
Calibration	Temperature	DCHG Temp Offset	DCHG pin thermistor	0.1 K
Calibration	Temperature	DDSG Temp Offset	DDSG pin thermistor	0.1 K

11 Primary and Secondary Protection Subsystems

11.1 Protections Overview

An extensive protection subsystem is integrated within BQ769142, which can monitor a variety of parameters, initiate protective actions, and autonomously recover based on conditions. The device also includes a wide range of flexibility, such that the device can be configured to monitor and initiate protective action, but with recovery controlled by the host processor, or such that the device only monitors and alerts the host processor whenever conditions warrant protective action, but with action and recovery fully controlled by the host processor.

The primary protection subsystem includes a suite of individual protections which can be individually enabled and configured, including cell undervoltage and overvoltage, overcurrent in charge, three separate overcurrent in discharge protections, short circuit current in discharge, cell overtemperature and undertemperature in charge and discharge, FET overtemperature, a host processor communication watchdog timeout, and PRECHARGE mode timeout. The cell undervoltage and overvoltage, overcurrent in charge, overcurrent in discharge 1 and 2, and short circuit in discharge protections are based on comparator thresholds, while the remaining protections (such as those involving temperature, host watchdog, and precharging) are based on firmware on the internal controller.

The device integrates NFET drivers for high-side CHG and DSG protection FETs, which can be configured in a series or parallel configuration. An integrated charge pump generates a voltage which is driven onto the NFET gates based on host command or the on-chip protection subsystem settings. Support is also included for high-side PFETs used to implement a precharge and predischarge functionality.

The secondary protection suite within the BQ769142 device can react to more serious faults and take action to permanently disable the pack, by initiating a Permanent Fail (PF). The secondary safety provides protection against safety cell undervoltage and overvoltage, safety overcurrent in charge and discharge, safety overtemperature for cells and FETs, excessive cell voltage imbalance, internal memory faults, and internal diagnostic failures.

When a Permanent Fail has occurred, the BQ769142 device can be configured to either simply provide a flag, or to indefinitely disable the protection FETs, or to assert the FUSE pin to permanently disable the pack. The FUSE pin can be used to blow an in-line fuse and also can monitor if a separate secondary protector IC has attempted to blow the fuse.

11.2 Primary Protections

The BQ769142 device integrates a broad suite of protections for battery management and provides the capability to enable individual protections, as well as to select which protections will result in autonomous control of the FETs. See the *BQ769142 Technical Reference Manual* for detailed descriptions of each protection function. The primary protection features include:

- Cell Undervoltage Protection
- Cell Overvoltage Protection
- Cell Overvoltage Latch Protection
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection (three tiers)
- Overcurrent in Discharge Latch Protection
- Short Circuit in Discharge Protection
- Short Circuit in Discharge Latch Protection
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Internal Undertemperature Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Internal Overtemperature Protection
- FET Overtemperature Protection
- Precharge Timeout Protection

- Host Watchdog Fault Protection

11.3 Secondary Protections

The BQ769142 device integrates a suite of secondary protection checks on battery operation and status that can trigger a Permanent Fail (PF) if conditions are considered so serious that the pack should be permanently disabled. The various PF checks can be enabled individually based on configuration settings, along with associated thresholds and delays for most checks. When a Permanent Fail has occurred, the BQ769142 device can be configured to either simply provide a flag, or to indefinitely disable the protection FETs, or to assert the FUSE pin to permanently disable the pack. The FUSE pin can be used to blow an in-line fuse and also can monitor if a separate secondary protector IC has attempted to blow the fuse.

Since the device stores Permanent Fail status in RAM, that status would be lost when the device resets. To mitigate this, the device can write Permanent Fail status to OTP based on configuration setting. OTP programming may be delayed in low-voltage and high-temperature conditions until OTP programming can reliably be accomplished.

Normally, a Permanent Fail causes the FETs to remain off indefinitely and the fuse may be blown. In that situation, no further action would be taken on further monitoring operations, and charging would no longer be possible. To avoid rapidly draining the battery, the device may be configured to enter DEEPSLEEP mode when a Permanent Fail occurs. Entrance to DEEPSLEEP mode will still be delayed until after fuse blow and OTP programming are completed, if those options are enabled.

When a Permanent Fail occurs, the device may be configured to either turn the REG1 and REG2 LDOs off, or to leave them in their present state. Once disabled, they may still be reenabled through command.

The Permanent Fail checks incorporate a programmable delay to avoid triggering a PF fault on an intermittent condition or measurement. When the threshold is first detected as being met or exceeded by an enabled PF check, the device will set a PF Alert signal, which can be monitored using commands and can also trigger an interrupt on the ALERT pin.

Note

The device only evaluates the conditions for Permanent Fail at one second intervals while in NORMAL and SLEEP modes, it does not continuously compare measurements to the Permanent Fail fault thresholds between intervals. Thus, it is possible for a condition to trigger a PF alert if detected over threshold, but even if the condition drops back below threshold briefly between the one second interval checks, the PF alert would not be cleared until it was detected below threshold at a periodic check.

For more details on the Permanent Fail checks implemented in the BQ769142, refer to the *BQ769142 Technical Reference Manual*. The secondary protection checks include:

- Safety Cell Undervoltage Permanent Fail
- Safety Cell Overvoltage Permanent Fail
- Safety Overcurrent in Charge Permanent Fail
- Safety Overcurrent in Discharge Permanent Fail
- Safety Overtemperature Permanent Fail
- Safety Overtemperature FET Permanent Fail
- Copper Deposition Permanent Fail
- Short Circuit in Discharge Latch Permanent Fail
- Voltage Imbalance Active Permanent Fail
- Voltage Imbalance at Rest Permanent Fail
- Second Level Protector Permanent Fail
- Discharge FET Permanent Fail
- Charge FET Permanent Fail
- OTP Memory Permanent Fail

- Data ROM Permanent Fail
- Instruction ROM Permanent Fail
- Internal LFO Permanent Fail
- Internal Voltage Reference Permanent Fail
- Internal VSS Measurement Permanent Fail
- Internal Stuck Hardware Mux Permanent Fail
- Commanded Permanent Fail
- Top of Stack Versus Cell Sum Permanent Fail

11.4 High-Side NFET Drivers

The BQ769142 device includes an integrated charge pump and high-side NFET drivers for driving CHG and DSG protection FETs. The charge pump uses an external capacitor connected between the BAT and CP1 pins that is charged to an overdrive voltage when the charge pump is enabled. Due to the time required for the charge pump to bring the overdrive voltage on the external CP1 pin to full voltage, it is recommended to leave the charge pump powered whenever it may be needed quickly to drive the CHG or DSG FETs.

The DSG FET driver includes a special option (denoted source follower mode) to drive the DSG FET with the BAT pin voltage during SLEEP mode. This capability is included to provide low power in SLEEP mode, when there is no significant charge or discharge current flowing. It is recommended to keep the charge pump enabled even when the source follower mode is enabled, so whenever a discharge current is detected, the device can quickly transition to driving the DSG FET using the charge pump voltage. The source follower mode is enabled using a configuration setting and is not intended to be used when significant charging or discharging current is flowing, since the FET will exhibit a large drain-source voltage and may undergo excessive heating.

The overdrive level of the charge pump voltage can be set to 5.5 V or 11 V, based on the configuration setting. In general, the 5.5-V setting results in lower power dissipation when a FET is being driven, while the higher 11-V overdrive reduces the on-resistance of the FET. If a FET exhibits significant gate leakage current when driven at the higher overdrive level, this can result in a higher device current for the charge pump to support this. In this case, using the lower overdrive level can reduce the leakage current and thus the device current.

The BQ769142 device supports a system with FETs in a series or parallel configuration, where the parallel configuration includes a separate path for the charger connection versus the discharge (load) connection. The control logic for the device operates slightly differently in these two cases, which is set based on the configuration setting.

The FET drivers in the BQ769142 device can be controlled in several different manner, depending on customer requirements:

Fully autonomous

The BQ769142 device can detect protection faults and autonomously disable the FETs, monitor for a recovery condition, and autonomously reenable the FETs, without requiring any host processor involvement.

Partially autonomous

The BQ769142 device can detect protection faults and autonomously disable the FETs. When the host receives an interrupt and recognizes the fault, the host can send commands across the digital communications interface to keep the FETs off until the host decides to release them.

Alternatively, the host can assert the CFETOFF or DFETOFF pins to keep the FETs off. As long as these pins are asserted, the FETs are blocked from being reenabled. When these pins are deasserted, the BQ769142 will reenable the FETs if nothing is blocking them being reenabled (such as fault conditions still present, or the CFETOFF or DFETOFF pins are asserted).

Manual control

The BQ769142 device can detect protection faults and provide an interrupt to a host processor over the ALERT pin. The host processor can read the status information of the fault over the communication bus (if desired) and can quickly force the CHG or DSG FETs off by driving the CFETOFF or DFETOFF pins from the host processor, or commands over the digital communications interface.

When the host decides to allow the FETs to turn on again, it writes the appropriate command or deasserts the CFETOFF and DFETOFF pins, and the BQ769142 device will reenable the FETs if nothing is blocking them being reenabled.

11.5 Protection FETs Configuration and Control

11.5.1 FET Configuration

The BQ769142 device supports a series configuration and a parallel configuration for the protection FETs in the system, as well as a system that does not use one or both FETs. When a series FET configuration is used, the BQ769142 device provides body diode protection for the case when one FET is off and one FET is on.

If the CHG FET is off, the DSG or PDSG FET is on, and a discharge current greater in magnitude than a programmable threshold (that is, a significant discharging current) is detected, the device will turn on the CHG FET, to avoid current flowing through the CHG FET body diode and damaging the FET. When the current rises above the threshold (that is, less discharge current flowing), the CHG FET will be turned off again if the reasons for its turn-off are still present.

If the DSG FET is off, the CHG or PCHG FET is on, and a current in excess of a programmable threshold (that is, a significant charging current) is detected, the device turns on the DSG FET to avoid current flowing through the DSG FET body diode and damaging the FET. When the current falls below the threshold (that is, less charging current flowing), the DSG FET is turned off again if the reasons for its turn-off are still present.

When a parallel configuration is used, the body diode protection is disabled.

11.5.2 PRECHARGE and PREDISCHARGE Modes

The BQ769142 device includes precharge functionality, which can be used to reduce the charging current for an undervoltage battery by charging using a high-side PCHG PFET (driven from the PCHG pin) with series resistor until the battery reaches a programmable voltage level. When the minimum cell voltage is less than a programmable threshold, the PCHG FET will be used for charging.

The device also supports predischarge functionality, which can be used to reduce inrush current when the load is initially powered, by first enabling a high-side PDSG PFET (driven from the PDSG pin) with series resistor, which enables the load to slowly charge. If PREDISCHARGE mode is enabled, whenever the DSG FET is turned on to power the load, the device will first enable the PDSG FET, then transition to turn on the DSG FET and turn off the PDSG FET.

The PCHG and PDSG drivers are limited in the current they can sink while enabled. As such, it is recommended to use 1 MΩ or larger resistance across the FET gate-source.

11.6 Load Detect Functionality

When a short circuit in discharge latch or overcurrent in discharge latch protection fault occurs and the DSG FET is off, the device can be configured to recover when load removal is detected. This feature is useful if the system has a removable pack, such that the user can remove the pack from the system when a fault occurs, or if the effective system load that remains on the battery pack is higher than ~20-kΩ when the DSG FET is disabled. The device periodically enables a current source out of the LD pin and recovers the fault if a voltage is detected at the LD pin above a 4-V level. If a low-impedance load is still present on the pack, the voltage the device measures on the LD pin is generally below 4 V, preventing recovery based on load detect. If the pack was removed from the system and the effective load is high, such that the current source generates a voltage on the LD pin above a 4-V level, then the device can recover from the fault.

Note

Typically, a 10-kΩ resistor is connected between the PACK+ terminal and the LD pin. This resistance should be understood when considering the load impedance. The load detect current is enabled for a programmable time duration, then is disabled for another programmable time duration, with this sequence repeating until the load is detected as removed or it times out.

12 Device Hardware Features

12.1 Voltage References

The BQ769142 device includes two voltage references, V_{REF1} and V_{REF2}, with V_{REF1} used by the voltage ADC for most measurements except external thermistors. V_{REF2} is used by the integrated 1.8 V LDO, internal oscillators, and integrated coulomb counter ADC. The value of V_{REF2} can be measured indirectly by the voltage ADC's measurement of the REG18 LDO voltage while using V_{REF1} for diagnostic purposes.

12.2 ADC Multiplexer

The ADC multiplexer connects various signals to the voltage ADC, including the individual differential cell voltage pins, the on-chip temperature sensor, the biased thermistor pins, the REG18 LDO voltage, the VSS pin voltage, and internal dividers connected to the VC14, PACK, and LD pins.

12.3 LDOs

The BQ769142 device contains an integrated 1.8-V LDO (REG18) that provides a regulated 1.8 V supply voltage for the device's internal circuitry and digital logic. This regulator uses an external capacitor connected to the REG18 pin, and it should only be used for internal circuitry.

The device also integrates two separately programmable LDOs (REG1 and REG2) for external circuitry, such as a host processor or external transceiver circuitry, which can be programmed to independent output voltages. The REG1 and REG2 LDOs take their input from the REGIN pin, with this voltage either provided externally or generated by an on-chip preregulator (referred to as REG0). The REG1 and REG2 LDOs can provide an output current of up to 45 mA each.

12.3.1 Preregulator Control

The REG1 and REG2 LDOs take their input from the REGIN pin, which should be approximately 5.5 V. This REGIN pin voltage can be supplied externally (such as by a separate DC/DC converter) or using the integrated voltage preregulator (referring to as REG0), which drives the base of an external NPN BJT (using the BREG pin) to provide the 5.5-V REGIN pin voltage. When the preregulator is used, special care should be taken to ensure the device retains sufficient voltage on its BAT pin, per the specifications in *Specifications*.

Note

The system designer should ensure the external BJT can tolerate the peak power that may be dissipated in it under maximum load expected on REG1 and REG2. If the maximum stack voltage is 80 V, then the BJT has a collector-emitter voltage of approximately 75 V, thereby dissipating 6.75 W if REG1 and REG2 are both used to support a 45 mA load.

There is a diode connection between the REGIN pin (anode) and the BAT pin (cathode), so the voltage on REGIN should not exceed the voltage on BAT.

12.3.2 REG1 and REG2 LDO Controls

The REG1 and REG2 LDOs in the BQ769142 device are for customer use, and their output voltages can be programmed independently to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V. The REG1 and REG2 LDOs and the REG0 preregulator are disabled by default in the BQ769142 device. While in SHUTDOWN mode, the REG1 and REG2 pins have ≈10-MΩ resistances to VSS to discharge any output capacitance. While in other power modes, when REG1 and REG2 are powered down, they are pulled to VSS with an internal resistance of ≈2.5 kΩ. If pullup resistors for serial communications are connected to the REG1 voltage output, the REG1 voltage can be

overdriven from an external voltage supply on the manufacturing line to enable communications with the device. The BQ769142 device can then be programmed to enable REG0 and REG1 with the desired configuration, and this setting can be programmed into OTP memory. Thus, at each later power-up, the device will autonomously load the OTP settings and enable the LDO as configured, without requiring communications first.

12.4 Standalone Versus Host Interface

The BQ769142 device can be configured to operate in a completely STANDALONE mode, without any host processor in the system, or together with a host processor. If in STANDALONE mode, the device can monitor conditions, control FETs and an in-line fuse based on threshold settings, and recover FETs when conditions allow, all without requiring any interaction with an external processor. If a host processor is present, the device can still be configured to operate fully autonomously, while the host processor can read measurements and exercise control as desired. In addition, the device can be configured for manual host control, such that the device can monitor and provide a flag when a protection alert or fault has occurred, but will rely on the host to disable FETs.

The host processor can interface with the BQ769142 device through a serial bus, as well as selected pin controls. Serial bus communication through I^2C (supporting speeds up to 400 kHz), SPI, or HDQ is available, with the serial bus configured for I^2C by default in the BQ769142, while the default communications mode may differ for other versions of the device. The pin controls available include RST_SHUT, ALERT, CFETOFF, DFETOFF, DDSG, and DCHG, which are described in detail below.

12.5 Multifunction Pin Controls

The BQ769142 device provides flexibility regarding the multifunction pins on the device, which includes the TS1, TS2, TS3, CFETOFF, DFETOFF, ALERT, HDQ, DCHG, and DDSG pins. Several of the pins can be used as active-high outputs with configurable output level. The digital output driver for these pins can be configured to drive an output powered from the REG1 LDO or from the internal REG18 LDO, and thus when asserted active-high will drive out the voltage of the selected LDO.

Note: the REG18 LDO is not capable of driving high current levels, so it is recommended to only use this LDO to provide a digital output if it will be driving a very high resistance (such as > 1 MΩ) or light capacitive load. Otherwise, the REG1 should be powered and used to drive the output signal.

The options supported on each pin include:

ALERT

Alarm interrupt output

HDQ communications

CFETOFF

Input to control the CHG FET (that is, CFETOFF functionality)

DFETOFF

Input to control the DSG FET (that is, DFETOFF functionality)

Input to control both the DSG and CHG FETs (that is, BOTHOFF functionality)

HDQ

HDQ communications

SPI MOSI pin

DCHG

DCHG functionality—A logic-level output corresponding to a fault that would normally cause the CHG driver to be disabled

DDSG

DDSG functionality—A logic-level output corresponding to a fault that would normally cause the DSG driver to be disabled

ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG

General purpose digital output

Can be driven high or low by command

Can be configured for an active-high output to be driven from the REG1 LDO or the REG18 LDO

Can be configured to have a weak pulldown to VSS or weak pullup to REG1 enabled continuously

ALERT, CFETOFF, DFETOFF, TS1, TS2, TS3, HDQ, DCHG, and DDSG

Thermistor temperature measurement

A thermistor can be attached between the pin and VSS.

ADCIN

Pin can be used for general purpose ADC measurement.

12.6 RST_SHUT Pin Operation

The RST_SHUT pin provides a simple way to reset or shutdown the BQ769142 device without needing to use serial bus communication. During normal operation, the RST_SHUT pin should be driven low. When the pin is driven high, the device will immediately reset most of the digital logic, including that associated with the serial communications bus. However, it does not reset the logic that holds the state of the protection FETs and FUSE, these remain as they were before the pin was driven high. If the pin continues to be driven high for 1 second, the device will then transition into SHUTDOWN mode, which involves disabling external protection FETs, and powering off the internal oscillators, the REG18 LDO, the on-chip preregulator, and the REG1 and REG2 LDOs.

12.7 CFETOFF, DFETOFF, and BOTHOFF Pin Functionality

The BQ769142 device includes two pins (CFETOFF and DFETOFF) which can be used to disable the protection FET drivers quickly, without going through the host serial communications interface. When the selected pin is asserted, the device disables the respective protection FET. Note: when the selected pin is deasserted, the respective FET will only be enabled if there are no other items blocking them being reenabled, such as if the host also sent a command to disable the FETs using the serial communications interface after setting the selected pin. Both the CFETOFF and DFETOFF pins can be used for other functions if the FET turnoff feature is not required.

The CFETOFF pin can optionally be used to disable the CHG and PCHG FETs, and the DFETOFF pin can optionally be used to disable the DSG and PDSG FETs. The device also includes the option to configure the DFETOFF pin as BOTHOFF functionality, such that if that pin is asserted, the CHG, PCHG, DSG, and PDSG FETs will be disabled. This allows the CFETOFF pin to be used for an additional thermistor in the system, while still providing pin control to disable the FETs.

The CFETOFF or BOTHOFF functionality disables both the CHG FET and the PCHG FET when asserted.

The DFETOFF or BOTHOFF functionality disables both the DSG FET and the PDSG FET when asserted.

12.8 ALERT Pin Operation

The ALERT pin is a multifunction pin that can be configured either as ALERT (to provide an interrupt to a host processor), a thermistor input, a general purpose ADC input, a general purpose digital output, or an HDQ serial communication interface. The pin can be configured as active-high, active-low, or open-drain to accommodate different system design preferences. When configured as the HDQ interface pin, the pin operates in open-drain mode.

When the pin is configured to drive an active high output, the output voltage is driven from either the REG18 1.8 V LDO or the REG1 LDO (which can be programmed from 1.8 V to 5.0 V).

Note

If a DC or significant transient current is driven by this pin, then the output should be configured to drive using the REG1 LDO, not the REG18 LDO.

The BQ769142 device includes functionality to generate an alarm signal at the ALERT pin, which can be used as an interrupt to a host processor. When used for the alarm function, the pin can be programmed to drive the signal as an active-low or hi-Z signal, an active-high or low signal, or an active-low or high signal (that is, inverted polarity). The alarm function within the BQ769142 device includes a programmable mask, to allow the customer to decide which of many flags or events can trigger an alarm.

12.9 DDSG and DCHG Pin Operation

The BQ769142 device includes two multifunction pins, DDSG and DCHG, which can be configured as logic-level outputs to provide a fault-related signal to a host processor or external circuitry (that is, DDSG and DCHG functionality), as a thermistor input, a general purpose ADC input, or a general purpose digital output.

When used as a digital output, the pins can be configured to drive an active high output, with the output voltage driven from either the REG18 1.8 V LDO or the REG1 LDO (which can be programmed from 1.8 V to 5.0 V). Note: if a DC or significant transient current may be driven by a pin, then the output should be configured to drive using the REG1 LDO, not the REG18 LDO.

When the pins are configured for DDSG and DCHG functionality, they provide signals related to protection faults that (on the DCHG pin) would normally cause the CHG driver to be disabled, or (on the DDSG pin) would normally cause the DSG driver to be disabled. These signals can be used to control external protection circuitry, if the integrated high-side NFET drivers will not be used in the system. They can also be used as interrupts in manual FET control mode for the host processor to decide whether to disable the FETs through commands or using the CFETOFF and DFETOFF pins.

12.10 Fuse Drive

The FUSE pin on the BQ769142 device can be used to blow a chemical fuse in the presence of a Permanent Fail (PF), as well as to determine if an external secondary protector in the system has detected a fault and is attempting to blow the fuse itself. The pin can drive the gate of an NFET, which can be combined with the drive from an external secondary protector, as shown in 図 12-1. When the FUSE pin is not asserted by the BQ769142 device, it remains in a high-impedance state and detects a voltage applied at the pin by a secondary protector. The device can be configured to generate a PF if it detects a high signal at the FUSE pin.

The device can be configured to blow the fuse when a PF occurs. In this case, the device will only attempt to blow the fuse if the stack voltage is above a programmed threshold, based on a system configuration with the fuse placed between the top of stack and the high-side protection FETs. If instead the fuse is placed between the FETs and the PACK+ connector, then the device bases its decision on the PACK pin voltage (based on configuration setting). This voltage threshold check may be disregarded under certain special cases, as described in the *BQ769142 Technical Reference Manual* .

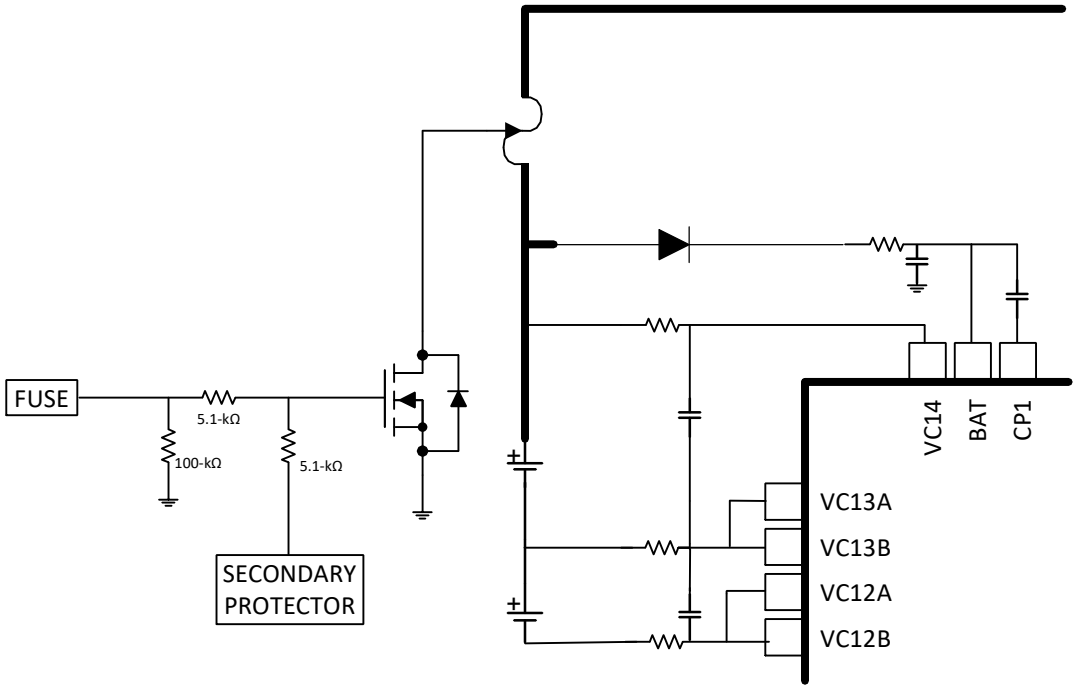


図 12-1. FUSE Pin Operation

12.11 Cell Open Wire

The BQ769142 device supports detection of a broken connection between a cell in the pack and the cell attachment to the PCB containing BQ769142. Without this check, the voltage at the cell input pin of the BQ769142 device may persist for some time on the board-level capacitor, leading to incorrect voltage readings. The Cell Open Wire detection in the BQ769142 device operates by enabling a small current source from each cell to VSS at programmable intervals. If a cell input pin is floating due to an open wire condition, this current discharges the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage eventually triggers a protection fault on that particular cell and the cell above it. Eventually, the voltage drops low enough to trigger a Permanent Fail on the particular cell and the cell above it.

The Cell Open Wire current is enabled at a periodic interval set by configuration register. The current source is enabled once every interval for a duration of the ADC measurement time (which is 3 ms by default). This provides programmability in the average current drawn from ≈0.65 nA to ≈165 nA, based on the typical current level of 55 µA.

Note

The Cell Open Wire check can create a cell imbalance, so the settings should be selected appropriately.

12.12 Low Frequency Oscillator

The low frequency oscillator (LFO) in the BQ769142 device operates continuously while in NORMAL and SLEEP modes, and can be configured to remain powered or shutdown (except when needed) during DEEPSLEEP mode. The LFO runs at ≈262.144 kHz during NORMAL mode, and reduces to ≈32.768 kHz in SLEEP or DEEPSLEEP modes. The LFO is trimmed during manufacturing to meet the specified accuracy across temperature.

12.13 High Frequency Oscillator

The high frequency oscillator (HFO) in the BQ769142 device operates at 16.78 MHz and is frequency locked to the LFO. The HFO powers up as needed for internal logic functions.

13 Device Functional Modes

13.1 Overview

This device supports four functional modes to support optimized features and power dissipation, with the device able to transition between modes either autonomously or controlled by a host processor.

- NORMAL mode: In this mode, the device performs frequent measurements of system current, cell voltages, internal and thermistor temperature, and various other voltages, operates protections as configured, and provides data and status updates.
- SLEEP mode: In this mode, the DSG FET is enabled, the CHG FET can optionally be disabled, and the device performs measurements, calculations, and data updates in adjustable time intervals. Battery protections are still enabled. Between the measurement intervals, the device is operating in a reduced power stage to minimize total average current consumption.
- DEEPSLEEP mode: In this mode, the CHG, PCHG, DSG, and PDSG FETs are disabled, all battery protections are disabled, and no current or voltage measurements are taken. The REG1 and REG2 LDOs can be kept powered, in order to maintain power to external circuitry, such as a host processor.
- SHUTDOWN mode: The device is completely disabled (including the internal, REG1, and REG2 LDOs), the CHG, PCHG, DSG, and PDSG FETs are all disabled, all battery protections are disabled, and no measurements are taken. This is the lowest power state of the device, which may be used for shipment or long-term storage. All register settings are lost when in SHUTDOWN mode.

The device also includes a CONFIG_UPDATE mode, which is used for parameter updates. Device Functional Modes shows the transitions between the functional modes.

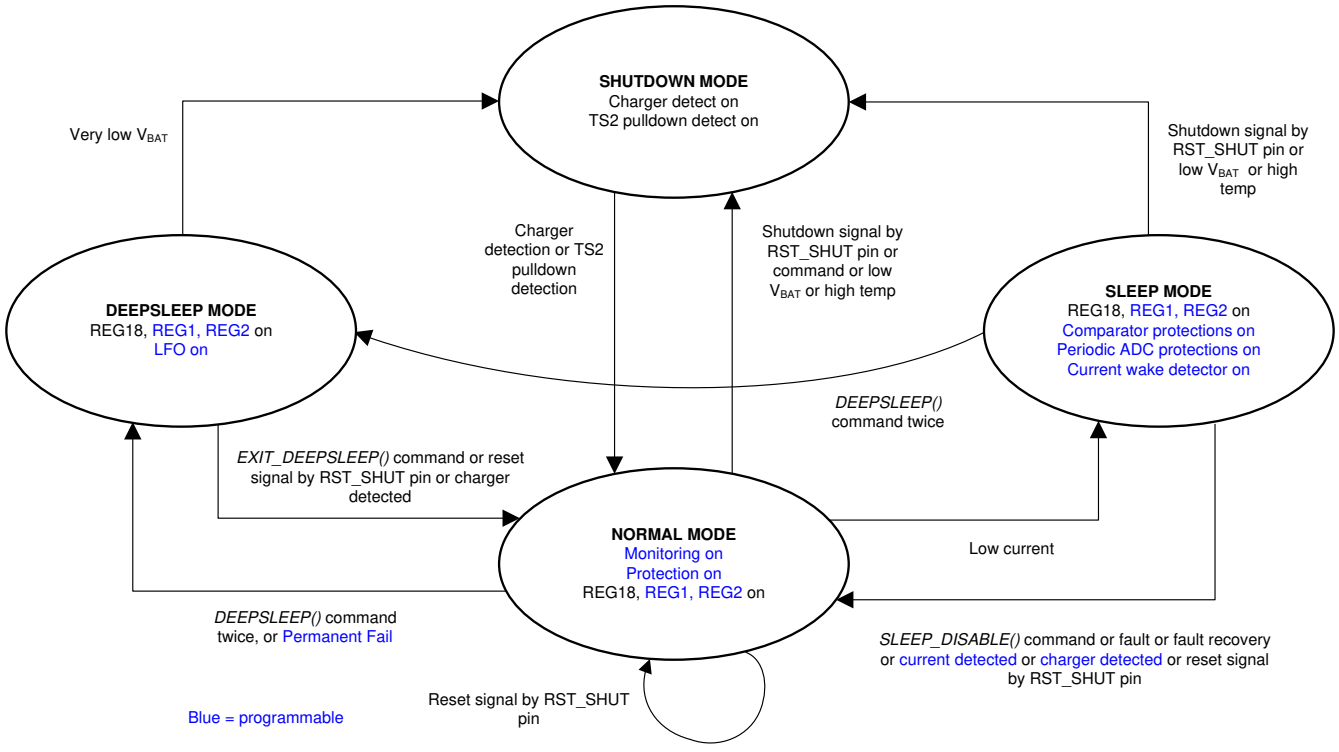


図 13-1. Device Functional Modes

13.2 NORMAL Mode

NORMAL mode is the highest performance mode of the device, in which the device makes regular measurements of voltage, current, and temperature, the LFO (low frequency oscillator) is operating, and the internal processor powers up (as needed) for data processing and control. Full battery protections are operating, based on device configuration settings. System current is measured at intervals of 3 ms, with cell voltages measured at intervals of 63 ms or slower, depending on the configuration. The device also provides a configuration bit that causes the conversion speed for both voltages and CC2 Current to be doubled, with a reduction in measurement resolution.

The device is generally in NORMAL mode when any active charging or discharging is underway. When the CC1 Current measurement falls below a programmable current threshold, the system is considered in RELAX mode, and the BQ769142 device can autonomously transition into SLEEP mode, depending on the configuration.

13.3 SLEEP Mode

SLEEP mode is a reduced functionality state that can be optionally used to reduce power dissipation when there is little or no system load current or charging in progress, but still provides voltage at the battery pack terminals to keep the system alive. At initial power up, a configuration bit determines whether the device can enter SLEEP mode. After initialization, SLEEP mode can be allowed or disallowed using subcommands. Status bits are provided to indicate whether the device is presently allowed to enter SLEEP mode or not, and whether it is presently in SLEEP mode or not.

When the magnitude of the CC1 Current measurement falls below a programmable current threshold, the system is considered in relax mode, and the BQ769142 device will autonomously transition into SLEEP mode, if settings permit. During SLEEP mode, comparator-based protections operate the same as during NORMAL mode. ADC-based current, voltage, and temperature measurements are taken at programmable intervals. All temperature protections use the ADC measurements taken at these intervals, so they will update at a reduced rate during SLEEP mode.

The BQ769142 device exits SLEEP mode if a protection fault occurs, if current begins flowing, if a charger is attached, if forced by a subcommand, or if the RST_SHUT pin is asserted for less than 1 second. When exiting based on current flow, the device will quickly enable the FETs (if the CHG FET was off, or the DSG FET was in source follower mode), but the standard measurement loop is not restarted until the next 1-s boundary occurs within the device timing. Therefore, new data may not be available for up to ≈1 second after the device exits SLEEP mode.

The coulomb counter ADC operates in a reduced power and speed mode to monitor current during SLEEP mode. The current is measured every 12 ms and, if it exceeds a programmable threshold in magnitude, the device quickly transitions back to NORMAL mode. In addition to this check, if the CC1 Current measurement taken at each programmed interval exceeds this threshold, the device will exit SLEEP mode.

The device monitors the PACK pin voltage and the top-of-stack voltage at each programmed measurement interval. If the PACK pin voltage is higher than the top-of-stack voltage by more than a programmable delta and the top-of-stack voltage is less than a programmed threshold, the device will exit SLEEP mode. The BQ769142 device also includes a hysteresis on the SLEEP mode entrance, in order to avoid the device quickly entering and exiting SLEEP mode based on a dynamic load. After transitioning to NORMAL mode, the device will not enter SLEEP mode again for a number of seconds given by the hysteresis setting.

During SLEEP mode, the DSG FET can be driven either using the charge pump or in source-follower mode, as described in セクション 11.4. The CHG FET can be disabled or driven using the charge pump, based on the configuration setting.

13.4 DEEPSLEEP Mode

The BQ769142 device integrates a DEEPSLEEP mode, which is a low power mode that allows the REG1 and REG2 LDOs to remain powered, but disables other subsystems. In this mode, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, and all voltage, current, and temperature measurements are disabled.

DEEPSLEEP mode can be entered by sending a subcommand over the serial communications interface. The device exits DEEPSLEEP mode and returns to NORMAL mode if directed by a subcommand, if the RST_SHUT pin is asserted for less than 1 second, or if a charger is attached (which is detected by the voltage on the LD pin rising from below $V_{WAKEONLD}$ to exceed it). In addition, if the BAT pin voltage falls below $V_{PORA} – V_{PORA\_HYS}$, the device transitions to SHUTDOWN mode.

When the device exits DEEPSLEEP mode, it first completes a full measurement loop and evaluates conditions relative to enabled protections, to ensure that conditions are acceptable to proceed to NORMAL mode. This may take ≈250 ms plus the time for the measurement loop to complete.

The REG1 and REG2 LDOs will maintain their power state when entering DEEPSLEEP mode based on the configuration setting. The device also provides the ability to keep the LFO running while in DEEPSLEEP mode, which allows for a faster responsiveness to communications and transition back to NORMAL mode, but will consume additional power.

Other than sending a subcommand to exit DEEPSLEEP mode, communications with the device over the serial interface will not cause it to exit DEEPSLEEP mode. However, since no measurements are taken while in DEEPSLEEP mode, there is no new information available for readout.

13.5 SHUTDOWN Mode

SHUTDOWN mode is the lowest power mode of the BQ769142, which can be used for shipping or long-term storage. In this mode, the device loses all register state information, the internal logic is powered down, and the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, all voltage, current, and temperature measurements are disabled, and no communications are supported. When the device exits SHUTDOWN, it boots and reads parameters stored in OTP (if that has been written). If the OTP has not been written, the device powers up with default settings, and then settings can be changed by the host writing device registers.

Entering SHUTDOWN mode involves a sequence of steps. The sequence can be initiated manually through the serial communications interface. The device can also be configured to enter SHUTDOWN mode automatically based on the top of stack voltage or the minimum cell voltage. If the top-of-stack voltage falls below a programmed stack voltage threshold, or if the minimum cell voltage falls below a programmed cell voltage threshold, the SHUTDOWN mode sequence is automatically initiated. The shutdown based on cell voltage does not apply to cell input pins being used to measure interconnect.

While the BQ769142 device is in NORMAL mode or SLEEP mode, the device can also be configured to enter SHUTDOWN mode if the internal temperature measurement exceeds a programmed temperature threshold for a programmed delay.

When the SHUTDOWN mode sequence is initiated by subcommand or the RST_SHUT pin driven high for 1 second, the device waits for a delay then disables the protection FETs. After the delay from when the sequence begins, the device enters SHUTDOWN mode. However, if the voltage on the LD pin is still above the $V_{WAKEONLD}$ level, shutdown will be delayed until the voltage on LD falls below that level.

While the device is in SHUTDOWN mode, ≈5 voltage is provided at the TS2 pin with high source impedance. If the TS2 pin is pulled low, such as by a switch to VSS, or if a voltage is applied at the LD pin above $V_{WAKEONLD}$ (such as when a charger is attached in series FET configuration), the device exits SHUTDOWN mode.

Note

If a thermistor is attached from the TS2 pin to VSS, this may prevent the device from fully entering SHUTDOWN mode.

As a countermeasure to avoid an unintentional wake from SHUTDOWN mode when putting the BQ769142 device into long-term storage, the device can be configured to automatically reenter SHUTDOWN mode after a programmed number of minutes.

The BQ769142 device performs periodic memory integrity checks and forces a watchdog reset if any corruption is detected. To avoid a cycle of resets in the case of a memory fault, the device enters SHUTDOWN mode rather

than reset if a memory error is detected within a programmed number of seconds after a watchdog reset has occurred.

When the device is wakened from SHUTDOWN, it generally requires approximately 200 ms–300 ms for the internal circuitry to power up, load settings from OTP memory, perform initial measurements, evaluate those relative to enabled protections, then to enable FETs if conditions allow. This can be much longer, depending on settings.

The BQ769142 device integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device automatically begins the sequence to enter SHUTDOWN mode if this functionality is enabled through configuration.

13.6 CONFIG_UPDATE Mode

The BQ769142 device uses a special CONFIG_UPDATE mode to make changes to the data memory settings. If changes were made to the data memory settings while the firmware was in normal operation, it could result in an unexpected operation or consequences if settings used by the firmware changed in the midst of operation. When changes to the data memory settings are needed (which generally should only be done on the customer manufacturing line or in an offline condition), the host should put the device into CONFIG_UPDATE mode, modify settings as required, then exit CONFIG_UPDATE mode. See the *BQ769142 Technical Reference Manual* for more details.

When in CONFIG_UPDATE mode, the device stops normal firmware operation and stops all measurements and protection monitoring. The host can then make changes to data memory settings (either writing registers directly into RAM, or instructing the device to program the RAM data into OTP). After changes are complete, the host then exits CONFIG_UPDATE mode, at which point the device restarts normal firmware operation using the new data memory settings.

14 Serial Communications Interface

14.1 Serial Communications Overview

The BQ769142 device integrates three serial communication interfaces—an I^2C bus, which supports 100-kHz and 400-kHz modes with an optional CRC check, an SPI bus with an optional CRC check, and a single-wire HDQ interface. The default configuration for the BQ769142 device is I^2C mode, while other versions of the device may have a different default configuration. The communication mode can be changed by programming either the register or OTP configuration. The customer can program the device's integrated OTP on the manufacturing line to set the desired communications speed and protocol to be used at power up in operation.

14.2 I^2C Communications

The I^2C serial communications interface in the BQ769142 device acts as a slave device and supports rates up to 400 kHz with an optional CRC check. If the OTP has not been programmed, the BQ769142 device will initially power up by default in 400 kHz I^2C mode, although other versions of the device may initially power up in a different mode, as described in the *Device Comparison Table*. The OTP setting can be programmed on the manufacturing line, then when the device powers up, it will automatically enter the selected mode per OTP setting. The host can also change the I^2C speed setting while in CONFIG_UPDATE mode, then the new speed setting will take effect upon exit of CONFIG_UPDATE mode. Alternatively, the host can use the *SWAP_TO_I2C()* subcommand to change the communications interface to I^2C immediately.

The I^2C device address (as an 8-bit value including slave address and R/W bit) is set by default as 0x10 (write), 0x11 (read), which can be changed by configuration setting.

The communications interface includes programmable timeout capability, this should only be used if the bus will be operating at 100 kHz or 400 kHz. If this is enabled with the device set to 100 kHz mode, then the device will reset the communications interface logic if a clock is detected low longer than a $t_{TIMEOUT}$ of 25 ms to 35 ms, or if the cumulative clock low slave extend time exceeds ≈25 ms, or if the cumulative clock low master extend time exceeds 10 ms. If the timeouts are enabled with the device set to 400 kHz mode, then the device will reset the communications interface logic if a clock is detected low longer than $t_{TIMEOUT}$ of 5 ms to 20 ms. The bus also

includes a long-term timeout if the SCL pin is detected low for more than 2 seconds, which applies whether or not the timeouts above are enabled.

I²C Write shows an I²C write transaction. Block writes are allowed by sending additional data bytes before the Stop. The I²C logic autoincrement the register address after each data byte.

When enabled, the CRC is calculated as follows:

- In a single-byte write transaction, the CRC is calculated over the slave address, register address, and data.
- In a block write transaction, the CRC for the first data byte is calculated over the slave address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the slave detects an invalid CRC, the I²C slave will NACK the CRC, which causes the I²C slave to go to an idle state.

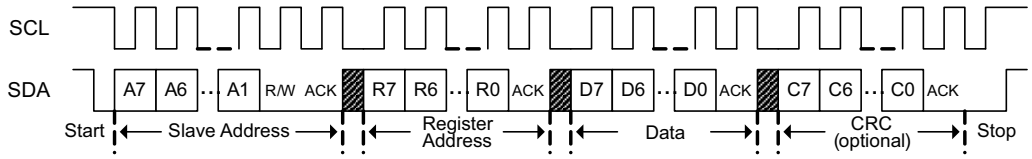


図 14-1. I²C Write

I²C Read with Repeated Start shows a read transaction using a Repeated Start.

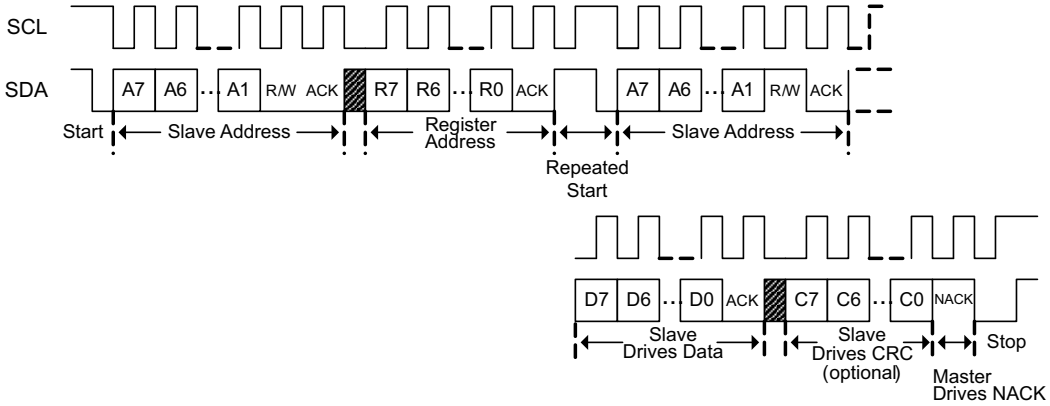


図 14-2. I²C Read with Repeated Start

I²C Read without Repeated Start shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read, the master ACKs each data byte except the last and continues to clock the interface. The I²C block will auto-increment the register address after each data byte.

When enabled, the CRC for a read transaction is calculated as follows:

- In a single-byte read transaction, the CRC is calculated beginning at the first start, so will include the slave address, the register address, then the slave address with read bit set, then the data byte.
- In a block read transaction, the CRC for the first data byte is calculated beginning at the first start and will include the slave address, the register address, then the slave address with read bit set, then the data byte. The CRC resets after each data byte and after each stop. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the master detects an invalid CRC, the I²C master will NACK the CRC, which causes the I²C slave to go to an idle state.

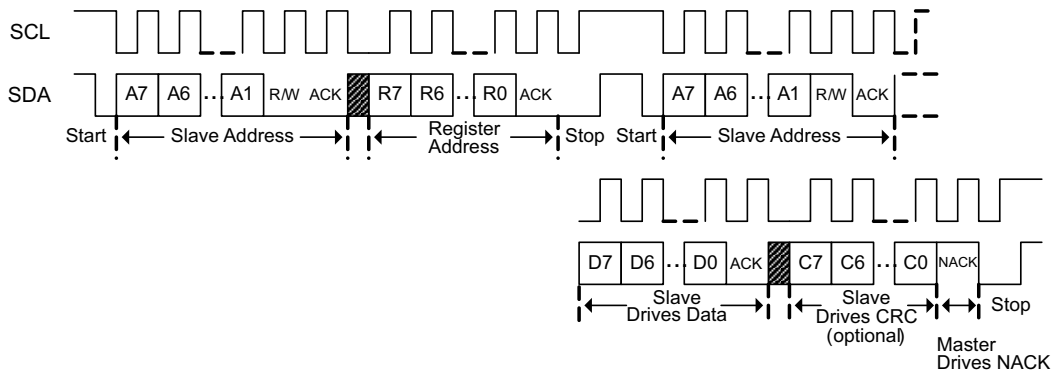


図 14-3. I²C Read Without Repeated Start

14.3 SPI Communications

The SPI interface in the BQ769142 device operates as a slave-only interface with an optional CRC check. If the OTP has not been programmed, the BQ769142 device initially powers up by default in 400 kHz I²C mode, while other device versions will initially power up by default in SPI mode with CRC enabled, as described in the *Device Comparison Table*. The OTP setting to select SPI mode can be programmed into the BQ769142 on the manufacturing line, then when the device powers up, it automatically enters SPI mode. The host can also change the serial communication setting while in CONFIG_UPDATE mode, although the device will not immediately change communication mode upon exit of CONFIG_UPDATE mode to avoid losing communications during evaluation or production. The host can reset the device or write the *SWAP_TO_SPI()* subcommand to change the communications interface to SPI immediately.

The SPI interface logic operates with clock polarity (CPOL) = 0 and clock phase (CPHA) = 0, as shown in the figure below.

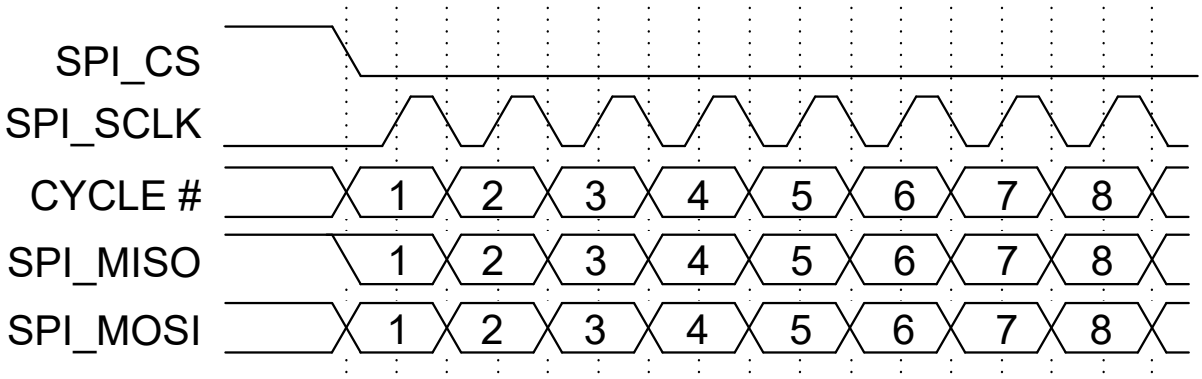


図 14-4. SPI with CPOL = 0 and CPHA = 0

The device also includes an optional 8-bit CRC using polynomial x^8+x^2+x+1. The interface must use 16-bit transactions if CRC is not enabled, and must use 24-bit transactions when CRC is enabled. CRC mode is enabled or disabled based on the setting of ***Settings:Configuration:Comm Type***. Based on configuration settings, the logic will:

(a) Only work with CRC, will not accept data without valid CRC, or

(b) Only accept transactions without CRC (so the host must only clock 16-bits per transaction, the device will detect an error if more or less clocks are sent).

If the host performs a write with CRC and the CRC is not correct, then the incoming data is not transferred to the incoming buffer, and the outgoing buffer (used for the next transaction) is also reset to 0xFFFF. This transaction

is considered invalid. On the next transaction, the CRC (if clocked out) will be 0xAA, so the 0xFFFFAA will indicate to the master that a CRC error was detected.

The internal oscillator in the BQ769142 device may not be running when the host initiates a transaction (for example, this can occur if the device is in SLEEP mode). If this occurs, the interface will drive out 0xFFFF on SPI_MISO for the first 16-bits clocked out. It will also drive out 0xFF for the third (CRC) byte as well, if CRC is enabled. So the 0xFFFF or 0xFFFFFF will indicate to the master that the internal oscillator is not ready yet.

The device will automatically wake the internal oscillator at a falling edge of SPI_CS, but it may take up to 50 µs to stabilize and be available for use to the SPI interface logic. The address 0x7F used in the device is defined in such a manner that there should be no valid transaction to write 0xFF into this address. Thus the two-byte pattern 0xFFFF should never occur as a valid sequence in the first two bytes of a transaction (that is, it is only used as a flag that something is wrong, similar to an I^2C NACK).

Due to the delay in the HFO powering up if initially off, the device includes a programmable hysteresis to cause the HFO to stay powered for a programmable number of seconds after it is wakened by a falling edge on SPI_CS. This hysteresis is controlled by the ***Settings:Configuration:Comm Idle Time*** configuration setting, which can be set from 0 to 255 seconds (while in SPI mode, the device will use a minimum hysteresis of 1 second even if the value is set to 0). The host can set this to a longer time (up to 255 seconds) and maintain regular communications within this time window, causing the HFO to stay powered, so the device can respond quickly to SPI transactions. However, keeping the HFO running continuously will cause the device to consume additional supply current beyond what it would consume if the HFO were only powered when needed (the HFO draws ≈30 µA when powered). In order to avoid this extra supply current, the host can send an initial, unnecessary SPI transaction to cause the HFO to waken, and retry this until a valid response is returned on SPI_MISO. At this point, the host can begin sending the intended SPI transactions.

If an excessive number of SPI transactions occur over a long period of time, the device may experience a watchdog fault. It is recommended to limit the frequency of SPI transactions by providing 50 µs or more from the end of one transaction to the start of a new transaction.

The device includes ability to detect a frozen or disconnected SPI bus condition, and it will then reset the bus logic. This condition is recognized when the SPI_CS is low and the SPI_SCLK is static and not changing for a two second timeout.

Depending on the version of the device being used, the SPI_MISO pin may be configured by default to use the REG18 LDO for its output drive, which will result in a 1.8-V signal level. This may cause communications errors if the host processor operates with a higher voltage, such as 3.3 V or 5 V. The SPI_MISO pin can be programmed to instead use the REG1 LDO for its output drive by setting the ***Settings:Configuration:SPI Configuration[MISO_REG1]*** data memory configuration bit. This bit should only be set if the REG1 LDO is powered. After this bit has been modified, it is necessary to send the *SWAP_TO_SPI()* or *SWAP_COMM_MODE()* subcommands for the device to use the new value.

The device includes optional pin filtering on the SPI input pins, which implements a filter with approximately 200-ns delay on each input pin. This filtering is enabled by default but can be disabled by clearing the ***Settings:Configuration:SPI Configuration[FILT]*** data memory configuration bit.

14.3.1 SPI Protocol

The first byte of a SPI transaction consists of an R/W bit (R=0, W=1), followed by a 7-bit address, MSB-first. If the master (host) is writing, then the second byte will be the data to be written. If the master is reading, then the second byte sent on SPI_MOSI is ignored (except for CRC calculation).

If CRC is enabled, then the master must send as the third byte the 8-bit CRC code, which is calculated over the first two bytes. If the CRC is correct, then the values clocked in will be put into the incoming buffer. If the CRC is not correct, then the outgoing buffer will be set to 0xFFFF, and the outgoing CRC will be set to 0xAA (these are clocked out on the next transaction).

During this transaction, the logic will clock out the contents of the outgoing buffer. If the outgoing buffer has not been updated since the last transaction, then the logic will clock out 0xFFFF, and if the CRC is clocked, it will clock out 0x00 for the CRC (if enabled). Thus the 0xFFFF00 will indicate to the master that the outgoing buffer

was not updated by the internal logic before the transaction occurred. This can occur when the device did not have sufficient time to update the buffer between consecutive transactions.

When the internal logic takes the write-data from the interface logic and processes it, it also causes the R/W bit, address, and data to be copied into the outgoing buffer. On the next transaction, this data is clocked back to the master.

When the master is initiating a read, the internal logic will put the R/W bit and address into the outgoing buffer, along with the data requested. The interface will compute the CRC on the two bytes in the outgoing buffer and clock that back to the master if CRC is enabled (with the exceptions associated with 0xFFFF as noted above). A diagram of three transaction sequences with and without CRC are shown below, assuming CPOL=0.

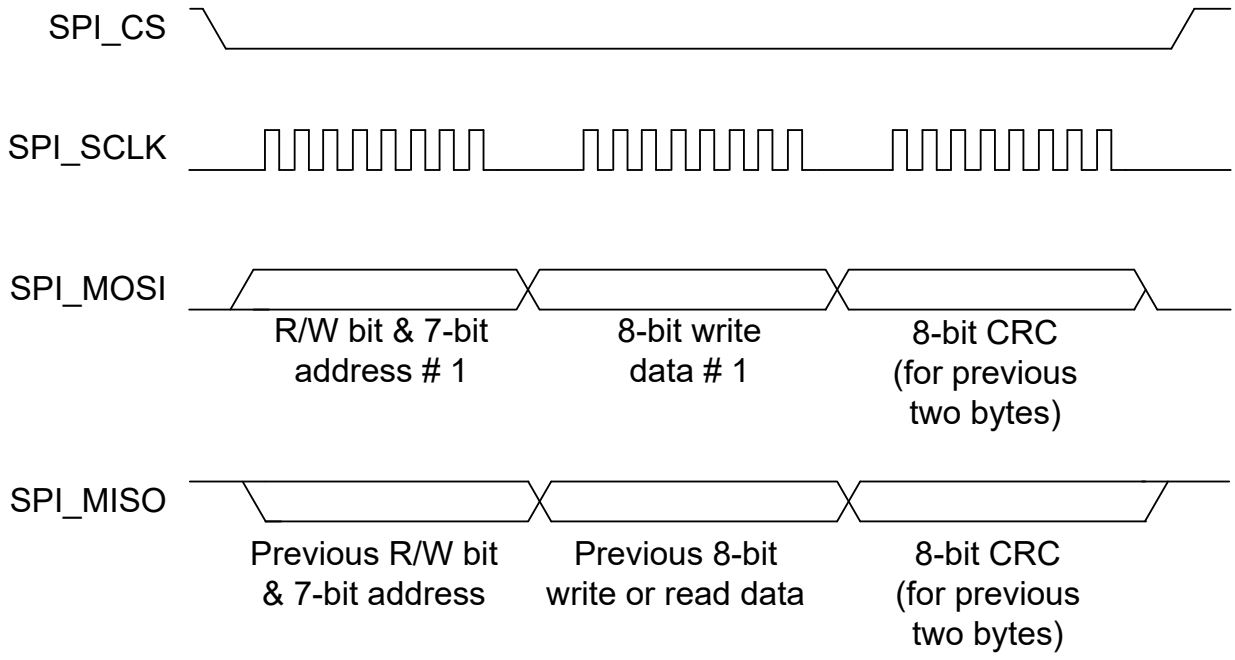


図 14-5. SPI Transaction #1 Using CRC

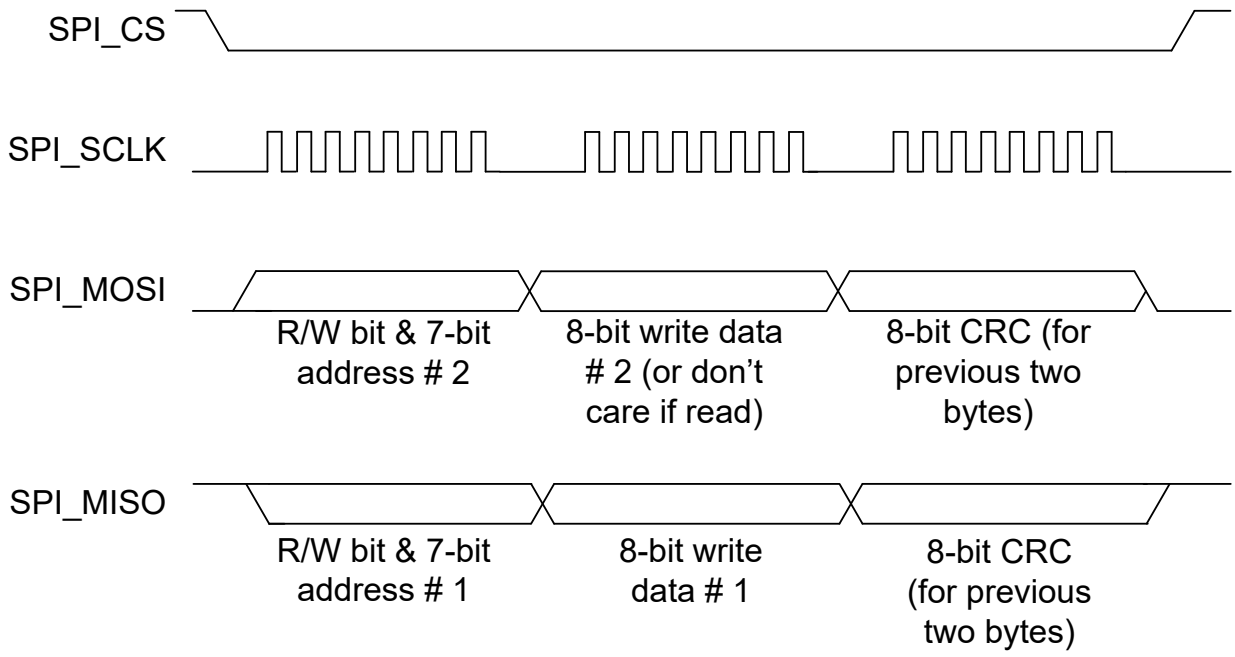


図 14-6. SPI Transaction #2 Using CRC

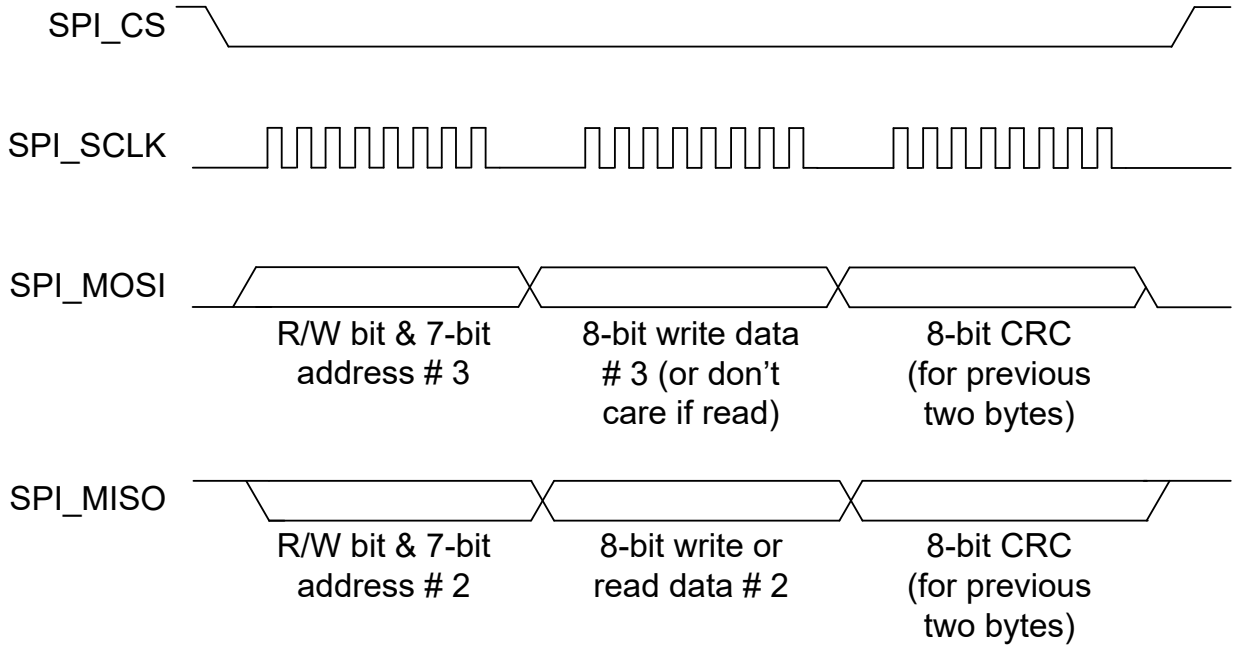


図 14-7. SPI Transaction #3 Using CRC

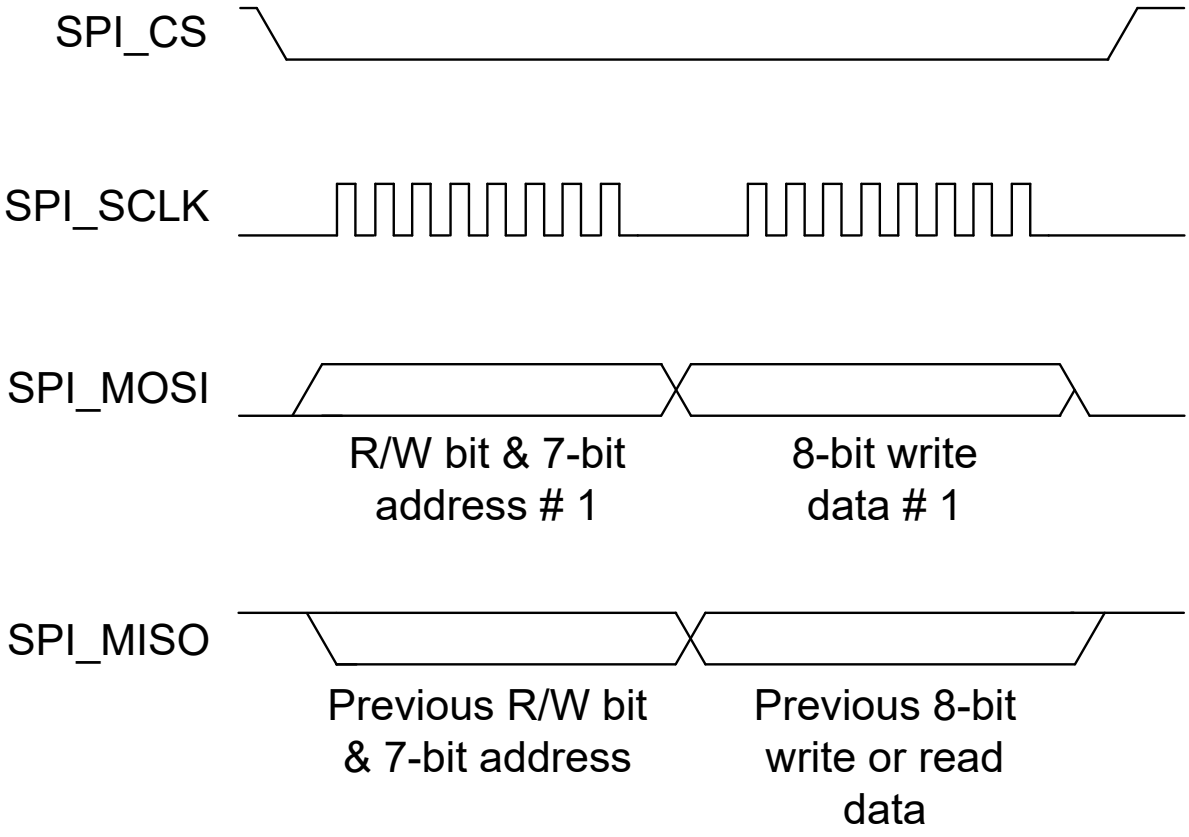


図 14-8. SPI Transaction #1 Without CRC

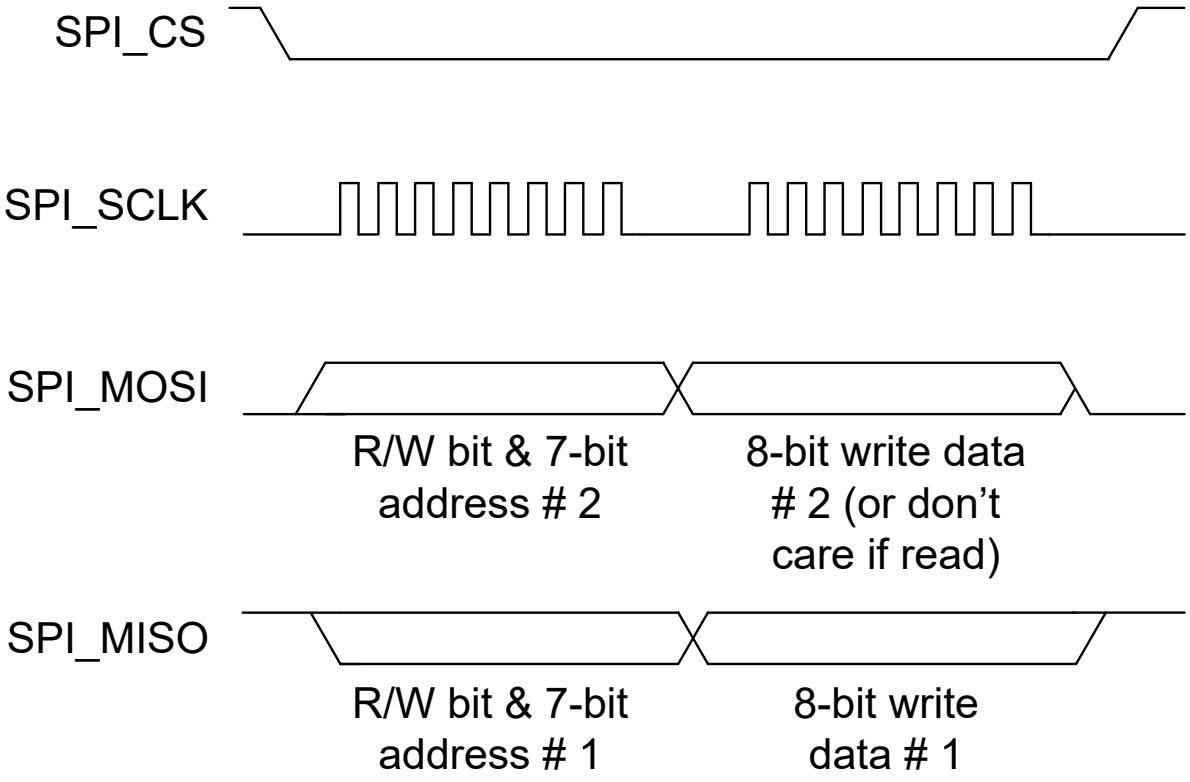


図 14-9. SPI Transaction #2 Without CRC

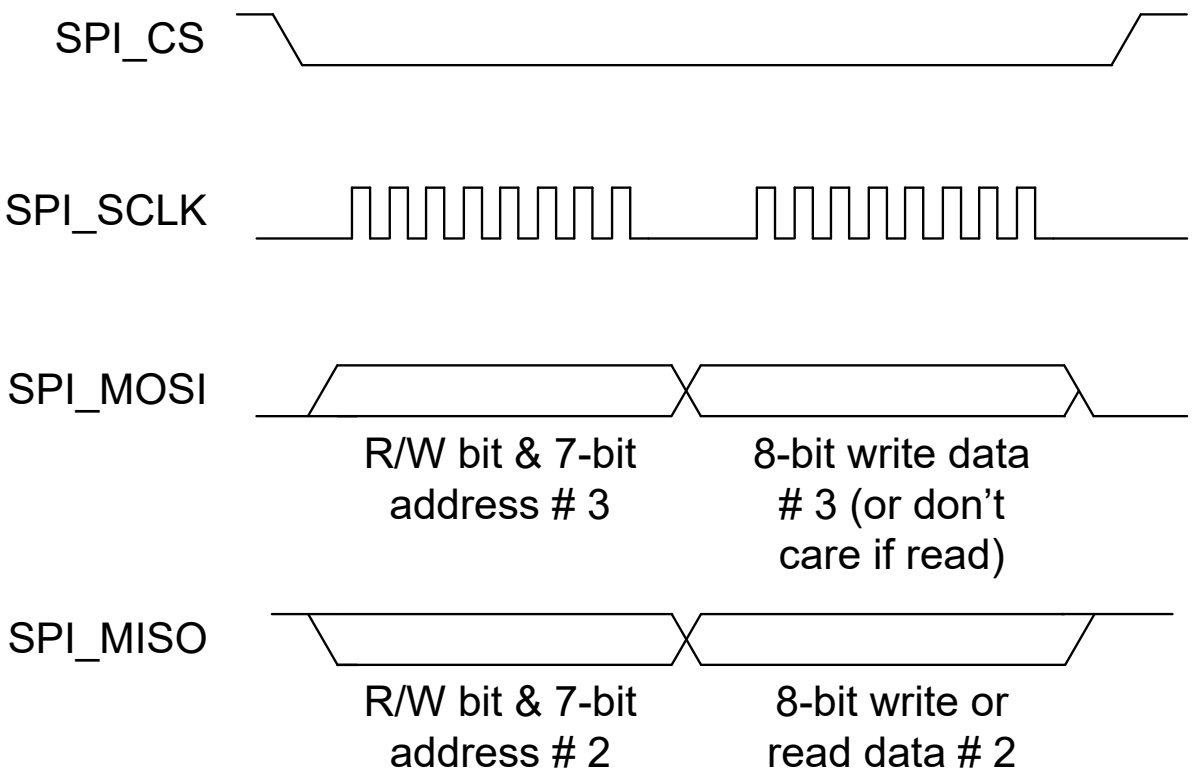


図 14-10. SPI Transaction #3 Without CRC

The time required for the device to process commands and subcommands will differ based on the specifics of each. The direct commands generally will complete within 50 µs, while subcommands can take longer, with different subcommands requiring different duration to complete. For example, when a particular subcommand is sent, the device requires approximately 200 µs to load the 32-byte data into the internal subcommand buffer. If the host provides sufficient time for this load to complete before beginning to read the buffer (readback from addresses 0x40 to 0x5F), the device will respond with valid data, rather than 0xFFFF00. When data has already been loaded into the subcommand buffer, this data can be read back with approximately 50-µs interval between SPI transactions. More detail regarding the approximate time duration required for specific commands and subcommands is provided in the *BQ769142 Technical Reference Manual* (SLUUCF2).

The host software should incorporate a scheme to retry transactions that may not be successful. For example, if the device returns 0xFFFFFF on SPI_MISO, then the internal clock was not powered, and the transaction will need to be retried. Similarly, if the device returns 0xFFFFAA on a transaction, this indicates the previous transaction encountered a CRC error, and so the previous transaction must be retried. And as described above, if the device returns 0xFFFF00, then the previous transaction had not completed when the present transaction was sent, which may mean the previous transaction should be retried, or at least needs more time to complete.

14.4 HDQ Communications

The HDQ interface is an asynchronous return-to-one protocol where a processor communicates with the BQ769142 device using a single-wire connection to the ALERT pin or the HDQ pin, depending on configuration. Both the master (host device) and slave (BQ769142) drive the HDQ interface using an open-drain driver, with a pullup resistor from the HDQ interface to a supply voltage required on the circuit board. The BQ769142 device can be changed from the default communication mode to HDQ communication mode by setting the ***Settings:Configuration:Comm Type*** configuration register, or sending a subcommand (at which point the device switches to HDQ mode immediately). Note that the *SWAP_COMM_MODE()* subcommand immediately

changes the communications interface to that selected by the ***Comm Type*** configuration, while the *SWAP_TO_HDQ()* subcommand immediately changes the interface to HDQ using the ALERT pin.

With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first.

The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0–6) and the 1-bit R/W field (MSB Bit 7). The R/W field directs the device to do one of the following:

- Accept the next 8 bits as data from the host to the device, or
- Output 8 bits of data from the device to the host in response to the 7-bit command.

The HDQ peripheral on the BQ769142 device can transmit and receive data as an HDQ slave only.

The return-to-one data bit frame of HDQ consists of the following sections:

1. The first section is used to start the transmission by the host sending a Break (the host drives the HDQ interface to a logic-low state for a time $t_{(B)}$) followed by a Break Recovery (the host releases the HDQ interface for a time $t_{(BR)}$).
2. The next section is for host command transmission, where the host transmits 8 bits by driving the HDQ interface for 8 $T_{(CYCH)}$ time slots. For each time slot, the HDQ line is driven low for a time $T_{(HW0)}$ (host writing a "0") or $T_{(HW1)}$ (host writing a "1"). The HDQ pin is then released and remains high to complete each $T_{(CYCH)}$ time slot.
3. The next section is for data transmission where the host (if a write was initiated) or device (if a read was initiated) transmits 8 bits by driving the HDQ interface for 8 $T_{(CYCH)}$ (if host is driving) or $T_{(CYCD)}$ (if device is driving) time slots. The HDQ line is driven low for a time $T_{(HW0)}$ (host writing a "0"), $T_{(HW1)}$ (host writing a "1"), $T_{(DW0)}$ (device writing a "0"), or $T_{(DW1)}$ (device writing a "1"). The HDQ pin is then released and remains high to complete the time slot. The HDQ interface does not auto-increment, so a separate transaction must be sent for each byte to be transferred.

15 Cell Balancing

15.1 Cell Balancing Overview

The BQ769142 device supports passive cell balancing by bypassing the current of a selected cell during charging or at rest, using either integrated bypass switches between cells, or external bypass FET switches. The device incorporates a voltage-based balancing algorithm which can optionally balance cells autonomously without requiring any interaction with a host processor. Or if preferred, balancing can be entirely controlled manually from a host processor. For autonomous balancing, the device will only balance non-adjacent cells in use (it does not consider inputs used to measure interconnect as cells in use). To avoid excessive power dissipation within the BQ769142 device, the maximum number of cells allowed to balance simultaneously can be limited by configuration setting. For host-controlled balancing, adjacent as well as non-adjacent cells can be balanced. Host-controlled balancing can be controlled using specific subcommands sent by the host. The device also returns status information regarding how long cells have been balanced through subcommands.

When host-controlled balancing is initiated using subcommands, the device starts a timer and will continue balancing until the timer reaches a programmed value, or a new balancing subcommand is issued (which resets the timer). This is included as a precaution, in case the host processor initiated balancing but then stopped communication with the BQ769142 device, so that balancing would not continue indefinitely.

The BQ769142 device can automatically balance cells using a voltage-based algorithm based on environmental and system conditions. Several settings are provided to control when balancing is allowed, which are described in detail in the *BQ769142 Technical Reference Manual*.

Due to the current that flows into the cell input pins on the BQ769142 device while balancing is active, the measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. Balancing is temporarily disabled during the regular measurement loop while the actively balanced cell is being measured by the ADC, as well as when the cells immediately adjacent to the active cell are being measured. Similarly, balancing on the top cell is disabled while the stack voltage measurement is underway. This occurs on every measurement loop, and so can result in significant reduction in the average balancing current that flows. In order to help alleviate this, additional configuration bits are provided which cause the device to slow the measurement loop speed when cell balancing is active. The BQ769142 device will insert current-only

measurements after each voltage and a temperature scan loop to slow down voltage measurements and thereby increase the average balancing current.

The device includes an internal die temperature check, to disable balancing if the die temperature exceeds a programmable threshold. However, the customer should still carefully analyze the thermal effect of the balancing on the device in system. Based on the planned ambient temperature of the device during operation and the thermal properties of the package, the maximum power should be calculated that can be dissipated within the device and still ensure operation remains within the recommended operating temperature range. The cell balancing configuration can then be determined such that the device power remains below this level by limiting the maximum number of cells that can be balanced simultaneously, or by reducing the balancing current of each cell by appropriate selection of the external resistance in series with each cell.

16 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

16.1 Application Information

The BQ769142 device can be used with 3-series to 14-series battery packs, supporting a top-of-stack voltage ranging from 5 V up to 80 V. To design and implement a comprehensive set of parameters for a specific battery pack, during development the user can use Battery Management Studio (BQSTUDIO), which is a graphical user-interface tool installed on a PC. Via BQSTUDIO, the device can be configured for specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable, or disable of certain features for operation, configuration of cells, and more are known. This results in a "golden image" of settings, which can then be programmed into the device registers or OTP memory.

16.2 Typical Applications

図 16-1 shows a simplified application schematic for a 14-series battery pack, using the BQ769142 together with an external secondary protector, a host microcontroller, and a communications transceiver. This configuration uses CHG and DSG FETs in series, together with high-side PFET devices used to implement precharge and predischarge functionality. See the following implementation considerations:

- The external NPN BJT used for the REGIN preregulator can be configured with its collector routed either to the cell battery stack or the middle of the protection FETs.
- A diode is recommended in the drain circuit of the external NPN BJT, which avoids reverse current flow from the BREG pin through the BJT base to collector in the event of a pack short circuit. This diode can be a Schottky diode if low voltage pack operation is needed, or a conventional diode can be used otherwise.
- A series diode is recommended at the BAT pin, together with a capacitor from the pin to VSS. These components allow the device to continue operating for a short time when a pack short circuit occurs, which may cause the PACK+ and top-of-stack voltages to drop to approximately 0 V. In this case, the diode prevents the BAT pin from being pulled low with the stack, and the device will continue to operate, drawing current from the capacitor. Generally operation is only required for a short time, until the device detects the short circuit event and disables the DSG FET. A Schottky diode can be used if low voltage pack operation is needed, or a conventional diode can be used otherwise.
- The diode in the BAT connection and the diode in the BJT collector should not be shared, since then the REG0 circuit might discharge the capacitor on BAT too quickly during a short circuit event.
- The recommended voltage range on the VC0 to VC4 pins extends to –0.2 V. This can be used, for example, to measure a differential voltage that extends slightly below ground, such as the voltage across a second sense resistor in parallel with that connected to the SRP and SRN pins.

- If a system does not use high-side protection FETs, then the PACK pin can be connected through a series 10-kΩ resistor to the top of stack. The LD pin can be connected to VSS. In this case, the LD pin can also be controlled separately, in order to wake the device from SHUTDOWN mode, such as through external circuitry which holds the LD pin at the voltage of VSS while the device stays in SHUTDOWN, and to be driven above a voltage of $V_{WAKEONLD}$ in order to wake from SHUTDOWN.
- TI recommends using 100 Ω resistors in series with the SRP and SRN pins, and a 100 nF with optional 100 pF differential filter capacitance between the pins for filtering. The routing of these components, together with the sense resistor, to the pins should be minimized and fully symmetric, with all components recommended to stay on the same side of the PCB with the device. Optional 0.1-µF filter capacitors can be added for additional noise filtering at each sense input pin to VSS.
- Due to thermistors often being attached to cells and possibly needing long wires to connect back to the device, it may be helpful to add a capacitor from the thermistor pin to the device VSS. However, it is important not to use too large of a value of capacitor, since this affects the settling time when the thermistor is biased and measured periodically. A rule of thumb is to keep the time constant of the circuit < 5% of the measurement time. When ***Settings:Configuration:Power Config[FASTADC]*** = 0, the measurement time is approximately 3 ms, and with ***[FASTADC]*** = 1 the measurement time is halved to approximately 1.5 ms. When using the 18-kΩ pullup resistor with the thermistor, the time constant is generally less than (18 kΩ) × C, so a capacitor less than 4 nF is recommended. When using the 180-kΩ pullup resistor, the capacitor should be less than 400 pF.
- The integrated charge pump generates a voltage on the CP1 capacitor, requiring approximately 60 ms to charge up to approximately 11 V when first enabled, when using the recommended 470-nF capacitor value. When the CHG or DSG drivers are enabled, charge redistribution occurs from the CP1 capacitor to the CHG and DSG capacitive FET loads. This generally results in a brief drop in the voltage on CP1, which is then replenished by the charge pump. If the FET capacitive loading is large, such that at FET turnon the voltage on CP1 drops below an acceptable level for the application, then the value of the CP1 capacitor can be increased. This has the drawback of requiring a longer startup time for the voltage on CP1 when the charge pump is first powered on, and so should be evaluated to ensure it is acceptable in the system. For example, if the CHG and DSG FETs are enabled simultaneously and their combined gate capacitance is approximately 400 nF, then changing CP1 to a value of 2200 nF will result in the 11-V charge pump level dropping to approximately 9 V, before being restored to the 11-V level by the charge pump.

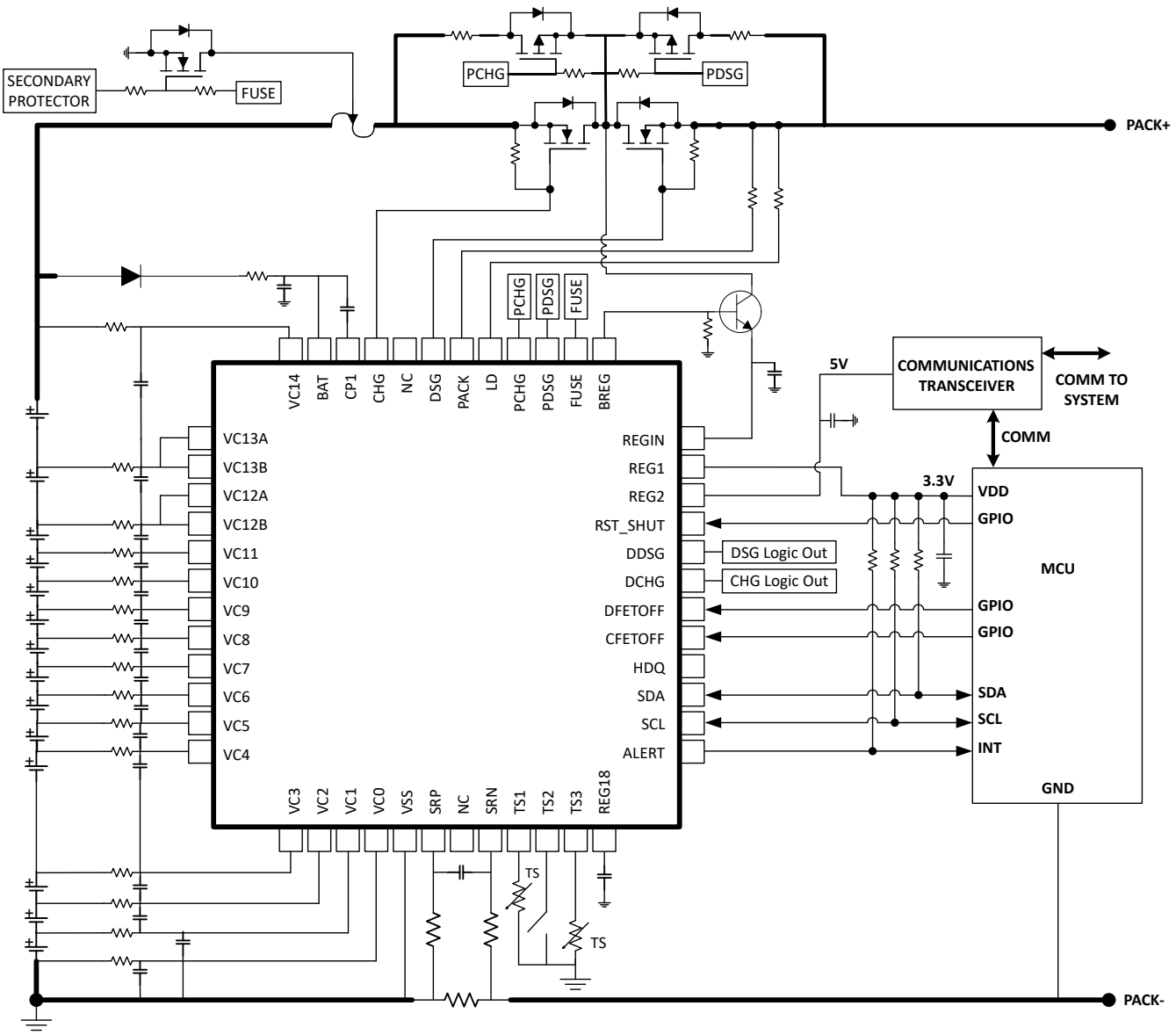


図 16-1. BQ769142 14-Series Cell Typical Implementation (Simplified Schematic)

図 16-2 and 図 16-3 show a full schematic of a basic monitor circuit based on the BQ769142 for a 14-series battery pack. The BQ76952 EVM also provides a good reference design for BQ769142, noting that the VC12 - VC16 connections in the BQ76952 EVM need to be modified as shown in 図 16-1.

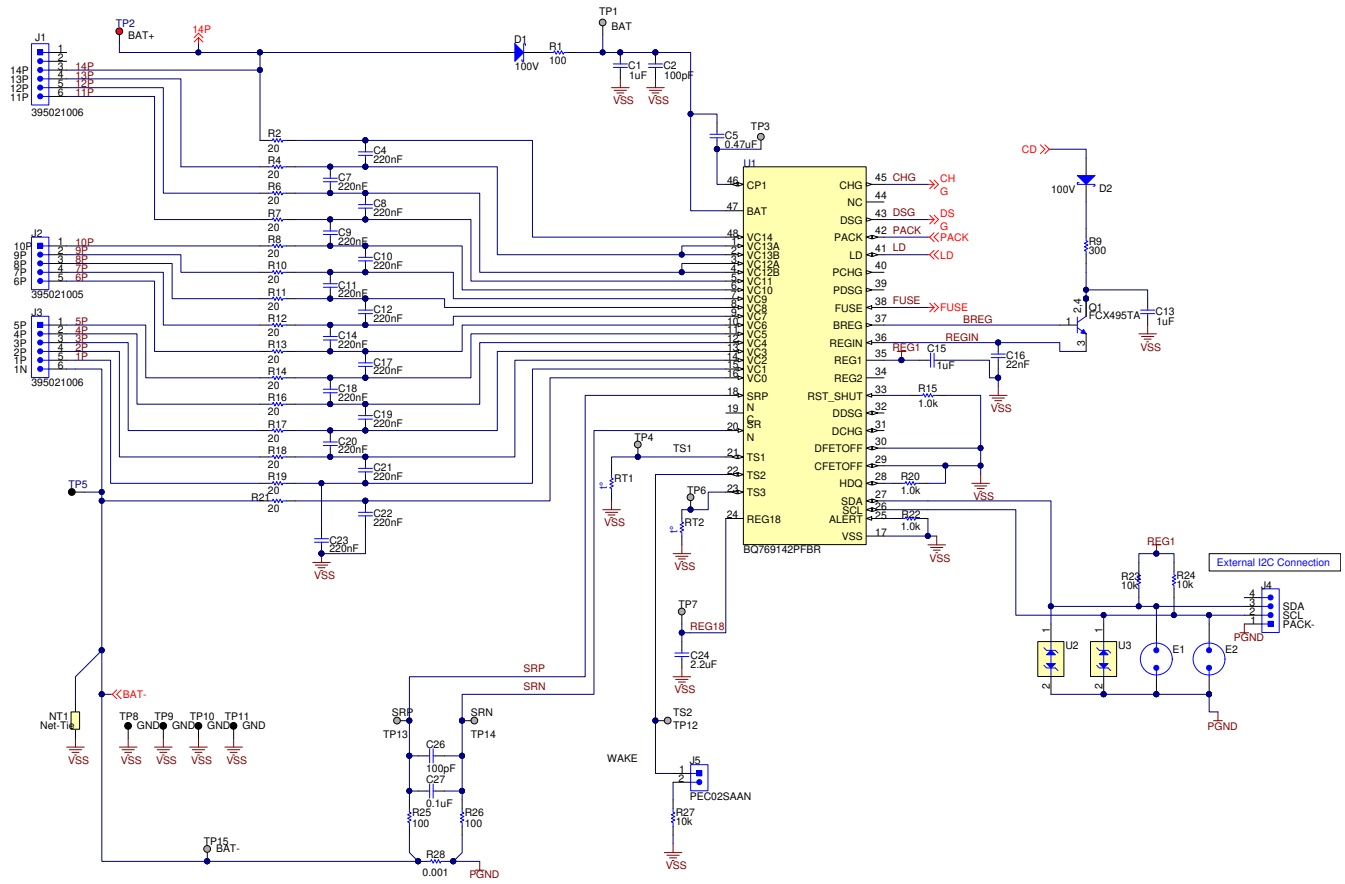


図 16-2. BQ769142 14-Series Cell Schematic Diagram—Monitor

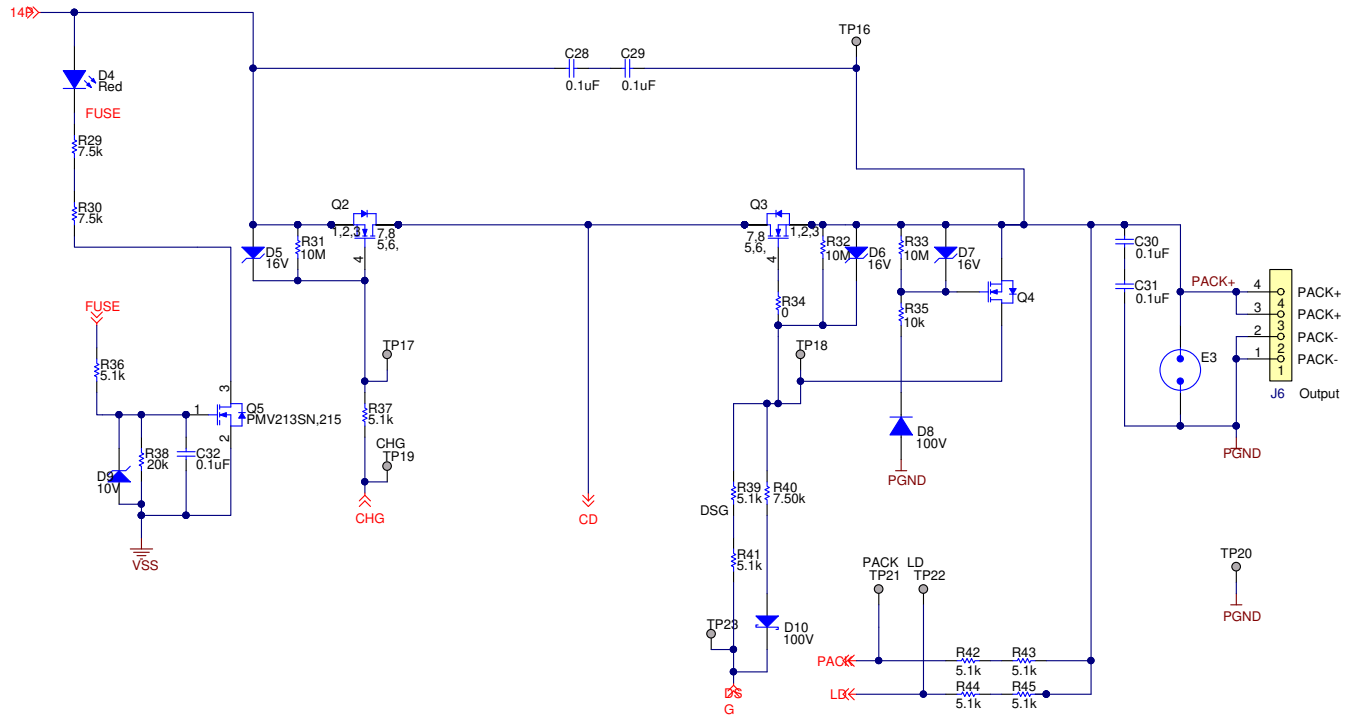


図 16-3. BQ769142 14-Series Cell Schematic Diagram—Additional Circuitry

The board layout for a similar design using the BQ76952 for a 16-series battery pack is shown in セクション 18.2.

16.2.1 Design Requirements (Example)

表 16-1. BQ769142 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Minimum system operating voltage	35 V
Cell minimum operating voltage	2.5 V
Series cell count	14
Sense resistor	1 mΩ
Number of thermistors	3 (using TS1, TS2, and TS3 pins, all for cells)
Charge voltage	60 V
Maximum charge current	8.0 A
Peak discharge current	20.0 A
Configuration settings	Programmed in OTP during customer production
Protection subsystem configuration	Series FET configuration, device monitors, disables FETs upon fault, recovers autonomously
OV protection threshold	4.35 V
OV protection delay	500 ms
OV protection recovery hysteresis	100 mV
UV protection threshold	2.5 V
UV protection delay	20 ms
UV protection recovery hysteresis	100 mV
SCD protection threshold	80 mV (corresponding to a nominal 80 A, based on a 1-mΩ sense resistor)
SCD protection delay	50 µs
OCD1 protection threshold	68 mV (corresponding to a nominal 68 A, based on a 1-mΩ sense resistor)
OCD1 protection delay	10 ms
OCD2 protection threshold	56 mV (corresponding to a nominal 56 A, based on a 1-mΩ sense resistor)
OCD2 protection delay	80 ms
OCD3 protection threshold	28 mV (corresponding to a nominal 28 A, based on a 1-mΩ sense resistor)
OCD3 protection delay	160 ms
OCC protection threshold	8 mV (corresponding to a nominal 8 A, based on a 1-mΩ sense resistor)
OCC protection delay	160 ms
OTD protection threshold	60°C
OTD protection delay	2 s
OTC protection threshold	45°C
OTC protection delay	2 s
UTD protection threshold	–20°C
UTD protection delay	10 s
UTC protection threshold	0°C
UTC protection delay	5 s
Host watchdog timeout protection delay	5 s
CFETOFF pin functionality	Use as CFETOFF, polarity = normally high, driven low to disable FET
DFETOFF pin functionality	Use as DFETOFF, polarity = normally high, driven low to disable FET
ALERT pin functionality	Use as ALERT interrupt pin, polarity = driven low when active, hi-Z otherwise
REG1 LDO Usage	Use for 3.3-V output
Cell balancing	Enabled when imbalance exceeds 100 mV

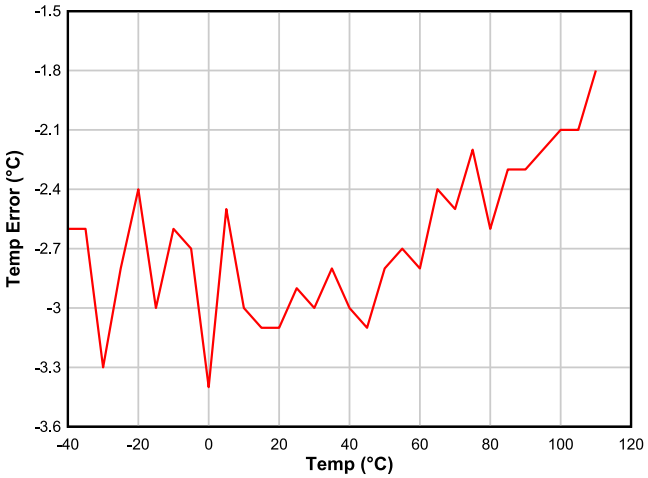
16.2.2 Detailed Design Procedure

- Determine the number of series cells.

  - This value depends on the cell chemistry and the load requirements of the system. For example, to support a minimum battery voltage of 35 V using Li-CO_2 type cells with a cell minimum voltage of 2.5 V, there needs to be at least 14-series cells.
  - For the correct cell connections, see セクション 10.1.2.
- Protection FET selection and configuration
  - The BQ769142 device is designed for use with high-side NFET protection (low-side protection NFETs can be used by leveraging the DCHG / DDSG signals).
  - The configuration should be selected for series versus parallel FETs, which may lead to different FET selection for charge versus discharge direction.
  - These FETs should be rated for the maximum:
    - Voltage, which should be approximately 5 V (DC) to 10 V (peak) per series cell
    - Current, which should be calculated based on both the maximum DC current and the maximum transient current with some margin
    - Power Dissipation, which can be a factor of the RDS(ON) rating of the FET, the FET package, and the PCB design
  - The overdrive level of the BQ769142 device charge pump should be selected based on RDS(ON) requirements for the protection FETs and their voltage handling requirements. If the FETs are selected with a maximum gate-to-source voltage of 15 V, then the 11-V overdrive mode within the BQ769142 device can be used. If the FETs are not specified to withstand this level or there is a concern over gate leakage current on the FETs, the lower overdrive level of 5.5 V can be selected.
- Sense resistor selection
  - The resistance value should be selected to maximize the input range of the coulomb counter, but not exceed the absolute maximum ratings, and avoid excessive heat generation within the resistor.
    - Using the normal maximum charge or discharge current, the sense resistor = 200 mV / 20.0 A = 10 mΩ maximum
    - However, considering a short circuit discharge current of 80 A, the recommended maximum SRP, SRN voltage of ≈0.75 V, and the maximum SCD threshold of 500 mV, the sense resistor should be below 500 mV / 80 A= 6.25 mΩ maximum.
  - Further tolerance analyses (value tolerance, temperature variation, and so on) and the PCB design margin should also be considered, so a sense resistor of 1 mΩ is suitable with a 50-ppm temperature coefficient and power rating of 1 W.
- The REG1 is selected to provide the supply for an external host processor with an output voltage selected for 3.3 V.
  - The NPN BJT used for the REG0 preregulator should be selected to support the maximum collector-to-emitter voltage of the maximum charging voltage of 60 V. The gain of the BJT should be chosen so it can provide the required maximum output current with a base current level that can be provided from the BQ769142 device.
  - The BJT should support the maximum current expected from the REG1 (maximum of 45 mA, with short circuit current limit of up to ≈80 mA).
  - A diode can be optionally included in the collector circuit of the BJT to avoid reverse current flow from BREG through the base-collector junction of the BJT to PACK+ during a pack short circuit event. This diode can be seen in 図 16-2 at D2.
  - A large resistor (such as 10 MΩ) is recommended from BREG to VSS to avoid any unintended leakage current that may occur during SHUTDOWN mode.

16.2.3 Application Performance Plot

The error in measured temperature using an external Semitec 103-AT thermistor, the default temperature polynomial, and the internal 18-kΩ pullup resistor is shown in 図 16-4.



Measurements taken using Semitec 103-AT thermistor, default temperature polynomial, and 18-kΩ internal pullup resistor.

図 16-4. Thermistor Temperature Error

16.2.4 Calibration Process

The BQ769142 device enables customers to calibrate the current, voltage, and temperature measurements on the customer production line. Detailed procedures are included in the *BQ769142 Technical Reference Manual* (SLUUCF2). The device provides the capability to calibrate individual cell voltage measurements, stack voltage, PACK pin voltage, LD pin voltage, current measurement, and individual temperature measurements.

16.3 Random Cell Connection Support

The BQ769142 device supports a random connection sequence of cells to the device during pack manufacturing. For example, cell-10 in a 14-cell stack might be first connected at the input terminals leading to pins VC10 and VC9, then cell-4 may next be connected at the input terminals leading to pins VC4 and VC3, and so on. It is not necessary to connect the negative terminal of cell-1 first at VC0. As another example, consider a cell stack that is already assembled and cells already interconnected to each other, then the stack is connected to the PCB through a connector, which is plugged or soldered to the PCB. In this case, the sequence order in which the connections are made to the PCB can be random in time, they do not need to be controlled in a certain sequence.

There are, however, some restrictions to how the cells are connected during manufacturing:

- To avoid misunderstanding, note that the cells in a stack ***cannot*** be randomly connected to ***any*** VC pin on the device, such as the lowest cell (cell-1) connected to VC13A, while the top cell (cell-14) is connected to VC4, and so on. It is important that the cells in the stack be connected in ascending pin order, with the lowest cell (cell-1) connected between VC1 and VC0, the next higher voltage cell (cell-2) connected between VC2 and VC1, and so on.
- The random cell connection support is possible due to high voltage tolerance on pins VC1–VC14.

Note

VC0 has a lower voltage tolerance. This is because VC0 should be connected through the series-cell input resistor to the VSS pin on the PCB, before any cells are attached to the PCB. Thus, the VC0 pin voltage is expected to remain close to the VSS pin voltage during cell attach. If VC0 is not connected through the series resistor to VSS on the PCB, then cells cannot be connected in random sequence.

- Each of the VC1–VC14 pins includes a diode between the pin and the adjacent lower cell input pin (that is, between VC14 and VC13A, between VC9 and VC8, and so on), which is reverse biased in normal operation. This means an upper cell input pin should not be driven to a low voltage while a lower cell input pin is driven to a higher voltage, since this would forward bias these diodes. During cell attach, the cell input terminals

should generally be floating before they are connected to the appropriate cell. It is expected that transient current will flow briefly when each cell is attached, but the cell voltages will quickly stabilize to a state without DC current flowing through the diodes. However, if a large capacitance is included between a cell input pin and another terminal (such as VSS or another cell input pin), the transient current may become excessive and lead to device heating. Therefore, it is recommended to limit capacitances applied at each cell input pin to the values recommended in the specifications.

16.4 Startup Timing

At initial power up of the BQ769142 device from a SHUTDOWN state, the device progresses through a sequence of events before entering NORMAL mode operation. These are described below for an example configuration, with approximate timing shown for the cases when ***[FASTADC]*** = 0 and ***[FASTADC]*** = 1.

Note

When the device is configured for autonomous FET control (that is, ***[FET_EN]*** = 1), the decision to enable FETs is only evaluated every 250 ms while in NORMAL mode, which is why the FETs are not enabled until approximately 280 ms after the wakeup event, even though the data was available earlier.

表 16-2. Startup Sequence and Timing

Step	Comment	FASTADC Setting	Time (relative to wakeup event)
Wakeup event	Either the TS2 pin is pulled low, or the LD pin is pulled up, triggering the device to exit SHUTDOWN mode.	0, 1	0
REG1 powered	This was measured with the OTP programmed to autonomously power the REG1 LDO.	0, 1	20 ms
INITSTART asserted	This was measured with the OTP programmed to provide the INITSTART bit in the Alarm signal on the ALERT pin.	0, 1	23 ms
INITCOMP and ADSCAN asserted	This was measured with the OTP programmed to provide the INITCOMP and ADSCAN bits in the Alarm signal on the ALERT pin.	0	88 ms
		1	58 ms
FULLSCAN asserted	This was measured with the OTP programmed to provide the FULLSCAN bit in the Alarm signal on the ALERT pin.	0	221 ms
		1	129 ms
FETs enabled	This was measured with the OTP programmed to autonomously enable FETs.	0	282 ms
		1	284 ms

図 16-5 shows an example of an oscilloscope plot of a startup sequence with the device configured in OTP with ***[FASTADC]*** = 1, ***[FET_EN]*** = 1 for autonomous FET control, setup to use three thermistors, and providing the *[INITCOMP]* flag on the ALERT pin. The TS2 pin is pulled low to initiate device wakeup from SHUTDOWN.

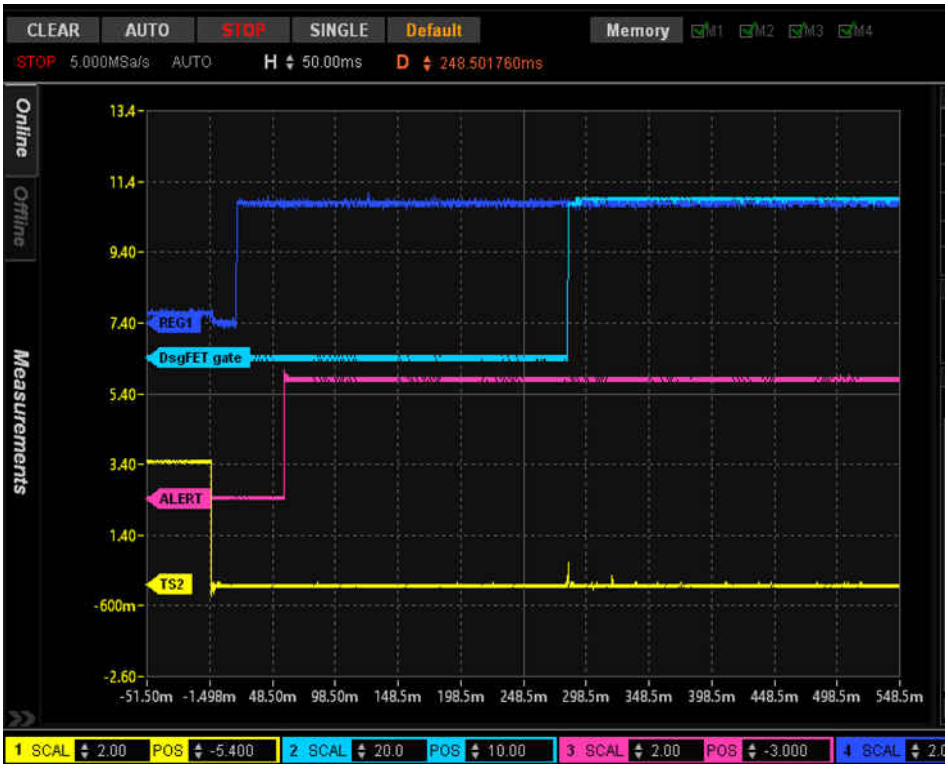


図 16-5. Startup Sequence Using *[FASTADC]* = 1, with the *[INITCOMP]* Flag Displayed on the ALERT Pin

16.5 FET Driver Turn-Off

The high-side CHG and DSG FET drivers operate differently when they are triggered to turn off their respective FET. The CHG driver includes an internal switch which discharges the CHG pin toward the BAT pin level. The DSG FET driver will discharge the DSG pin toward the LD pin level, but it includes a more complex structure than just a switch, to support a faster turn off.

When the DSG driver is triggered to turn off, the device will initially begin discharging the DSG pin toward VSS. However, since the PACK+ terminal may not fall to a voltage near VSS quickly, the DSG FET gate should not be driven significantly below PACK+, otherwise the DSG FET may be damaged due to excessive negative gate-source voltage. Thus, the device monitors the voltage on the LD pin (which is connected to PACK+ through an external series resistor) and will stop the discharge when the DSG pin voltage drops below the LD pin voltage. When the discharge has stopped, the DSG pin voltage may relax back above the LD pin voltage, at which point the device will again discharge the DSG pin toward VSS, until the DSG gate voltage again falls below the LD pin voltage. This repeats in a series of pulses which over time discharge the DSG gate to the voltage of the LD pin. This pulsing continues for approximately 100 to 200 µs, after which the driver remains in a high impedance state if within approximately 500 mV of the voltage of the LD pin. The external resistor between the DSG gate and source then discharges the remaining FET V_{GS} voltage so the FET remains off.

The external series gate resistor between the DSG pin and the DSG FET gate is used to adjust the speed of the turn-off transient. A low resistance (such as 100 Ω) will provide a fast turn-off during a short circuit event, but this may result in an overly large inductive spike at the top of stack when the FET is disabled. A larger resistor value (such as 1 kΩ or 4.7 kΩ) will reduce this speed and the corresponding inductive spike level.

Oscilloscope captures of DSG driver turn-off are shown below, with the DSG pin driving the gate of a CSD19536KCS NFET, which has a typical C_{iss} of 9250 pF. 図 16-6 shows the signals when using a 1-kΩ series gate resistor between the DSG pin and the FET gate, and a light load on PACK+, such that the voltage on PACK+ drops slowly as the FET is disabled. The pulsing on the DSG pin can be seen lasting for approximately 170 µs.

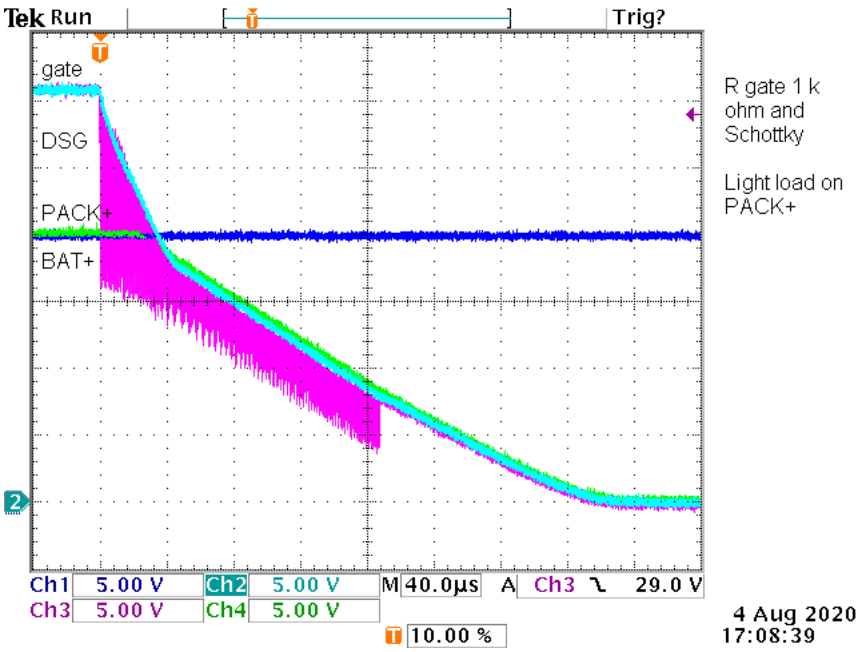


図 16-6. Moderate Speed DSG FET Turn-Off, Using a 1-kΩ Series Gate Resistor, and a Light Load on PACK+.

A zoomed-in version of the pulsing generated by the DSG pin is shown in 図 16-7, this time with PACK+ shorted to the top of stack.

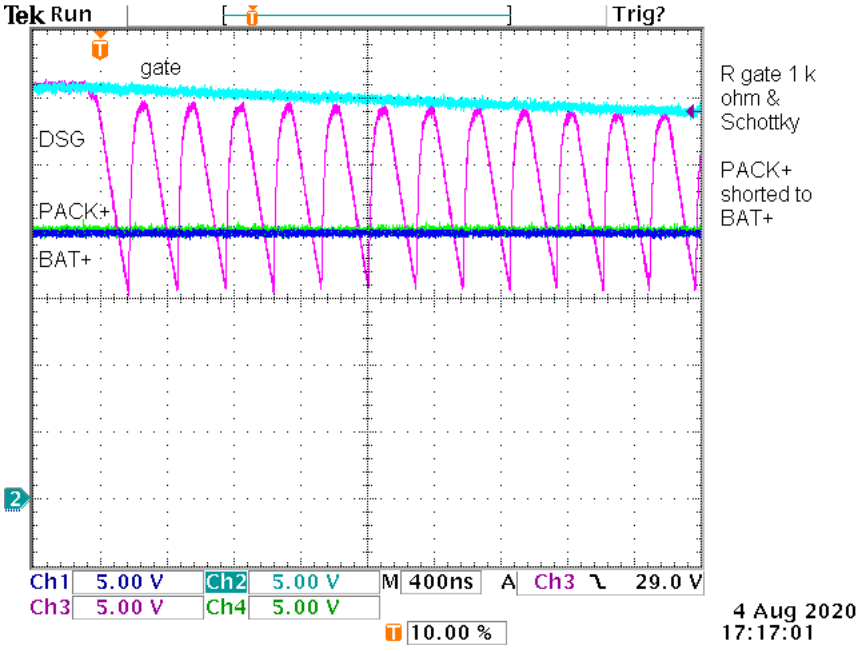


図 16-7. Zoomed-In View of the Pulsing on the DSG Pin During FET Turn-Off

A slower turn-off case is shown in 図 16-8, using a 4.7-kΩ series gate resistor, and the PACK+ connector shorted to the top of stack.

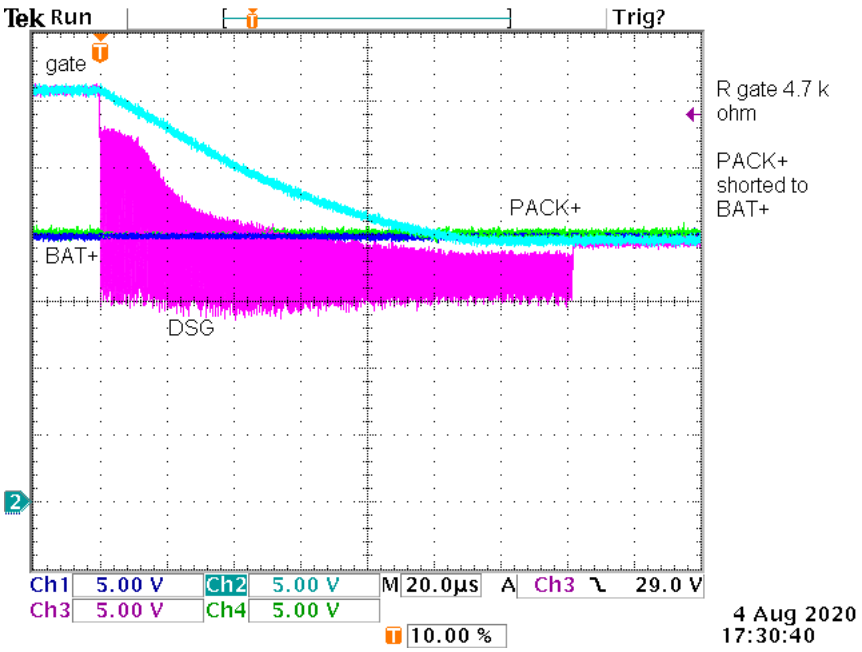


図 16-8. A Slower Turn-Off Case Using a 4.7-kΩ Series Gate Resistor, and the PACK+ Connector Shorted to the Top of the Stack

A fast turn-off case is shown in 図 16-9, in which a 100-Ω series gate resistor is used between the DSG pin and the FET gate.

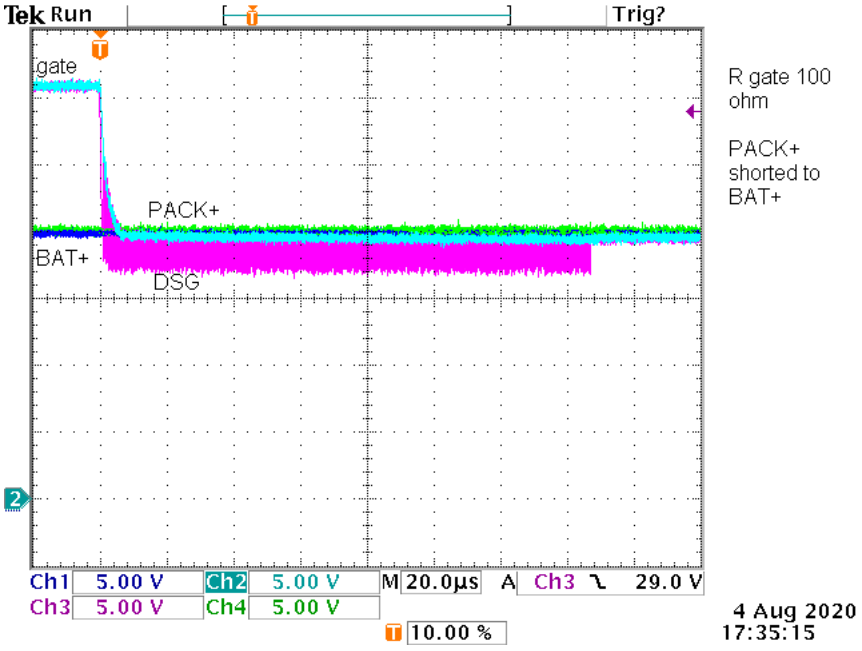


図 16-9. A Fast Turn-Off Case with a 100-Ω Series Gate Resistor

16.6 Unused Pins

Some device pins may not be needed in a particular application. The manner in which each should be terminated in this case is described below.

表 16-3. Terminating Unused Pins

Pin	Name	Recommendation
1–16, 48	VC0–VC14	Cell inputs 1, 2, and 14 should always be connected to actual cells, with cells connected between VC1 and VC0, VC2 and VC1, and VC14 and VC13A. VC0 should be connected through a resistor and capacitor on the pcb to pin 17 (VSS). Pins related to unused cells (which may be cell 3–cell 13) can be connected to the cell stack to measure interconnect resistance or provide a Kelvin-connection to actual cells, in which case they should include a series resistor and parallel capacitor, in similar fashion to pins connected to actual cells (see Usage of VC Pins for Cells Versus Interconnect). Another option is to short unused VC pins directly to an adjacent VC pin. All VC pins should be connected to either an adjacent VC pin, an actual cell (through R and C) or stack interconnect resistance (through R and C).
18, 20	SRP, SRN	If not used, these pins should be connected to pin 17 (VSS).
19, 44	NC	These pins are not connected to silicon. They can be left floating or connected to an adjacent pin or connected to VSS.
21, 23, 25, 28, 29, 30, 31, 32	TS1, TS3, ALERT, HDQ, CFETOFF, DFETOFF, DCHG, DDSG	If not used, these pins can be left floating or connected to pin 17 (VSS). Any of these pins (except for TS1 and TS3) may be configured with the internal weak pulldown resistance enabled during operation, although this is not necessary.
22	TS2	If the device is intended to enter SHUTDOWN mode, the TS2 pin should be left floating. If SHUTDOWN mode will not be used in the application, and the TS2 pin will not be used for a thermistor or ADCIN measurement, the TS2 pin can be left floating or connected to pin 17 (VSS).
33	RST_SHUT	If not used, this pin should be connected to pin 17 (VSS).
34, 35	REG1, REG2	If not used, these pins can be left floating or connected to pin 17 (VSS).
36	REGIN	If not used, this pin should be connected to pin 17 (VSS).
37	BREG	If this pin is not used and pin 36 (REGIN) is also not used, both pins should be connected to pin 17 (VSS). If this pin is not used but pin 36 is used (such as driven from an external source), then this pin should be connected to pin 36 (REGIN).
38	FUSE	If not used, this pin can be left floating or connected to pin 17 (VSS).
39	PDSG	If not used, this pin should be left floating.
40	PCHG	If not used, this pin should be left floating.
41	LD	If the DSG driver will not be used, this pin can be connected through a series resistor to the PACK+ connector, or can be connected to pin 17 (VSS).
43	DSG	If not used, this pin should be left floating.
45	CHG	If not used, this pin should be left floating.
46	CP1	If not used, this pin should be connected to pin 47 (BAT). **Note** If the charge pump is enabled with CP1 connected to BAT, the device will consume an additional ≈200 µA.

17 Power Supply Requirements

The BQ769142 device draws its supply current from the BAT pin, which is typically connected to the top of stack point through a series diode, to protect against any fault within the device resulting in unintended charging of the pack. A series resistor and capacitor is included to lowpass filter fast variations on the stack voltage. During a short circuit event, the stack voltage may be momentarily pulled to a very low voltage before the protection FETs are disabled. In this case, the charge on the BAT pin capacitor will temporarily support the BQ769142 device's supply current, to avoid the device losing power.

18 Layout

18.1 Layout Guidelines

- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-

circuit ranges of the BQ769142 device. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ sense resistor.

- In reference to the system circuitry, the following features require attention for component placement and layout: Differential Low-Pass Filter, and I^2C communication.
- The BQ769142 device uses an integrating delta-sigma ADC for current measurements. For best performance, 100-Ω resistors should be included from the sense resistor terminals to the SRP and SRN inputs of the device, with a 0.1-µF filter capacitor placed across the SRP and SRN pins. Optional 0.1-µF filter capacitors can be added for additional noise filtering at each sense input pin to ground. All filter components should be placed as close as possible to the device, rather than close to the sense resistor, and the traces from the sense resistor routed in parallel to the filter circuit. A ground plane can also be included around the filter network to add additional noise immunity.
- The BQ769142 device internal REG18 LDO requires an external decoupling capacitor, which should be placed as close to the REG18 pin as possible, with minimized trace inductance, and connected to a ground plane electrically connected to VSS.
- The I^2C clock and data pins have integrated ESD protection circuits; however, adding a Zener diode and series resistor on each pin provides more robust ESD performance.

18.2 Layout Example

An example circuit layout using the BQ76952 device in a 16-series cell design is described below. The design implements the schematic shown in and uses a 2.75-inch × 3.9-inch 2-layer circuit card assembly, with cell connections on the left edge, and pack connections along the top edge of the board. Wide trace areas are used, reducing voltage drops on the high current paths.

The board layout, which is shown in 図 18-1 and 図 18-2, includes spark gaps with the reference designator prefix *E*. These spark gaps are fabricated with the board and no component is installed.

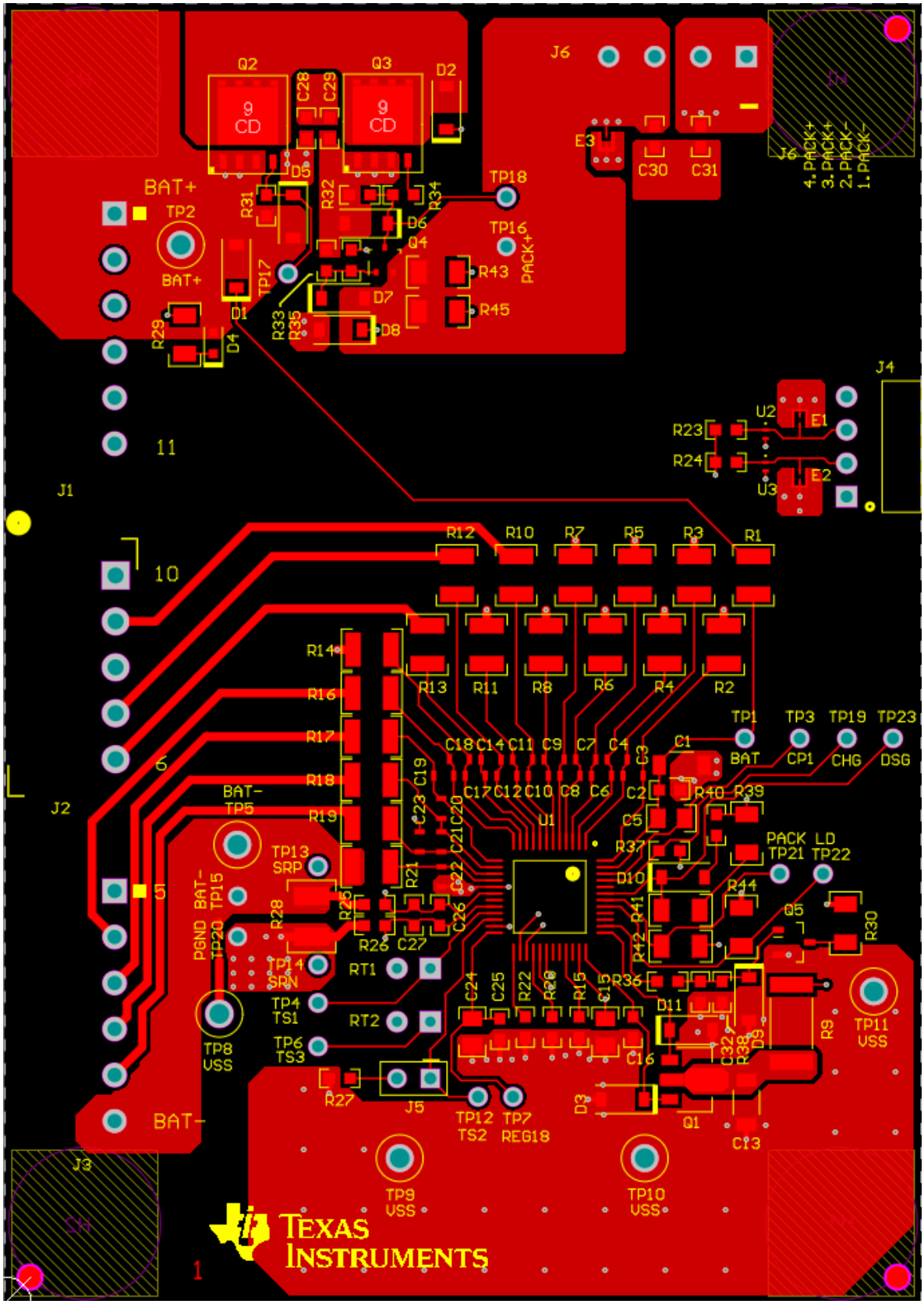


図 18-1. BQ76952 Two-Layer Board Layout–Top Layer

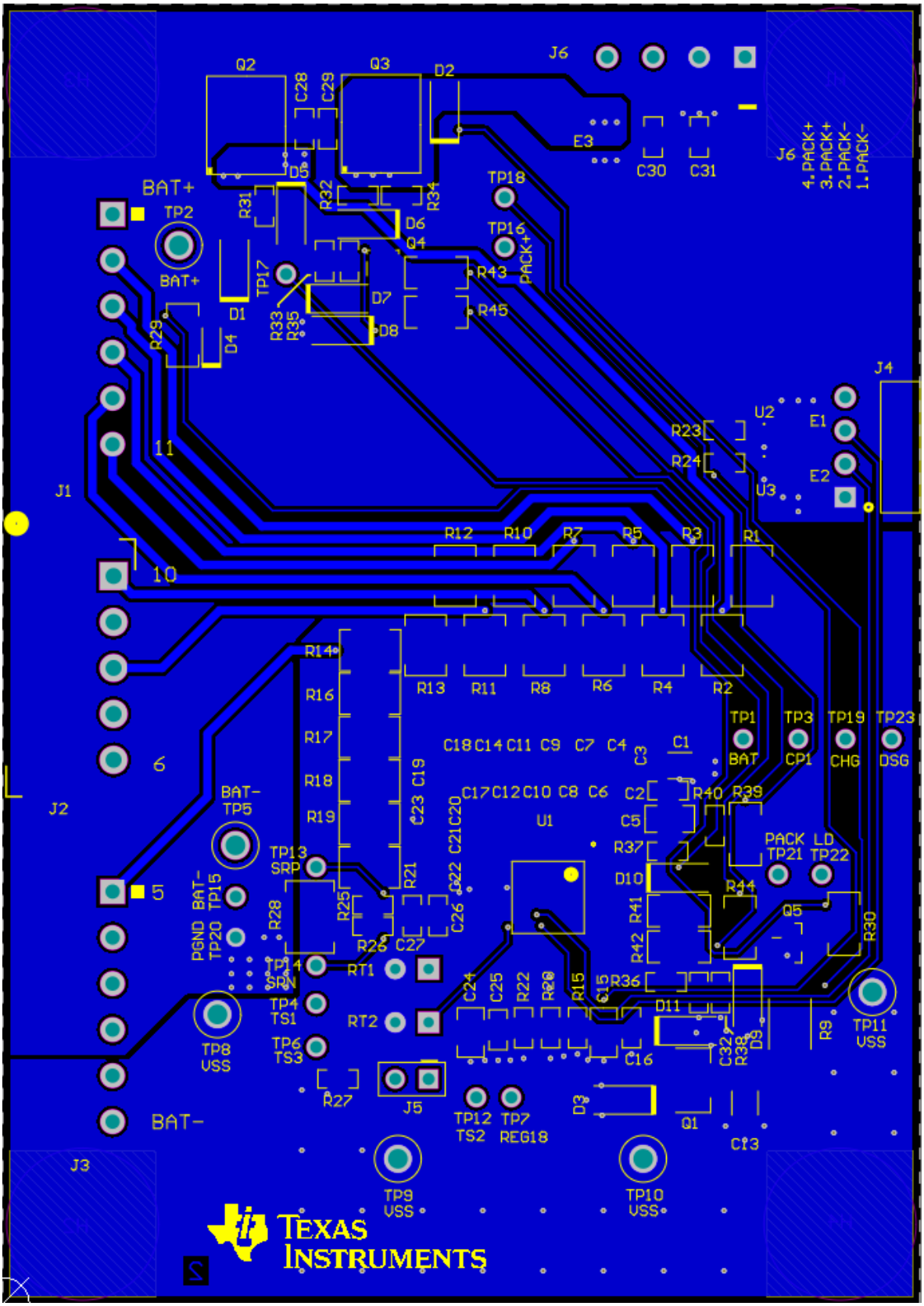


図 18-2. BQ76952 Two-Layer Board Layout–Bottom Layer

19 Device and Documentation Support

19.1 Third-Party Products Disclaimer

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19.2 Documentation Support

For additional information, see the following related documents:

- *BQ769142 Technical Reference Manual*
- *Using Low-Side FETs with the BQ769x2 Battery Monitor Family*
- *Cell Balancing with BQ769x2 Battery Monitors*
- *Multiple FETs with the BQ769x2 Battery Monitors*
- *BQ769x2 Software Development Guide*
- *BQ769x2 Calibration and OTP Programming Guide*
- *Pin Equivalent Diagrams for the BQ76952, BQ76942, and BQ769142*
- A glossary that defines terms, acronyms, and definitions can be found at *TI Glossary*.

Additional documents can be found in the product folder at *BQ769142 Technical documentation*.

19.3 サポート・リソース

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19.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

19.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

20 Mechanical, Packaging, Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ769142PFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ769142
BQ769142PFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ769142
BQ769142PFBR.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ769142

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

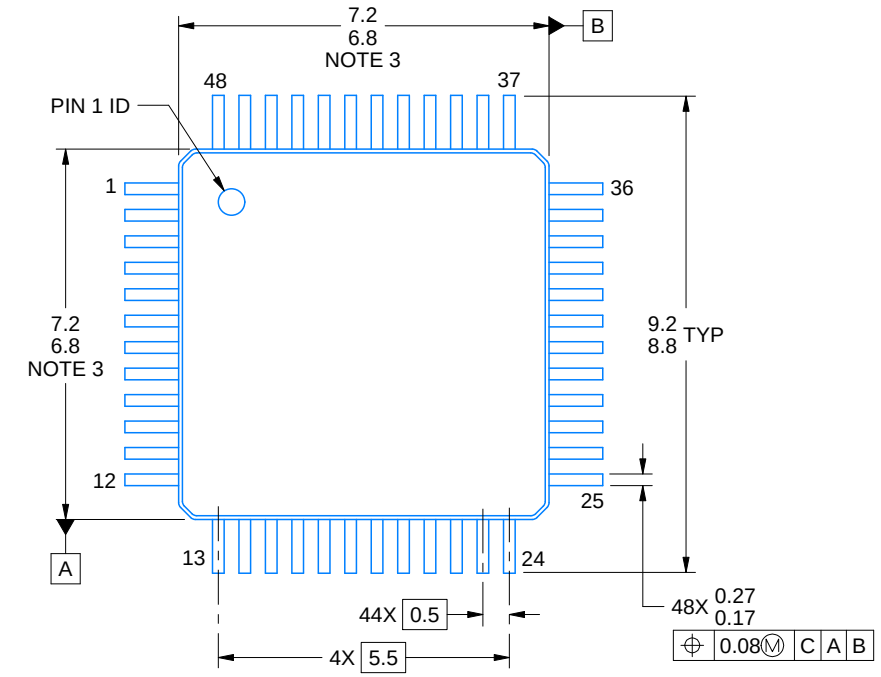
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

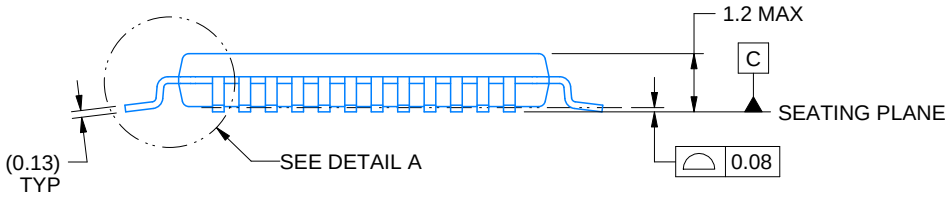
PACKAGE OUTLINE

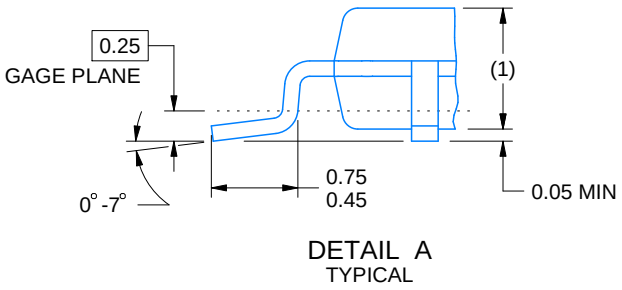
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK





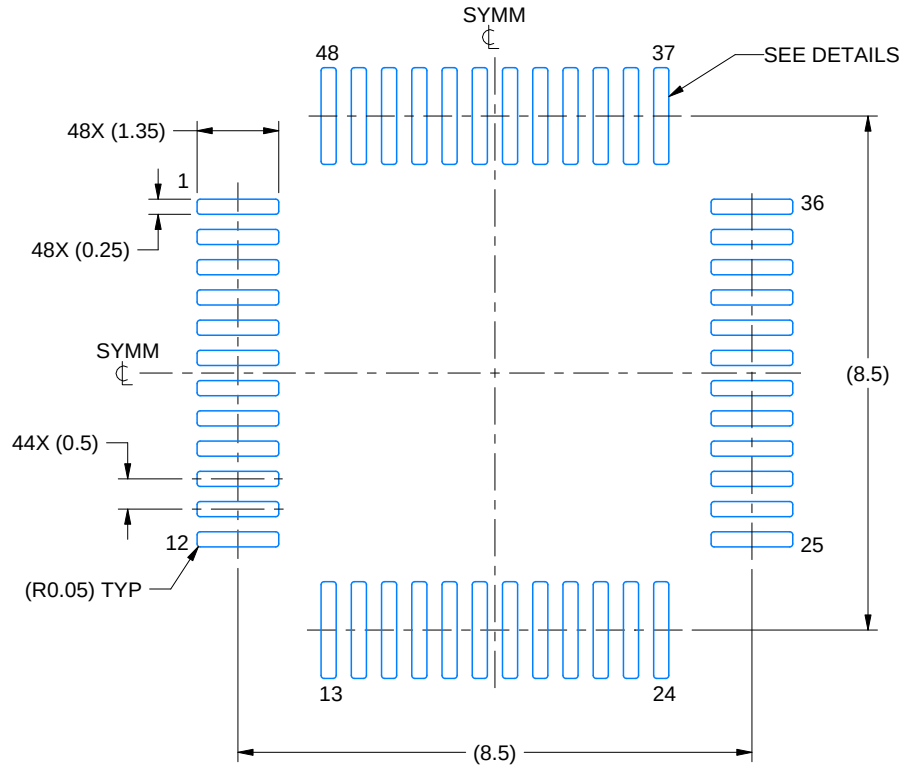


DETAIL A
TYPICAL

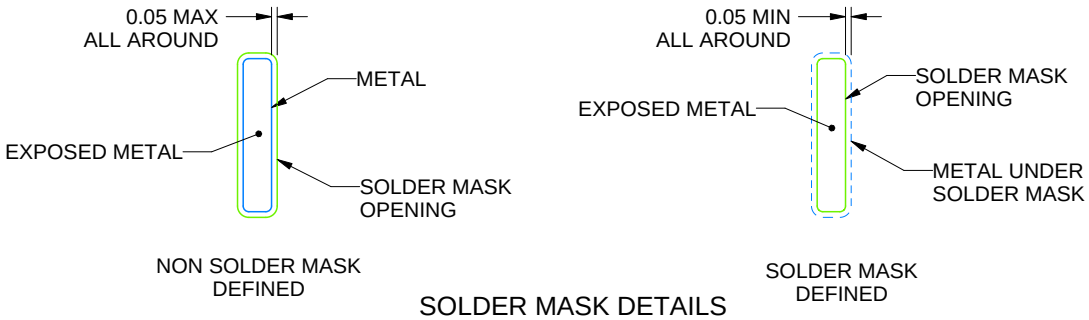
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

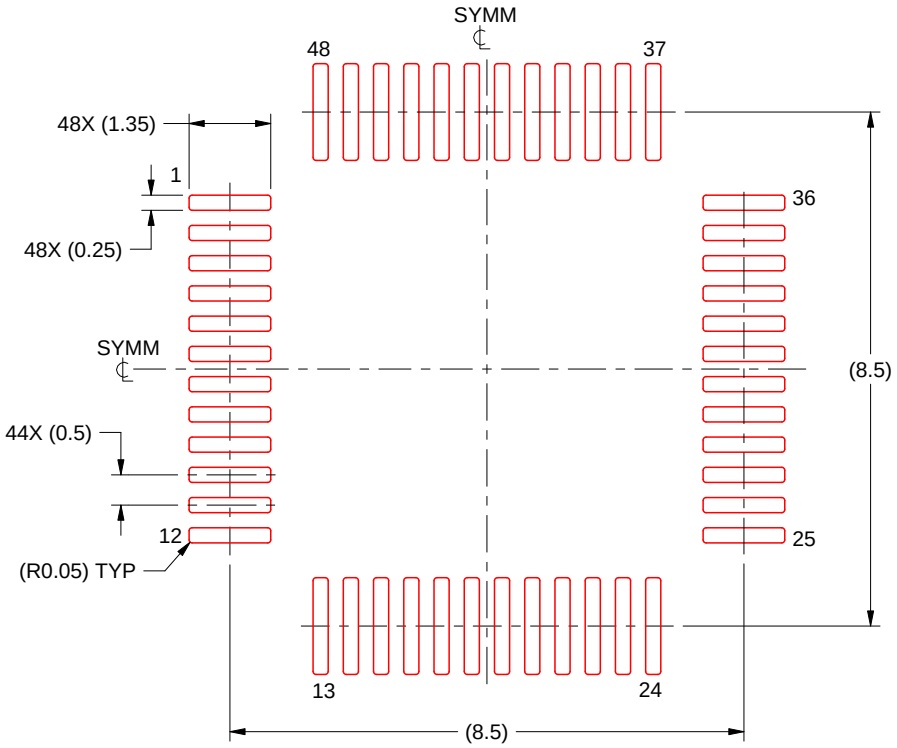


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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