BQ2405x 1-A、シングル・セル・リチウムイオンおよびリチウムポリマ・バッテリ・チャージャ、自動アダプタおよび USB 検出機能付き

1 特長

- 充電
  - 1% の充電電圧精度
  - 10% の充電電流精度
  - 最大入力電流制限として USB 100mA と 500mA をピン選択可能
  - 終端とプリチャージのスレッショルドをプログラム可能
- 保護
  - 入力定格 30V、6.6V の入力過電圧保護機能付き
  - 入力電圧のダイナミックな電源管理
  - 125℃のサーマル・レギュレーション、150℃のサーマル・シャットダウン保護
  - OUT 短絡保護および ISET 短絡検出
  - バッテリ NTC により JEITA 範囲全体で動作 - 低温時は ½ 高速充電電流、高温時は 4.06V
  - 固定の 10 時間安全タイマ
- システム
  - 自動入力ソース検出 (D+ ピン、D– ピン)
    - デバイス・トランシーバ不要
    - USB 対応
  - サーミスタ付きバッテリ・パックがない場合の自動終端およびタイマ・ディスエーブル・モード (TTDM)
  - ステータス表示 - 充電中/完了
  - 小型 2mm × 2mm パッケージで供給

2 アプリケーション

- ヘッドホン、スピーカ、オーディオ・アクセサリ
- リストバンドとウェアラブル
- スマート・ドア・ロック
- 低消費電力のハンドヘルド・デバイス

3 概要

BQ2405x シリーズのデバイスは、スペースに制約のあるポータブル・アプリケーションを対象とした高集積リチウムイオンおよびリチウムポリマ・リニア・チャージャ・デバイスです。これらのデバイスは、USB ポートまたは AC アダプタで動作します。入力電圧範囲が高く、入力過電圧保護が搭載されているため、レギュレーションのない低コストのアダプタもサポートできます。

BQ2405x には、バッテリを充電する電源出力が 1 つあります。平均システム負荷によって 10 時間の安全タイマ内でバッテリをフル充電できなくならない限り、バッテリと並行してシステム負荷を使用できます。

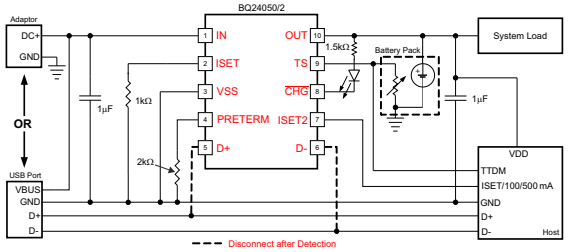
バッテリの充電は、コンディショニング、定電流、定電圧の 3 フェーズで行われます。すべての充電フェーズで、内部の制御ループが IC の接合部温度を監視し、内部温度スレッショルドを超えた場合には充電電流を減少させます。

充電器の出力段と、充電電流検出機能は、完全に統合されています。チャージャには、高精度の電流および電圧レギュレーション・ループ、充電ステータスの表示、および充電終了の機能があります。プリチャージ電流および終了電流スレッショルドは、外部抵抗を介してプログラムできます。高速充電電流値も外部抵抗を介してプログラムできます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
BQ24050	WSON (10)	2.00mm × 2.00mm
BQ24052		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (December 2014) to Revision D (May 2021) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- データシートから BQ24055 を削除。 ... 1
- 「アプリケーション」の一覧を変更 ... 1
- Deleted $\overline{PG}$ pin information from the *Specifications* section ... 5
- Moved T_{stg} From: *ESD Ratings* To: *Absolute Maximum Ratings* ... 5
- Changed the *Handling Ratings* table To: *ESD Ratings* table ... 5
- Changed $I_{BD-Sink}$ minimum from 7 mA to 6 mA ... 6
- Changed I_{IH} Source current required for HI from 8 µA to 9.6 µA ... 6
- Deleted graphs "OVP 8-V Adapter – Hot Plug" and "OVP from Normal Operation" from the *Power Up, Down, OVP, Disable and Enable Waveforms* section ... 11
- Deleted graph "Entering and Exiting Sleep Mode" from the *Battery Removal With Fixed TS = 0.5 V* section ... 13
- Changed text From: "2-mm × 2-mm or 2-mm × 3-mm single-cell Li-Ion..." To: "2-mm × 2-mm single-cell Li-Ion..." in the first paragraph of the *Overview* section ... 15
- Deleted the PG pin information from the *Feature Description* section ... 17
- Deleted text "the $\overline{PG}$ pin goes low." from the *Overvoltage Protection (OVP) – Continuously Monitored* section ... 19
- Deleted the PG pin information from the *Device Functional Modes* section ... 25
- Deleted the PG pin information from the *Application and Implementation* section ... 26
- Removed the Vpg curve from 図 8-3 and 図 8-4 ... 27

Changes from Revision B (June 2012) to Revision C (December 2014) — **Page**

- 「取り扱い定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

Changes from Revision A (September 2009) to Revision B (June 2012) — **Page**

- リチウムイオンのすべてのオカレンスを以下のように変更：リチウムイオンとリチウムポリマ ... 1

Changes from Revision * (August 2009) to Revision A (September 2009) **Page**

- 文書のステータスを以下のように変更:「製品プレビュー」から「量産データ」..... 1

5 Pin Configuration and Functions

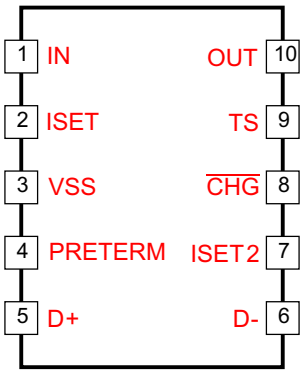


図 5-1. DSQ Package 10-Pin WSON With Exposed Thermal Pad BQ24050/BQ24052 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CHG}$	8	O	Low (FET on) indicates charging and Open Drain (FET off) indicates no Charging or Charge complete.
D+	5	I	USB port D+ input connection
D–	6	I	USB port D– input connection
IN	1	I	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1 µF to 10 µF, connect from IN to V_{SS}.
ISET	2	I	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is 52.3k (10 mA) to 540 Ω (1 A).
ISET2	7	I	Programming the Input/Output Current Limit for the USB or Adaptor source: High = 500 mA max, Low = ISET, FLOAT = 100 mA max. D+D– Detection initially sets the charge threshold and requires ISET2 to change states to take control.
OUT	10	O	Battery Connection. System Load may be connected. Average load should not be excessive, allowing battery to charge within the 10-hour safety timer window. Expected range of bypass capacitors 1 µF to 10 µF.
PRE-TERM	4	I	Programs the Current Termination Threshold (5 to 50% of Iout which is set by ISET) and Sets the Precharge Current to twice the Termination Current Level. Expected range of programming resistor is 1k to 10 kΩ (2k: I_{OUT}/10 for term; I_{OUT}/5 for precharge)
TS	9 (1)	I	Temperature sense pin connected to ‘50 — 10k at 25°C NTC thermistor, ’52 — 100k NTC at 25°C, in the battery pack. Floating TS Pin or pulling High puts part in TTDM and disable TS monitoring, Timers and Termination. Pulling pin Low disables the IC (CE function). If NTC sensing is not needed, connect this pin to VSS through an external ‘50 — 10-kΩ /’52—100-kΩ resistor. A ‘50 — 250-kΩ/’52 880-kΩ from TS to ground will prevent IC entering TTDM when battery with thermistor is removed.
VSS	3	–	Ground terminal
Thermal Pad	Pad 2x2mm^2	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

(1) Spins have different pin definitions

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	IN (with respect to VSS)	–0.3	30	V
	OUT (with respect to VSS)	–0.3	7	V
	PRE-TERM, ISET, ISET2, TS, $\overline{CHG}$, D+, D–, (with respect to VSS)	–0.3	7	V
Input Current	IN		1.25	A
Output Current (Continuous)	OUT		1.25	A
Output Sink Current	$\overline{CHG}$		15	mA
Junction temperature, T_J		–40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

		MIN	NOM	UNIT
V_{IN}	IN voltage range	3.5	28	V
	IN operating voltage range, Restricted by V_{DPM} and V_{OVP}	4.45	6.45	V
I_{IN}	Input current, IN pin		1.0	A
I_{OUT}	Current, OUT pin		1.0	A
T_J	Junction temperature	0	125	°C
$R_{PRE-TERM}$	Programs precharge and termination current thresholds	1	10	kΩ
R_{ISET}	Fast-charge current programming resistor	0.540	52.3	kΩ
R_{TS}	10k NTC thermistor range without entering TTDM, BQ24050	1.66	258	kΩ
	100k NTC thermistor range without entering TTDM, BQ24052	24	885	kΩ

(1) Operation with V_{IN} less than 4.5 V or in drop-out may result in reduced performance.

6.4 Thermal Information

THERMAL METRIC[1]		BQ24050 BQ24052 DSQ (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	
ψ_{JT}	Junction-to-top characterization parameter	7.8	
ψ_{JB}	Junction-to-board characterization parameter	34.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out Exit	V_{IN}: 0V → 4V Update based on sim/char	3.15	3.3	3.45	V
V_{HYS_UVLO}	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 4V→0V, $V_{UVLO\_FALL} = V_{UVLO\_RISE} – V_{HYS-UVLO}$	175	230	280	mV
V_{IN-DT}	Input power good detection threshold is $V_{OUT} + V_{IN-DT}$	(Input power good if $V_{IN} > V_{OUT} + V_{IN-DT}$); V_{OUT} = 3.6V, V_{IN}: 3.5V → 4V	30	80	145	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6V, V_{IN}: 4V → 3.5V		31		mV
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5V → 7V (50/52)	6.5	6.65	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11V → 5V		95		mV
V_{IN-DPM}	USB/Adaptor low input voltage protection. Restricts Iout at V_{IN-DPM}	Feature active in USB mode; Limit Input Source Current to 50mA; V_{OUT} = 3.5V; R_{ISET} = 825Ω	4.34	4.4	4.46	V
		Feature active in Adaptor mode; Limit Input Source Current to 50mA; V_{OUT} = 3 .5V; R_{ISET} = 825Ω	4.24	4.3	4.36	
$I_{IN-USB-CL}$	USB input I-Limit 100 mA	ISET2 = Float; R_{ISET} = 825Ω	85	92	100	mA
	USB input I-Limit 500 mA	ISET2 = High; R_{ISET} = 825Ω	430	462	500	
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest Resistor value considered a fault (short). Monitored for Iout>90mA	Riset: 600Ω → 250Ω, Iout latches off. Cycle power to Reset. USB100 mode.	280		500	Ω
I_{OUT_CL}	Maximum OUT current limit Regulation (Clamp)	V_{IN} = 5V, V_{OUT} = 3.6V, V_{ISET2} = Low, Riset: 600Ω → 250Ω, I_{OUT} latches off after $t_{DGL-SHORT}$	1.05		1.4	A
BATTERY SHORT PROTECTION						
$V_{OUT(SC)}$	OUT pin short-circuit detection threshold/ precharge threshold	V_{OUT}: 3V → 0.5V, no deglitch	0.75	0.8	0.85	V
$V_{OUT(SC-HYS)}$	OUT pin Short hysteresis	Recovery ≥ $V_{OUT(SC)} + V_{OUT(SC-HYS)}$; Rising, no Deglitch		77		mV
$I_{OUT(SC)}$	Source current to OUT pin during short-circuit detection		10	15	20	mA
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT pin	V_{IN} = 0V			1	μA
$I_{OUT(DONE)}$	OUT pin current, charging terminated	V_{IN} = 6V, $V_{OUT} > V_{OUT(REG)}$			6	
$I_{IN(STDBY)}$	Standby current into IN pin	TS = LO, V_{IN} ≤ 6V			125	μA
I_{CC}	Active supply current, IN pin	TS = open, V_{IN} = 6V, TTDM – no load on OUT pin, $V_{OUT} > V_{OUT(REG)}$, IC enabled		0.8	1	mA
BATTERY CHARGER FAST-CHARGE						
$V_{OUT(REG)}$	Battery regulation voltage	V_{IN} = 5.5V, I_{OUT} = 25mA, $V_{TS-45°C} ≤ V_{TS} ≤ V_{TS-0°C}$	4.16	4.20	4.23	V

6.5 Electrical Characteristics (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O\_HT(REG)}$	Battery hot regulation Voltage	V_{IN} = 5.5V, I_{OUT} = 25mA, $V_{TS-60°C}$ ≤ V_{TS} ≤ $V_{TS-45°C}$	4.02	4.06	4.1	V
$I_{OUT(RANGE)}$	Programmed Output “fast charge” current range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}, V_{IN} = 5V, ISET2=Lo, R_{ISET} = 675 to 10.8kΩ	10		800	mA
$V_{DO(IN-OUT)}$	Drop-Out, VIN – VOUT	Adjust VIN down until I_{OUT} = 0.5A, V_{OUT} = 4.15V, R_{ISET} = 675 , ISET2 = Lo (Adaptor Mode); Tj ≤ 100°C		325	500	mV
I_{OUT}	Output “fast charge” formula	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}, V_{IN} = 5V, ISET2 = Lo		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor	R_{ISET} = K_{ISET} /I_{OUT} 50 < I_{OUT} < 1 A	510	540	570	AΩ
		R_{ISET} = K_{ISET} /I_{OUT} 25 < I_{OUT} < 50 mA	480	527	600	
		R_{ISET} = K_{ISET} /I_{OUT} 10 < I_{OUT} < 25 mA	350	520	680	
PRECHARGE – SET BY PRETERM PIN						
V_{LOWV}	Precharge to fast-charge transition threshold		2.4	2.5	2.6	V
$t_{DGL1(LOWV)}$	Deglitch time on precharge to fast-charge transition			70		µs
$I_{PRE-TERM}$	Refer to the Termination Section					
$\%_{PRECHG}$	Precharge Current Level, Default Setting	V_{OUT} < V_{LOWV}; **$R_{PRE-TERM}$ = High Z** (≥13kΩ); R_{ISET} = 1k	18	20	22	$\%I_{OUT-CC}$
	Precharge current formula	$R_{PRE-TERM}$ = $K_{PRE-CHG}$ (Ω/%) × $\%_{PRE-CHG}$ (%)		$R_{PRE-TERM}/K_{PRE-CHG}$		
$K_{PRE-CHG}$	% Precharge Factor	V_{OUT} < V_{LOWV}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2k to 10kΩ; R_{ISET} = 1080Ω , $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 20 to 100%	90	100	110	Ω/%
		V_{OUT} < V_{LOWV}, V_{IN} = 5V, $R_{PRE-TERM}$ = 1k to 2kΩ; R_{ISET} = 1080Ω, $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10% to 20%	84	100	117	Ω/%
TERMINATION – SET BY PRE-TERM PIN						
$\%_{TERM}$	Termination Current Threshold, Default Setting	V_{OUT} > V_{RCH}; **$R_{PRE-TERM}$ = High Z** (≥13kΩ); R_{ISET} = 1k	9	10	11	$\%I_{OUT-CC}$
	Termination Current Threshold Formula	$R_{PRE-TERM}$ = K_{TERM} (Ω/%) × %TERM (%)		$R_{PRE-TERM}/ K_{TERM}$		
K_{TERM}	% Term Factor	V_{OUT} > V_{RCH}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2k to 10kΩ ; R_{ISET} = 750Ω; K_{TERM} × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10 to 50%	182	200	216	Ω/%
		V_{OUT} > V_{RCH}, V_{IN} = 5V, $R_{PRE-TERM}$ = 1k to 2kΩ ; R_{ISET} = 750Ω; K_{TERM} × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 5 to 10%	174	199	224	
$I_{PRE-TERM}$	Current for programming the term. and precharge with resistor. $I_{Term-Start}$ is the initial PRE-TERM curent.	$R_{PRE-TERM}$ = 2k, V_{OUT} = 4.15V	71	75	81	µA
%TERM	Termination current formula			R_{TERM}/ K_{TERM}		
$I_{Term-Start}$	Elevated PRE-TERM current for, $t_{Term-Start}$, during start of charge to prevent recharge of full battery,		80	85	92	µA
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold – Normal Temp	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT}: 4.25V → V_{RCH}	$V_{O(REG)}$– 0.120	$V_{O(REG)}$ – 0.095	$V_{O(REG)}$– 0.070	V
	Recharge detection threshold – Hot Temp	V_{IN} = 5V, V_{TS} = 0.2V, V_{OUT}: 4.15V → V_{RCH}	$V_{O\_HT(REG)}$ –0.130	$V_{O\_HT(REG)}$ –0.105	$V_{O\_HT(REG)}$ –0.080	V
BATTERY DETECT ROUTINE(1)						
V_{REG-BD}	VOUT Reduced regulation during battery detect	V_{IN} = 5V, V_{TS} = 0.5V, Battery Absent	$V_{O(REG)}$– 0.450	$V_{O(REG}$– 0.400	$V_{O(REG)}$– 0.350	V
$I_{BD-SINK}$	Sink current during V_{REG-BD}		6		10	mA
V_{BD-HI}	High battery detection threshold	V_{IN} = 5V, V_{TS} = 0.5V, Battery Absent	$V_{O(REG)}$– 0.150	$V_{O(REG)}$– 0.100	$V_{O(REG)}$– 0.050	V
V_{BD-LO}	Low battery detection threshold	V_{IN} = 5V, V_{TS} = 0.5V, Battery Absent	V_{REG-BD} +0.050	V_{REG-BD} +0.100	V_{REG-BD} +0.150	V

6.5 Electrical Characteristics (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY-PACK NTC MONITOR[2]						
$I_{NTC-10k}$	NTC bias current; 10k NTC thermistor, BQ24050	V_{TS} = 0.3V	48	50	52	µA
$I_{NTC-100k}$	NTC bias current; 100k NTC thermistor, BQ24052	V_{TS} = 0.3V	4.8	5	5.2	µA
$I_{NTC-DIS-10k}$	BQ24050 bias current when Charging is disabled.	V_{TS} = 0V	27	30	34	µA
$I_{NTC-DIS-100k}$	BQ24052 bias current when Charging is disabled.	V_{TS} = 0V	4.4	5	5.8	µA
$I_{NTC-FLDBK-10k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM, BQ24050	V_{TS}: Set to 1.525V	4	5	6.5	µA
$I_{NTC-FLDBK-100k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM, BQ24052	V_{TS}: Set to 1.525V	1.1	1.5	1.9	µA
$V_{TTDM(TS)}$	Termination and timer disable mode Threshold – Enter	V_{TS}: 0.5V → 1.7V; Timer Held in Reset	1550	1600	1650	mV
$V_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7V → 0.5V; Timer Enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS}= Open (Float)	1800	1950	2000	mV
$V_{TS\_I-FLDBK}$	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6uA) takes place near this spec threshold. V_{TS}: 1.425V → 1.525V		1475		mV
C_{TS}	Optional Capacitance – ESD			0.22		µF
$V_{TS-0°C}$	BQ2405x Low temperature CHG Pending	Low Temp Charging to Pending; V_{TS}: 1V → 1.5V	1205	1230	1255	mV
$V_{HYS-0°C}$	Hysteresis at 0°C	Charge pending to low temp charging; V_{TS}: 1.5V → 1V		86		mV
$V_{TS-10°C}$	Low temperature, half charge	Normal charging to low temp charging; V_{TS}: 0.5V → 1V	765	790	815	mV
$V_{HYS-10°C}$	Hysteresis at 10°C	Low temp charging to normal CHG; V_{TS}: 1V → 0.5V		35		mV
$V_{TS-45°C}$	High temperature at 4.1V	Normal charging to high temp CHG; V_{TS}: 0.5V → 0.2V	263	278	293	mV
$V_{HYS-45°C}$	Hysteresis at 45°C	High temp charging to normal CHG; V_{TS}: 0.2V → 0.5V		10.7		mV
$V_{TS-60°C}$	High temperature Disable	High temp charge to pending; V_{TS}: 0.2V → 0.1V	170	178	186	mV
$V_{HYS-60°C}$	Hysteresis at 60°C	Charge pending to high temp CHG; V_{TS}: 0.1V → 0.2V		11.5		mV
$V_{TS-EN-10k}$	Charge Enable Threshold, (10k NTC)	V_{TS}: 0V → 0.175V;	80	88	96	mV
$V_{TS-DIS\_HYS-10k}$	HYS below $V_{TS-EN-10k}$ to Disable, (10k NTC)	V_{TS}: 0.125V → 0V;		12		mV
$V_{TS-EN-100k}$	Charge Enable Threshold, (100k NTC)	V_{TS}: 0V → 0.175V	140	150	160	mV
$V_{TS-DIS\_HYS-100k}$	HYS below $V_{TS-EN-100k}$ to Disable, (100k NTC)	V_{TS}: 0.125V → 0V;		50		mV
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON ISET2						
V_{IL}	Logic LOW input voltage	Sink more than 8µA			0.4	V
V_{IH}	Logic HIGH input voltage	Source more than 8µA	1.4			V
I_{IL}	Sink current required for LO		2		9	µA
I_{IH}	Source current required for HI		1.1		9.5	µA

6.5 Electrical Characteristics (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FLT}	ISET2 Float Voltage		650	900	1200	mV
D+/D– DETECTION – BQ2405x						
V_{D+}	Bias at D+, during detection routine	Can source at least 200µA	0.475	0.6	0.7	V
I_{D+}	Current Limit at D+ pin, during detection routine	V_{D+} = 0V			1.5	mA
$I_{D–}$	Current Sink at D– pin, during detection routine	$V_{D–}$ = 0.5V	50	100	150	µA
I_{D+_LEAK}	D+ leakage when not in detection mode	V_{D+} = 5V			1	µA
$I_{D–\_LEAK}$	D– leakage when not in detection mode	$V_{D–}$ = 5V			1	µA
$V_{DPDM\_0.4V}$	D– Comparator Threshold Rising		0.35		0.45	V
$V_{DPDM\_HYS\_0.4V}$	D– Comparator Hysteresis			42		mV
$V_{DPDM\_0.8V}$	D+/D– Comparator Threshold Rising		0.75		0.875	V
$V_{DPDM\_HYS\_0.8V}$	D+/D– Comparator Hysteresis			42		mV
LOGIC LEVELS ON $\overline{CHG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5mA			0.4	V
I_{lkg}	Leakage current into IC	$V_{\overline{CHG}}$ = 5V			1	µA

(1) In Hot Mode $V_{O(REG)}$ becomes $V_{O\_HT(REG)}$
(2) TS pin: BQ24050: 10k NTC; BQ24052: 100k NTC; see セクション 7.3.11 for thermistor information.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
PRECHARGE – SET BY PRETERM PIN					
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to precharge transition		32		ms
TERMINATION – SET BY PRE-TERM PIN					
$t_{DGL(TERM)}$	Deglitch time, termination detected		29		ms
$t_{Term-Start}$	Elevated termination threshold initially active for $t_{Term-Start}$		1.25		min
BATTERY-PACK NTC MONITOR(2)					
$t_{DGL(TTDM)}$	Deglitch exit TTDM between states		57		ms
	Deglitch enter TTDM between states		8		µs

6.7 Switching Characteristics

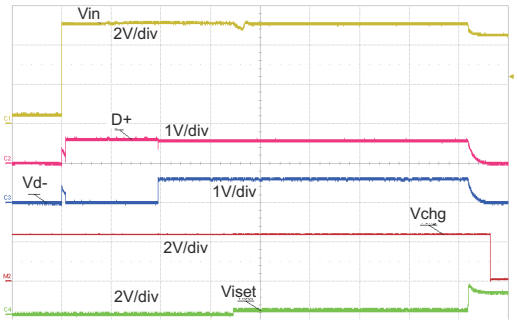
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
$t_{DGL(OVP-SET)}$	Input overvoltage blanking time	V_{IN}: 5V → 12V		113		µs
$t_{DGL(OVP-REC)}$	Deglitch time exiting OVP	Time measured from V_{IN}: 12V → 5V		30		µs
ISET SHORT CIRCUIT TEST						
t_{DGL_SHORT}	Deglitch time transition from ISET short to Iout disable	Clear fault by cycling IN or TS		1		ms
RECHARGE OR REFRESH						
$t_{DGL1(RCH)}$	Deglitch time, recharge threshold detected	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT}: 4.25V → 3.5V in 1µs; $t_{DGL1(RCH)}$ is time to ISET ramp		29		ms
$t_{DGL2(RCH)}$	Deglitch time, recharge threshold detected in OUT-Detect Mode	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT} = 3.5V inserted; $t_{DGL2(RCH)}$ is time to ISET ramp		3.6		ms
BATTERY DETECT ROUTINE(1)						
$t_{DGL(HI/LOW\ REG)}$	Regulation time at V_{REG} or V_{REG-BD}	V_{IN} = 5V, V_{TS} = 0.5V, Battery Absent		25		ms
BATTERY CHARGING TIMERS AND FAULT TIMERS						
t_{PRECHG}	Precharge safety timer value	Restarts when entering precharge; Always enabled when in precharge.	1700	1940	2250	s
t_{MAXCH}	Charge safety timer value	Clears fault or resets at UVLO, TS (*CE*) disable, OUT Short, exiting LOWV and Refresh	34000	38800	45000	s
BATTERY-PACK NTC MONITOR(2)						
$t_{DGL(TS\_10C)}$	Deglitch for TS thresholds: 10°C	Normal to Cold Operation: V_{TS}: 0.6V → 1V		40		ms
		Cold to Normal Operation: V_{TS}: 1.0V → 0.6V		12		ms
$t_{DGL(TS)}$	Deglitch for TS thresholds: 0/45/60C.	Battery charging		30		ms
D+/D– DETECTION – BQ2405x						
t_{DPDM}	DetectionTime from start of D+/D– detection to latched output	t = 0 at D– pulled-up > 0.5V or D+ pulled up externally, >0.8V		65		ms

6.8 Typical Characteristics

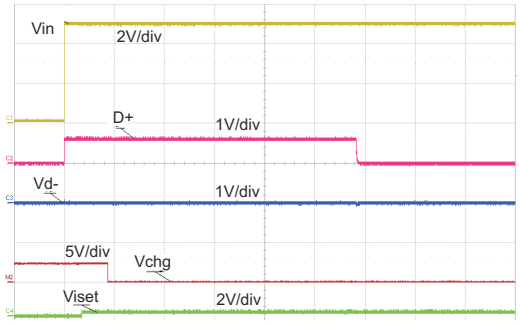
SETUP: BQ24050, BQ24052 typical applications schematic; V_{IN} = 5 V, V_{BAT} = 3.6 V (unless otherwise indicated)
R_{ISET} = 1k; $I_{OUT\_FAST\_CHG}$ = 540 mA; R_{PAC_TERM} = 2k; $I_{OUT\_PRE\_CHG}$ = 108 mA; I_{OUT_TERM} = 54 mA

6.8.1 Power Up, Down, OVP, Disable and Enable Waveforms



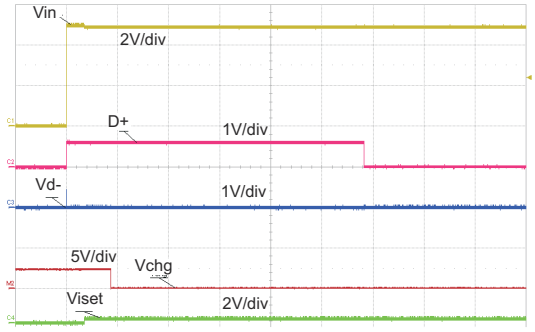
Detected D– line pulled to 0.6 V and the detection routine is started

図 6-1. D+ D– Detection for Adaptor Hot Plug



No signal detected on D+ or D–. After 500 ms, the detection routine is forced to run

図 6-2. D+ D– Detection for Unknown Source Hot Plug



(Device transceiver is "dead") After 500 ms, the detection routine is forced to run.

図 6-3. D+ D– Detection for USB Hot Plug No Pullup

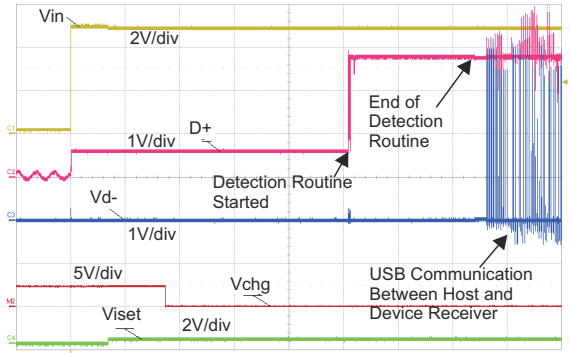
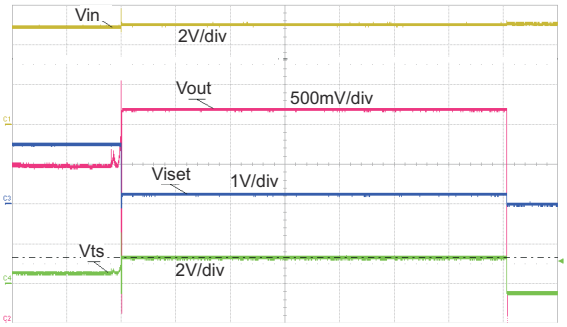
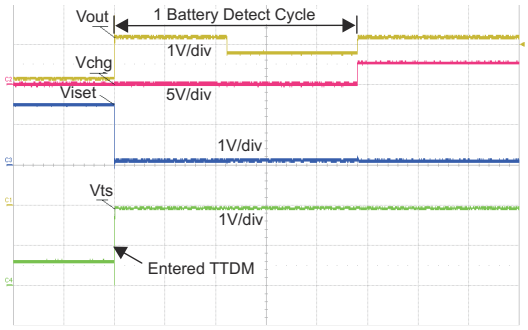


図 6-4. D+ D– Detection for USB Hot Plug With Pullup



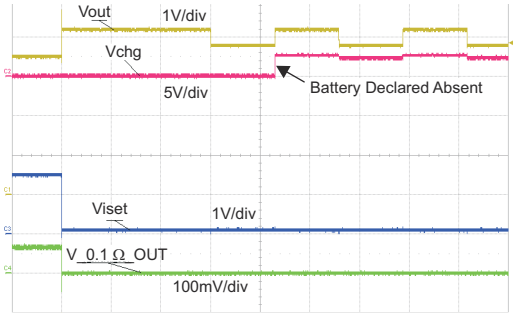
42-Ω Load

図 6-5. Battery Removal – GND Removed First



100–Ω Load

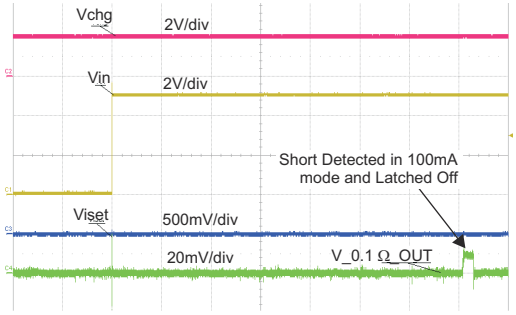
図 6-6. Battery Removal With OUT and TS Disconnect First



Continuous battery detection when not in TTDM

図 6-7. Battery Removal With Fixed TS = 0.5 V

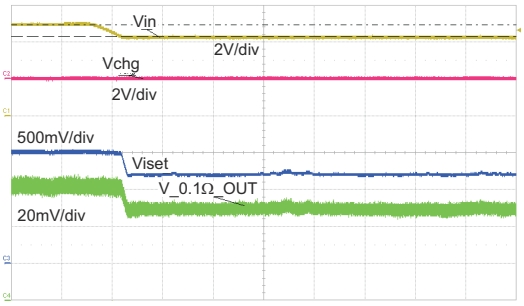
6.8.2 Protection Circuits Waveforms



t - time - 5ms/div

CH4: I_{OUT} (0.2 A/Div)

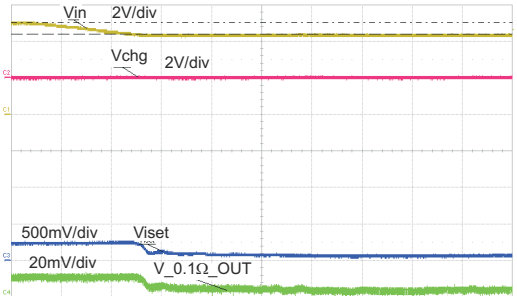
図 6-8. ISET Shorted Before USB Power Up



t - time - 1ms/div

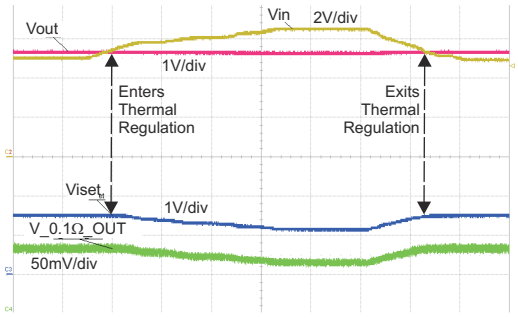
CH4: I_{OUT} (0.2 A/Div)

図 6-9. DPM – Adaptor Current Limits – V_{IN} Regulated to 4.3 V



t - time - 500µs/div

図 6-10. DPM – USB Current Limits – V_{IN} Regulated to 4.4 V



t - time - 1s/div

The IC temperature rises to 125°C and enters thermal regulation. Charge current is reduced to regulate the IC at 125°C .

VIN is reduced, the IC temperature drops, the charge current returns to the programmed value.

図 6-11. Thermal Regulator – V_{IN} Increases

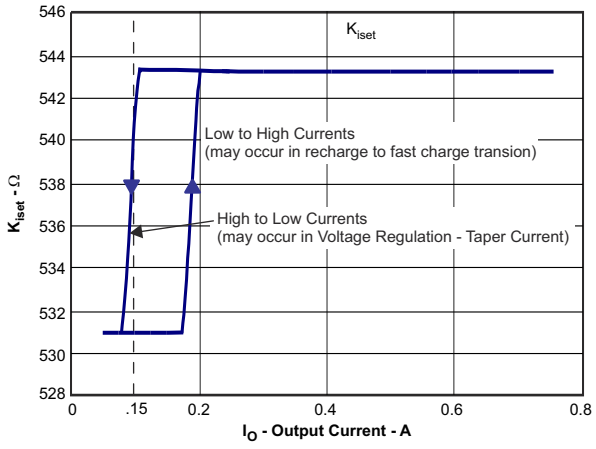


図 6-12. K_{ISET} for Low and High Currents

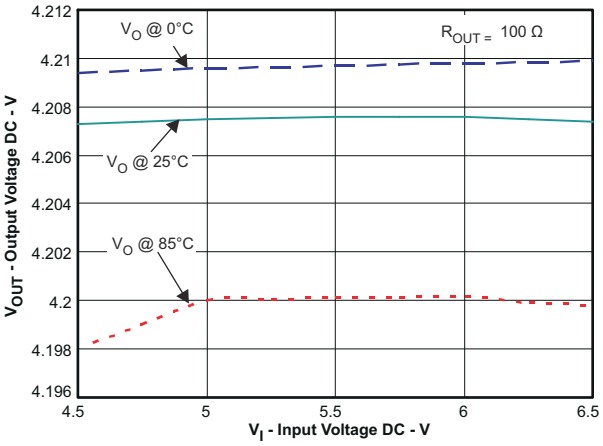


図 6-13. Line Regulation

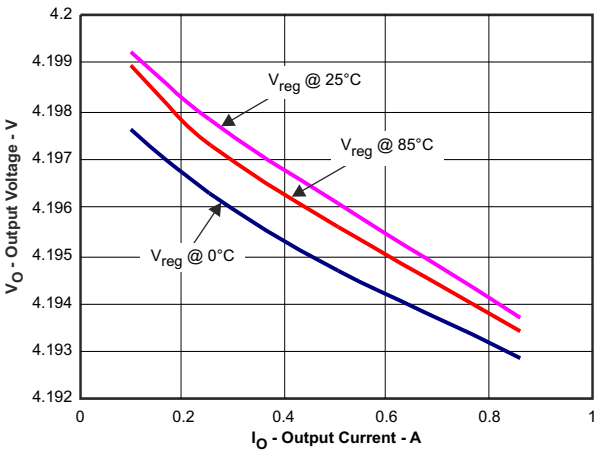


図 6-14. Load Regulation Overtemperature

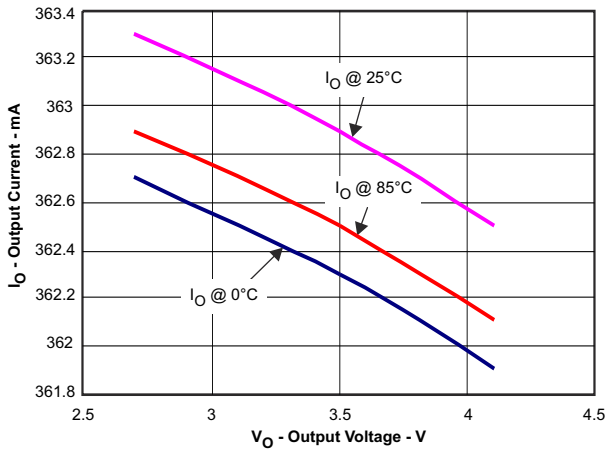


図 6-15. Current Regulation Overtemperature

7 Detailed Description

7.1 Overview

The BQ2405x is a highly integrated family of 2-mm × 2-mm single-cell Li-Ion and Li-Pol chargers. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: precharge to recover a fully discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity. The charger is flexible, allowing programming of the fast-charge current, precharge current and termination. This charger is designed to work with a USB connection or adaptor (DC out). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: JEITA Temperature Standard, Overvoltage Protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5VDC power source the D+, D– detection routine is run to determine if the source is an Adaptor or a USB port. This feature is useful, when the battery is discharged (USB transceiver dead) or there is no transceiver, by early detection of an adaptor, thus allowing initial charging at the adaptor level. ISET and OUT short checks are performed in parallel with the detection routine to assure a proper charge cycle.

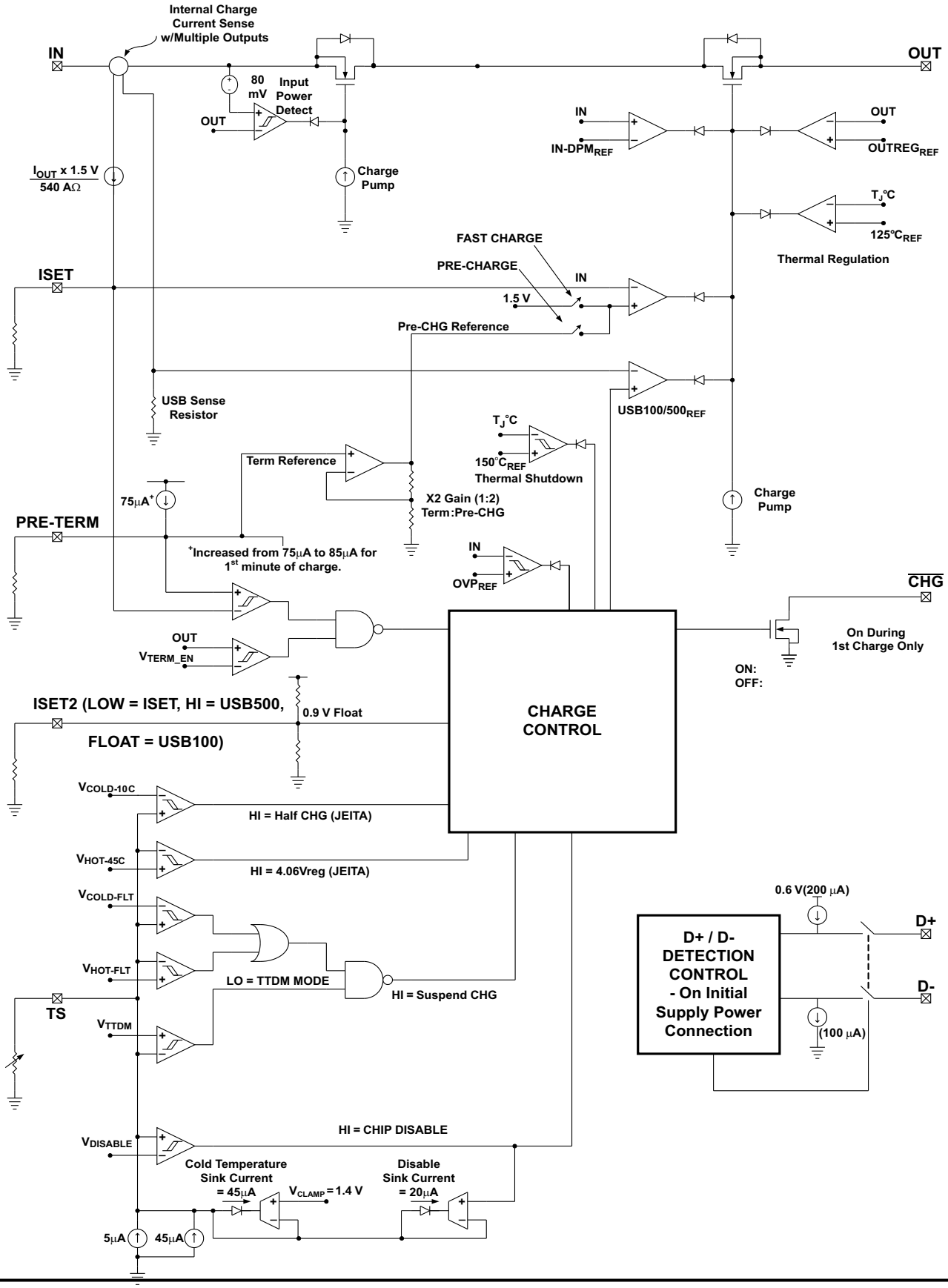
If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of precharge current can be programmed using the PRE-TERM pin which programs a percent of fast charge current (10 to 100%) as the precharge current. This feature is useful when the system load is connected across the battery *stealing* the battery current. The precharge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. The PRE-TERM pin is a dual-function pin which sets the precharge current level and the termination threshold level. The termination "current threshold" is always half of the precharge programmed current level.

Once the battery voltage has charged to the V_{LOWV} threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET pin. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C, the IC enters thermal regulation. Slow the timer clock by half and reduce the charge current as needed to keep the temperature from rising any further. 図 7-1 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC's junction temperature is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The charge termination can be disabled if desired. The $\overline{CHG}$ pin is low (LED on) during the first charge cycle only and turns off once the charge termination threshold is reached, regardless if termination is enabled or disabled.

The TS pin monitors the voltage across the pack thermistor and implements the JEITA standard. This allows for reduced voltage regulation at hot temperatures and reduced charge currents at low temperatures. The TS pin incorporates a chip disable feature when pulled low and an Termination and Timer Disable Mode (TTDM) feature when left floating or pulled high.

7.2 Functional Block Diagram



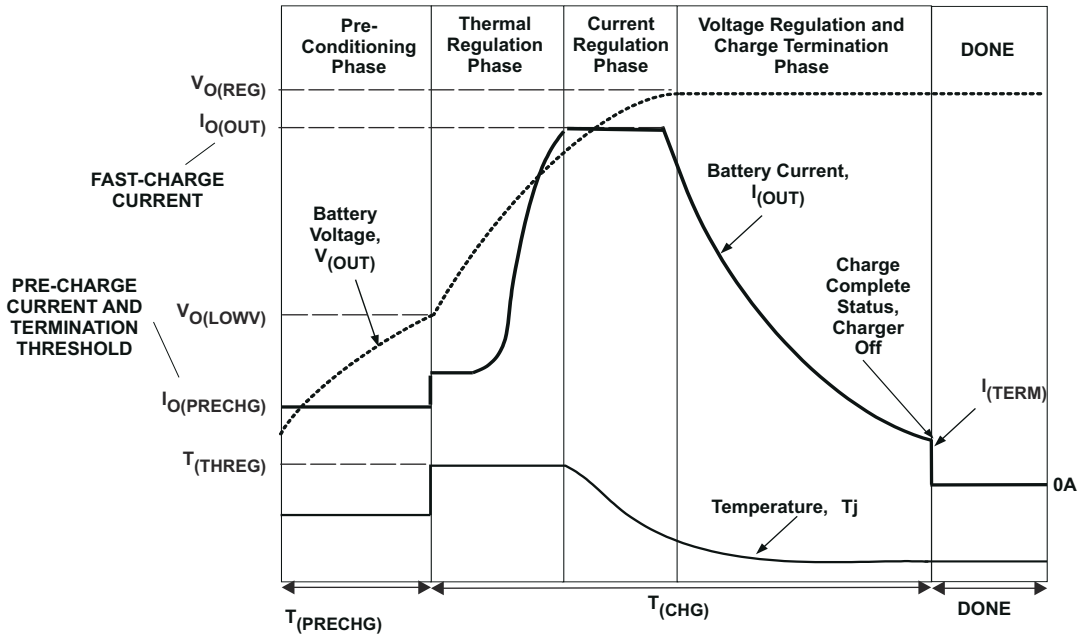


図 7-1. Charging Profile With Thermal Regulation

7.3 Feature Description

7.3.1 Power Down, or Undervoltage Lockout (UVLO)

The BQ2405x family is in power down mode if the voltage of the IN pin is less than UVLO. The part is considered *dead* and all the pins are high impedance. Once the IN voltage rises above the UVLO threshold the IC enters Sleep Mode or Active mode depending on the voltage of the OUT pin (battery).

7.3.2 Power Up

The IC is alive after the IN voltage ramps above UVLO (see セクション 7.4.1), resets all logic and timers, and starts to perform the D+D– detection along with many of the continuous monitoring routines. The D+/D– detection typically take less than 100 ms, but can take as long as 600 ms if there is no activity on the D+ or D– lines which indicates the device transceiver nor an adaptor is present. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 100 mA, finishes the USB detection routine, sets the input current limit threshold base on the source detected (ISET=adaptor or 100mA=USB), starts the safety timer, and enables the $\overline{\text{CHG}}$ pin. See 図 7-3.

7.3.3 D+, D– Detection

This detection is designed to give the charger advance notice that an adaptor or USB port is connect for the cases where the battery is discharged and device transceiver is not able to communicate with a USB host or there is not a device transceiver. If an adaptor is detected, then the charger can immediately start charging at the programmed ISET level. Without this early detection, the charger would have to default to the 100-mA input current level to make sure it was not over-loading a low power USB port. The detection method monitors the D+, D– communication lines looking for a short between the lines (Adaptor source connected) or pulldown resistors on D+, D– (USB source connected) to determine what source is connected (no USB communication takes place). If an adaptor source is detected then the charger will transition from the 100 mA startup level to the ISET programmed current level. If a USB port is detected, the input current limit will stay at the 100 mA level. If a different charge level is desired, than the one detected, the host has to change the state of the ISET2 pin (signals the internal logic to start using the ISET2 as the program pin) and then set to the desired state.

The D+ and D– pin connections inside the charger are disconnected within 100 ms of the D+ or D– lines being pulled high (start of detection), to minimize any interaction between the charger detection pins and the USB normal communications. If the device transceiver is able to communicate with the USB host, communication

typically starts after 100 ms after the device has pulled the D+ or D– line high indicating it is “on line”, and by then the IC detection is complete and has been disconnected. The device host then may change the ISET2 level or disable the IC by pulling the TS pin low.

7.3.4 New Charge Cycle

A new charge cycle is started when a good power source is applied, performing a chip disable/enable (TS pin), exiting Termination and Timer Disable Mode (TTDM), detecting a battery insertion or the OUT voltage dropping below the VRCH threshold. The $\overline{CHG}$ pin is active low only during the first charge cycle, therefore exiting TTDM or a dropping below VRCH will not turn on the $\overline{CHG}$ pin FET, if the $\overline{CHG}$ pin is already high impedance.

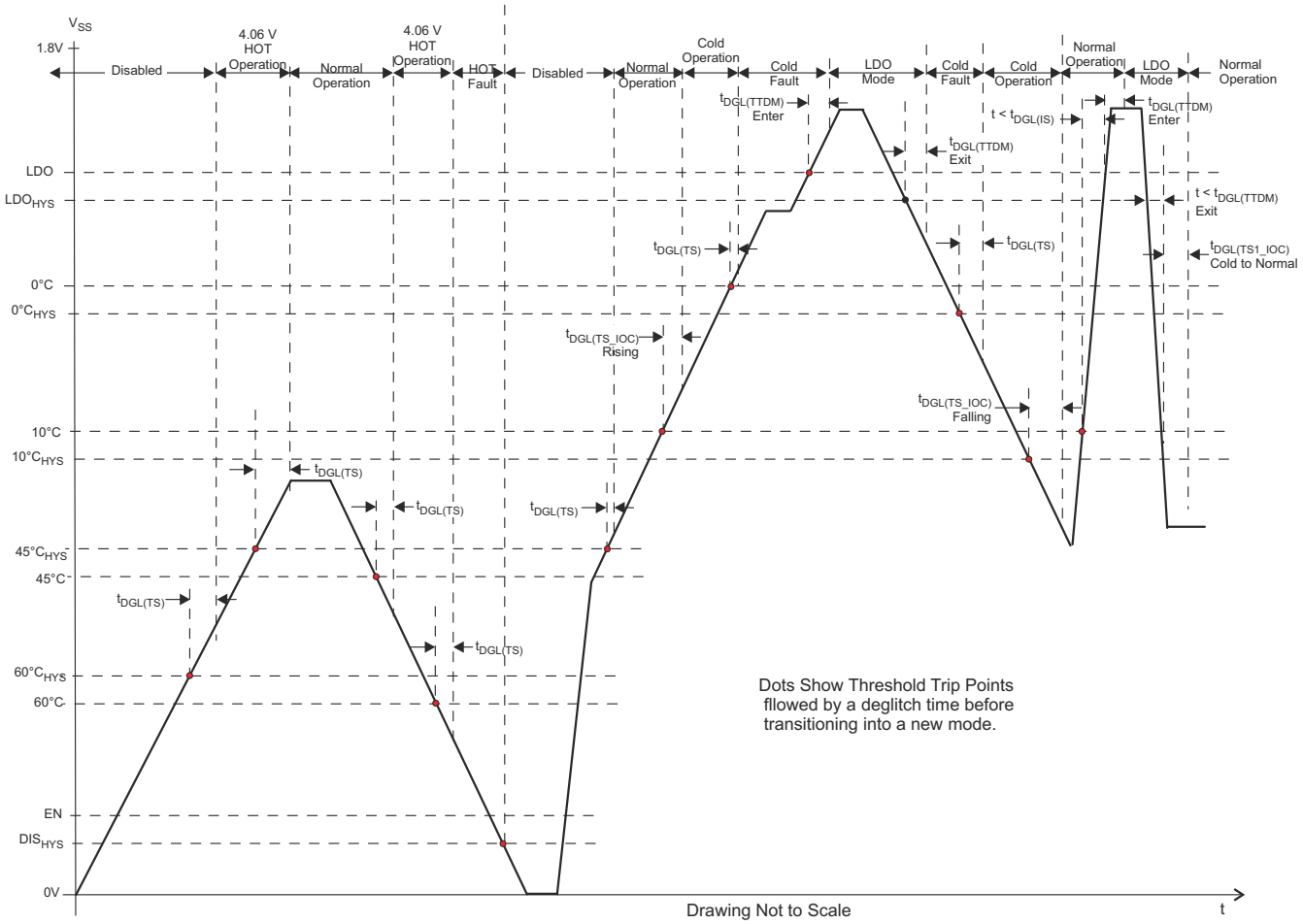


図 7-2. TS Battery Temperature Bias Threshold and Deglitch Timers

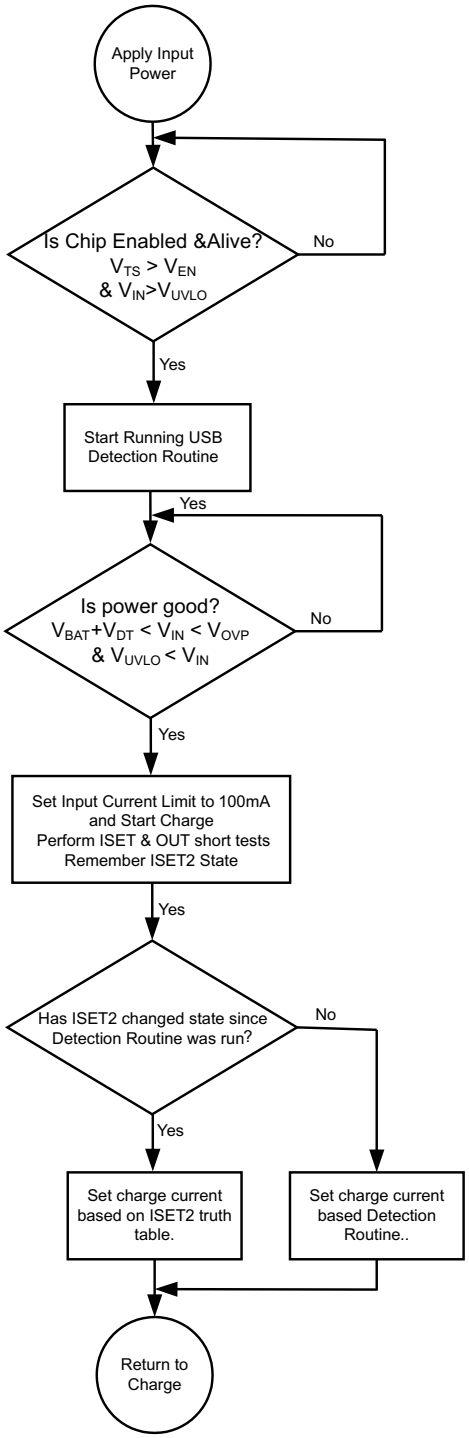


図 7-3. Power Up Flow Diagram

7.3.5 Overvoltage Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the $\overline{CHG}$ pin goes to a high impedance state. Once the overvoltage returns to a normal voltage, timer continues, charge continues and the $\overline{CHG}$ pin goes low after a 25-ms deglitch.

7.3.6 CHG Pin Indication

The charge pin has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor.

The charge pin will be high impedance in sleep mode and OVP and return to its previous state when the condition is removed.

Cycling input power, pulling the TS pin low and releasing or entering precharge mode will cause the $\overline{CHG}$ pin to reset and is considered the start of a first charge.

7.3.7 $\overline{CHG}$ LED Pullup Source

For host monitoring, a pullup resistor is used between the *STATUS* pin and the V_{CC} of the host and for a visual indication a resistor in series with an LED is connected between the *STATUS* pin and a power source. If the $\overline{CHG}$ source can exceed 7 V, a 6.2-V Zener diode should be used to clamp the voltage. If the source is the OUT pin, note that as the battery changes voltage, the brightness of the LEDs vary.

CHARGING STATE	$\overline{CHG}$ FET/LED
1st Charge	ON
Refresh Charge	OFF
OVP	
SLEEP	
TEMP FAULT	ON for 1st Charge

7.3.8 Input DPM Mode (V_{IN}-DPM or IN-DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to an excessive load. When the input voltage drops to the V_{IN-DPM} threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than V_{IN-DPM} to power the out pin. This works well with current limited adaptors and USB ports as long as the nominal voltage is above 4.3 V and 4.4 V respectively. This is an added safety feature that helps protect the source from excessive loads.

7.3.9 OUT

The OUT pin of the charger provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT pin is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

7.3.10 ISET

An external resistor is used to Program the Output Current (10 mA to 1.0 A) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} \div I_{OUT} \quad (1)$$

Where:

I_{OUT} is the desired fast charge current;
K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. 図 6-12 shows the transition from low current to higher current. Going from higher currents to low currents, there is hysteresis and the transition occurs around 0.15 A.

The ISET resistor is short protected and will detect a resistance lower than ≠340 Ω. The detection requires at least 80 mA of output current. If a “short” is detected, then the IC will latch off and can only be reset by cycling the power. The OUT current is internally clamped to a maximum current between 1.05 A and 1.4 A and is independent of the ISET short detection circuitry, as shown in 図 7-5. Also, see 図 8-2 and 図 6-8.

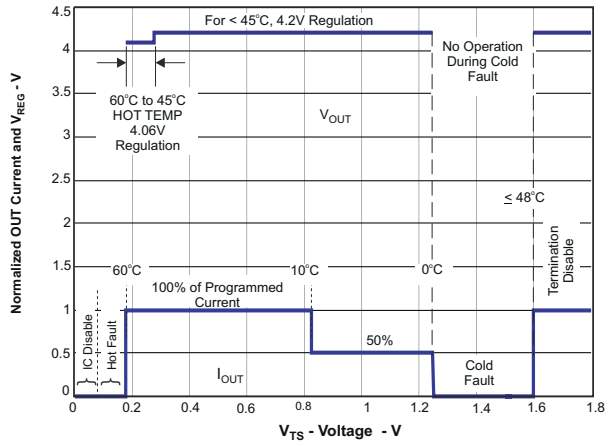


図 7-4. Operation Over TS Bias Voltage

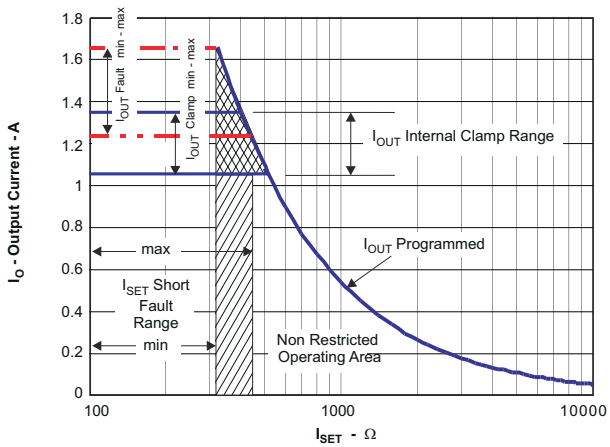


図 7-5. Programmed / Clamped Out Current

7.3.11 TS

The TS pin is designed to follow the new JEITA temperature standard for Li-Ion and Li-Pol batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs from 10°C to 45°C. If between 0°C and 10°C the charge current level is cut in half and if between 45°C and 60°C the regulation voltage is reduced to 4.1 Vmax, see 図 7-4. The TS feature is implemented using an internal 50-µA current source to bias the thermistor (BQ24050 designed for use with a 10k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F), and BQ24052 with a 100k NTC β = 3540 (Mitsubishi TH05-36104F) or equivalent) connected from the TS pin to V_{SS}. If this feature is not needed, a fixed 10k can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS pin low to disable charge.

The TS pin has two additional features, when the TS pin is pulled low or floated/driven high. A low disables charge (similar to a CE feature) and a high puts the charger in TTDM.

Above 60°C or below 0°C the charge is disable. Once the thermistor reaches ≠–10°C the TS current folds back to keep a cold thermistor (from –10°C to –50°C) from placing the IC in the TTDM mode. If the TS pin is pulled low into disable mode, the current is reduce to ≠30 µA, see 図 7-2. Because the I_{TS} current is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10k and 100k.

7.3.12 Termination and Timer Disable Mode (TTDM) -TS Pin High

The battery charger is in TTDM when the TS pin goes high from removing the thermistor (removing battery pack/ floating the TS pin) or by pulling the TS pin up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. If the battery was removed then the $\overline{CHG}$ pin will go to its high impedance state if not already there. If a battery is detected the $\overline{CHG}$ pin does not change states until the current tapers to the termination threshold, where the $\overline{CHG}$ pin goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has precharge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the $\overline{CHG}$ LED turns on.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237k resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS pin into TTDM. This creates ≠0.1°C error at hot and a ≠3°C error at cold.

7.3.13 Timers

The precharge timer is set to 30 minutes . The precharge current, can be programmed to offset any system load, making sure that the 30 minutes is adequate.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation, IN-DPM or if in USB current limit. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or 10-hour timer times out, the charging is terminated and the $\overline{CHG}$ pin goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power, or going into and out of TTDM.

7.3.14 Termination

Once the OUT pin goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold, the $\overline{CHG}$ pin goes high impedance and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current terminates. If the battery was removed along with the thermistor, then the TS pin is driven high and the charge enters TTDM. If the battery was removed and the TS pin is held in the active region, then the battery detect routine continues until a battery is inserted.

7.3.15 Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT pin at a useable voltage. Whenever the battery is missing the $\overline{CHG}$ pin should be high impedance.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine will be disabled while the IC is in TTDM or has a TS fault. See 図 7-6 for the Battery Detect Flow diagram.

7.3.16 Refresh Threshold

After termination, if the OUT pin voltage drops to VRCH (100 mV below regulation) then a new charge is initiated, but the $\overline{CHG}$ pin remains at a high impedance (off).

7.3.17 Starting a Charge on a Full Battery

The termination threshold is raised by ≠14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.

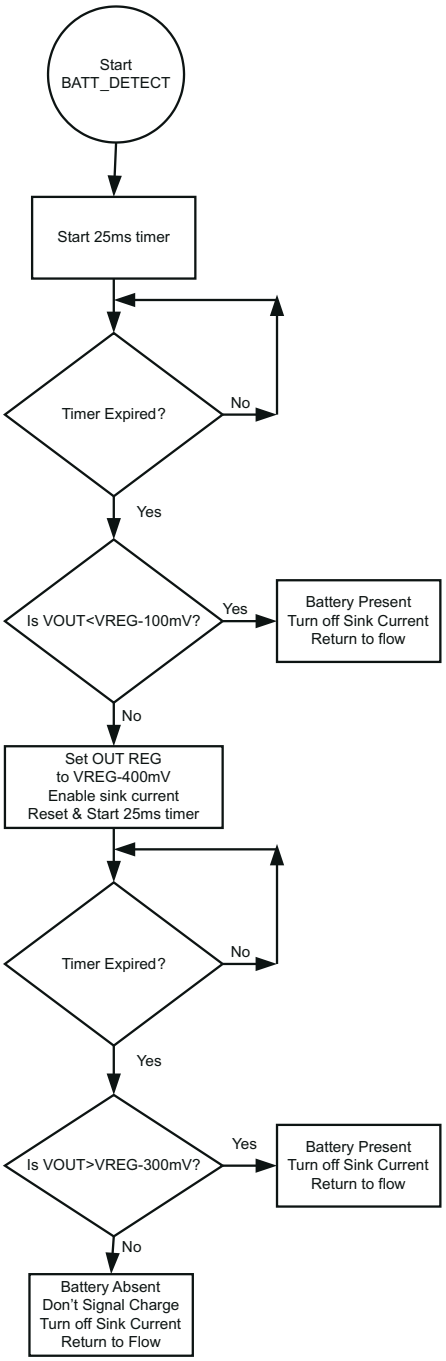


図 7-6. Battery Detect Flow Diagram

7.4 Device Functional Modes

7.4.1 Sleep Mode

If the IN pin voltage is between V_{OUT}+V_{DT} and UVLO, the charge current is disabled, the safety timer counting stops (not reset) and the $\overline{CHG}$ pins are high impedance. As the input voltage rises and the charger exits sleep mode, the safety timer continues to count, charge is enabled and the $\overline{CHG}$ pin returns to its previous state.

7.5 Programming

7.5.1 PRE_TERM – Precharge and Termination Programmable Threshold

Pre-Term is used to program both the precharge current and the termination current threshold, on the BQ2405x. The precharge current level is a factor of two higher than the termination current level. The termination can be set between 5 and 50% of the programmed output current level set by ISET. If left floating the termination and precharge are set internally at 10/20%, respectively. The precharge-to-fast-charge, V_{lowv} threshold is set to 2.5 V.

$$R_{PRE\text{-}TERM} = \%Term \times K_{TERM} = \%Pre\text{-}CHG \times K_{PRE\text{-}CHG} \quad (2)$$

Where:

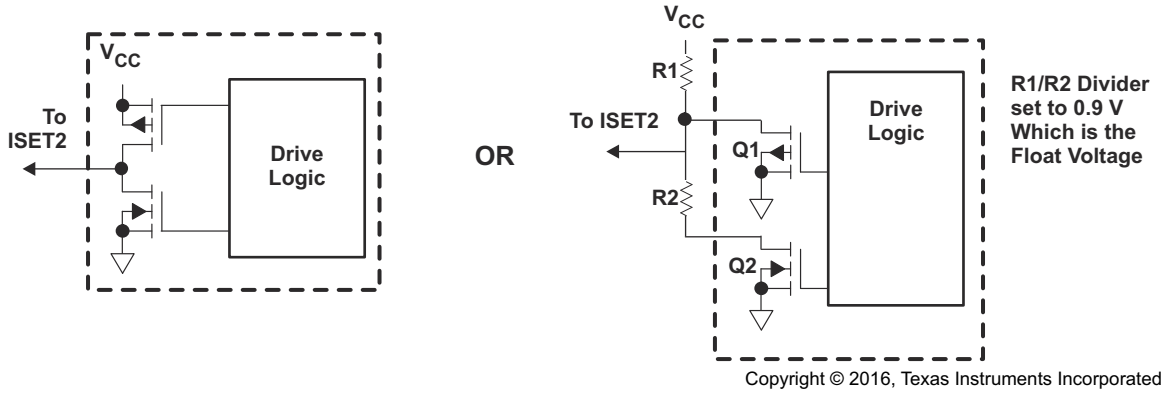
%Term is the percent of fast charge current where termination occurs;
%Pre-CHG is the percent of fast charge current that is desired during precharge;
K_{TERM} and $K_{PRE\text{-}CHG}$ are gain factors found in the electrical specifications.

7.5.2 ISET2

Is a 3-state input and programs the Input Current Limit/Regulation Threshold. A low will program a regulated fast charge current via the ISET resistor and is the maximum allowed input/output current for any ISET2 setting, Float will program a 100-mA Current limit and High will program a 500-mA Current limit. Note that initially the D+/D– detection will latch the charge mode according to the source detected (dedicated charger: ISET; USB Host: at 100 mA) until the ISET2 pin has changed states, indicating the processor or transceiver is controlling the pin.

The detection routine registers the input level (Low–High-Z–High) of the ISET2 pin typically 532 µs after applying input power (V_{IN} > 3.4 V – UVLO). After the detection routine is complete, which is typically 100 ms after a pullup on the D+ or D– line or after typically 570 ms if no pullup, the IC monitors the ISET2 pin for a change of state. If the state changes (Low–High-Z–High) from the one registered, for more than 5 µs, then the "detected" latched charge mode is released and is then controlled by the ISET2 pin. The completion of the detection routine varies due to the mechanical-plugging action of the USB cable; therefore, it is best to wait ≥ 600 ms after V_{IN} > 3.4 V to take control of the ISET2 pin.

The following illustration shows two configurations for driving the 3-state ISET2 pin:



8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

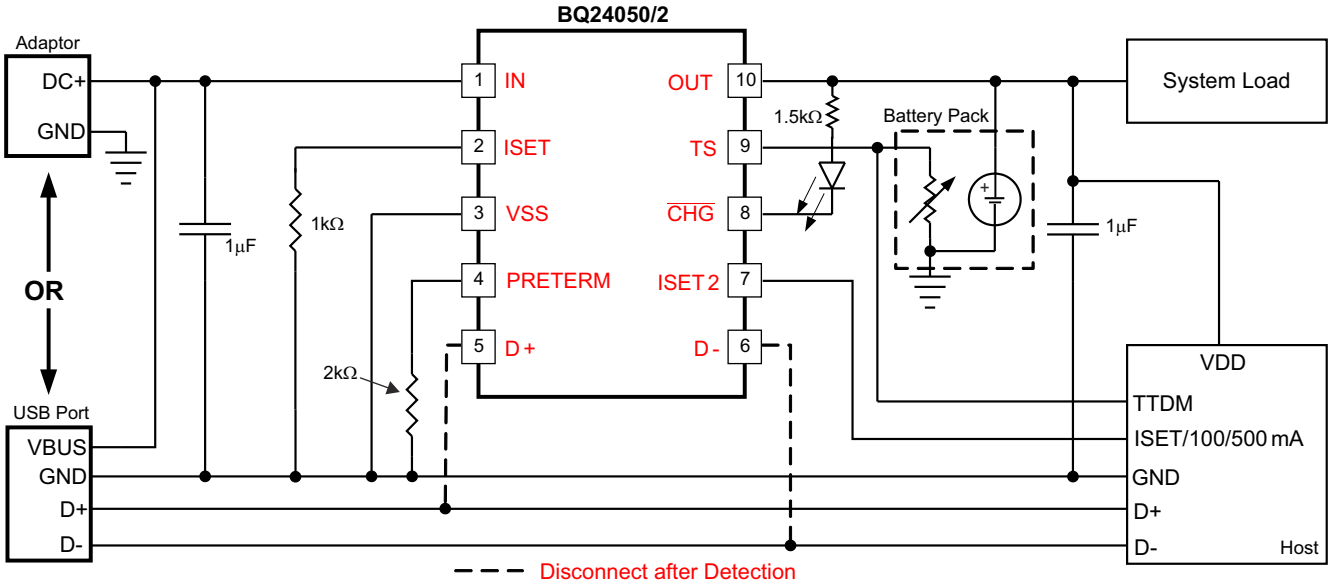
8.1 Application Information

The BQ2405x evaluation module (EVM) is used to perform a stand-alone evaluation for the BQ2405x device family. Refer to the *0.8-A, Single-Input, Single-Cell Li-Ion Battery Charger User's Guide* for details.

8.2 Typical Applications

8.2.1 BQ2405x Charger Application Design Example

The BQ2405x chargers are designed to deliver up to 800 mA of continuous current to the battery output when programmed with a resistor on the ISET pin and is programmed for typically 540 mA at the factory. The USB current limit modes are selected by the ISET2 pin and ISET2 pin programs the charge current using the ISET resistor.



$I_{OUT\_FAST\_CHG}$ = 540 mA; $I_{OUT\_PRE\_CHG}$ = 108 mA; I_{OUT_TERM} = 54 mA

図 8-1. Typical Application Circuit, BQ24050, BQ24052

8.2.1.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current: I_{OUT-FC} = 540 mA; ISET-pin 2
- Termination Current Threshold: $\%_{IOUT-FC}$ = 10% of Fast Charge or ≠54 mA
- Precharge Current by default is twice the termination Current or ≠108 mA
- TS – Battery Temperature Sense = 10-kΩ NTC (103AT)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Program the Fast Charge Current, ISET

$R_{ISET} = [K_{(ISET)} / I_{(OUT)}]$
from electrical characteristics table. . . $K_{(SET)}$ = 540 AΩ
R_{ISET} = [540AΩ/0.54A] = 1.0 kΩ
Selecting the closest standard value, use a 1-kΩ resistor between ISET (pin 16) and V_{SS}.

8.2.1.2.2 Program the Termination Current Threshold, ITERM

$R_{PRE-TERM} = K_{(TERM)} \times \%_{IOUT-FC}$
$R_{PRE-TERM}$ = 200Ω/% × 10% = 2 kΩ
Selecting the closest standard value, use a 2-kΩ resistor between ITERM (pin 15) and Vss.
One can arrive at the same value by using 20% for a precharge value (factor of 2 difference).
$R_{PRE-TERM} = K_{(PRE-CHG)} \times \%_{IOUT-FC}$
$R_{PRE-TERM}$ = 100Ω/% × 20%= 2 kΩ

8.2.1.2.3 TS Function

Use a 10-kΩ NTC thermistor in the battery pack (103AT).

To disable the temp sense function, use a fixed 10-kΩ resistor between the TS (Pin 1) and V_{SS}.

8.2.1.2.4 $\overline{CHG}$

LED Status: connect a 1.5-kΩ resistor in series with a LED between the OUT pin and the $\overline{CHG}$ pin.

Processor Monitoring: Connect a pullup resistor between the power rail of the processor and the $\overline{CHG}$ pin.

8.2.1.2.5 Selecting IN and OUT Pin Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input and output pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16-V capacitor may be adequate for a 30-V transient (verify tested rating with capacitor manufacturer).

8.2.1.3 Application Curves

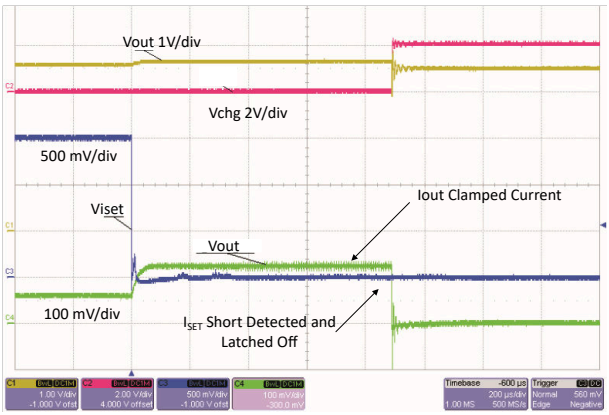
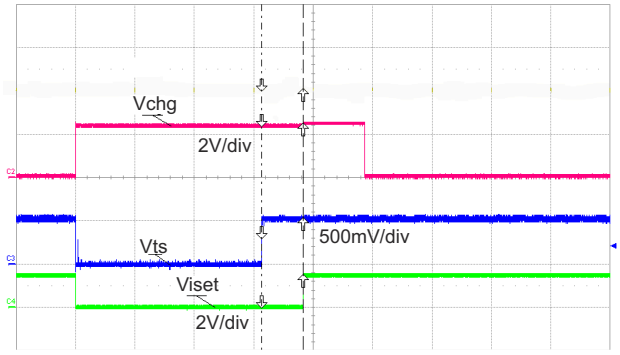


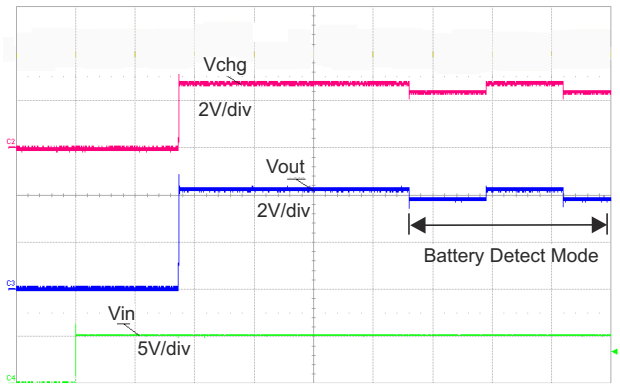
図 8-2. ISET Shorted During Normal Operation



t - time - 50ms/div

10-kΩ resistor from TS to GND.
10 kΩ is shorted to disable the IC.

図 8-3. TS Enable and Disable



t - time - 20ms/div

Fixed 10-kΩ resistor, between TS and GND

図 8-4. Hot Plug Source w/No Battery – Battery Detection

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 28 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the BQ2405x IN and GND terminals, a larger capacitor is recommended.

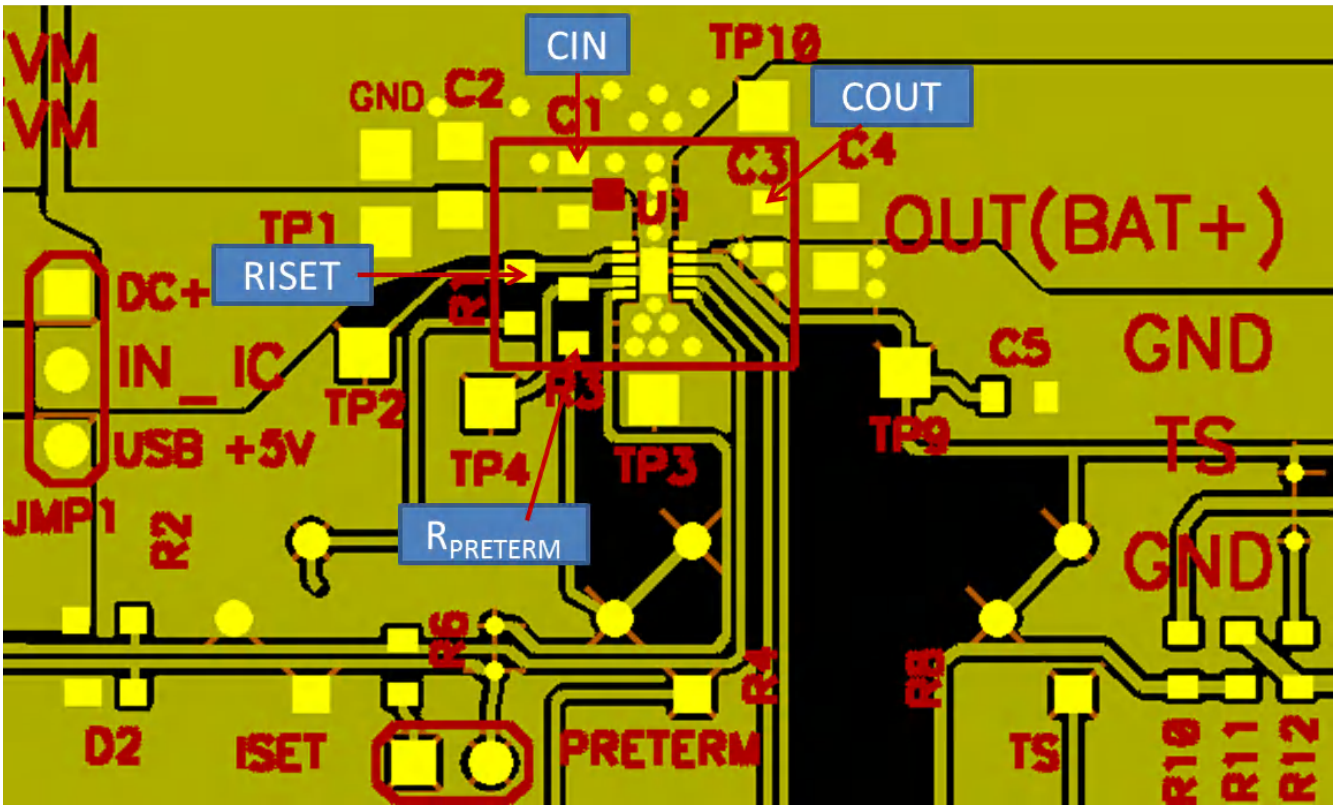
10 Layout

10.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the BQ2405x, with short trace runs to both IN, OUT and GND (thermal pad).

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The BQ2405x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. It is best to use multiple 10-mill vias in the power pad of the IC and in close proximity to conduct the heat to the bottom ground plane. The bottom ground place should avoid traces that “cut off” the thermal path. The thinner the PCB the less temperature rise. The EVM PCB has a thickness of 0.031 inches and uses 2 oz. (2.8-mill thick) copper on top and bottom, and is a good example of optimal thermal performance.

10.2 Layout Example



10.3 Thermal Considerations

The BQ2405x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the VSS pin. Full PCB design guidelines for this package are provided in the *QFN and SON PCB Attachment Application Report*. The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = (T_J - T) / P \quad (3)$$

Where:

T_J = chip junction temperature
T = ambient temperature
P = device power dissipation

Factors that can influence the measurement and calculation of θ_{JA} include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion and Li-Pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4 V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} - V_{(OUT)}] \times I_{(OUT)} \quad (4)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. TI recommends that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for nontypical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

10.3.1 Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery discharges, the battery is used for the calculation. The time from full to discharge can be calculated by dividing the Amp-Hour Capacity of the battery by the leakage current. For a 0.75AHr battery and a 10-µA leakage current (750mAHr/0.010mA = 75000 hours), it would take 75k hours or 8.8 years to discharge. In reality, the self discharge of the cell is much faster, so the 10 µA leakage would be considered negligible.

11 Device and Documentation Support

11.1 Device Support

11.1.1 サード・パーティ製品に関する免責事項

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following: *QFN and SON PCB Attachment Application Report*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24050DSQR	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CVC
BQ24050DSQR.A	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CVC
BQ24050DSQR.B	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CVC
BQ24050DSQT	Active	Production	WSON (DSQ) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CVC
BQ24050DSQT.A	Active	Production	WSON (DSQ) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CVC
BQ24050DSQT.B	Active	Production	WSON (DSQ) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CVC
BQ24052DSQR	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CGT
BQ24052DSQR.A	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CGT
BQ24052DSQR.B	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CGT
BQ24052DSQT	Active	Production	WSON (DSQ) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CGT
BQ24052DSQT.A	Active	Production	WSON (DSQ) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CGT
BQ24052DSQT.B	Active	Production	WSON (DSQ) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	CGT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

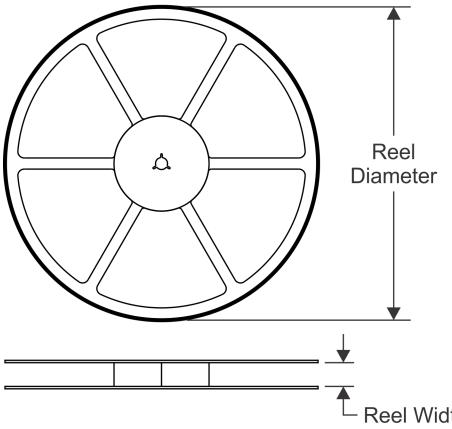
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

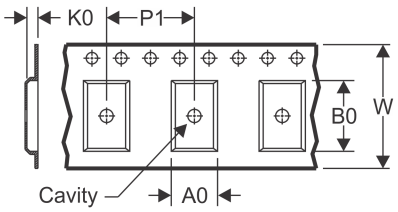
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

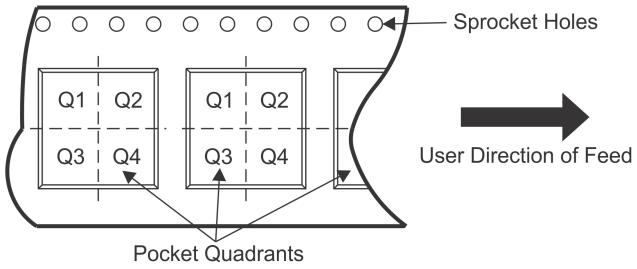


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

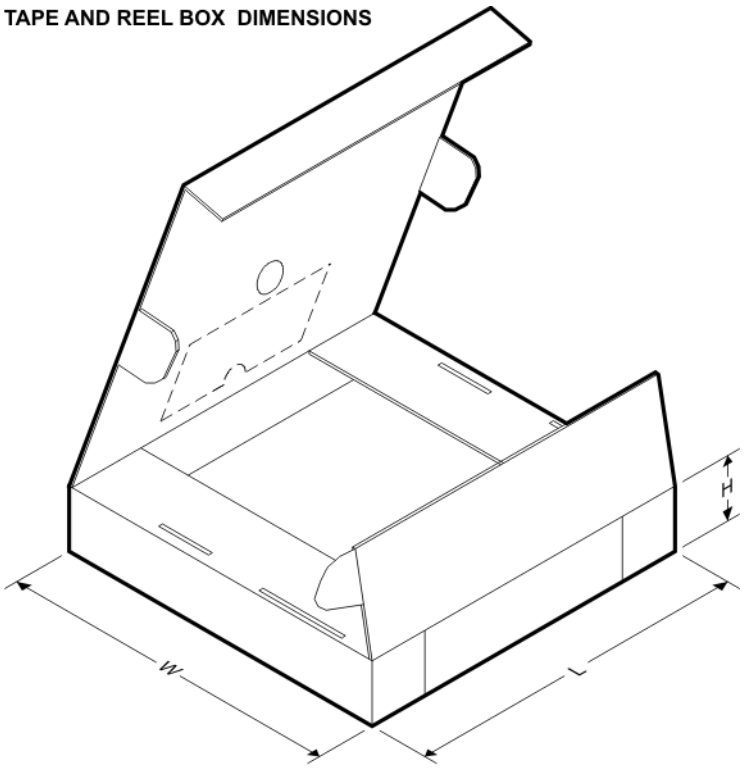
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24050DSQR	WSON	DSQ	10	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24050DSQT	WSON	DSQ	10	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24052DSQR	WSON	DSQ	10	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24052DSQT	WSON	DSQ	10	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

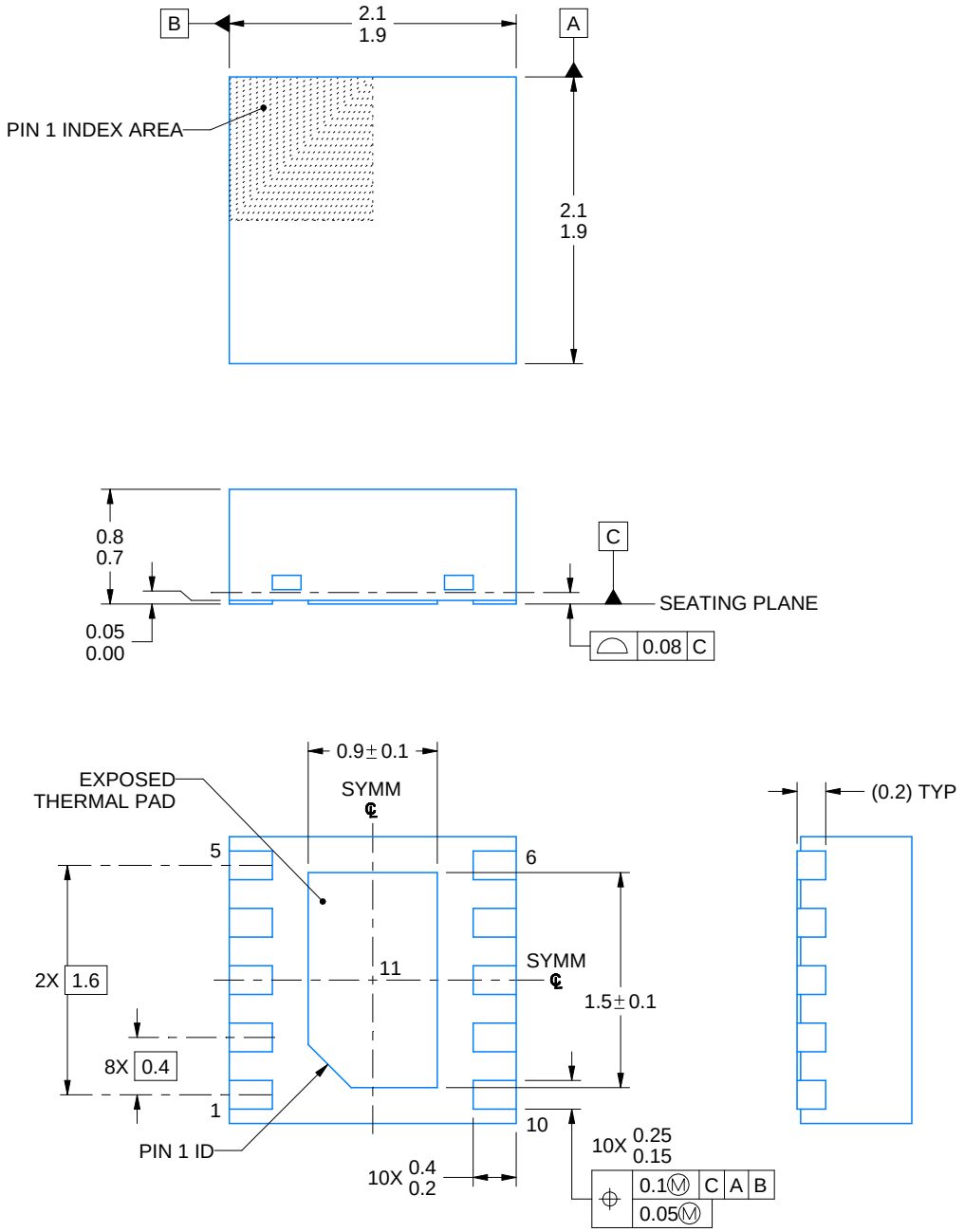
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24050DSQR	WSON	DSQ	10	3000	213.0	191.0	35.0
BQ24050DSQT	WSON	DSQ	10	250	213.0	191.0	35.0
BQ24052DSQR	WSON	DSQ	10	3000	213.0	191.0	35.0
BQ24052DSQT	WSON	DSQ	10	250	213.0	191.0	35.0

PACKAGE OUTLINE

DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

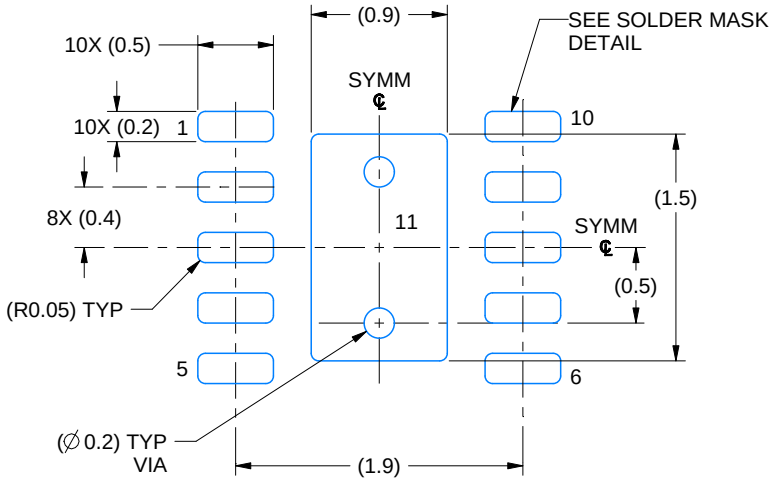
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

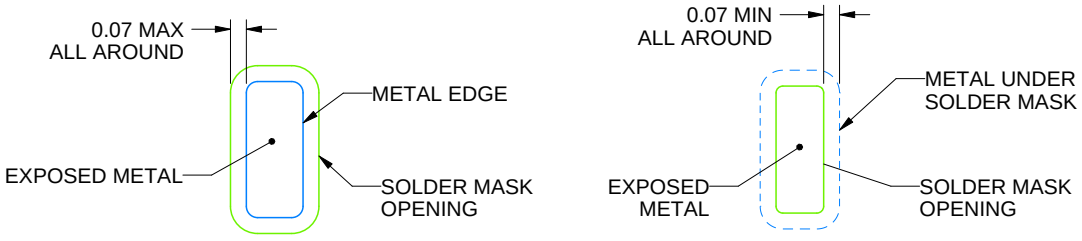
DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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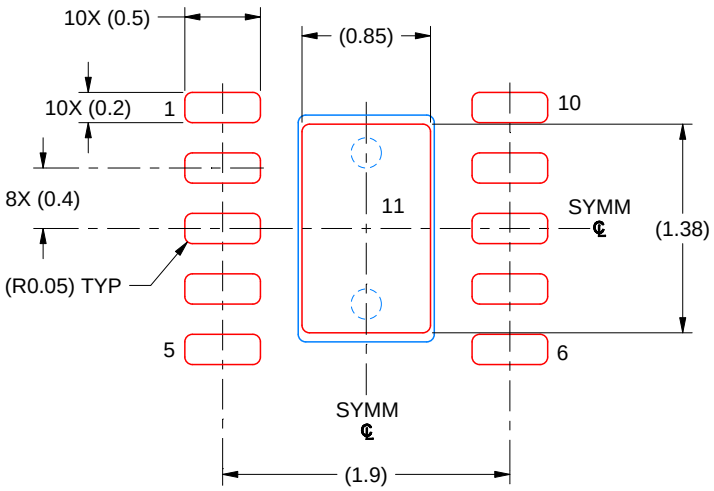
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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