![Texas Instruments]

ATL43x 2.5V、低 Iq、可変、高精度シャント レギュレータ

1 特長

- 2.5V ～ 36V の調整可能なレギュレーション済み出力
- 非常に小さい動作時電流
    - $I_{KA(min)}$ = 35µA (最大値)
    - I_{REF} = 150nA (最大値)
- 安定性を実現する内部補償
    - 容量性負荷なしで安定
- 25℃での基準電圧の許容公差
    - 0.5% (B グレード)
    - 1% (A グレード)
- 標準の温度ドリフト
    - 5mV (–40°C ～ +85°C)、I バージョン
    - 6mV (–40°C ～ +125°C)、Q バージョン
- カソード電流範囲を拡大
  35µA ～ 100mA
- 小さい出力インピーダンス：0.3Ω (最大値)

2 アプリケーション

- フライバック SMPS の 2 次側レギュレーション
- 産業用、コンピューティング、コンシューマ、ポータブル
- 可変の基準電圧および電流
- パワー マネージメント
- 電源の絶縁
- ツェナーの代替品

3 概要

ATL431 と ATL432 は、3 ピンの可変シャント レギュレータで、該当する車載用、商業用、工業用の温度範囲の全体にわたって、規定された熱安定性を維持します。出力電圧は、2 つの外付け抵抗を使用して、V_{ref} (約 2.5V) から 36V までの範囲で任意の値に設定できます。

これらのデバイスの出力インピーダンスは 0.05Ω (標準値) です。これらのデバイスは、アクティブ出力回路による非常に鋭いターンオン特性を備えているため、オンボード レギュレーション、可変電源、スイッチング電源など、多くのアプリケーションにおいて、ツェナー ダイオードの優れた代替品となります。

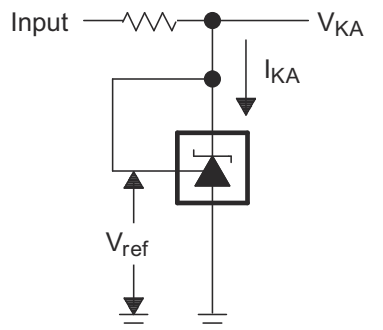ATL43x は、前世代の TL43x に比べてカソード電流範囲が 20 倍以上改善されています。また、より広い範囲の負荷容量のタイプと値でも安定して動作します。

ATL431 と ATL432 はまったく同じ部品ですが、ピン配置と注文番号が異なります。ATL43x は、初期公差 (25℃ 時) が 0.5% の B グレードと、1% の A グレードの 2 つのグレードで供給されます。さらに、温度による出力ドリフトの変動が小さいため、温度範囲全体にわたって定電圧レギュレーションが保証されます。

ATL43xxI デバイスは -40℃～+85℃、ATL43xxQ デバイスは -40℃～+125℃ の温度範囲で動作が規定されています。

製品情報

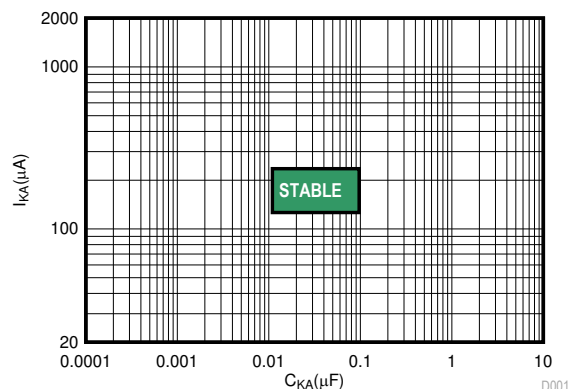| 部品番号	パッケージ [1]	本体サイズ (公称) [2]
ATL431 ATL432	SOT (3)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。

概略回路図

V_{KA} の安定領域= 15V

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4 Pin Configuration and Functions
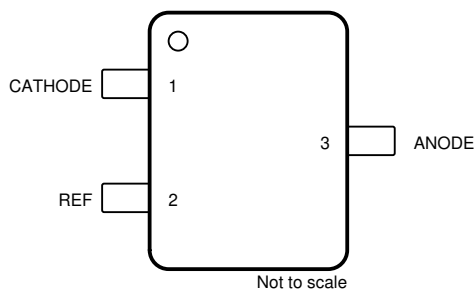
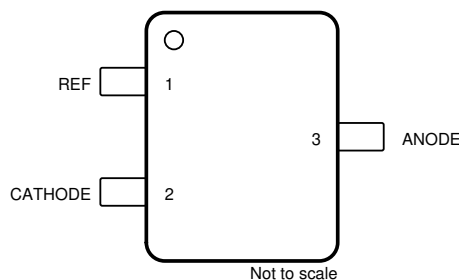**図 4-1. ATL431 DBZ Package**
3-Pin SOT-23
Top View

図 4-2. ATL432 DBZ Package
3-Pin SOT-23
Top View

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	ATL431x	ATL432x		
CATHODE	1	2	I/O	Shunt Current/Voltage input
REF	2	1	I	Threshold relative to common anode
ANODE	3	3	O	Common pin, normally connected to ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{KA}	Cathode voltage[2]		40	V
I_{KA}	Continuous cathode current	−100	150	mA
$I_{I(ref)}$	Reference input current	−0.05	10	mA
T_J	Operating virtual junction temperature	−40	150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ANODE, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{KA}	Cathode voltage	V_{ref}	36	V
I_{KA}	Cathode current	.035	100	mA

				MIN	MAX	UNIT
T_A	Operating free-air temperature	I Grade		−40	85	°C
		Q Grade		−40	125	

5.4 Thermal Information

THERMAL METRIC[1]		ATL43x	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	331.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics, ATL431Ax, ATL432Ax

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage	図 6-1	$V_{KA} = V_{ref}$, $I_{KA} = 1mA$		2475	2500	2525	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range, see section	図 6-1	$V_{KA} = V_{ref}$, $I_{KA} = 1mA$,	ATL43xAI; T_A = -40°C to 85°C		5	15	mV
				ATL43xAQ; T_A = -40°C to 125°C		6	34	
$\Delta V_{ref} / \Delta V_{KA}$	Ratio of change in reference voltage to the change in cathode voltage	図 6-2	$I_{KA} = 1mA$	$\Delta V_{KA} = 10V - V_{ref}$		−0.4	−2.7	mV/V
				$\Delta V_{KA} = 36V - 10V$		−0.1	−2	
I_{ref}	Reference input current	図 6-2	$I_{KA} = 1mA$, R1 = 10kΩ, R2 = ∞			30	150	nA
$I_{I(dev)}$	Deviation of reference input current over full temperature range, see section	図 6-2	$I_{KA} = 1mA$, R1 = 10kΩ, R2 = ∞			20	50	nA
I_{min}	Minimum cathode current for regulation	図 6-1 図 5-5	$V_{KA} = V_{ref}$			20	35	µA
I_{off}	Off-state cathode current	図 6-3	$V_{KA} = 36V$, $V_{ref} = 0$			0.05	0.2	µA
$|Z_{KA}|$	Dynamic impedance, see section	図 6-1	$V_{KA} = V_{ref}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.05	0.3	Ω

5.6 Electrical Characteristics, ATL431Bx, ATL432Bx

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage	図 6-1	$V_{KA} = V_{ref}$, $I_{KA} = 1mA$		2487	2500	2512	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range, see section	図 6-1	$V_{KA} = V_{ref}$, $I_{KA} = 1mA$	ATL43xBI; T_A = −40°C to 85°C		5	15	mV
				ATL43xBQ; T_A = −40°C to 125°C		6	34	
$\Delta V_{ref} / \Delta V_{KA}$	Ratio of change in reference voltage to the change in cathode voltage	図 6-2	$I_{KA} = 1mA$	$\Delta V_{KA} = 10V - V_{ref}$		−0.4	−2.7	mV/V
				$\Delta V_{KA} = 36V - 10V$		−0.1	−2	
I_{ref}	Reference input current	図 6-2	$I_{KA} = 1mA$, R1 = 10kΩ, R2 = ∞			30	150	nA
$I_{I(dev)}$	Deviation of reference input current over full temperature range, see section	図 6-2	$I_{KA} = 1mA$, R1 = 10kΩ, R2 = ∞			20	50	nA
I_{min}	Minimum cathode current for regulation	図 6-1 図 5-5	$V_{KA} = V_{ref}$			20	35	µA
I_{off}	Off-state cathode current	図 6-3	$V_{KA} = 36V$, $V_{ref} = 0$			0.05	0.2	µA

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5.6 Electrical Characteristics, ATL431Bx, ATL432Bx (続き)

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$|z_{KA}|$	Dynamic impedance, see section	図 6-1	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA		0.05	0.3	Ω

Product Folder Links: *ATL431 ATL432*

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5.7 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.
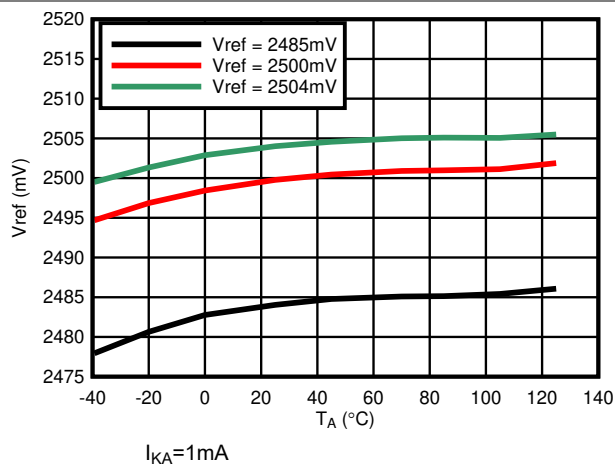
図 5-1. Reference Voltage vs Free-Air Temperature
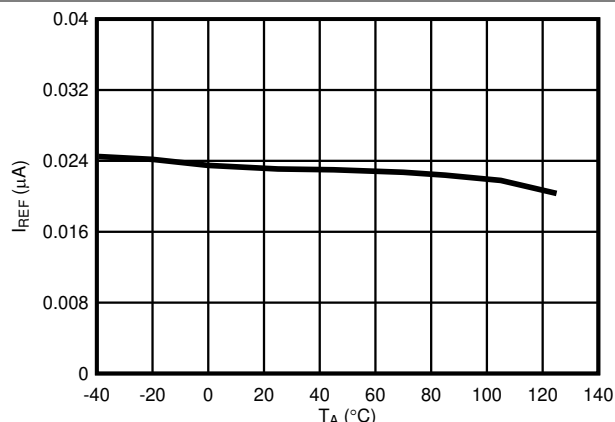
図 5-2. Reference Current vs Free-Air Temperature
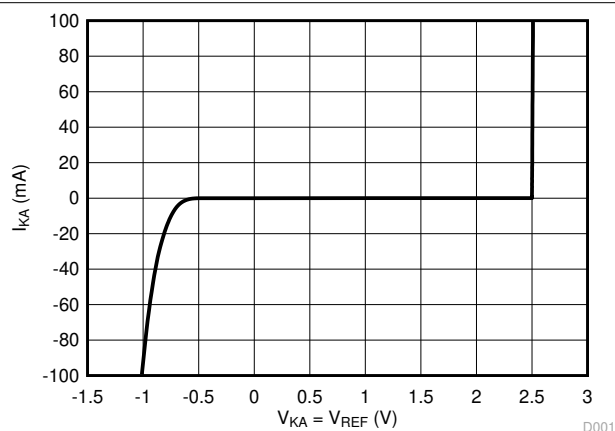
図 5-3. Cathode Current vs Cathode Voltage
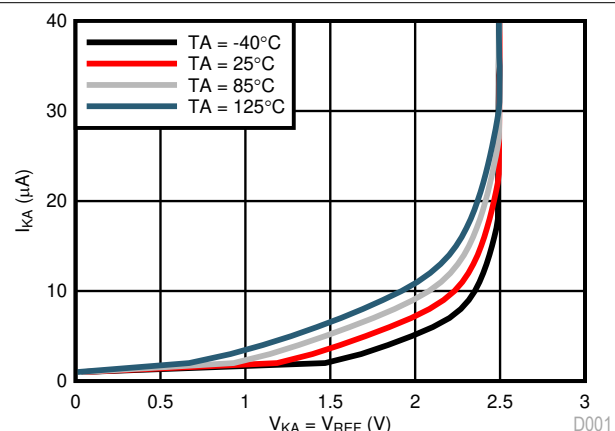
図 5-4. Cathode Current vs Cathode Voltage
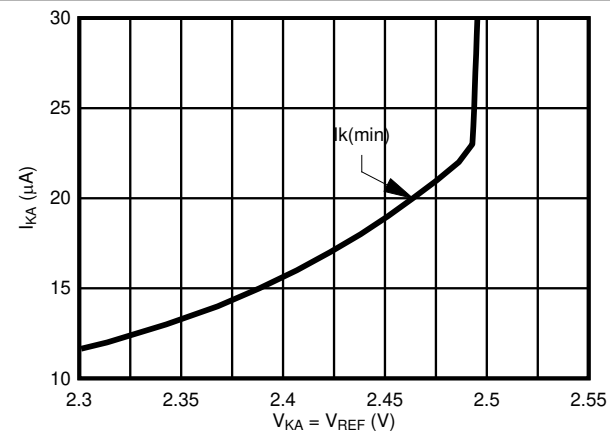
図 5-5. Cathode Current vs Cathode Voltage
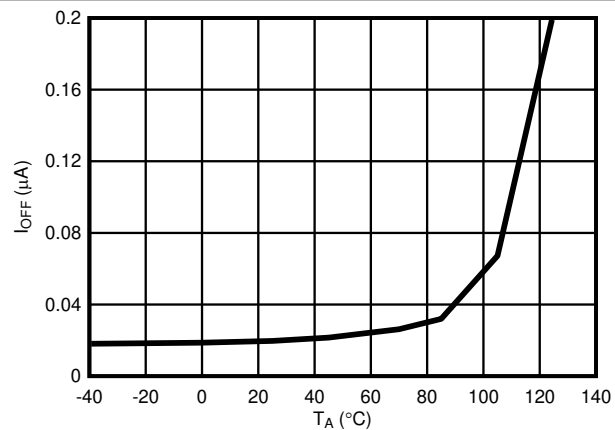
図 5-6. Off-State Cathode Current vs Free-Air Temperature

Product Folder Links: *ATL431 ATL432*

English Data Sheet: SLVSCV5

5.7 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

I_{KA}=1mA
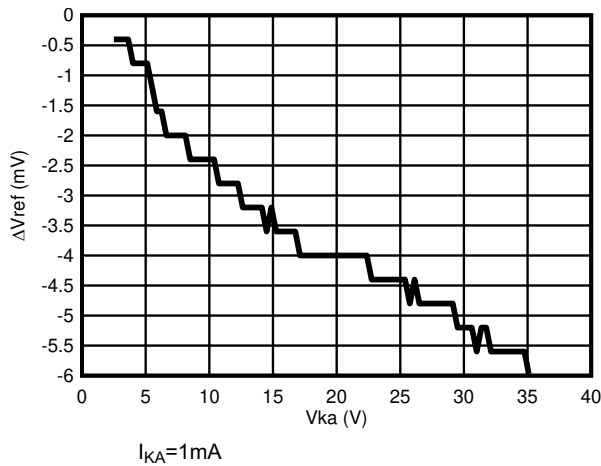
図 5-7. Delta Reference Voltage vs Cathode Voltage

I_{KA}=1mA
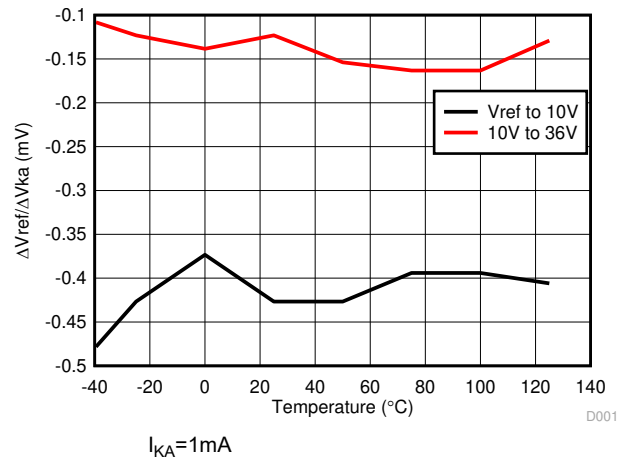
図 5-8. Delta Reference Voltage vs Cathode Voltage

I_{KA} = 1mA

図 5-9. Noise Voltage
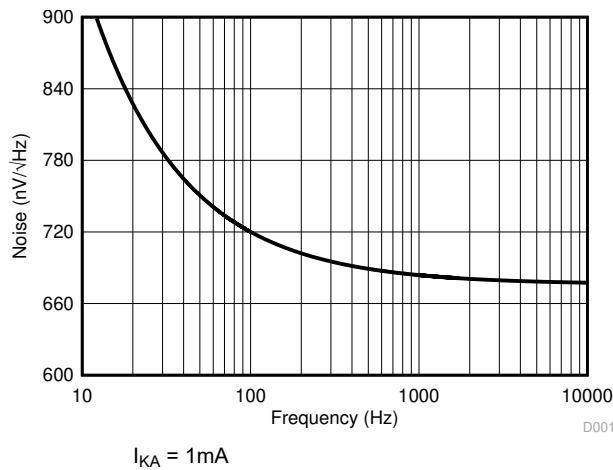
図 6-4 used for this measurement. I_{KA}=1mA
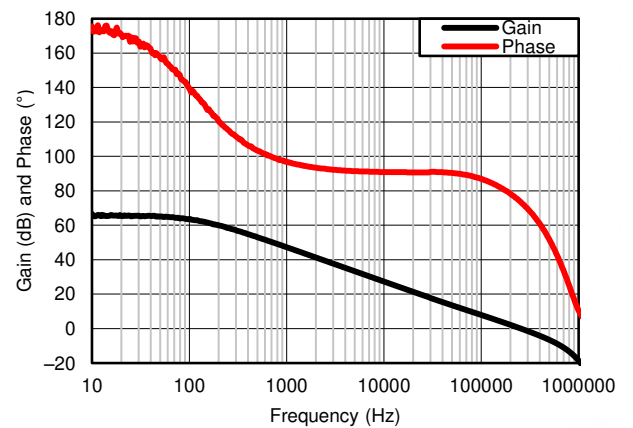
図 5-10. Small-Signal Voltage Amplification vs Frequency
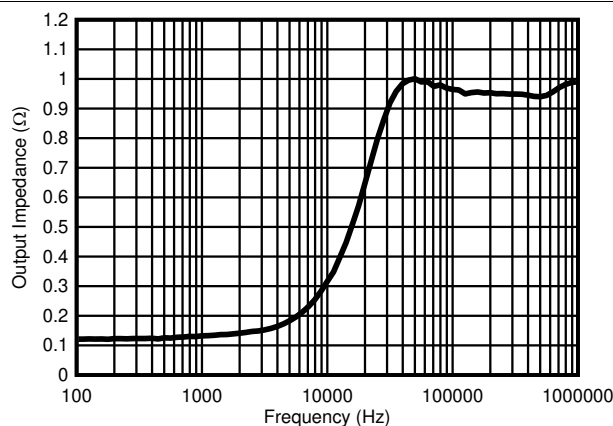
図 6-5 used for this measurement.

図 5-11. Output Impedance vs Frequency
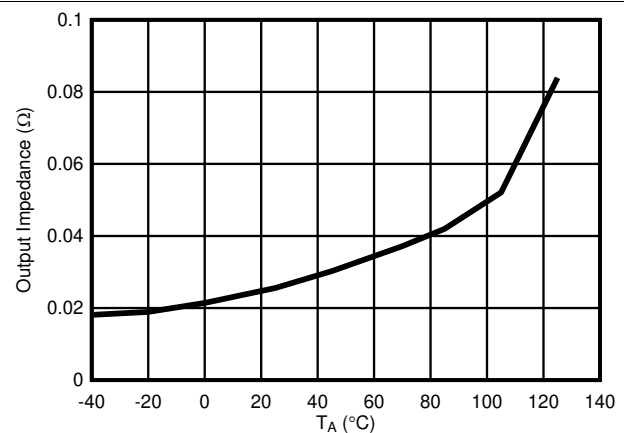
図 6-5 used for this measurement.

図 5-12. DC Output Impedance vs Temperature

資料に関するフィードバック (ご意見やお問い合わせ) を送信

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5.7 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

I_{KA} = 100µA   図 6-7 used for this measurement.

図 5-13. Pulse Response

ESR < 20mΩ   図 6-6 used to verify stability.

図 5-14. Low I_{KA} (V_{KA} = 2.5V) Stability Boundary Conditions All ATL43xx Devices

ESR < 20mΩ   図 6-6 used to verify stability.

図 5-15. Low I_{KA} (V_{KA} = 5.0V) Stability Boundary Conditions All ATL43xx Devices

ESR < 20mΩ   図 6-6 used to verify stability.

図 5-16. Low I_{KA} (V_{KA} = 10.0V) Stability Boundary Conditions All ATL43xx Devices

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5.7 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

ESR < 20mΩ   図 6-6 used to verify stability.

図 5-17. Low I_{KA} (V_{KA} = 15.0V) Stability Boundary Conditions All ATL43xx Devices

ESR < 20mΩ   図 6-6 used to verify stability.

図 5-18. High I_{KA} (V_{KA} = 2.5V) Stability Boundary Conditions All ATL43xx Devices

ESR < 20mΩ   図 6-6 used to verify stability.

図 5-19. High I_{KA} (V_{KA} = 5.0V) Stability Boundary Conditions All ATL43xx Devices

ESR < 20mΩ   図 6-6 used to verify stability.

図 5-20. High I_{KA} (V_{KA} = 10.0V) Stability Boundary Conditions All ATL43xx Devices

資料に関するフィードバック (ご意見やお問い合わせ) を送信   9

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5.7 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.


ESR < 20mΩ

図 6-6 used to verify stability.

図 5-21. High I_{KA} (V_{KA} = 15.0V) Stability Boundary Conditions All ATL43xx Devices

English Data Sheet: SLVSCV5

6 Parameter Measurement Information

The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left| \alpha_{Vref} \right| \left(\frac{ppm}{°C} \right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25°C}} \right) \times 10^6}{\Delta T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.
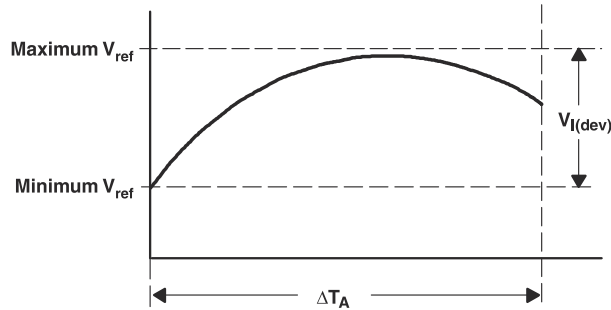
α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see 図 6-2), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$ which is approximately equal to $|z_{KA}| \left(1 + \frac{R1}{R2} \right)$
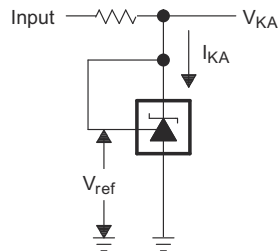
図 6-1. Test Circuit for $V_{KA} = V_{ref}$

$$V_{KA} = V_{ref} \left(1 + \frac{R1}{R2} \right) + I_{ref} \times R1$$
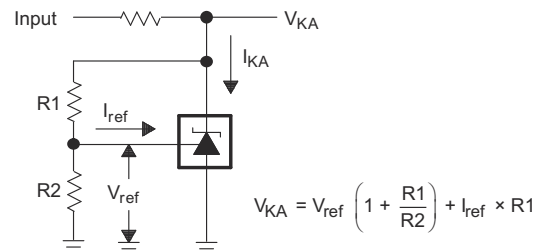
図 6-2. Test Circuit for $V_{KA} > V_{ref}$
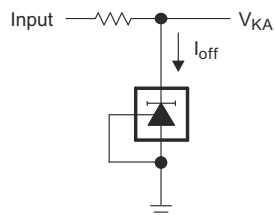
図 6-3. Test Circuit for I_{off}
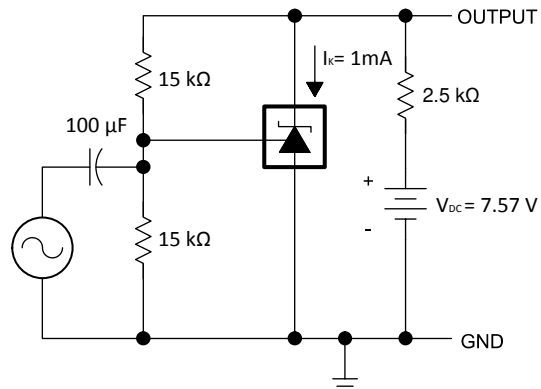
図 6-4. Test Circuit for Phase and Gain Measurement
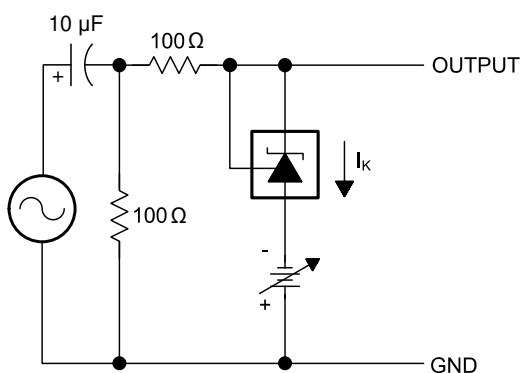
図 6-5. Test Circuit for Reference Impedance (Z_{KA})
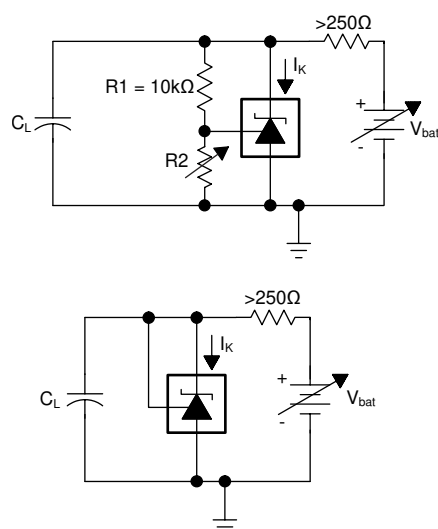
図 6-6. Test Circuit for Stability Boundary Conditions
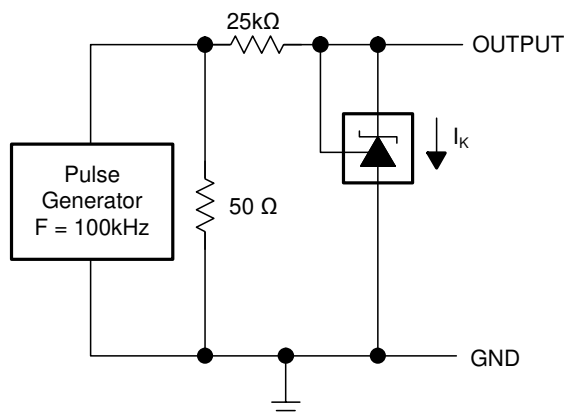
図 6-7. Test Circuit for Pulse Response

Product Folder Links: *ATL431 ATL432*

English Data Sheet: SLVSCV5

7 Detailed Description

7.1 Overview

The ATL43x is a low power counterpart to TL431 and TLV431, having lower minimum cathode current ($I_{k(min)}$ = 35µA). Like the TL431, the ATL43x is used in conjunction with it's key components to behave as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference.

The ATL43x can be operated and adjusted to cathode voltages from 2.5V to 36V, this part is an excellent choice for a wide range of end equipments in industrial, auto, telecom and computing. For this device to behave as a shunt regulator or error amplifier, > 35µA ($I_{min}(max)$) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5% and 1.0%. These reference options are denoted by B (0.5%) and A (1.0%) after the ATL43x.

The ATL43xxI devices are characterized for operation from −40°C to +85°C, and the ATL43xxQ devices are characterized for operation from −40°C to +125°C.

7.2 Functional Block Diagram
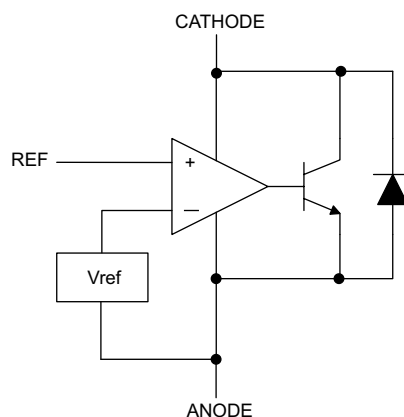
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7.3 Feature Description

ATL43x consists of an internal reference and amplifier that outputs a sink current based on the difference between the reference pin and the virtual internal pin. The sink current is produced by an internal Darlington pair.

When operated with enough voltage headroom (≥ 2.5V) and cathode current (I_{KA}), ATL43x forces the reference pin to 2.5V. However, the reference pin can not be left floating, as it needs I_{ref} ≥ 0.1µA (please see the *Functional Block Diagram*). This is because the reference pin is driven into an NPN, which needs base current in order operate properly.

When feedback is applied from the Cathode and Reference pins, ATL43x behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current required in the above feedback situation must be applied to this device in open-loop, servo, or error amplifying implementations for the current to be in the proper linear region to give the ATL43x enough gain.

Unlike many linear regulators, ATL43x is internally compensated to be stable without an output capacitor between the cathode and anode; however, if it is desired to use an output capacitor, 図 5-14 through 図 5-21 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

7.4 Device Functional Modes

7.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of ATL43x is not being fed back to the reference/input pin in any form, this device is operating in open loop. With such high gain in this configuration, the ATL43x is typically used as a comparator. Due to the integrated reference, the ATL43x allows users to monitor a certain level of a single signal.

7.4.2 Closed Loop

When the cathode/output voltage or current of ATL43x is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving the ATL43x use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

図 8-1 shows the ATL43x used in a 24-V isolated flyback supply. The output of the regulator, plus the forward voltage drop of the optocoupler LED (2.5 + 0.7 = 3.2V), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 5.0Vdc is possible in the topology shown in 図 8-1.

The 431 family of devices are prevalent in these applications, being designers go-to choice for secondary side regulation. Due to this prevalence, this section will further go on to explain operation and design in both states of the ATL43x that this application sees: open-loop (Comparator + V_{ref}) and closed-loop (Shunt Regulator).

The key benefit in isolated supplies for the ATL43x is the no load power savings gained by the > 20x decrease in I_{Kmin} from TL431. More information about this and other benefits can be found in *Designing with the "Advanced" TL431, ATL431* (SLVA685). Further information about system stability and using a ATL43x device for compensation can be found in *Compensation Design With TL431 for UCC28600* (SLUA671).

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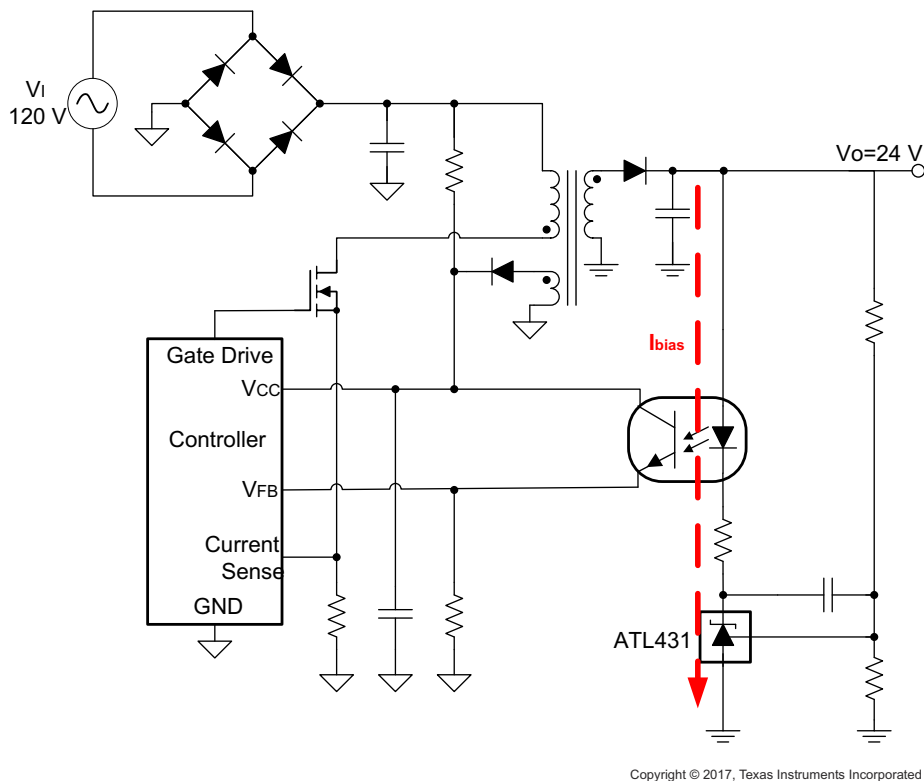
図 8-1. Flyback With Isolation Using ATL43x as Voltage Reference and Error Amplifier

It is important to consider the cathode voltage ramp rate when using ATL431 or ATL432 in overvoltage protection or other voltage monitoring applications, in optocoupler configurations, or any configuration where a power supply may ramp the cathode voltage quickly while ATL431 or ATL432 is meant to be in operation. For fast cathode current ramp rates, inaccurate responses may occur which can trip voltage monitoring circuits when an overvoltage or undervoltage condition has not actually been met. When designing with ATL431 or ATL432, it is

---

recommended that the ramp rate of the cathode voltage remain below 0.0125V/μs to mitigate potential inaccuracies.

For voltage monitoring or other applications where a ramp rate faster than 0.0125 V/μs is required, please consider other high-performance, pin-to-pin devices from TI: ATL431LI, TLA431, or TL431.

8.2 Typical Applications

8.2.1 Comparator With Integrated Reference (Open-Loop)
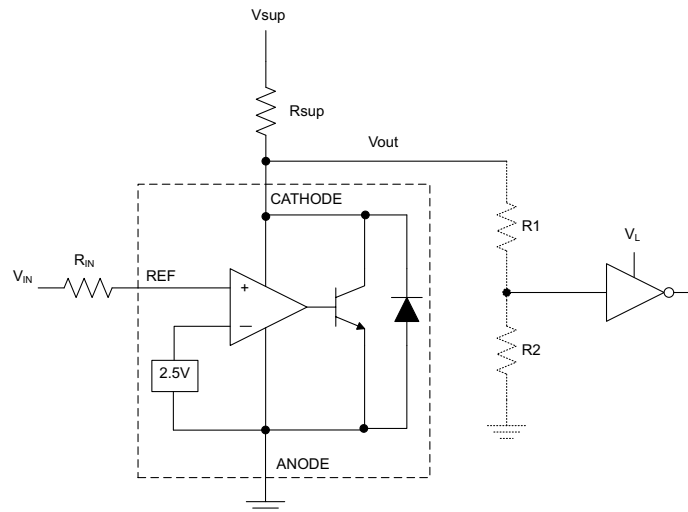
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図 8-2. Comparator Application Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0V to 3.3V
Input resistance	100kΩ
Supply voltage	5V
Cathode current (I_K)	50μA
High output voltage level (Vin < 2.5V)	Vsup
Low output voltage (Vin > 2.5V)	~2V

8.2.1.2 Detailed Design Procedure

When using the ATL43x as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

8.2.1.2.1 Basic Operation

In the configuration shown in 図 8-2, the ATL43x behaves as a comparator, comparing the V_{ref} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_k), ATL43x have enough open-loop

Product Folder Links: *ATL431 ATL432*

English Data Sheet: SLVSCV5

gain to provide a quick response. With the maximum operating current (I_{min}) of ATL43x being 35µA, operation below that can result in low gain; leading to a slow response.

8.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of 2.5V ± (0.5% or 1.0%) depending on which version is being used.

The more overdrive voltage provided, the faster the ATL43x responds.

For applications where ATL43x is being used as a comparator, it is best to set the trip point to greater than the positive expected error (that is, +1.0% for the A version). For fast response, setting the trip point to > 10% of the internal V_{ref} should suffice. 図 8-3 shows the transition from V_{OH} to V_{OL} based on the input voltage and can be used as a guide for selecting the overdrive voltage.

For minimal voltage drop or difference from Vin to the ref pin, TI recommends using an input resistor < 1MΩ to provide I_{ref}.

8.2.1.2.3 Output Voltage and Logic Input Level

In order for ATL43x to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} and V_{IL}.

As seen in 図 8-3, the output low level voltage for ATL43x in open-loop/comparator mode is ~2V, which is sufficient for some ≥ 5-V supplied logic. However, would not work for 3.3-V and 1.8-V supplied logic. To accommodate this, a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

The output high voltage for ATL43x is approximately V_{sup} due to ATL43x being open-collector. If V_{sup} is much higher than the receiving maximum input voltage tolerance of the logic, the output must be attenuated to accommodate the reliability of the outgoing logic.

When using a resistive divider on the output, ensure that the sum of the resistive divider (R1 and R2 in 図 8-2) is much greater than R_{sup} so that the resistive divider does not interfere with the ability of the ATL43x to pull close to V_{sup} when turning off.

8.2.1.2.3.1 Input Resistance

ATL43x requires an input resistance in this application in order to source the reference current (I_{ref}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be:

$$V_{ref} = V_{in} - I_{ref} \times R_{in} \tag{1}$$

Because I_{ref} can be as high as 0.15µA, TI recommends using a resistance small enough that will mitigate the error that I_{ref} creates from V_{in}. Also, the input resistance must be set high enough as to not surpass the absolute maximum of 10mA.

8.2.1.3 Application Curve

$R_{IN} = 100k\Omega$ $V_{SUP} = 5.0V$ $R_{SUP} = 10k\Omega$
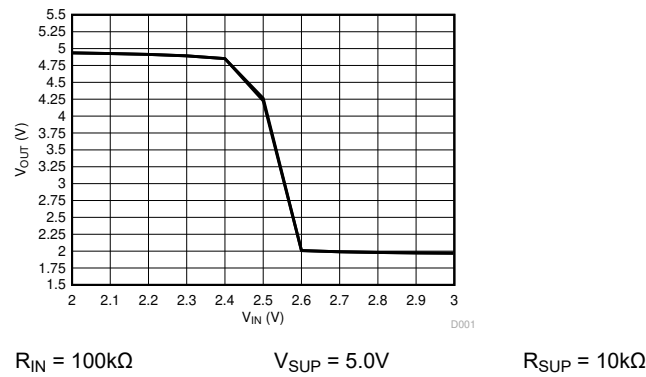
図 8-3. Open-Loop (Comparator Mode) V_{OUT} vs V_{IN}

8.2.2 Shunt Regulator/Reference

$$V_O = \left(1 + \frac{R1}{R2} \right) V_{REF}$$
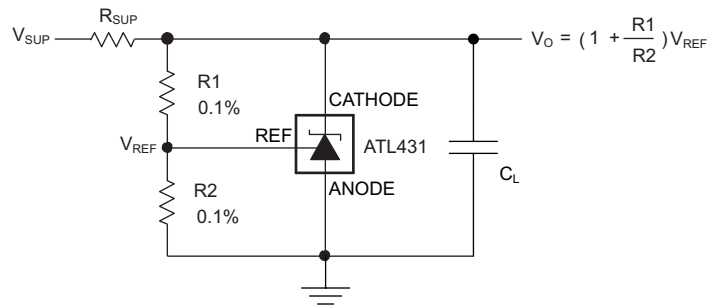
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図 8-4. Shunt Regulator Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-2 as the input parameters.

表 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference initial accuracy	1.0%
Supply voltage	48V
Cathode current (I_K)	50µA
Output voltage level	2.5V to 36V
Load capacitance	1nF
Feedback resistor values (R1 and R2)	10kΩ

8.2.2.2 Detailed Design Procedure

When using the ATL43x as a Shunt Regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

Product Folder Links: *ATL431 ATL432*

English Data Sheet: SLVSCV5

8.2.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in 図 8-4, with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in 図 8-4. The cathode voltage can be more accurately determined by taking in to account the cathode current:

$$V_O = (1 + R1 / R2) \times V_{ref} - I_{ref} \times R1 \tag{2}$$

For this equation to be valid, the ATL43x must be fully biased so that it has enough open-loop gain to mitigate any gain error. This can be done by meeting the I_{min} spec denoted in *Electrical Characteristics, ATL431Ax, ATL432Ax* table.

8.2.2.2.2 Total Accuracy

When programming the output above unity gain (V_{KA} = V_{ref}), ATL43x is susceptible to other errors that may effect the overall accuracy beyond V_{ref}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ – Change in reference voltage over temperature
- ΔV_{ref} / ΔV_{KA} – Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ – Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account. *Setting the Shunt Voltage on an Adjustable Shunt* (SLVA445), assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

8.2.2.2.3 Stability

Though the ATL43x is stable with no capacitive load, the device that receives the output voltage of the shunt regulator could present a capacitive load that is within the ATL43x region of stability, shown in 図 5-14 through 図 5-21. Also, designers can use capacitive loads to improve the transient response or for power supply decoupling.

図 5-14 through 図 5-21 should be used as a guide for capacitor selection and compensation. It is characterized using ceramic capacitors with very-low ESR. When it is desirable to use a capacitor within the unstable region, higher ESR capacitors can be used to stabilize ATL43x or an external series resistance can be added. For more information and guidance on ESR values, see *Designing with the "Advanced" TL431, ATL431* (SLVA685).

Unlike the TL431, the stability boundary is characterized and determined with resistors 250Ω and greater. Which is designed for low cathode current applications.

8.2.2.3 Application Curves

I_{KA} = 50µA

図 8-5. ATL43x Start-Up Response

I_{KA} = 1mA

図 8-6. ATL43x Start-Up Response

Product Folder Links: *ATL431 ATL432*

English Data Sheet: SLVSCV5
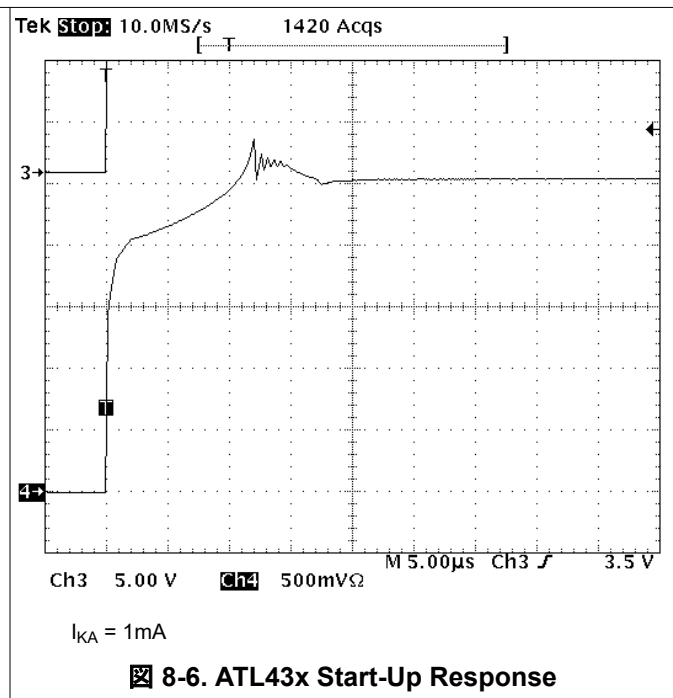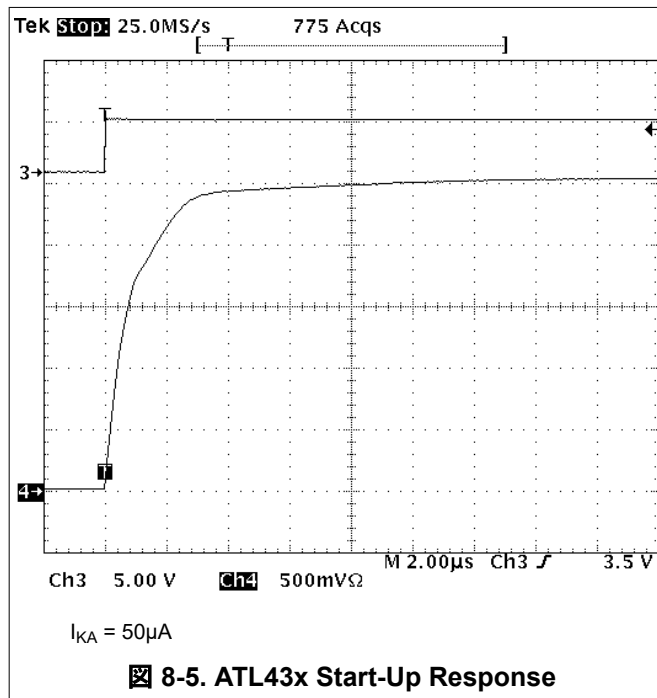
9 Power Supply Recommendations

When using the ATL43x in a flyback supply (see 図 8-1), it is often common for designers to place the bias resistor between the Anode of the Opto-Coupler and the output voltage (V_O = 24V). However, this makes the ATL43x more susceptible to EOS/ESD damage. Therefore, TI recommends placing the bias resistor between the Cathodes of the Opto-Coupler and the ATL43x, as shown in 図 8-1. For further explanation, see *Designing with the "Advanced" TL431, ATL431* (SLVA685).

When using the ATL43x as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. Be sure that the capacitance is within the stability criteria shown in 図 5-14 through 図 5-21.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed the absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

10 Layout

10.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

10.2 Layout Example
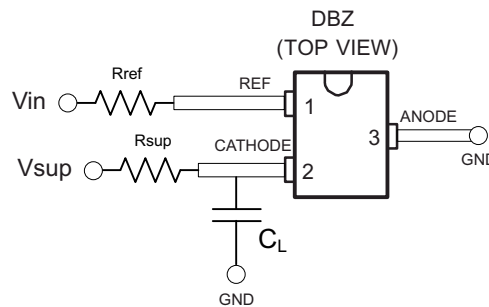
図 10-1. DBZ Layout Example

11 Device and Documentation Support

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Product Folder Links: *ATL431 ATL432*

English Data Sheet: SLVSCV5

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ATL431AIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(ZCKS, ZCR3)
ATL431AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ZCKS, ZCR3)
ATL431AQDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(ZCLS, ZCS3)
ATL431AQDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ZCLS, ZCS3)
ATL431AQDBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ZCLS, ZCS3)
ATL431BIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(ZCMS, ZCT3)
ATL431BIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ZCMS, ZCT3)
ATL431BQDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(ZCJS, ZCU3)
ATL431BQDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ZCJS, ZCU3)
ATL432AIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(ZCNS, ZCV3)
ATL432AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ZCNS, ZCV3)
ATL432AQDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(ZCOS, ZCW3)
ATL432AQDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ZCOS, ZCW3)
ATL432AQDBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ZCOS, ZCW3)
ATL432BIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(ZCPS, ZCX3)
ATL432BIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ZCPS, ZCX3)
ATL432BQDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(ZCQS, ZCY3)
ATL432BQDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ZCQS, ZCY3)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ATL431AIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL431AQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL431AQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
ATL431BIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL431BIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
ATL431BQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432AIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432AQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
ATL432AQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432BIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432BQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS
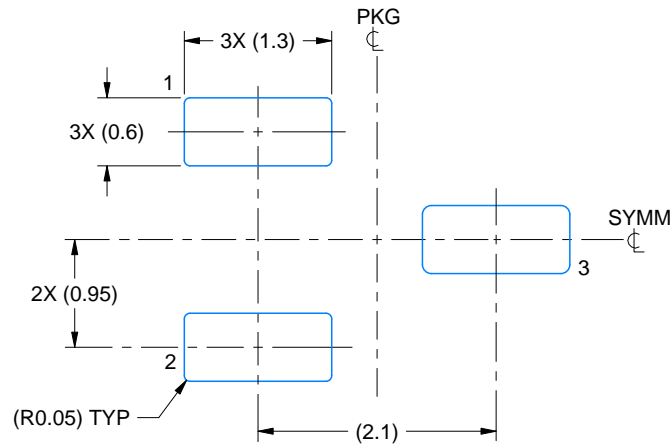

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ATL431AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431AQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431AQDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
ATL431BIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431BIDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
ATL431BQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432AQDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
ATL432AQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432BIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432BQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

2.64
2.10

1.4
1.2

B

A

PIN 1
INDEX AREA

1

0.95

(0.125)

1.9

3.04
2.80

3

(0.15)

NOTE 4

2

3X 0.5
0.3

⊕ 0.2Ⓜ C A B

C

1.12 MAX

⌒ 0.1 C

4X 0°-15°

(0.95)

0.10
0.01 TYP

4X 4°-15°

0.25

GAGE PLANE

0.20
0.08 TYP

0.6
0.2 TYP

SEATING PLANE

0°-8° TYP

4214838/F   08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR

PKG

3X (1.3)

1

3X (0.6)

SYMM

3

2X (0.95)

2

(R0.05) TYP

(2.1)

LAND PATTERN EXAMPLE
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
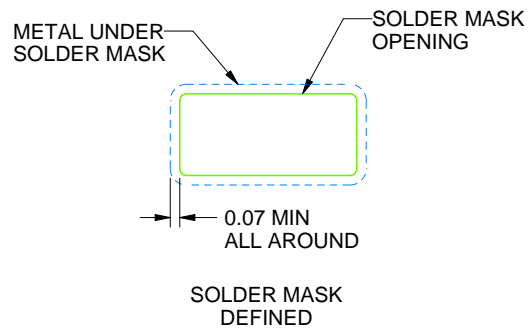
SOLDER MASK DETAILS

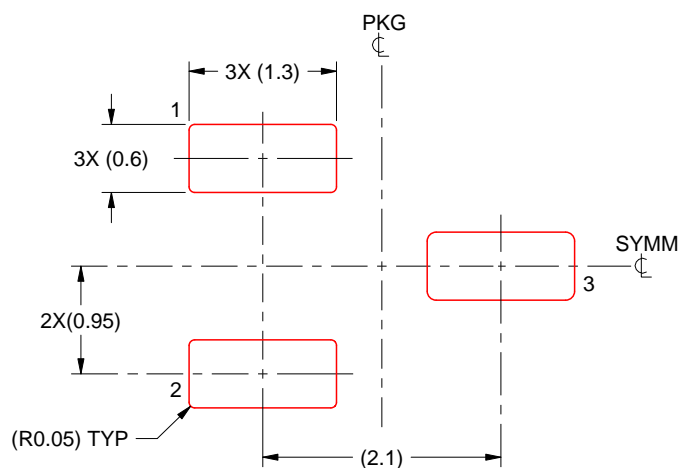4214838/F   08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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