

AMC0381D-Q1 車載対応、固定ゲイン差動出力付き、高精度、高電圧 DC 入力、強化絶縁型アンプ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$, T_A
- 外付け抵抗なしで DC、電圧を直接検出できる内蔵高電圧抵抗分圧器
- システムレベルのキャリブレーションなしで、温度範囲と寿命全体にわたって 1% 未満の高精度
- 差動出力
- 電源電圧範囲:
 - ハイサイド (VDD1): $3.0\text{V} \sim 5.5\text{V}$
 - ローサイド (VDD2): $3.0\text{V} \sim 5.5\text{V}$
- 小さい DC 誤差:
 - オフセット誤差: $\pm 1.5\text{mV}$ (最大値)
 - オフセットドリフト: $\pm 20\mu\text{V}/^{\circ}\text{C}$ (最大値)
 - 減衰誤差: $\pm 0.25\%$ (最大値)
 - 減衰ドリフト: $\pm 40\text{ppm}/^{\circ}\text{C}$ (最大値)
 - 非線形性: 0.05% (最大値)
- 「高 CMTI: 50V/ns (最小値)
- 低 EMI: CISPR-11 および CISPR-25 規制に準拠
- 利用可能な入力オプション:
 - AMC0381D06-Q1: 600V , $10\text{M}\Omega$
 - AMC0381D10-Q1: 1000V , $12.5\text{M}\Omega$
 - AMC0381D16-Q1: 1600V , $33\text{M}\Omega$
- 安全関連認証:
 - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧: 7000V_{PK}
 - UL 1577 に準拠した絶縁耐圧: $5000\text{V}_{\text{RMS}}$ (1 分間)

2 アプリケーション

- トラクション インバータ
- オンボード チャージャ
- DC/DC コンバータ
- バッテリー ジャンクション ボックス

3 概要

AMC0381D-Q1 は、高電圧 DC、高インピーダンス入力、固定ゲイン、差動出力備えた高精度、電氣的絶縁型アンプです。入力は、高電圧信号源に直接接続できる設計を採用しています。

この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離します。絶縁バリアは、磁気干渉に対して高い耐性があり、最大 5kV_{RMS} (60s) の強化絶縁を実現することが認証されています。

AMC0381D-Q1 は、入力電圧に比例する差動信号を出力します。差動出力はグラウンド シフトの影響を受けず、長距離にわたる出力信号の配線が可能です。

AMC0381D-Q1 は、次の 3 つのリニア入力電圧範囲で供給されます。(600V、1000V、1600V) を使用しています。高精度の抵抗分圧器を内蔵した、AMC0381D-Q1 は寿命ドリフトも含め全温度範囲で 1% 未満の精度を達成しています。

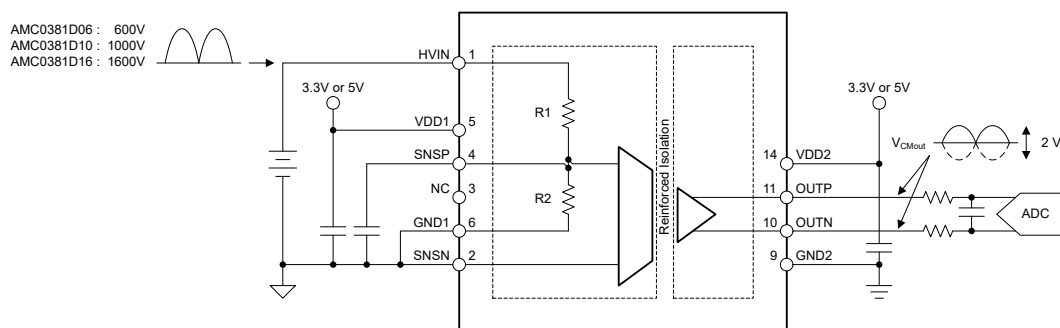
AMC0381D-Q1 は 15 ピン、0.65mm ピッチの SSOP パッケージで供給され、 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ の温度範囲で完全に動作が規定されています。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ サイズ ⁽²⁾
AMC0381D-Q1	DFX (SSOP, 15)	12.8mm × 10.3mm

- 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。





代表的なアプリケーション

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Device Comparison Table

表 4-1. Device Comparison

DEVICE	R1	R2	DIVIDER RATIO	LINEAR INPUT RANGE	CLIPPING VOLTAGE	ABS MAX INPUT VOLTAGE
AMC0381D06-Q1 ⁽¹⁾	10MΩ	16.6kΩ	601:1	600V	769V	900V
AMC0381D10-Q1	12.5MΩ	12.5kΩ	1001:1	1000V	1281V	1500V
AMC0381D16-Q1 ⁽¹⁾	33MΩ	21kΩ	1601:1	1600V	2049V	2000V

(1) Product preview.

4 Pin Configuration and Functions

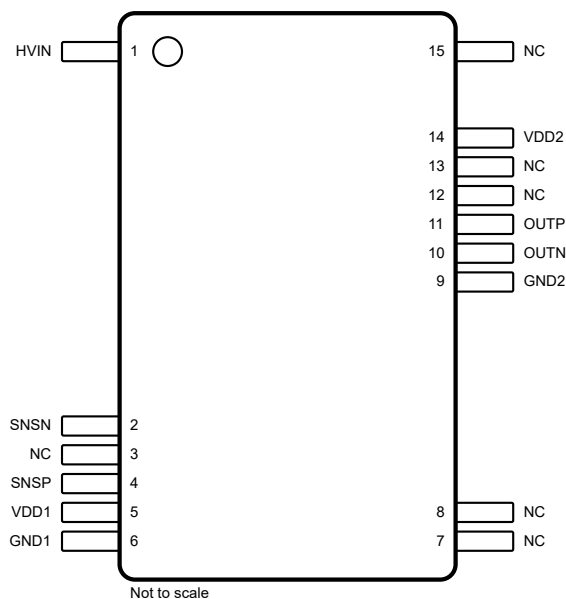


図 4-1. DFX パッケージ, 15 ピン SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	HVIN	Analog input	High-voltage input
2	INN	Analog input	Ground sense pin and inverting analog input to the modulator. Connect to GND1.
3, 7, 8, 12, 13, 15	NC	N/A	No internal connection. The pin can be connected to any potential or left floating.
4	SNSP	Analog input	Sense voltage pin and non-inverting analog input to the modulator. Connect to an external filter capacitor or leave floating.
5	VDD1	High-side power	Analog (high-side) power supply ⁽¹⁾
6	GND1	High-side ground	High-side ground
9	GND2	Low-side ground	Low-side ground
10	OUTN	Analog output	Inverting analog output
11	OUTP	Analog input	Noninverting analog output
14	VDD2	Low-side power	Low-side power supply ⁽¹⁾

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

5 Specifications

5.1 Absolute Maximum Ratings

see⁽¹⁾

		MIN	MAX	UNIT
Power-supply voltage	High-side, VDD1 to GND1	−0.3	6.5	V
	Low-side, VDD2 to GND2	−0.3	6.5	
Analog input voltage	HVIN to GND1, AMC0381D06-Q1	−150	900	V
	HVIN to GND1, AMC0381D10-Q1	−150	1500	
	HVIN to GND1, AMC0381D16-Q1	−150	2000	
	SNSP, SNSN	GND1 − 0.5	VDD1 + 0.5	
Analog output voltage	OUTP, OUTN	GND2 − 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply and HVIN pins	−10	10	mA
Temperature	Junction, T _J		150	°C
	Storage, T _{stg}	−65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ , HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD1	High-side power supply	VDD1 to GND1	3	5.0	5.5	V
VDD2	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
V _{Clipping}	Nominal input voltage before clipping output	Referred to SNSP	1.28			V
		Referred to HVIN, AMC0381D06-Q1	769			
		Referred to HVIN, AMC0381D10-Q1	1281			
		Referred to HVIN, AMC0381D16-Q1	2049			
V _{FSR}	Specified linear input voltage	Referred to SNSP	−0.05	1		V
		Referred to HVIN, AMC0381D06-Q1	−30	600		
		Referred to HVIN, AMC0381D10-Q1	−50	1000		
		Referred to HVIN, AMC0381D16-Q1	−80	1600		
TEMPERATURE RANGE						
T _A	Specified ambient temperature		−40	125		°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DFX (SSOP)	UNIT
		15 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	86.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	36.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	17	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	41.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P _D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5V	TBD	mW
P _{D1}	Maximum power dissipation (high-side)	AVDD = 3.6V	TBD	mW
		AVDD = 5.5V	TBD	
P _{D2}	Maximum power dissipation (low-side)	DVDD = 3.6V	TBD	mW
		DVDD = 5.5V	TBD	

5.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage ⁽¹⁾	Shortest pin-to-pin distance across the package surface	≥ 9.2	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V _{RMS}	I-III	
		Rated mains voltage ≤ 1000V _{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1410	V _{PK}
V _{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1000	V _{RMS}
		At DC voltage	1410	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60s (qualification test), V _{TEST} = 1.2 × V _{IOTM} , t = 1s (100% production test)	7000	V _{PK}
V _{IMP}	Maximum impulse voltage ⁽³⁾	Tested in air, 1.2/50μs waveform per IEC 62368-1	7700	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽⁴⁾	Tested in oil (qualification test), 1.2/50μs waveform per IEC 62368-1	10000	V _{PK}
q _{pd}	Apparent charge ⁽⁵⁾	Method a, after input/output safety test subgroups 2 and 3, V _{pd(ini)} = V _{IOTM} , t _{ini} = 60s, V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V _{pd(ini)} = V _{IOTM} , t _{ini} = 60s, V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, V _{pd(ini)} = 1.2 × V _{IOTM} , t _{ini} = 1s, V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1s	≤ 5	
		Method b2, at routine test (100% production) ⁽⁷⁾ V _{pd(ini)} = V _{pd(m)} = 1.2 × V _{IOTM} , t _{ini} = t _m = 1s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁶⁾	V _{IO} = 0.5 V _{PP} at 1MHz	~1.5	pF
R _{IO}	Insulation resistance, input to output ⁽⁶⁾	V _{IO} = 500V at T _A = 25°C	> 10 ¹²	Ω
		V _{IO} = 500V at 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	
		V _{IO} = 500V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} , t = 60s (qualification test), V _{TEST} = 1.2 × V _{ISO} , t = 1s (100% production test)	5000	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.

5.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

5.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current	R _{θJA} = TBD°C/W, VDDx = 5.5V, T _J = 150°C, T _A = 25°C			TBD	mA
I _S	Safety input, output, or supply current	R _{θJA} = TBD°C/W, VDDx = 3.6V, T _J = 150°C, T _A = 25°C			TBD	mA
P _S	Safety input, output, or total power	R _{θJA} = TBD°C/W, T _J = 150°C, T _A = 25°C			TBD	mW
T _S	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.

T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum junction temperature.

P_S = I_S × VDD_{max}, where VDD_{max} is the maximum supply voltage for high-side and low-side.

5.9 Electrical Characteristics

minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{V}$ to 5.5V , $V_{DD2} = 3.0\text{V}$ to 5.5V , $V_{SNSP} = 0\text{V}$ to $+1\text{V}$, and $V_{SNSN} = 0\text{V}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{V}$, $V_{DD2} = 3.3\text{V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
ANALOG INPUT							
R _{IN}	Input resistance	AMC0381D06-Q1	TBD	10	TBD	MΩ	
		AMC0381D10-Q1	TBD	12.5	TBD		
		AMC0381D16-Q1	TBD	33	TBD		
	Nominal resistive divider ratio	V _{HVIN} / V _{SNSP} , AMC0381D06-Q1	601			V/V	
		V _{HVIN} / V _{SNSP} , AMC0381D10-Q1	1001				
		V _{HVIN} / V _{SNSP} , AMC0381D16-Q1	1601				
CMTI	Common-mode transient immunity		50			V/ns	
ANALOG OUTPUT							
	Nominal attenuation	V _{HVIN} / (V _{OUTP} – V _{OUTN}), AMC038D06-Q1	601 : 2			V/V	
		V _{HVIN} / (V _{OUTP} – V _{OUTN}), AMC038D10-Q1	1001 : 2				
		V _{HVIN} / (V _{OUTP} – V _{OUTN}), AMC038D16-Q1	1601 : 2				
V _{CMout}	Output common-mode voltage		1.39	1.44	1.49	V	
V _{CLIPout}	Clipping differential output voltage	V _{OUT} = (V _{OUTP} – V _{OUTN}); V _{IN} > V _{Clipping}	2.49			V	
V _{FAILSAFE}	Failsafe differential output voltage	VDD1 undervoltage, or VDD1 missing	–2.6			–2.5	V
R _{OUT}	Output resistance	OUTP or OUTN	<0.2			Ω	
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, HVIN = GND1, outputs shorted to either GND or VDD2	11			mA	
DC ACCURACY							
V _{OS}	Input offset voltage	Referred to SNSP, T _A = 25°C, HVIN = GND1	–1.5	±0.4	1.5	mV	
		Referred to HVIN, HVIN = GND1, T _A = 25°C, AMC038D06-Q1	–900	±240	900		
		Referred to HVIN, HVIN = GND1, T _A = 25°C, AMC038D10-Q1	–1500	±400	1500		
		Referred to HVIN, HVIN = GND1, T _A = 25°C, AMC038D16-Q1	–2400	±640	2400		
TCV _{OS}	Input offset thermal drift ⁽³⁾	Referred to SNSP, HVIN = GND1	–0.01	±0.003	0.01	mV/°C	
		Referred to HVIN, HVIN = GND1, AMC038D06-Q1	–6	±1.8	6		
		Referred to HVIN, HVIN = GND1, AMC038D10-Q1	–10	±3	10		
		Referred to HVIN, HVIN = GND1, AMC038D16-Q1	–16	±4.8	16		
E _A	Attenuation error ⁽¹⁾	T _A = 25°C	–0.25	±0.05	0.25	%	
TCE _A	Attenuation error temperature drift ⁽⁴⁾		–40	±20	40	ppm/°C	
	Nonlinearity ⁽²⁾		–0.05%	±0.01%	0.05%		
	Output noise	V _{IN} = GND1, BW = 100kHz	TBD			μVrms	
PSRR	Power-supply rejection ratio ⁽⁵⁾	VDD1 DC PSRR, HVIN = GND1, VDD1 from 3V to 5.5V	–80			dB	
		VDD1 AC PSRR, HVIN = GND1, VDD1 with 10kHz / 100mV ripple	–80				
		VDD2 DC PSRR, HVIN = GND1, VDD2 from 3V to 5.5V	–100				
		VDD2 AC PSRR, HVIN = GND1, VDD2 with 10kHz / 100mV ripple	–86				
AC ACCURACY							
BW	Output bandwidth		90	110		kHz	

5.9 Electrical Characteristics (続き)

minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{V}$ to 5.5V , $V_{DD2} = 3.0\text{V}$ to 5.5V , $V_{SNSP} = 0\text{V}$ to $+1\text{V}$, and $V_{SNSN} = 0\text{V}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{V}$, $V_{DD2} = 3.3\text{V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{SNSP} = 1V_{PP}$, $SNSN = \text{GND1}$, $f_{IN} = 10\text{kHz}$, $BW = 10\text{kHz}$		–93		dB
SNR	Signal-to-noise ratio	$V_{SNSP} = 1V_{PP}$, $SNSN = \text{GND1}$, $f_{IN} = 1\text{kHz}$, $BW = 10\text{kHz}$	73	79		dB
SNR	Signal-to-noise ratio	$V_{SNSP} = 1V_{PP}$, $SNSN = \text{GND1}$, $f_{IN} = 10\text{kHz}$, $BW = 100\text{kHz}$		64.9		dB
POWER SUPPLY						
I_{DD1}	High-side supply current			5.3	7.5	mA
I_{DD2}	Low-side supply current			3.6	5.1	mA
V_{DD1UV}	High-side undervoltage detection threshold	VDD1 rising	2.3	2.55	2.75	V
		VDD1 falling	2.15	2.35	2.55	
V_{DD2UV}	Low-side undervoltage detection threshold	VDD2 rising	2.3	2.55	2.75	V
		VDD2 falling	2.15	2.35	2.55	

- (1) The typical value includes one sigma statistical variation.
- (2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
- (3) Offset error drift is calculated using the box method, as described by the following equation:

$$TCE_O = (\text{value}_{MAX} - \text{value}_{MIN}) / \text{TempRange}$$
- (4) Gain error drift is calculated using the box method, as described by the following equation:

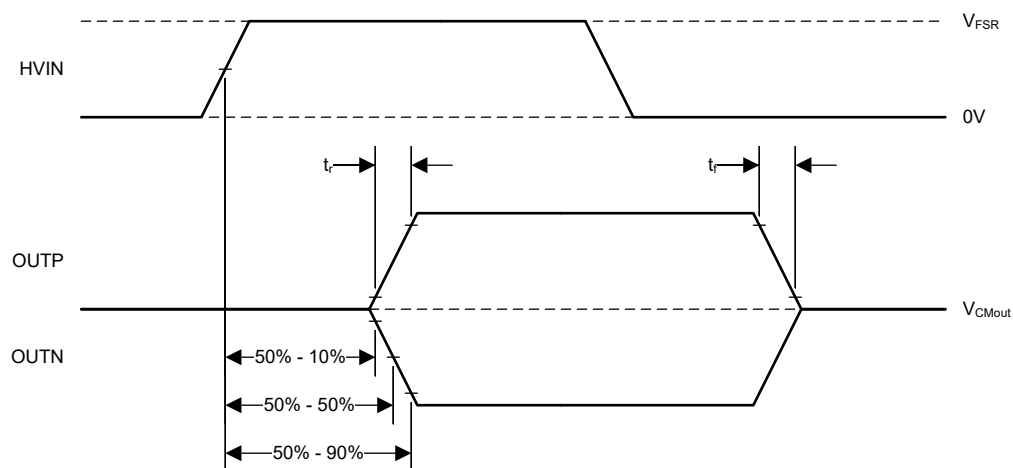
$$TCE_G (\text{ppm}) = ((\text{value}_{MAX} - \text{value}_{MIN}) / (\text{value} \times \text{TempRange})) \times 10^6$$
- (5) This parameter is referred to SNSP.

5.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.8		μs
t_f	Output signal fall time			1.8		μs
	V_{HVIN} to V_{OUTX} signal delay (50% – 10%)	Unfiltered output		2.4		μs
	V_{HVIN} to V_{OUTX} signal delay (50% – 50%)	Unfiltered output		3.0	3.2	μs
	V_{HVIN} to V_{OUTX} signal delay (50% – 90%)	Unfiltered output		4.2		μs
t_{AS}	Analog settling time	VDD1 step to 3.0V with $V_{DD2} \geq 3.0\text{V}$, to V_{OUTP} , V_{OUTN} valid, 0.1% settling		50	100	μs

5.11 Timing Diagram



5-1. Rise, Fall, and Delay Time Definition

6 Detailed Description

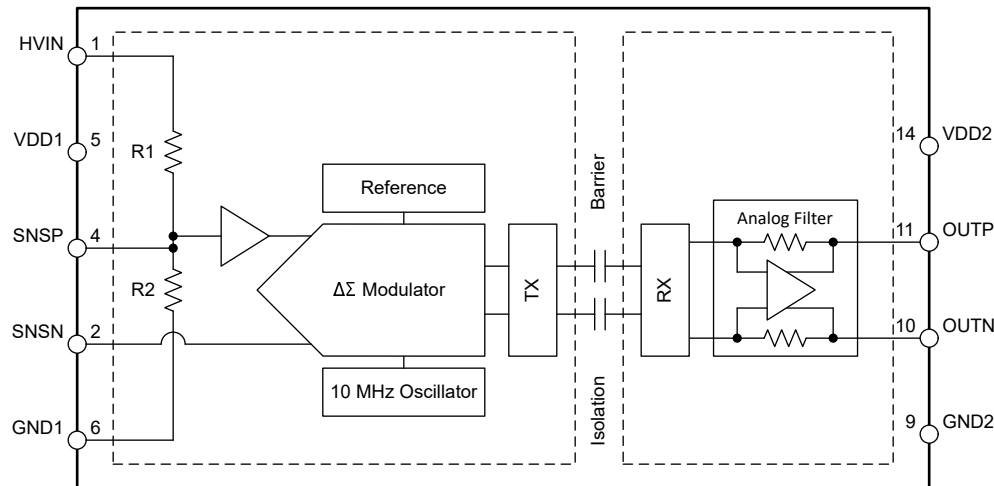
6.1 Overview

The AMC0381D-Q1 is a precision, galvanically isolated amplifier with a 高電圧 DC、高インピーダンス入力、固定ゲイン、差動出力. The input stage of the device drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high side from the low side.

On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins. This differential output signal is proportional to the input signal.

The SiO₂-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application note](#). The digital modulation used in the AMC0381D-Q1 transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

6.2 Functional Block Diagram



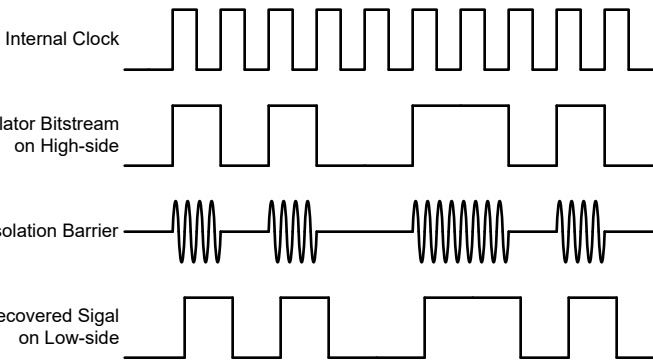
6.3 Feature Description

6.3.1 Analog Input

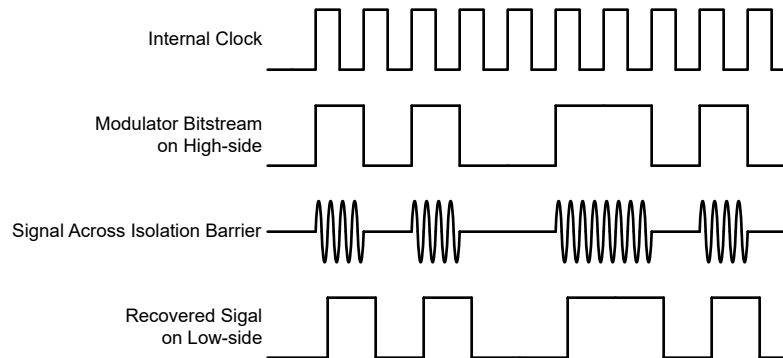
The resistive divider at the input of the AMC0381D-Q1 scales down the voltage applied to the HVIN pin to a 1V linear fullscale level. This signal is available on the SNSP pin, which is also the input of the analog signal chain.

The input stage of the AMC0381D-Q1 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

6.3.2 Isolation Channel Signal Transmission

The AMC0381D-Q1 uses an on-off keying (OOK) modulation scheme, as shown in  6-1, to transmit the modulator output bitstream across the SiO₂-based isolation barrier. The transmit driver (TX), as illustrated in the [Functional Block Diagram](#), transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0381D-Q1 is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC0381D-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.



 6-1. OOK-Based Modulation Scheme

6.3.3 Analog Output

The AMC0381D-Q1 provides a differential analog output voltage on the OUTP and OUTN pins that is proportional to the input voltage. For input voltages in the range from $V_{FSR, MIN}$ to $V_{FSR, MAX}$, the device has a linear response with an output voltage equal to:

$$(V_{OUTP} - V_{OUTN}) = V_{IN} = V_{HVIN} / \text{Attenuation} - V_{SNSN} \quad (1)$$

At zero input, both pins output the same common-mode output voltage V_{CMout} , as specified in the *Electrical Characteristics* table. For absolute input voltages greater than $|V_{FSR}|$ but less than $|V_{Clipping}|$, the differential output voltage continues to increase in magnitude, but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in 図 6-2, if the input voltage exceeds the $V_{Clipping}$ value.

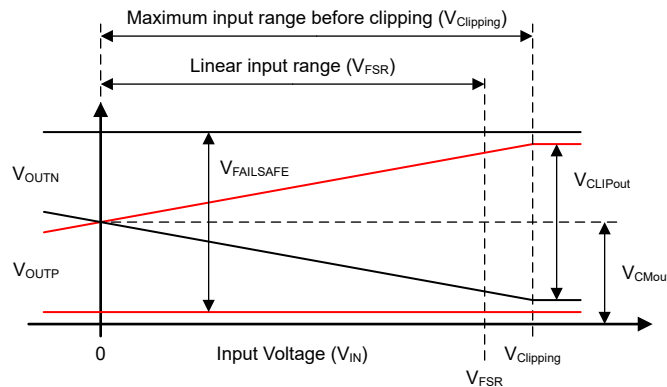


図 6-2. Input to Output Transfer Curve of the AMC0381D-Q1

The AMC0381D-Q1 output offers a fail-safe feature that simplifies diagnostics on a system level. 図 6-2 shows the behavior in fail-safe mode, in which the AMC0381D-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active:

- When the high-side supply VDD1 of the AMC0381D-Q1 device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold $VDD1_{UV}$

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on a system level.

6.4 Device Functional Modes

The AMC0381D-Q1 operates in one of the following states:

- **OFF-state:** The low-side supply ($VDD2$) is below the $VDD2_{UV}$ threshold. The device is not responsive. OUTP と OUTN は Hi-Z 状態です。内部では、OUTP および OUTN は ESD 保護ダイオードによって $VDD2$ および $GND2$ にクランプされます。
- **Missing high-side supply:** The low-side of the device ($VDD2$) is supplied and within the *Recommended Operating Conditions* section. The high-side supply ($VDD1$) is below the $VDD1_{UV}$ threshold. このデバイスは $V_{FAILSAFE}$ 電圧を出力します。
- **Analog input overrange (positive fullscale input):** $VDD1$ and $VDD2$ are within recommended operating conditions but the analog input voltage V_{IN} is above the maximum clipping voltage $V_{Clipping, MAX}$. このデバイスは正の $V_{CLIPout}$ を出力します。
- **Analog input underrange (negative fullscale input):** $VDD1$ and $VDD2$ are within recommended operating conditions but the analog input voltage V_{IN} is below the minimum clipping voltage $V_{Clipping, MIN}$. このデバイスは負の $V_{CLIPout}$ を出力します。
- **Normal operation:** $VDD1$, $VDD2$, and V_{IN} are within the recommended operating conditions. このデバイスは、入力電圧に比例する差動電圧を出力します。

表 6-1 lists the operating modes.

表 6-1. Device Operational Modes

OPERATING CONDITION	VDD1	VDD2	V _{IN}	DEVICE RESPONSE
OFF	Don't care	VDD2 < VDD2 _{UV}	Don't care	OUTP と OUTN は Hi-Z 状態です。内部では、OUTP および OUTN は ESD 保護ダイオードによって VDD2 および GND2 にクランプされます。
Missing high-side supply	VDD1 < VDD1 _{UV}	Valid ⁽¹⁾	Don't care	このデバイスは V _{FAILSAFE} 電圧を出力します。
Input overrange	Valid ⁽¹⁾	Valid ⁽¹⁾	V _{IN} > V _{Clipping, MAX}	このデバイスは正の V _{CLIPout} を出力します。
Input underrange	Valid ⁽¹⁾	Valid ⁽¹⁾	V _{IN} < V _{Clipping, MIN}	このデバイスは負の V _{CLIPout} を出力します。
Normal operation	Valid ⁽¹⁾	Valid ⁽¹⁾	Valid ⁽¹⁾	このデバイスは、入力電圧に比例する差動電圧を出力します。

(1) "Valid" denotes within the recommended operating conditions.

7 Application and Implementation

注

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7.1 Application Information

The high input impedance, low input bias current, excellent accuracy, and low-temperature drift make the AMC0381D-Q1 a high-performance system for automotive applications where voltage sensing in the presence of high common-mode voltage levels is required.

7.2 Best Design Practices

Avoid any kind of leakage current between the INP and SNSP pin. Leakage current potentially introduces significant measurement error. See the [Layout Example](#) for layout recommendations.

7.3 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0381D-Q1 is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver [SN6501-Q1](#) and a transformer that supports the desired isolation voltage ratings.

The AMC0381D-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1μF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1μF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. [Figure 7-1](#) shows a decoupling diagram for the AMC0381D-Q1.

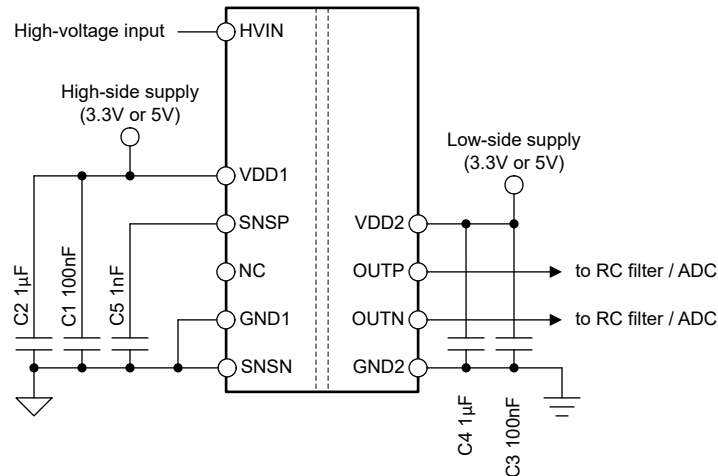


Figure 7-1. Decoupling of the AMC0381D-Q1

Capacitors provide adequate effective capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Take into consideration this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

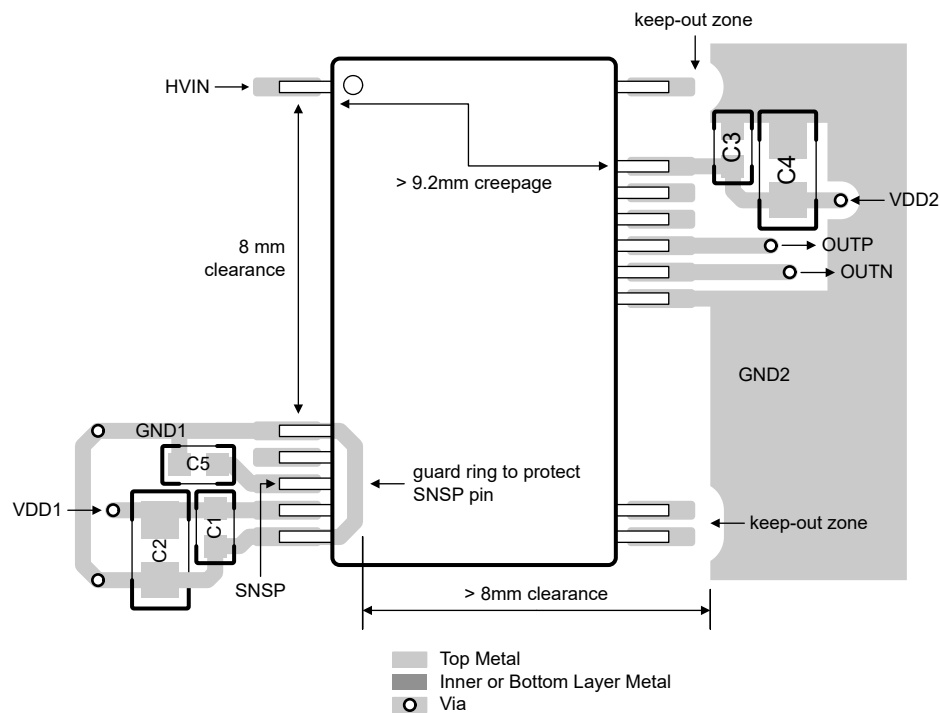
7.4 Layout

7.4.1 Layout Guidelines

The [Layout Example](#) section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0381D-Q1 supply pins). This example also depicts the placement of other components required by the device. For best performance, place the sense resistor close to the device input pin (INP).

7.4.2 Layout Example

図 7-2. Recommended Layout of the AMC0381D-Q1



8 デバイスおよびドキュメントのサポート

8.1 ドキュメントのサポート

8.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『[絶縁の用語集](#)』アプリケーション レポート
- テキサス・インスツルメンツ、『[半導体および IC パッケージの熱評価基準](#)』アプリケーション レポート
- テキサス・インスツルメンツ、『[ISO72x デジタル アイソレータの磁界耐性](#)』アプリケーション レポート
- テキサス・インスツルメンツ、『[絶縁型アンプの電圧センシング Excel カリキュレータ](#)』設計ツール

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 商標

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8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

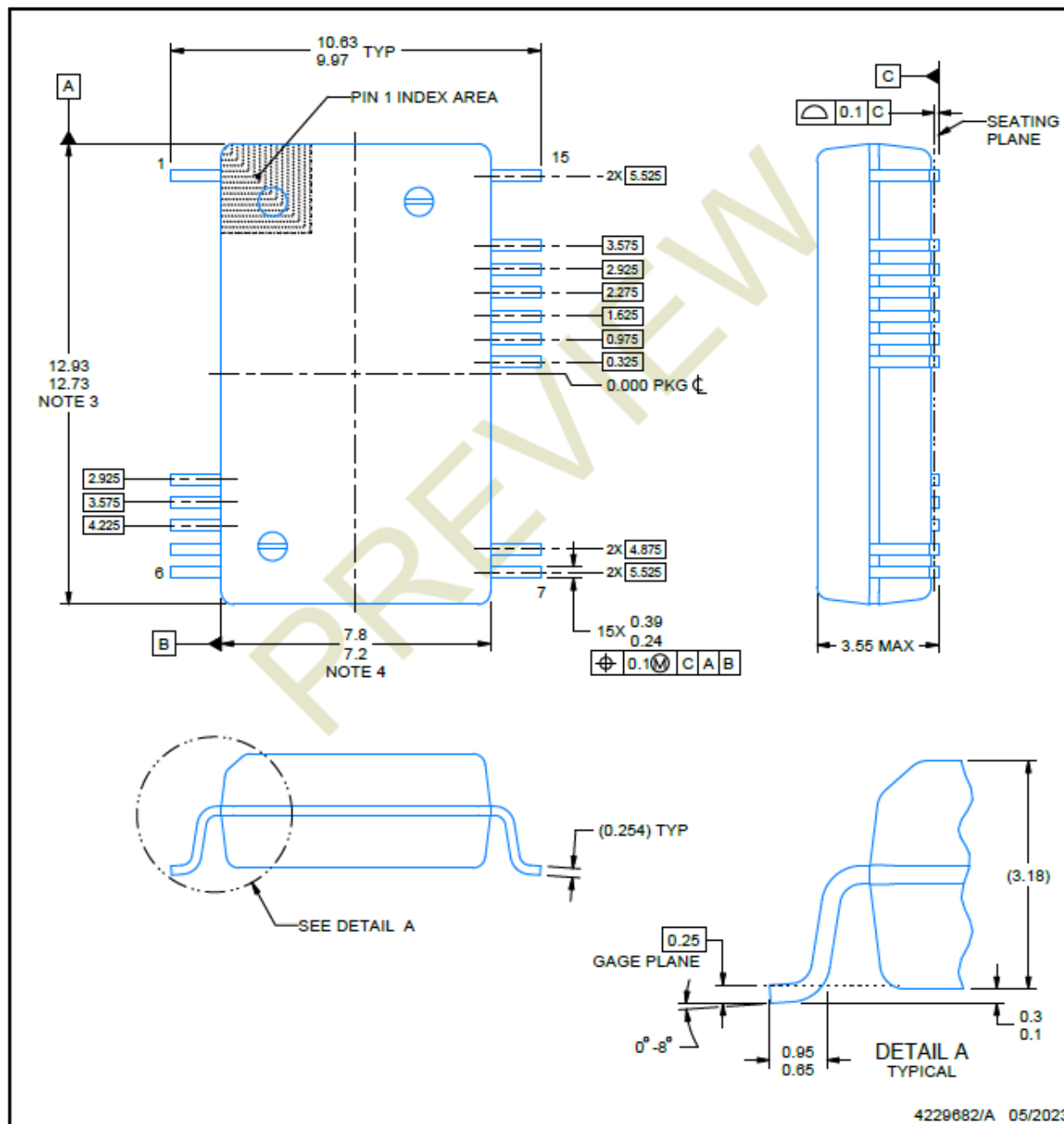


PACKAGE OUTLINE

DFX0015A

SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES:

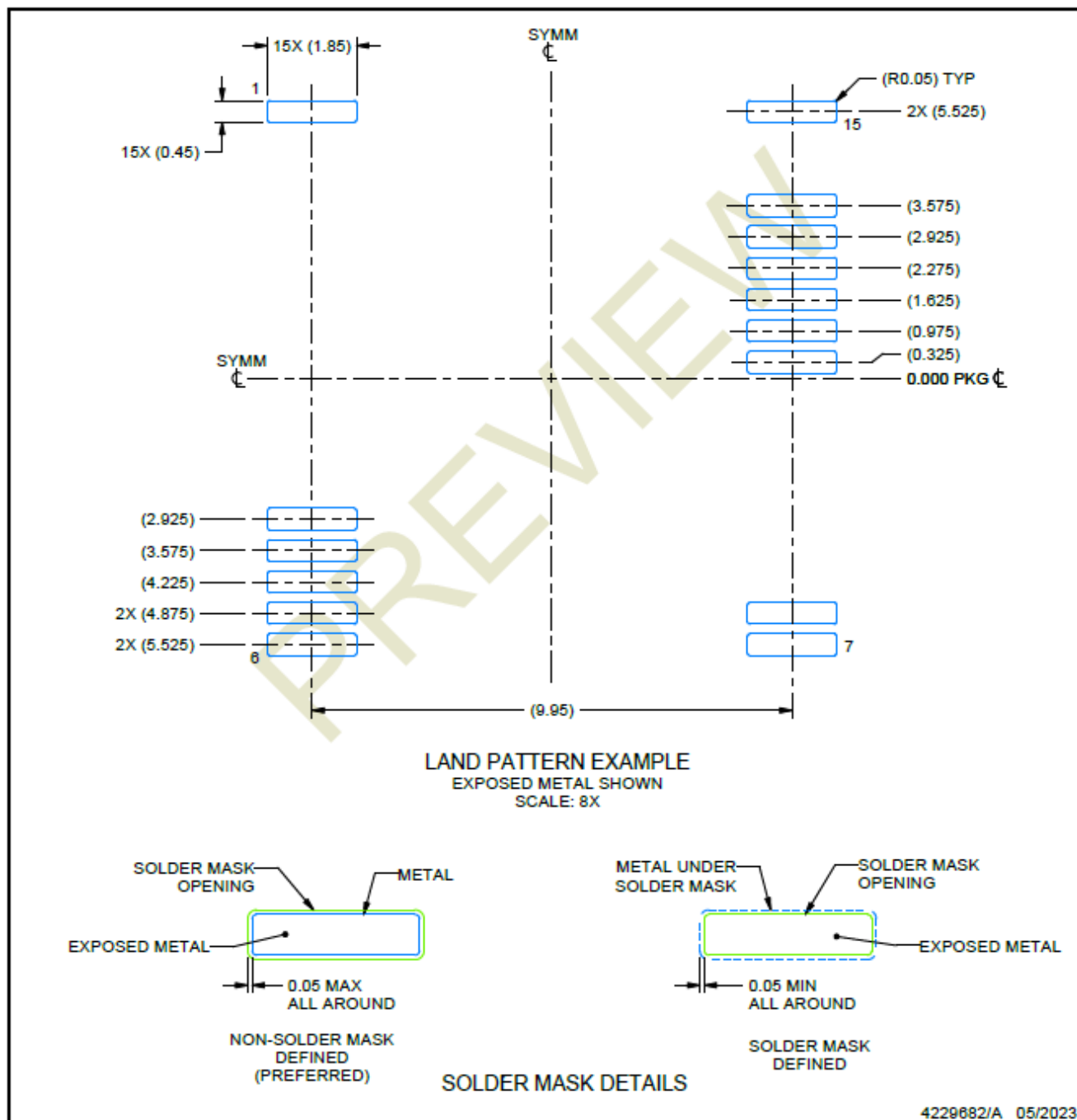
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

DFX0015A

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NOTES: (continued)

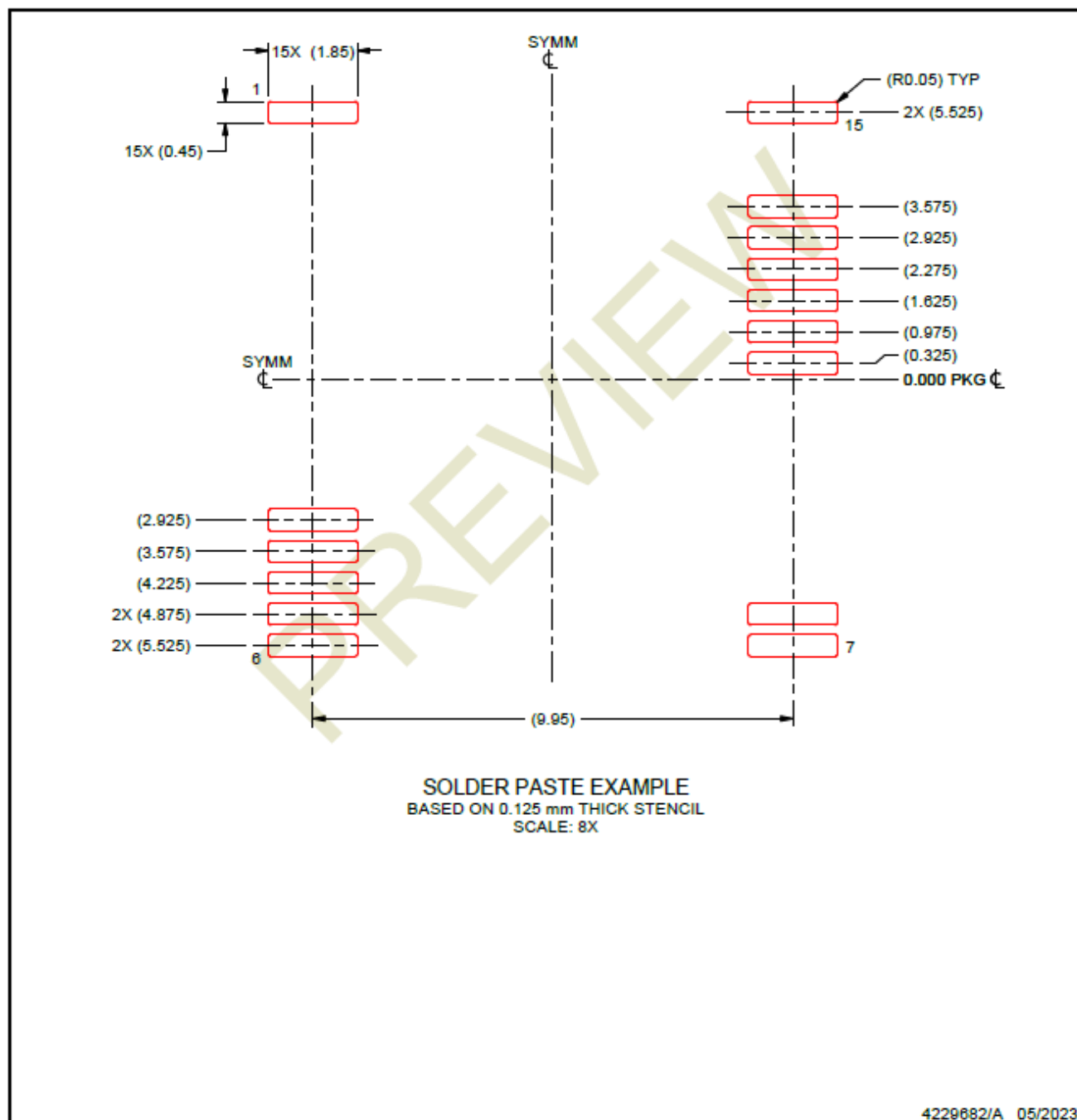
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFX0015A

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PAMC0381D10QDFXRQ1	Active	Preproduction	SSOP (DFX) 15	750 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PAMC0381D10QDFXRQ1.A	Active	Preproduction	SSOP (DFX) 15	750 LARGE T&R	-	Call TI	Call TI	See PAMC0381D10QDFXRQ	
PAMC0381D10QDFXRQ1.B	Active	Preproduction	SSOP (DFX) 15	750 LARGE T&R	-	Call TI	Call TI	See PAMC0381D10QDFXRQ	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

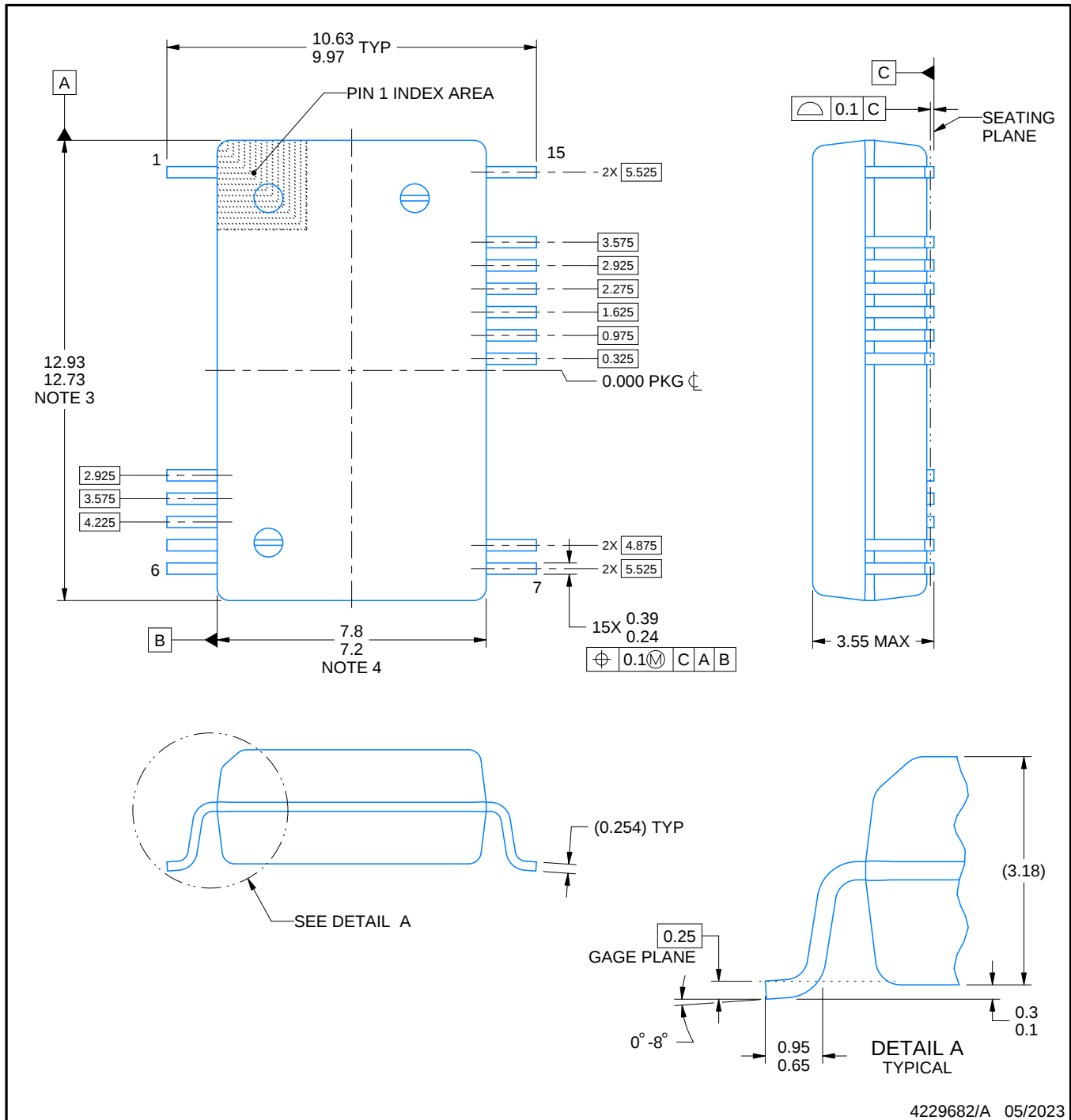
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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NOTES:

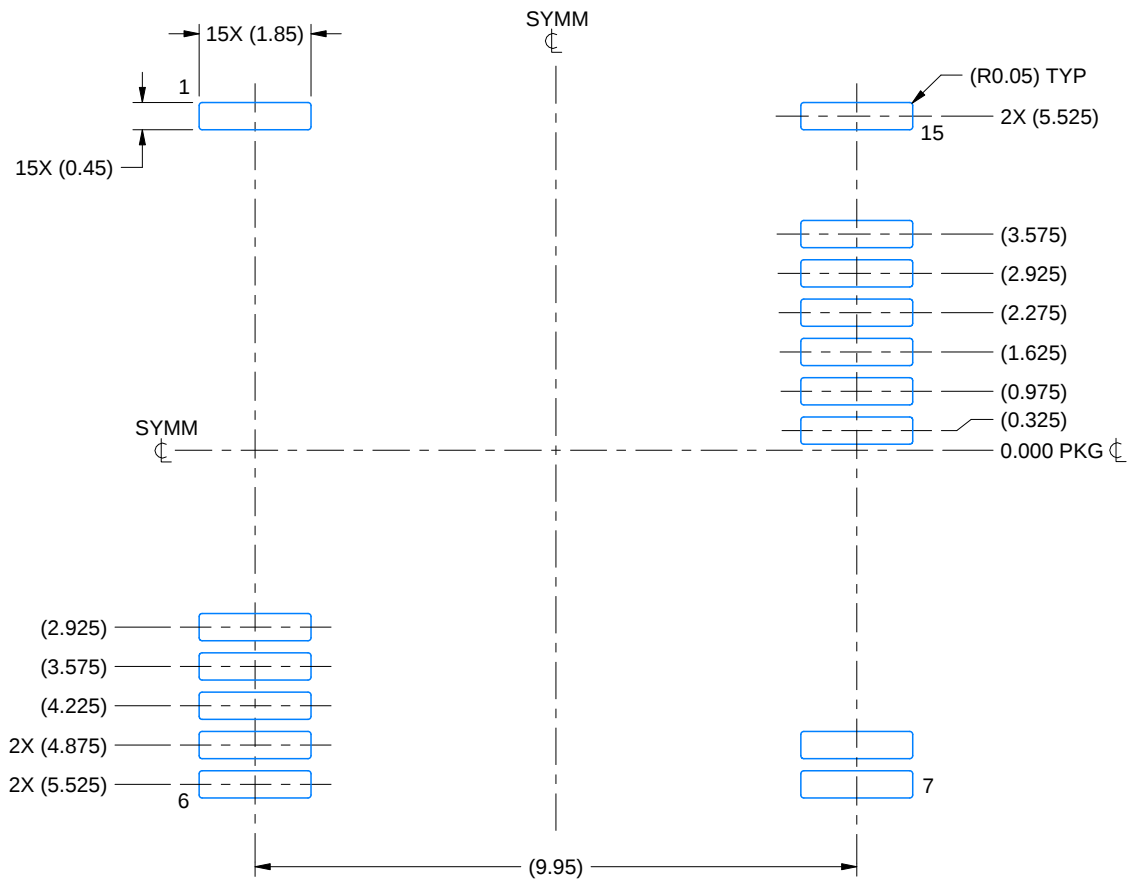
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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EXAMPLE BOARD LAYOUT

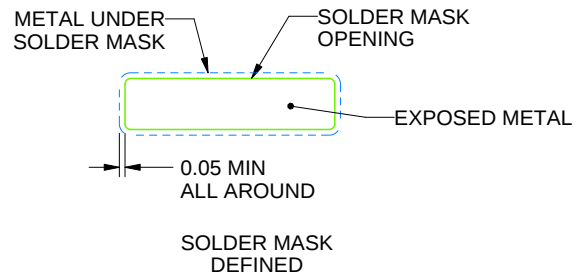
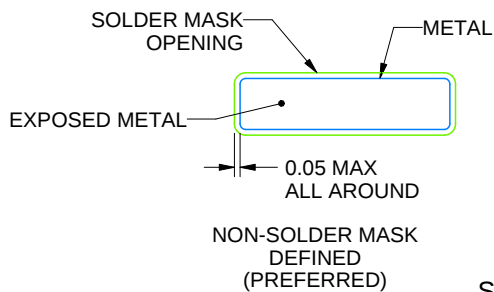
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LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4229682/A 05/2023

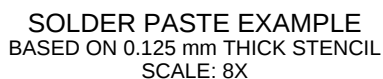
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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