AMC0x11S 固定ゲイン シングルエンド出力付き、高精度、2.25V 入力、基本および強化絶縁型アンプ

1 特長

- リニア入力電圧範囲：0～2.25 V
- 高い入力インピーダンス：1GΩ (標準値)
- 電源電圧範囲：
  - ハイサイド (VDD1)：3.0V～5.5V
  - ローサイド (VDD2)：3.0V～5.5V
- 固定ゲイン：1V/V
- シングルエンド出力
- 小さい DC 誤差：
  - オフセット誤差：±1mV (最大値)
  - オフセット ドリフト：±25µV/°C (最大値)
  - ゲイン誤差：±0.25% (最大値)
  - ゲイン ドリフト：±40ppm/°C (最大値)
  - 非線形性：±0.02% (最大値)
- 「高 CMTI：50V/ns (最小値)
- 低 EMI：CISPR-11 および CISPR-25 規格に準拠
- 絶縁定格：
  - AMC0211S：基本絶縁型
  - AMC0311S：強化絶縁型
- 安全関連認証：
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577
- 産業温度範囲の全体にわたって完全に仕様を規定：-40℃～+105℃

2 アプリケーション

- モーター ドライブ
- 太陽光発電インバータ
- サーバー電源ユニット (PSU)
- EV 充電ステーション

3 概要

AMC0x11S は、2.25V、高インピーダンス入力、固定ゲイン、シングルエンド出力備えた高精度、電気的絶縁型アンプです。高インピーダンス入力は、高インピーダンスの抵抗分圧器や出力抵抗の高い他の電圧信号源と接続するよう最適化されています。

この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離します。絶縁バリアは磁気干渉に対して非常に耐性があります。この絶縁バリアは、最大 5kV$_{RMS}$ (DWV パッケージ) の強化絶縁と、最大 3kV$_{RMS}$ (D パッケージ) (60s) の基本絶縁を実現することが認定されています。

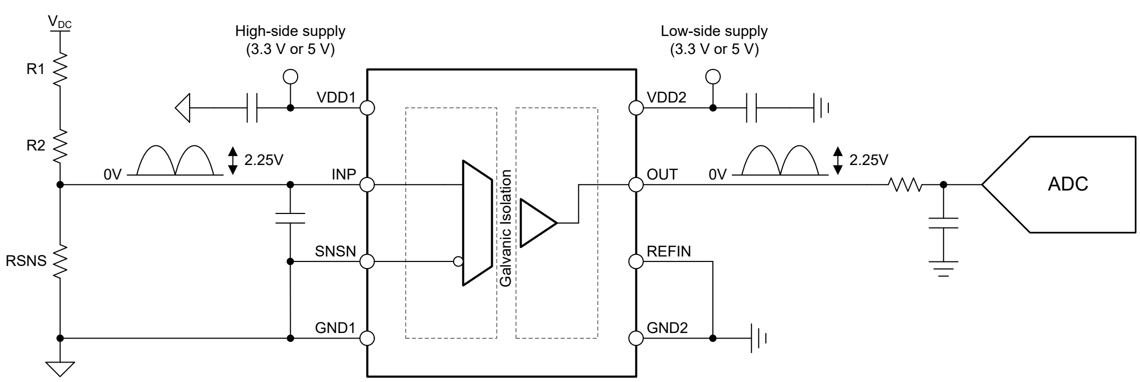
AMC0x11S は、1V/V の固定ゲインで入力電圧に比例するシングルエンド信号を出力します。出力は、ADC の入力に直接接続できるように設計されています。REFIN ピンに印加される電圧によって、0V 入力の出力電圧が設定されます。

AMC0x11S デバイスは、8 ピンのワイド ボディおよびナロー ボディ SOIC パッケージで供給され、–40°C から +105°C までの温度範囲で完全に動作が規定されています。

パッケージ情報

部品番号	パッケージ [1]	パッケージ サイズ[2]
AMC0211S [3]	D (SOIC 8)	4.9mm × 6.0mm
AMC0311S	DWV (SOIC 8)	5.85mm × 11.5mm

(1) 詳細については、付録「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。
(3) 製品プレビュー



代表的なアプリケーション

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4 Device Comparison Table

PARAMETER	AMC0211S [(1)]	AMC0311S
Isolation rating per VDE 0884-17	Basic	Reinforced
Package	Narrow-body SOIC (D)	Wide-body SOIC (DWV)

(1) PRODUCT PREVIEW

5 Pin Configuration and Functions

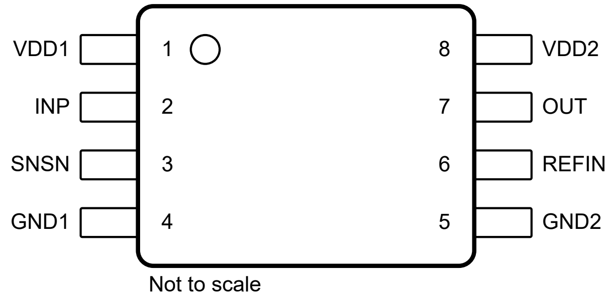


図 5-1. DWV および D パッケージ, 8 ピン SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply(1)
2	INP	Analog input	Analog input
3	SNSN	Analog input	GND1 sense pin and inverting analog input to the modulator. Connect to GND1.
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	REFIN	Analog input	このピンに印加される電圧は、本デバイスの出力電圧に対するオフセットとして追加されます。内部では、90kΩ 抵抗が REFIN と GND2 の間に接続されています。未使用時は GND2 に接続してください。
7	OUT	Analog output	Analog output
8	VDD2	Low-side power	Low-side power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, SNSN to GND1	GND1 – 3	VDD1 + 0.5	V
Reference input voltage	REFIN to GND2	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD1	High-side power supply	VDD1 to GND1	3	5.0	5.5	V
VDD2	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Nominal input voltage before clipping output	$V_{IN} = V_{INP} – V_{SNSN}$	0		2.56	V
V_{FSR}	Specified linear input voltage	$V_{IN} = V_{INP} – V_{SNSN}$	0[1]		2.25	V
V_{REFIN}	Reference input voltage	REFIN to GND2	0		VDD2	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	OUT to GND2			500	pF
R_{LOAD}	Resistive load	OUT to GND2		10	1	kΩ
TEMPERATURE RANGE						
T_A	Specified ambient temperature	Specified ambient temperature	–40		105	°C

(1) See the *Analog Output* section for details.

6.4 Thermal Information (D Package)

THERMAL METRIC[(1)]		D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Thermal Information (DWV Package)

THERMAL METRIC[1]		DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5V	72	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 5.5V	33	mW
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5V	39	mW

6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1130	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	800	V_{RMS}
		At DC voltage	1130	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	4250	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7), $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $300V_{RMS}$	I-IV	
		Rated mains voltage ≤ $6000V_{RMS}$	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	$V_{IO} = 0.5V_{PP}$ at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.9 Safety-Related Certifications (Basic Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic insulation	Single protection
Certificate number: Pending	File number: Pending

6.10 Safety-Related Certifications (Reinforced Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

6.11 Safety Limiting Values (D Package)

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 116.5°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			195	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 116.5°C/W, T_J = 150°C, T_A = 25°C			1070	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.12 Safety Limiting Values (DWV Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			220	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1210	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.13 Electrical Characteristics

minimum and maximum specification0s apply from T_A = –40°C to +105°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, REFIN = GND2, SNSN = GND1, V_{INP} = 0.25V to 2.25V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5V, and VDD2 = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
C_{IN}	Input capacitance			2		pF
R_{INP}	Input impedance	INP pin to GND1	0.1	1		GΩ
$I_{IB, INP}$	Input bias current(1)	INP pin, INP = GND1	–10	±3	10	nA
CMTI	Common-mode transient immunity		50			V/ns
ANALOG OUTPUT						
	Nominal gain			1		V/V
R_{OUT}	Output resistance	OUTP or OUTN		<0.2		Ω
	Output short-circuit current	sourcing or sinking, INP = GND1, output shorted to either GND2 or VDD2		11		mA
DC ACCURACY						
V_{OS}	Input offset voltage(1) (2)	V_{OS} = (V_{OUT} – V_{REFIN}), INP = SNSN = GND1, V_{REFIN} = 250mV, T_A = 25°C	–1	±0.2	1	mV
TCV_{OS}	Input offset thermal drift(1) (2) (4)		–25	±4	25	µV/°C
E_G	Gain error(1)	T_A = 25℃	–0.25%	±0.05%	0.25%	
TCE_G	Gain error drift(1) (5)		–40	±5	40	ppm/°C
	Nonlinearity		–0.02%	±0.002%	0.02%	
	Output noise	INP = GND1, BW = 50kHz		220		µVrms
PSRR	Power-supply rejection ratio(2)	VDD1 DC PSRR, V_{INP} = 250mV, VDD1 from 3V to 5.5V		–80		dB
		VDD1 AC PSRR, V_{INP} = 250mV, VDD1 with 10kHz / 100mV ripple		–56		
		VDD2 DC PSRR, V_{INP} = 250mV, VDD2 from 3V to 5.5V		–90		
		VDD2 AC PSRR, V_{INP} = 250mV, VDD2 with 10kHz / 100mV ripple		–69		
AC ACCURACY						
BW	Output bandwidth		100	125		kHz
THD	Total harmonic distortion(3)	V_{INP} = $2V_{PP}$, V_{INP} > 0V, f_{IN} = 10kHz		–77		dB
SNR	Signal-to-noise ratio	V_{INP} = $2.25V_{PP}$, f_{INP} = 1kHz, BW = 10kHz	76	80		dB
		V_{INP} = $2.25V_{PP}$, f_{INP} = 10kHz, BW = 50kHz		70		
POWER SUPPLY						
I_{DD1}	High-side supply current			4.4	6.0	mA
I_{DD2}	Low-side supply current			4.8	7.0	mA
$VDD1_{UV}$	High-side undervoltage detection threshold	VDD1 rising	2.4	2.6	2.7	V
		VDD1 falling	1.9	2.0	2.1	
$VDD2_{UV}$	Low-side undervoltage detection threshold	VDD2 rising	2.4	2.6	2.7	V
		VDD2 falling	1.9	2.0	2.1	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:

TCV_{OS} = ($Value_{MAX}$ - $Value_{MIN}$) / TempRange

(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
TCE_G (ppm) = ($Value_{MAX}$ - $Value_{MIN}$) / ($Value_{(T=25℃)}$ x TempRange) x 10^6

6.14 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time	10% to 90%, unfiltered output		2.6		μs
t_f	Output signal fall time	10% to 90%, unfiltered output		2.6		μs
	V_{INP} to V_{OUT} signal delay (50% - 10%)	Unfiltered output		2.4		μs
	V_{INP} to V_{OUT} signal delay (50% - 50%)	Unfiltered output		3.0	3.2	μs
	V_{INP} to V_{OUT} signal delay (50% - 90%)	Unfiltered output		4.2		μs
t_{AS}	Analog settling time	AVDD step to 3.0V with DVDD ≥ 3.0V to V_{OUT} valid, 0.1% settling		20		μs

6.15 Timing Diagram

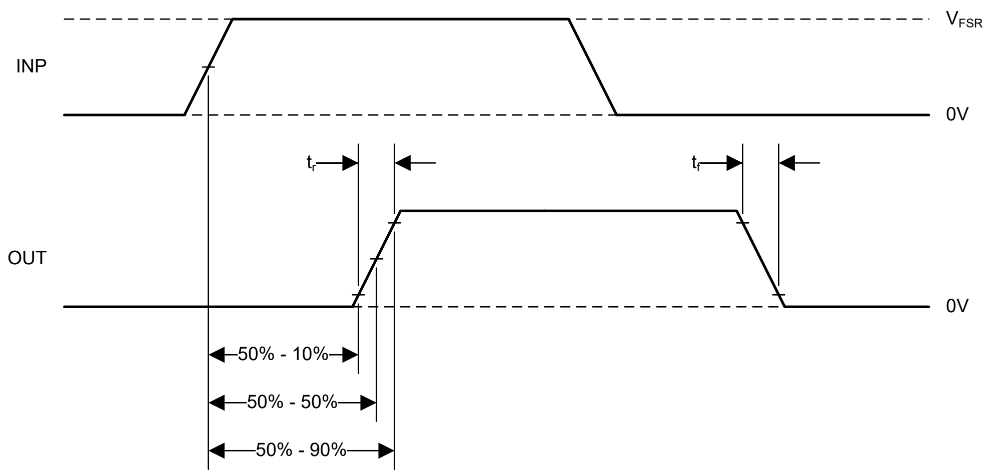


図 6-1. Rise, Fall, and Delay Time Definition

6.16 Insulation Characteristics Curves

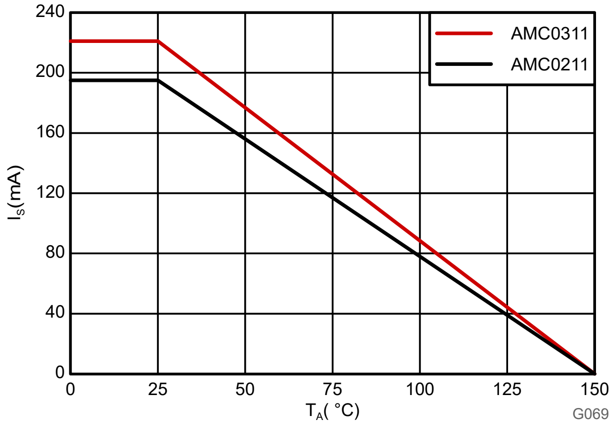


図 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

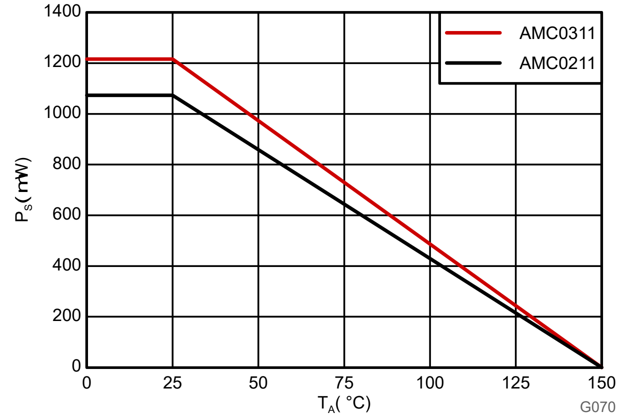
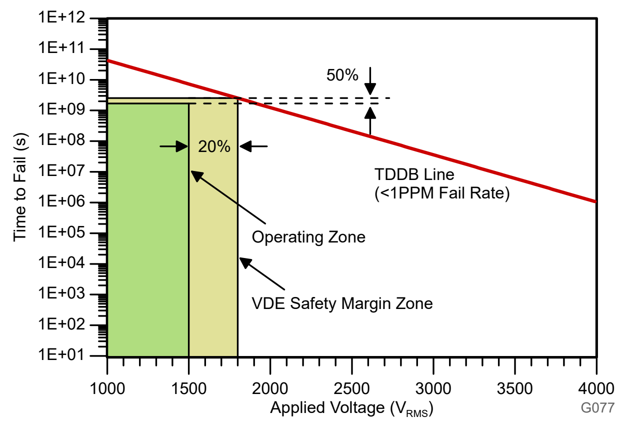


図 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, projected operating lifetime ≥50 years

図 6-4. Isolation Capacitor Lifetime Projection

6.17 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, SNSN = GND1, REFIN = GND2, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

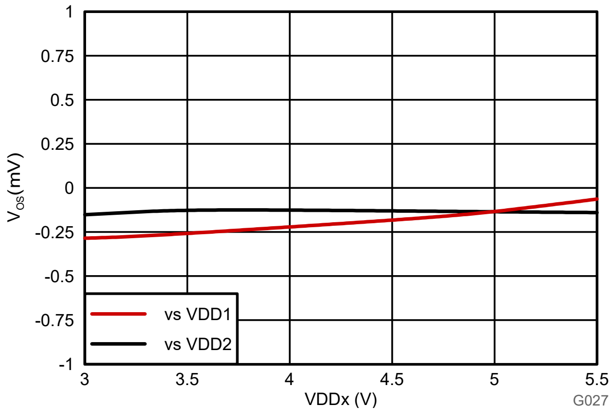


図 6-5. Input Offset Voltage vs Supply Voltage

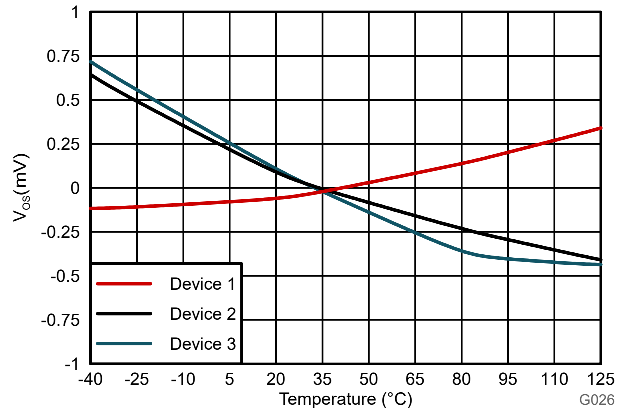


図 6-6. Input Offset Voltage vs Temperature

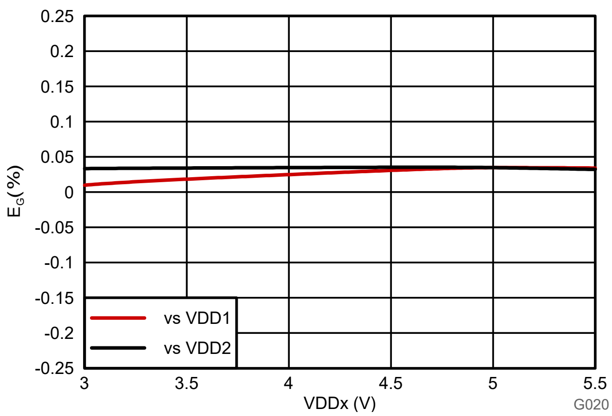


図 6-7. Gain Error vs Supply Voltage

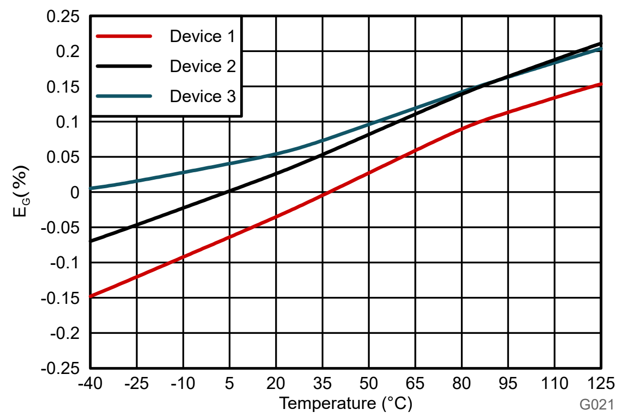


図 6-8. Gain Error vs Temperature

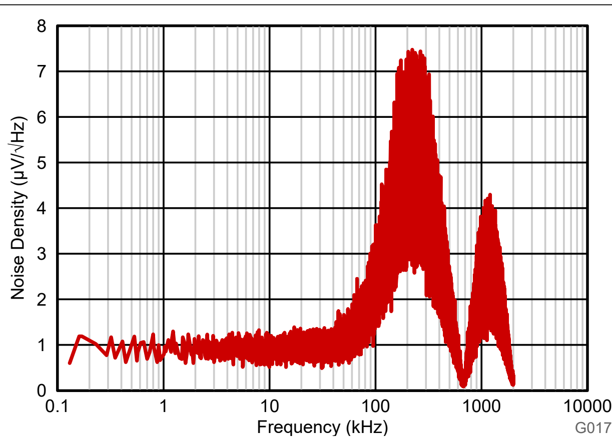


図 6-9. Input-Referred Noise Density vs Frequency

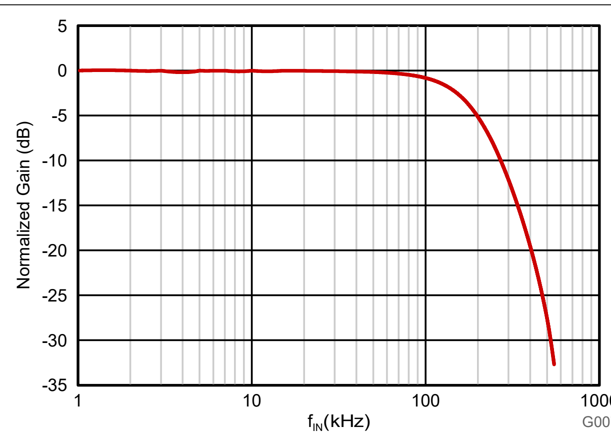


図 6-10. Normalized Gain vs Input Frequency

6.17 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SNSN = GND1, REFIN = GND2, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

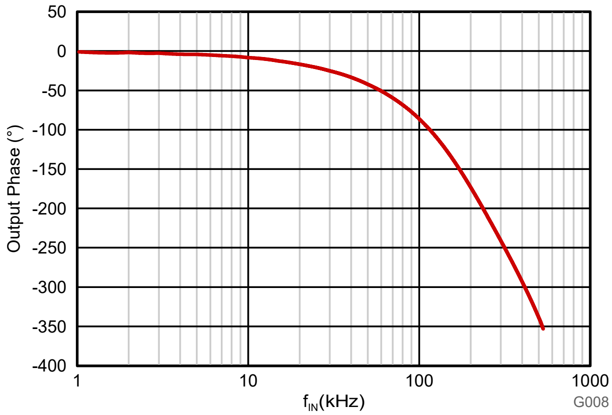


図 6-11. Output Phase vs Input Frequency

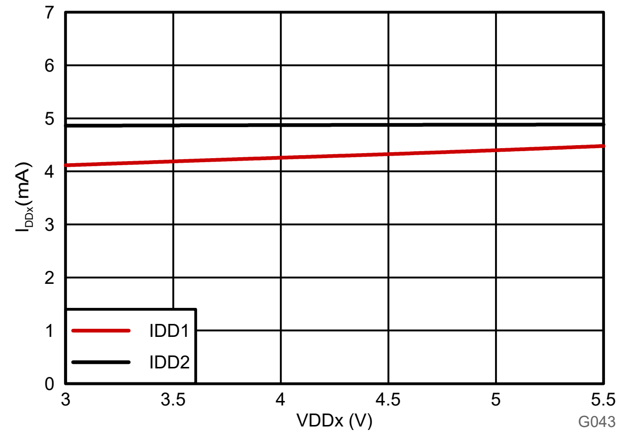


図 6-12. Supply Current vs Supply Voltage

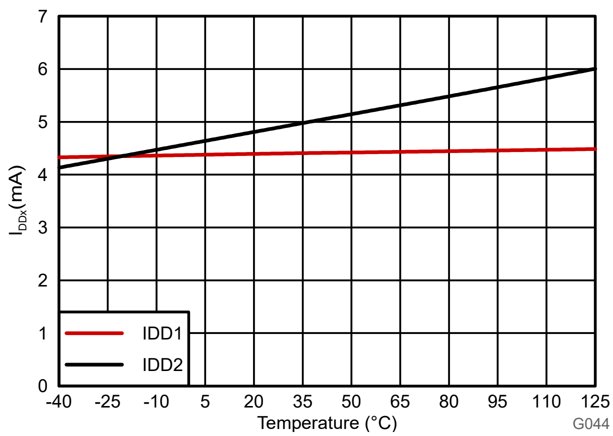


図 6-13. Supply Current vs Temperature

7 Detailed Description

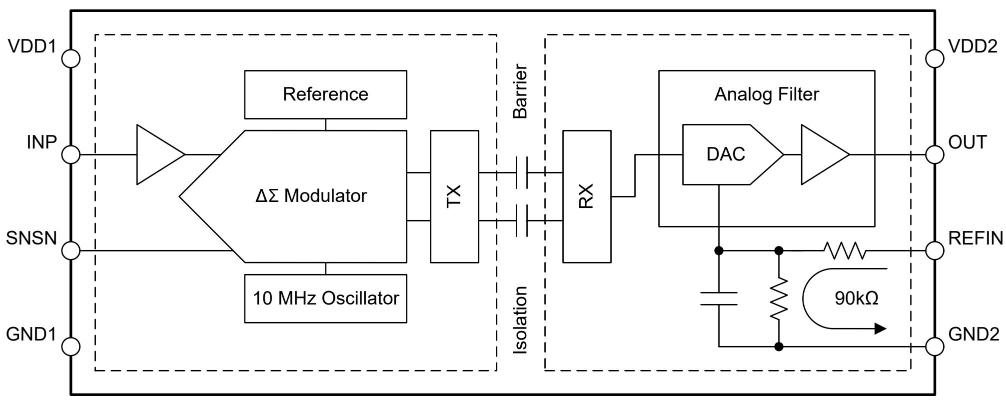
7.1 Overview

The AMC0x11S is a precision, galvanically isolated amplifier with a 2.25V、高インピーダンス入力、固定ゲイン、シングルエンド出力. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high side from the low side.

On the low-side, the received bitstream is processed by an analog filter that outputs a GND2-referenced, single-ended signal at the OUT pin. This single-ended output signal is proportional to the input signal. The output voltage at 0V input is set by the voltage applied to the REFIN pin.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation used in the AMC0x11S transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The high-impedance input buffer on the INP pin feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear full-scale range (V_{FSR}). V_{FSR} is specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC0x11S uses an on-off keying (OOK) modulation scheme, as shown in 図 7-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) as illustrated in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0x11S is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the analog filter. The AMC0x11S transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

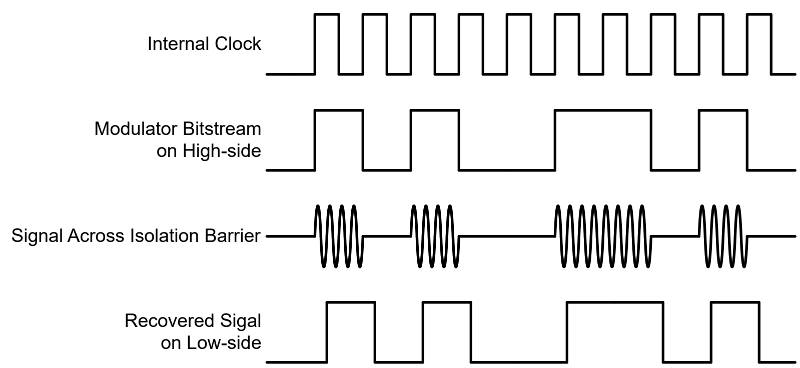


図 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC0x11S provides a single-ended analog output voltage proportional to the input voltage. The output is referred to GND2 and is galvanically isolated from the input of the device. The output is designed to connect directly to the input of an ADC.

The output buffer requires a minimum headroom of 250mV for linear operation. Therefore, with REFIN shorted to GND2, the device shows non-linear behavior for input voltages near 0V. To extend the linear input range to 0V, connect a reference voltage to the REFIN pin that is ≥250mV. The voltage applied to the REFIN pin is added to the output voltage as an offset and provides headroom for the output buffer. The output voltage of the AMC0x11S is equal to:

$$V_{OUT} = V_{IN} + V_{REFIN} = (V_{INP} - V_{SNSN}) + V_{REFIN} \quad (1)$$

Connect the REFIN pin to GND2 if no offset is required. 図 7-2 shows the input-to-output transfer characteristic of the device.

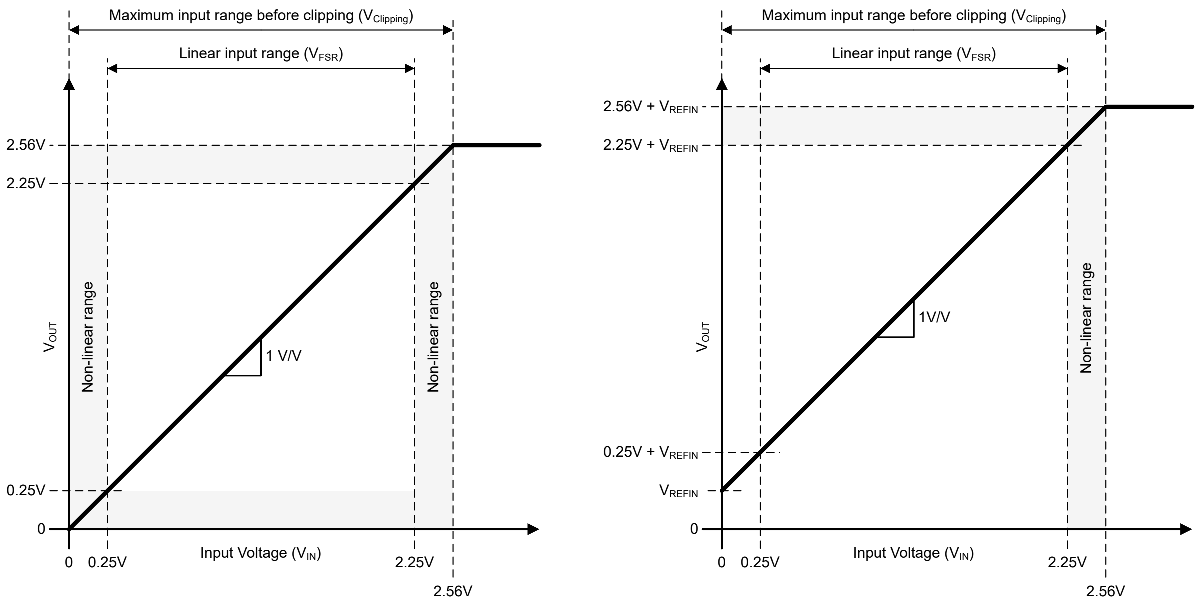


図 7-2. Input to Output Transfer Curve of the AMC0x11S
Left: REFIN shorted to GND2. Right: V_{REFIN} = 250mV

7.4 Reference Input

The voltage applied to the REFIN pin is added to the output voltage as an offset as described in the *Analog Output* section. In a typical application, REFIN is either shorted to GND2 or biased at ≥250mV.

The output buffer is linear in the range of 250mV < V_{OUT} < (VDD2 – 250mV). For linear operation, bias the REFIN pin such that:

$$V_{REFIN} \geq 250mV \quad (2)$$

and

$$V_{REFIN} + V_{FSR, MAX} \leq VDD2 - 250mV \quad (3)$$

7.5 Device Functional Modes

The AMC0x11S operates in one of the following states:

- OFF-state: The low-side supply (VDD2) is below the $VDD2_{UV}$ threshold. The device is not responsive. OUT はハイ インピーダンス状態。内部では、OUT は ESD 保護ダイオードによって VDD2 および GND2 にクランプされます。
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within the *Recommended Operating Conditions* section. The high-side supply (VDD1) is below the $VDD1_{UV}$ threshold. OUT ピンは V_{REFIN} に駆動されます (REFIN が GND2 に短絡している場合は 0V)。
- Analog input overrange (positive full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is above the maximum clipping voltage $V_{Clipping, MAX}$. 本デバイスは OUT ピンに $V_{Clipping}$ + V_{REFIN} を出力します。
- Analog input underrange (negative full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is below the minimum clipping voltage $V_{Clipping, MIN}$. OUT ピンは V_{REFIN} に駆動されます (REFIN が GND2 に短絡している場合は 0V)。
- Normal operation: VDD1, VDD2, and V_{IN} are within the recommended operating conditions. 本デバイスは、入力電圧に比例する電圧を出力します。

表 7-1 lists the operating modes.

表 7-1. Device Operational Modes

OPERATING CONDITION	VDD1	VDD2	V_{IN}	DEVICE RESPONSE
OFF	Don't care	VDD2 < $VDD2_{UV}$	Don't care	OUT はハイ インピーダンス状態。内部では、OUT は ESD 保護ダイオードによって VDD2 および GND2 にクランプされます。
Missing high-side supply	VDD1 < $VDD1_{UV}$	Valid(1)	Don't care	OUT ピンは V_{REFIN} に駆動されます (REFIN が GND2 に短絡している場合は 0V)。
Input overrange	Valid(1)	Valid(1)	$V_{IN} > V_{Clipping, MAX}$	本デバイスは OUT ピンに $V_{Clipping}$ + V_{REFIN} を出力します。
Input underrange	Valid(1)	Valid(1)	$V_{IN} < V_{Clipping, MIN}$	OUT ピンは V_{REFIN} に駆動されます (REFIN が GND2 に短絡している場合は 0V)。
Normal operation	Valid(1)	Valid(1)	Valid(1)	本デバイスは、入力電圧に比例する電圧を出力します。

(1) "Valid" denotes within the recommended operating conditions.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Industrial power systems such as motor drives are divided into two or more voltage domains that are galvanically isolated from each other. For example, the high-voltage domain includes the AC grid, DC-link, and power stage for driving the motor. The low-voltage includes the system controller and human interface. The controller must measure the value of the DC-Link voltage while remaining galvanically isolated from the high-voltage side for safety reasons. With the high-impedance input and galvanically isolated output, the AMC0x11S enables this measurement.

8.2 Typical Application

図 8-1 illustrates a simplified schematic of an AC inverter for a 3-phase motor drive. The AMC0x11S device is used for DC-link voltage sensing. In the power domain, the DC-link voltage is divided down to a 2V level across the bottom resistor (RSNS) of a high-impedance resistive divider. The voltage across RSNS is sensed by the AMC0x11S. The low-side gate driver supply is regulated to a 5V level to power the high-voltage side of the AMC0x11S. In the signal domain, on the opposite side of the isolation barrier, the AMC0x11S outputs a voltage proportional to the DC-link voltage.

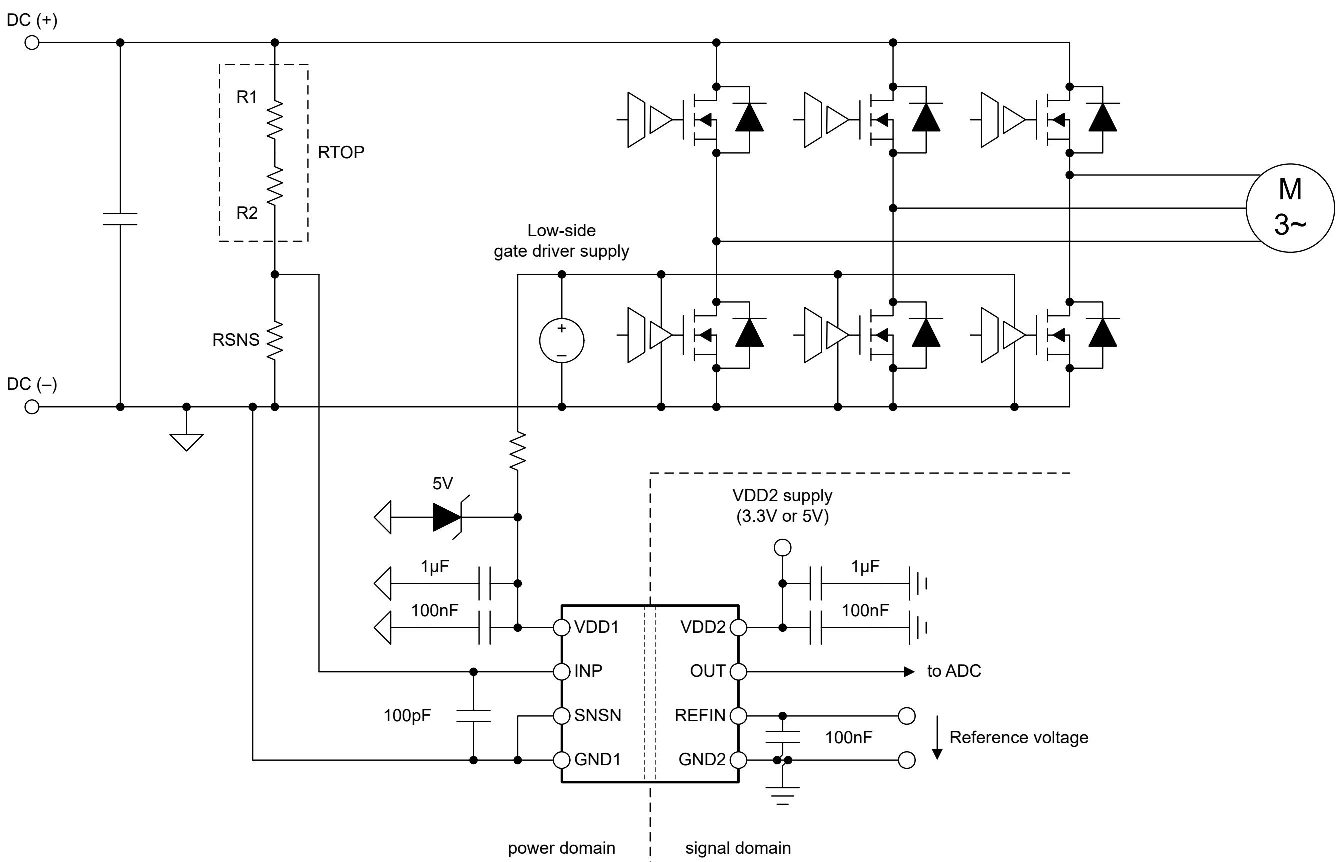


図 8-1. Using the AMC0x11S in a Typical Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
DC-link voltage	450V (maximum)
High-side supply voltage	5V
Low-side supply voltage	3.3V
Maximum resistor operating voltage	125V
Voltage drop across the sense resistor (RSNS) for a linear response	2.25V (maximum)
Current through the resistive divider, I_{CROSS}	200µA (maximum)

8.2.2 Detailed Design Procedure

The 200µA cross-current requirement at the maximum DC-link voltage (450V) determines that the total impedance of the resistive divider is 2.25MΩ. The impedance of the resistive divider is dominated by the top portion (shown exemplary as R1 and R2 in 図 8-1) and the voltage drop across RSNS can be neglected for a moment. The maximum allowed voltage drop per unit resistor is specified as 125V; therefore, the minimum number of unit resistors in the top portion of the resistive divider is 450V / 125V ≅ 4. The calculated unit value is 2.25MΩ / 4 = 563kΩ and the next closest value from the E96 series is 562kΩ. The sense resistor (RSNS) is sized such that the voltage drop across the resistor at the maximum DC-link voltage (450V) equals the linear full-scale range input voltage (V_{FSR}) of the AMC0x11S, which is 2.25V. This resistance is calculated as RSNS = V_{FSR} / ($V_{DC\text{-link, MAX}}$ – V_{FSR}) × R_{TOP}, where R_{TOP} is the total value of the top resistor string (4 × 562kΩ = 2.248MΩ). RSNS is calculated as 11.3kΩ and matches a value from the E96 series.

表 8-2 summarizes the design of the resistive divider.

表 8-2. Resistor Value Examples

PARAMETER	VALUE
Unit resistor value, R_{TOP}	562kΩ
Number of unit resistors in R_{TOP}	4
Sense resistor value, RSNS	11.3kΩ
Total resistance value (R_{TOP} + RSNS)	2.251MΩ
Resulting current through resistive divider, I_{CROSS}	199.2µA
Resulting full-scale voltage drop across sense resistor RSNS	2.251V
Peak power dissipated in R_{TOP} unit resistor	22.3mW
Total peak power dissipated in resistive divider	89.6mW

8.2.2.1 Input Filter Design

Place a RC filter in front of the device to improve signal-to-noise performance of the signal path. Input noise with a frequency close to the ΔΣ modulator sampling frequency (typically 10MHz) is folded back into the low-frequency range by the modulator. The purpose of the RC filter is to attenuate high-frequency noise below the desired noise level of the measurement. In practice, a cutoff frequency that is two orders of magnitude lower than the modulator frequency yields good results.

Most voltage-sensing applications use high-impedance resistive dividers in front of the isolated modulator to scale down the input voltage. In this case, a single capacitor, as shown in 図 8-2, is sufficient to filter the input signal. For (R1 + R2) >> RSNS, the cut-off frequency of the input filter is 1 / (2 x π x RSNS x C5). For example, RSNS =10kΩ and C5 = 100pF results in a cutoff frequency of 160kHz.

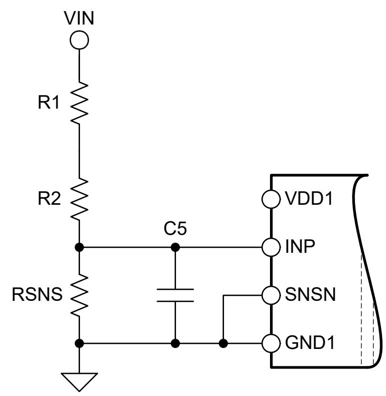


図 8-2. Input Filter

8.2.2.2 Connecting the REFIN pin

The reference input has an internal, 90kOhm impedance connected to GND2. This impedance needs to be considered when driving the REFIN pin from a high-impedance source. Connect a 100nF capacitor from REFIN to GND2 to filter out high-frequency noise at the reference input. 図 8-3 shows different options for connecting the REFIN pin.

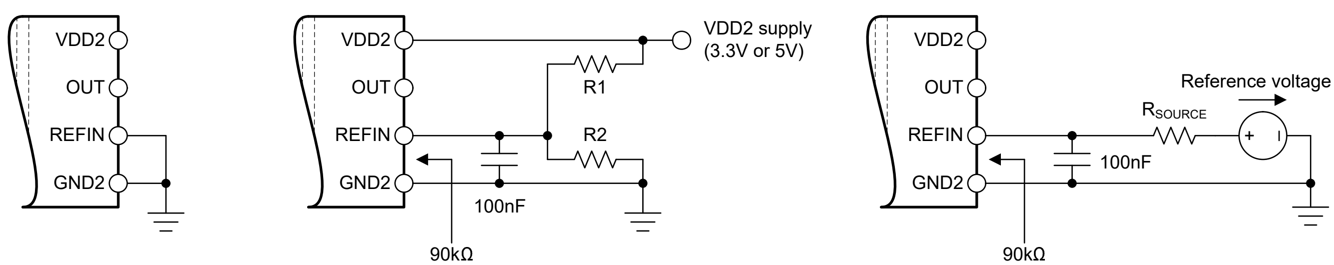


図 8-3. Connecting the REFIN pin

In the first example, REFIN is shorted to GND2 and the resulting reference voltage is 0V. In the second example, V_{REFIN} is derived from VDD2 through a resistive divider. In the third example, an external voltage source drives the reference input pin.

8.2.3 Application Curve

図 8-4 shows the typical full-scale step response of the AMC0x11S.

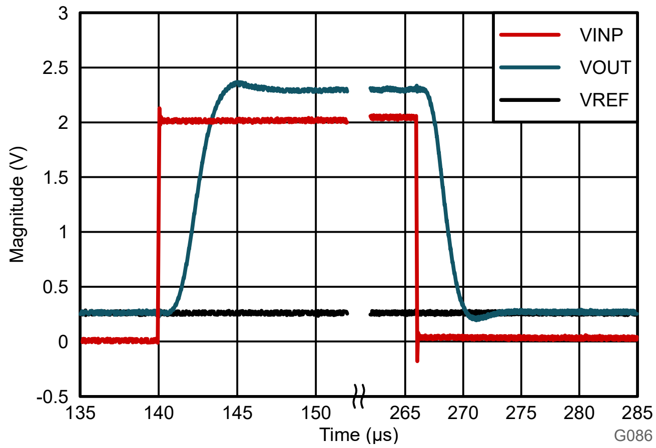


図 8-4. Step Response of the AMC0x11S

8.3 Best Design Practices

Do not leave the analog input (INP pin) of the AMC0x11S unconnected (floating) when the device is powered up. If the device input is left floating, the output of the device is not valid.

Do not connect protection diodes to the input (INP pin) of the AMC0x11S. Diode leakage current potentially introduces significant measurement error especially at high temperatures. The input pin is protected against high voltages by the ESD protection circuit and the high impedance of the external resistive divider.

8.4 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0x11S is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC0x11S does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. 図 8-5 shows a decoupling diagram for the AMC0x11S.

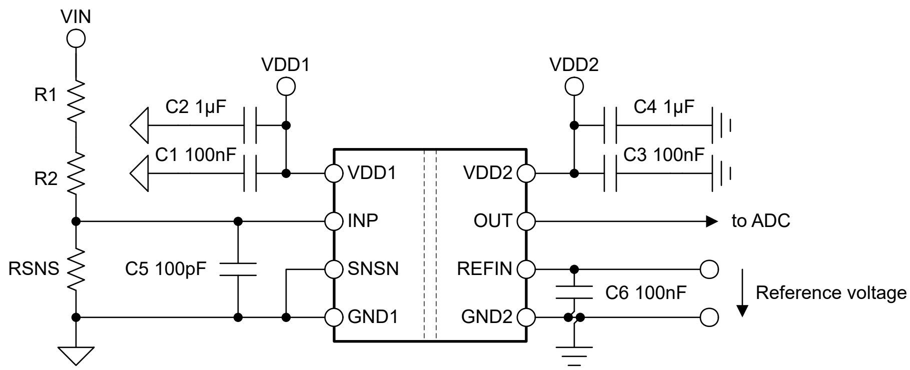


図 8-5. Decoupling of the AMC0x11S

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

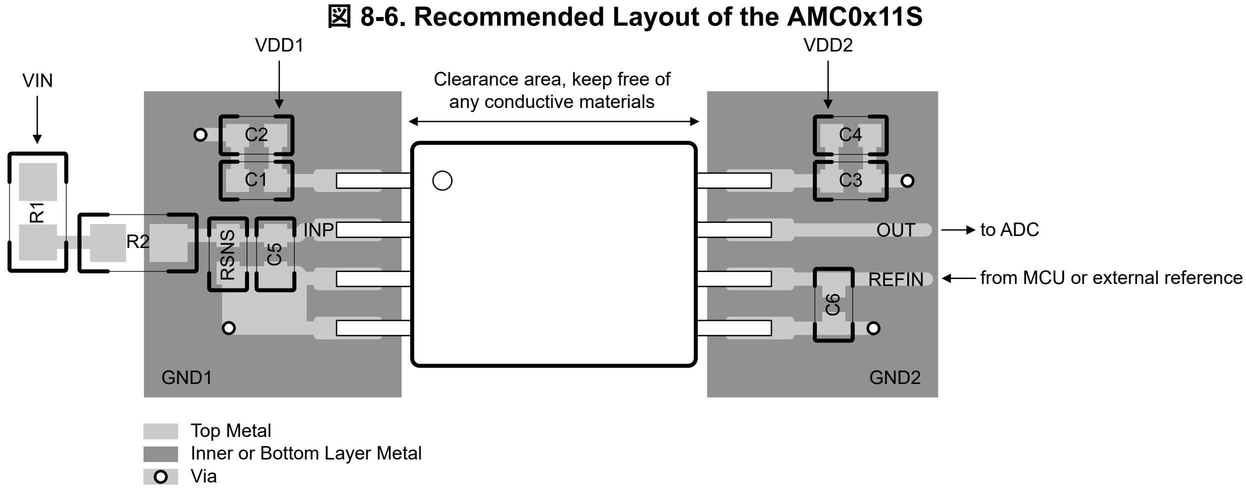
8.5 Layout

8.5.1 Layout Guidelines

The *Layout* section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0x11S supply pins). This example also depicts the placement of other components required by the device.

8.5.2 Layout Example

図 8-6. Recommended Layout of the AMC0x11S



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC0311SDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC0311S
AMC0311SDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC0311S
AMC0311SDWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

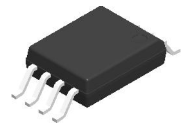
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

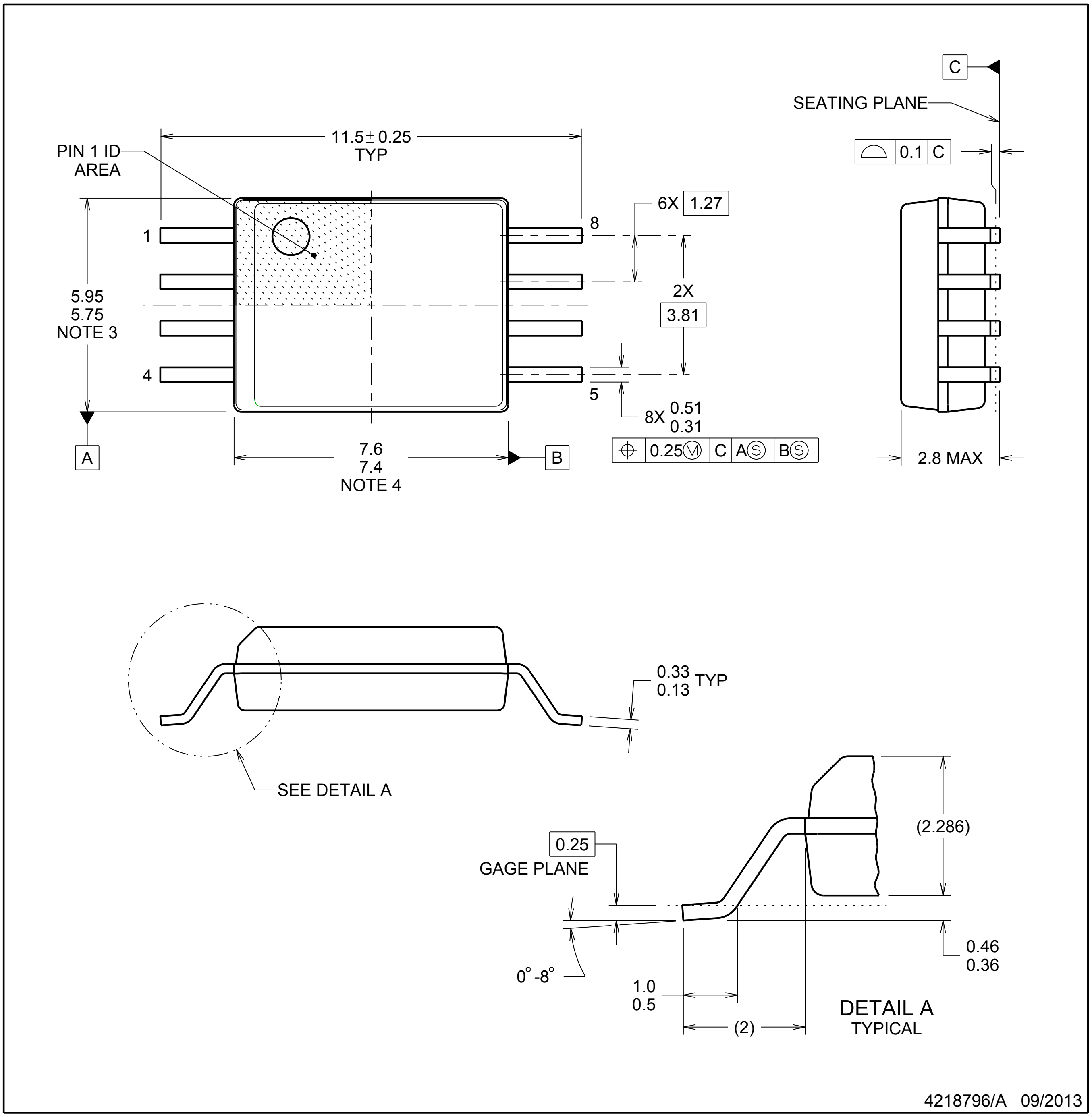
OTHER QUALIFIED VERSIONS OF AMC0311S :

- Automotive : AMC0311S-Q1

NOTE: Qualified Version Definitions:

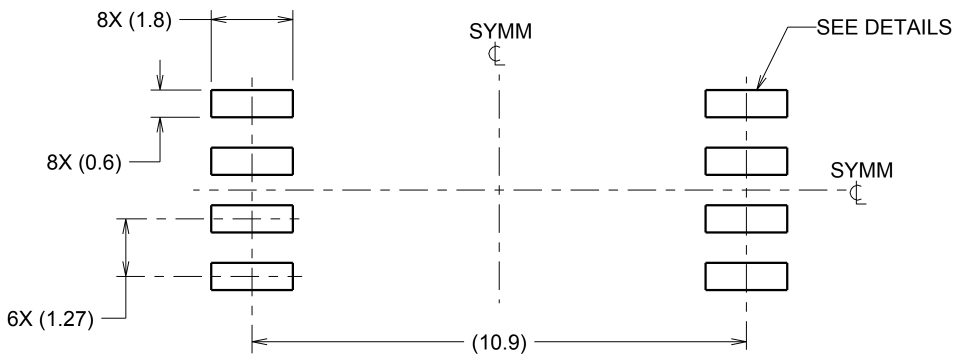
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



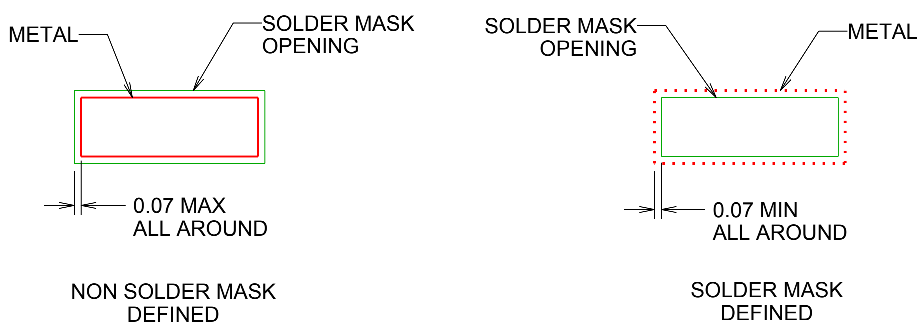


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

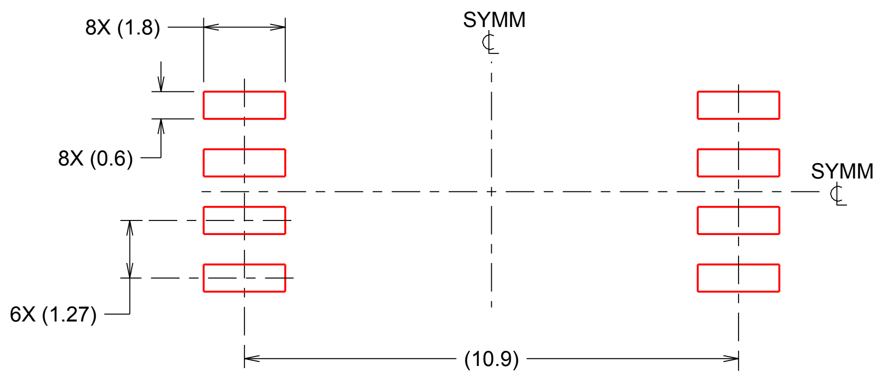


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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