

## AM64x Sitara™ プロセッサ

### 1 特長

#### プロセッサ コア:

- 最高 1.0GHz、1 つのデュアル 64 ビット Arm® Cortex®-A53 マイクロプロセッサ サブシステム
  - SECEDED ECC 付き 256KB L2 共有キャッシュを搭載したデュアル コア Cortex-A53 クラスタ
  - 各 A53 コアには、SECEDED ECC を備えた 32KB L1 D キャッシュおよびパリティ保護を備えた 32KB L1 I キャッシュを搭載
- リアルタイム処理向けに統合された、最高 800MHz、最大 2 つのデュアル コア Arm® Cortex®-R5F MCU サブシステム
  - デュアル コア Arm® Cortex®-R5F により、デュアル コアおよびシングル コア モードをサポート
  - 各 R5F コアごとに 32KB I キャッシュ、32KB D キャッシュ、64KB TCM を搭載、すべてのメモリに SECEDED ECC 付きで合計 256KB の TCM 搭載
- 最高 400MHz、1 つのシングル コア Arm® Cortex®-M4F MCU
  - 256KB の SRAM (SECEDED ECC 付き)

#### 産業用サブシステム:

- 2 つのギガビット産業用通信サブシステム (PRU\_ICSSG)
  - Profinet IRT、Profinet RT、Ethernet/IP、EtherCAT、Time-Sensitive Networking (TSN)、その他をサポート
  - 10/100Mb PRU\_ICSS と下位互換
  - 各 PRU\_ICSSG は以下を内蔵:
    - に 2 つのイーサネット ポートを搭載
      - MII (10/100)
      - RGMII (10/100/1000)
    - 各 PRU\_ICSSG に 6 つの PRU RISC コアを搭載、各コアに以下を内蔵:
      - 命令 RAM (ECC 付き)
      - ブロードサイド RAM
      - アキュムレータ付き乗算器 (MAC)
      - CRC16/32 ハードウェア アクセラレータ
      - バイト スワップによるビッグ / リトル エンディアン変換
      - SUM32 ハードウェア アクセラレータによる UDP チェックサム
      - タスク マネージャによるプリエンブションのサポート
  - 3 つのデータ RAM (ECC 付き)

- 8 バンクの 30 × 32 ビットレジスタ スクラッチパッド メモリ
- 割り込みコントローラとタスク マネージャ
- 2 つの 64 ビット産業用イーサネット ペリフェラル (IEP) によるタイム スタンプ機能とその他の時間同期機能
- 18 個のシグマ デルタ フィルタ
  - 短絡ロジック
  - 過電流ロジック
- 6 つのマルチプロトコル位置エンコーダ インターフェイス
- 1 つの拡張キャプチャ モジュール (ECAP)
- 16550 互換 UART、専用の 192MHz クロックによる 12Mbps PROFIBUS のサポート

#### メモリ サブシステム:

- 最大 2MB のオンチップ RAM (OCSRAM) (SECEDED ECC 付き):
  - 256KB 単位で小さいバンクに分割し、最大 8 つの独立したメモリ バンクを構成可能
  - ソフトウェア タスクの分割を容易にするため、各メモリ バンクを 1 つのコアに割り当て可能
- DDR サブシステム (DDRSS)
  - LPDDR4、DDR4 メモリ タイプをサポート
  - インライン ECC 付きの 16 ビット データ バス
  - 最大 1600MT/s の速度をサポート
- 1 つの汎用メモリ コントローラ (GPMC)
  - 133MHz クロックの 16 ビット パラレル バスまたは
  - 100MHz クロックの 32 ビット パラレル バス
  - エラー特定モジュール (ELM) のサポート

#### システム オン チップ (SoC) サービス:

- デバイス管理セキュリティ コントローラ (DMSC-L)
  - 集中 SoC システム コントローラ
  - 初期ブート、セキュリティ、クロック / リセット / 電源管理を含むシステム サービスを管理
  - メッセージ マネージャを介したさまざまな処理ユニットとの通信
  - シンプルなインターフェイスにより未使用ペリフェラルを最適化
- データ移動サブシステム (DMSS: Data Movement Subsystem)
  - ブロック コピー DMA (BCDMA)
  - パケット DMA (PKTDMA)
  - セキュア プロキシ (SEC\_PROXY)
  - リング アクセラレータ (RINGACC)

#### セキュリティ:



- セキュア ブート対応
  - ハードウェアで強化された RoT (Root-of-Trust: 信頼の基点)
  - バックアップ キーによる RoT の切り替えをサポート
  - テイクオーバー保護、IP 保護、ロールバック禁止保護のサポート
- 信頼できる実行環境 (TEE) に対応
  - Arm TrustZone® をベースとする TEE
  - セキュアなウォッチドッグ / タイマ / IPC
  - 分離用の広範なファイアウォール サポート
  - セキュアなストレージのサポート
  - リプレイ保護メモリ ブロック (RPMB) のサポート
- セキュリティ コプロセッサ (DMSC-L) によりキーおよびセキュリティ管理を実現、専用のデバイス レベル インターコネクトによりセキュリティを確保
- 暗号化アクセラレーションに対応
  - 受信データ ストリームに基づいてキーマテリアルを自動的に切り替えできるセッション認識暗号化エンジン
    - 暗号化コアをサポート
  - AES - 128/192/256 ビットのキー サイズ
  - SHA2 - 224/256/384/512 ビットのキー サイズ
  - DRBG と真性乱数発生器
  - セキュア ブート対応のため PKA (公開鍵アクセラレータ) により RSA/ECC 処理を支援
- デバッグのセキュリティ
  - ソフトウェア制御によるセキュアなデバッグ アクセス
  - セキュリティ対応のデバッグ

#### 高速インターフェイス:

- 以下をサポートする 1 つの統合型イーサネット スイッチ (CPSW3G):
  - 最大 2 つのイーサネット ポート
    - RMII (10/100)
    - RGMII (10/100/1000)
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) と 802.1AS PTP
  - Clause 45 MDIO PHY 管理
  - 省電力イーサネット (802.3az)
- 1 つの PCI-Express® Gen2 コントローラ (PCIE)
  - Gen2 動作をサポート
  - シングル レーン動作をサポート
- 1 つの USB 3.1 デュアルロール デバイス (DRD) サブシステム (USBSS)
  - USB ホスト、USB デバイス、または USB デュアルロール デバイスとして構成可能なポート
  - USB デバイス: 高速 (480Mbps)、フルスピード (12Mbps)

- USB ホスト: SuperSpeed Gen 1 (5Gbps)、高速 (480Mbps)、フルスピード (12Mbps)、低速 (1.5Mbps)

#### 一般的な接続機能:

- 6 つの I2C (Inter-Integrated Circuit) ポート
- 9 つの構成可能な UART (Universal Asynchronous Receiver/Transmitter) モジュール
- オクタル SPI (OSPI) フラッシュ インターフェイスまたは 1 つのクワッド SPI (QSPI) として構成可能な 1 つのフラッシュ サブシステム (FSS)
- 1 つの 12 ビット アナログ/デジタル コンバータ (ADC)
  - 最大 4MSPS
  - 8 つの多重アナログ入力
- 7 つのマルチチャネル シリアル ペリフェラル インターフェイス (MCSPI) コントローラ
- 6 つの高速シリアル インターフェイス レシーバ (FSI\_RX) コア
- 2 つの高速シリアル インターフェイス トランスミッタ (FSI\_TX) コア
- 3 つの汎用 I/O (GPIO) モジュール

#### 制御インターフェイス:

- 9 つの拡張パルス幅変調器 (EPWM) モジュール
- 3 つの拡張キャプチャ (ECAP) モジュール
- 3 つの拡張直交エンコーダ パルス (EQEP) モジュール
- CAN-FD をフルサポートする 2 つのモジュラー コントローラ エリア ネットワーク (MCAN) モジュール

#### メディアおよびデータ ストレージ:

- 2 つのマルチメディア カード / セキュア デジタル (MMC/SD/SDIO) インターフェイス
  - 1 つの 4 ビット インターフェイス (SD/SDIO 用)
  - 1 つの 8 ビット インターフェイス (eMMC 用)
  - 高速カードの電圧切り替え (3.3V、1.8V) のための内蔵アナログ スイッチ

#### パワー マネージメント:

- シンプルな電源シーケンスで
- 内蔵 SDIO LDO により SD インターフェイスでの自動電圧遷移に対応
- 内蔵の電圧スーパーバイザによる過電圧 / 低電圧状態の安全監視
- 内蔵の電源グリッチ検出器により高速電源過渡を検出

#### 機能安全:

- [機能安全準拠](#)
  - 機能安全アプリケーション向けに開発

- IEC 61508 機能安全システム設計を支援するドキュメントを提供
- SIL 3 までの決定論的対応能力
- SIL 2 までのハードウェア整合性
- 安全関連の認証
  - TÜV SÜD による IEC 61508 認定
- 機能安全関連の特徴
  - 演算上特に重要なメモリの ECC またはパリティ
  - 一部の内部バス インターコネクットの ECC とパリティ
  - CPU とオンチップ RAM の内蔵セルフテスト (BIST)
  - エラー ピン付きのエラー シグナリング モジュール (ESM)
  - ランタイム安全診断、電圧 / 温度 / クロックの監視、ウィンドウ付きウォッチドッグ タイマ、CRC エンジンによるメモリ整合性チェック
  - FFI (Freedom From Interference) 機能により SoC 全体から分離できる、専用 MCU ドメイン メモリ、インターフェイス、M4F コア

- 独立したインターコネク
- ファイアウォールとタイムアウト ガスケット
- 専用 PLL
- 専用 I/O 電源
- 独立したリセット

#### SoC アーキテクチャ:

- UART、I2C、OSPI/QSPI フラッシュ、SPI フラッシュ、パラレル NOR フラッシュ、パラレル NAND フラッシュ、SD、eMMC、USB、PCIe、イーサネット インターフェイスからの 1 次ブートをサポート
- 16nm FinFET テクノロジ
- 17.2mm × 17.2mm、0.8mm ピッチ、441 ピン BGA パッケージ

## 2 アプリケーション

- プログラマブル ロジック コントローラ (PLC)
- モーター ドライブ
- リモート I/O
- 産業用ロボット
- 状況監視ゲートウェイ

### 3 概要

AM64x は、Sitara™ 産業用グレード ファミリを拡張したヘテロジニアス Arm® プロセッサです。AM64x は、リアルタイムの処理とアプリケーション処理を伴う通信との独自の組み合わせが求められる、モーター ドライブやプログラマブル ロジック コントローラ (PLC) のような産業用アプリケーション向けに構築されています。AM64x は、Sitara デバイスのギガビット TSN 対応 PRU-ICSSG を 2 インスタンス搭載し、さらに最大 2 つの Arm® Cortex®-A53 コア、最大 4 つの Cortex-R5F MCU、1 つの Cortex-M4F MCU を搭載しています。

AM64x は、高性能 R5F、密結合メモリ バンク、構成可能な SRAM パーティショニング、SoC 内外の高速データ移動を可能にする対ペリフェラル専用の低レイテンシ パスを使用して、リアルタイム性能を発揮するように設計されています。この決定論的アーキテクチャは、サーボ ドライブに見られる厳密な制御ループを AM64x が処理することを可能にし、AM64x のペリフェラル (例: FSI、GPMC、PWM、シグマ デルタ デシメーション フィルタ、アブソリュート エンコーダ インターフェイス) は、これらのシステムに見られる各種アーキテクチャを実現するのに役立ちます。

Cortex-A53 は、Linux アプリケーションに必要な強力なコンピューティング エレメントを提供します。Linux およびリアルタイム (RT) Linux は、TI のプロセッサ SDK Linux を通じて提供されており、最新の長期サポート (LTS) Linux カーネル、ブートローダ、Yocto ファイル システムに毎年更新されます。AM64x は、構成可能なメモリ パーティション分割により、Linux アプリケーションとリアルタイム ストリーム間の分離を実現することで、Linux の世界とリアルタイムの世界を橋渡しします。Cortex-A53 は 厳密に Linux 用 DDR から動作するように割り当てることができます。また、内蔵 SRAM は、さまざまなサイズに分割して、Cortex-R5F がまとめて使用したり、または個別に使用したりできます。

AM64x は、EtherCAT サブデバイス、PROFINET デバイス、EtherNet/IP アダプタ、IO-Link マスタのためのフル プロトコル スタックなどフレキシブルな産業用通信機能を提供します。PRU\_ICSSG は、ギガビットおよび TSN ベースのプロトコルの機能を提供します。また、PRU-ICSSG を使うと、シグマ デルタ デシメーション フィルタ、アブソリュート エンコーダ インターフェイスなどのインターフェイスも SoC に追加できます。

機能安全のための機能は、内蔵の Cortex-M4F と専用ペリフェラルによって実現されます。このペリフェラルは、SoC のその他の部分から完全に分離できます。AM64x はセキュア ブートもサポートしています。

#### パッケージ情報

| 部品番号   | パッケージ (1)        | パッケージ サイズ(2)    |
|--------|------------------|-----------------|
| AM6442 | ALV (FCBGA, 441) | 17.2mm × 17.2mm |
| AM6441 | ALV (FCBGA, 441) | 17.2mm × 17.2mm |
| AM6422 | ALV (FCBGA, 441) | 17.2mm × 17.2mm |
| AM6421 | ALV (FCBGA, 441) | 17.2mm × 17.2mm |
| AM6412 | ALV (FCBGA, 441) | 17.2mm × 17.2mm |
| AM6411 | ALV (FCBGA, 441) | 17.2mm × 17.2mm |

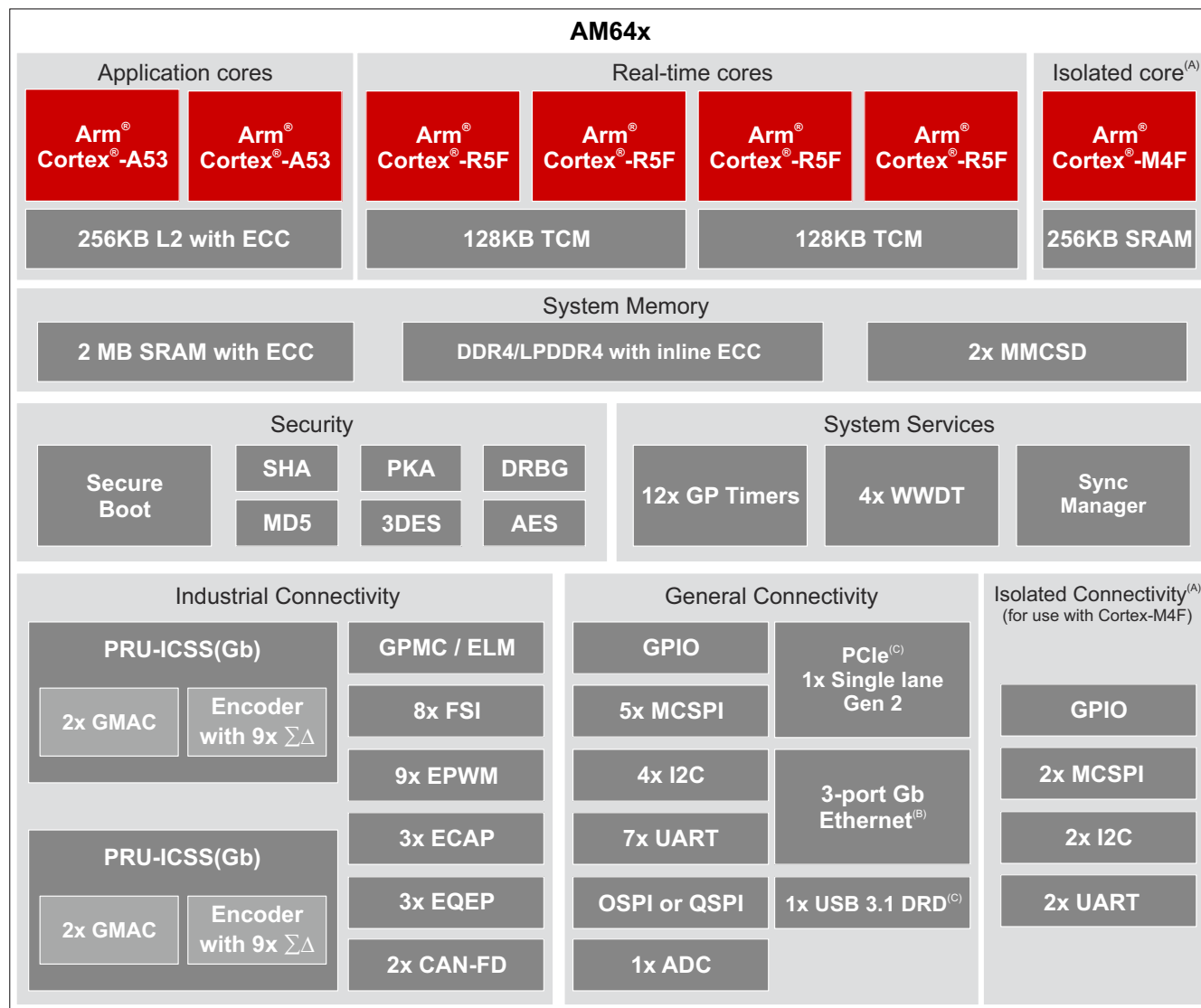
- (1) 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。  
 (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

### 3.1 機能ブロック図

図 1-1 は、デバイスの機能ブロック図です。

#### 注

テキサス・インスツルメンツのソフトウェア開発キット (SDK) が現在サポートしているデバイス機能を理解するには、[Processor-SDK-AM64x](#) にある「ダウンロード」タブ オプションの AM64x ソフトウェア ビルド シートを検索してください。



- A. ペリフェラルと M4F コアの分離は任意の機能です。  
B. ポートの 1 つは内部接続のみで、どのピンにも接続されていません。  
C. USB SuperSpeed と PCIe は共通の SerDes レーンを共有します。したがって、PCIe に SerDes PHY を使用する場合、USB は SuperSpeed 以外のモードに制限されます。

図 3-1. 機能ブロック図

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## 4 Device Comparison

表 4-1 shows a comparison between devices, highlighting the differences.

### 注

Availability of features listed in this table are a function of shared IO pins, where IO signals associated with many of the features are multiplexed to a limited number of pins. The SysConfig tool should be used to assign signal functions to pins. This will provide a better understanding of limitations associated with pin multiplexing.

### 注

To understand what device features are currently supported by TI Software Development Kits (SDKs), search for the *AM64x Software Build Sheet* located in the Downloads tab option provided at [Processor-SDK-AM64x](#).

**表 4-1. Device Comparison**

| FEATURES                                                                                                                                                                                             | REFERENCE NAME | AM6442    | AM6441      | AM6422    | AM6421      | AM6412    | AM6411      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------|-------------|-----------|-------------|-----------|-------------|
| <b>CTRL_MMR_CFG0_JTAG_USER_ID[31:13]<sup>(1)</sup></b><br>Register bit values by device "Features" code (See <a href="#">Nomenclature Description</a> table for more information on device features) |                |           |             |           |             |           |             |
| C:                                                                                                                                                                                                   |                | –         | –           | –         | –           | 0x19403   | 0x19203     |
| D:                                                                                                                                                                                                   |                | 0x19464   | 0x19264     | 0x19424   | 0x19224     | –         | –           |
| E:                                                                                                                                                                                                   |                | 0x19465   | 0x19265     | –         | 0x19225     | –         | –           |
| F:                                                                                                                                                                                                   |                | 0x19466   | 0x19266     | –         | 0x19226     | –         | –           |
| <b>PROCESSORS AND ACCELERATORS</b>                                                                                                                                                                   |                |           |             |           |             |           |             |
| Speed Grades (See 表 6-1)                                                                                                                                                                             |                | S         |             |           |             | S, K      |             |
| Arm Cortex-A53 Microprocessor Subsystem                                                                                                                                                              | Arm A53        | Dual Core | Single Core | Dual Core | Single Core | Dual Core | Single Core |

**表 4-1. Device Comparison (続き)**

| FEATURES                                                                                                      | REFERENCE NAME | AM6442                                                                        | AM6441   | AM6422                                          | AM6421   | AM6412                      | AM6411      |
|---------------------------------------------------------------------------------------------------------------|----------------|-------------------------------------------------------------------------------|----------|-------------------------------------------------|----------|-----------------------------|-------------|
| Arm Cortex-R5F                                                                                                | Arm R5F        | 2 × Dual Core<br>R5FSS0_CORE0<br>R5FSS0_CORE1<br>R5FSS1_CORE0<br>R5FSS1_CORE1 |          | 2 × Single Core<br>R5FSS0_CORE0<br>R5FSS1_CORE0 |          | Single Core<br>R5FSS0_CORE0 |             |
| Arm Cortex-M4F                                                                                                | Arm M4F        | Single Core<br>Functional Safety Optional <sup>(4)</sup>                      |          |                                                 |          |                             | Single Core |
| Device Management Security Controller                                                                         | DMSC-L         | Yes                                                                           |          |                                                 |          |                             |             |
| Crypto Accelerators                                                                                           | Security       | Yes                                                                           |          |                                                 |          |                             |             |
| PROGRAM AND DATA STORAGE                                                                                      |                |                                                                               |          |                                                 |          |                             |             |
| On-Chip Shared Memory (RAM) in MAIN Domain                                                                    | OCSRAM         | 2MB                                                                           |          |                                                 |          |                             |             |
| R5F Tightly Coupled Memory (TCM)                                                                              | TCM            | 4 x 64KB                                                                      |          | 2 x 128KB                                       |          | 1 x 128KB                   |             |
| On-Chip Shared Memory (RAM) in M4F Domain                                                                     | MCU_MSRAM      | 256KB                                                                         |          |                                                 |          |                             |             |
| DDR4/LPDDR4 DDR Subsystem                                                                                     | DDRSS          | Up to 2GB (16-bit data) with inline ECC                                       |          |                                                 |          |                             |             |
| General-Purpose Memory Controller                                                                             | GPMC           | Up to 128MB with ECC                                                          |          |                                                 |          |                             |             |
| PERIPHERALS                                                                                                   |                |                                                                               |          |                                                 |          |                             |             |
| Modular Controller Area Network Interface                                                                     | MCAN           | 2                                                                             |          |                                                 |          |                             |             |
| Full CAN-FD Support <sup>(2)</sup>                                                                            | MCAN           | Optional                                                                      | Optional | No                                              | Optional | No                          | No          |
| General-Purpose I/O                                                                                           | GPIO           | Up to 198                                                                     |          |                                                 |          |                             |             |
| Inter-Integrated Circuit Interface                                                                            | I2C            | 6                                                                             |          |                                                 |          |                             |             |
| Analog-to-Digital Converter                                                                                   | ADC            | 1                                                                             |          |                                                 |          | No                          |             |
| Multichannel Serial Peripheral Interface                                                                      | MCSPI          | 7                                                                             |          |                                                 |          |                             |             |
| Multi-Media Card/ Secure Digital Interface                                                                    | MMCSD0         | eMMC (8-bits)                                                                 |          |                                                 |          |                             |             |
|                                                                                                               | MMCSD1         | SD/SDIO (4-bits)                                                              |          |                                                 |          |                             |             |
| Fast Serial Interface                                                                                         | FSI_TX         | 2                                                                             |          |                                                 |          |                             |             |
|                                                                                                               | FSI_RX         | 6                                                                             |          |                                                 |          |                             |             |
| Flash Subsystem (FSS) <sup>(3)</sup>                                                                          | OSPI0/QSPI0    | Yes                                                                           |          |                                                 |          |                             |             |
| PCI Express Port with Integrated SerDes PHY                                                                   | PCIE0          | Single Lane <sup>(7)</sup>                                                    |          |                                                 |          |                             |             |
| Programmable Real-Time Unit Subsystem <sup>(5)</sup>                                                          | PRU_ICSSG      | 2                                                                             |          |                                                 |          |                             |             |
| PRU_ICSSG Industrial Communication Support <sup>(6)</sup>                                                     | PRU_ICSSG      | Optional                                                                      | Optional | Yes                                             | Optional | No                          | No          |
| Gigabit Ethernet Interface                                                                                    | CPSW3G         | Yes                                                                           |          |                                                 |          |                             |             |
| General-Purpose Timers                                                                                        | TIMER          | 16 (4 in MCU Channel)                                                         |          |                                                 |          |                             |             |
| Enhanced Pulse-Width Modulator Module                                                                         | EPWM           | 9                                                                             |          |                                                 |          |                             |             |
| Enhanced Capture Module                                                                                       | ECAP           | 3                                                                             |          |                                                 |          |                             |             |
| Enhanced Quadrature Encoder Pulse Module                                                                      | EQEP           | 3                                                                             |          |                                                 |          |                             |             |
| Universal Asynchronous Receiver and Transmitter                                                               | UART           | 9                                                                             |          |                                                 |          |                             |             |
| Universal Serial Bus (USB3.1 Gen1) SuperSpeed Dual-Role-Device (DRD) Ports with SS SerDes PHY and USB 2.0 PHY | USB0           | Yes <sup>(7)</sup>                                                            |          |                                                 |          |                             |             |

- (1) For more details about the CTRL\_MMR\_CFG0\_JTAG\_USER\_ID register and DEVICE\_ID bit field, see the device TRM.
- (2) Full CAN-FD Support is available when selecting an orderable part number that includes a feature code of E or F. Refer to [Nomenclature Description](#) table for the definition of feature codes.
- (3) One flash interface, configured as OSPI0 or QSPI0.
- (4) Functional Safety is available when selecting an orderable part number that includes a feature code of F. Refer to [Nomenclature Description](#) table for the definition of feature codes.
- (5) Orderable part numbers with a feature code of C support using PRU\_ICSSG for use cases other than industrial communication. Refer to [Nomenclature Description](#) table for the definition of feature codes.
- (6) PRU\_ICSSG industrial communication includes Ethernet networking (MII/RGMII, MDIO), Sigma-Delta (SD) decimation, and three channel peripheral interface (EnDat 2.2 and BiSS). PRU\_ICSSG industrial communication support is available when selecting an orderable part number that includes a feature code of D, E, or F. Refer to [Nomenclature Description](#) table for the definition of feature codes.

- (7) USB SuperSpeed and PCIe share a common SerDes PHY. Therefore, USB will be limited to non-SuperSpeed modes when using the SerDes PHY for PCIe.

## 4.1 Related Products

**Sitara™ processors** Broad family of scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity and unified software support – perfect for sensors to servers. Sitara processors have the reliability needed for use in industrial applications.

**AM64x Sitara™ processors** AM6x processors enable gigabit industrial Ethernet networks, robust operation with extensive ECC on memories, and enhanced security features.

**Sitara™ processors - Applications** Sitara™ processors provide scalable solutions for a wide range of applications from HMI and gateways to more complex equipment such as drives and substation automation equipment. Sitara processors also offer multi-protocol support for industrial communication protocols such as EtherCAT®, Ethernet/IP, and Profinet.

**Sitara™ processors - Reference designs** TI provides many reference designs containing 'building block' solutions to enable customers to rapidly develop their own unique products and solutions.

**Companion Products for AM64x** Review products that are frequently purchased or used in conjunction with this product to complete your design.

## 5 Terminal Configuration and Functions

### 5.1 Pin Diagrams

注

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

図 5-1 shows the ball locations for the 441-ball flip chip ball grid array (FCBGA) package to quickly locate signal names and ball grid numbering. This figure is used in conjunction with 表 5-1 through 表 5-80 (*Pin Attributes table and all Signal Descriptions tables, including the Connectivity Requirements table*).

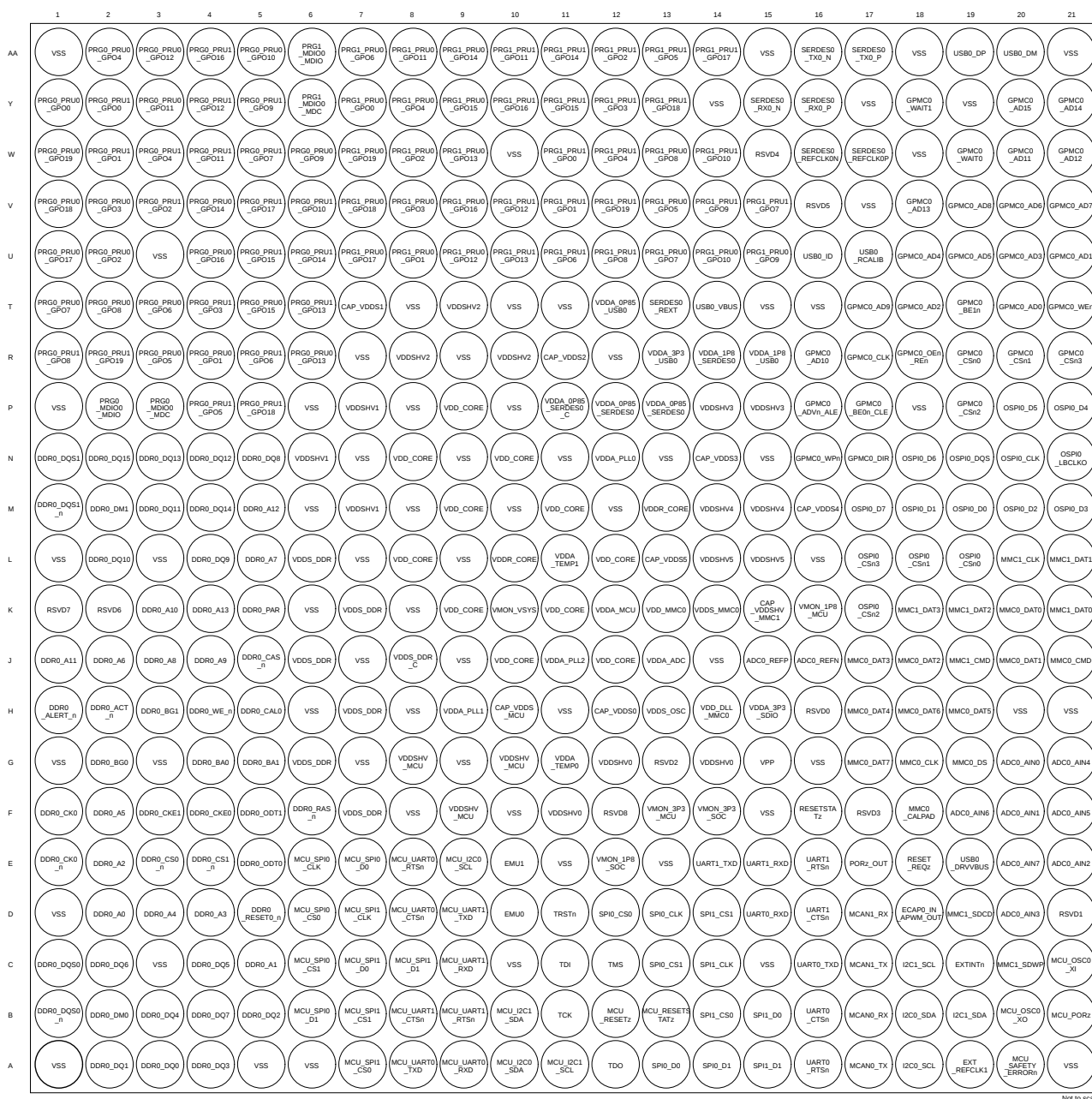


図 5-1. ALV FCBGA-N441 Pin Diagram (Bottom View)

## 5.2 Pin Attributes

The following list describes the contents of each column in 表 5-1, *Pin Attributes*:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

### 注

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

表 5-1, *Pin Attributes* only defines signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see the *Pad Configuration Registers* section in the *Device Configuration* chapter of the device TRM. For information associated with peripheral signal multiplexing, see the respective peripheral chapter in the device TRM.

4. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
  - a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

### 注

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU\_PORz is deasserted.

- b. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the [Pin Attributes](#) table. Only valid values of MUXMODE should be used.
- c. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz\_OUT. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
- d. An empty box means Not Applicable.

### 注

The following configurations of MUXMODE must be avoided for proper device operation.

- Configuring multiple pins operating as inputs to the same pin multiplexed signal function is not supported as it can yield unexpected results.
- Configuring a pin to an undefined pin multiplexing mode will cause the pin behavior to be undefined.

5. **TYPE:** Signal type and direction:
  - I = Input
  - O = Output
  - OD = Output, with open-drain output function
  - IO = Input, Output, or simultaneously Input and Output
  - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
  - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
  - OZ = Output with three-state output function
  - A = Analog
  - PWR = Power
  - GND = Ground
  - CAP = LDO Capacitor.
6. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
  - 0: Logic 0 driven to the subsystem input.
  - 1: Logic 1 driven to the subsystem input.
  - pad: Logic state of the pad is driven to the subsystem input.
  - An empty box means Not Applicable.
7. **BALL STATE DURING RESET RX/TX/PULL:** State of the terminal while MCU\_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
  - RX (Input buffer)
    - Off: The input buffer is disabled.
    - On: The input buffer is enabled.
  - TX (Output buffer)
    - Off: The output buffer is disabled.
    - Low: The output buffer is enabled and drives  $V_{OL}$ .
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned off.
    - Up: Internal pull-up resistor is turned on.
    - Down: Internal pull-down resistor is turned on.
    - NA: Not Applicable.
  - An empty box means Not Applicable.
8. **BALL STATE AFTER RESET RX/TX/PULL:** State of the terminal after MCU\_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
  - RX (Input buffer)
    - Off: The input buffer is disabled.
    - On: The input buffer is enabled.
  - TX (Output buffer)
    - Off: The output buffer is disabled.
    - SS: The subsystem selected with MUXMODE determines the output buffer state.
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned off.
    - Up: Internal pull-up resistor is turned on.
    - Down: Internal pull-down resistor is turned on.
    - NA: Not Applicable.
  - An empty box means Not Applicable.
9. **MUX MODE AFTER RESET:** The value found in this column defines the default pin multiplexed signal function after MCU\_PORz is deasserted.

An empty box means Not Applicable.

10. **I/O OPERATING VOLTAGE:** This column describes I/O operating voltage options of the respective power supply, when applicable.

An empty box means Not Applicable.

For more information, see valid operating voltage range(s) defined for each power supply in [セクション 6.4, Recommended Operating Conditions](#).

11. **POWER:** The power supply of the associated I/O, when applicable.

An empty box means Not Applicable.

12. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:

- Yes: With hysteresis
- No: Without hysteresis
- An empty box means Not Applicable.

For more information, see the hysteresis values in [セクション 6.7, Electrical Characteristics](#).

13. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

An empty box means Not Applicable.

For electrical characteristics, refer to the appropriate buffer type table in [セクション 6.7, Electrical Characteristics](#).

14. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

- PU: Internal pull-up
- PD: Internal pull-down
- PU/PD: Internal pull-up and pull-down
- An empty box means No internal pull.

15. **PADCONFIG Register:** Name of the IO pad configuration register associated with Ball.

16. **PADCONFIG Address:** Physical address of the IO pad configuration register associated with Ball.

**表 5-1. Pin Attributes (ALV Package)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]              | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|-------------------------|----------|---------------------|------------------------------|
| J16                | ADC0_REFN                                                          | ADC0_REFN       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               |          | ADC12B              |                              |
| J15                | ADC0_REFP                                                          | ADC0_REFP       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               |          | ADC12B              |                              |
| G20                | ADC0_AIN0                                                          | ADC0_AIN0       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| F20                | ADC0_AIN1                                                          | ADC0_AIN1       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| E21                | ADC0_AIN2                                                          | ADC0_AIN2       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| D20                | ADC0_AIN3                                                          | ADC0_AIN3       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| G21                | ADC0_AIN4                                                          | ADC0_AIN4       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| F21                | ADC0_AIN5                                                          | ADC0_AIN5       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| F19                | ADC0_AIN6                                                          | ADC0_AIN6       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| E20                | ADC0_AIN7                                                          | ADC0_AIN7       |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_ADC0               | Yes      | ADC12B              |                              |
| H12                | CAP_VDDS0                                                          | CAP_VDDS0       |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| T7                 | CAP_VDDS1                                                          | CAP_VDDS1       |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| R11                | CAP_VDDS2                                                          | CAP_VDDS2       |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| N14                | CAP_VDDS3                                                          | CAP_VDDS3       |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| M16                | CAP_VDDS4                                                          | CAP_VDDS4       |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| L13                | CAP_VDDS5                                                          | CAP_VDDS5       |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| K15                | CAP_VDDSHV_MMC1                                                    | CAP_VDDSHV_MMC1 |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| H10                | CAP_VDDS_MCU                                                       | CAP_VDDS_MCU    |                 | CAP      |          |                                                    |                                                   |                                      |                                  |                         |          |                     |                              |
| H2                 | DDR0_ACT_n                                                         | DDR0_ACT_n      |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| H1                 | DDR0_ALERT_n                                                       | DDR0_ALERT_n    |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| J5                 | DDR0_CAS_n                                                         | DDR0_CAS_n      |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| K5                 | DDR0_PAR                                                           | DDR0_PAR        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| F6                 | DDR0_RAS_n                                                         | DDR0_RAS_n      |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| H4                 | DDR0_WE_n                                                          | DDR0_WE_n       |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| D2                 | DDR0_A0                                                            | DDR0_A0         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| C5                 | DDR0_A1                                                            | DDR0_A1         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| E2                 | DDR0_A2                                                            | DDR0_A2         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| D4                 | DDR0_A3                                                            | DDR0_A3         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |
| D3                 | DDR0_A4                                                            | DDR0_A4         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDS_DDR,<br>VDDS_DDR_C |          | DDR                 |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]            | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|-----------------------|----------|---------------------|------------------------------|
| F2                 | DDR0_A5                                                            | DDR0_A5         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| J2                 | DDR0_A6                                                            | DDR0_A6         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| L5                 | DDR0_A7                                                            | DDR0_A7         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| J3                 | DDR0_A8                                                            | DDR0_A8         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| J4                 | DDR0_A9                                                            | DDR0_A9         |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| K3                 | DDR0_A10                                                           | DDR0_A10        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| J1                 | DDR0_A11                                                           | DDR0_A11        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| M5                 | DDR0_A12                                                           | DDR0_A12        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| K4                 | DDR0_A13                                                           | DDR0_A13        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| G4                 | DDR0_BA0                                                           | DDR0_BA0        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| G5                 | DDR0_BA1                                                           | DDR0_BA1        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| G2                 | DDR0_BG0                                                           | DDR0_BG0        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| H3                 | DDR0_BG1                                                           | DDR0_BG1        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| H5                 | DDR0_CAL0                                                          | DDR0_CAL0       |                 | A        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| F1                 | DDR0_CK0                                                           | DDR0_CK0        |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| E1                 | DDR0_CK0_n                                                         | DDR0_CK0_n      |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| F4                 | DDR0_CKE0                                                          | DDR0_CKE0       |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| F3                 | DDR0_CKE1                                                          | DDR0_CKE1       |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| E3                 | DDR0_CS0_n                                                         | DDR0_CS0_n      |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| E4                 | DDR0_CS1_n                                                         | DDR0_CS1_n      |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| B2                 | DDR0_DM0                                                           | DDR0_DM0        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| M2                 | DDR0_DM1                                                           | DDR0_DM1        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]            | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|-----------------------|----------|---------------------|------------------------------|
| A3                 | DDR0_DQ0                                                           | DDR0_DQ0        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| A2                 | DDR0_DQ1                                                           | DDR0_DQ1        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| B5                 | DDR0_DQ2                                                           | DDR0_DQ2        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| A4                 | DDR0_DQ3                                                           | DDR0_DQ3        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| B3                 | DDR0_DQ4                                                           | DDR0_DQ4        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| C4                 | DDR0_DQ5                                                           | DDR0_DQ5        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| C2                 | DDR0_DQ6                                                           | DDR0_DQ6        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| B4                 | DDR0_DQ7                                                           | DDR0_DQ7        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| N5                 | DDR0_DQ8                                                           | DDR0_DQ8        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| L4                 | DDR0_DQ9                                                           | DDR0_DQ9        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| L2                 | DDR0_DQ10                                                          | DDR0_DQ10       |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| M3                 | DDR0_DQ11                                                          | DDR0_DQ11       |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| N4                 | DDR0_DQ12                                                          | DDR0_DQ12       |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| N3                 | DDR0_DQ13                                                          | DDR0_DQ13       |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| M4                 | DDR0_DQ14                                                          | DDR0_DQ14       |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| N2                 | DDR0_DQ15                                                          | DDR0_DQ15       |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| C1                 | DDR0_QS0                                                           | DDR0_QS0        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| B1                 | DDR0_QS0_n                                                         | DDR0_QS0_n      |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| N1                 | DDR0_QS1                                                           | DDR0_QS1        |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| M1                 | DDR0_QS1_n                                                         | DDR0_QS1_n      |                 | IO       |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| E5                 | DDR0_ODT0                                                          | DDR0_ODT0       |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| F5                 | DDR0_ODT1                                                          | DDR0_ODT1       |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]        | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]            | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|-----------------------|----------|---------------------|------------------------------|
| D5                 | DDR0_RESET0_n                                                      | DDR0_RESET0_n          |                 | O        |          |                                                    |                                                   |                                      | 1.1 V/1.2 V                      | VDDSDDR,<br>VDDSDDR_C |          | DDR                 |                              |
| D18                | ECAP0_IN_APWM_OUT<br><br>PADCONFIG:<br>PADCONFIG156<br>0x000F4270  | ECAP0_IN_APWM_OUT      | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0               | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | SYNCO_OUT              | 1               | O        |          |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | CPTS0_RFT_CLK          | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_RFT_CLK | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | SPI4_CS3               | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | GPIO1_68               | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
| D10                | EMU0<br><br>PADCONFIG:<br>MCU_PADCONFIG31<br>0x0408407C            | EMU0                   | 0               | IO       | 1        | On / Off / Up                                      | On / Off / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU            | Yes      | LVCMOS              | PU/PD                        |
| E10                | EMU1<br><br>PADCONFIG:<br>MCU_PADCONFIG32<br>0x04084080            | EMU1                   | 0               | IO       | 1        | On / Off / Up                                      | On / Off / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU            | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_OBSCCLK0           | 15              | O        |          |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
| C19                | EXTINTn<br><br>PADCONFIG:<br>PADCONFIG158<br>0x000F4278            | EXTINTn                | 0               | I        | 1        | Off / Off / NA                                     | Off / Off / NA                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV0               | Yes      | I2C OD FS           |                              |
|                    |                                                                    | GPIO1_70               | 7               | IOD      | pad      |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
| A19                | EXT_REFCLK1<br><br>PADCONFIG:<br>PADCONFIG157<br>0x000F4274        | EXT_REFCLK1            | 0               | I        | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0               | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | SYNC1_OUT              | 1               | O        |          |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | SPI2_CS3               | 2               | IO       | 1        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | CLKOUT0                | 5               | O        |          |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | GPIO1_69               | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
| P16                | GPMC0_ADVn_ALE<br><br>PADCONFIG:<br>PADCONFIG33<br>0x000F4084      | GPMC0_ADVn_ALE         | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3               | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX5_CLK            | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | UART5_RXD              | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN3         | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | TRC_DATA15             | 6               | O        |          |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | GPIO0_32               | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |
|                    |                                                                    | PRG0_PWM3_TZ_IN        | 9               | I        | 0        |                                                    |                                                   |                                      |                                  |                       |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]  | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| R17                | GPMC0_CLK<br>PADCONFIG:<br>PADCONFIG31<br>0x000F407C               | GPMC0_CLK        | 0               | O        | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX4_CLK      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_RTSn       | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM3_SYNC0    | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_FCLK_MUX   | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA14       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_31         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| N17                | GPMC0_DIR<br>PADCONFIG:<br>PADCONFIG41<br>0x000F40A4               | PRG0_PWM3_TZ_OUT | 9               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPMC0_DIR        | 0               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP0_B          | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_40         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM6_B        | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| R18                | GPMC0_OEn_REn<br>PADCONFIG:<br>PADCONFIG34<br>0x000F4088           | PRG1_PWM2_B0     | 9               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPMC0_OEn_REn    | 0               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | FSI_RX5_D0       | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART5_TXD        | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM4_A        | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA16       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_33         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| T21                | GPMC0_WEn<br>PADCONFIG:<br>PADCONFIG35<br>0x000F408C               | PRG0_PWM3_A1     | 9               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPMC0_WEn        | 0               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | FSI_RX5_D1       | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART5_RTSn       | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM4_B        | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA17       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_34         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| N16                | GPMC0_WPn<br>PADCONFIG:<br>PADCONFIG40<br>0x000F40A0               | PRG0_PWM3_B1     | 9               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPMC0_WPn        | 0               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | FSI_TX1_CLK      | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP0_A          | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A22        | 4               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA22       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_39         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM6_A        | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_A0     | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]  | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| T20                | GPMC0_AD0<br>PADCONFIG:<br>PADCONFIG15<br>0x000F403C               | GPMC0_AD0        | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX2_CLK      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART2_RXD        | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM0_SYNCI    | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_CLK          | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_15         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | BOOTMODE00       | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| U21                | GPMC0_AD1<br>PADCONFIG:<br>PADCONFIG16<br>0x000F4040               | GPMC0_AD1        | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX2_D0       | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART2_TXD        | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM0_SYNCO    | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_CTL          | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_16         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_TZ_OUT | 9               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| T18                | GPMC0_AD2<br>PADCONFIG:<br>PADCONFIG17<br>0x000F4044               | GPMC0_AD2        | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX2_D1       | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART2_RTSn       | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN0   | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA0        | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_17         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_TZ_IN  | 9               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| U20                | GPMC0_AD3<br>PADCONFIG:<br>PADCONFIG18<br>0x000F4048               | GPMC0_AD3        | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX3_CLK      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART3_RXD        | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM0_A        | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA1        | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_18         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_A0     | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | BOOTMODE03       | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    |                  |                 |          |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    |                  |                 |          |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    |                  |                 |          |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    |                  |                 |          |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    |                  |                 |          |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    |                  |                 |          |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| U18                | GPMC0_AD4<br>PADCONFIG:<br>PADCONFIG19<br>0x000F404C               | GPMC0_AD4       | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX3_D0      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART3_TXD       | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM0_B       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA2       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_82        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_B0    | 9               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | BOOTMODE04      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| U19                | GPMC0_AD5<br>PADCONFIG:<br>PADCONFIG20<br>0x000F4050               | GPMC0_AD5       | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX3_D1      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART3_RTSn      | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM1_A       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA3       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_83        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_A1    | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | BOOTMODE05      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V20                | GPMC0_AD6<br>PADCONFIG:<br>PADCONFIG21<br>0x000F4054               | GPMC0_AD6       | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX4_D0      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_RXD       | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM1_B       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA4       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_21        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_B1    | 9               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | BOOTMODE06      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V21                | GPMC0_AD7<br>PADCONFIG:<br>PADCONFIG22<br>0x000F4058               | GPMC0_AD7       | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX4_D1      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_TXD       | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN1  | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM8_A       | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA5       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_22        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_A2    | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | BOOTMODE07      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| V19                | GPMC0_AD8<br>PADCONFIG:<br>PADCONFIG23<br>0x000F405C               | GPMC0_AD8       | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX0_CLK     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART2_CTSn      | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM2_A       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA6       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_23        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM2_A2    | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE08      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| T17                | GPMC0_AD9<br>PADCONFIG:<br>PADCONFIG24<br>0x000F4060               | GPMC0_AD9       | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX0_D0      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART3_CTSn      | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM2_B       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA7       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_24        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM2_B2    | 9               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE09      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| R16                | GPMC0_AD10<br>PADCONFIG:<br>PADCONFIG25<br>0x000F4064              | GPMC0_AD10      | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX0_D1      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART4_CTSn      | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN2  | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM8_B       | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA8       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_25        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM2_B2    | 9               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE10      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| W20                | GPMC0_AD11<br>PADCONFIG:<br>PADCONFIG26<br>0x000F4068              | GPMC0_AD11      | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX1_CLK     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART5_CTSn      | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP1_A         | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA9       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_26        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM7_A       | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE11      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| W21                | GPMC0_AD12<br>PADCONFIG:<br>PADCONFIG27<br>0x000F406C              | GPMC0_AD12      | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX1_D0      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART6_CTSn      | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP1_B         | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA10      | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_27        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM7_B       | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE12      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| V18                | GPMC0_AD13<br>PADCONFIG:<br>PADCONFIG28<br>0x000F4070              | GPMC0_AD13      | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_RX1_D1      | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM3_A       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA11      | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_28        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM3_A0    | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE13      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| Y21                | GPMC0_AD14<br>PADCONFIG:<br>PADCONFIG29<br>0x000F4074              | GPMC0_AD14      | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_TX0_D0      | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART6_RXD       | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM3_B       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA12      | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_29        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM3_B0    | 9               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE14      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| Y20                | GPMC0_AD15<br>PADCONFIG:<br>PADCONFIG30<br>0x000F4078              | GPMC0_AD15      | 0               | IO       | 0        | On / Off / Off                                     | On / Off / Off                                    | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_TX0_D1      | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART6_TXD       | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM3_SYNCI   | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA13      | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_30        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | BOOTMODE15      | Bootstrap       | I        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]  | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| P17                | GPMC0_BE0n_CLE<br><br>PADCONFIG:<br>PADCONFIG36<br>0x000F4090      | GPMC0_BE0n_CLE   | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_TX1_D0       | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART6_RTSn       | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN4   | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM7_A        | 5               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA18       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_35         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_A1     | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| T19                | GPMC0_BE1n<br><br>PADCONFIG:<br>PADCONFIG37<br>0x000F4094          | GPMC0_BE1n       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_TX0_CLK      | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM5_A        | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA19       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_36         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM3_A2     | 9               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| R19                | GPMC0_CSn0<br><br>PADCONFIG:<br>PADCONFIG42<br>0x000F40A8          | GPMC0_CSn0       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | EQEP0_S          | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TRC_DATA23       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_41         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM6_SYNCI    | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| R20                | GPMC0_CSn1<br><br>PADCONFIG:<br>PADCONFIG43<br>0x000F40AC          | GPMC0_CSn1       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | EQEP0_I          | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN2   | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_42         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM6_SYNC0    | 8               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_TZ_OUT | 9               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| P19                | GPMC0_CSn2<br><br>PADCONFIG:<br>PADCONFIG44<br>0x000F40B0          | GPMC0_CSn2       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | I2C2_SCL         | 1               | IOD      | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TIMER_IO8        | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP1_S          | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN4   | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_43         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_TZ_IN  | 9               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| R21                | GPMC0_CSn3<br>PADCONFIG:<br>PADCONFIG45<br>0x000F40B4              | GPMC0_CSn3      | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | I2C2_SDA        | 1               | IOD      | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO9       | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP1_I         | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A20       | 4               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN5  | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_44        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| W19                | GPMC0_WAIT0<br>PADCONFIG:<br>PADCONFIG38<br>0x000F4098             | GPMC0_WAIT0     | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | EHRPWM5_B       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA20      | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_37        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM3_B2    | 9               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| Y18                | GPMC0_WAIT1<br>PADCONFIG:<br>PADCONFIG39<br>0x000F409C             | GPMC0_WAIT1     | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV3    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | FSI_TX1_D1      | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM_TZn_IN5  | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A21       | 4               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM7_B       | 5               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TRC_DATA21      | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_38        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM2_B1    | 9               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| A18                | I2C0_SCL<br>PADCONFIG:<br>PADCONFIG152<br>0x000F4260               | I2C0_SCL        | 0               | IOD      | 1        | Off / Off / NA                                     | On / SS / NA                                      | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | I2C OD FS           |                              |
|                    |                                                                    | GPIO1_64        | 7               | IOD      | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| B18                | I2C0_SDA<br>PADCONFIG:<br>PADCONFIG153<br>0x000F4264               | I2C0_SDA        | 0               | IOD      | 1        | Off / Off / NA                                     | On / SS / NA                                      | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | I2C OD FS           |                              |
|                    |                                                                    | GPIO1_65        | 7               | IOD      | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| C18                | I2C1_SCL<br>PADCONFIG:<br>PADCONFIG154<br>0x000F4268               | I2C1_SCL        | 0               | IOD      | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | CPTS0_HW1TSPUSH | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO0       | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI2_CS1        | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_66        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| B19                | I2C1_SDA<br>PADCONFIG:<br>PADCONFIG155<br>0x000F426C               | I2C1_SDA        | 0               | IOD      | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | CPTS0_HW2TSPUSH | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO1       | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI2_CS2        | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_67        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]   | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| B17                | MCAN0_RX<br>PADCONFIG:<br>PADCONFIG149<br>0x000F4254               | MCAN0_RX          | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | UART4_TXD         | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO3         | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SYNC3_OUT         | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI4_CS2          | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_61          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP2_S           | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART0_RIn         | 9               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| A17                | MCAN0_TX<br>PADCONFIG:<br>PADCONFIG148<br>0x000F4250               | MCAN0_TX          | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | UART4_RXD         | 1               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO2         | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SYNC2_OUT         | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI4_CS1          | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_60          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP2_I           | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART0_DTRn        | 9               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| D17                | MCAN1_RX<br>PADCONFIG:<br>PADCONFIG151<br>0x000F425C               | MCAN1_RX          | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | I2C3_SDA          | 1               | IOD      | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | ECAP2_IN_APWM_OUT | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | OBSClk0           | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO5         | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART5_TXD         | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM_SOCB       | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_63          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP2_B           | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART0_DSRn        | 9               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | OBSClk0           | 15              | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]   | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| C17                | MCAN1_TX<br>PADCONFIG:<br>PADCONFIG150<br>0x000F4258               | MCAN1_TX          | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | I2C3_SCL          | 1               | IOD      | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | ECAP1_IN_APWM_OUT | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SYSCLKOUT0        | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_I04         | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART5_RXD         | 5               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM_SOC_A      | 6               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_62          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP2_A           | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART0_DCDn        | 9               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| E9                 | MCU_I2C0_SCL<br>PADCONFIG:<br>MCU_PADCONFIG18<br>0x04084048        | MCU_I2C0_SCL      | 0               | IOD      | 1        | Off / Off / NA                                     | On / SS / NA                                      | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | I2C OD FS           |                              |
|                    |                                                                    | MCU_GPIO0_18      | 7               | IOD      | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| A10                | MCU_I2C0_SDA<br>PADCONFIG:<br>MCU_PADCONFIG19<br>0x0408404C        | MCU_I2C0_SDA      | 0               | IOD      | 1        | Off / Off / NA                                     | On / SS / NA                                      | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | I2C OD FS           |                              |
|                    |                                                                    | MCU_GPIO0_19      | 7               | IOD      | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| A11                | MCU_I2C1_SCL<br>PADCONFIG:<br>MCU_PADCONFIG20<br>0x04084050        | MCU_I2C1_SCL      | 0               | IOD      | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_20      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| B10                | MCU_I2C1_SDA<br>PADCONFIG:<br>MCU_PADCONFIG21<br>0x04084054        | MCU_I2C1_SDA      | 0               | IOD      | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_21      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| C21                | MCU_OSC0_XI                                                        | MCU_OSC0_XI       |                 | I        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDS_OSC   | Yes      | HFOSC               |                              |
| B20                | MCU_OSC0_XO                                                        | MCU_OSC0_XO       |                 | O        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDS_OSC   | Yes      | HFOSC               |                              |
| B21                | MCU_PORz<br>PADCONFIG:<br>MCU_PADCONFIG23<br>0x0408405C            | MCU_PORz          | 0               | I        |          |                                                    |                                                   | 0                                    | 1.8 V                            | VDDS_OSC   | Yes      | FS RESET            |                              |
| B13                | MCU_RESETSTATz<br>PADCONFIG:<br>MCU_PADCONFIG24<br>0x04084060      | MCU_RESETSTATz    | 0               | O        |          | Off / Low / Off                                    | Off / SS / Off                                    | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_22      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| B12                | MCU_RESETz<br>PADCONFIG:<br>MCU_PADCONFIG22<br>0x04084058          | MCU_RESETz        | 0               | I        |          | On / Off / Up                                      | On / Off / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVCMOS              | PU/PD                        |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]   | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| A20                | MCU_SAFETY_ERRORn<br>PADCONFIG:<br>MCU_PADCONFIG25<br>0x04084064   | MCU_SAFETY_ERRORn | 0               | IO       |          | Off / Off / Down                                   | On / SS / Down                                    | 0                                    | 1.8 V                            | VDDS_OSC   | Yes      | LVC MOS             | PU/PD                        |
| E6                 | MCU_SPI0_CLK<br>PADCONFIG:<br>MCU_PADCONFIG2<br>0x04084008         | MCU_SPI0_CLK      | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_11      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| D7                 | MCU_SPI1_CLK<br>PADCONFIG:<br>MCU_PADCONFIG7<br>0x0408401C         | MCU_SPI1_CLK      | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_7       | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| D6                 | MCU_SPI0_CS0<br>PADCONFIG:<br>MCU_PADCONFIG0<br>0x04084000         | MCU_SPI0_CS0      | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_13      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| C6                 | MCU_SPI0_CS1<br>PADCONFIG:<br>MCU_PADCONFIG1<br>0x04084004         | MCU_SPI0_CS1      | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_OBSCLK0       | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | MCU_SYSCLKOUT0    | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | MCU_GPIO0_12      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| E7                 | MCU_SPI0_D0<br>PADCONFIG:<br>MCU_PADCONFIG3<br>0x0408400C          | MCU_SPI0_D0       | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_10      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| B6                 | MCU_SPI0_D1<br>PADCONFIG:<br>MCU_PADCONFIG4<br>0x04084010          | MCU_SPI0_D1       | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_4       | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| A7                 | MCU_SPI1_CS0<br>PADCONFIG:<br>MCU_PADCONFIG5<br>0x04084014         | MCU_SPI1_CS0      | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_5       | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| B7                 | MCU_SPI1_CS1<br>PADCONFIG:<br>MCU_PADCONFIG6<br>0x04084018         | MCU_SPI1_CS1      | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_EXT_REFCLK0   | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | MCU_GPIO0_6       | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| C7                 | MCU_SPI1_D0<br>PADCONFIG:<br>MCU_PADCONFIG8<br>0x04084020          | MCU_SPI1_D0       | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_8       | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| C8                 | MCU_SPI1_D1<br>PADCONFIG:<br>MCU_PADCONFIG9<br>0x04084024          | MCU_SPI1_D1       | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_9       | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]                              | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|-----------------------------------------|----------|---------------------|------------------------------|
| D8                 | MCU_UART0_CTSn<br>PADCONFIG:<br>MCU_PADCONFIG12<br>0x04084030      | MCU_UART0_CTSn  | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_TIMER_IO0   | 1               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_SPI0_CS2    | 2               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_GPIO0_1     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| E8                 | MCU_UART0_RTSn<br>PADCONFIG:<br>MCU_PADCONFIG13<br>0x04084034      | MCU_UART0_RTSn  | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_TIMER_IO1   | 1               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_SPI1_CS2    | 2               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_GPIO0_0     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| A9                 | MCU_UART0_RXD<br>PADCONFIG:<br>MCU_PADCONFIG10<br>0x04084028       | MCU_UART0_RXD   | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_3     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| A8                 | MCU_UART0_TXD<br>PADCONFIG:<br>MCU_PADCONFIG11<br>0x0408402C       | MCU_UART0_TXD   | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_2     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| B8                 | MCU_UART1_CTSn<br>PADCONFIG:<br>MCU_PADCONFIG16<br>0x04084040      | MCU_UART1_CTSn  | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_TIMER_IO2   | 1               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_SPI0_CS3    | 2               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_GPIO0_16    | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| B9                 | MCU_UART1_RTSn<br>PADCONFIG:<br>MCU_PADCONFIG17<br>0x04084044      | MCU_UART1_RTSn  | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_TIMER_IO3   | 1               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_SPI1_CS3    | 2               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | MCU_GPIO0_17    | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| C9                 | MCU_UART1_RXD<br>PADCONFIG:<br>MCU_PADCONFIG14<br>0x04084038       | MCU_UART1_RXD   | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_14    | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| D9                 | MCU_UART1_TXD<br>PADCONFIG:<br>MCU_PADCONFIG15<br>0x0408403C       | MCU_UART1_TXD   | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV_MCU                              | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MCU_GPIO0_15    | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| F18                | MMC0_CALPAD                                                        | MMC0_CALPAD     |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMC PHY            |                              |
| G18                | MMC0_CLK                                                           | MMC0_CLK        |                 | IO       |          | On / Low / Off                                     | On / SS / Off                                     |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMC PHY            | PU/PD                        |
| J21                | MMC0_CMD                                                           | MMC0_CMD        |                 | IO       |          | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMC PHY            | PU/PD                        |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]                              | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|-----------------------------------------|----------|---------------------|------------------------------|
| G19                | MMC0_DS                                                            | MMC0_DS         |                 | IO       |          | On / Off / Down                                    | On / Off / Down                                   |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMCPHY             | PU/PD                        |
| L20                | MMC1_CLK<br>PADCONFIG:<br>PADCONFIG163<br>0x000F428C               | MMC1_CLK        | 0               | IO       |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV5                                 | Yes      | SDIO                | PU/PD                        |
|                    |                                                                    | UART2_CTSn      | 1               | I        | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | TIMER_IO4       | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | UART4_RXD       | 3               | I        | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | GPIO1_75        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| J19                | MMC1_CMD<br>PADCONFIG:<br>PADCONFIG165<br>0x000F4294               | MMC1_CMD        | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV5                                 | Yes      | SDIO                | PU/PD                        |
|                    |                                                                    | UART2_RTSn      | 1               | O        |          |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | TIMER_IO5       | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | UART4_TXD       | 3               | O        |          |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | GPIO1_76        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| D19                | MMC1_SDCD<br>PADCONFIG:<br>PADCONFIG166<br>0x000F4298              | MMC1_SDCD       | 0               | I        | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                 | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | UART3_CTSn      | 1               | I        | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | TIMER_IO6       | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | UART5_RXD       | 3               | I        | 1        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | GPIO1_77        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| C20                | MMC1_SDWP<br>PADCONFIG:<br>PADCONFIG167<br>0x000F429C              | MMC1_SDWP       | 0               | I        | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                 | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | UART3_RTSn      | 1               | O        |          |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | TIMER_IO7       | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | UART5_TXD       | 3               | O        |          |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
|                    |                                                                    | GPIO1_78        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                         |          |                     |                              |
| K20                | MMC0_DAT0                                                          | MMC0_DAT0       |                 | IO       |          | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMCPHY             | PU/PD                        |
| J20                | MMC0_DAT1                                                          | MMC0_DAT1       |                 | IO       |          | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMCPHY             | PU/PD                        |
| J18                | MMC0_DAT2                                                          | MMC0_DAT2       |                 | IO       |          | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMCPHY             | PU/PD                        |
| J17                | MMC0_DAT3                                                          | MMC0_DAT3       |                 | IO       |          | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMCPHY             | PU/PD                        |
| H17                | MMC0_DAT4                                                          | MMC0_DAT4       |                 | IO       |          | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMCPHY             | PU/PD                        |
| H19                | MMC0_DAT5                                                          | MMC0_DAT5       |                 | IO       |          | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |          | eMMCPHY             | PU/PD                        |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]          | MUX<br>MODE [4] | TYPE<br>[5] | DSIS<br>[6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]                              | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------------|-----------------|-------------|-------------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|-----------------------------------------|-------------|---------------------|------------------------------|
| H18                | MMC0_DAT6                                                          | MMC0_DAT6                |                 | IO          |             | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |             | eMMC PHY            | PU/PD                        |
| G17                | MMC0_DAT7                                                          | MMC0_DAT7                |                 | IO          |             | On / Off / Up                                      | On / SS / Up                                      |                                      | 1.8 V                            | VDDS_MMC0,<br>VDD_MMC0,<br>VDD_DLL_MMC0 |             | eMMC PHY            | PU/PD                        |
| K21                | MMC1_DAT0<br>PADCONFIG:<br>PADCONFIG162<br>0x000F4288              | MMC1_DAT0                | 0               | IO          | 1           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV5                                 | Yes         | SDIO                | PU/PD                        |
|                    |                                                                    | CP_GEMAC_CPTS0_HW2TSPUSH | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | TIMER_IO3                | 2               | IO          | 0           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | UART3_TXD                | 3               | O           |             |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | GPIO1_74                 | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
| L21                | MMC1_DAT1<br>PADCONFIG:<br>PADCONFIG161<br>0x000F4284              | MMC1_DAT1                | 0               | IO          | 1           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV5                                 | Yes         | SDIO                | PU/PD                        |
|                    |                                                                    | CP_GEMAC_CPTS0_HW1TSPUSH | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | TIMER_IO2                | 2               | IO          | 0           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | UART3_RXD                | 3               | I           | 1           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | GPIO1_73                 | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
| K19                | MMC1_DAT2<br>PADCONFIG:<br>PADCONFIG160<br>0x000F4280              | MMC1_DAT2                | 0               | IO          | 1           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV5                                 | Yes         | SDIO                | PU/PD                        |
|                    |                                                                    | CP_GEMAC_CPTS0_TS_SYNC   | 1               | O           |             |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | TIMER_IO1                | 2               | IO          | 0           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | UART2_TXD                | 3               | O           |             |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | GPIO1_72                 | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
| K18                | MMC1_DAT3<br>PADCONFIG:<br>PADCONFIG159<br>0x000F427C              | MMC1_DAT3                | 0               | IO          | 1           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV5                                 | Yes         | SDIO                | PU/PD                        |
|                    |                                                                    | CP_GEMAC_CPTS0_TS_COMP   | 1               | O           |             |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | TIMER_IO0                | 2               | IO          | 0           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | UART2_RXD                | 3               | I           | 1           |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
|                    |                                                                    | GPIO1_71                 | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
| N20                | OSPI0_CLK<br>PADCONFIG:<br>PADCONFIG0<br>0x000F4000                | OSPI0_CLK                | 0               | O           |             | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4                                 | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_0                  | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
| N19                | OSPI0_DQS<br>PADCONFIG:<br>PADCONFIG2<br>0x000F4008                | OSPI0_DQS                | 0               | I           | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4                                 | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_2                  | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |
| N21                | OSPI0_LBCLKO<br>PADCONFIG:<br>PADCONFIG1<br>0x000F4004             | OSPI0_LBCLKO             | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4                                 | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_1                  | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |                                         |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]  | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| L19                | OSPI0_CSn0<br>PADCONFIG:<br>PADCONFIG11<br>0x000F402C              | OSPI0_CSn0       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_11         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| L18                | OSPI0_CSn1<br>PADCONFIG:<br>PADCONFIG12<br>0x000F4030              | OSPI0_CSn1       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_12         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| K17                | OSPI0_CSn2<br>PADCONFIG:<br>PADCONFIG13<br>0x000F4034              | OSPI0_CSn2       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | OSPI0_RESET_OUT1 | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_13         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| L17                | OSPI0_CSn3<br>PADCONFIG:<br>PADCONFIG14<br>0x000F4038              | OSPI0_CSn3       | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | OSPI0_RESET_OUT0 | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | OSPI0_ECC_FAIL   | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_14         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| M19                | OSPI0_D0<br>PADCONFIG:<br>PADCONFIG3<br>0x000F400C                 | OSPI0_D0         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_3          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| M18                | OSPI0_D1<br>PADCONFIG:<br>PADCONFIG4<br>0x000F4010                 | OSPI0_D1         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_4          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| M20                | OSPI0_D2<br>PADCONFIG:<br>PADCONFIG5<br>0x000F4014                 | OSPI0_D2         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_5          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| M21                | OSPI0_D3<br>PADCONFIG:<br>PADCONFIG6<br>0x000F4018                 | OSPI0_D3         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_6          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| P21                | OSPI0_D4<br>PADCONFIG:<br>PADCONFIG7<br>0x000F401C                 | OSPI0_D4         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_7          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| P20                | OSPI0_D5<br>PADCONFIG:<br>PADCONFIG8<br>0x000F4020                 | OSPI0_D5         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_8          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| N18                | OSPI0_D6<br>PADCONFIG:<br>PADCONFIG9<br>0x000F4024                 | OSPI0_D6         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_9          | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| M17                | OSPI0_D7<br>PADCONFIG:<br>PADCONFIG10<br>0x000F4028                | OSPI0_D7        | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV4    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO0_10        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| E17                | PORz_OUT<br>PADCONFIG:<br>PADCONFIG171<br>0x000F42AC               | PORz_OUT        | 0               | O        |          | Off / Low / Off                                    | Off / SS / Off                                    | 0                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVCMOS              | PU/PD                        |
| P3                 | PRG0_MDIO0_MDC<br>PADCONFIG:<br>PADCONFIG129<br>0x000F4204         | PRG0_MDIO0_MDC  | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO1_41        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A13       | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| P2                 | PRG0_MDIO0_MDIO<br>PADCONFIG:<br>PADCONFIG128<br>0x000F4200        | PRG0_MDIO0_MDIO | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO1_40        | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A12       | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| Y1                 | PRG0_PRU0_GPO0<br>PADCONFIG:<br>PADCONFIG88<br>0x000F4160          | PRG0_PRU0_GPO0  | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI0  | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII1_RD0 | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM3_A0    | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_0         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART2_CTSn      | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| R4                 | PRG0_PRU0_GPO1<br>PADCONFIG:<br>PADCONFIG89<br>0x000F4164          | PRG0_PRU0_GPO1  | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI1  | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII1_RD1 | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM3_B0    | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_1         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART2_TXD       | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| U2                 | PRG0_PRU0_GPO2<br>PADCONFIG:<br>PADCONFIG90<br>0x000F4168          | PRG0_PRU0_GPO2  | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI2  | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII1_RD2 | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM2_A0    | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_2         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A0        | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART2_RTSn      | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]          | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| V2                 | PRG0_PRU0_GPO3<br>PADCONFIG:<br>PADCONFIG91<br>0x000F416C          | PRG0_PRU0_GPO3           | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI3           | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII1_RD3          | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM3_A2             | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_3                  | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART3_CTSn               | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA2                | PRG0_PRU0_GPO4<br>PADCONFIG:<br>PADCONFIG92<br>0x000F4170          | PRG0_PRU0_GPO4           | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI4           | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII1_RX_CTL       | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_B0             | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_4                  | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A1                 | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| R3                 | PRG0_PRU0_GPO5<br>PADCONFIG:<br>PADCONFIG93<br>0x000F4174          | PRG0_PRU0_GPO5           | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI5           | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM3_B2             | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_5                  | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART3_RTSn               | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| T3                 | PRG0_PRU0_GPO6<br>PADCONFIG:<br>PADCONFIG94<br>0x000F4178          | PRG0_PRU0_GPO6           | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI6           | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII1_RXC          | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM3_A1             | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_6                  | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_CTSn               | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| T1                 | PRG0_PRU0_GPO7<br>PADCONFIG:<br>PADCONFIG95<br>0x000F417C          | PRG0_PRU0_GPO7           | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI7           | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDC_LATCH_IN1  | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM3_B1             | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CPTS0_HW2TSPUSH          | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_HW2TSPUSH | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TIMER_IO6                | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_7                  | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_TXD                | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]              | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| T2                 | PRG0_PRU0_GPO8<br><br>PADCONFIG:<br>PADCONFIG96<br>0x000F4180      | PRG0_PRU0_GPO8               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI8               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_A1                 | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_8                      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A2                     | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_RTSn                   | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W6                 | PRG0_PRU0_GPO9<br><br>PADCONFIG:<br>PADCONFIG97<br>0x000F4184      | PRG0_PRU0_GPO9               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI9               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_UART0_CTSn              | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM3_TZ_IN              | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMI1_RX_CTL                 | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII1_RX_ER                  | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDIO_DATA_IN_OUT28 | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_9                      | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA5                | PRG0_PRU0_GPO10<br><br>PADCONFIG:<br>PADCONFIG98<br>0x000F4188     | PRG0_PRU0_GPO10              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI10              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_UART0_RTSn              | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_B1                 | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMI1_RXC                    | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII_REF_CLK                 | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDIO_DATA_IN_OUT29 | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_10                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| Y3                 | PRG0_PRU0_GPO11<br><br>PADCONFIG:<br>PADCONFIG99<br>0x000F418C     | PRG0_PRU0_GPO11              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI11              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMI1_TD0               | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM3_TZ_OUT             | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_11                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_RXD                    | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA3                | PRG0_PRU0_GPO12<br><br>PADCONFIG:<br>PADCONFIG100<br>0x000F4190    | PRG0_PRU0_GPO12              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI12              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMI1_TD1               | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM0_A0                 | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_12                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A14                    | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]    | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| R6                 | PRG0_PRU0_GPO13<br>PADCONFIG:<br>PADCONFIG101<br>0x000F4194        | PRG0_PRU0_GPO13    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI13    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII1_TD2    | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM0_B0       | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI3_D0            | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_13           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A15          | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| V4                 | PRG0_PRU0_GPO14<br>PADCONFIG:<br>PADCONFIG102<br>0x000F4198        | PRG0_PRU0_GPO14    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI14    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII1_TD3    | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM0_A1       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI3_D1            | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_14           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A3           | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| T5                 | PRG0_PRU0_GPO15<br>PADCONFIG:<br>PADCONFIG103<br>0x000F419C        | PRG0_PRU0_GPO15    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI15    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII1_TX_CTL | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM0_B1       | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI3_CS1           | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_15           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A16          | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| U4                 | PRG0_PRU0_GPO16<br>PADCONFIG:<br>PADCONFIG104<br>0x000F41A0        | PRG0_PRU0_GPO16    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI16    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII1_TXC    | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM0_A2       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI3_CLK           | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_16           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A4           | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]          | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| U1                 | PRG0_PRU0_GPO17<br>PADCONFIG:<br>PADCONFIG105<br>0x000F41A4        | PRG0_PRU0_GPO17          | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI17          | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDC_SYNC_OUT1  | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM0_B2             | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CPTS0_TS_SYNC            | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_TS_SYNC   | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | SPI3_CS0                 | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_17                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TIMER_IO11               | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A17                | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V1                 | PRG0_PRU0_GPO18<br>PADCONFIG:<br>PADCONFIG106<br>0x000F41A8        | PRG0_PRU0_GPO18          | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI18          | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDC_LATCH_IN0  | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM0_TZ_IN          | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CPTS0_HW1TSPUSH          | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_HW1TSPUSH | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM8_A                | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_18                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_CTSn               | 8               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A5                 | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART2_RXD                | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W1                 | PRG0_PRU0_GPO19<br>PADCONFIG:<br>PADCONFIG107<br>0x000F41AC        | PRG0_PRU0_GPO19          | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU0_GPI19          | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDC_SYNC_OUT0  | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM0_TZ_OUT         | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CPTS0_TS_COMP            | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_TS_COMP   | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EHRPWM8_B                | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_19                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_RTSn               | 8               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A6                 | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART3_RXD                | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]    | MUX<br>MODE [4] | TYPE<br>[5] | DSIS<br>[6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------|-----------------|-------------|-------------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| Y2                 | PRG0_PRU1_GPO0<br>PADCONFIG:<br>PADCONFIG108<br>0x000F41B0         | PRG0_PRU1_GPO0     | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI0     | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII2_RD0    | 2               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_20           | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP0_A            | 8               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART5_CTSn         | 10              | I           | 1           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W2                 | PRG0_PRU1_GPO1<br>PADCONFIG:<br>PADCONFIG109<br>0x000F41B4         | PRG0_PRU1_GPO1     | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI1     | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII2_RD1    | 2               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_21           | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP0_B            | 8               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART5_TXD          | 10              | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V3                 | PRG0_PRU1_GPO2<br>PADCONFIG:<br>PADCONFIG110<br>0x000F41B8         | PRG0_PRU1_GPO2     | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI2     | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII2_RD2    | 2               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_A2       | 3               | IO          | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_22           | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP0_S            | 8               | IO          | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| T4                 | PRG0_PRU1_GPO3<br>PADCONFIG:<br>PADCONFIG111<br>0x000F41BC         | PRG0_PRU1_GPO3     | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI3     | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII2_RD3    | 2               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_23           | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP1_A            | 8               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A18          | 9               | OZ          |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W3                 | PRG0_PRU1_GPO4<br>PADCONFIG:<br>PADCONFIG112<br>0x000F41C0         | PRG0_PRU1_GPO4     | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI4     | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII2_RX_CTL | 2               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_B2       | 3               | IO          | 1           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_24           | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP1_B            | 8               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART6_TXD          | 10              | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]              | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| P4                 | PRG0_PRU1_GPO5<br>PADCONFIG:<br>PADCONFIG113<br>0x000F41C4         | PRG0_PRU1_GPO5               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI5               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_25                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP1_S                      | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART6_RTSn                   | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| R5                 | PRG0_PRU1_GPO6<br>PADCONFIG:<br>PADCONFIG114<br>0x000F41C8         | PRG0_PRU1_GPO6               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI6               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_RGMII2_RXC              | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_26                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP2_A                      | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A19                    | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_CTSn                   | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W5                 | PRG0_PRU1_GPO7<br>PADCONFIG:<br>PADCONFIG115<br>0x000F41CC         | PRG0_PRU1_GPO7               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI7               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP1_EDC_LATCH_IN1      | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII1_RD0                   | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII1_RXD0                   | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_27                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP2_B                      | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_TXD                    | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| R1                 | PRG0_PRU1_GPO8<br>PADCONFIG:<br>PADCONFIG116<br>0x000F41D0         | PRG0_PRU1_GPO8               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI8               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_PWM2_TZ_OUT             | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_28                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP2_S                      | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART4_RTSn                   | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| Y5                 | PRG0_PRU1_GPO9<br>PADCONFIG:<br>PADCONFIG117<br>0x000F41D4         | PRG0_PRU1_GPO9               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI9               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_UART0_RXD               | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII1_RD1                   | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII1_RXD1                   | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDIO_DATA_IN_OUT30 | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_29                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | EQEP0_I                      | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART5_RXD                    | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]              | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| V6                 | PRG0_PRU1_GPO10<br>PADCONFIG:<br>PADCONFIG118<br>0x000F41D8        | PRG0_PRU1_GPO10              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI10              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_UART0_TXD               | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM2_TZ_IN              | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII1_RD2                   | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RMII1_TXD0                   | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDIO_DATA_IN_OUT31 | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_30                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP1_I                      | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART6_RXD                    | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| W4                 | PRG0_PRU1_GPO11<br>PADCONFIG:<br>PADCONFIG119<br>0x000F41DC        | PRG0_PRU1_GPO11              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI11              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII2_TD0              | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_31                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP2_I                      | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART4_RXD                    | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| Y4                 | PRG0_PRU1_GPO12<br>PADCONFIG:<br>PADCONFIG120<br>0x000F41E0        | PRG0_PRU1_GPO12              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI12              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII2_TD1              | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_A0                 | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_32                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP2_B                      | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A7                     | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART4_TXD                    | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| T6                 | PRG0_PRU1_GPO13<br>PADCONFIG:<br>PADCONFIG121<br>0x000F41E4        | PRG0_PRU1_GPO13              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI13              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII2_TD2              | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_B0                 | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_33                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP0_I                      | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A8                     | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART5_RXD                    | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]         | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| U6                 | PRG0_PRU1_GPO14<br>PADCONFIG:<br>PADCONFIG122<br>0x000F41E8        | PRG0_PRU1_GPO14         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI14         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII2_TD3         | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_A1            | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_34                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP1_I                 | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A9                | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART6_RXD               | 10              | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| U5                 | PRG0_PRU1_GPO15<br>PADCONFIG:<br>PADCONFIG123<br>0x000F41EC        | PRG0_PRU1_GPO15         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI15         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII2_TX_CTL      | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_B1            | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_35                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A10               | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_ECAP0_IN_APWM_OUT  | 10              | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| AA4                | PRG0_PRU1_GPO16<br>PADCONFIG:<br>PADCONFIG124<br>0x000F41F0        | PRG0_PRU1_GPO16         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI16         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_RGMII2_TXC         | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_A2            | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_36                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A11               | 9               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_ECAP0_SYNC_OUT     | 10              | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| V5                 | PRG0_PRU1_GPO17<br>PADCONFIG:<br>PADCONFIG125<br>0x000F41F4        | PRG0_PRU1_GPO17         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI17         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_IEP1_EDC_SYNC_OUT1 | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_B2            | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII1_RD3              | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RMII1_TXD1              | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_37                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_ECAP0_SYNC_OUT     | 8               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_ECAP0_SYNC_IN      | 10              | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]         | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| P5                 | PRG0_PRU1_GPO18<br>PADCONFIG:<br>PADCONFIG126<br>0x000F41F8        | PRG0_PRU1_GPO18         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI18         | 1               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_IEP1_EDC_LATCH_IN0 | 2               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_TZ_IN         | 3               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | MDIO0_MDIO              | 4               | IO       | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | RMII1_TX_EN             | 5               | O        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM7_A               | 6               | IO       | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_38                | 7               | IO       | pad      |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| R2                 | PRG0_PRU1_GPO19<br>PADCONFIG:<br>PADCONFIG127<br>0x000F41FC        | PRG0_PRU1_GPO19         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 1.8 V/3.3 V                      | VDDSHV1    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG0_PRU1_GPI19         | 1               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_IEP1_EDC_SYNC_OUT0 | 2               | O        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG0_PWM1_TZ_OUT        | 3               | O        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | MDIO0_MDC               | 4               | O        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | RMII1_CRS_DV            | 5               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | EHRPWM7_B               | 6               | IO       | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_39                | 7               | IO       | pad      |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| Y6                 | PRG1_MDIO0_MDC<br>PADCONFIG:<br>PADCONFIG87<br>0x000F415C          | PRG1_MDIO0_MDC          | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MDIO0_MDC               | 4               | O        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_86                | 7               | IO       | pad      |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| AA6                | PRG1_MDIO0_MDIO<br>PADCONFIG:<br>PADCONFIG86<br>0x000F4158         | PRG1_MDIO0_MDIO         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | MDIO0_MDIO              | 4               | IO       | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_85                | 7               | IO       | pad      |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| Y7                 | PRG1_PRU0_GPO0<br>PADCONFIG:<br>PADCONFIG46<br>0x000F40B8          | PRG1_PRU0_GPO0          | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI0          | 1               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_RGMII1_RD0         | 2               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM3_A0            | 3               | IO       | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_45                | 7               | IO       | pad      |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_AD16              | 8               | IO       | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| U8                 | PRG1_PRU0_GPO1<br>PADCONFIG:<br>PADCONFIG47<br>0x000F40BC          | PRG1_PRU0_GPO1          | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI1          | 1               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_RGMII1_RD1         | 2               | I        | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM3_B0            | 3               | IO       | 1        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_46                | 7               | IO       | pad      |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_AD17              | 8               | IO       | 0        |                                                    |                                                   |                                   |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]    | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| W8                 | PRG1_PRU0_GPO2<br>PADCONFIG:<br>PADCONFIG48<br>0x000F40C0          | PRG1_PRU0_GPO2     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI2     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_RD2    | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_A0       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_47           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD18         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V8                 | PRG1_PRU0_GPO3<br>PADCONFIG:<br>PADCONFIG49<br>0x000F40C4          | PRG1_PRU0_GPO3     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI3     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_RD3    | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM3_A2       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_48           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD19         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| Y8                 | PRG1_PRU0_GPO4<br>PADCONFIG:<br>PADCONFIG50<br>0x000F40C8          | PRG1_PRU0_GPO4     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI4     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_RX_CTL | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_B0       | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_49           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD20         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V13                | PRG1_PRU0_GPO5<br>PADCONFIG:<br>PADCONFIG51<br>0x000F40CC          | PRG1_PRU0_GPO5     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI5     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM3_B2       | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII1_RX_CTL      | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_50           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD21         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA7                | PRG1_PRU0_GPO6<br>PADCONFIG:<br>PADCONFIG52<br>0x000F40D0          | PRG1_PRU0_GPO6     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI6     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_RXC    | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM3_A1       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_51           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD22         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]              | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| U13                | PRG1_PRU0_GPO7<br>PADCONFIG:<br>PADCONFIG53<br>0x000F40D4          | PRG1_PRU0_GPO7               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI7               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDC_LATCH_IN1      | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM3_B1                 | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CPTS0_HW2TSPUSH              | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | CLKOUT0                      | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TIMER_IO10                   | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_52                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W13                | PRG1_PRU0_GPO8<br>PADCONFIG:<br>PADCONFIG54<br>0x000F40D8          | PRG1_PRU0_GPO8               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI8               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_A1                 | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMI11_RXC                   | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_53                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| U15                | PRG1_PRU0_GPO9<br>PADCONFIG:<br>PADCONFIG55<br>0x000F40DC          | PRG1_PRU0_GPO9               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI9               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_UART0_CTSn              | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM3_TZ_IN              | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMI11_TX_CTL                | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII1_RX_ER                  | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDIO_DATA_IN_OUT28 | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_54                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| U14                | PRG1_PRU0_GPO10<br>PADCONFIG:<br>PADCONFIG56<br>0x000F40E0         | PRG1_PRU0_GPO10              | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI10              | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_UART0_RTSn              | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_B1                 | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMI11_TXC                   | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII_REF_CLK                 | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDIO_DATA_IN_OUT29 | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_55                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD26                   | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]    | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| AA8                | PRG1_PRU0_GPO11<br>PADCONFIG:<br>PADCONFIG57<br>0x000F40E4         | PRG1_PRU0_GPO11    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI11    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_TD0    | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM3_TZ_OUT   | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_56           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD27         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| U9                 | PRG1_PRU0_GPO12<br>PADCONFIG:<br>PADCONFIG58<br>0x000F40E8         | PRG1_PRU0_GPO12    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI12    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_TD1    | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM0_A0       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_57           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD28         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W9                 | PRG1_PRU0_GPO13<br>PADCONFIG:<br>PADCONFIG59<br>0x000F40EC         | PRG1_PRU0_GPO13    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI13    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_TD2    | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM0_B0       | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_58           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD29         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA9                | PRG1_PRU0_GPO14<br>PADCONFIG:<br>PADCONFIG60<br>0x000F40F0         | PRG1_PRU0_GPO14    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI14    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_TD3    | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM0_A1       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_59           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD30         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| Y9                 | PRG1_PRU0_GPO15<br>PADCONFIG:<br>PADCONFIG61<br>0x000F40F4         | PRG1_PRU0_GPO15    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI15    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_TX_CTL | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM0_B1       | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_60           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_AD31         | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V9                 | PRG1_PRU0_GPO16<br>PADCONFIG:<br>PADCONFIG62<br>0x000F40F8         | PRG1_PRU0_GPO16    | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI16    | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII1_TXC    | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM0_A2       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_61           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_BE2n         | 8               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]         | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| U7                 | PRG1_PRU0_GPO17<br>PADCONFIG:<br>PADCONFIG63<br>0x000F40FC         | PRG1_PRU0_GPO17         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI17         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDC_SYNC_OUT1 | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM0_B2            | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | CPTS0_TS_SYNC           | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO7               | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_62                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A0                | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| V7                 | PRG1_PRU0_GPO18<br>PADCONFIG:<br>PADCONFIG64<br>0x000F4100         | PRG1_PRU0_GPO18         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI18         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDC_LATCH_IN0 | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM0_TZ_IN         | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | CPTS0_HW1TSPUSH         | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO8               | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_63                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A1                | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| W7                 | PRG1_PRU0_GPO19<br>PADCONFIG:<br>PADCONFIG65<br>0x000F4104         | PRG1_PRU0_GPO19         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU0_GPI19         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDC_SYNC_OUT0 | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM0_TZ_OUT        | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | CPTS0_TS_COMP           | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO9               | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_64                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A2                | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| W11                | PRG1_PRU1_GPO0<br>PADCONFIG:<br>PADCONFIG66<br>0x000F4108          | PRG1_PRU1_GPO0          | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI0          | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_RGMII2_RD0         | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII2_RD0              | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RMII2_RXD0              | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_65                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A3                | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]    | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| V11                | PRG1_PRU1_GPO1<br>PADCONFIG:<br>PADCONFIG67<br>0x000F410C          | PRG1_PRU1_GPO1     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI1     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII2_RD1    | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII2_RD1         | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII2_RXD1         | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_66           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A4           | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA12               | PRG1_PRU1_GPO2<br>PADCONFIG:<br>PADCONFIG68<br>0x000F4110          | PRG1_PRU1_GPO2     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI2     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII2_RD2    | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_A2       | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII2_RD2         | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_67           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A5           | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| Y12                | PRG1_PRU1_GPO3<br>PADCONFIG:<br>PADCONFIG69<br>0x000F4114          | PRG1_PRU1_GPO3     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI3     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII2_RD3    | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII2_RD3         | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_68           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A6           | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W12                | PRG1_PRU1_GPO4<br>PADCONFIG:<br>PADCONFIG70<br>0x000F4118          | PRG1_PRU1_GPO4     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI4     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII2_RX_CTL | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_B2       | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII2_RX_CTL      | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII2_RX_ER        | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_69           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A7           | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA13               | PRG1_PRU1_GPO5<br>PADCONFIG:<br>PADCONFIG71<br>0x000F411C          | PRG1_PRU1_GPO5     | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI5     | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII1_RD0         | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_70           | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A8           | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]              | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| U11                | PRG1_PRU1_GPO6<br>PADCONFIG:<br>PADCONFIG72<br>0x000F4120          | PRG1_PRU1_GPO6               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI6               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_RGMII2_RXC              | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII2_RXC                   | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_71                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A9                     | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| V15                | PRG1_PRU1_GPO7<br>PADCONFIG:<br>PADCONFIG73<br>0x000F4124          | PRG1_PRU1_GPO7               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI7               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_IEP1_EDC_LATCH_IN1      | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII1_TD0                   | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RMII1_RXD0                   | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI3_CS3                     | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_72                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| U12                | PRG1_PRU1_GPO8<br>PADCONFIG:<br>PADCONFIG74<br>0x000F4128          | PRG1_PRU1_GPO8               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI8               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM2_TZ_OUT             | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII1_RD1                   | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_73                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A11                    | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| V14                | PRG1_PRU1_GPO9<br>PADCONFIG:<br>PADCONFIG75<br>0x000F412C          | PRG1_PRU1_GPO9               | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI9               | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_UART0_RXD               | 2               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII1_TD1                   | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RMII1_RXD1                   | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDIO_DATA_IN_OUT30 | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_74                     | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A12                    | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]              | MUX<br>MODE [4] | TYPE<br>[5] | DSIS<br>[6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------------|-----------------|-------------|-------------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| W14                | PRG1_PRU1_GPO10<br>PADCONFIG:<br>PADCONFIG76<br>0x000F4130         | PRG1_PRU1_GPO10              | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI10              | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_UART0_TXD               | 2               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM2_TZ_IN              | 3               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII1_TD2                   | 4               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII1_TXD0                   | 5               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDIO_DATA_IN_OUT31 | 6               | IO          | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_75                     | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| AA10               | PRG1_PRU1_GPO11<br>PADCONFIG:<br>PADCONFIG77<br>0x000F4134         | PRG1_PRU1_GPO11              | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI11              | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII2_TD0              | 2               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII2_TD0                   | 4               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII2_TXD0                   | 5               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_76                     | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V10                | PRG1_PRU1_GPO12<br>PADCONFIG:<br>PADCONFIG78<br>0x000F4138         | PRG1_PRU1_GPO12              | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI12              | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII2_TD1              | 2               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM1_A0                 | 3               | IO          | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII2_TD1                   | 4               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII2_TXD1                   | 5               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_77                     | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| U10                | PRG1_PRU1_GPO13<br>PADCONFIG:<br>PADCONFIG79<br>0x000F413C         | PRG1_PRU1_GPO13              | 0               | IO          | 0           | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI13              | 1               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_RGMII2_TD2              | 2               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM1_B0                 | 3               | IO          | 1           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII2_TD2                   | 4               | O           |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII2_CRS_DV                 | 5               | I           | 0           |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_78                     | 7               | IO          | pad         |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPMC0_A16                    | 8               | OZ          |             |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]         | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| AA11               | PRG1_PRU1_GPO14<br>PADCONFIG:<br>PADCONFIG80<br>0x000F4140         | PRG1_PRU1_GPO14         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI14         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_RGMII2_TD3         | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM1_A1            | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII2_TD3              | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_79                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A17               | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| Y11                | PRG1_PRU1_GPO15<br>PADCONFIG:<br>PADCONFIG81<br>0x000F4144         | PRG1_PRU1_GPO15         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI15         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_RGMII2_TX_CTL      | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM1_B1            | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII2_TX_CTL           | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RMII2_TX_EN             | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_80                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| Y10                | PRG1_PRU1_GPO16<br>PADCONFIG:<br>PADCONFIG82<br>0x000F4148         | PRG1_PRU1_GPO16         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI16         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_RGMII2_TXC         | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM1_A2            | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII2_TXC              | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_81                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_A19               | 8               | OZ       |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| AA14               | PRG1_PRU1_GPO17<br>PADCONFIG:<br>PADCONFIG83<br>0x000F414C         | PRG1_PRU1_GPO17         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI17         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_IEP1_EDC_SYNC_OUT1 | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_PWM1_B2            | 3               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RGMII1_TD3              | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | RMII1_TXD1              | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO0_19                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPMC0_BE3n              | 8               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | PRG1_ECAP0_SYNC_OUT     | 9               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]         | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| Y13                | PRG1_PRU1_GPO18<br>PADCONFIG:<br>PADCONFIG84<br>0x000F4150         | PRG1_PRU1_GPO18         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI18         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_IEP1_EDC_LATCH_IN0 | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM1_TZ_IN         | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII1_RD2              | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII1_TX_EN             | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_20                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART5_CTSn              | 8               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V12                | PRG1_PRU1_GPO19<br>PADCONFIG:<br>PADCONFIG85<br>0x000F4154         | PRG1_PRU1_GPO19         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV2    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | PRG1_PRU1_GPI19         | 1               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_IEP1_EDC_SYNC_OUT0 | 2               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_PWM1_TZ_OUT        | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RGMII1_RD3              | 4               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | RMII1_CRS_DV            | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | SPI3_CS2                | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO0_84                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| F16                | RESETSTATz<br>PADCONFIG:<br>PADCONFIG169<br>0x000F42A4             | RESETSTATz              | 0               | O        |          | Off / Low / Off                                    | Off / SS / Off                                    | 0                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | RESET_REQz              | 0               | I        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| E18                | RESET_REQz<br>PADCONFIG:<br>PADCONFIG168<br>0x000F42A0             | RESET_REQz              | 0               | I        |          | On / Off / Up                                      | On / Off / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
| H16                | RSVD0                                                              | RSVD0                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| D21                | RSVD1                                                              | RSVD1                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| G13                | RSVD2                                                              | RSVD2                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| F17                | RSVD3                                                              | RSVD3                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| W15                | RSVD4                                                              | RSVD4                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| V16                | RSVD5                                                              | RSVD5                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| K2                 | RSVD6                                                              | RSVD6                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| K1                 | RSVD7                                                              | RSVD7                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| F12                | RSVD8                                                              | RSVD8                   |                 | N/A      |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]  | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]                                                   | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|--------------------------------------------------------------|----------|---------------------|------------------------------|
| T13                | SERDES0_REXT                                                       | SERDES0_REXT     |                 | A        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_1P8_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C |          | SERDES              |                              |
| W16                | SERDES0_REFCLK0N                                                   | SERDES0_REFCLK0N |                 | IO       |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_1P8_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C |          | SERDES              |                              |
| W17                | SERDES0_REFCLK0P                                                   | SERDES0_REFCLK0P |                 | IO       |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_1P8_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C |          | SERDES              |                              |
| Y15                | SERDES0_RX0_N                                                      | SERDES0_RX0_N    |                 | I        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_1P8_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C |          | SERDES              |                              |
| Y16                | SERDES0_RX0_P                                                      | SERDES0_RX0_P    |                 | I        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_1P8_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C |          | SERDES              |                              |
| AA16               | SERDES0_TX0_N                                                      | SERDES0_TX0_N    |                 | O        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_1P8_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C |          | SERDES              |                              |
| AA17               | SERDES0_TX0_P                                                      | SERDES0_TX0_P    |                 | O        |          |                                                    |                                                   |                                      | 1.8 V                            | VDDA_1P8_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C |          | SERDES              |                              |
| D13                | SPI0_CLK<br>PADCONFIG:<br>PADCONFIG132<br>0x000F4210               | SPI0_CLK         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                                      | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO1_44         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                              |          |                     |                              |
| C14                | SPI1_CLK<br>PADCONFIG:<br>PADCONFIG137<br>0x000F4224               | SPI1_CLK         | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                                      | Yes      | LVCMOS              | PU/PD                        |
|                    |                                                                    | EHRPWM6_SYNCI    | 3               | I        | 0        |                                                    |                                                   |                                      |                                  |                                                              |          |                     |                              |
|                    |                                                                    | GPIO1_49         | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                              |          |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]         | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|-------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|-------------|---------------------|------------------------------|
| D12                | SPI0_CS0<br>PADCONFIG:<br>PADCONFIG130<br>0x000F4208               | SPI0_CS0                | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO1_42                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| C13                | SPI0_CS1<br>PADCONFIG:<br>PADCONFIG131<br>0x000F420C               | SPI0_CS1                | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | CPTS0_TS_COMP           | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | I2C2_SCL                | 2               | IOD      | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | TIMER_IO10              | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG0_IEP0_EDIO_OUTVALID | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART6_RXD               | 5               | I        | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | ADC_EXT_TRIGGER0        | 6               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| A13                | SPI0_D0<br>PADCONFIG:<br>PADCONFIG133<br>0x000F4214                | SPI0_D0                 | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO1_45                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| A14                | SPI0_D1<br>PADCONFIG:<br>PADCONFIG134<br>0x000F4218                | SPI0_D1                 | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | GPIO1_46                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| B14                | SPI1_CS0<br>PADCONFIG:<br>PADCONFIG135<br>0x000F421C               | SPI1_CS0                | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | EHRPWM6_A               | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_47                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| D14                | SPI1_CS1<br>PADCONFIG:<br>PADCONFIG136<br>0x000F4220               | SPI1_CS1                | 0               | IO       | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | CPTS0_TS_SYNC           | 1               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | I2C2_SDA                | 2               | IOD      | 1        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | PRG1_IEP0_EDIO_OUTVALID | 4               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | UART6_TXD               | 5               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | ADC_EXT_TRIGGER1        | 6               | I        | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_48                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| B15                | SPI1_D0<br>PADCONFIG:<br>PADCONFIG138<br>0x000F4228                | SPI1_D0                 | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | EHRPWM6_SYNC0           | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_50                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
| A15                | SPI1_D1<br>PADCONFIG:<br>PADCONFIG139<br>0x000F422C                | SPI1_D1                 | 0               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | EHRPWM6_B               | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |             |                     |                              |
|                    |                                                                    | GPIO1_51                | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |             |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]        | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| B11                | TCK<br>PADCONFIG:<br>MCU_PADCONFIG26<br>0x04084068                 | TCK                    | 0               | I        |          | On / Off / Up                                      | On / Off / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
| C11                | TDI<br>PADCONFIG:<br>MCU_PADCONFIG28<br>0x04084070                 | TDI                    | 0               | I        |          | On / Off / Up                                      | On / Off / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
| A12                | TDO<br>PADCONFIG:<br>MCU_PADCONFIG29<br>0x04084074                 | TDO                    | 0               | OZ       |          | Off / Off / Up                                     | Off / SS / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
| C12                | TMS<br>PADCONFIG:<br>MCU_PADCONFIG30<br>0x04084078                 | TMS                    | 0               | I        |          | On / Off / Up                                      | On / Off / Up                                     | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
| D11                | TRSTn<br>PADCONFIG:<br>MCU_PADCONFIG27<br>0x0408406C               | TRSTn                  | 0               | I        |          | On / Off / Down                                    | On / Off / Down                                   | 0                                    | 1.8 V/3.3 V                      | VDDSHV_MCU | Yes      | LVC MOS             | PU/PD                        |
| B16                | UART0_CTSn<br>PADCONFIG:<br>PADCONFIG142<br>0x000F4238             | UART0_CTSn             | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | SPI0_CS2               | 1               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | ADC_EXT_TRIGGER0       | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART2_RXD              | 3               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO6              | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI4_CLK               | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_54               | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP0_S                | 8               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| A16                | UART0_RTSn<br>PADCONFIG:<br>PADCONFIG143<br>0x000F423C             | CP_GEMAC_CPTS0_TS_SYNC | 9               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | UART0_RTSn             | 0               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI0_CS3               | 1               | IO       | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | UART2_TXD              | 3               | O        |          |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | TIMER_IO7              | 4               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI4_D0                | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_55               | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| D15                | UART0_RXD<br>PADCONFIG:<br>PADCONFIG140<br>0x000F4230              | EQEP0_I                | 8               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | UART0_RXD              | 0               | I        | 1        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | SPI2_D0                | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | GPIO1_52               | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
| D15                | EQEP0_A                                                            | EQEP0_A                | 8               | I        | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0    | Yes      | LVC MOS             | PU/PD                        |
|                    |                                                                    | EQEP0_A                | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP0_A                | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |
|                    |                                                                    | EQEP0_A                | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |            |          |                     |                              |

**表 5-1. Pin Attributes (ALV Package) (続き)**

| BALL<br>NUMBER [1] | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]          | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]                                         | HYS<br>[12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|--------------------|--------------------------------------------------------------------|--------------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|----------------------------------------------------|-------------|---------------------|------------------------------|
| C16                | UART0_TXD<br>PADCONFIG:<br>PADCONFIG141<br>0x000F4234              | UART0_TXD                | 0               | O        |          | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                            | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | SPI2_D1                  | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | GPIO1_53                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | EQEP0_B                  | 8               | I        | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
| D16                | UART1_CTSn<br>PADCONFIG:<br>PADCONFIG146<br>0x000F4248             | UART1_CTSn               | 0               | I        | 1        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                            | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | SPI1_CS2                 | 1               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | ADC_EXT_TRIGGER1         | 2               | I        | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | PCIE0_CLKREQn            | 3               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | UART3_RXD                | 4               | I        | 1        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_TS_SYNC   | 5               | O        |          |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | SPI4_D1                  | 6               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | GPIO1_58                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
| E16                | UART1_RTSn<br>PADCONFIG:<br>PADCONFIG147<br>0x000F424C             | EQEP1_S                  | 8               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                            | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | UART1_RTSn               | 0               | O        |          |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | SPI1_CS3                 | 1               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | UART3_TXD                | 4               | O        |          |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_HW2TSPUSH | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | SPI4_CS0                 | 6               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | GPIO1_59                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
| E15                | UART1_RXD<br>PADCONFIG:<br>PADCONFIG144<br>0x000F4240              | EQEP1_I                  | 8               | IO       | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                            | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | UART1_RXD                | 0               | I        | 1        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | SPI2_CS0                 | 2               | IO       | 1        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_TS_COMP   | 5               | O        |          |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | GPIO1_56                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
| E14                | UART1_TXD<br>PADCONFIG:<br>PADCONFIG145<br>0x000F4244              | EQEP1_A                  | 8               | I        | 0        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                            | Yes         | LVCMOS              | PU/PD                        |
|                    |                                                                    | UART1_TXD                | 0               | O        |          |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | SPI2_CLK                 | 2               | IO       | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | CP_GEMAC_CPTS0_HW1TSPUSH | 5               | I        | 0        |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
|                    |                                                                    | GPIO1_57                 | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
| AA20               | USB0_DM                                                            | EQEP1_B                  | 8               | I        | 0        |                                                    |                                                   |                                      | 1.8 V/3.3 V                      | VDDA_3P3_USB0,<br>VDDA_1P8_USB0,<br>VDDA_0P85_USB0 |             | USB2PHY             |                              |
|                    |                                                                    | USB0_DM                  |                 | IO       |          |                                                    |                                                   |                                      |                                  |                                                    |             |                     |                              |
| AA19               | USB0_DP                                                            | USB0_DP                  |                 | IO       |          |                                                    |                                                   |                                      | 1.8 V/3.3 V                      | VDDA_3P3_USB0,<br>VDDA_1P8_USB0,<br>VDDA_0P85_USB0 |             | USB2PHY             |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1]        | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3]     | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET<br>[9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11]                                         | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|---------------------------|--------------------------------------------------------------------|---------------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|--------------------------------------|----------------------------------|----------------------------------------------------|----------|---------------------|------------------------------|
| E19                       | USB0_DRVVBUS<br>PADCONFIG:<br>PADCONFIG170<br>0x000F42A8           | USB0_DRVVBUS        | 0               | O        |          | Off / Off / Down                                   | Off / Off / Down                                  | 7                                    | 1.8 V/3.3 V                      | VDDSHV0                                            | Yes      | LVC MOS             | PU/PD                        |
|                           |                                                                    | GPIO1_79            | 7               | IO       | pad      |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| U16                       | USB0_ID                                                            | USB0_ID             |                 | A        |          |                                                    |                                                   |                                      | 1.8 V/3.3 V                      | VDDA_3P3_USB0,<br>VDDA_1P8_USB0,<br>VDDA_0P85_USB0 |          | USB2PHY             |                              |
| U17                       | USB0_RCALIB                                                        | USB0_RCALIB         |                 | A        |          |                                                    |                                                   |                                      | 1.8 V/3.3 V                      | VDDA_3P3_USB0,<br>VDDA_1P8_USB0,<br>VDDA_0P85_USB0 |          | USB2PHY             |                              |
| T14                       | USB0_VBUS                                                          | USB0_VBUS           |                 | A        |          |                                                    |                                                   |                                      | 1.8 V/3.3 V                      | VDDA_3P3_USB0,<br>VDDA_1P8_USB0,<br>VDDA_0P85_USB0 |          | USB2PHY             |                              |
| P12, P13                  | VDDA_0P85_SERDES0                                                  | VDDA_0P85_SERDES0   |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| P11                       | VDDA_0P85_SERDES0_C                                                | VDDA_0P85_SERDES0_C |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| T12                       | VDDA_0P85_USB0                                                     | VDDA_0P85_USB0      |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| R14                       | VDDA_1P8_SERDES0                                                   | VDDA_1P8_SERDES0    |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| R15                       | VDDA_1P8_USB0                                                      | VDDA_1P8_USB0       |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| H15                       | VDDA_3P3_SDIO                                                      | VDDA_3P3_SDIO       |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| R13                       | VDDA_3P3_USB0                                                      | VDDA_3P3_USB0       |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| J13                       | VDDA_ADC                                                           | VDDA_ADC            |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| K12                       | VDDA_MCU                                                           | VDDA_MCU            |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| N12                       | VDDA_PLL0                                                          | VDDA_PLL0           |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| H9                        | VDDA_PLL1                                                          | VDDA_PLL1           |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| J11                       | VDDA_PLL2                                                          | VDDA_PLL2           |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| G11                       | VDDA_TEMP0                                                         | VDDA_TEMP0          |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| L11                       | VDDA_TEMP1                                                         | VDDA_TEMP1          |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| L10, M13                  | VDDR_CORE                                                          | VDDR_CORE           |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| F11, G12,<br>G14          | VDDSHV0                                                            | VDDSHV0             |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| M7, N6, P7                | VDDSHV1                                                            | VDDSHV1             |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| R10, R8, T9               | VDDSHV2                                                            | VDDSHV2             |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| P14, P15                  | VDDSHV3                                                            | VDDSHV3             |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| M14, M15                  | VDDSHV4                                                            | VDDSHV4             |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| L14, L15                  | VDDSHV5                                                            | VDDSHV5             |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| F9, G10, G8               | VDDSHV_MCU                                                         | VDDSHV_MCU          |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| F7, G6, H7,<br>J6, K7, L6 | VDDS_DDR                                                           | VDDS_DDR            |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| J8                        | VDDS_DDR_C                                                         | VDDS_DDR_C          |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |
| K14                       | VDDS_MMC0                                                          | VDDS_MMC0           |                 | PWR      |          |                                                    |                                                   |                                      |                                  |                                                    |          |                     |                              |

表 5-1. Pin Attributes (ALV Package) (続き)

| BALL<br>NUMBER [1]                                                                                                                                                                                                                                                                                                                                                                      | BALL NAME [2]<br>PADCONFIG Register [15]<br>PADCONFIG Address [16] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | DSIS [6] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | I/O<br>OPERATING<br>VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER<br>TYPE [13] | PULL<br>UP/DOWN<br>TYPE [14] |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|-----------------|-----------------|----------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|----------------------------------|------------|----------|---------------------|------------------------------|
| H13                                                                                                                                                                                                                                                                                                                                                                                     | VDDS_OSC                                                           | VDDS_OSC        |                 | PWR      |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| J10, J12,<br>K11, K9, L12,<br>L8, M11, M9,<br>N10, N8, P9                                                                                                                                                                                                                                                                                                                               | VDD_CORE                                                           | VDD_CORE        |                 | PWR      |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| H14                                                                                                                                                                                                                                                                                                                                                                                     | VDD_DLL_MMC0                                                       | VDD_DLL_MMC0    |                 | PWR      |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| K13                                                                                                                                                                                                                                                                                                                                                                                     | VDD_MMC0                                                           | VDD_MMC0        |                 | PWR      |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| K16                                                                                                                                                                                                                                                                                                                                                                                     | VMON_1P8_MCU                                                       | VMON_1P8_MCU    |                 | A        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| E12                                                                                                                                                                                                                                                                                                                                                                                     | VMON_1P8_SOC                                                       | VMON_1P8_SOC    |                 | A        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| F13                                                                                                                                                                                                                                                                                                                                                                                     | VMON_3P3_MCU                                                       | VMON_3P3_MCU    |                 | A        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| F14                                                                                                                                                                                                                                                                                                                                                                                     | VMON_3P3_SOC                                                       | VMON_3P3_SOC    |                 | A        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| K10                                                                                                                                                                                                                                                                                                                                                                                     | VMON_VSYS                                                          | VMON_VSYS       |                 | A        |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| G15                                                                                                                                                                                                                                                                                                                                                                                     | VPP                                                                | VPP             |                 | PWR      |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |
| A1, A21, A5,<br>A6, AA1,<br>AA15, AA18,<br>AA21, C10,<br>C15, C3, D1,<br>E11, E13,<br>F10, F15, F8,<br>G1, G16, G3,<br>G7, G9, H11,<br>H20, H21,<br>H6, H8, J14,<br>J7, J9, K6,<br>K8, L1, L16,<br>L3, L7, L9,<br>M10, M12,<br>M6, M8, N11,<br>N13, N15,<br>N7, N9, P1,<br>P10, P18, P6,<br>P8, R12, R7,<br>R9, T10, T11,<br>T15, T16, T8,<br>U3, V17,<br>W10, W18,<br>Y14, Y17,<br>Y19 | VSS                                                                | VSS             |                 | GND      |          |                                                    |                                                   |                                   |                                  |            |          |                     |                              |

## 5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

### 注

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:

- I = Input
- O = Output
- OD = Output, with open-drain output function
- IO = Input, Output, or simultaneously Input and Output
- IOD = Input, Output, or simultaneously Input and Output with open-drain output function
- IOZ = Input, Output, or simultaneously Input and Output with three-state output function
- OZ = Output with three-state output function
- A = Analog
- PWR = Power
- GND = Ground
- CAP = LDO Capacitor

3. **DESCRIPTION:** Description of the signal

4. **BALL:** Ball number(s) associated with signal

For more information on the IO cell configurations, see the *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM.

### 5.3.1 ADC

### 注

The ADC can be configured to operate as eight general-purpose digital inputs. For more information, see Analog-to-Digital Converter (ADC) section in Peripherals chapter in the device TRM.

#### 5.3.1.1 MAIN Domain

表 5-2. ADC0 Signal Descriptions

| SIGNAL NAME [1]                  | PIN TYPE [2] | DESCRIPTION [3]                            | ALV PIN [4] |
|----------------------------------|--------------|--------------------------------------------|-------------|
| ADC0_REFN <sup>(4)</sup>         | A            | ADC0 Negative Reference                    | J16         |
| ADC0_REFP <sup>(4)</sup>         | A            | ADC0 Positive Reference                    | J15         |
| ADC0_AIN0 <sup>(1) (2) (3)</sup> | A            | ADC Analog Input 0 / GPIO1_80 (Input Only) | G20         |
| ADC0_AIN1 <sup>(1) (2) (3)</sup> | A            | ADC Analog Input 1 / GPIO1_81 (Input Only) | F20         |
| ADC0_AIN2 <sup>(1) (2) (3)</sup> | A            | ADC Analog Input 2 / GPIO1_82 (Input Only) | E21         |
| ADC0_AIN3 <sup>(1) (2) (3)</sup> | A            | ADC Analog Input 3 / GPIO1_83 (Input Only) | D20         |
| ADC0_AIN4 <sup>(1) (2) (3)</sup> | A            | ADC Analog Input 4 / GPIO1_84 (Input Only) | G21         |
| ADC0_AIN5 <sup>(1) (2) (3)</sup> | A            | ADC Analog Input 5 / GPIO1_85 (Input Only) | F21         |

表 5-2. ADC0 Signal Descriptions (続き)

| SIGNAL NAME [1]       | PIN TYPE [2] | DESCRIPTION [3]                            | ALV PIN [4] |
|-----------------------|--------------|--------------------------------------------|-------------|
| ADC0_AIN6 (1) (2) (3) | A            | ADC Analog Input 6 / GPIO1_86 (Input Only) | F19         |
| ADC0_AIN7 (1) (2) (3) | A            | ADC Analog Input 7 / GPIO1_87 (Input Only) | E20         |
| ADC_EXT_TRIGGER0      | I            | ADC Trigger Input                          | B16, C13    |
| ADC_EXT_TRIGGER1      | I            | ADC Trigger Input                          | D14, D16    |

- (1) The General Purpose Input signal associated with this ADC0\_AIN input has a debounce function when ADC0 is configured to operate in GPI mode. For more information on configuring ADC0 to operate in GPI mode, see the TRM *Analog-to-Digital Converter (ADC)* section in the *Peripherals* chapter. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.
- (2) The ADC0\_AIN[7:0] inputs only have hysteresis when ADC0 is configured to operate in GPI mode.
- (3) Any unused ADC0\_AIN inputs must be pulled to VSS through a resistor or connected directly to VSS when VDDA\_ADC is connected to a power source.
- (4) The ADC0\_REFP and ADC0\_REFN reference inputs are analog inputs which must be treated like high transient power supply rails, where ADC0\_REFN is expected to be connected directly to the PCB ground plane along with all other VSS pins, and ADC0\_REFP is connected to a power source capable of providing at least 4mA of current. ADC0\_REFP may be connected to the same power source as VDDA\_ADC if the voltage tolerance of the supply provides an acceptable accuracy for the ADC reference. A high frequency decoupling capacitor must be connected directly between ADC0\_REFP and ADC0\_REFN. The high frequency decoupling capacitor should be placed in the ball array on the back side of the PCB and connected directly to the ADC0\_REFP and ADC0\_REFN pins with vias. ADC0\_REFP may be connected to VSS if ADC0 is not used and VDDA\_ADC has been connected to VSS. The high frequency decoupling capacitor described above will not be required if ADC0 is not used and ADC0\_REFP is connected to VSS. See the *Pin Connectivity Requirements* section for more information on ADC0 connectivity.

### 5.3.2 CPSW3G

#### 5.3.2.1 MAIN Domain

表 5-3. CPSW3G0 RGMII1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ALV PIN [4] |
|-----------------|--------------|------------------------|-------------|
| RGMII1_RXC      | I            | RGMII Receive Clock    | AA5, W13    |
| RGMII1_RX_CTL   | I            | RGMII Receive Control  | V13, W6     |
| RGMII1_TXC      | IO           | RGMII Transmit Clock   | U14         |
| RGMII1_TX_CTL   | O            | RGMII Transmit Control | U15         |
| RGMII1_RD0      | I            | RGMII Receive Data 0   | AA13, W5    |
| RGMII1_RD1      | I            | RGMII Receive Data 1   | U12, Y5     |
| RGMII1_RD2      | I            | RGMII Receive Data 2   | V6, Y13     |
| RGMII1_RD3      | I            | RGMII Receive Data 3   | V12, V5     |
| RGMII1_TD0      | O            | RGMII Transmit Data 0  | V15         |
| RGMII1_TD1      | O            | RGMII Transmit Data 1  | V14         |
| RGMII1_TD2      | O            | RGMII Transmit Data 2  | W14         |
| RGMII1_TD3      | O            | RGMII Transmit Data 3  | AA14        |

表 5-4. CPSW3G0 RGMII2 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ALV PIN [4] |
|-----------------|--------------|------------------------|-------------|
| RGMII2_RXC      | I            | RGMII Receive Clock    | U11         |
| RGMII2_RX_CTL   | I            | RGMII Receive Control  | W12         |
| RGMII2_TXC      | IO           | RGMII Transmit Clock   | Y10         |
| RGMII2_TX_CTL   | O            | RGMII Transmit Control | Y11         |
| RGMII2_RD0      | I            | RGMII Receive Data 0   | W11         |
| RGMII2_RD1      | I            | RGMII Receive Data 1   | V11         |
| RGMII2_RD2      | I            | RGMII Receive Data 2   | AA12        |
| RGMII2_RD3      | I            | RGMII Receive Data 3   | Y12         |
| RGMII2_TD0      | O            | RGMII Transmit Data 0  | AA10        |
| RGMII2_TD1      | O            | RGMII Transmit Data 1  | V10         |

表 5-4. CPSW3G0 RGMII2 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]       | ALV PIN [4] |
|-----------------|--------------|-----------------------|-------------|
| RGMII2_TD2      | O            | RGMII Transmit Data 2 | U10         |
| RGMII2_TD3      | O            | RGMII Transmit Data 3 | AA11        |

表 5-5. CPSW3G0 RMII1 and RMII2 Signal Descriptions

| SIGNAL NAME [1]             | PIN TYPE [2] | DESCRIPTION [3]                 | ALV PIN [4] |
|-----------------------------|--------------|---------------------------------|-------------|
| RMII1_CRS_DV                | I            | RMII Carrier Sense / Data Valid | R2, V12     |
| RMII1_RX_ER                 | I            | RMII Receive Data Error         | U15, W6     |
| RMII1_TX_EN                 | O            | RMII Transmit Enable            | P5, Y13     |
| RMII2_CRS_DV                | I            | RMII Carrier Sense / Data Valid | U10         |
| RMII2_RX_ER                 | I            | RMII Receive Data Error         | W12         |
| RMII2_TX_EN                 | O            | RMII Transmit Enable            | Y11         |
| RMII1_RXD0                  | I            | RMII Receive Data 0             | V15, W5     |
| RMII1_RXD1                  | I            | RMII Receive Data 1             | V14, Y5     |
| RMII1_TXD0                  | O            | RMII Transmit Data 0            | V6, W14     |
| RMII1_TXD1                  | O            | RMII Transmit Data 1            | AA14, V5    |
| RMII2_RXD0                  | I            | RMII Receive Data 0             | W11         |
| RMII2_RXD1                  | I            | RMII Receive Data 1             | V11         |
| RMII2_TXD0                  | O            | RMII Transmit Data 0            | AA10        |
| RMII2_TXD1                  | O            | RMII Transmit Data 1            | V10         |
| RMII_REF_CLK <sup>(1)</sup> | I            | RMII Reference Clock            | AA5, U14    |

(1) RMII\_REF\_CLK is common to both RMII1 and RMII2.

### 5.3.3 CPTS

#### 5.3.3.1 MAIN Domain

表 5-6. CP GEMAC CPTS0 Signal Descriptions

| SIGNAL NAME [1]          | PIN TYPE [2] | DESCRIPTION [3]                                          | ALV PIN [4]       |
|--------------------------|--------------|----------------------------------------------------------|-------------------|
| CP_GEMAC_CPTS0_RFT_CLK   | I            | CPTS Reference Clock Input to CPSW3G0 CPTS               | D18               |
| CP_GEMAC_CPTS0_TS_COMP   | O            | CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS | E15, K18, W1      |
| CP_GEMAC_CPTS0_TS_SYNC   | O            | CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS     | B16, D16, K19, U1 |
| CP_GEMAC_CPTS0_HW1TSPUSH | I            | CPTS Hardware Time Stamp Push Input to CPSW3G0 CPTS      | E14, L21, V1      |
| CP_GEMAC_CPTS0_HW2TSPUSH | I            | CPTS Hardware Time Stamp Push Input to CPSW3G0 CPTS      | E16, K21, T1      |

表 5-7. CPTS0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4]  |
|-----------------|--------------|--------------------------------------------------------------|--------------|
| CPTS0_RFT_CLK   | I            | CPTS Reference Clock Input                                   | D18          |
| CPTS0_TS_COMP   | O            | CPTS Time Stamp Counter Compare Output                       | C13, W1, W7  |
| CPTS0_TS_SYNC   | O            | CPTS Time Stamp Counter Bit Output                           | D14, U1, U7  |
| CPTS0_HW1TSPUSH | I            | CPTS Hardware Time Stamp Push Input to Time Sync Router      | C18, V1, V7  |
| CPTS0_HW2TSPUSH | I            | CPTS Hardware Time Stamp Push Input to Time Sync Router      | B19, T1, U13 |
| SYNC0_OUT       | O            | CPTS Time Stamp Generator Bit 0 Output from Time Sync Router | D18          |

表 5-7. CPTS0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------------------------|-------------|
| SYNC1_OUT       | O            | CPTS Time Stamp Generator Bit 1 Output from Time Sync Router | A19         |
| SYNC2_OUT       | O            | CPTS Time Stamp Generator Bit 2 Output from Time Sync Router | A17         |
| SYNC3_OUT       | O            | CPTS Time Stamp Generator Bit 3 Output from Time Sync Router | B17         |

### 5.3.4 DDRSS

#### 5.3.4.1 MAIN Domain

表 5-8. DDRSS0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALV PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| DDR0_ACT_n      | O            | DDRSS Activation Command         | H2          |
| DDR0_ALERT_n    | IO           | DDRSS Alert                      | H1          |
| DDR0_CAS_n      | O            | DDRSS Column Address Strobe      | J5          |
| DDR0_PAR        | O            | DDRSS Command and Address Parity | K5          |
| DDR0_RAS_n      | O            | DDRSS Row Address Strobe         | F6          |
| DDR0_WE_n       | O            | DDRSS Write Enable               | H4          |
| DDR0_A0         | O            | DDRSS Address Bus                | D2          |
| DDR0_A1         | O            | DDRSS Address Bus                | C5          |
| DDR0_A2         | O            | DDRSS Address Bus                | E2          |
| DDR0_A3         | O            | DDRSS Address Bus                | D4          |
| DDR0_A4         | O            | DDRSS Address Bus                | D3          |
| DDR0_A5         | O            | DDRSS Address Bus                | F2          |
| DDR0_A6         | O            | DDRSS Address Bus                | J2          |
| DDR0_A7         | O            | DDRSS Address Bus                | L5          |
| DDR0_A8         | O            | DDRSS Address Bus                | J3          |
| DDR0_A9         | O            | DDRSS Address Bus                | J4          |
| DDR0_A10        | O            | DDRSS Address Bus                | K3          |
| DDR0_A11        | O            | DDRSS Address Bus                | J1          |
| DDR0_A12        | O            | DDRSS Address Bus                | M5          |
| DDR0_A13        | O            | DDRSS Address Bus                | K4          |
| DDR0_BA0        | O            | DDRSS Bank Address               | G4          |
| DDR0_BA1        | O            | DDRSS Bank Address               | G5          |
| DDR0_BG0        | O            | DDRSS Bank Group                 | G2          |
| DDR0_BG1        | O            | DDRSS Bank Group                 | H3          |
| DDR0_CAL0 (1)   | A            | IO Pad Calibration Resistor      | H5          |
| DDR0_CK0        | O            | DDRSS Clock                      | F1          |
| DDR0_CK0_n      | O            | DDRSS Negative Clock             | E1          |
| DDR0_CKE0       | O            | DDRSS Clock Enable               | F4          |
| DDR0_CKE1       | O            | DDRSS Clock Enable               | F3          |
| DDR0_CS0_n      | O            | DDRSS Chip Select 0              | E3          |
| DDR0_CS1_n      | O            | DDRSS Chip Select 1              | E4          |
| DDR0_DM0        | IO           | DDRSS Data Mask                  | B2          |
| DDR0_DM1        | IO           | DDRSS Data Mask                  | M2          |
| DDR0_DQ0        | IO           | DDRSS Data                       | A3          |
| DDR0_DQ1        | IO           | DDRSS Data                       | A2          |

表 5-8. DDRSS0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                            | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------|-------------|
| DDR0_DQ2        | IO           | DDRSS Data                                 | B5          |
| DDR0_DQ3        | IO           | DDRSS Data                                 | A4          |
| DDR0_DQ4        | IO           | DDRSS Data                                 | B3          |
| DDR0_DQ5        | IO           | DDRSS Data                                 | C4          |
| DDR0_DQ6        | IO           | DDRSS Data                                 | C2          |
| DDR0_DQ7        | IO           | DDRSS Data                                 | B4          |
| DDR0_DQ8        | IO           | DDRSS Data                                 | N5          |
| DDR0_DQ9        | IO           | DDRSS Data                                 | L4          |
| DDR0_DQ10       | IO           | DDRSS Data                                 | L2          |
| DDR0_DQ11       | IO           | DDRSS Data                                 | M3          |
| DDR0_DQ12       | IO           | DDRSS Data                                 | N4          |
| DDR0_DQ13       | IO           | DDRSS Data                                 | N3          |
| DDR0_DQ14       | IO           | DDRSS Data                                 | M4          |
| DDR0_DQ15       | IO           | DDRSS Data                                 | N2          |
| DDR0_DQS0       | IO           | DDRSS Data Strobe 0                        | C1          |
| DDR0_DQS0_n     | IO           | DDRSS Complimentary Data Strobe 0          | B1          |
| DDR0_DQS1       | IO           | DDRSS Data Strobe 1                        | N1          |
| DDR0_DQS1_n     | IO           | DDRSS Complimentary Data Strobe 1          | M1          |
| DDR0_ODT0       | O            | DDRSS On-Die Termination for Chip Select 0 | E5          |
| DDR0_ODT1       | O            | DDRSS On-Die Termination for Chip Select 1 | F5          |
| DDR0_RESET0_n   | O            | DDRSS Reset                                | D5          |

- (1) An external 240 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage should be applied to this pin.

### 5.3.5 ECAP

#### 5.3.5.1 MAIN Domain

表 5-9. ECAP0 Signal Descriptions

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP0_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | D18         |

表 5-10. ECAP1 Signal Descriptions

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP1_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | C17         |

表 5-11. ECAP2 Signal Descriptions

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP2_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | D17         |

### 5.3.6 Emulation and Debug

#### 5.3.6.1 MAIN Domain

表 5-12. Trace Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| TRC_CLK         | O            | Trace Clock     | T20         |

表 5-12. Trace Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| TRC_CTL         | O            | Trace Control   | U21         |
| TRC_DATA0       | O            | Trace Data 0    | T18         |
| TRC_DATA1       | O            | Trace Data 1    | U20         |
| TRC_DATA2       | O            | Trace Data 2    | U18         |
| TRC_DATA3       | O            | Trace Data 3    | U19         |
| TRC_DATA4       | O            | Trace Data 4    | V20         |
| TRC_DATA5       | O            | Trace Data 5    | V21         |
| TRC_DATA6       | O            | Trace Data 6    | V19         |
| TRC_DATA7       | O            | Trace Data 7    | T17         |
| TRC_DATA8       | O            | Trace Data 8    | R16         |
| TRC_DATA9       | O            | Trace Data 9    | W20         |
| TRC_DATA10      | O            | Trace Data 10   | W21         |
| TRC_DATA11      | O            | Trace Data 11   | V18         |
| TRC_DATA12      | O            | Trace Data 12   | Y21         |
| TRC_DATA13      | O            | Trace Data 13   | Y20         |
| TRC_DATA14      | O            | Trace Data 14   | R17         |
| TRC_DATA15      | O            | Trace Data 15   | P16         |
| TRC_DATA16      | O            | Trace Data 16   | R18         |
| TRC_DATA17      | O            | Trace Data 17   | T21         |
| TRC_DATA18      | O            | Trace Data 18   | P17         |
| TRC_DATA19      | O            | Trace Data 19   | T19         |
| TRC_DATA20      | O            | Trace Data 20   | W19         |
| TRC_DATA21      | O            | Trace Data 21   | Y18         |
| TRC_DATA22      | O            | Trace Data 22   | N16         |
| TRC_DATA23      | O            | Trace Data 23   | R19         |

### 5.3.6.2 MCU Domain

表 5-13. JTAG Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]             | ALV PIN [4] |
|-----------------|--------------|-----------------------------|-------------|
| EMU0            | IO           | Emulation Control 0         | D10         |
| EMU1            | IO           | Emulation Control 1         | E10         |
| TCK             | I            | JTAG Test Clock Input       | B11         |
| TDI             | I            | JTAG Test Data Input        | C11         |
| TDO             | OZ           | JTAG Test Data Output       | A12         |
| TMS             | I            | JTAG Test Mode Select Input | C12         |
| TRSTn           | I            | JTAG Reset                  | D11         |

### 5.3.7 EPWM

#### 5.3.7.1 MAIN Domain

表 5-14. EPWM Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALV PIN [4] |
|-----------------|--------------|---------------------------------------|-------------|
| EHRPWM_SOC_A    | O            | EHRPWM Start of Conversion A          | C17         |
| EHRPWM_SOC_B    | O            | EHRPWM Start of Conversion B          | D17         |
| EHRPWM_TZn_IN0  | I            | EHRPWM Trip Zone Input 0 (active low) | T18         |
| EHRPWM_TZn_IN1  | I            | EHRPWM Trip Zone Input 1 (active low) | V21         |

表 5-14. EPWM Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALV PIN [4] |
|-----------------|--------------|---------------------------------------|-------------|
| EHRPWM_TZn_IN2  | I            | EHRPWM Trip Zone Input 2 (active low) | R16, R20    |
| EHRPWM_TZn_IN3  | I            | EHRPWM Trip Zone Input 3 (active low) | P16         |
| EHRPWM_TZn_IN4  | I            | EHRPWM Trip Zone Input 4 (active low) | P17, P19    |
| EHRPWM_TZn_IN5  | I            | EHRPWM Trip Zone Input 5 (active low) | R21, Y18    |

表 5-15. EPWM0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------------|-------------|
| EHRPWM0_A       | IO           | EHRPWM Output A                                  | U20         |
| EHRPWM0_B       | IO           | EHRPWM Output B                                  | U18         |
| EHRPWM0_SYNCI   | I            | Sync Input to EHRPWM module from an external pin | T20         |
| EHRPWM0_SYNCO   | O            | Sync Output to EHRPWM module to an external pin  | U21         |

表 5-16. EPWM1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM1_A       | IO           | EHRPWM Output A | U19         |
| EHRPWM1_B       | IO           | EHRPWM Output B | V20         |

表 5-17. EPWM2 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM2_A       | IO           | EHRPWM Output A | V19         |
| EHRPWM2_B       | IO           | EHRPWM Output B | T17         |

表 5-18. EPWM3 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------------|-------------|
| EHRPWM3_A       | IO           | EHRPWM Output A                                  | V18         |
| EHRPWM3_B       | IO           | EHRPWM Output B                                  | Y21         |
| EHRPWM3_SYNCI   | I            | Sync Input to EHRPWM module from an external pin | Y20         |
| EHRPWM3_SYNCO   | O            | Sync Output to EHRPWM module to an external pin  | R17         |

表 5-19. EPWM4 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM4_A       | IO           | EHRPWM Output A | R18         |
| EHRPWM4_B       | IO           | EHRPWM Output B | T21         |

表 5-20. EPWM5 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM5_A       | IO           | EHRPWM Output A | T19         |
| EHRPWM5_B       | IO           | EHRPWM Output B | W19         |

表 5-21. EPWM6 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------------|-------------|
| EHRPWM6_A       | IO           | EHRPWM Output A                                  | B14, N16    |
| EHRPWM6_B       | IO           | EHRPWM Output B                                  | A15, N17    |
| EHRPWM6_SYNCI   | I            | Sync Input to EHRPWM module from an external pin | C14, R19    |

表 5-21. EPWM6 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                 | ALV PIN [4] |
|-----------------|--------------|-------------------------------------------------|-------------|
| EHRPWM6_SYNCO   | O            | Sync Output to EHRPWM module to an external pin | B15, R20    |

表 5-22. EPWM7 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4]  |
|-----------------|--------------|-----------------|--------------|
| EHRPWM7_A       | IO           | EHRPWM Output A | P17, P5, W20 |
| EHRPWM7_B       | IO           | EHRPWM Output B | R2, W21, Y18 |

表 5-23. EPWM8 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM8_A       | IO           | EHRPWM Output A | V1, V21     |
| EHRPWM8_B       | IO           | EHRPWM Output B | R16, W1     |

### 5.3.8 EQEP

#### 5.3.8.1 MAIN Domain

表 5-24. EQEP0 Signal Descriptions

| SIGNAL NAME [1]        | PIN TYPE [2] | DESCRIPTION [3]         | ALV PIN [4]      |
|------------------------|--------------|-------------------------|------------------|
| EQEP0_A <sup>(1)</sup> | I            | EQEP Quadrature Input A | D15, N16, Y2     |
| EQEP0_B <sup>(1)</sup> | I            | EQEP Quadrature Input B | C16, N17, W2     |
| EQEP0_I <sup>(1)</sup> | IO           | EQEP Index              | A16, R20, T6, Y5 |
| EQEP0_S <sup>(1)</sup> | IO           | EQEP Strobe             | B16, R19, V3     |

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 5-25. EQEP1 Signal Descriptions

| SIGNAL NAME [1]        | PIN TYPE [2] | DESCRIPTION [3]         | ALV PIN [4]      |
|------------------------|--------------|-------------------------|------------------|
| EQEP1_A <sup>(1)</sup> | I            | EQEP Quadrature Input A | E15, T4, W20     |
| EQEP1_B <sup>(1)</sup> | I            | EQEP Quadrature Input B | E14, W21, W3     |
| EQEP1_I <sup>(1)</sup> | IO           | EQEP Index              | E16, R21, U6, V6 |
| EQEP1_S <sup>(1)</sup> | IO           | EQEP Strobe             | D16, P19, P4     |

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 5-26. EQEP2 Signal Descriptions

| SIGNAL NAME [1]        | PIN TYPE [2] | DESCRIPTION [3]         | ALV PIN [4] |
|------------------------|--------------|-------------------------|-------------|
| EQEP2_A <sup>(1)</sup> | I            | EQEP Quadrature Input A | C17, R5     |
| EQEP2_B <sup>(1)</sup> | I            | EQEP Quadrature Input B | D17, W5, Y4 |
| EQEP2_I <sup>(1)</sup> | IO           | EQEP Index              | A17, W4     |
| EQEP2_S <sup>(1)</sup> | IO           | EQEP Strobe             | B17, R1     |

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

## 5.3.9 FSI

### 5.3.9.1 MAIN Domain

表 5-27. FSI0 RX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_RX0_CLK     | I            | FSI Clock       | V19         |
| FSI_RX0_D0      | I            | FSI Data        | T17         |
| FSI_RX0_D1      | I            | FSI Data        | R16         |

表 5-28. FSI0 TX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_TX0_CLK     | O            | FSI Clock       | T19         |
| FSI_TX0_D0      | O            | FSI Data        | Y21         |
| FSI_TX0_D1      | O            | FSI Data        | Y20         |

表 5-29. FSI1 RX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_RX1_CLK     | I            | FSI Clock       | W20         |
| FSI_RX1_D0      | I            | FSI Data        | W21         |
| FSI_RX1_D1      | I            | FSI Data        | V18         |

表 5-30. FSI1 TX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_TX1_CLK     | O            | FSI Clock       | N16         |
| FSI_TX1_D0      | O            | FSI Data        | P17         |
| FSI_TX1_D1      | O            | FSI Data        | Y18         |

表 5-31. FSI2 RX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_RX2_CLK     | I            | FSI Clock       | T20         |
| FSI_RX2_D0      | I            | FSI Data        | U21         |
| FSI_RX2_D1      | I            | FSI Data        | T18         |

表 5-32. FSI3 RX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_RX3_CLK     | I            | FSI Clock       | U20         |
| FSI_RX3_D0      | I            | FSI Data        | U18         |
| FSI_RX3_D1      | I            | FSI Data        | U19         |

表 5-33. FSI4 RX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_RX4_CLK     | I            | FSI Clock       | R17         |
| FSI_RX4_D0      | I            | FSI Data        | V20         |
| FSI_RX4_D1      | I            | FSI Data        | V21         |

表 5-34. FSI5 RX Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSI_RX5_CLK     | I            | FSI Clock       | P16         |
| FSI_RX5_D0      | I            | FSI Data        | R18         |
| FSI_RX5_D1      | I            | FSI Data        | T21         |

### 5.3.10 GPIO

#### 5.3.10.1 MAIN Domain

表 5-35. GPIO0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALV PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO0_0         | IO           | General Purpose Input/Output | N20         |
| GPIO0_1         | IO           | General Purpose Input/Output | N21         |
| GPIO0_2         | IO           | General Purpose Input/Output | N19         |
| GPIO0_3         | IO           | General Purpose Input/Output | M19         |
| GPIO0_4         | IO           | General Purpose Input/Output | M18         |
| GPIO0_5         | IO           | General Purpose Input/Output | M20         |
| GPIO0_6         | IO           | General Purpose Input/Output | M21         |
| GPIO0_7         | IO           | General Purpose Input/Output | P21         |
| GPIO0_8         | IO           | General Purpose Input/Output | P20         |
| GPIO0_9         | IO           | General Purpose Input/Output | N18         |
| GPIO0_10        | IO           | General Purpose Input/Output | M17         |
| GPIO0_11        | IO           | General Purpose Input/Output | L19         |
| GPIO0_12        | IO           | General Purpose Input/Output | L18         |
| GPIO0_13        | IO           | General Purpose Input/Output | K17         |
| GPIO0_14        | IO           | General Purpose Input/Output | L17         |
| GPIO0_15        | IO           | General Purpose Input/Output | T20         |
| GPIO0_16        | IO           | General Purpose Input/Output | U21         |
| GPIO0_17        | IO           | General Purpose Input/Output | T18         |
| GPIO0_18        | IO           | General Purpose Input/Output | U20         |
| GPIO0_19        | IO           | General Purpose Input/Output | AA14        |
| GPIO0_20        | IO           | General Purpose Input/Output | Y13         |
| GPIO0_21        | IO           | General Purpose Input/Output | V20         |
| GPIO0_22        | IO           | General Purpose Input/Output | V21         |
| GPIO0_23        | IO           | General Purpose Input/Output | V19         |
| GPIO0_24        | IO           | General Purpose Input/Output | T17         |
| GPIO0_25        | IO           | General Purpose Input/Output | R16         |
| GPIO0_26        | IO           | General Purpose Input/Output | W20         |
| GPIO0_27        | IO           | General Purpose Input/Output | W21         |
| GPIO0_28        | IO           | General Purpose Input/Output | V18         |
| GPIO0_29        | IO           | General Purpose Input/Output | Y21         |
| GPIO0_30        | IO           | General Purpose Input/Output | Y20         |
| GPIO0_31        | IO           | General Purpose Input/Output | R17         |
| GPIO0_32        | IO           | General Purpose Input/Output | P16         |
| GPIO0_33        | IO           | General Purpose Input/Output | R18         |
| GPIO0_34        | IO           | General Purpose Input/Output | T21         |
| GPIO0_35        | IO           | General Purpose Input/Output | P17         |
| GPIO0_36        | IO           | General Purpose Input/Output | T19         |

表 5-35. GPIO0 Signal Descriptions (続き)

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3]              | ALV PIN [4] |
|-------------------------|--------------|------------------------------|-------------|
| GPIO0_37                | IO           | General Purpose Input/Output | W19         |
| GPIO0_38                | IO           | General Purpose Input/Output | Y18         |
| GPIO0_39                | IO           | General Purpose Input/Output | N16         |
| GPIO0_40                | IO           | General Purpose Input/Output | N17         |
| GPIO0_41                | IO           | General Purpose Input/Output | R19         |
| GPIO0_42                | IO           | General Purpose Input/Output | R20         |
| GPIO0_43 <sup>(1)</sup> | IO           | General Purpose Input/Output | P19         |
| GPIO0_44 <sup>(1)</sup> | IO           | General Purpose Input/Output | R21         |
| GPIO0_45                | IO           | General Purpose Input/Output | Y7          |
| GPIO0_46                | IO           | General Purpose Input/Output | U8          |
| GPIO0_47                | IO           | General Purpose Input/Output | W8          |
| GPIO0_48                | IO           | General Purpose Input/Output | V8          |
| GPIO0_49                | IO           | General Purpose Input/Output | Y8          |
| GPIO0_50                | IO           | General Purpose Input/Output | V13         |
| GPIO0_51                | IO           | General Purpose Input/Output | AA7         |
| GPIO0_52                | IO           | General Purpose Input/Output | U13         |
| GPIO0_53                | IO           | General Purpose Input/Output | W13         |
| GPIO0_54                | IO           | General Purpose Input/Output | U15         |
| GPIO0_55                | IO           | General Purpose Input/Output | U14         |
| GPIO0_56                | IO           | General Purpose Input/Output | AA8         |
| GPIO0_57                | IO           | General Purpose Input/Output | U9          |
| GPIO0_58                | IO           | General Purpose Input/Output | W9          |
| GPIO0_59                | IO           | General Purpose Input/Output | AA9         |
| GPIO0_60                | IO           | General Purpose Input/Output | Y9          |
| GPIO0_61                | IO           | General Purpose Input/Output | V9          |
| GPIO0_62                | IO           | General Purpose Input/Output | U7          |
| GPIO0_63                | IO           | General Purpose Input/Output | V7          |
| GPIO0_64                | IO           | General Purpose Input/Output | W7          |
| GPIO0_65                | IO           | General Purpose Input/Output | W11         |
| GPIO0_66                | IO           | General Purpose Input/Output | V11         |
| GPIO0_67                | IO           | General Purpose Input/Output | AA12        |
| GPIO0_68                | IO           | General Purpose Input/Output | Y12         |
| GPIO0_69                | IO           | General Purpose Input/Output | W12         |
| GPIO0_70                | IO           | General Purpose Input/Output | AA13        |
| GPIO0_71                | IO           | General Purpose Input/Output | U11         |
| GPIO0_72                | IO           | General Purpose Input/Output | V15         |
| GPIO0_73                | IO           | General Purpose Input/Output | U12         |
| GPIO0_74                | IO           | General Purpose Input/Output | V14         |
| GPIO0_75                | IO           | General Purpose Input/Output | W14         |
| GPIO0_76                | IO           | General Purpose Input/Output | AA10        |
| GPIO0_77                | IO           | General Purpose Input/Output | V10         |
| GPIO0_78                | IO           | General Purpose Input/Output | U10         |
| GPIO0_79                | IO           | General Purpose Input/Output | AA11        |
| GPIO0_80                | IO           | General Purpose Input/Output | Y11         |
| GPIO0_81                | IO           | General Purpose Input/Output | Y10         |

表 5-35. GPIO0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALV PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO0_82        | IO           | General Purpose Input/Output | U18         |
| GPIO0_83        | IO           | General Purpose Input/Output | U19         |
| GPIO0_84        | IO           | General Purpose Input/Output | V12         |
| GPIO0_85        | IO           | General Purpose Input/Output | AA6         |
| GPIO0_86        | IO           | General Purpose Input/Output | Y6          |

- (1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 5-36. GPIO1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALV PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO1_0         | IO           | General Purpose Input/Output | Y1          |
| GPIO1_1         | IO           | General Purpose Input/Output | R4          |
| GPIO1_2         | IO           | General Purpose Input/Output | U2          |
| GPIO1_3         | IO           | General Purpose Input/Output | V2          |
| GPIO1_4         | IO           | General Purpose Input/Output | AA2         |
| GPIO1_5         | IO           | General Purpose Input/Output | R3          |
| GPIO1_6         | IO           | General Purpose Input/Output | T3          |
| GPIO1_7         | IO           | General Purpose Input/Output | T1          |
| GPIO1_8         | IO           | General Purpose Input/Output | T2          |
| GPIO1_9         | IO           | General Purpose Input/Output | W6          |
| GPIO1_10        | IO           | General Purpose Input/Output | AA5         |
| GPIO1_11        | IO           | General Purpose Input/Output | Y3          |
| GPIO1_12        | IO           | General Purpose Input/Output | AA3         |
| GPIO1_13        | IO           | General Purpose Input/Output | R6          |
| GPIO1_14        | IO           | General Purpose Input/Output | V4          |
| GPIO1_15        | IO           | General Purpose Input/Output | T5          |
| GPIO1_16        | IO           | General Purpose Input/Output | U4          |
| GPIO1_17        | IO           | General Purpose Input/Output | U1          |
| GPIO1_18        | IO           | General Purpose Input/Output | V1          |
| GPIO1_19        | IO           | General Purpose Input/Output | W1          |
| GPIO1_20        | IO           | General Purpose Input/Output | Y2          |
| GPIO1_21        | IO           | General Purpose Input/Output | W2          |
| GPIO1_22        | IO           | General Purpose Input/Output | V3          |
| GPIO1_23        | IO           | General Purpose Input/Output | T4          |
| GPIO1_24        | IO           | General Purpose Input/Output | W3          |
| GPIO1_25        | IO           | General Purpose Input/Output | P4          |
| GPIO1_26        | IO           | General Purpose Input/Output | R5          |
| GPIO1_27        | IO           | General Purpose Input/Output | W5          |
| GPIO1_28        | IO           | General Purpose Input/Output | R1          |
| GPIO1_29        | IO           | General Purpose Input/Output | Y5          |
| GPIO1_30        | IO           | General Purpose Input/Output | V6          |
| GPIO1_31        | IO           | General Purpose Input/Output | W4          |
| GPIO1_32        | IO           | General Purpose Input/Output | Y4          |
| GPIO1_33        | IO           | General Purpose Input/Output | T6          |
| GPIO1_34        | IO           | General Purpose Input/Output | U6          |

表 5-36. GPIO1 Signal Descriptions (続き)

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3]              | ALV PIN [4] |
|-------------------------|--------------|------------------------------|-------------|
| GPIO1_35                | IO           | General Purpose Input/Output | U5          |
| GPIO1_36                | IO           | General Purpose Input/Output | AA4         |
| GPIO1_37                | IO           | General Purpose Input/Output | V5          |
| GPIO1_38                | IO           | General Purpose Input/Output | P5          |
| GPIO1_39                | IO           | General Purpose Input/Output | R2          |
| GPIO1_40                | IO           | General Purpose Input/Output | P2          |
| GPIO1_41                | IO           | General Purpose Input/Output | P3          |
| GPIO1_42                | IO           | General Purpose Input/Output | D12         |
| GPIO1_43                | IO           | General Purpose Input/Output | C13         |
| GPIO1_44                | IO           | General Purpose Input/Output | D13         |
| GPIO1_45                | IO           | General Purpose Input/Output | A13         |
| GPIO1_46                | IO           | General Purpose Input/Output | A14         |
| GPIO1_47                | IO           | General Purpose Input/Output | B14         |
| GPIO1_48                | IO           | General Purpose Input/Output | D14         |
| GPIO1_49                | IO           | General Purpose Input/Output | C14         |
| GPIO1_50                | IO           | General Purpose Input/Output | B15         |
| GPIO1_51                | IO           | General Purpose Input/Output | A15         |
| GPIO1_52                | IO           | General Purpose Input/Output | D15         |
| GPIO1_53                | IO           | General Purpose Input/Output | C16         |
| GPIO1_54                | IO           | General Purpose Input/Output | B16         |
| GPIO1_55                | IO           | General Purpose Input/Output | A16         |
| GPIO1_56                | IO           | General Purpose Input/Output | E15         |
| GPIO1_57                | IO           | General Purpose Input/Output | E14         |
| GPIO1_58                | IO           | General Purpose Input/Output | D16         |
| GPIO1_59                | IO           | General Purpose Input/Output | E16         |
| GPIO1_60                | IO           | General Purpose Input/Output | A17         |
| GPIO1_61                | IO           | General Purpose Input/Output | B17         |
| GPIO1_62                | IO           | General Purpose Input/Output | C17         |
| GPIO1_63                | IO           | General Purpose Input/Output | D17         |
| GPIO1_64                | IOD          | General Purpose Input/Output | A18         |
| GPIO1_65                | IOD          | General Purpose Input/Output | B18         |
| GPIO1_66                | IO           | General Purpose Input/Output | C18         |
| GPIO1_67                | IO           | General Purpose Input/Output | B19         |
| GPIO1_68 <sup>(1)</sup> | IO           | General Purpose Input/Output | D18         |
| GPIO1_69                | IO           | General Purpose Input/Output | A19         |
| GPIO1_70 <sup>(1)</sup> | IOD          | General Purpose Input/Output | C19         |
| GPIO1_71 <sup>(1)</sup> | IO           | General Purpose Input/Output | K18         |
| GPIO1_72 <sup>(1)</sup> | IO           | General Purpose Input/Output | K19         |
| GPIO1_73 <sup>(1)</sup> | IO           | General Purpose Input/Output | L21         |
| GPIO1_74 <sup>(1)</sup> | IO           | General Purpose Input/Output | K21         |
| GPIO1_75 <sup>(1)</sup> | IO           | General Purpose Input/Output | L20         |
| GPIO1_76 <sup>(1)</sup> | IO           | General Purpose Input/Output | J19         |
| GPIO1_77 <sup>(1)</sup> | IO           | General Purpose Input/Output | D19         |
| GPIO1_78 <sup>(1)</sup> | IO           | General Purpose Input/Output | C20         |

表 5-36. GPIO1 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALV PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO1_79        | IO           | General Purpose Input/Output | E19         |

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

### 5.3.10.2 MCU Domain

表 5-37. MCU\_GPIO0 Signal Descriptions

| SIGNAL NAME [1]             | PIN TYPE [2] | DESCRIPTION [3]              | ALV PIN [4] |
|-----------------------------|--------------|------------------------------|-------------|
| MCU_GPIO0_0 <sup>(1)</sup>  | IO           | General Purpose Input/Output | E8          |
| MCU_GPIO0_1 <sup>(1)</sup>  | IO           | General Purpose Input/Output | D8          |
| MCU_GPIO0_2                 | IO           | General Purpose Input/Output | A8          |
| MCU_GPIO0_3                 | IO           | General Purpose Input/Output | A9          |
| MCU_GPIO0_4                 | IO           | General Purpose Input/Output | B6          |
| MCU_GPIO0_5 <sup>(1)</sup>  | IO           | General Purpose Input/Output | A7          |
| MCU_GPIO0_6 <sup>(1)</sup>  | IO           | General Purpose Input/Output | B7          |
| MCU_GPIO0_7                 | IO           | General Purpose Input/Output | D7          |
| MCU_GPIO0_8                 | IO           | General Purpose Input/Output | C7          |
| MCU_GPIO0_9                 | IO           | General Purpose Input/Output | C8          |
| MCU_GPIO0_10                | IO           | General Purpose Input/Output | E7          |
| MCU_GPIO0_11                | IO           | General Purpose Input/Output | E6          |
| MCU_GPIO0_12 <sup>(1)</sup> | IO           | General Purpose Input/Output | C6          |
| MCU_GPIO0_13 <sup>(1)</sup> | IO           | General Purpose Input/Output | D6          |
| MCU_GPIO0_14                | IO           | General Purpose Input/Output | C9          |
| MCU_GPIO0_15                | IO           | General Purpose Input/Output | D9          |
| MCU_GPIO0_16 <sup>(1)</sup> | IO           | General Purpose Input/Output | B8          |
| MCU_GPIO0_17 <sup>(1)</sup> | IO           | General Purpose Input/Output | B9          |
| MCU_GPIO0_18                | IOD          | General Purpose Input/Output | E9          |
| MCU_GPIO0_19                | IOD          | General Purpose Input/Output | A10         |
| MCU_GPIO0_20 <sup>(1)</sup> | IO           | General Purpose Input/Output | A11         |
| MCU_GPIO0_21 <sup>(1)</sup> | IO           | General Purpose Input/Output | B10         |
| MCU_GPIO0_22                | IO           | General Purpose Input/Output | B13         |

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

### 5.3.11 GPMC

#### 5.3.11.1 MAIN Domain

表 5-38. GPMC0 Signal Descriptions

| SIGNAL NAME [1]          | PIN TYPE [2] | DESCRIPTION [3]                                             | ALV PIN [4] |
|--------------------------|--------------|-------------------------------------------------------------|-------------|
| GPMC0_ADVn_ALE           | O            | GPMC Address Valid (active low) or Address Latch Enable     | P16         |
| GPMC0_CLK <sup>(1)</sup> | O            | GPMC clock                                                  | R17         |
| GPMC0_DIR                | O            | GPMC Data Bus Signal Direction Control                      | N17         |
| GPMC0_FCLK_MUX           | O            | GPMC functional clock output selected through a mux logic   | R17         |
| GPMC0_OEn_REn            | O            | GPMC Output Enable (active low) or Read Enable (active low) | R18         |
| GPMC0_WEn                | O            | GPMC Write Enable (active low)                              | T21         |

表 5-38. GPMC0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                | ALV PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_WPn       | O            | GPMC Flash Write Protect (active low)                                                                          | N16         |
| GPMC0_A0        | OZ           | GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories                    | U2, U7      |
| GPMC0_A1        | OZ           | GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode                       | AA2, V7     |
| GPMC0_A2        | OZ           | GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode                       | T2, W7      |
| GPMC0_A3        | OZ           | GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode                       | V4, W11     |
| GPMC0_A4        | OZ           | GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode                       | U4, V11     |
| GPMC0_A5        | OZ           | GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode                       | AA12, V1    |
| GPMC0_A6        | OZ           | GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode                       | W1, Y12     |
| GPMC0_A7        | OZ           | GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode                       | W12, Y4     |
| GPMC0_A8        | OZ           | GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode                       | AA13, T6    |
| GPMC0_A9        | OZ           | GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode                       | U11, U6     |
| GPMC0_A10       | OZ           | GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode                      | U5, V15     |
| GPMC0_A11       | OZ           | GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AA4, U12    |
| GPMC0_A12       | OZ           | GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | P2, V14     |
| GPMC0_A13       | OZ           | GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | P3, W14     |
| GPMC0_A14       | OZ           | GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AA10, AA3   |
| GPMC0_A15       | OZ           | GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | R6, V10     |
| GPMC0_A16       | OZ           | GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | T5, U10     |
| GPMC0_A17       | OZ           | GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AA11, U1    |
| GPMC0_A18       | OZ           | GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | T4, Y11     |
| GPMC0_A19       | OZ           | GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | R5, Y10     |
| GPMC0_A20       | OZ           | GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | R21         |
| GPMC0_A21       | OZ           | GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | Y18         |
| GPMC0_A22       | OZ           | GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | N16         |
| GPMC0_AD0       | IO           | GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode | T20         |
| GPMC0_AD1       | IO           | GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode | U21         |

**表 5-38. GPMC0 Signal Descriptions (続き)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                  | ALV PIN [4] |
|-----------------|--------------|------------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_AD2       | IO           | GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode   | T18         |
| GPMC0_AD3       | IO           | GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode   | U20         |
| GPMC0_AD4       | IO           | GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode   | U18         |
| GPMC0_AD5       | IO           | GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode   | U19         |
| GPMC0_AD6       | IO           | GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode   | V20         |
| GPMC0_AD7       | IO           | GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode   | V21         |
| GPMC0_AD8       | IO           | GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode   | V19         |
| GPMC0_AD9       | IO           | GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode  | T17         |
| GPMC0_AD10      | IO           | GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode | R16         |
| GPMC0_AD11      | IO           | GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode | W20         |
| GPMC0_AD12      | IO           | GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode | W21         |
| GPMC0_AD13      | IO           | GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode | V18         |
| GPMC0_AD14      | IO           | GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode | Y21         |
| GPMC0_AD15      | IO           | GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode | Y20         |
| GPMC0_AD16      | IO           | GPMC Data 16 Input/Output in A/D non-multiplexed mode and additionally Address 17 Output in A/D multiplexed mode | Y7          |
| GPMC0_AD17      | IO           | GPMC Data 17 Input/Output in A/D non-multiplexed mode and additionally Address 18 Output in A/D multiplexed mode | U8          |
| GPMC0_AD18      | IO           | GPMC Data 18 Input/Output in A/D non-multiplexed mode and additionally Address 19 Output in A/D multiplexed mode | W8          |
| GPMC0_AD19      | IO           | GPMC Data 19 Input/Output in A/D non-multiplexed mode and additionally Address 20 Output in A/D multiplexed mode | V8          |
| GPMC0_AD20      | IO           | GPMC Data 20 Input/Output in A/D non-multiplexed mode and additionally Address 21 Output in A/D multiplexed mode | Y8          |

表 5-38. GPMC0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                  | ALV PIN [4] |
|-----------------|--------------|------------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_AD21      | IO           | GPMC Data 21 Input/Output in A/D non-multiplexed mode and additionally Address 22 Output in A/D multiplexed mode | V13         |
| GPMC0_AD22      | IO           | GPMC Data 22 Input/Output in A/D non-multiplexed mode and additionally Address 23 Output in A/D multiplexed mode | AA7         |
| GPMC0_AD23      | IO           | GPMC Data 23 Input/Output in A/D non-multiplexed mode and additionally Address 24 Output in A/D multiplexed mode | U13         |
| GPMC0_AD24      | IO           | GPMC Data 24 Input/Output in A/D non-multiplexed mode and additionally Address 25 Output in A/D multiplexed mode | W13         |
| GPMC0_AD25      | IO           | GPMC Data 25 Input/Output in A/D non-multiplexed mode and additionally Address 26 Output in A/D multiplexed mode | U15         |
| GPMC0_AD26      | IO           | GPMC Data 26 Input/Output in A/D non-multiplexed mode and additionally Address 27 Output in A/D multiplexed mode | U14         |
| GPMC0_AD27      | IO           | GPMC Data 27 Input/Output in A/D non-multiplexed mode and additionally Address 28 Output in A/D multiplexed mode | AA8         |
| GPMC0_AD28      | IO           | GPMC Data 28 Input/Output in A/D non-multiplexed mode and additionally Address 29 Output in A/D multiplexed mode | U9          |
| GPMC0_AD29      | IO           | GPMC Data 29 Input/Output in A/D non-multiplexed mode and additionally Address 30 Output in A/D multiplexed mode | W9          |
| GPMC0_AD30      | IO           | GPMC Data 30 Input/Output in A/D non-multiplexed mode and additionally Address 31 Output in A/D multiplexed mode | AA9         |
| GPMC0_AD31      | IO           | GPMC Data 31 Input/Output in A/D non-multiplexed mode and additionally Address 0 Output in A/D multiplexed mode  | Y9          |
| GPMC0_BE0n_CLE  | O            | GPMC Lower-Byte Enable (active low) or Command Latch Enable                                                      | P17         |
| GPMC0_BE1n      | O            | GPMC Upper-Byte Enable (active low)                                                                              | T19         |
| GPMC0_BE2n      | O            | GPMC Upper-Byte Enable (active low)                                                                              | V9          |
| GPMC0_BE3n      | O            | GPMC Upper-Byte Enable (active low)                                                                              | AA14        |
| GPMC0_CS0       | O            | GPMC Chip Select 0 (active low)                                                                                  | R19         |
| GPMC0_CS1       | O            | GPMC Chip Select 1 (active low)                                                                                  | R20         |
| GPMC0_CS2       | O            | GPMC Chip Select 2 (active low)                                                                                  | P19         |
| GPMC0_CS3       | O            | GPMC Chip Select 3 (active low)                                                                                  | R21         |
| GPMC0_WAIT0     | I            | GPMC External Indication of Wait                                                                                 | W19         |
| GPMC0_WAIT1     | I            | GPMC External Indication of Wait                                                                                 | Y18         |

- (1) The RXACTIVE bit of the CTRLMMR\_PADCONFIG32 register must be set to 0x1 and the TX\_DIS bit of the CTRLMMR\_PADCONFIG32 register must be reset to 0x0 when GPMC0 is operating in synchronous mode.

### 5.3.12 I2C

#### 5.3.12.1 MAIN Domain

表 5-39. I2C0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C0_SCL        | IOD          | I2C Clock       | A18         |

表 5-39. I2C0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C0_SDA        | IOD          | I2C Data        | B18         |

表 5-40. I2C1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C1_SCL        | IOD          | I2C Clock       | C18         |
| I2C1_SDA        | IOD          | I2C Data        | B19         |

表 5-41. I2C2 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C2_SCL        | IOD          | I2C Clock       | C13, P19    |
| I2C2_SDA        | IOD          | I2C Data        | D14, R21    |

表 5-42. I2C3 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C3_SCL        | IOD          | I2C Clock       | C17         |
| I2C3_SDA        | IOD          | I2C Data        | D17         |

### 5.3.12.2 MCU Domain

表 5-43. MCU\_I2C0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_I2C0_SCL    | IOD          | I2C Clock       | E9          |
| MCU_I2C0_SDA    | IOD          | I2C Data        | A10         |

表 5-44. MCU\_I2C1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_I2C1_SCL    | IOD          | I2C Clock       | A11         |
| MCU_I2C1_SDA    | IOD          | I2C Data        | B10         |

### 5.3.13 MCAN

#### 5.3.13.1 MAIN Domain

表 5-45. MCAN0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALV PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN0_RX        | I            | MCAN Receive Data  | B17         |
| MCAN0_TX        | O            | MCAN Transmit Data | A17         |

表 5-46. MCAN1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALV PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN1_RX        | I            | MCAN Receive Data  | D17         |
| MCAN1_TX        | O            | MCAN Transmit Data | C17         |

### 5.3.14 MCSPI

#### 5.3.14.1 MAIN Domain

**表 5-47. MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI0_CLK        | IO           | SPI Clock         | D13         |
| SPI0_CS0        | IO           | SPI Chip Select 0 | D12         |
| SPI0_CS1        | IO           | SPI Chip Select 1 | C13         |
| SPI0_CS2        | IO           | SPI Chip Select 2 | B16         |
| SPI0_CS3        | IO           | SPI Chip Select 3 | A16         |
| SPI0_D0         | IO           | SPI Data 0        | A13         |
| SPI0_D1         | IO           | SPI Data 1        | A14         |

**表 5-48. MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI1_CLK        | IO           | SPI Clock         | C14         |
| SPI1_CS0        | IO           | SPI Chip Select 0 | B14         |
| SPI1_CS1        | IO           | SPI Chip Select 1 | D14         |
| SPI1_CS2        | IO           | SPI Chip Select 2 | D16         |
| SPI1_CS3        | IO           | SPI Chip Select 3 | E16         |
| SPI1_D0         | IO           | SPI Data 0        | B15         |
| SPI1_D1         | IO           | SPI Data 1        | A15         |

**表 5-49. MCSPI2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI2_CLK        | IO           | SPI Clock         | E14         |
| SPI2_CS0        | IO           | SPI Chip Select 0 | E15         |
| SPI2_CS1        | IO           | SPI Chip Select 1 | C18         |
| SPI2_CS2        | IO           | SPI Chip Select 2 | B19         |
| SPI2_CS3        | IO           | SPI Chip Select 3 | A19         |
| SPI2_D0         | IO           | SPI Data 0        | D15         |
| SPI2_D1         | IO           | SPI Data 1        | C16         |

**表 5-50. MCSPI3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI3_CLK        | IO           | SPI Clock         | U4          |
| SPI3_CS0        | IO           | SPI Chip Select 0 | U1          |
| SPI3_CS1        | IO           | SPI Chip Select 1 | T5          |
| SPI3_CS2        | IO           | SPI Chip Select 2 | V12         |
| SPI3_CS3        | IO           | SPI Chip Select 3 | V15         |
| SPI3_D0         | IO           | SPI Data 0        | R6          |
| SPI3_D1         | IO           | SPI Data 1        | V4          |

**表 5-51. MCSPI4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI4_CLK        | IO           | SPI Clock         | B16         |
| SPI4_CS0        | IO           | SPI Chip Select 0 | E16         |

表 5-51. MCSPI4 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI4_CS1        | IO           | SPI Chip Select 1 | A17         |
| SPI4_CS2        | IO           | SPI Chip Select 0 | B17         |
| SPI4_CS3        | IO           | SPI Chip Select 2 | D18         |
| SPI4_D0         | IO           | SPI Data 0        | A16         |
| SPI4_D1         | IO           | SPI Data 1        | D16         |

#### 5.3.14.2 MCU Domain

表 5-52. MCU\_MCSPI0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| MCU_SPI0_CLK    | IO           | SPI Clock         | E6          |
| MCU_SPI0_CS0    | IO           | SPI Chip Select 0 | D6          |
| MCU_SPI0_CS1    | IO           | SPI Chip Select 1 | C6          |
| MCU_SPI0_CS2    | IO           | SPI Chip Select 2 | D8          |
| MCU_SPI0_CS3    | IO           | SPI Chip Select 3 | B8          |
| MCU_SPI0_D0     | IO           | SPI Data 0        | E7          |
| MCU_SPI0_D1     | IO           | SPI Data 1        | B6          |

表 5-53. MCU\_MCSPI1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALV PIN [4] |
|-----------------|--------------|-------------------|-------------|
| MCU_SPI1_CLK    | IO           | SPI Clock         | D7          |
| MCU_SPI1_CS0    | IO           | SPI Chip Select 0 | A7          |
| MCU_SPI1_CS1    | IO           | SPI Chip Select 1 | B7          |
| MCU_SPI1_CS2    | IO           | SPI Chip Select 2 | E8          |
| MCU_SPI1_CS3    | IO           | SPI Chip Select 3 | B9          |
| MCU_SPI1_D0     | IO           | SPI Data 0        | C7          |
| MCU_SPI1_D1     | IO           | SPI Data 1        | C8          |

#### 5.3.15 MDIO

##### 5.3.15.1 MAIN Domain

表 5-54. MDIO0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MDIO0_MDC       | O            | MDIO Clock      | R2, Y6      |
| MDIO0_MDIO      | IO           | MDIO Data       | AA6, P5     |

#### 5.3.16 MMC

##### 5.3.16.1 MAIN Domain

表 5-55. MMC0 Signal Descriptions

| SIGNAL NAME [1]            | PIN TYPE [2] | DESCRIPTION [3]                  | ALV PIN [4] |
|----------------------------|--------------|----------------------------------|-------------|
| MMC0_CALPAD <sup>(1)</sup> | A            | MMC/SD/SDIO Calibration Resistor | F18         |
| MMC0_CLK                   | IO           | MMC/SD/SDIO Clock                | G18         |
| MMC0_CMD                   | IO           | MMC/SD/SDIO Command              | J21         |
| MMC0_DS                    | IO           | MMC Data Strobe                  | G19         |
| MMC0_DAT0                  | IO           | MMC/SD/SDIO Data                 | K20         |
| MMC0_DAT1                  | IO           | MMC/SD/SDIO Data                 | J20         |

表 5-55. MMC0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]  | ALV PIN [4] |
|-----------------|--------------|------------------|-------------|
| MMC0_DAT2       | IO           | MMC/SD/SDIO Data | J18         |
| MMC0_DAT3       | IO           | MMC/SD/SDIO Data | J17         |
| MMC0_DAT4       | IO           | MMC/SD/SDIO Data | H17         |
| MMC0_DAT5       | IO           | MMC/SD/SDIO Data | H19         |
| MMC0_DAT6       | IO           | MMC/SD/SDIO Data | H18         |
| MMC0_DAT7       | IO           | MMC/SD/SDIO Data | G17         |

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

表 5-56. MMC1 Signal Descriptions

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3]     | ALV PIN [4] |
|-------------------------|--------------|---------------------|-------------|
| MMC1_CLK <sup>(1)</sup> | IO           | MMC/SD/SDIO Clock   | L20         |
| MMC1_CMD                | IO           | MMC/SD/SDIO Command | J19         |
| MMC1_SDCD               | I            | SD Card Detect      | D19         |
| MMC1_SDWP               | I            | SD Write Protect    | C20         |
| MMC1_DAT0               | IO           | MMC/SD/SDIO Data    | K21         |
| MMC1_DAT1               | IO           | MMC/SD/SDIO Data    | L21         |
| MMC1_DAT2               | IO           | MMC/SD/SDIO Data    | K19         |
| MMC1_DAT3               | IO           | MMC/SD/SDIO Data    | K18         |

(1) For MMC1\_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR\_PADCONFIG164 register must remain in its default state of 0x1 because of retiming purposes.

### 5.3.17 OSPI

#### 5.3.17.1 MAIN Domain

表 5-57. OSPI0 Signal Descriptions

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3]                                | ALV PIN [4] |
|-------------------------|--------------|------------------------------------------------|-------------|
| OSPI0_CLK               | O            | OSPI Clock                                     | N20         |
| OSPI0_DQS               | I            | OSPI Data Strobe (DQS) or Loopback Clock Input | N19         |
| OSPI0_ECC_FAIL          | I            | OSPI ECC Status                                | L17         |
| OSPI0_LBCLKO            | IO           | OSPI Loopback Clock Output                     | N21         |
| OSPI0_CS <sub>n</sub> 0 | O            | OSPI Chip Select 0 (active low)                | L19         |
| OSPI0_CS <sub>n</sub> 1 | O            | OSPI Chip Select 1 (active low)                | L18         |
| OSPI0_CS <sub>n</sub> 2 | O            | OSPI Chip Select 2 (active low)                | K17         |
| OSPI0_CS <sub>n</sub> 3 | O            | OSPI Chip Select 3 (active low)                | L17         |
| OSPI0_D0                | IO           | OSPI Data 0                                    | M19         |
| OSPI0_D1                | IO           | OSPI Data 1                                    | M18         |
| OSPI0_D2                | IO           | OSPI Data 2                                    | M20         |
| OSPI0_D3                | IO           | OSPI Data 3                                    | M21         |
| OSPI0_D4                | IO           | OSPI Data 4                                    | P21         |
| OSPI0_D5                | IO           | OSPI Data 5                                    | P20         |
| OSPI0_D6                | IO           | OSPI Data 6                                    | N18         |
| OSPI0_D7                | IO           | OSPI Data 7                                    | M17         |
| OSPI0_RESET_OUT0        | O            | OSPI Reset                                     | L17         |
| OSPI0_RESET_OUT1        | O            | OSPI Reset                                     | K17         |

### 5.3.18 Power Supply

**表 5-58. Power Supply Signal Descriptions**

| SIGNAL NAME [1]                | PIN TYPE [2] | DESCRIPTION [3]                              | ALV PIN [4]                                      |
|--------------------------------|--------------|----------------------------------------------|--------------------------------------------------|
| CAP_VDDS0 <sup>(1)</sup>       | CAP          | External capacitor connection for IO group 0 | H12                                              |
| CAP_VDDS1 <sup>(1)</sup>       | CAP          | External capacitor connection for IO group 1 | T7                                               |
| CAP_VDDS2 <sup>(1)</sup>       | CAP          | External capacitor connection for IO group 2 | R11                                              |
| CAP_VDDS3 <sup>(1)</sup>       | CAP          | External capacitor connection for IO group 3 | N14                                              |
| CAP_VDDS4 <sup>(1)</sup>       | CAP          | External capacitor connection for IO group 4 | M16                                              |
| CAP_VDDS5 <sup>(1)</sup>       | CAP          | External capacitor connection for IO group 5 | L13                                              |
| CAP_VDDSHV_MMC1 <sup>(2)</sup> | CAP          | External capacitor connection for MMC1       | K15                                              |
| CAP_VDDS_MCU <sup>(1)</sup>    | CAP          | External capacitor connection for IO MCU     | H10                                              |
| VDDA_0P85_SERDES0              | PWR          | SERDES0 0.85 V analog supply                 | P12, P13                                         |
| VDDA_0P85_SERDES0_C            | PWR          | SERDES0 clock 0.85 V analog supply           | P11                                              |
| VDDA_0P85_USB0                 | PWR          | USB0 0.85 V analog supply                    | T12                                              |
| VDDA_1P8_SERDES0               | PWR          | SERDES0 1.8 V analog supply                  | R14                                              |
| VDDA_1P8_USB0                  | PWR          | USB0 1.8 V analog supply                     | R15                                              |
| VDDA_3P3_SDIO                  | PWR          | SDIO 3.3 V analog supply                     | H15                                              |
| VDDA_3P3_USB0                  | PWR          | USB0 3.3 V analog supply                     | R13                                              |
| VDDA_ADC                       | PWR          | ADC0 analog supply                           | J13                                              |
| VDDA_MCU                       | PWR          | POR and MCU PLL analog supply                | K12                                              |
| VDDA_PLL0                      | PWR          | Main, PER1, and R5F PLL analog supply        | N12                                              |
| VDDA_PLL1                      | PWR          | ARM and DDR PLL analog supply                | H9                                               |
| VDDA_PLL2                      | PWR          | PER0 PLL analog supply                       | J11                                              |
| VDDA_TEMP0                     | PWR          | TEMP0 analog supply                          | G11                                              |
| VDDA_TEMP1                     | PWR          | TEMP1 analog supply                          | L11                                              |
| VDDR_CORE                      | PWR          | RAM supply                                   | L10, M13                                         |
| VDDSHV0                        | PWR          | IO supply for IO group 0                     | F11, G12, G14                                    |
| VDDSHV1                        | PWR          | IO supply for IO group 1                     | M7, N6, P7                                       |
| VDDSHV2                        | PWR          | IO supply for IO group 2                     | R10, R8, T9                                      |
| VDDSHV3                        | PWR          | IO supply for IO group 3                     | P14, P15                                         |
| VDDSHV4                        | PWR          | IO supply for IO group 4                     | M14, M15                                         |
| VDDSHV5                        | PWR          | IO supply for IO group 5                     | L14, L15                                         |
| VDDSHV_MCU                     | PWR          | IO supply for IO MCU                         | F9, G10, G8                                      |
| VDDS_DDR                       | PWR          | DDR PHY IO supply                            | F7, G6, H7, J6, K7, L6                           |
| VDDS_DDR_C                     | PWR          | DDR clock IO supply                          | J8                                               |
| VDDS_MMC0                      | PWR          | MMC0 PHY IO supply                           | K14                                              |
| VDDS_OSC                       | PWR          | MCU_OSC0 supply                              | H13                                              |
| VDD_CORE                       | PWR          | Core supply                                  | J10, J12, K11, K9, L12, L8, M11, M9, N10, N8, P9 |
| VDD_DLL_MMC0                   | PWR          | MMC0 PLL analog supply                       | H14                                              |
| VDD_MMC0                       | PWR          | MMC0 PHY core supply                         | K13                                              |
| VPP                            | PWR          | eFuse ROM programming supply                 | G15                                              |

表 5-58. Power Supply Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4]                                                                                                                                                                                                                                                                                                  |
|-----------------|--------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VSS             | GND          | Ground          | A1, A21, A5, A6, AA1, AA15, AA18, AA21, C10, C15, C3, D1, E11, E13, F10, F15, F8, G1, G16, G3, G7, G9, H11, H20, H21, H6, H8, J14, J7, J9, K6, K8, L1, L16, L3, L7, L9, M10, M12, M6, M8, N11, N13, N15, N7, N9, P1, P10, P18, P6, P8, R12, R7, R9, T10, T11, T15, T16, T8, U3, V17, W10, W18, Y14, Y17, Y19 |

- (1) This pin must always be connected via a 1- $\mu$ F capacitor to VSS.  
(2) This pin must always be connected via a 3.3- $\mu$ F  $\pm$ 20% capacitor to VSS when the SDIO\_LDO is being used to source VDDSHV5. Otherwise, this pin may be connected directly to VSS when the VDDA\_3P3\_SDIO pin is also connected directly to VSS.

### 5.3.19 PRU\_ICSSG

#### 注

The PRU\_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU\_ICSSG chapter in the device TRM.

#### 5.3.19.1 MAIN Domain

表 5-59. PRU\_ICSSG0 Signal Descriptions

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                                        | ALV PIN [4] |
|------------------------------|--------------|------------------------------------------------------------------------|-------------|
| PRG0_ECAP0_IN_APWM_OUT       | IO           | PRU-ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | R2, U5      |
| PRG0_ECAP0_SYNC_IN           | I            | PRU-ICSSG ECAP Sync Input                                              | P5, V5      |
| PRG0_ECAP0_SYNC_OUT          | O            | PRU-ICSSG ECAP Sync Output                                             | AA4, V5     |
| PRG0_IEP0_EDIO_OUTVALID      | O            | PRU_ICSSG Industrial Ethernet Digital I/O Outvalid                     | C13         |
| PRG0_IEP0_EDC_LATCH_IN0      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | V1          |
| PRG0_IEP0_EDC_LATCH_IN1      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | T1          |
| PRG0_IEP0_EDC_SYNC_OUT0      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | W1          |
| PRG0_IEP0_EDC_SYNC_OUT1      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | U1          |
| PRG0_IEP0_EDIO_DATA_IN_OUT28 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | W6          |
| PRG0_IEP0_EDIO_DATA_IN_OUT29 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | AA5         |
| PRG0_IEP0_EDIO_DATA_IN_OUT30 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | Y5          |

**表 5-59. PRU\_ICSSG0 Signal Descriptions (続き)**

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                             | ALV PIN [4] |
|------------------------------|--------------|-------------------------------------------------------------|-------------|
| PRG0_IEP0_EDIO_DATA_IN_OUT31 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | V6          |
| PRG0_IEP1_EDC_LATCH_IN0      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | P5          |
| PRG0_IEP1_EDC_LATCH_IN1      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | W5          |
| PRG0_IEP1_EDC_SYNC_OUT0      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | R2          |
| PRG0_IEP1_EDC_SYNC_OUT1      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | V5          |
| PRG0_MDIO0_MDC               | O            | PRU-ICSSG MDIO Clock                                        | P3          |
| PRG0_MDIO0_MDIO              | IO           | PRU-ICSSG MDIO Data                                         | P2          |
| PRG0_PRU0_GPI0               | I            | PRU-ICSSG PRU Data Input                                    | Y1          |
| PRG0_PRU0_GPI1               | I            | PRU-ICSSG PRU Data Input                                    | R4          |
| PRG0_PRU0_GPI2               | I            | PRU-ICSSG PRU Data Input                                    | U2          |
| PRG0_PRU0_GPI3               | I            | PRU-ICSSG PRU Data Input                                    | V2          |
| PRG0_PRU0_GPI4               | I            | PRU-ICSSG PRU Data Input                                    | AA2         |
| PRG0_PRU0_GPI5               | I            | PRU-ICSSG PRU Data Input                                    | R3          |
| PRG0_PRU0_GPI6               | I            | PRU-ICSSG PRU Data Input                                    | T3          |
| PRG0_PRU0_GPI7               | I            | PRU-ICSSG PRU Data Input                                    | T1          |
| PRG0_PRU0_GPI8               | I            | PRU-ICSSG PRU Data Input                                    | T2          |
| PRG0_PRU0_GPI9               | I            | PRU-ICSSG PRU Data Input                                    | W6          |
| PRG0_PRU0_GPI10              | I            | PRU-ICSSG PRU Data Input                                    | AA5         |
| PRG0_PRU0_GPI11              | I            | PRU-ICSSG PRU Data Input                                    | Y3          |
| PRG0_PRU0_GPI12              | I            | PRU-ICSSG PRU Data Input                                    | AA3         |
| PRG0_PRU0_GPI13              | I            | PRU-ICSSG PRU Data Input                                    | R6          |
| PRG0_PRU0_GPI14              | I            | PRU-ICSSG PRU Data Input                                    | V4          |
| PRG0_PRU0_GPI15              | I            | PRU-ICSSG PRU Data Input                                    | T5          |
| PRG0_PRU0_GPI16              | I            | PRU-ICSSG PRU Data Input                                    | U4          |
| PRG0_PRU0_GPI17              | I            | PRU-ICSSG PRU Data Input                                    | U1          |
| PRG0_PRU0_GPI18              | I            | PRU-ICSSG PRU Data Input                                    | V1          |
| PRG0_PRU0_GPI19              | I            | PRU-ICSSG PRU Data Input                                    | W1          |
| PRG0_PRU0_GPO0               | IO           | PRU-ICSSG PRU Data Output                                   | Y1          |
| PRG0_PRU0_GPO1               | IO           | PRU-ICSSG PRU Data Output                                   | R4          |
| PRG0_PRU0_GPO2               | IO           | PRU-ICSSG PRU Data Output                                   | U2          |
| PRG0_PRU0_GPO3               | IO           | PRU-ICSSG PRU Data Output                                   | V2          |
| PRG0_PRU0_GPO4               | IO           | PRU-ICSSG PRU Data Output                                   | AA2         |
| PRG0_PRU0_GPO5               | IO           | PRU-ICSSG PRU Data Output                                   | R3          |
| PRG0_PRU0_GPO6               | IO           | PRU-ICSSG PRU Data Output                                   | T3          |
| PRG0_PRU0_GPO7               | IO           | PRU-ICSSG PRU Data Output                                   | T1          |
| PRG0_PRU0_GPO8               | IO           | PRU-ICSSG PRU Data Output                                   | T2          |
| PRG0_PRU0_GPO9               | IO           | PRU-ICSSG PRU Data Output                                   | W6          |
| PRG0_PRU0_GPO10              | IO           | PRU-ICSSG PRU Data Output                                   | AA5         |
| PRG0_PRU0_GPO11              | IO           | PRU-ICSSG PRU Data Output                                   | Y3          |
| PRG0_PRU0_GPO12              | IO           | PRU-ICSSG PRU Data Output                                   | AA3         |
| PRG0_PRU0_GPO13              | IO           | PRU-ICSSG PRU Data Output                                   | R6          |

表 5-59. PRU\_ICSSG0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]           | ALV PIN [4] |
|-----------------|--------------|---------------------------|-------------|
| PRG0_PRU0_GPO14 | IO           | PRU-ICSSG PRU Data Output | V4          |
| PRG0_PRU0_GPO15 | IO           | PRU-ICSSG PRU Data Output | T5          |
| PRG0_PRU0_GPO16 | IO           | PRU-ICSSG PRU Data Output | U4          |
| PRG0_PRU0_GPO17 | IO           | PRU-ICSSG PRU Data Output | U1          |
| PRG0_PRU0_GPO18 | IO           | PRU-ICSSG PRU Data Output | V1          |
| PRG0_PRU0_GPO19 | IO           | PRU-ICSSG PRU Data Output | W1          |
| PRG0_PRU1_GPI0  | I            | PRU-ICSSG PRU Data Input  | Y2          |
| PRG0_PRU1_GPI1  | I            | PRU-ICSSG PRU Data Input  | W2          |
| PRG0_PRU1_GPI2  | I            | PRU-ICSSG PRU Data Input  | V3          |
| PRG0_PRU1_GPI3  | I            | PRU-ICSSG PRU Data Input  | T4          |
| PRG0_PRU1_GPI4  | I            | PRU-ICSSG PRU Data Input  | W3          |
| PRG0_PRU1_GPI5  | I            | PRU-ICSSG PRU Data Input  | P4          |
| PRG0_PRU1_GPI6  | I            | PRU-ICSSG PRU Data Input  | R5          |
| PRG0_PRU1_GPI7  | I            | PRU-ICSSG PRU Data Input  | W5          |
| PRG0_PRU1_GPI8  | I            | PRU-ICSSG PRU Data Input  | R1          |
| PRG0_PRU1_GPI9  | I            | PRU-ICSSG PRU Data Input  | Y5          |
| PRG0_PRU1_GPI10 | I            | PRU-ICSSG PRU Data Input  | V6          |
| PRG0_PRU1_GPI11 | I            | PRU-ICSSG PRU Data Input  | W4          |
| PRG0_PRU1_GPI12 | I            | PRU-ICSSG PRU Data Input  | Y4          |
| PRG0_PRU1_GPI13 | I            | PRU-ICSSG PRU Data Input  | T6          |
| PRG0_PRU1_GPI14 | I            | PRU-ICSSG PRU Data Input  | U6          |
| PRG0_PRU1_GPI15 | I            | PRU-ICSSG PRU Data Input  | U5          |
| PRG0_PRU1_GPI16 | I            | PRU-ICSSG PRU Data Input  | AA4         |
| PRG0_PRU1_GPI17 | I            | PRU-ICSSG PRU Data Input  | V5          |
| PRG0_PRU1_GPI18 | I            | PRU-ICSSG PRU Data Input  | P5          |
| PRG0_PRU1_GPI19 | I            | PRU-ICSSG PRU Data Input  | R2          |
| PRG0_PRU1_GPO0  | IO           | PRU-ICSSG PRU Data Output | Y2          |
| PRG0_PRU1_GPO1  | IO           | PRU-ICSSG PRU Data Output | W2          |
| PRG0_PRU1_GPO2  | IO           | PRU-ICSSG PRU Data Output | V3          |
| PRG0_PRU1_GPO3  | IO           | PRU-ICSSG PRU Data Output | T4          |
| PRG0_PRU1_GPO4  | IO           | PRU-ICSSG PRU Data Output | W3          |
| PRG0_PRU1_GPO5  | IO           | PRU-ICSSG PRU Data Output | P4          |
| PRG0_PRU1_GPO6  | IO           | PRU-ICSSG PRU Data Output | R5          |
| PRG0_PRU1_GPO7  | IO           | PRU-ICSSG PRU Data Output | W5          |
| PRG0_PRU1_GPO8  | IO           | PRU-ICSSG PRU Data Output | R1          |
| PRG0_PRU1_GPO9  | IO           | PRU-ICSSG PRU Data Output | Y5          |
| PRG0_PRU1_GPO10 | IO           | PRU-ICSSG PRU Data Output | V6          |
| PRG0_PRU1_GPO11 | IO           | PRU-ICSSG PRU Data Output | W4          |
| PRG0_PRU1_GPO12 | IO           | PRU-ICSSG PRU Data Output | Y4          |
| PRG0_PRU1_GPO13 | IO           | PRU-ICSSG PRU Data Output | T6          |
| PRG0_PRU1_GPO14 | IO           | PRU-ICSSG PRU Data Output | U6          |
| PRG0_PRU1_GPO15 | IO           | PRU-ICSSG PRU Data Output | U5          |
| PRG0_PRU1_GPO16 | IO           | PRU-ICSSG PRU Data Output | AA4         |
| PRG0_PRU1_GPO17 | IO           | PRU-ICSSG PRU Data Output | V5          |
| PRG0_PRU1_GPO18 | IO           | PRU-ICSSG PRU Data Output | P5          |

**表 5-59. PRU\_ICSSG0 Signal Descriptions (続き)**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]                  | ALV PIN [4] |
|--------------------|--------------|----------------------------------|-------------|
| PRG0_PRU1_GPO19    | IO           | PRU-ICSSG PRU Data Output        | R2          |
| PRG0_PWM0_TZ_IN    | I            | PRU_ICSSG PWM Trip Zone Input    | V1          |
| PRG0_PWM0_TZ_OUT   | O            | PRU_ICSSG PWM Trip Zone Output   | W1          |
| PRG0_PWM1_TZ_IN    | I            | PRU_ICSSG PWM Trip Zone Input    | P5          |
| PRG0_PWM1_TZ_OUT   | O            | PRU_ICSSG PWM Trip Zone Output   | R2          |
| PRG0_PWM2_TZ_IN    | I            | PRU_ICSSG PWM Trip Zone Input    | T18, V6     |
| PRG0_PWM2_TZ_OUT   | O            | PRU_ICSSG PWM Trip Zone Output   | R1, U21     |
| PRG0_PWM3_TZ_IN    | I            | PRU_ICSSG PWM Trip Zone Input    | P16, W6     |
| PRG0_PWM3_TZ_OUT   | O            | PRU_ICSSG PWM Trip Zone Output   | R17, Y3     |
| PRG0_PWM0_A0       | IO           | PRU_ICSSG PWM Output A           | AA3         |
| PRG0_PWM0_A1       | IO           | PRU_ICSSG PWM Output A           | V4          |
| PRG0_PWM0_A2       | IO           | PRU_ICSSG PWM Output A           | U4          |
| PRG0_PWM0_B0       | IO           | PRU_ICSSG PWM Output B           | R6          |
| PRG0_PWM0_B1       | IO           | PRU_ICSSG PWM Output B           | T5          |
| PRG0_PWM0_B2       | IO           | PRU_ICSSG PWM Output B           | U1          |
| PRG0_PWM1_A0       | IO           | PRU_ICSSG PWM Output A           | Y4          |
| PRG0_PWM1_A1       | IO           | PRU_ICSSG PWM Output A           | U6          |
| PRG0_PWM1_A2       | IO           | PRU_ICSSG PWM Output A           | AA4         |
| PRG0_PWM1_B0       | IO           | PRU_ICSSG PWM Output B           | T6          |
| PRG0_PWM1_B1       | IO           | PRU_ICSSG PWM Output B           | U5          |
| PRG0_PWM1_B2       | IO           | PRU_ICSSG PWM Output B           | V5          |
| PRG0_PWM2_A0       | IO           | PRU_ICSSG PWM Output A           | U2, U20     |
| PRG0_PWM2_A1       | IO           | PRU_ICSSG PWM Output A           | T2, U19     |
| PRG0_PWM2_A2       | IO           | PRU_ICSSG PWM Output A           | V19, V3     |
| PRG0_PWM2_B0       | IO           | PRU_ICSSG PWM Output B           | AA2, U18    |
| PRG0_PWM2_B1       | IO           | PRU_ICSSG PWM Output B           | AA5, V20    |
| PRG0_PWM2_B2       | IO           | PRU_ICSSG PWM Output B           | T17, W3     |
| PRG0_PWM3_A0       | IO           | PRU_ICSSG PWM Output A           | V18, Y1     |
| PRG0_PWM3_A1       | IO           | PRU_ICSSG PWM Output A           | R18, T3     |
| PRG0_PWM3_A2       | IO           | PRU_ICSSG PWM Output A           | T19, V2     |
| PRG0_PWM3_B0       | IO           | PRU_ICSSG PWM Output B           | R4, Y21     |
| PRG0_PWM3_B1       | IO           | PRU_ICSSG PWM Output B           | T1, T21     |
| PRG0_PWM3_B2       | IO           | PRU_ICSSG PWM Output B           | R3, W19     |
| PRG0_RGMII1_RXC    | I            | PRU_ICSSG RGMII Receive Clock    | T3          |
| PRG0_RGMII1_RX_CTL | I            | PRU_ICSSG RGMII Receive Control  | AA2         |
| PRG0_RGMII1_TXC    | IO           | PRU_ICSSG RGMII Transmit Clock   | U4          |
| PRG0_RGMII1_TX_CTL | O            | PRU_ICSSG RGMII Transmit Control | T5          |
| PRG0_RGMII2_RXC    | I            | PRU_ICSSG RGMII Receive Clock    | R5          |
| PRG0_RGMII2_RX_CTL | I            | PRU_ICSSG RGMII Receive Control  | W3          |
| PRG0_RGMII2_TXC    | IO           | PRU_ICSSG RGMII Transmit Clock   | AA4         |
| PRG0_RGMII2_TX_CTL | O            | PRU_ICSSG RGMII Transmit Control | U5          |
| PRG0_RGMII1_RD0    | I            | PRU_ICSSG RGMII Receive Data     | Y1          |
| PRG0_RGMII1_RD1    | I            | PRU_ICSSG RGMII Receive Data     | R4          |
| PRG0_RGMII1_RD2    | I            | PRU_ICSSG RGMII Receive Data     | U2          |
| PRG0_RGMII1_RD3    | I            | PRU_ICSSG RGMII Receive Data     | V2          |

表 5-59. PRU\_ICSSG0 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                             | ALV PIN [4] |
|-----------------|--------------|---------------------------------------------|-------------|
| PRG0_RGMII1_TD0 | O            | PRU_ICSSG RGMII Transmit Data               | Y3          |
| PRG0_RGMII1_TD1 | O            | PRU_ICSSG RGMII Transmit Data               | AA3         |
| PRG0_RGMII1_TD2 | O            | PRU_ICSSG RGMII Transmit Data               | R6          |
| PRG0_RGMII1_TD3 | O            | PRU_ICSSG RGMII Transmit Data               | V4          |
| PRG0_RGMII2_RD0 | I            | PRU_ICSSG RGMII Receive Data                | Y2          |
| PRG0_RGMII2_RD1 | I            | PRU_ICSSG RGMII Receive Data                | W2          |
| PRG0_RGMII2_RD2 | I            | PRU_ICSSG RGMII Receive Data                | V3          |
| PRG0_RGMII2_RD3 | I            | PRU_ICSSG RGMII Receive Data                | T4          |
| PRG0_RGMII2_TD0 | O            | PRU_ICSSG RGMII Transmit Data               | W4          |
| PRG0_RGMII2_TD1 | O            | PRU_ICSSG RGMII Transmit Data               | Y4          |
| PRG0_RGMII2_TD2 | O            | PRU_ICSSG RGMII Transmit Data               | T6          |
| PRG0_RGMII2_TD3 | O            | PRU_ICSSG RGMII Transmit Data               | U6          |
| PRG0_UART0_CTSn | I            | PRU-ICSSG UART Clear to Send (active low)   | W6          |
| PRG0_UART0_RTSn | O            | PRU-ICSSG UART Request to Send (active low) | AA5         |
| PRG0_UART0_RXD  | I            | PRU-ICSSG UART Receive Data                 | Y5          |
| PRG0_UART0_TXD  | O            | PRU-ICSSG UART Transmit Data                | V6          |

表 5-60. PRU\_ICSSG1 Signal Descriptions

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                                        | ALV PIN [4] |
|------------------------------|--------------|------------------------------------------------------------------------|-------------|
| PRG1_ECAP0_IN_APWM_OUT       | IO           | PRU-ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | V12         |
| PRG1_ECAP0_SYNC_IN           | I            | PRU-ICSSG ECAP Sync Input                                              | Y13         |
| PRG1_ECAP0_SYNC_OUT          | O            | PRU-ICSSG ECAP Sync Output                                             | AA14        |
| PRG1_IEP0_EDIO_OUTVALID      | O            | PRU_ICSSG Industrial Ethernet Digital I/O Outvalid                     | D14         |
| PRG1_IEP0_EDC_LATCH_IN0      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | V7          |
| PRG1_IEP0_EDC_LATCH_IN1      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | U13         |
| PRG1_IEP0_EDC_SYNC_OUT0      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | W7          |
| PRG1_IEP0_EDC_SYNC_OUT1      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | U7          |
| PRG1_IEP0_EDIO_DATA_IN_OUT28 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | U15         |
| PRG1_IEP0_EDIO_DATA_IN_OUT29 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | U14         |
| PRG1_IEP0_EDIO_DATA_IN_OUT30 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | V14         |
| PRG1_IEP0_EDIO_DATA_IN_OUT31 | IO           | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | W14         |
| PRG1_IEP1_EDC_LATCH_IN0      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | Y13         |
| PRG1_IEP1_EDC_LATCH_IN1      | I            | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | V15         |
| PRG1_IEP1_EDC_SYNC_OUT0      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | V12         |
| PRG1_IEP1_EDC_SYNC_OUT1      | O            | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | AA14        |
| PRG1_MDIO0_MDC               | O            | PRU-ICSSG MDIO Clock                                                   | Y6          |

**表 5-60. PRU\_ICSSG1 Signal Descriptions (続き)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]           | ALV PIN [4] |
|-----------------|--------------|---------------------------|-------------|
| PRG1_MDIO0_MDIO | IO           | PRU-ICSSG MDIO Data       | AA6         |
| PRG1_PRU0_GPI0  | I            | PRU-ICSSG PRU Data Input  | Y7          |
| PRG1_PRU0_GPI1  | I            | PRU-ICSSG PRU Data Input  | U8          |
| PRG1_PRU0_GPI2  | I            | PRU-ICSSG PRU Data Input  | W8          |
| PRG1_PRU0_GPI3  | I            | PRU-ICSSG PRU Data Input  | V8          |
| PRG1_PRU0_GPI4  | I            | PRU-ICSSG PRU Data Input  | Y8          |
| PRG1_PRU0_GPI5  | I            | PRU-ICSSG PRU Data Input  | V13         |
| PRG1_PRU0_GPI6  | I            | PRU-ICSSG PRU Data Input  | AA7         |
| PRG1_PRU0_GPI7  | I            | PRU-ICSSG PRU Data Input  | U13         |
| PRG1_PRU0_GPI8  | I            | PRU-ICSSG PRU Data Input  | W13         |
| PRG1_PRU0_GPI9  | I            | PRU-ICSSG PRU Data Input  | U15         |
| PRG1_PRU0_GPI10 | I            | PRU-ICSSG PRU Data Input  | U14         |
| PRG1_PRU0_GPI11 | I            | PRU-ICSSG PRU Data Input  | AA8         |
| PRG1_PRU0_GPI12 | I            | PRU-ICSSG PRU Data Input  | U9          |
| PRG1_PRU0_GPI13 | I            | PRU-ICSSG PRU Data Input  | W9          |
| PRG1_PRU0_GPI14 | I            | PRU-ICSSG PRU Data Input  | AA9         |
| PRG1_PRU0_GPI15 | I            | PRU-ICSSG PRU Data Input  | Y9          |
| PRG1_PRU0_GPI16 | I            | PRU-ICSSG PRU Data Input  | V9          |
| PRG1_PRU0_GPI17 | I            | PRU-ICSSG PRU Data Input  | U7          |
| PRG1_PRU0_GPI18 | I            | PRU-ICSSG PRU Data Input  | V7          |
| PRG1_PRU0_GPI19 | I            | PRU-ICSSG PRU Data Input  | W7          |
| PRG1_PRU0_GPO0  | IO           | PRU-ICSSG PRU Data Output | Y7          |
| PRG1_PRU0_GPO1  | IO           | PRU-ICSSG PRU Data Output | U8          |
| PRG1_PRU0_GPO2  | IO           | PRU-ICSSG PRU Data Output | W8          |
| PRG1_PRU0_GPO3  | IO           | PRU-ICSSG PRU Data Output | V8          |
| PRG1_PRU0_GPO4  | IO           | PRU-ICSSG PRU Data Output | Y8          |
| PRG1_PRU0_GPO5  | IO           | PRU-ICSSG PRU Data Output | V13         |
| PRG1_PRU0_GPO6  | IO           | PRU-ICSSG PRU Data Output | AA7         |
| PRG1_PRU0_GPO7  | IO           | PRU-ICSSG PRU Data Output | U13         |
| PRG1_PRU0_GPO8  | IO           | PRU-ICSSG PRU Data Output | W13         |
| PRG1_PRU0_GPO9  | IO           | PRU-ICSSG PRU Data Output | U15         |
| PRG1_PRU0_GPO10 | IO           | PRU-ICSSG PRU Data Output | U14         |
| PRG1_PRU0_GPO11 | IO           | PRU-ICSSG PRU Data Output | AA8         |
| PRG1_PRU0_GPO12 | IO           | PRU-ICSSG PRU Data Output | U9          |
| PRG1_PRU0_GPO13 | IO           | PRU-ICSSG PRU Data Output | W9          |
| PRG1_PRU0_GPO14 | IO           | PRU-ICSSG PRU Data Output | AA9         |
| PRG1_PRU0_GPO15 | IO           | PRU-ICSSG PRU Data Output | Y9          |
| PRG1_PRU0_GPO16 | IO           | PRU-ICSSG PRU Data Output | V9          |
| PRG1_PRU0_GPO17 | IO           | PRU-ICSSG PRU Data Output | U7          |
| PRG1_PRU0_GPO18 | IO           | PRU-ICSSG PRU Data Output | V7          |
| PRG1_PRU0_GPO19 | IO           | PRU-ICSSG PRU Data Output | W7          |
| PRG1_PRU1_GPI0  | I            | PRU-ICSSG PRU Data Input  | W11         |
| PRG1_PRU1_GPI1  | I            | PRU-ICSSG PRU Data Input  | V11         |
| PRG1_PRU1_GPI2  | I            | PRU-ICSSG PRU Data Input  | AA12        |
| PRG1_PRU1_GPI3  | I            | PRU-ICSSG PRU Data Input  | Y12         |

表 5-60. PRU\_ICSSG1 Signal Descriptions (続き)

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                | ALV PIN [4] |
|------------------|--------------|--------------------------------|-------------|
| PRG1_PRU1_GPI4   | I            | PRU-ICSSG PRU Data Input       | W12         |
| PRG1_PRU1_GPI5   | I            | PRU-ICSSG PRU Data Input       | AA13        |
| PRG1_PRU1_GPI6   | I            | PRU-ICSSG PRU Data Input       | U11         |
| PRG1_PRU1_GPI7   | I            | PRU-ICSSG PRU Data Input       | V15         |
| PRG1_PRU1_GPI8   | I            | PRU-ICSSG PRU Data Input       | U12         |
| PRG1_PRU1_GPI9   | I            | PRU-ICSSG PRU Data Input       | V14         |
| PRG1_PRU1_GPI10  | I            | PRU-ICSSG PRU Data Input       | W14         |
| PRG1_PRU1_GPI11  | I            | PRU-ICSSG PRU Data Input       | AA10        |
| PRG1_PRU1_GPI12  | I            | PRU-ICSSG PRU Data Input       | V10         |
| PRG1_PRU1_GPI13  | I            | PRU-ICSSG PRU Data Input       | U10         |
| PRG1_PRU1_GPI14  | I            | PRU-ICSSG PRU Data Input       | AA11        |
| PRG1_PRU1_GPI15  | I            | PRU-ICSSG PRU Data Input       | Y11         |
| PRG1_PRU1_GPI16  | I            | PRU-ICSSG PRU Data Input       | Y10         |
| PRG1_PRU1_GPI17  | I            | PRU-ICSSG PRU Data Input       | AA14        |
| PRG1_PRU1_GPI18  | I            | PRU-ICSSG PRU Data Input       | Y13         |
| PRG1_PRU1_GPI19  | I            | PRU-ICSSG PRU Data Input       | V12         |
| PRG1_PRU1_GPO0   | IO           | PRU-ICSSG PRU Data Output      | W11         |
| PRG1_PRU1_GPO1   | IO           | PRU-ICSSG PRU Data Output      | V11         |
| PRG1_PRU1_GPO2   | IO           | PRU-ICSSG PRU Data Output      | AA12        |
| PRG1_PRU1_GPO3   | IO           | PRU-ICSSG PRU Data Output      | Y12         |
| PRG1_PRU1_GPO4   | IO           | PRU-ICSSG PRU Data Output      | W12         |
| PRG1_PRU1_GPO5   | IO           | PRU-ICSSG PRU Data Output      | AA13        |
| PRG1_PRU1_GPO6   | IO           | PRU-ICSSG PRU Data Output      | U11         |
| PRG1_PRU1_GPO7   | IO           | PRU-ICSSG PRU Data Output      | V15         |
| PRG1_PRU1_GPO8   | IO           | PRU-ICSSG PRU Data Output      | U12         |
| PRG1_PRU1_GPO9   | IO           | PRU-ICSSG PRU Data Output      | V14         |
| PRG1_PRU1_GPO10  | IO           | PRU-ICSSG PRU Data Output      | W14         |
| PRG1_PRU1_GPO11  | IO           | PRU-ICSSG PRU Data Output      | AA10        |
| PRG1_PRU1_GPO12  | IO           | PRU-ICSSG PRU Data Output      | V10         |
| PRG1_PRU1_GPO13  | IO           | PRU-ICSSG PRU Data Output      | U10         |
| PRG1_PRU1_GPO14  | IO           | PRU-ICSSG PRU Data Output      | AA11        |
| PRG1_PRU1_GPO15  | IO           | PRU-ICSSG PRU Data Output      | Y11         |
| PRG1_PRU1_GPO16  | IO           | PRU-ICSSG PRU Data Output      | Y10         |
| PRG1_PRU1_GPO17  | IO           | PRU-ICSSG PRU Data Output      | AA14        |
| PRG1_PRU1_GPO18  | IO           | PRU-ICSSG PRU Data Output      | Y13         |
| PRG1_PRU1_GPO19  | IO           | PRU-ICSSG PRU Data Output      | V12         |
| PRG1_PWM0_TZ_IN  | I            | PRU_ICSSG PWM Trip Zone Input  | V7          |
| PRG1_PWM0_TZ_OUT | O            | PRU_ICSSG PWM Trip Zone Output | W7          |
| PRG1_PWM1_TZ_IN  | I            | PRU_ICSSG PWM Trip Zone Input  | Y13         |
| PRG1_PWM1_TZ_OUT | O            | PRU_ICSSG PWM Trip Zone Output | V12         |
| PRG1_PWM2_TZ_IN  | I            | PRU_ICSSG PWM Trip Zone Input  | P19, W14    |
| PRG1_PWM2_TZ_OUT | O            | PRU_ICSSG PWM Trip Zone Output | R20, U12    |
| PRG1_PWM3_TZ_IN  | I            | PRU_ICSSG PWM Trip Zone Input  | U15         |
| PRG1_PWM3_TZ_OUT | O            | PRU_ICSSG PWM Trip Zone Output | AA8         |
| PRG1_PWM0_A0     | IO           | PRU_ICSSG PWM Output A         | U9          |

**表 5-60. PRU\_ICSSG1 Signal Descriptions (続き)**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]                  | ALV PIN [4] |
|--------------------|--------------|----------------------------------|-------------|
| PRG1_PWM0_A1       | IO           | PRU_ICSSG PWM Output A           | AA9         |
| PRG1_PWM0_A2       | IO           | PRU_ICSSG PWM Output A           | V9          |
| PRG1_PWM0_B0       | IO           | PRU_ICSSG PWM Output B           | W9          |
| PRG1_PWM0_B1       | IO           | PRU_ICSSG PWM Output B           | Y9          |
| PRG1_PWM0_B2       | IO           | PRU_ICSSG PWM Output B           | U7          |
| PRG1_PWM1_A0       | IO           | PRU_ICSSG PWM Output A           | V10         |
| PRG1_PWM1_A1       | IO           | PRU_ICSSG PWM Output A           | AA11        |
| PRG1_PWM1_A2       | IO           | PRU_ICSSG PWM Output A           | Y10         |
| PRG1_PWM1_B0       | IO           | PRU_ICSSG PWM Output B           | U10         |
| PRG1_PWM1_B1       | IO           | PRU_ICSSG PWM Output B           | Y11         |
| PRG1_PWM1_B2       | IO           | PRU_ICSSG PWM Output B           | AA14        |
| PRG1_PWM2_A0       | IO           | PRU_ICSSG PWM Output A           | N16, W8     |
| PRG1_PWM2_A1       | IO           | PRU_ICSSG PWM Output A           | P17, W13    |
| PRG1_PWM2_A2       | IO           | PRU_ICSSG PWM Output A           | AA12, V21   |
| PRG1_PWM2_B0       | IO           | PRU_ICSSG PWM Output B           | N17, Y8     |
| PRG1_PWM2_B1       | IO           | PRU_ICSSG PWM Output B           | U14, Y18    |
| PRG1_PWM2_B2       | IO           | PRU_ICSSG PWM Output B           | R16, W12    |
| PRG1_PWM3_A0       | IO           | PRU_ICSSG PWM Output A           | Y7          |
| PRG1_PWM3_A1       | IO           | PRU_ICSSG PWM Output A           | AA7         |
| PRG1_PWM3_A2       | IO           | PRU_ICSSG PWM Output A           | V8          |
| PRG1_PWM3_B0       | IO           | PRU_ICSSG PWM Output B           | U8          |
| PRG1_PWM3_B1       | IO           | PRU_ICSSG PWM Output B           | U13         |
| PRG1_PWM3_B2       | IO           | PRU_ICSSG PWM Output B           | V13         |
| PRG1_RGMII1_RXC    | I            | PRU_ICSSG RGMII Receive Clock    | AA7         |
| PRG1_RGMII1_RX_CTL | I            | PRU_ICSSG RGMII Receive Control  | Y8          |
| PRG1_RGMII1_TXC    | IO           | PRU_ICSSG RGMII Transmit Clock   | V9          |
| PRG1_RGMII1_TX_CTL | O            | PRU_ICSSG RGMII Transmit Control | Y9          |
| PRG1_RGMII2_RXC    | I            | PRU_ICSSG RGMII Receive Clock    | U11         |
| PRG1_RGMII2_RX_CTL | I            | PRU_ICSSG RGMII Receive Control  | W12         |
| PRG1_RGMII2_TXC    | IO           | PRU_ICSSG RGMII Transmit Clock   | Y10         |
| PRG1_RGMII2_TX_CTL | O            | PRU_ICSSG RGMII Transmit Control | Y11         |
| PRG1_RGMII1_RD0    | I            | PRU_ICSSG RGMII Receive Data     | Y7          |
| PRG1_RGMII1_RD1    | I            | PRU_ICSSG RGMII Receive Data     | U8          |
| PRG1_RGMII1_RD2    | I            | PRU_ICSSG RGMII Receive Data     | W8          |
| PRG1_RGMII1_RD3    | I            | PRU_ICSSG RGMII Receive Data     | V8          |
| PRG1_RGMII1_TD0    | O            | PRU_ICSSG RGMII Transmit Data    | AA8         |
| PRG1_RGMII1_TD1    | O            | PRU_ICSSG RGMII Transmit Data    | U9          |
| PRG1_RGMII1_TD2    | O            | PRU_ICSSG RGMII Transmit Data    | W9          |
| PRG1_RGMII1_TD3    | O            | PRU_ICSSG RGMII Transmit Data    | AA9         |
| PRG1_RGMII2_RD0    | I            | PRU_ICSSG RGMII Receive Data     | W11         |
| PRG1_RGMII2_RD1    | I            | PRU_ICSSG RGMII Receive Data     | V11         |
| PRG1_RGMII2_RD2    | I            | PRU_ICSSG RGMII Receive Data     | AA12        |
| PRG1_RGMII2_RD3    | I            | PRU_ICSSG RGMII Receive Data     | Y12         |
| PRG1_RGMII2_TD0    | O            | PRU_ICSSG RGMII Transmit Data    | AA10        |
| PRG1_RGMII2_TD1    | O            | PRU_ICSSG RGMII Transmit Data    | V10         |

表 5-60. PRU\_ICSSG1 Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                             | ALV PIN [4] |
|-----------------|--------------|---------------------------------------------|-------------|
| PRG1_RGMII2_TD2 | O            | PRU_ICSSG RGMII Transmit Data               | U10         |
| PRG1_RGMII2_TD3 | O            | PRU_ICSSG RGMII Transmit Data               | AA11        |
| PRG1_UART0_CTSn | I            | PRU-ICSSG UART Clear to Send (active low)   | U15         |
| PRG1_UART0_RTSn | O            | PRU-ICSSG UART Request to Send (active low) | U14         |
| PRG1_UART0_RXD  | I            | PRU-ICSSG UART Receive Data                 | V14         |
| PRG1_UART0_TXD  | O            | PRU-ICSSG UART Transmit Data                | W14         |

### 5.3.20 Reserved

表 5-61. Reserved Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                    | ALV PIN [4] |
|-----------------|--------------|------------------------------------|-------------|
| RSVD0           | N/A          | Reserved, must be left unconnected | H16         |
| RSVD1           | N/A          | Reserved, must be left unconnected | D21         |
| RSVD2           | N/A          | Reserved, must be left unconnected | G13         |
| RSVD3           | N/A          | Reserved, must be left unconnected | F17         |
| RSVD4           | N/A          | Reserved, must be left unconnected | W15         |
| RSVD5           | N/A          | Reserved, must be left unconnected | V16         |
| RSVD6           | N/A          | Reserved, must be left unconnected | K2          |
| RSVD7           | N/A          | Reserved, must be left unconnected | K1          |
| RSVD8           | N/A          | Reserved, must be left unconnected | F12         |

### 5.3.21 SERDES

#### 5.3.21.1 MAIN Domain

表 5-62. SERDES0 Signal Descriptions

| SIGNAL NAME [1] (2) | PIN TYPE [2] | DESCRIPTION [3]                                    | ALV PIN [4] |
|---------------------|--------------|----------------------------------------------------|-------------|
| PCIE0_CLKREQn       | IO           | PCIE Clock Request Signal                          | D16         |
| SERDES0_REXT (1)    | A            | External SerDes PHY Calibration Resistor           | T13         |
| SERDES0_REFCLK0N    | IO           | SerDes PHY Reference Clock Input/Output (negative) | W16         |
| SERDES0_REFCLK0P    | IO           | SerDes PHY Reference Clock Input/Output (positive) | W17         |
| SERDES0_RX0_N       | I            | SerDes PHY Differential Receive Data (negative)    | Y15         |
| SERDES0_RX0_P       | I            | SerDes PHY Differential Receive Data (positive)    | Y16         |
| SERDES0_TX0_N       | O            | SerDes PHY Differential Transmit Data (negative)   | AA16        |
| SERDES0_TX0_P       | O            | SerDes PHY Differential Transmit Data (positive)   | AA17        |

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

(2) The functionality of these pins is controlled by SERDES0\_LN0\_CTRL\_LANE\_FUNC\_SEL.

### 5.3.22 System and Miscellaneous

#### 5.3.22.1 Boot Mode Configuration

##### 5.3.22.1.1 MAIN Domain

表 5-63. Sysboot Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| BOOTMODE00      | I            | Bootmode pin 0  | T20         |
| BOOTMODE01      | I            | Bootmode pin 1  | U21         |
| BOOTMODE02      | I            | Bootmode pin 2  | T18         |
| BOOTMODE03      | I            | Bootmode pin 3  | U20         |
| BOOTMODE04      | I            | Bootmode pin 4  | U18         |

表 5-63. Sysboot Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALV PIN [4] |
|-----------------|--------------|-----------------|-------------|
| BOOTMODE05      | I            | Bootmode pin 5  | U19         |
| BOOTMODE06      | I            | Bootmode pin 6  | V20         |
| BOOTMODE07      | I            | Bootmode pin 7  | V21         |
| BOOTMODE08      | I            | Bootmode pin 8  | V19         |
| BOOTMODE09      | I            | Bootmode pin 9  | T17         |
| BOOTMODE10      | I            | Bootmode pin 10 | R16         |
| BOOTMODE11      | I            | Bootmode pin 11 | W20         |
| BOOTMODE12      | I            | Bootmode pin 12 | W21         |
| BOOTMODE13      | I            | Bootmode pin 13 | V18         |
| BOOTMODE14      | I            | Bootmode pin 14 | Y21         |
| BOOTMODE15      | I            | Bootmode pin 15 | Y20         |

### 5.3.22.2 Clock

#### 5.3.22.2.1 MCU Domain

表 5-64. MCU Clock Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALV PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCU_OSC0_XI     | I            | High frequency oscillator input  | C21         |
| MCU_OSC0_XO     | O            | High frequency oscillator output | B20         |

### 5.3.22.3 System

#### 5.3.22.3.1 MAIN Domain

表 5-65. System Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                                                                                    | ALV PIN [4] |
|-----------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| CLKOUT0         | O            | RMII Clock Output (50 MHz). This pin is used for clock source to the external PHY and must be routed back to the RMII_REF_CLK pin for proper device operation.                     | A19, U13    |
| EXTINTn         | I            | External Interrupt                                                                                                                                                                 | C19         |
| EXT_REFCLK1     | I            | External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL) | A19         |
| OBSCLK0         | O            | Observation clock output for test and debug purposes only                                                                                                                          | D17         |
| PORz_OUT        | O            | Main Domain POR status output                                                                                                                                                      | E17         |
| RESETSTATz      | O            | Main Domain warm reset status output                                                                                                                                               | F16         |
| RESET_REQz      | I            | Main Domain external warm reset request input                                                                                                                                      | E18         |
| SYSCLKOUT0      | O            | SYSCLK0 output from Main PLL controller (divided by 6) for test and debug purposes only                                                                                            | C17         |

#### 5.3.22.3.2 MCU Domain

表 5-66. MCU System Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                           | ALV PIN [4] |
|-----------------|--------------|-----------------------------------------------------------|-------------|
| MCU_EXT_REFCLK0 | I            | External system clock input                               | B7          |
| MCU_OBSCLK0     | O            | Observation clock output for test and debug purposes only | C6, E10     |
| MCU_PORz        | I            | MCU Domain cold reset                                     | B21         |
| MCU_RESETSTATz  | O            | MCU Domain warm reset status output                       | B13         |

表 5-66. MCU System Signal Descriptions (続き)

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                                 | ALV PIN [4] |
|-------------------|--------------|-----------------------------------------------------------------|-------------|
| MCU_RESETz        | I            | MCU Domain warm reset                                           | B12         |
| MCU_SAFETY_ERRORn | IO           | Error signal output from MCU Domain ESM                         | A20         |
| MCU_SYSCLKOUT0    | O            | MCU Domain system clock output for test and debug purposes only | C6          |

## 5.3.22.4 VMON

表 5-67. VMON Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                                                                    | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| VMON_1P8_MCU    | A            | Voltage monitor input for 1.8 V MCU power supply                                                                                                                   | K16         |
| VMON_1P8_SOC    | A            | Voltage monitor input for 1.8 V SoC power supply                                                                                                                   | E12         |
| VMON_3P3_MCU    | A            | Voltage monitor input for 3.3 V MCU power supply                                                                                                                   | F13         |
| VMON_3P3_SOC    | A            | Voltage monitor input for 3.3 V SoC power supply                                                                                                                   | F14         |
| VMON_VSYS       | A            | Voltage monitor input, fixed 0.45 V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply. | K10         |

## 5.3.23 TIMER

## 5.3.23.1 MAIN Domain

表 5-68. TIMER Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4]  |
|-----------------|--------------|--------------------------------------------------------------|--------------|
| TIMER_IO0       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | C18, K18     |
| TIMER_IO1       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | B19, K19     |
| TIMER_IO2       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | A17, L21     |
| TIMER_IO3       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | B17, K21     |
| TIMER_IO4       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | C17, L20     |
| TIMER_IO5       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | D17, J19     |
| TIMER_IO6       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | B16, D19, T1 |
| TIMER_IO7       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | A16, C20, U7 |
| TIMER_IO8       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | P19, V7      |
| TIMER_IO9       | IO           | Timer Inputs and Outputs (not tied to single timer instance) | R21, W7      |
| TIMER_IO10      | IO           | Timer Inputs and Outputs (not tied to single timer instance) | C13, U13     |
| TIMER_IO11      | IO           | Timer Inputs and Outputs (not tied to single timer instance) | D14, U1      |

## 5.3.23.2 MCU Domain

表 5-69. MCU\_TIMER Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------------------------|-------------|
| MCU_TIMER_IO0   | IO           | Timer Inputs and Outputs (not tied to single timer instance) | D8          |

表 5-69. MCU\_TIMER Signal Descriptions (続き)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                              | ALV PIN [4] |
|-----------------|--------------|--------------------------------------------------------------|-------------|
| MCU_TIMER_IO1   | IO           | Timer Inputs and Outputs (not tied to single timer instance) | E8          |
| MCU_TIMER_IO2   | IO           | Timer Inputs and Outputs (not tied to single timer instance) | B8          |
| MCU_TIMER_IO3   | IO           | Timer Inputs and Outputs (not tied to single timer instance) | B9          |

### 5.3.24 UART

#### 5.3.24.1 MAIN Domain

表 5-70. UART0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALV PIN [4] |
|-----------------|--------------|---------------------------------------|-------------|
| UART0_CTSn      | I            | UART Clear to Send (active low)       | B16         |
| UART0_DCDn      | I            | UART Data Carrier Detect (active low) | C17         |
| UART0_DSRn      | I            | UART Data Set Ready (active low)      | D17         |
| UART0_DTRn      | O            | UART Data Terminal Ready (active low) | A17         |
| UART0_RIn       | I            | UART Ring Indicator                   | B17         |
| UART0_RTSn      | O            | UART Request to Send (active low)     | A16         |
| UART0_RXD       | I            | UART Receive Data                     | D15         |
| UART0_TXD       | O            | UART Transmit Data                    | C16         |

表 5-71. UART1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART1_CTSn      | I            | UART Clear to Send (active low)   | D16         |
| UART1_RTSn      | O            | UART Request to Send (active low) | E16         |
| UART1_RXD       | I            | UART Receive Data                 | E15         |
| UART1_TXD       | O            | UART Transmit Data                | E14         |

表 5-72. UART2 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4]           |
|-----------------|--------------|-----------------------------------|-----------------------|
| UART2_CTSn      | I            | UART Clear to Send (active low)   | L20, V19, Y1          |
| UART2_RTSn      | O            | UART Request to Send (active low) | J19, T18, U2          |
| UART2_RXD       | I            | UART Receive Data                 | B16, K18, T20, V1, W6 |
| UART2_TXD       | O            | UART Transmit Data                | A16, K19, R4, U21     |

表 5-73. UART3 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4]            |
|-----------------|--------------|-----------------------------------|------------------------|
| UART3_CTSn      | I            | UART Clear to Send (active low)   | D19, T17, V2           |
| UART3_RTSn      | O            | UART Request to Send (active low) | C20, R3, U19           |
| UART3_RXD       | I            | UART Receive Data                 | AA5, D16, L21, U20, W1 |
| UART3_TXD       | O            | UART Transmit Data                | AA2, E16, K21, U18     |

**表 5-74. UART4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4]               |
|-----------------|--------------|-----------------------------------|---------------------------|
| UART4_CTSn      | I            | UART Clear to Send (active low)   | R16, R5, T3, V1           |
| UART4_RTSn      | O            | UART Request to Send (active low) | R1, R17, T2, W1           |
| UART4_RXD       | I            | UART Receive Data                 | A17, L20, V20, W4, Y3     |
| UART4_TXD       | O            | UART Transmit Data                | B17, J19, T1, V21, W5, Y4 |

**表 5-75. UART5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4]           |
|-----------------|--------------|-----------------------------------|-----------------------|
| UART5_CTSn      | I            | UART Clear to Send (active low)   | W20, Y13, Y2          |
| UART5_RTSn      | O            | UART Request to Send (active low) | T21, V12, V3          |
| UART5_RXD       | I            | UART Receive Data                 | C17, D19, P16, T6, Y5 |
| UART5_TXD       | O            | UART Transmit Data                | C20, D17, R18, W2     |

**表 5-76. UART6 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4]      |
|-----------------|--------------|-----------------------------------|------------------|
| UART6_CTSn      | I            | UART Clear to Send (active low)   | T4, W21          |
| UART6_RTSn      | O            | UART Request to Send (active low) | P17, P4          |
| UART6_RXD       | I            | UART Receive Data                 | C13, U6, V6, Y21 |
| UART6_TXD       | O            | UART Transmit Data                | D14, W3, Y20     |

### 5.3.24.2 MCU Domain

**表 5-77. MCU\_UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| MCU_UART0_CTSn  | I            | UART Clear to Send (active low)   | D8          |
| MCU_UART0_RTSn  | O            | UART Request to Send (active low) | E8          |
| MCU_UART0_RXD   | I            | UART Receive Data                 | A9          |
| MCU_UART0_TXD   | O            | UART Transmit Data                | A8          |

**表 5-78. MCU\_UART1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALV PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| MCU_UART1_CTSn  | I            | UART Clear to Send (active low)   | B8          |
| MCU_UART1_RTSn  | O            | UART Request to Send (active low) | B9          |
| MCU_UART1_RXD   | I            | UART Receive Data                 | C9          |
| MCU_UART1_TXD   | O            | UART Transmit Data                | D9          |

### 5.3.25 USB

#### 5.3.25.1 MAIN Domain

**表 5-79. USB0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALV PIN [4] |
|-----------------|--------------|---------------------------------------|-------------|
| USB0_DM         | IO           | USB 2.0 Differential Data (negative)  | AA20        |
| USB0_DP         | IO           | USB 2.0 Differential Data (positive)  | AA19        |
| USB0_DRVVBUS    | O            | USB VBUS control output (active high) | E19         |

**表 5-79. USB0 Signal Descriptions (続き)**

| SIGNAL NAME [1]            | PIN TYPE [2] | DESCRIPTION [3]                        | ALV PIN [4] |
|----------------------------|--------------|----------------------------------------|-------------|
| USB0_ID                    | A            | USB 2.0 Dual-Role Device Role Select   | U16         |
| USB0_RCALIB <sup>(1)</sup> | A            | Pin to connect to calibration resistor | U17         |
| USB0_VBUS <sup>(2)</sup>   | A            | USB Level-shifted VBUS Input           | T14         |

- (1) An external 499 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
- (2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see [セクション 8.2.3](#), *USB VBUS Design Guidelines*.

## 5.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

注

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified.

注

For additional clarification, "leave unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

**表 5-80. Connectivity Requirements**

| BALL NUMBER                                                                                                  | BALL NAME                                                                                                                                                                                                          | CONNECTION REQUIREMENTS                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A20<br>D11                                                                                                   | MCU_SAFETY_ERRORn<br>TRSTn                                                                                                                                                                                         | Each of these balls must be connected to VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-down can be used to hold a valid logic low level if no PCB signal trace is connected to the ball.                                           |
| D10<br>E10<br>B12<br>E18<br>B11<br>C11<br>C12                                                                | EMU0<br>EMU1<br>MCU_RESETz<br>RESET_REQz<br>TCK<br>TDI<br>TMS                                                                                                                                                      | Each of these balls must be connected to the corresponding power supply <sup>(1)</sup> through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-up can be used to hold a valid logic high level if no PCB signal trace is connected to the ball. |
| A18<br>B18<br>E9<br>A10                                                                                      | I2C0_SCL<br>I2C0_SDA<br>MCU_I2C0_SCL<br>MCU_I2C0_SDA                                                                                                                                                               | Each of these balls must be connected to the corresponding power supply <sup>(1)</sup> through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level.                                                                                                                                                                                                     |
| T20<br>U21<br>T18<br>U20<br>U18<br>U19<br>V20<br>V21<br>V19<br>T17<br>R16<br>W20<br>W21<br>V18<br>Y21<br>Y20 | GPMC0_AD0<br>GPMC0_AD1<br>GPMC0_AD2<br>GPMC0_AD3<br>GPMC0_AD4<br>GPMC0_AD5<br>GPMC0_AD6<br>GPMC0_AD7<br>GPMC0_AD8<br>GPMC0_AD9<br>GPMC0_AD10<br>GPMC0_AD11<br>GPMC0_AD12<br>GPMC0_AD13<br>GPMC0_AD14<br>GPMC0_AD15 | Each of these balls must be connected to the corresponding power supply <sup>(1)</sup> or VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.                                                                                                                                 |
| J13<br>G20<br>F20<br>E21,<br>D20<br>G21<br>F21<br>F19<br>E20<br>J15<br>J16                                   | VDDA_ADC<br>ADC0_AIN0<br>ADC0_AIN1<br>ADC0_AIN2<br>ADC0_AIN3<br>ADC0_AIN4<br>ADC0_AIN5<br>ADC0_AIN6<br>ADC0_AIN7<br>ADC0_REFP<br>ADC0_REFN                                                                         | If the entire ADC0 is not used, each of these balls must be connected directly to VSS.                                                                                                                                                                                                                                                                                                                                     |

**表 5-80. Connectivity Requirements (続き)**

| BALL NUMBER                                           | BALL NAME                                                                                            | CONNECTION REQUIREMENTS                                                                                                                           |
|-------------------------------------------------------|------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| G20<br>F20<br>E21,<br>D20<br>G21<br>F21<br>F19<br>E20 | ADC0_AIN0<br>ADC0_AIN1<br>ADC0_AIN2<br>ADC0_AIN3<br>ADC0_AIN4<br>ADC0_AIN5<br>ADC0_AIN6<br>ADC0_AIN7 | Any unused ADC0_AIN[7:0] ball must be pulled to VSS through a resistor or connected directly to VSS when VDDA_ADC is connected to a power source. |
| F7<br>G6<br>H7<br>J6,<br>K7<br>L6<br>J8               | VDDS_DDR<br>VDDS_DDR<br>VDDS_DDR<br>VDDS_DDR<br>VDDS_DDR<br>VDDS_DDR<br>VDDS_DDR_C                   | If DDRSS0 is not used, each of these balls must be connected directly to VSS.                                                                     |

表 5-80. Connectivity Requirements (続き)

| BALL NUMBER                                                                                                                                                                                                                                                                                                                                  | BALL NAME                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | CONNECTION REQUIREMENTS                                                                                                                                                                                                                                                                                                                              |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H2<br>H1<br>J5<br>K5<br>F6<br>H4<br>D2<br>C5<br>E2<br>D4<br>D3<br>F2<br>J2<br>L5<br>J3<br>J4<br>K3<br>J1<br>M5<br>K4<br>G4<br>G5<br>G2<br>H3<br>H5<br>F1<br>E1<br>F4<br>F3<br>E3<br>E4<br>B2<br>M2<br>A3<br>A2<br>B5<br>A4<br>B3<br>C4<br>C2<br>B4<br>N5<br>L4<br>L2<br>M3<br>N4<br>N3<br>M4<br>N2<br>C1<br>B1<br>N1<br>M1<br>E5<br>F5<br>D5 | DDR0_ACT_n<br>DDR0_ALERT_n<br>DDR0_CAS_n<br>DDR0_PAR<br>DDR0_RAS_n<br>DDR0_WE_n<br>DDR0_A0<br>DDR0_A1<br>DDR0_A2<br>DDR0_A3<br>DDR0_A4<br>DDR0_A5<br>DDR0_A6<br>DDR0_A7<br>DDR0_A8<br>DDR0_A9<br>DDR0_A10<br>DDR0_A11<br>DDR0_A12<br>DDR0_A13<br>DDR0_BA0<br>DDR0_BA1<br>DDR0_BG0<br>DDR0_BG1<br>DDR0_CAL0<br>DDR0_CK0<br>DDR0_CK0_n<br>DDR0_CKE0<br>DDR0_CKE1<br>DDR0_CS0_n<br>DDR0_CS1_n<br>DDR0_DM0<br>DDR0_DM1<br>DDR0_DQ0<br>DDR0_DQ1<br>DDR0_DQ2<br>DDR0_DQ3<br>DDR0_DQ4<br>DDR0_DQ5<br>DDR0_DQ6<br>DDR0_DQ7<br>DDR0_DQ8<br>DDR0_DQ9<br>DDR0_DQ10<br>DDR0_DQ11<br>DDR0_DQ12<br>DDR0_DQ13<br>DDR0_DQ14<br>DDR0_DQ15<br>DDR0_DQS0<br>DDR0_DQS0_n<br>DDR0_DQS1<br>DDR0_DQS1_n<br>DDR0_ODT0<br>DDR0_ODT1<br>DDR0_RESET0_n | <p>If DDRSS0 is not used, leave unconnected.</p> <p>Note: The DDR0 pins in this list can only be left unconnected when VDDSDR and VDDSDR_C are connected to VSS. The DDR0 pins must be connected as defined in the <a href="#">AM64xAM243x DDR Board Design and Layout Guidelines</a>, when VDDSDR and VDDSDR_C are connected to a power source.</p> |
| K13<br>H14                                                                                                                                                                                                                                                                                                                                   | VDD_MMC0<br>VDD_DLL_MMC0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | If MMC0 is not used, each of these balls must be connected to the same power source as VDD_CORE.                                                                                                                                                                                                                                                     |
| K14                                                                                                                                                                                                                                                                                                                                          | VDDSDR_MMC0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | If MMC0 is not used, each of these balls must be connected to any 1.8-V power source that does not violate device power supply sequencing requirements.                                                                                                                                                                                              |

表 5-80. Connectivity Requirements (続き)

| BALL NUMBER                                                                      | BALL NAME                                                                                                                                              | CONNECTION REQUIREMENTS                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F18<br>G18<br>J21<br>G19<br>K20<br>J20<br>J18<br>J17<br>H17<br>H19<br>H18<br>G17 | MMC0_CALPAD<br>MMC0_CLK<br>MMC0_CMD<br>MMC0_DS<br>MMC0_DAT0<br>MMC0_DAT1<br>MMC0_DAT2<br>MMC0_DAT3<br>MMC0_DAT4<br>MMC0_DAT5<br>MMC0_DAT6<br>MMC0_DAT7 | If MMC0 is not used, each of these balls must be left unconnected.                                                                                                                                                                                                                                                                                                                          |
| H15<br>K15                                                                       | VDDA_3P3_SDIO<br>CAP_VDDSHV_MMC1                                                                                                                       | If SDIO_LDO is not used to power VDDSHV5, each of these balls must be connected directly to VSS.                                                                                                                                                                                                                                                                                            |
| P12<br>P13<br>P11<br>R14                                                         | VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0<br>VDDA_0P85_SERDES0_C<br>VDDA_1P8_SERDES0                                                                      | If SERDES0 is not used and the device boundary scan function is required, each of these balls must be connected to valid power sources.<br><br>If SERDES0 is not used and the device boundary scan function is not required, each of these balls can alternatively be connected directly to VSS.                                                                                            |
| T13<br>W16<br>W17<br>Y15<br>Y16<br>AA16<br>AA17                                  | SERDES0_REXT<br>SERDES0_REFCLK0N<br>SERDES0_REFCLK0P<br>SERDES0_RX0_N<br>SERDES0_RX0_P<br>SERDES0_TX0_N<br>SERDES0_TX0_P                               | If SERDES0 is not used, leave unconnected.<br><br>Note: The SERDES0_REXT pin can only be left unconnected when VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, and VDDA_1P8_SERDES0 are connected to VSS. The SERDES0_REXT pin must be connected to VSS through the appropriate external resistor when VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, and VDDA_1P8_SERDES0 are connected to power sources. |
| T12<br>R15<br>R13                                                                | VDDA_0P85_USB0<br>VDDA_1P8_USB0<br>VDDA_3P3_USB0                                                                                                       | If USB0 is not used, each of these balls must be connected directly to VSS.                                                                                                                                                                                                                                                                                                                 |
| AA20<br>AA19<br>U16<br>U17<br>T14                                                | USB0_DM<br>USB0_DP<br>USB0_ID<br>USB0_RCALIB<br>USB0_VBUS                                                                                              | If USB0 is not used, leave unconnected.<br><br>Note: The USB0_RCALIB pin can only be left unconnected when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to VSS. The USB0_RCALIB pin must be connected to VSS through the appropriate external resistor when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to power sources.                              |
| K10                                                                              | VMON_VSYS                                                                                                                                              | If VMON_VSYS is not used, this ball must be connected directly to VSS.                                                                                                                                                                                                                                                                                                                      |
| K16<br>E12<br>F13<br>F14                                                         | VMON_1P8_MCU<br>VMON_1P8_SOC<br>VMON_3P3_MCU<br>VMON_3P3_SOC                                                                                           | If VMON_1P8_MCU, VMON_1P8_SOC, VMON_3P3_MCU, and VMON_3P3_SOC are not used to monitor the MCU and SOC power rails, these balls must still be connected to their respective 1.8-V and 3.3-V power rails.                                                                                                                                                                                     |

(1) To determine which power supply is associated with any IO, see the POWER column of the *Pin Attributes* table.

## 注

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This can be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors are recommended to hold a valid logic level on balls with external connections.

Many of the device IOs are turned off by default and external pull resistors may be required to hold inputs of any attached device in a valid logic state until software initializes the respective IOs. The state of configurable device IOs are defined in the BALL STATE DURING RESET RX/TX/PULL and BALL STATE AFTER RESET RX/TX/PULL columns of the *Pin Attributes* table. Any IO with its input buffer (RX) turned off is allowed to float without damaging the device. However, any IO with its input buffer (RX) turned on shall never be allowed to float to any potential between  $V_{ILSS}$  and  $V_{IHSS}$ . The input buffer can enter a high-current state which could damage the IO cell if allowed to float between these levels.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                         |                                                                                    | MIN  | MAX                 | UNIT |
|---------------------------------------------------|------------------------------------------------------------------------------------|------|---------------------|------|
| VDD_CORE                                          | Core supply                                                                        | -0.3 | 1.05                | V    |
| VDDR_CORE                                         | RAM supply                                                                         | -0.3 | 1.05                | V    |
| VDD_MMC0                                          | MMC0 PHY core supply                                                               | -0.3 | 1.05                | V    |
| VDD_DLL_MMC0                                      | MMC0 PLL analog supply                                                             | -0.3 | 1.05                | V    |
| VDDA_0P85_SERDES0                                 | SERDES0 0.85-V analog supply                                                       | -0.3 | 1.05                | V    |
| VDDA_0P85_SERDES0_C                               | SERDES0 clock 0.85-V analog supply                                                 | -0.3 | 1.05                | V    |
| VDDA_0P85_USB0                                    | USB0 0.85-V analog supply                                                          | -0.3 | 1.05                | V    |
| VDDS_DDR                                          | DDR PHY IO supply                                                                  | -0.3 | 1.57                | V    |
| VDDS_DDR_C                                        | DDR clock IO supply                                                                | -0.3 | 1.57                | V    |
| VDDS_MMC0                                         | MMC0 PHY IO supply                                                                 | -0.3 | 1.98                | V    |
| VDDS_OSC                                          | MCU_OSC0 supply                                                                    | -0.3 | 1.98                | V    |
| VDDA_MCU                                          | POR and MCU PLL analog supply                                                      | -0.3 | 1.98                | V    |
| VDDA_ADC0                                         | ADC0 analog supply                                                                 | -0.3 | 1.98                | V    |
| VDDA_PLL0                                         | Main, PER1, and R5F PLL analog supply                                              | -0.3 | 1.98                | V    |
| VDDA_PLL1                                         | ARM and DDR PLL analog supply                                                      | -0.3 | 1.98                | V    |
| VDDA_PLL2                                         | PER0 PLL analog supply                                                             | -0.3 | 1.98                | V    |
| VDDA_1P8_SERDES0                                  | SERDES0 1.8-V analog supply                                                        | -0.3 | 1.98                | V    |
| VDDA_1P8_USB0                                     | USB0 1.8-V analog supply                                                           | -0.3 | 1.98                | V    |
| VDDA_TEMP0                                        | TEMP0 analog supply                                                                | -0.3 | 1.98                | V    |
| VDDA_TEMP1                                        | TEMP1 analog supply                                                                | -0.3 | 1.98                | V    |
| VPP                                               | eFuse ROM programming supply                                                       | -0.3 | 1.98                | V    |
| VDDSHV_MCU                                        | IO supply for IO MCU                                                               | -0.3 | 3.63                | V    |
| VDDSHV0                                           | IO supply for IO group 0                                                           | -0.3 | 3.63                | V    |
| VDDSHV1                                           | IO supply for IO group 1                                                           | -0.3 | 3.63                | V    |
| VDDSHV2                                           | IO supply for IO group 2                                                           | -0.3 | 3.63                | V    |
| VDDSHV3                                           | IO supply for IO group 3                                                           | -0.3 | 3.63                | V    |
| VDDSHV4                                           | IO supply for IO group 4                                                           | -0.3 | 3.63                | V    |
| VDDSHV5                                           | IO supply for IO group 5                                                           | -0.3 | 3.63                | V    |
| VDDA_3P3_USB0                                     | USB0 3.3-V analog supply                                                           | -0.3 | 3.63                | V    |
| VDDA_3P3_SDIO                                     | SDIO 3.3-V analog supply                                                           | -0.3 | 3.63                | V    |
| Steady-state max voltage at all fail-safe IO pins | MCU_PORz                                                                           | -0.3 | 3.63                | V    |
|                                                   | MCU_I2C0_SCL, MCU_I2C0_SDA, I2C0_SCL, I2C0_SDA, and EXTINTn When operating at 1.8V | -0.3 | 1.98 <sup>(3)</sup> | V    |
|                                                   | MCU_I2C0_SCL, MCU_I2C0_SDA, I2C0_SCL, I2C0_SDA, and EXTINTn When operating at 3.3V | -0.3 | 3.63 <sup>(3)</sup> |      |
|                                                   | VMON_1P8_MCU, and VMON_1P8_SOC                                                     | -0.3 | 1.98                | V    |
|                                                   | VMON_3P3_MCU, and VMON_3P3_SOC                                                     | -0.3 | 3.63                | V    |
|                                                   | VMON_VSYS <sup>(4)</sup>                                                           | -0.3 | 1.98                | V    |

over operating junction temperature range (unless otherwise noted)<sup>(1)(2)</sup>

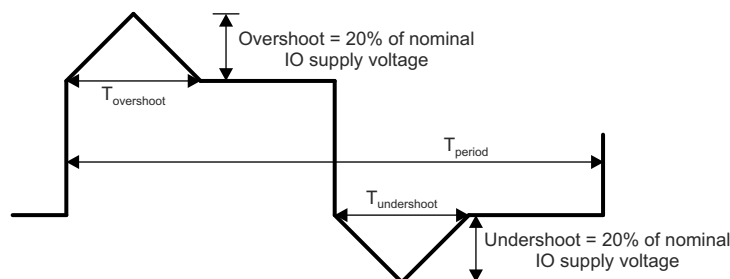
| PARAMETER                                                    |                                                                                                                       | MIN  | MAX                      | UNIT |
|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|------|--------------------------|------|
| Steady-state max voltage at all other IO pins <sup>(5)</sup> | USB0_VBUS <sup>(6)</sup>                                                                                              | -0.3 | 3.6                      | V    |
|                                                              | USB0_ID <sup>(7)</sup>                                                                                                | -0.3 | 3.6                      |      |
|                                                              | All other IO pins                                                                                                     | -0.3 | IO supply voltage + 0.3  | V    |
| Transient overshoot and undershoot at IO pin                 | 20% of IO supply voltage for up to 20% of the signal period (see <a href="#">図 6-1, IO Transient Voltage Ranges</a> ) |      | 0.2 × VDD <sup>(8)</sup> | V    |
| Latch-up performance <sup>(9)</sup>                          | I-Test                                                                                                                | -100 | +100                     | mA   |
|                                                              | Over-Voltage (OV) Test                                                                                                |      | 1.5 × VDD <sup>(8)</sup> | V    |
| T <sub>STG</sub>                                             | Storage temperature                                                                                                   | -55  | +150                     | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the [セクション 6.4, Recommended Operating Conditions](#) but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to VSS, unless otherwise noted.
- (3) The absolute maximum ratings for these fail-safe pins depends on their IO supply operating voltage. Therefore, this value is also defined by the maximum V<sub>IH</sub> value found in the *I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics* section, where the electrical characteristics table has separate parameter values for 1.8-V mode and 3.3-V mode.
- (4) The VMON\_VSYS pin provides a way to monitor the system power supply. For more information, see [セクション 8.2.4, System Power Supply Monitor Design Guidelines](#).
- (5) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
- (6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [セクション 8.2.3, USB Design Guidelines](#).
- (7) The USB0\_ID pin is connected to analog circuits in the USB0 PHY. The analog circuits source a known current while measuring voltage, to determine the resistance value (RID), if connected to VSS through a resistor. This pin should be connected to VSS for USB host operation, or left unconnected for USB device operation, and should never be connected to any external voltage source.
- (8) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
- (9) For current pulse injection (I-Test):
  - Pins stressed per JEDEC JESD78 (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

For over-voltage performance (Over-Voltage (OV) Test):

- Supplies stressed per JEDEC JESD78 (Class II) and passed specified voltage injection.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The MCU\_I2C0\_SCL, MCU\_I2C0\_SDA, I2C0\_SCL, I2C0\_SDA, EXTINTn, VMON\_1P8\_MCU, VMON\_1P8\_SOC, VMON\_3P3\_MCU, VMON\_3P3\_SOC, VMON\_VSYS, and MCU\_PORz are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in [セクション 6.1](#).



A.  $T_{overshoot} + T_{undershoot} < 20\%$  of  $T_{period}$

## 6-1. IO Transient Voltage Ranges

## 6.2 ESD Ratings

|             |                               |                                                                       | VALUE | UNIT |
|-------------|-------------------------------|-----------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±1000 | V    |
|             |                               | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±250  |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Power-On Hours (POH)

| POWER ON HOURS (POH) <sup>(1) (2) (3)</sup> |                |                |
|---------------------------------------------|----------------|----------------|
| JUNCTION TEMPERATURE RANGE ( $T_J$ )        |                | LIFETIME (POH) |
| Extended Industrial                         | –40°C to 105°C | 100000         |

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.

(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.

## 6.4 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| SUPPLY NAME                                          | DESCRIPTION                                |                  | MIN <sup>(1)</sup> | NOM                | MAX <sup>(1)</sup> | UNIT |
|------------------------------------------------------|--------------------------------------------|------------------|--------------------|--------------------|--------------------|------|
| VDD_CORE                                             | Core supply                                | 0.75-V operation | 0.715              | 0.75               | 0.79               | V    |
|                                                      |                                            | 0.85-V operation | 0.81               | 0.85               | 0.895              | V    |
| VDDR_CORE                                            | RAM supply                                 |                  | 0.81               | 0.85               | 0.895              | V    |
| VDD_MMC0 <sup>(2)</sup>                              | MMC0 PHY core supply                       |                  | 0.81               | 0.85               | 0.895              | V    |
| VDD_DLL_MMC0 <sup>(2)</sup>                          | MMC0 PLL analog supply                     |                  | 0.81               | 0.85               | 0.895              | V    |
| VDDA_0P85_SERDES0                                    | SERDES0 0.85 V analog supply               |                  | 0.81               | 0.85               | 0.895              | V    |
| VDDA_0P85_SERDES0_C                                  | SERDES0 clock 0.85 V analog supply         |                  | 0.81               | 0.85               | 0.895              | V    |
| VDDA_0P85_USB0                                       | USB0 0.85 V analog supply                  |                  | 0.81               | 0.85               | 0.895              | V    |
| VDDS_DDR <sup>(3)</sup><br>VDDS_DDR_C <sup>(3)</sup> | DDR PHY IO supply<br>DDR clock IO supply   | 1.1-V operation  | 1.06               | 1.1                | 1.17               | V    |
|                                                      |                                            | 1.2-V operation  | 1.14               | 1.2                | 1.26               | V    |
| VDDS_MMC0                                            | MMC0 PHY IO supply                         |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDS_OSC                                             | MCU_OSC0 supply                            |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_MCU                                             | POR and MCU PLL analog supply              |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_ADC0                                            | ADC0 analog supply                         |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_PLL0                                            | Main, PER and R5F PLL analog supply        |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_PLL1                                            | ARM and DDR PLL analog supply              |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_PLL2                                            | PER0 PLL analog supply                     |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_1P8_SERDES0                                     | SERDES0 1.8 V analog supply                |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_1P8_USB0                                        | USB0 1.8 V analog supply                   |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_TEMP0                                           | TEMP0 analog supply                        |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_TEMP1                                           | TEMP1 analog supply                        |                  | 1.71               | 1.8                | 1.89               | V    |
| VPP                                                  | eFuse ROM programming supply               |                  | 1.71               | 1.8                | 1.89               | V    |
| VMON_1P8_MCU                                         | Voltage monitor for 1.8 V MCU power supply |                  | 1.71               | 1.8                | 1.89               | V    |
| VMON_1P8_SOC                                         | Voltage monitor for 1.8 V SoC power supply |                  | 1.71               | 1.8                | 1.89               | V    |
| VDDA_3P3_USB0                                        | USB0 3.3 V analog supply                   |                  | 3.135              | 3.3                | 3.465              | V    |
| VDDA_3P3_SDIO                                        | SDIO 3.3 V analog supply                   |                  | 3.135              | 3.3                | 3.465              | V    |
| VMON_3P3_MCU                                         | Voltage monitor for 3.3 V MCU power supply |                  | 3.135              | 3.3                | 3.465              | V    |
| VMON_3P3_SOC                                         | Voltage monitor for 3.3 V SoC power supply |                  | 3.135              | 3.3                | 3.465              | V    |
| VMON_VSYS                                            | Voltage monitor pin                        |                  | 0                  | see <sup>(4)</sup> | 1                  | V    |
| USB0_VBUS                                            | USB Level-shifted VBUS Input               |                  | 0                  | see <sup>(5)</sup> | 3.465              | V    |
| USB0_ID                                              | USB0 analog I/O for RID detection          |                  |                    | see <sup>(6)</sup> |                    | V    |
| VDDSHV_MCU                                           | Dual-voltage IO supply                     | 1.8-V operation  | 1.71               | 1.8                | 1.89               | V    |
|                                                      |                                            | 3.3-V operation  | 3.135              | 3.3                | 3.465              | V    |
| VDDSHV0                                              | Dual-voltage IO supply                     | 1.8-V operation  | 1.71               | 1.8                | 1.89               | V    |
|                                                      |                                            | 3.3-V operation  | 3.135              | 3.3                | 3.465              | V    |
| VDDSHV1                                              | Dual-voltage IO supply                     | 1.8-V operation  | 1.71               | 1.8                | 1.89               | V    |
|                                                      |                                            | 3.3-V operation  | 3.135              | 3.3                | 3.465              | V    |
| VDDSHV2                                              | Dual-voltage IO supply                     | 1.8-V operation  | 1.71               | 1.8                | 1.89               | V    |
|                                                      |                                            | 3.3-V operation  | 3.135              | 3.3                | 3.465              | V    |
| VDDSHV3                                              | Dual-voltage IO supply                     | 1.8-V operation  | 1.71               | 1.8                | 1.89               | V    |
|                                                      |                                            | 3.3-V operation  | 3.135              | 3.3                | 3.465              | V    |
| VDDSHV4                                              | Dual-voltage IO supply                     | 1.8-V operation  | 1.71               | 1.8                | 1.89               | V    |
|                                                      |                                            | 3.3-V operation  | 3.135              | 3.3                | 3.465              | V    |

over operating junction temperature range (unless otherwise noted)

| SUPPLY NAME    | DESCRIPTION                          |                     | MIN <sup>(1)</sup> | NOM | MAX <sup>(1)</sup> | UNIT |
|----------------|--------------------------------------|---------------------|--------------------|-----|--------------------|------|
| VDDSHV5        | Dual-voltage IO supply               | 1.8-V operation     | 1.71               | 1.8 | 1.89               | V    |
|                |                                      | 3.3-V operation     | 3.135              | 3.3 | 3.465              | V    |
| T <sub>J</sub> | Operating junction temperature range | Automotive          | –40                |     | 125                | °C   |
|                |                                      | Extended Industrial | –40                |     | 105                |      |

- (1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
- (2) VDD\_MMC0 and VDD\_DLL\_MMC0 must be connected to the same power source as VDD\_CORE when MMC0 is not used. In this case, VDD\_MMC0 and VDD\_DLL\_MMC0 may be operated at a nominal voltage of 0.75 or 0.85.
- (3) VDDS\_DDR and VDDS\_DDR\_C shall be sourced from the same power source.
- (4) The VMON\_VSYS pin provides a way to monitor the system power supply. For more information, see [セクション 8.2.4, System Power Supply Monitor Design Guidelines](#).
- (5) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [セクション 8.2.3, USB Design Guidelines](#).
- (6) The USB0\_ID pin is connected to analog circuits in the USB0 PHY. The analog circuits source a known current while measuring voltage, to determine the resistance value (RID), if connected to VSS through a resistor. This pin should be connected to VSS for USB host operation, or left unconnected for USB device operation, and should never be connected to any external voltage source.

## 6.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

[表 6-1](#) describes the maximum supported frequency per speed grade for the device.

**表 6-1. Speed Grade Maximum Frequency**

| DEVICE | MAXIMUM FREQUENCY (MHz) |       |       |       |        |       |        |                     |                       |
|--------|-------------------------|-------|-------|-------|--------|-------|--------|---------------------|-----------------------|
|        | SPEED GRADE             | A53SS | R5FSS | M4FSS | CBASS0 | ICSSG | DMSC-L | DDR4 <sup>(1)</sup> | LPDDR4 <sup>(1)</sup> |
| AM64x  | S                       | 1000  | 800   | 400   | 250    | 333   | 250    | 800 (DDR-1600)      | 800 (LPDDR-1600)      |
| AM64x  | K                       | 800   | 400   | 400   | 250    | 333   | 250    | 800 (DDR-1600)      | 800 (LPDDR-1600)      |

- (1) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to [AM64x/AM243x DDR Board Design and Layout Guidelines](#) for the proper PCB implementation to achieve maximum DDR frequency.

## 6.6 Power Consumption Summary

For information on the device power consumption, see the [AM64x/AM243x Power Estimation Tool](#) application note.

## 6.7 Electrical Characteristics

### 注

The interfaces or signals described in セクション 6.7.1 through セクション 6.7.10 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### 6.7.1 I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                        |                                 | TEST CONDITIONS                                      | MIN                                | TYP                       | MAX                 | UNIT |
|----------------------------------|---------------------------------|------------------------------------------------------|------------------------------------|---------------------------|---------------------|------|
| <b>1.8 V MODE</b>                |                                 |                                                      |                                    |                           |                     |      |
| V <sub>IL</sub>                  | Input Low Voltage               |                                                      |                                    | 0.3 × VDD <sup>(1)</sup>  |                     | V    |
| V <sub>ILSS</sub>                | Input Low Voltage Steady State  |                                                      |                                    | 0.3 × VDD <sup>(1)</sup>  |                     | V    |
| V <sub>IH</sub>                  | Input High Voltage              |                                                      | 0.7 × VDD <sup>(1)</sup>           |                           | 1.98 <sup>(2)</sup> | V    |
| V <sub>IHSS</sub>                | Input High Voltage Steady State |                                                      | 0.7 × VDD <sup>(1)</sup>           |                           |                     | V    |
| V <sub>HYS</sub>                 | Input Hysteresis Voltage        |                                                      | 0.1 × VDD <sup>(1)</sup>           |                           |                     | mV   |
| I <sub>IN</sub>                  | Input Leakage Current.          | V <sub>I</sub> = 1.8 V<br>or<br>V <sub>I</sub> = 0 V |                                    |                           | ±10                 | μA   |
| V <sub>OL</sub>                  | Output Low Voltage              |                                                      |                                    | 0.2 × VDD <sup>(1)</sup>  |                     | V    |
| I <sub>OL</sub> <sup>(3)</sup>   | Low Level Output Current        | V <sub>OL(MAX)</sub>                                 | 10                                 |                           |                     | mA   |
| SR <sub>I</sub> <sup>(5)</sup>   | Input Slew Rate                 |                                                      | 18f <sup>(4)</sup><br>or<br>1.8E+6 |                           |                     | V/s  |
| <b>3.3 V MODE <sup>(6)</sup></b> |                                 |                                                      |                                    |                           |                     |      |
| V <sub>IL</sub>                  | Input Low Voltage               |                                                      |                                    | 0.3 × VDD <sup>(1)</sup>  |                     | V    |
| V <sub>ILSS</sub>                | Input Low Voltage Steady State  |                                                      |                                    | 0.25 × VDD <sup>(1)</sup> |                     | V    |
| V <sub>IH</sub>                  | Input High Voltage              |                                                      | 0.7 × VDD <sup>(1)</sup>           |                           | 3.63 <sup>(2)</sup> | V    |
| V <sub>IHSS</sub>                | Input High Voltage Steady State |                                                      | 0.7 × VDD <sup>(1)</sup>           |                           |                     | V    |
| V <sub>HYS</sub>                 | Input Hysteresis Voltage        |                                                      | 0.05 × VDD <sup>(1)</sup>          |                           |                     | mV   |
| I <sub>IN</sub>                  | Input Leakage Current.          | V <sub>I</sub> = 3.3 V<br>or<br>V <sub>I</sub> = 0 V |                                    |                           | ±10                 | μA   |
| V <sub>OL</sub>                  | Output Low Voltage              |                                                      |                                    | 0.4                       |                     | V    |
| I <sub>OL</sub> <sup>(3)</sup>   | Low Level Output Current        | V <sub>OL(MAX)</sub>                                 | 10                                 |                           |                     | mA   |
| SR <sub>I</sub> <sup>(5)</sup>   | Input Slew Rate                 |                                                      | 33f <sup>(4)</sup><br>or<br>3.3E+6 |                           | 8E+7                | V/s  |

- (1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
- (2) This value also defines the Absolute Maximum Ratings value the IO.
- (3) The I<sub>OL</sub> parameter defines the minimum Low Level Output Current for which the device is able to maintain the specified V<sub>OL</sub> value. The value defined by this parameter should be considered the maximum current available to a system implementation which needs to maintain the specified V<sub>OL</sub> value for attached components.
- (4) f = toggle frequency of the input signal in Hz.
- (5) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.
- (6) I2C Hs-mode is not supported when operating the IO in 3.3 V mode.

### 6.7.2 Fail-Safe Reset (FS RESET) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                      |                                 | TEST CONDITIONS                                      | MIN                                | TYP | MAX                        | UNIT |
|--------------------------------|---------------------------------|------------------------------------------------------|------------------------------------|-----|----------------------------|------|
| V <sub>IL</sub>                | Input Low Voltage               |                                                      |                                    |     | 0.3 × V <sub>DD5_OSC</sub> | V    |
| V <sub>ILSS</sub>              | Input Low Voltage Steady State  |                                                      |                                    |     | 0.3 × V <sub>DD5_OSC</sub> | V    |
| V <sub>IH</sub>                | Input High Voltage              |                                                      | 0.7 × V <sub>DD5_OSC</sub>         |     |                            | V    |
| V <sub>IHSS</sub>              | Input High Voltage Steady State |                                                      | 0.7 × V <sub>DD5_OSC</sub>         |     |                            | V    |
| V <sub>HYS</sub>               | Input Hysteresis Voltage        |                                                      | 200                                |     |                            | mV   |
| I <sub>IN</sub>                | Input Leakage Current.          | V <sub>I</sub> = 1.8 V<br>or<br>V <sub>I</sub> = 0 V |                                    |     | ±10                        | μA   |
| SR <sub>I</sub> <sup>(2)</sup> | Input Slew Rate                 |                                                      | 18f <sup>(1)</sup><br>or<br>1.8E+6 |     |                            | V/s  |

(1) f = toggle frequency of the input signal in Hz.

(2) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

### 6.7.3 High-Frequency Oscillator (HFOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER        |                          | TEST CONDITIONS                                        | MIN                         | TYP | MAX                         | UNIT |
|------------------|--------------------------|--------------------------------------------------------|-----------------------------|-----|-----------------------------|------|
| V <sub>IL</sub>  | Input Low Voltage        |                                                        |                             |     | 0.35 × V <sub>DD5_OSC</sub> | V    |
| V <sub>IH</sub>  | Input High Voltage       |                                                        | 0.65 × V <sub>DD5_OSC</sub> |     |                             | V    |
| V <sub>HYS</sub> | Input Hysteresis Voltage |                                                        |                             | 49  |                             | mV   |
| I <sub>IN</sub>  | Input Leakage Current.   | V <sub>I</sub> = 1.8 V<br>or<br>V <sub>I</sub> = 0.0 V |                             |     | ±10                         | μA   |

### 6.7.4 eMMC PHY Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                                 | TEST CONDITIONS               | MIN                             | TYP | MAX                          | UNIT |
|-------------------|---------------------------------|-------------------------------|---------------------------------|-----|------------------------------|------|
| V <sub>IL</sub>   | Input Low Voltage               |                               |                                 |     | 0.35 × V <sub>DD5_MMC0</sub> | V    |
| V <sub>ILSS</sub> | Input Low Voltage Steady State  |                               |                                 |     | 0.20                         | V    |
| V <sub>IH</sub>   | Input High Voltage              |                               | 0.65 × V <sub>DD5_MMC0</sub>    |     |                              | V    |
| V <sub>IHSS</sub> | Input High Voltage Steady State |                               | 1.4                             |     |                              | V    |
| I <sub>IN</sub>   | Input Leakage Current.          | V <sub>I</sub> = 1.8 V or 0 V |                                 |     | ±10                          | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                |                               | 15                              | 20  | 25                           | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor              |                               | 15                              | 20  | 25                           | kΩ   |
| V <sub>OL</sub>   | Output Low Voltage              | I <sub>OL</sub> = 2 mA        |                                 |     | 0.30                         | V    |
| V <sub>OH</sub>   | Output High Voltage             | I <sub>OH</sub> = -2 mA       | V <sub>DD5_MMC0</sub><br>- 0.30 |     |                              | V    |
| SR <sub>I</sub>   | Input Slew Rate                 |                               | 5E+8                            |     |                              | V/s  |

### 6.7.5 SDIO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER        |                                 | TEST CONDITIONS                                  | MIN                                | TYP | MAX                         | UNIT |
|------------------|---------------------------------|--------------------------------------------------|------------------------------------|-----|-----------------------------|------|
| <b>1.8V MODE</b> |                                 |                                                  |                                    |     |                             |      |
| $V_{IL}$         | Input Low Voltage               |                                                  |                                    |     | 0.58                        | V    |
| $V_{ILSS}$       | Input Low Voltage Steady State  |                                                  |                                    |     | 0.58                        | V    |
| $V_{IH}$         | Input High Voltage              |                                                  | 1.27                               |     |                             | V    |
| $V_{IHSS}$       | Input High Voltage Steady State |                                                  | 1.7                                |     |                             | V    |
| $V_{HYS}$        | Input Hysteresis Voltage        |                                                  | 150                                |     |                             | mV   |
| $I_{IN}$         | Input Leakage Current.          | $V_I = 1.8\text{ V}$<br>or<br>$V_I = 0\text{ V}$ |                                    |     | ±10                         | μA   |
| $R_{PU}$         | Pull-up Resistor                |                                                  | 40                                 | 50  | 60                          | kΩ   |
| $R_{PD}$         | Pull-down Resistor              |                                                  | 40                                 | 50  | 60                          | kΩ   |
| $V_{OL}$         | Output Low Voltage              |                                                  |                                    |     | 0.45                        | V    |
| $V_{OH}$         | Output High Voltage             |                                                  | $V_{DD}^{(1)} - 0.45$              |     |                             | V    |
| $I_{OL}^{(2)}$   | Low Level Output Current        | $V_{OL(MAX)}$                                    | 4                                  |     |                             | mA   |
| $I_{OH}^{(2)}$   | High Level Output Current       | $V_{OH(MIN)}$                                    | 4                                  |     |                             | mA   |
| $SR_I^{(4)}$     | Input Slew Rate                 |                                                  | 18f <sup>(3)</sup><br>or<br>1.8E+6 |     |                             | V/s  |
| <b>3.3V MODE</b> |                                 |                                                  |                                    |     |                             |      |
| $V_{IL}$         | Input Low Voltage               |                                                  |                                    |     | $0.25 \times V_{DD}^{(1)}$  | V    |
| $V_{ILSS}$       | Input Low Voltage Steady State  |                                                  |                                    |     | $0.15 \times V_{DD}^{(1)}$  | V    |
| $V_{IH}$         | Input High Voltage              |                                                  | $0.625 \times V_{DD}^{(1)}$        |     |                             | V    |
| $V_{IHSS}$       | Input High Voltage Steady State |                                                  | $0.625 \times V_{DD}^{(1)}$        |     |                             | V    |
| $V_{HYS}$        | Input Hysteresis Voltage        |                                                  | 150                                |     |                             | mV   |
| $I_{IN}$         | Input Leakage Current.          | $V_I = 3.3\text{ V}$<br>or<br>$V_I = 0\text{ V}$ |                                    |     | ±10                         | μA   |
| $R_{PU}$         | Pull-up Resistor                |                                                  | 40                                 | 50  | 60                          | kΩ   |
| $R_{PD}$         | Pull-down Resistor              |                                                  | 40                                 | 50  | 60                          | kΩ   |
| $V_{OL}$         | Output Low Voltage              |                                                  |                                    |     | $0.125 \times V_{DD}^{(1)}$ | V    |
| $V_{OH}$         | Output High Voltage             |                                                  | $0.75 \times V_{DD}^{(1)}$         |     |                             | V    |
| $I_{OL}^{(2)}$   | Low Level Output Current        | $V_{OL(MAX)}$                                    | 6                                  |     |                             | mA   |
| $I_{OH}^{(2)}$   | High Level Output Current       | $V_{OH(MIN)}$                                    | 10                                 |     |                             | mA   |
| $SR_I^{(4)}$     | Input Slew Rate                 |                                                  | 33f <sup>(3)</sup><br>or<br>3.3E+6 |     |                             | V/s  |

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

(2) The  $I_{OL}$  and  $I_{OH}$  parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified  $V_{OL}$  and  $V_{OH}$  values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified  $V_{OL}$  and  $V_{OH}$  values for attached components.

(3) f = toggle frequency of the input signal in Hz.

(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

## 6.7.6 LVC MOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                      |                                 | TEST CONDITIONS                                        | MIN                                | TYP                       | MAX  | UNIT |
|--------------------------------|---------------------------------|--------------------------------------------------------|------------------------------------|---------------------------|------|------|
| <b>1.8-V MODE</b>              |                                 |                                                        |                                    |                           |      |      |
| V <sub>IL</sub>                | Input Low Voltage               |                                                        |                                    | 0.35 × VDD <sup>(1)</sup> |      | V    |
| V <sub>ILSS</sub>              | Input Low Voltage Steady State  |                                                        |                                    | 0.3 × VDD <sup>(1)</sup>  |      | V    |
| V <sub>IH</sub>                | Input High Voltage              |                                                        | 0.65 × VDD <sup>(1)</sup>          |                           |      | V    |
| V <sub>IHSS</sub>              | Input High Voltage Steady State |                                                        | 0.85 × VDD <sup>(1)</sup>          |                           |      | V    |
| V <sub>HYS</sub>               | Input Hysteresis Voltage        |                                                        | 150                                |                           |      | mV   |
| I <sub>IN</sub>                | Input Leakage Current.          | V <sub>I</sub> = 1.8 V<br>or<br>V <sub>I</sub> = 0.0 V |                                    |                           | ±10  | μA   |
| R <sub>PU</sub>                | Pull-up Resistor                |                                                        | 15                                 | 22                        | 30   | kΩ   |
| R <sub>PD</sub>                | Pull-down Resistor              |                                                        | 15                                 | 22                        | 30   | kΩ   |
| V <sub>OL</sub>                | Output Low Voltage              |                                                        |                                    |                           | 0.45 | V    |
| V <sub>OH</sub>                | Output High Voltage             |                                                        | VDD <sup>(1)</sup> - 0.45          |                           |      | V    |
| I <sub>OL</sub> <sup>(2)</sup> | Low Level Output Current        | V <sub>OL</sub> (MAX)                                  | 3                                  |                           |      | mA   |
| I <sub>OH</sub> <sup>(2)</sup> | High Level Output Current       | V <sub>OH</sub> (MIN)                                  | 3                                  |                           |      | mA   |
| SR <sub>I</sub> <sup>(4)</sup> | Input Slew Rate                 |                                                        | 18f <sup>(3)</sup><br>or<br>1.8E+6 |                           |      | V/s  |
| <b>3.3-V MODE</b>              |                                 |                                                        |                                    |                           |      |      |
| V <sub>IL</sub>                | Input Low Voltage               |                                                        |                                    |                           | 0.8  | V    |
| V <sub>ILSS</sub>              | Input Low Voltage Steady State  |                                                        |                                    |                           | 0.6  | V    |
| V <sub>IH</sub>                | Input High Voltage              |                                                        | 2.0                                |                           |      | V    |
| V <sub>IHSS</sub>              | Input High Voltage Steady State |                                                        | 2.0                                |                           |      | V    |
| V <sub>HYS</sub>               | Input Hysteresis Voltage        |                                                        | 150                                |                           |      | mV   |
| I <sub>IN</sub>                | Input Leakage Current.          | V <sub>I</sub> = 3.3 V<br>or<br>V <sub>I</sub> = 0.0 V |                                    |                           | ±10  | μA   |
| R <sub>PU</sub>                | Pull-up Resistor                |                                                        | 15                                 | 22                        | 30   | kΩ   |
| R <sub>PD</sub>                | Pull-down Resistor              |                                                        | 15                                 | 22                        | 30   | kΩ   |
| V <sub>OL</sub>                | Output Low Voltage              |                                                        |                                    |                           | 0.4  | V    |
| V <sub>OH</sub>                | Output High Voltage             |                                                        | 2.4                                |                           |      | V    |
| I <sub>OL</sub> <sup>(2)</sup> | Low Level Output Current        | V <sub>OL</sub> (MAX)                                  | 5                                  |                           |      | mA   |
| I <sub>OH</sub> <sup>(2)</sup> | High Level Output Current       | V <sub>OH</sub> (MIN)                                  | 9                                  |                           |      | mA   |
| SR <sub>I</sub> <sup>(4)</sup> | Input Slew Rate                 |                                                        | 33f <sup>(3)</sup><br>or<br>3.3E+6 |                           |      | V/s  |

- (1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
- (2) The I<sub>OL</sub> and I<sub>OH</sub> parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V<sub>OL</sub> and V<sub>OH</sub> values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V<sub>OL</sub> and V<sub>OH</sub> values for attached components.
- (3) f = toggle frequency of the input signal in Hz.
- (4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

### 6.7.7 ADC12B Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                        |                                                | TEST CONDITIONS                                             | MIN                         | TYP                         | MAX  | UNIT                 |
|--------------------------------------------------|------------------------------------------------|-------------------------------------------------------------|-----------------------------|-----------------------------|------|----------------------|
| $V_{ADC0\_VREFP}$ <sup>(1)</sup>                 | Positive Reference Voltage, ADC0_VREFP         |                                                             | 1.71                        |                             | 1.89 | V                    |
| $V_{ADC0\_VREFN}$ <sup>(1)</sup>                 | Negative Reference Voltage, ADC0_VREFN         |                                                             |                             | VSS                         |      | V                    |
| $V_{ADC\_AIN[7:0]}$                              | Analog Input Voltage, ADC_AIN[7:0], Full-scale |                                                             | VSS                         | VDDA_ADC0                   |      | V                    |
| DNL                                              | Differential Non-Linearity                     |                                                             | > -1                        |                             | +1   | LSB                  |
| INL                                              | Integral Non-Linearity                         |                                                             | -2                          |                             | +2   | LSB                  |
| LSB <sub>GAIN-ERROR</sub>                        | Gain Error                                     |                                                             |                             | ±10                         |      | LSB                  |
| LSB <sub>OFFSET-ERROR</sub>                      | Offset Error                                   |                                                             |                             | ±5                          |      | LSB                  |
| SNR                                              | Signal-to-Noise Ratio                          | Input Signal:<br>200 kHz sine wave at<br>-0.5 dB Full Scale |                             | 70                          |      | dB                   |
| THD                                              | Total Harmonic Distortion                      | Input Signal:<br>200 kHz sine wave at<br>-0.5 dB Full Scale |                             | -75                         |      | dB                   |
| $Z_{ADC\_AIN[0:7]}$                              | Analog Input Impedance, ADC0_AIN[7:0]          |                                                             |                             | (2)                         |      | Ω                    |
| $I_{IN}$                                         | Input Leakage                                  |                                                             |                             | ±10                         |      | μA                   |
| $C_{SMPL}$                                       | Sampling Capacitance                           |                                                             |                             | 5.5                         |      | pF                   |
| <b>Sampling Dynamics</b>                         |                                                |                                                             |                             |                             |      |                      |
| $F_{SMPL\_CLK}$                                  | ADC0 SMPL_CLK Frequency                        |                                                             |                             | 60                          |      | MHz                  |
| $t_C$                                            | Conversion Time                                |                                                             |                             | 13                          |      | ADC0 SMPL_CLK Cycles |
| $t_{ACQ}$                                        | Acquisition Time                               |                                                             | 2                           |                             | 257  | ADC0 SMPL_CLK Cycles |
| $T_R$                                            | Sampling Rate                                  | ADC0 SMPL_CLK = 60 MHz                                      |                             |                             | 4    | MSPS                 |
| <b>General Purpose Input Mode</b> <sup>(3)</sup> |                                                |                                                             |                             |                             |      |                      |
| $V_{IL}$                                         | Input Low Voltage                              |                                                             |                             | $0.35 \times V_{DDA\_ADC0}$ |      | V                    |
| $V_{ILSS}$                                       | Input Low Voltage Steady State                 |                                                             |                             | $0.35 \times V_{DDA\_ADC0}$ |      | V                    |
| $V_{IH}$                                         | Input High Voltage                             |                                                             | $0.65 \times V_{DDA\_ADC0}$ |                             |      | V                    |
| $V_{IHSS}$                                       | Input High Voltage Steady State                |                                                             | $0.65 \times V_{DDA\_ADC0}$ |                             |      | V                    |
| $V_{HYS}$                                        | Input Hysteresis Voltage                       |                                                             | 200                         |                             |      | mV                   |
| $I_I$                                            | Input Leakage Current                          | ADC0_AIN[7:0] = VDDA_ADC0<br>or<br>ADC0_AIN[7:0] = VSS      |                             |                             | 10   | μA                   |

- (1) The ADC0\_REFP and ADC0\_REFN reference inputs are analog inputs which must be treated like high transient power supply rails. ADC0\_REFN is expected to be connected directly to the PCB ground plane along with all other VSS pins, and ADC0\_REFP is connected to a power source capable of providing at least 4 mA of current. ADC0\_REFP can be connected to the same power source as VDDA\_ADC0 if the voltage tolerance of the supply provides an acceptable accuracy for the ADC reference. A high frequency decoupling capacitor must be connected directly to the ADC0\_REFP and ADC0\_REFN pins with vias and be placed in the ball array on the back side of the PCB.
- (2) The ADC0\_AIN pins are connected to an internal sampling capacitor for a user configurable acquisition time and acquisition frequency. The input impedance of the ADC0\_AIN pins is a function of the sampling capacitance along with user configurable acquisition time and

acquisition frequency. The designer must understand the time required for the source impedance of each ADC0\_AIN pin to charge the internal sampling capacitor. The acquisition time must be set long enough for the internal sampling capacitor to settle to greater than 14 bits of accuracy.

- (3) ADC0 can be configured to operate in General Purpose Input mode, where all ADC0\_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0\_CTRL register (gpi\_mode\_en = 1).

### 6.7.8 USB2PHY Electrical Characteristics

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注

USB0 interface is compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

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### 6.7.9 SerDes PHY Electrical Characteristics

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注

The PCIe interface is compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, February 19, 2014.

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注

USB0 instance is compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013.

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### 6.7.10 DDR Electrical Characteristics

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注

The DDR interface is compatible with DDR4 devices that are **JESD79-4B standard-compliant**, and LPDDR4 devices that are **JESD209-4B standard-compliant**

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## 6.8 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses..

### 6.8.1 Recommended Operating Conditions for OTP eFuse Programming

over operating junction temperature range (unless otherwise noted)

| PARAMETER           | DESCRIPTION                                                                                                         | MIN                                         | NOM | MAX  | UNIT |
|---------------------|---------------------------------------------------------------------------------------------------------------------|---------------------------------------------|-----|------|------|
| VDD_CORE            | Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)                                       | See <i>Recommended Operating Conditions</i> |     |      | V    |
| VPP                 | Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM | NC <sup>(1)</sup>                           |     |      | V    |
|                     | Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM    | 0                                           |     |      | V    |
|                     | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(2)</sup>                                 | 1.71                                        | 1.8 | 1.89 | V    |
| I <sub>(VPP)</sub>  | VPP current                                                                                                         | 400                                         |     |      | mA   |
| SR <sub>(VPP)</sub> | VPP Slew Rate                                                                                                       | 6E+4                                        |     |      | V/s  |
| T <sub>J</sub>      | Operating junction temperature range while programming eFuse ROM.                                                   | 0                                           | 25  | 85   | °C   |

(1) NC stands for No Connect.

(2) Supply voltage range includes DC errors and peak-to-peak noise.

### 6.8.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see [セクション 6.10.2, Power Supply Sequencing](#)).

### 6.8.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in [セクション 6.8.1](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

### 6.8.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

## 6.9 Thermal Resistance Characteristics

For operation and reliability concerns, the maximum junction temperature of the device must be equal to or less than the  $T_J$  value identified in *Recommended Operating Conditions*.

### 6.9.1 Thermal Resistance Characteristics

**表 6-2. Thermal Resistance Characteristics**

TI recommends performing system level thermal simulations with worst case device power consumption.

| NO.         | PARAMETER <sup>(1)</sup> | DESCRIPTION             | °C/W <sup>(2)</sup> | AIR FLOW<br>(m/s) <sup>(3)</sup> |
|-------------|--------------------------|-------------------------|---------------------|----------------------------------|
| ALV Package |                          |                         |                     |                                  |
| T1          | $RO_{JC}$                | Junction-to-case        | 0.98                | N/A                              |
| T2          | $RO_{JB}$                | Junction-to-board       | 3.87                | N/A                              |
| T3          | $RO_{JA}$                | Junction-to-free air    | 12.8                | 0                                |
| T4          | $RO_{JA}$                | Junction-to-moving air  | 9.2                 | 1                                |
| T5          |                          |                         | 8.2                 | 2                                |
| T6          |                          |                         | 7.6                 | 3                                |
| T7          | $\Psi_{JT}$              | Junction-to-package top | 0.53                | 0                                |
| T8          |                          |                         | 0.55                | 1                                |
| T9          |                          |                         | 0.57                | 2                                |
| T10         |                          |                         | 0.58                | 3                                |
| T11         | $\Psi_{JB}$              | Junction-to-board       | 3.74                | 0                                |
| T12         |                          |                         | 3.5                 | 1                                |
| T13         |                          |                         | 3.4                 | 2                                |
| T14         |                          |                         | 3.3                 | 3                                |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [ $RO_{JC}$ ] value, which is based on a JEDEC defined 1S0P system) and is subject to change based on environment as well as application. For more information, see the EIA/JEDEC standards.

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) °C/W = degrees Celsius per watt.

(3) m/s = meters per second.

## 6.10 Timing and Switching Characteristics

注

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

注

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

### 6.10.1 Timing Parameters and Information

The timing parameter symbols used in *Timing and Switching Characteristics* sections are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in 表 6-3:

表 6-3. Timing Parameters Subscripts

| SYMBOL | PARAMETER                              |
|--------|----------------------------------------|
| c      | Cycle time (period)                    |
| d      | Delay time                             |
| dis    | Disable time                           |
| en     | Enable time                            |
| h      | Hold time                              |
| su     | Setup time                             |
| START  | Start bit                              |
| t      | Transition time                        |
| v      | Valid time                             |
| w      | Pulse duration (width)                 |
| X      | Unknown, changing, or don't care level |
| F      | Fall time                              |
| H      | High                                   |
| L      | Low                                    |
| R      | Rise time                              |
| V      | Valid                                  |
| IV     | Invalid                                |
| AE     | Active Edge                            |
| FE     | First Edge                             |
| LE     | Last Edge                              |
| Z      | High impedance                         |

## 6.10.2 Power Supply Requirements

This section describes the power supply requirements to ensure proper device operation.

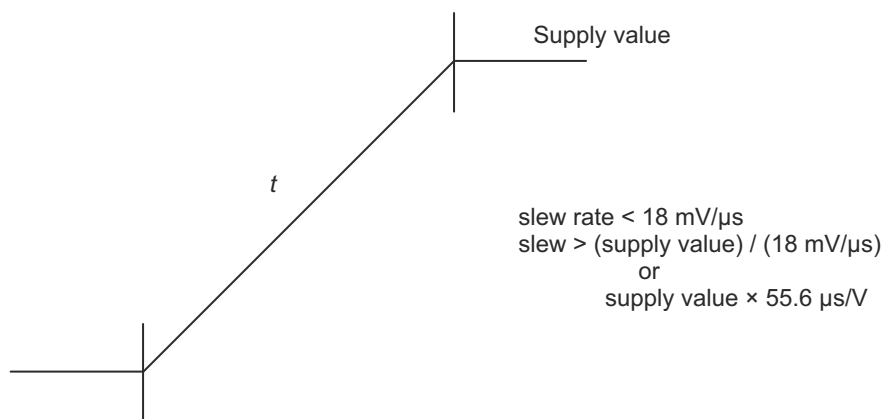
注

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified in *Signal Descriptions* and *Pin Connectivity Requirements*.

### 6.10.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18 mV/μs. For instance, as shown in [図 6-2](#), TI recommends having the supply ramp slew for a 1.8-V supply of more than 100 μs.

[図 6-2](#) describes the Power Supply Slew Rate Requirement in the device.



SPRT740\_ELCH\_06

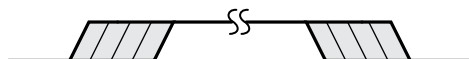
**図 6-2. Power Supply Slew and Slew Rate**

### 6.10.2.2 Power Supply Sequencing

This section describes power sequence requirements using power sequence diagrams and associated notes. Each power sequence diagram demonstrates the sequential order expected for each device power rail. This is done by assigning each device power rail to one or more waveform. A dual-voltage power rail may be associated with more than one waveform and the associated note will describe which waveform is applicable. Each waveform defines a transition region for the associated power rails and shows its sequential relationship to the transition regions of other power rails. The notes associated with the power sequence diagram provides further detail of these requirements. See the *Power-up Sequence* section for details on power-up requirements, and the *Power-down Sequence* section for details on power-down requirements.

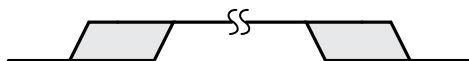
Two types of power supply transition regions are used to simplify the power supply sequencing diagrams. The legends shown in [Figure 6-3](#) and [Figure 6-4](#) along with their descriptions are provided to clarify what each transition regions represents.

[Figure 6-3](#) defines a transition region with multiple power rails which may be sourced from multiple power supplies or a single power supply. Transitions shown within the transition region represent a use case where multiple power supplies are used to source power rails associated with this waveform, and these power supplies are allowed to ramp at different times within the region since they do not have any specific sequence requirement relative to each other.



**Figure 6-3. Multiple Power Supply Transition Legend**

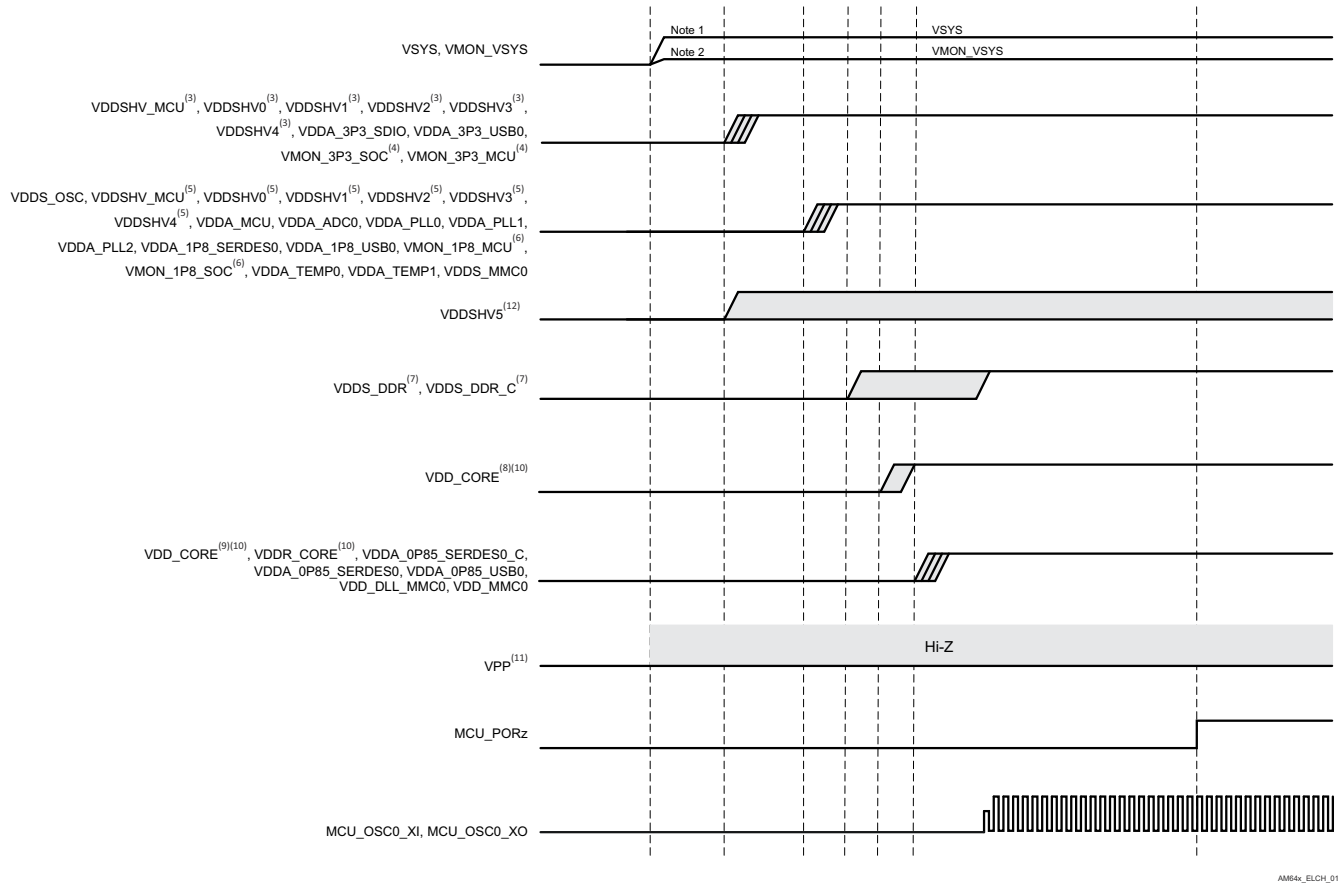
[Figure 6-4](#) defines a transition region with one or more power rails which must be sourced from a single common power supply. No transitions are shown within the region to represent a single ramp within the transition region.



**Figure 6-4. Single Common Power Supply Transition Legend**

### 6.10.2.2.1 Power-Up Sequencing

☒ 6-5 describes the device power-up sequencing.



☒ 6-5. Power-Up Sequencing

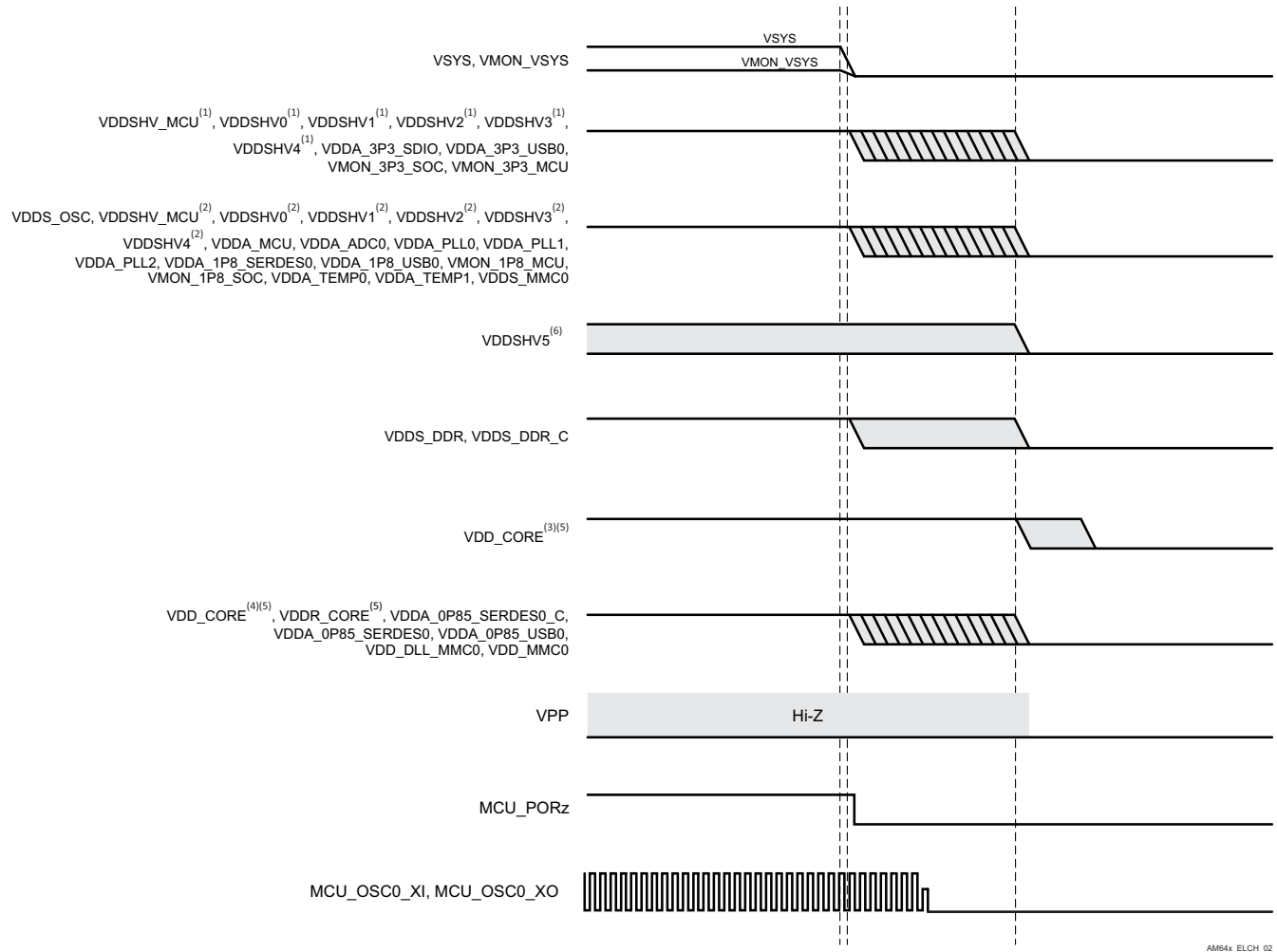
- VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.
- VMON\_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see [セクション 8.2.4, System Power Supply Monitor Design Guidelines](#).
- VDDSHV\_MCU and VDDSHVx [x=0-5] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV\_MCU or VDDSHVx [x=0-5] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.
- The VMON\_3P3\_MCU and VMON\_3P3\_SOC inputs are used to monitor supply voltage and shall be connected to the respective 3.3V supply source.
- VDDSHV\_MCU and VDDSHVx [x=0-5] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV\_MCU or VDDSHVx [x=0-5] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.
- The VMON\_1P8\_MCU and VMON\_1P8\_SOC inputs are used to monitor supply voltage and shall be connected to the respective 1.8V supply source.
- VDDSDR and VDDSDR\_C are expected to be powered by the same source such that they ramp together.
- VDDCORE can be operated at 0.75V or 0.85V. When VDDCORE is operating at 0.75V, it shall be ramped up prior to all 0.85V supplies as shown in this waveform.

9. VDD\_CORE can be operated at 0.75V or 0.85V. When VDD\_CORE is operating at 0.85V, it shall be ramped up with other 0.85V supplies during the 0.85V ramp period defined by this waveform.

10. The potential applied to VDDR\_CORE must never be greater than the potential applied to VDD\_CORE + 0.18V during power-up or power-down. This requires VDD\_CORE to ramp up before and ramp down after VDDR\_CORE when VDD\_CORE is operating at 0.75V. VDD\_CORE does not have any ramp requirements beyond the one defined for VDDR\_CORE. VDD\_CORE and VDDR\_CORE are expected to be powered by the same source so they ramp together when VDD\_CORE is operating at 0.85V.
11. VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.
12. VDDSHV5 was designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

#### 6.10.2.2.2 Power-Down Sequencing

6-6 describes the device power-down sequencing.



6-6. Power-Down Sequencing

1. VDDSHV\_MCU and VDDSHVx [x=0-5] when operating at 3.3V.
2. VDDSHV\_MCU and VDDSHVx [x=0-5] when operating at 1.8V.
3. VDD\_CORE when operating at 0.75V.
4. VDD\_CORE when operating at 0.85V.
5. The potential applied to VDDR\_CORE must never be greater than the potential applied to VDD\_CORE + 0.18V during power-up or power-down. This requires VDD\_CORE to ramp up before and ramp down after VDDR\_CORE when VDD\_CORE is operating at 0.75V. VDD\_CORE does not have any ramp requirements beyond the one defined for VDDR\_CORE. VDD\_CORE and VDDR\_CORE are expected to be powered by the same source so they ramp together when VDD\_CORE is operating at 0.85V.
6. VDDSHV5 was designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

### 6.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 6.10.3.1 Reset Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for reset related signals.

**表 6-4. Reset Timing Conditions**

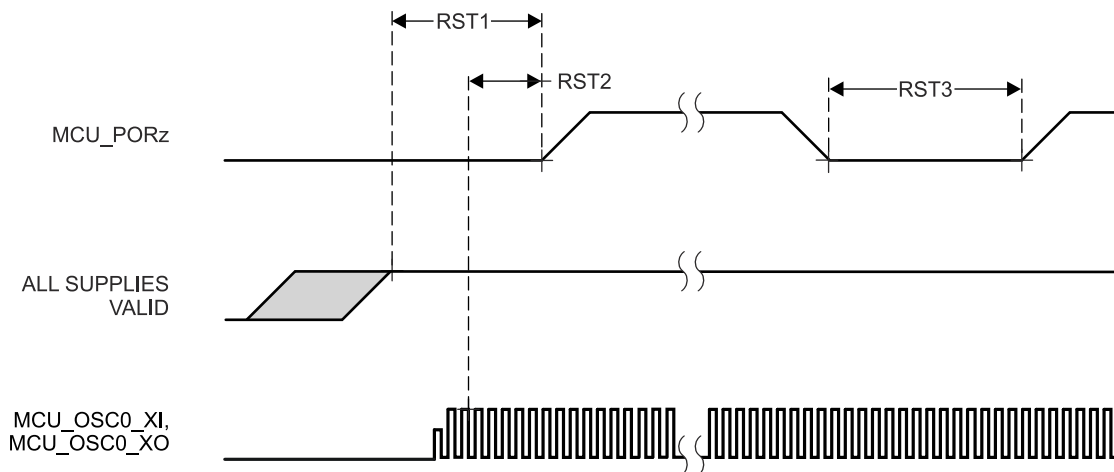
| PARAMETER         |                         |                           | MIN    | MAX | UNIT |
|-------------------|-------------------------|---------------------------|--------|-----|------|
| INPUT CONDITIONS  |                         |                           |        |     |      |
| SR <sub>I</sub>   | Input slew rate         | VDD <sup>(1)</sup> = 1.8V | 0.0018 |     | V/ns |
|                   |                         | VDD <sup>(1)</sup> = 3.3V | 0.0033 |     | V/ns |
| OUTPUT CONDITIONS |                         |                           |        |     |      |
| C <sub>L</sub>    | Output load capacitance |                           |        | 30  | pF   |

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

**表 6-5. MCU\_PORz Timing Requirements**

see 図 6-7

| NO.  | PARAMETER                                  |                                                                                                                                  | MIN     | MAX | UNIT |
|------|--------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|---------|-----|------|
| RST1 |                                            | Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)                               | 9500000 |     | ns   |
| RST2 | t <sub>h</sub> (SUPPLIES_VALID - MCU_PORz) | Hold time, MCU_PORz active (low) at Power-up after supplies valid and external clock stable (using external LVCMOS clock source) | 1200    |     | ns   |
| RST3 | t <sub>w</sub> (MCU_PORzL)                 | Pulse Width, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)                     | 1200    |     | ns   |



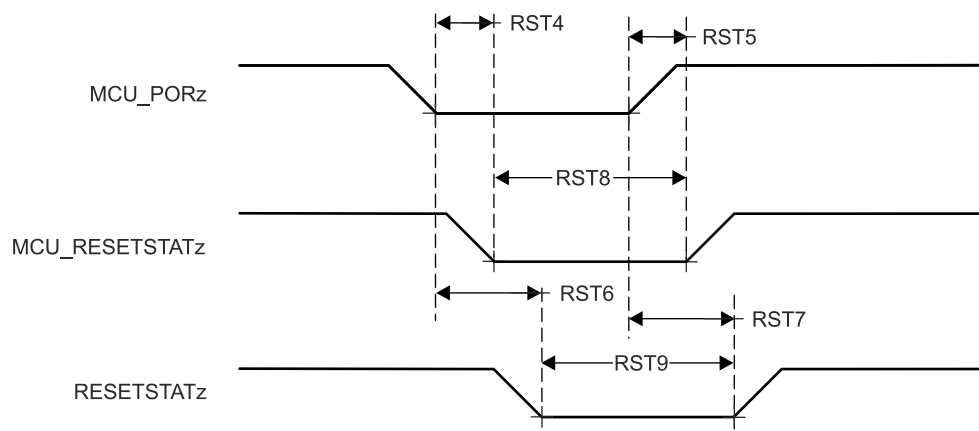
**図 6-7. MCU\_PORz Timing Requirements**

**表 6-6. MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

see 図 6-8

| NO.  | PARAMETER                                                                                                      | MIN                  | MAX | UNIT |
|------|----------------------------------------------------------------------------------------------------------------|----------------------|-----|------|
| RST4 | $t_{d(MCU\_PORzL-MCU\_RESETSTATzL)}$<br>Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)       | 0                    |     | ns   |
| RST5 | $t_{d(MCU\_PORzH-MCU\_RESETSTATzH)}$<br>Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high) | $6120 \cdot S^{(1)}$ |     | ns   |
| RST6 | $t_{d(MCU\_PORzL-RESETSTATzL)}$<br>Delay time, MCU_PORz active (low) to RESETSTATz active (low)                | 0                    |     | ns   |
| RST7 | $t_{d(MCU\_PORzH-RESETSTATzH)}$<br>Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)          | $9195 \cdot S^{(1)}$ |     | ns   |
| RST8 | $t_w(MCU\_RESETSTATzL)$<br>Pulse Width, MCU_RESETSTATz low (SW_MCU_WARMRST)                                    | $966 \cdot S^{(1)}$  |     | ns   |
| RST9 | $t_w(RESETSTATzL)$<br>Pulse Width, RESETSTATz low (SW_MCU_WARMRST, SW_MAIN_PORz, or SW_MAIN_WARMRST)           | $4040 \cdot S$       |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period in ns.

**図 6-8. MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

## 表 6-7. MCU\_RESETz Timing Requirements

see 図 6-9

| NO.   | PARAMETER                            | MIN                                  | MAX  | UNIT |
|-------|--------------------------------------|--------------------------------------|------|------|
| RST10 | $t_{w(MCU\_RESETzL)}$ <sup>(1)</sup> | Pulse Width, MCU_RESETz active (low) | 1200 | ns   |

(1) This timing parameter is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

## 表 6-8. MCU\_RESETSTATz, and RESETSTATz Switching Characteristics

see 図 6-9

| NO.   | PARAMETER                              | MIN                                                                      | MAX                  | UNIT |
|-------|----------------------------------------|--------------------------------------------------------------------------|----------------------|------|
| RST11 | $t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$ | Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)       | 0                    | ns   |
| RST12 | $t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$ | Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high) | $966 \cdot S^{(1)}$  | ns   |
| RST13 | $t_{d(MCU\_RESETzL-RESETSTATzL)}$      | Delay time, MCU_RESETz active (low) to RESETSTATz active (low)           | 960                  | ns   |
| RST14 | $t_{d(MCU\_RESETzH-RESETSTATzH)}$      | Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)     | $4040 \cdot S^{(1)}$ | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period in ns.

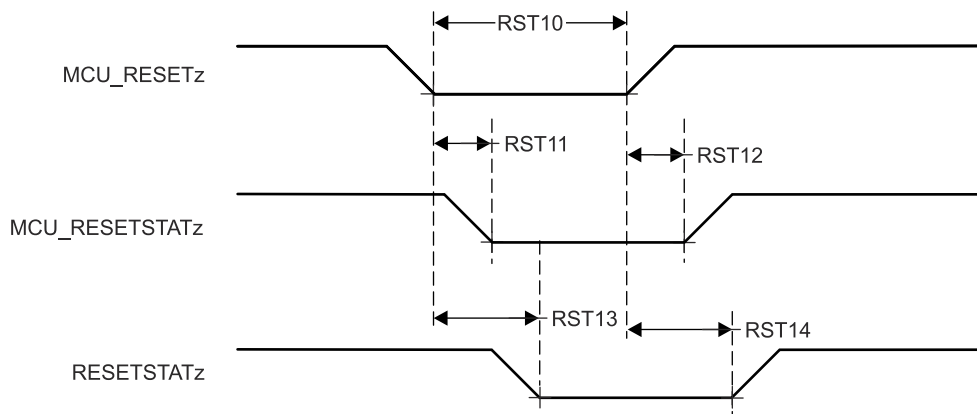


図 6-9. MCU\_RESETz, MCU\_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

## 表 6-9. RESET\_REQz Timing Requirements

see 図 6-10

| NO.   | PARAMETER                             | MIN  | MAX | UNIT |
|-------|---------------------------------------|------|-----|------|
| RST15 | $t_{w(RESSET\_REQzL)}$ <sup>(1)</sup> | 1200 |     | ns   |

(1) This timing parameter is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

## 表 6-10. RESETSTATz Switching Characteristics

see 図 6-10

| NO.   | PARAMETER                          | MIN                  | MAX | UNIT |
|-------|------------------------------------|----------------------|-----|------|
| RST16 | $t_{d(RESSET\_REQzL-RESETSTATzL)}$ | $900 \cdot T^{(1)}$  |     | ns   |
| RST17 | $t_{d(RESSET\_REQzH-RESETSTATzH)}$ | $4040 \cdot S^{(2)}$ |     | ns   |

(1) T = Reset Isolation Time (Software Dependent)

(2) S = MCU\_OSC0\_XI/XO clock period in ns.

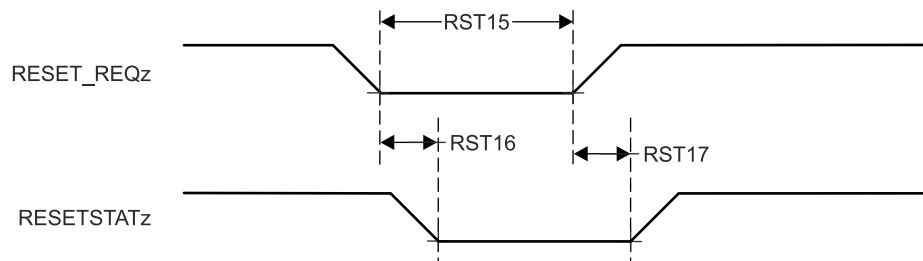


図 6-10. RESET\_REQz and RESETSTATz Timing Requirements and Switching Characteristics

## 表 6-11. EMUx Timing Requirements

see 図 6-11

| NO.   | PARAMETER                 | MIN               | MAX | UNIT |
|-------|---------------------------|-------------------|-----|------|
| RST18 | $t_{su(EMUx-MCU\_PORz)}$  | $3 \cdot S^{(1)}$ |     | ns   |
| RST19 | $t_{h(MCU\_PORz - EMUx)}$ | 10                |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period in ns.

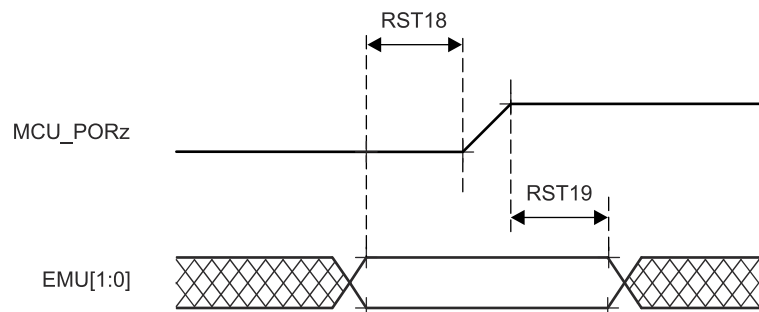


図 6-11. EMUx Timing Requirements

**表 6-12. BOOTMODE Timing Requirements**

see 図 6-12

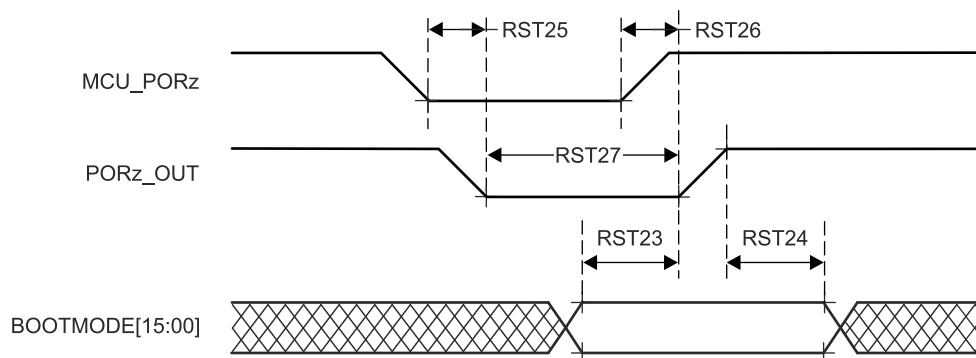
| NO.   | PARAMETER                           | MIN                                                                                                 | MAX               | UNIT |
|-------|-------------------------------------|-----------------------------------------------------------------------------------------------------|-------------------|------|
| RST23 | $t_{su}(\text{BOOTMODE-PORz\_OUT})$ | Setup time, BOOTMODE[15:00] before PORz_OUT high (External MCU PORz event or Software SW_MAIN_PORz) | $3 \cdot S^{(1)}$ | ns   |
| RST24 | $t_h(\text{PORz\_OUT - BOOTMODE})$  | Hold time, BOOTMODE[15:00] after PORz_OUT high (External MCU PORz event, or Software SW_MAIN_PORz)  | 0                 | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period in ns.

**表 6-13. PORz\_OUT Switching Characteristics**

see 図 6-12

| NO.   | PARAMETER                          | MIN                                                              | MAX  | UNIT |
|-------|------------------------------------|------------------------------------------------------------------|------|------|
| RST25 | $t_d(\text{MCU\_PORzL-PORz\_OUT})$ | Delay time, MCU_PORz active (low) to PORz_OUT active (low)       | 0    | ns   |
| RST26 | $t_d(\text{MCU\_PORzH-PORz\_OUT})$ | Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high) | 1840 | ns   |
| RST27 | $t_w(\text{PORz\_OUTL})$           | Pulse Width, PORz_OUT low (MCU_PORz or SW_MAIN_PORz)             | 1200 | ns   |



**図 6-12. BOOTMODE Timing Requirements and PORz\_OUT Switching Characteristics**

### 6.10.3.2 Safety Signal Timing

Tables and figures provided in this section define timing conditions and switching characteristics for MCU\_SAFETY\_ERRORn.

**表 6-14. MCU\_SAFETY\_ERRORn Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance |     | 30  | pF   |

**表 6-15. MCU\_SAFETY\_ERRORn Switching Characteristics**

see 図 6-13

| NO.   | PARAMETER                                      |                                                                                  | MIN                         | MAX | UNIT |
|-------|------------------------------------------------|----------------------------------------------------------------------------------|-----------------------------|-----|------|
| SFTY1 | $t_{c(MCU\_SAFETY\_ERRORn)}$                   | Cycle time minimum, MCU_SAFETY_ERRORn (PWM mode enabled)                         | $(P*H)+(P*L)^{(1) (3) (4)}$ |     | ns   |
| SFTY2 | $t_{w(MCU\_SAFETY\_ERRORn)}$                   | Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled) <sup>(5)</sup> | $P*R^{(1) (2)}$             |     | ns   |
| SFTY3 | $t_d (ERROR\_CONDITION- MCU\_SAFETY\_ERRORnL)$ | Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active <sup>(5)</sup>           | $50*P^{(1)}$                |     | ns   |

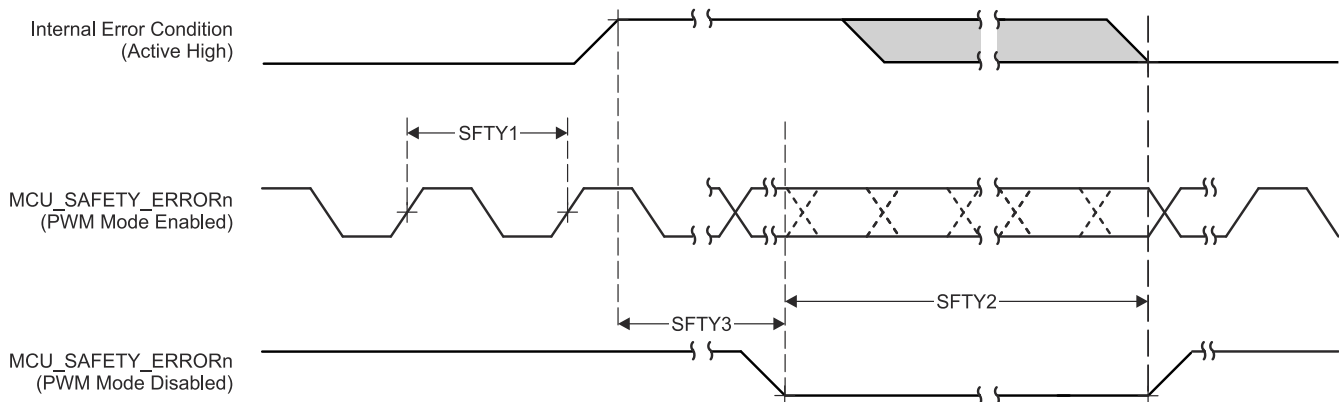
(1) P = ESM functional clock

(2) R = Error Pin Counter Pre-Load Register count value

(3) H = Error Pin PWM High Pre-Load Register count value

(4) L = Error Pin PWM Low Pre-Load Register count value

(5) When PWM mode is enabled, MCU\_SAFETY\_ERRORn stops toggling after SFTY3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, MCU\_SAFETY\_ERRORn is active low.



**図 6-13. MCU\_SAFETY\_ERRORn Timing Requirements and Switching Characteristics**

### 6.10.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for clock signals.

**表 6-16. Clock Timing Conditions**

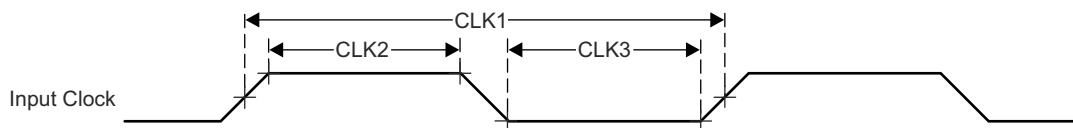
| PARAMETER                |                         | MIN                            | MAX | UNIT |
|--------------------------|-------------------------|--------------------------------|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |                                |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5                            |     | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |                                |     |      |
| C <sub>L</sub>           | Output load capacitance | 10 ns ≤ t <sub>c</sub> < 20 ns | 10  | pF   |
|                          |                         | 20 ns ≤ t <sub>c</sub>         | 30  | pF   |

**表 6-17. Clock Timing Requirements**

see 図 6-14

| NO.  |                                   |                                      | MIN                   | MAX                   | UNIT |
|------|-----------------------------------|--------------------------------------|-----------------------|-----------------------|------|
| CLK1 | t <sub>c</sub> (EXT_REFCLK1)      | Cycle time minimum, EXT_REFCLK1      | 10                    |                       | ns   |
| CLK2 | t <sub>w</sub> (EXT_REFCLK1H)     | Pulse Duration, EXT_REFCLK1 high     | E*0.45 <sup>(1)</sup> | E*0.55 <sup>(1)</sup> | ns   |
| CLK3 | t <sub>w</sub> (EXT_REFCLK1L)     | Pulse Duration, EXT_REFCLK1 low      | E*0.45 <sup>(1)</sup> | E*0.55 <sup>(1)</sup> | ns   |
| CLK1 | t <sub>c</sub> (MCU_EXT_REFCLK0)  | Cycle time minimum, MCU_EXT_REFCLK0  | 10                    |                       | ns   |
| CLK2 | t <sub>w</sub> (MCU_EXT_REFCLK0H) | Pulse Duration, MCU_EXT_REFCLK0 high | F*0.45 <sup>(2)</sup> | F*0.55 <sup>(2)</sup> | ns   |
| CLK3 | t <sub>w</sub> (MCU_EXT_REFCLK0L) | Pulse Duration, MCU_EXT_REFCLK0 low  | F*0.45 <sup>(2)</sup> | F*0.55 <sup>(2)</sup> | ns   |

- (1) E = EXT\_REFCLK1 cycle time  
(2) F = MCU\_EXT\_REFCLK0 cycle time



**図 6-14. Clock Timing Requirements**

**表 6-18. Clock Switching Characteristics**

see 図 6-15

| NO.  | PARAMETER                 |                                     | MIN            | MAX            | UNIT |
|------|---------------------------|-------------------------------------|----------------|----------------|------|
| CLK4 | $t_{c(SYSCLKOUT0)}$       | Cycle time minimum, SYSCLKOUT0      | 8              |                | ns   |
| CLK5 | $t_{w(SYSCLKOUT0H)}$      | Pulse Duration, SYSCLKOUT0 high     | $A*0.4^{(1)}$  | $A*0.6^{(1)}$  | ns   |
| CLK6 | $t_{w(SYSCLKOUT0L)}$      | Pulse Duration, SYSCLKOUT0 low      | $A*0.4^{(1)}$  | $A*0.6^{(1)}$  | ns   |
| CLK4 | $t_{c(OBSCLK0)}$          | Cycle time minimum, OBSCLK0         | 5              |                | ns   |
| CLK5 | $t_{w(OBSCLK0H)}$         | Pulse Duration, OBSCLK0 high        | $B*0.45^{(2)}$ | $B*0.55^{(2)}$ | ns   |
| CLK6 | $t_{w(OBSCLK0L)}$         | Pulse Duration, OBSCLK0 low         | $B*0.45^{(2)}$ | $B*0.55^{(2)}$ | ns   |
| CLK4 | $t_{c(CLKOUT0)}$          | Cycle time minimum, CLKOUT0         | 20             |                | ns   |
| CLK5 | $t_{w(CLKOUT0H)}$         | Pulse Duration, CLKOUT0 high        | $C*0.4^{(3)}$  | $C*0.6^{(3)}$  | ns   |
| CLK6 | $t_{w(CLKOUT0L)}$         | Pulse Duration, CLKOUT0 low         | $C*0.4^{(3)}$  | $C*0.6^{(3)}$  | ns   |
| CLK4 | $t_{c(MCU\_SYSCLKOUT0)}$  | Cycle time minimum, MCU_SYSCLKOUT0  | 10             |                | ns   |
| CLK5 | $t_{w(MCU\_SYSCLKOUT0H)}$ | Pulse Duration, MCU_SYSCLKOUT0 high | $G*0.4^{(4)}$  | $G*0.6^{(4)}$  | ns   |
| CLK6 | $t_{w(MCU\_SYSCLKOUT0L)}$ | Pulse Duration, MCU_SYSCLKOUT0 low  | $G*0.4^{(4)}$  | $G*0.6^{(4)}$  | ns   |
| CLK4 | $t_{c(MCU\_OBSCLK0)}$     | Cycle time minimum, MCU_OBSCLK0     | 5              |                | ns   |
| CLK5 | $t_{w(MCU\_OBSCLK0H)}$    | Pulse Duration, MCU_OBSCLK0 high    | $H*0.45^{(5)}$ | $H*0.55^{(5)}$ | ns   |
| CLK6 | $t_{w(MCU\_OBSCLK0L)}$    | Pulse Duration, MCU_OBSCLK0 low     | $H*0.45^{(5)}$ | $H*0.55^{(5)}$ | ns   |

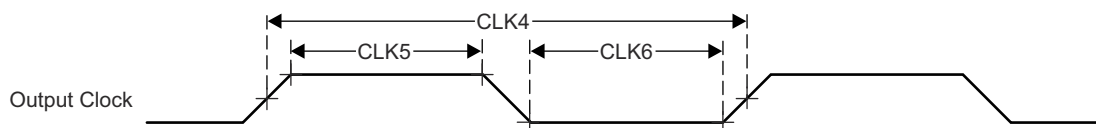
(1) A = SYSCLKOUT0 cycle time

(2) B = OBSCLK0 cycle time

(3) C = CLKOUT0 cycle time

(4) G = MCU\_SYSCLKOUT0 cycle time

(5) H = MCU\_OBSCLK0 cycle time

**図 6-15. Clock Switching Characteristics**

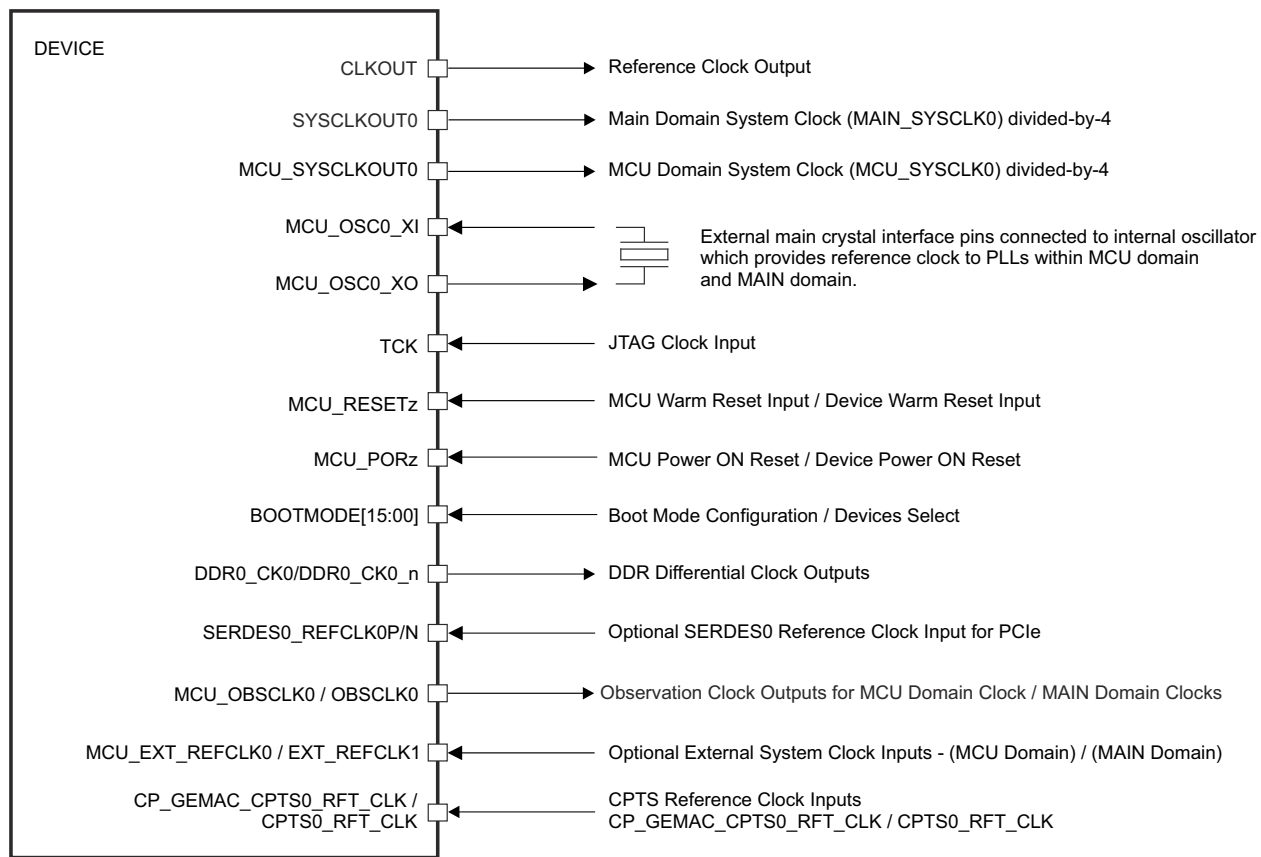
## 6.10.4 Clock Specifications

### 6.10.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- MCU\_OSC0\_XI/MCU\_OSC0\_XO — External main crystal interface pins connected to the internal high-frequency oscillator (MCU\_HFOSC0), which is the default clock source for internal reference clock MCU\_HFOSC0\_CLKOUT.
- General purpose clock inputs
  - MCU\_EXT\_REFCLK0 — Optional external system clock input for MCU domain.
  - EXT\_REFCLK1 — Optional external system clock input for MAIN domain.
  - SERDES0\_REFCLK0P/N — Optional SERDES0 reference clock input for PCIe.
- External CPTS reference clock inputs
  - CP\_GEMAC\_CPTS0\_RFT\_CLK — CPTS reference clock input.
  - CPTS\_RFT\_CLK — CPTS reference clock input.

Figure 6-16 shows the external input clock sources and the output clocks to peripherals.

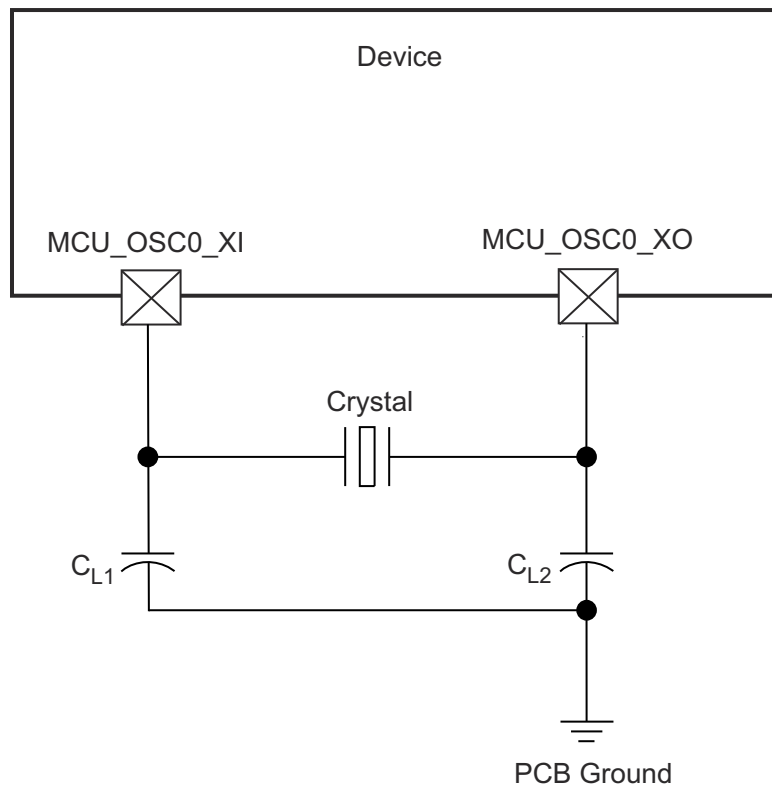


**Figure 6-16. Input Clocks Interface**

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

#### 6.10.4.1.1 MCU\_OSC0 Internal Oscillator Clock Source

図 6-17 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit must be placed as close as possible to the MCU\_OSC0\_XI and MCU\_OSC0\_XO pins.



AM64x\_MCU\_OSC\_INT\_01

図 6-17. MCU\_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 6-19 summarizes the required electrical constraints.

表 6-19. MCU\_OSC0 Crystal Circuit Requirements

| PARAMETER             |                                                     |                            |                                             | MIN | TYP | MAX  | UNIT |
|-----------------------|-----------------------------------------------------|----------------------------|---------------------------------------------|-----|-----|------|------|
| F <sub>xtal</sub>     | Crystal Parallel Resonance Frequency                |                            |                                             | 25  |     |      | MHz  |
| F <sub>xtal</sub>     | Crystal Frequency Stability and Tolerance           |                            | Ethernet RGMII and RMII not used            |     |     | ±100 | ppm  |
|                       |                                                     |                            | Ethernet RGMII and RMII using derived clock |     |     | ±50  |      |
| C <sub>L1+PCBXI</sub> | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub> |                            |                                             | 12  |     | 24   | pF   |
| C <sub>L2+PCBXO</sub> | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub> |                            |                                             | 12  |     | 24   | pF   |
| C <sub>L</sub>        | Crystal Load Capacitance                            |                            |                                             | 6   |     | 12   | pF   |
| C <sub>shunt</sub>    | Crystal Circuit Shunt Capacitance                   | ESR <sub>xtal</sub> = 30 Ω | 25 MHz                                      |     |     | 7    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 40 Ω | 25 MHz                                      |     |     | 5    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 50 Ω | 25 MHz                                      |     |     | 5    | pF   |
| ESR <sub>xtal</sub>   | Crystal Effective Series Resistance                 |                            |                                             |     |     | (1)  | Ω    |

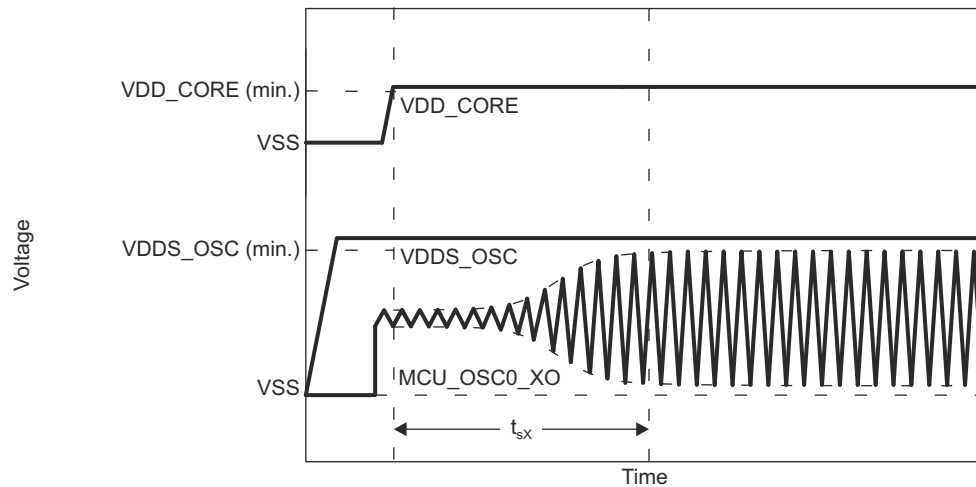
(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C<sub>shunt</sub> parameter.

When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

表 6-20 details the switching characteristics of the oscillator.

**表 6-20. MCU\_OSC0 Switching Characteristics - Crystal Mode**

| PARAMETER  |                             | MIN | TYP | MAX  | UNIT |
|------------|-----------------------------|-----|-----|------|------|
| $C_{XI}$   | XI Capacitance              |     |     | 1.44 | pF   |
| $C_{XO}$   | XO Capacitance              |     |     | 1.52 | pF   |
| $C_{XIXO}$ | XI to XO Mutual Capacitance |     |     | 0.01 | pF   |
| $t_s$      | Start-up Time               |     | 4   |      | ms   |



**図 6-18. MCU\_OSC0 Start-up Time**

#### 6.10.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load,  $C_L$ , of this circuit is a combination of discrete capacitors  $C_{L1}$ ,  $C_{L2}$ , and several parasitic contributions. PCB signal traces which connect crystal circuit components to MCU\_OSC0\_XI and MCU\_OSC0\_XO have parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where the PCB designer should be able to extract parasitic capacitance for each signal trace. The MCU\_OSC0 circuits and device package have combined parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where these parasitic capacitance values are defined in 表 6-20.

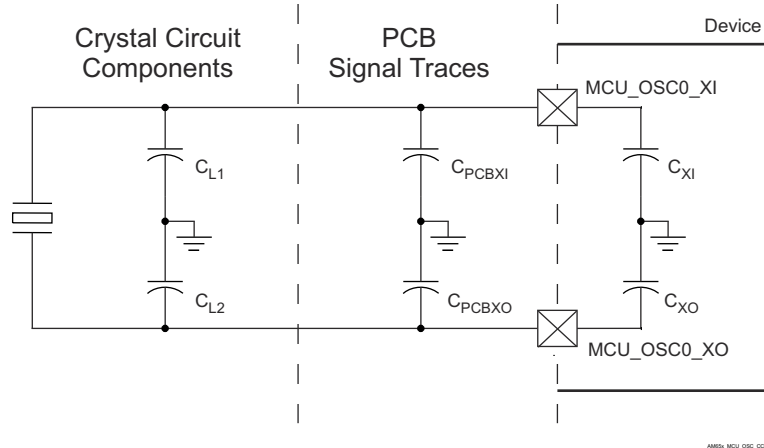


図 6-19. Load Capacitance

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in 図 6-17, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2.9$  pF,  $C_{XI} = 0.5$  pF,  $C_{PCBXO} = 3.7$  pF,  $C_{XO} = 0.5$  pF, the value of  $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10 \text{ pF}) - 2.9 \text{ pF} - 0.5 \text{ pF}] = 16.6 \text{ pF}$  and  $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 3.7 \text{ pF} - 0.5 \text{ pF}] = 15.8 \text{ pF}$

#### 6.10.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for MCU\_OSC0 operating conditions defined in 表 6-19. Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to MCU\_OSC0 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in 表 6-20.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

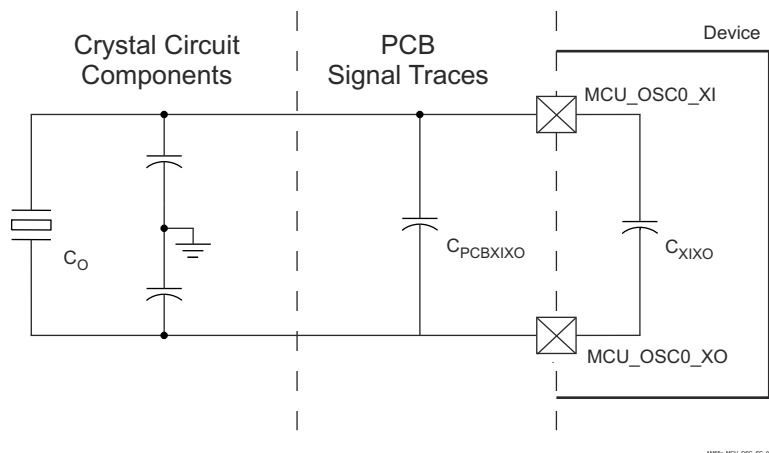


図 6-20. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{\text{shunt}} \geq C_O + C_{\text{PCBXIXO}} + C_{\text{XIXO}}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{\text{PCBXIXO}} = 0.04$  pF,  $C_{\text{XIXO}} = 0.01$  pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

#### 6.10.4.1.2 MCU\_OSC0 LVCMOS Digital Clock Source

図 6-21 shows the recommended oscillator connections when MCU\_OSC0\_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

#### 注

A DC steady-state condition is not allowed on MCU\_OSC0\_XI when the oscillator is powered up. This is not allowed because MCU\_OSC0\_XI is internally AC coupled to a comparator that can enter an unknown state when DC is applied to the input. Therefore, application software must power down MCU\_OSC0 any time MCU\_OSC0\_XI is not toggling between logic states.

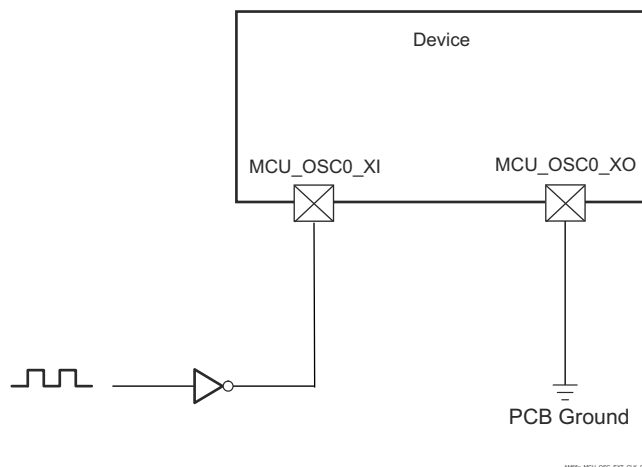


図 6-21. 1.8-V LVCMOS-Compatible Clock Input

#### 6.10.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU\_SYSCCLKOUT0**
  - MCU\_SYSCCLKOUT0 is the MCU domain system clock (MCU\_SYSCCK0) divided-by-4. This clock output is provided for test and debug purposes only.
- **MCU\_OBSCCLK0**
  - Observation clock output for test and debug purposes only.
- **SYSCCLKOUT0**
  - SYSCCLKOUT0 is the MAIN domain system clock (MAIN\_SYSCCLK0) divided-by-4. This clock output is provided for test and debug purposes only.
- **CLKOUT0**
  - CLKOUT0 is the Ethernet subsystem clock (MAIN\_PLL0\_HSDIV4\_CLKOUT) divided-by-5 or divided-by-10. This clock output was provided to source to the external PHY. When configured to operate as the RMI Clock source (50 MHz) the signal must also be routed back to the RMII\_REF\_CLK pin for proper device operation.
- **OBSCCLK0**
  - Observation clock output for test and debug purposes only.
- **GPMC\_FCLK\_MUX**
  - GPMC\_FCLK\_MUX is the GPMC0 functional clock (GPMC\_FCLK). This clock is provided as an alternative GPMC interface clock when attached devices require a continuous running clock.

For more information, see *Clock Outputs* section in *Clocking* chapter and *GPMC Clock Configuration* section in *Peripherals* chapter in the device TRM.

#### 6.10.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuits (PLLs) by internal regulators that derive their power from off-chip power-sources.

There is one PLL in the MCU domain:

- MCU0\_PLL

There are six PLLs in the MAIN domain:

- ARM0\_PLL
- MAIN\_PLL
- PER0\_PLL
- PER1\_PLL
- DDR PLL
- R5F PLL

---

注

For more information, see:

- *Device Configuration / Clocking / PLLs* section in the device TRM.
  - *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in the device TRM.
- 

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注

The input reference clock (MCU\_OSC0\_XI / MCU\_OSC0\_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

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#### 6.10.4.4 Recommended System Precautions for Clock and Control Signal Transitions

All clock and strobe signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.

Monotonic transitions are more likely to occur with fast signal transitions. It is easy for noise to create non-monotonic events on a signal with slow transitions. Therefore, avoid slow signal transitions on all clock and control signals since they are more likely to generate glitches inside the device.

## 6.10.5 Peripherals

### 6.10.5.1 CPSW3G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

注

CPSW3G MDIO0, CPSW3G RMII1, CPSW3G RMII2, and CPSW3G RGMII1 have one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for these interfaces can be found in the tables of the [CPSW3G IOSETs](#) section.

#### 6.10.5.1.1 CPSW3G MDIO Timing

表 6-21, 表 6-22, 表 6-23, and 図 6-22 present timing conditions, requirements, and switching characteristics for CPSW3G MDIO.

**表 6-21. CPSW3G MDIO Timing Conditions**

| PARAMETER                             |                                              | MIN | MAX | UNIT |
|---------------------------------------|----------------------------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>               |                                              |     |     |      |
| SR <sub>I</sub>                       | Input slew rate                              | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |     |     |      |
| C <sub>L</sub>                        | Output load capacitance                      | 10  | 470 | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |     |     |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 0   | 5   | ns   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |     | 1   | ns   |

**表 6-22. CPSW3G MDIO Timing Requirements**

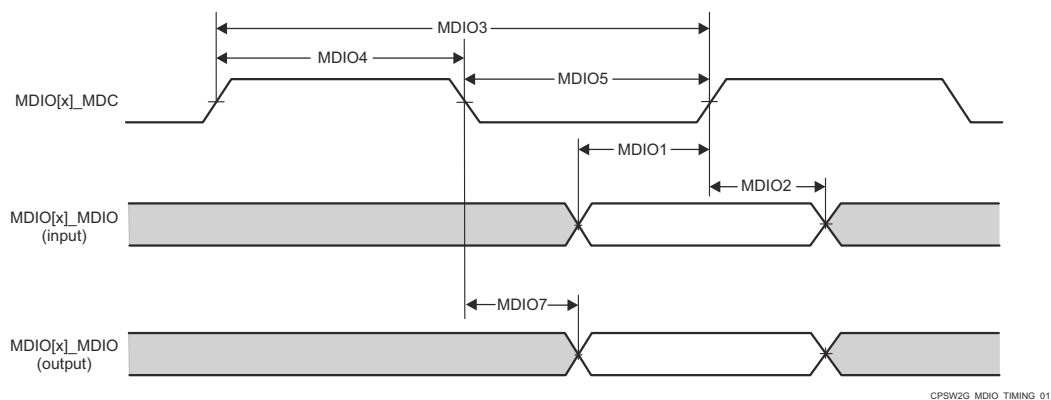
see 図 6-22

| NO.   | PARAMETER                  |                                                        | MIN | MAX | UNIT |
|-------|----------------------------|--------------------------------------------------------|-----|-----|------|
| MDIO1 | t <sub>su</sub> (MDIO_MDC) | Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high | 45  |     | ns   |
| MDIO2 | t <sub>h</sub> (MDC_MDIO)  | Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high   | 0   |     | ns   |

**表 6-23. CPWS3G MDIO Switching Characteristics**

see 図 6-22

| NO.   | PARAMETER                 |                                                   | MIN | MAX | UNIT |
|-------|---------------------------|---------------------------------------------------|-----|-----|------|
| MDIO3 | t <sub>c</sub> (MDC)      | Cycle time, MDIO[x]_MDC                           | 400 |     | ns   |
| MDIO4 | t <sub>w</sub> (MDCH)     | Pulse Duration, MDIO[x]_MDC high                  | 160 |     | ns   |
| MDIO5 | t <sub>w</sub> (MDCL)     | Pulse Duration, MDIO[x]_MDC low                   | 160 |     | ns   |
| MDIO7 | t <sub>d</sub> (MDC_MDIO) | Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid | -10 | 10  | ns   |



**6-22. CPSW3G MDIO Timing Requirements and Switching Characteristics**

#### 6.10.5.1.2 CPSW3G RMII Timing

表 6-24, 表 6-25, 図 6-23, 表 6-26, 図 6-24 表 6-27, and 図 6-25 present timing conditions, requirements, and switching characteristics for CPSW3G RMII.

**表 6-24. CPSW3G RMII Timing Conditions**

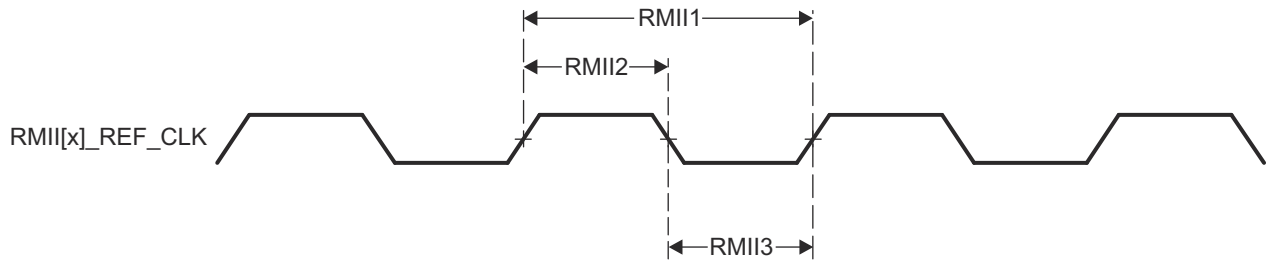
| PARAMETER         |                         |                           | MIN  | MAX  | UNIT |
|-------------------|-------------------------|---------------------------|------|------|------|
| INPUT CONDITIONS  |                         |                           |      |      |      |
| SR <sub>i</sub>   | Input slew rate         | VDD <sup>(1)</sup> = 1.8V | 0.18 | 0.54 | V/ns |
|                   |                         | VDD <sup>(1)</sup> = 3.3V | 0.4  | 1.2  | V/ns |
| OUTPUT CONDITIONS |                         |                           |      |      |      |
| C <sub>L</sub>    | Output load capacitance |                           | 3    | 25   | pF   |

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the Pin Attributes table.

**表 6-25. RMII[x]\_REF\_CLK Timing Requirements – RMII Mode**

see 図 6-23

| NO.   | PARAMETER                 | DESCRIPTION                          | MIN    | MAX    | UNIT |
|-------|---------------------------|--------------------------------------|--------|--------|------|
| RMII1 | t <sub>c</sub> (REF_CLK)  | Cycle time, RMII[x]_REF_CLK          | 19.999 | 20.001 | ns   |
| RMII2 | t <sub>w</sub> (REF_CLKH) | Pulse Duration, RMII[x]_REF_CLK High | 7      | 13     | ns   |
| RMII3 | t <sub>w</sub> (REF_CLKL) | Pulse Duration, RMII[x]_REF_CLK Low  | 7      | 13     | ns   |

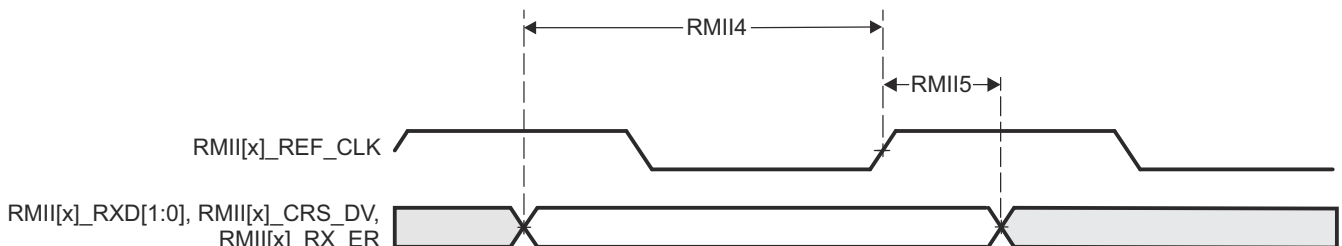


**図 6-23. CPSW3G RMII[x]\_REF\_CLK Timing Requirements – RMII Mode**

**表 6-26. RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, and RMII[x]\_RX\_ER Timing Requirements – RMII Mode**

see 図 6-24

| NO.   | PARAMETER                        | DESCRIPTION                                               | MIN | MAX | UNIT |
|-------|----------------------------------|-----------------------------------------------------------|-----|-----|------|
| RMII4 | t <sub>su</sub> (RXD-REF_CLK)    | Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK | 4   |     | ns   |
|       | t <sub>su</sub> (CRS_DV-REF_CLK) | Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK   | 4   |     | ns   |
|       | t <sub>su</sub> (RX_ER-REF_CLK)  | Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK    | 4   |     | ns   |
| RMII5 | t <sub>h</sub> (REF_CLK-RXD)     | Hold time RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK    | 2   |     | ns   |
|       | t <sub>h</sub> (REF_CLK-CRS_DV)  | Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK     | 2   |     | ns   |
|       | t <sub>h</sub> (REF_CLK-RX_ER)   | Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK      | 2   |     | ns   |



**図 6-24. CPSW3G RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RX\_ER Timing Requirements – RMII Mode**

表 6-27. RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode

see  6-25

| NO.   | PARAMETER                | DESCRIPTION                                                | MIN | MAX | UNIT |
|-------|--------------------------|------------------------------------------------------------|-----|-----|------|
| RMII6 | $t_{d(REF\_CLK-TXD)}$    | Delay time, RMII[x]_REF_CLK High to RMII[x]_TXD[1:0] valid | 2   | 10  | ns   |
|       | $t_{d(REF\_CLK-TX\_EN)}$ | Delay time, RMII[x]_REF_CLK to RMII[x]_TX_EN valid         | 2   | 10  | ns   |

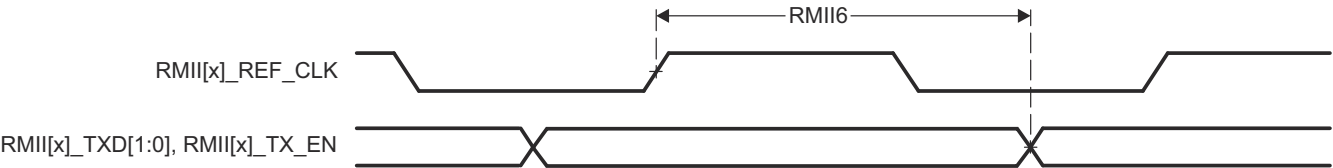


図 6-25. RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode

#### 6.10.5.1.3 CPSW3G RGMII Timing

表 6-28, 表 6-29, 表 6-30, 図 6-26, 表 6-31, 表 6-32, and 図 6-27 present timing conditions, requirements, and switching characteristics for CPSW3G RGMII.

**表 6-28. CPSW3G RGMII Timing Conditions**

| PARAMETER                             |                                              |                                                       | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|-------------------------------------------------------|------|-----|------|
| <b>INPUT CONDITIONS</b>               |                                              |                                                       |      |     |      |
| SR <sub>I</sub>                       | Input slew rate                              |                                                       | 2.64 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |                                                       |      |     |      |
| C <sub>L</sub>                        | Output load capacitance                      |                                                       | 2    | 20  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |                                                       |      |     |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | RGMII[x]_RXC,<br>RGMII[x]_RD[3:0],<br>RGMII[x]_RX_CTL |      | 50  | ps   |
|                                       |                                              | RGMII[x]_TXC,<br>RGMII[x]_TD[3:0],<br>RGMII[x]_TX_CTL |      | 50  | ps   |

表 6-29. RGMII[x]\_RXC Timing Requirements – RGMII Mode

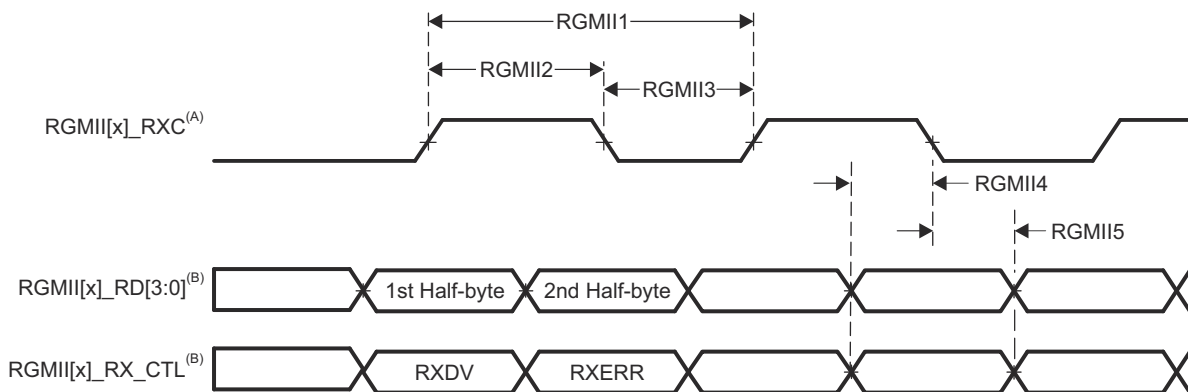
see 図 6-26

| NO.    | PARAMETER     | DESCRIPTION                       | MODE     | MIN | MAX | UNIT |
|--------|---------------|-----------------------------------|----------|-----|-----|------|
| RGMII1 | $t_{c(RXC)}$  | Cycle time, RGMII[x]_RXC          | 10Mbps   | 360 | 440 | ns   |
|        |               |                                   | 100Mbps  | 36  | 44  | ns   |
|        |               |                                   | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII2 | $t_{w(RXCH)}$ | Pulse duration, RGMII[x]_RXC high | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII3 | $t_{w(RXCL)}$ | Pulse duration, RGMII[x]_RXC low  | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |

表 6-30. RGMII[x]\_RD[3:0], and RGMII[x]\_RX\_CTL Timing Requirements – RGMII Mode

see 図 6-26

| NO.    | PARAMETER             | DESCRIPTION                                                     | MODE     | MIN | MAX | UNIT |
|--------|-----------------------|-----------------------------------------------------------------|----------|-----|-----|------|
| RGMII4 | $t_{su(RD-RXC)}$      | Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC high/low | 10Mbps   | 1   |     | ns   |
|        |                       |                                                                 | 100Mbps  | 1   |     | ns   |
|        |                       |                                                                 | 1000Mbps | 1   |     | ns   |
|        | $t_{su(RX\_CTL-RXC)}$ | Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low  | 10Mbps   | 1   |     | ns   |
|        |                       |                                                                 | 100Mbps  | 1   |     | ns   |
|        |                       |                                                                 | 1000Mbps | 1   |     | ns   |
| RGMII5 | $t_h(RXC-RD)$         | Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low   | 10Mbps   | 1   |     | ns   |
|        |                       |                                                                 | 100Mbps  | 1   |     | ns   |
|        |                       |                                                                 | 1000Mbps | 1   |     | ns   |
|        | $t_h(RXC-RX\_CTL)$    | Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low    | 10Mbps   | 1   |     | ns   |
|        |                       |                                                                 | 100Mbps  | 1   |     | ns   |
|        |                       |                                                                 | 1000Mbps | 1   |     | ns   |



- A. RGMII[x]\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII[x]\_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_RXC and data bits 7-4 on the falling edge of RGMII[x]\_RXC. Similarly, RGMII[x]\_RX\_CTL carries RXDV on rising edge of RGMII[x]\_RXC and RXERR on falling edge of RGMII[x]\_RXC.

図 6-26. CPSW3G RGMII[x]\_RXC, RGMII[x]\_RD[3:0], RGMII[x]\_RX\_CTL Timing Requirements - RGMII Mode

**表 6-31. RGMII[x]\_TXC Switching Characteristics – RGMII Mode**

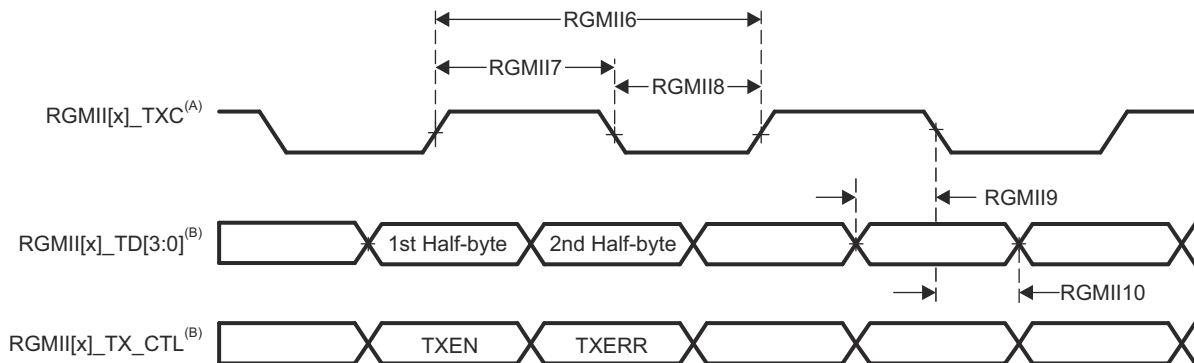
see 図 6-27

| NO.    | PARAMETER     | DESCRIPTION                       | MODE     | MIN | MAX | UNIT |
|--------|---------------|-----------------------------------|----------|-----|-----|------|
| RGMII6 | $t_{c(TXC)}$  | Cycle time, RGMII[x]_TXC          | 10Mbps   | 360 | 440 | ns   |
|        |               |                                   | 100Mbps  | 36  | 44  | ns   |
|        |               |                                   | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII7 | $t_{w(TXCH)}$ | Pulse duration, RGMII[x]_TXC high | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII8 | $t_{w(TXCL)}$ | Pulse duration, RGMII[x]_TXC low  | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |

**表 6-32. RGMII[x]\_TD[3:0] and RGMII[x]\_TX\_CTL Switching Characteristics – RGMII Mode**

see 図 6-27

| NO.     | PARAMETER              | DESCRIPTION                                                          | MODE     | MIN | MAX | UNIT |
|---------|------------------------|----------------------------------------------------------------------|----------|-----|-----|------|
| RGMII9  | $t_{osu(TD-TXC)}$      | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low   | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |
|         | $t_{osu(TX\_CTL-TXC)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low    | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |
| RGMII10 | $t_{oh(TXC-TD)}$       | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |
|         | $t_{oh(TXC-TX\_CTL)}$  | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low  | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |



- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII[x]\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_TXC and data bits 7-4 on the falling edge of RGMII[x]\_TXC. Similarly, RGMII[x]\_TX\_CTL carries TXEN on rising edge of RGMII[x]\_TXC and TXERR on falling edge of RGMII[x]\_TXC.

**図 6-27. CPSW3G RGMII[x]\_TXC, RGMII[x]\_TD[3:0], and RGMII[x]\_TX\_CTL Switching Characteristics - RGMII Mode**

#### 6.10.5.1.4 CPSW3G IOSETs

表 6-33 defines valid pin combinations of each CPSW3G MDIO0 IOSET.

**表 6-33. CPSW3G MDIO0 IOSETs**

| SIGNALS    | IOSET1          |         | IOSET2          |         |
|------------|-----------------|---------|-----------------|---------|
|            | BALL NAME       | MUXMODE | BALL NAME       | MUXMODE |
| MDIO0_MDIO | PRG0_PRU1_GPO18 | 4       | PRG1_MDIO0_MDIO | 4       |
| MDIO0_MDC  | PRG0_PRU1_GPO19 | 4       | PRG1_MDIO0_MDC  | 4       |

表 6-34 defines valid pin combinations of each CPSW3G RMII1 and RMII2 IOSET.

**表 6-34. CPSW3G RMII1 and RMII2 IOSETs**

| SIGNALS                     | IOSET1          |         | IOSET2          |         |
|-----------------------------|-----------------|---------|-----------------|---------|
|                             | BALL NAME       | MUXMODE | BALL NAME       | MUXMODE |
| RMII_REF_CLK <sup>(1)</sup> | PRG1_PRU0_GPO10 | 5       | PRG0_PRU0_GPO10 | 5       |
| RMII1_CRS_DV                | PRG1_PRU1_GPO19 | 5       | PRG0_PRU1_GPO19 | 5       |
| RMII1_RX_ER                 | PRG1_PRU0_GPO9  | 5       | PRG0_PRU0_GPO9  | 5       |
| RMII1_RXD0                  | PRG1_PRU1_GPO7  | 5       | PRG0_PRU1_GPO7  | 5       |
| RMII1_RXD1                  | PRG1_PRU1_GPO9  | 5       | PRG0_PRU1_GPO9  | 5       |
| RMII1_TXD0                  | PRG1_PRU1_GPO10 | 5       | PRG0_PRU1_GPO10 | 5       |
| RMII1_TXD1                  | PRG1_PRU1_GPO17 | 5       | PRG0_PRU1_GPO17 | 5       |
| RMII1_TX_EN                 | PRG1_PRU1_GPO18 | 5       | PRG0_PRU1_GPO18 | 5       |
| RMII2_CRS_DV                | PRG1_PRU1_GPO13 | 5       | PRG1_PRU1_GPO13 | 5       |
| RMII2_RX_ER                 | PRG1_PRU1_GPO4  | 5       | PRG1_PRU1_GPO4  | 5       |
| RMII2_RXD0                  | PRG1_PRU1_GPO0  | 5       | PRG1_PRU1_GPO0  | 5       |
| RMII2_RXD1                  | PRG1_PRU1_GPO1  | 5       | PRG1_PRU1_GPO1  | 5       |
| RMII2_TXD0                  | PRG1_PRU1_GPO11 | 5       | PRG1_PRU1_GPO11 | 5       |
| RMII2_TXD1                  | PRG1_PRU1_GPO12 | 5       | PRG1_PRU1_GPO12 | 5       |
| RMII2_TX_EN                 | PRG1_PRU1_GPO15 | 5       | PRG1_PRU1_GPO15 | 5       |

(1) RMII\_REF\_CLK is common to both RMII1 and RMII2. For proper operation, all pin multiplexed signal assignments must use the same IOSET.

表 6-35 defines valid pin combinations of each CPSW3G RGMII1 IOSET.

**表 6-35. CPSW3G RGMII1 IOSETs**

| SIGNALS       | IOSET1          |         | IOSET2          |         |
|---------------|-----------------|---------|-----------------|---------|
|               | BALL NAME       | MUXMODE | BALL NAME       | MUXMODE |
| RGMII1_TX_CTL | PRG1_PRU0_GPO9  | 4       | PRG1_PRU0_GPO9  | 4       |
| RGMII1_TXC    | PRG1_PRU0_GPO10 | 4       | PRG1_PRU0_GPO10 | 4       |
| RGMII1_TD0    | PRG1_PRU1_GPO7  | 4       | PRG1_PRU1_GPO7  | 4       |
| RGMII1_TD1    | PRG1_PRU1_GPO9  | 4       | PRG1_PRU1_GPO9  | 4       |
| RGMII1_TD2    | PRG1_PRU1_GPO10 | 4       | PRG1_PRU1_GPO10 | 4       |
| RGMII1_TD3    | PRG1_PRU1_GPO17 | 4       | PRG1_PRU1_GPO17 | 4       |
| RGMII1_RX_CTL | PRG0_PRU0_GPO9  | 4       | PRG1_PRU0_GPO5  | 4       |
| RGMII1_RXC    | PRG0_PRU0_GPO10 | 4       | PRG1_PRU0_GPO8  | 4       |
| RGMII1_RD0    | PRG0_PRU1_GPO7  | 4       | PRG1_PRU1_GPO5  | 4       |
| RGMII1_RD1    | PRG0_PRU1_GPO9  | 4       | PRG1_PRU1_GPO8  | 4       |
| RGMII1_RD2    | PRG0_PRU1_GPO10 | 4       | PRG1_PRU1_GPO18 | 4       |

表 6-35. CPSW3G RGMII1 IOSETs (続き)

| SIGNALS    | IOSET1          |         | IOSET2          |         |
|------------|-----------------|---------|-----------------|---------|
|            | BALL NAME       | MUXMODE | BALL NAME       | MUXMODE |
| RGMII1_RD3 | PRG0_PRU1_GPO17 | 4       | PRG1_PRU1_GPO19 | 4       |

#### 6.10.5.2 DDRSS

For more details about features and additional description information on the device (LP)DDR4 Memory Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-36 and 図 6-28 present switching characteristics for DDRSS.

表 6-36. DDRSS Switching Characteristics

see 図 6-28

| NO. | PARAMETER                  |                                 | DDR TYPE | MIN                 | MAX | UNIT |
|-----|----------------------------|---------------------------------|----------|---------------------|-----|------|
| 1   | $t_{c(DDR\_CKP/DDR\_CKN)}$ | Cycle time, DDR_CKP and DDR_CKN | LPDDR4   | 1.25 <sup>(1)</sup> | 20  | ns   |
|     |                            |                                 | DDR4     | 1.25 <sup>(1)</sup> | 1.6 | ns   |

- (1) Minimum DDR clock Cycle time will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to [AM64x\AM243x DDR Board Design and Layout Guidelines](#) for the proper PCB implementation to achieve maximum DDR frequency.

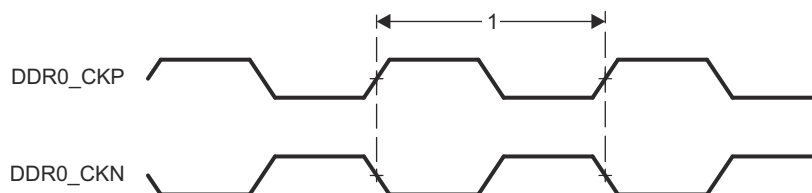


図 6-28. DDRSS Switching Characteristics

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

### 6.10.5.3 ECAP

表 6-37, 表 6-38, 図 6-29, 表 6-39, and 図 6-30 present timing conditions, requirements, and switching characteristics for ECAP.

**表 6-37. ECAP Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

**表 6-38. ECAP Timing Requirements**

see 図 6-29

| NO.  | PARAMETER            | DESCRIPTION                        | MIN                   | MAX | UNIT |
|------|----------------------|------------------------------------|-----------------------|-----|------|
| CAP1 | t <sub>w</sub> (CAP) | Pulse duration, CAP (asynchronous) | 2 + 2P <sup>(1)</sup> |     | ns   |

(1) P = sysclk period in ns.



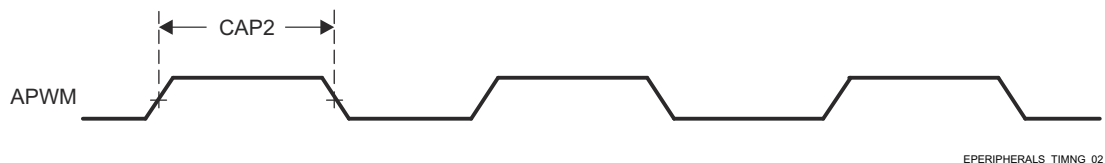
**図 6-29. ECAP Timings Requirements**

**表 6-39. ECAP Switching Characteristics**

see 図 6-30

| NO.  | PARAMETER             | DESCRIPTION                    | MIN                    | MAX | UNIT |
|------|-----------------------|--------------------------------|------------------------|-----|------|
| CAP2 | t <sub>w</sub> (APWM) | Pulse duration, APWMx high/low | -2 + 2P <sup>(1)</sup> |     | ns   |

(1) P = sysclk period in ns.



**図 6-30. ECAP Switching Characteristics**

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.4 EPWM

表 6-40, 表 6-41, 図 6-31, 表 6-42, 図 6-32, 図 6-33, and 図 6-34 present timing conditions, requirements, and switching characteristics for EPWM.

**表 6-40. EPWM Timing Conditions**

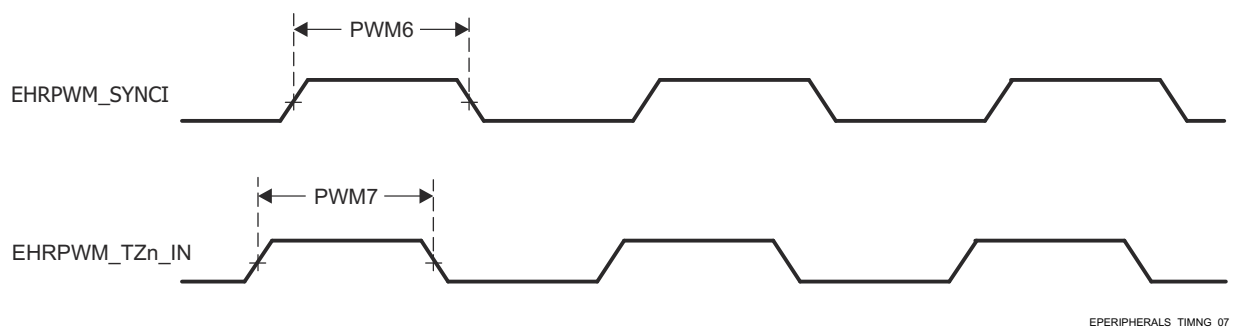
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

**表 6-41. EPWM Timing Requirements**

see 図 6-31

| NO.  | PARAMETER               | DESCRIPTION                       | MIN                   | MAX | UNIT |
|------|-------------------------|-----------------------------------|-----------------------|-----|------|
| PWM6 | t <sub>w</sub> (SYNCIN) | Pulse duration, EHRPWM_SYNCIN     | 2 + 2P <sup>(1)</sup> |     | ns   |
| PWM7 | t <sub>w</sub> (TZ)     | Pulse duration, EHRPWM_TZn_IN low | 2 + 3P <sup>(1)</sup> |     | ns   |

(1) P = sysclk period in ns.



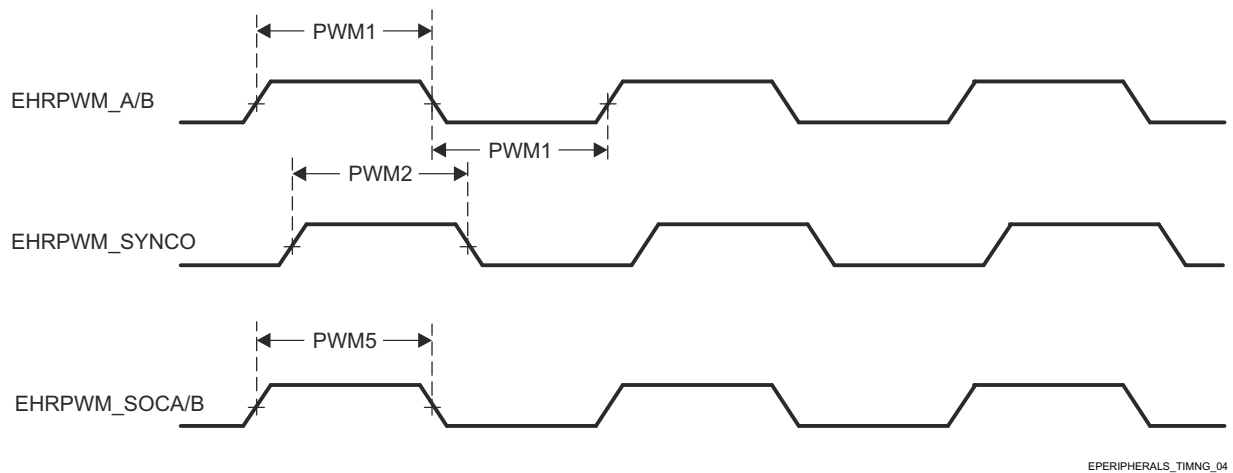
**図 6-31. EPWM Timing Requirements**

**表 6-42. EPWM Switching Characteristics**

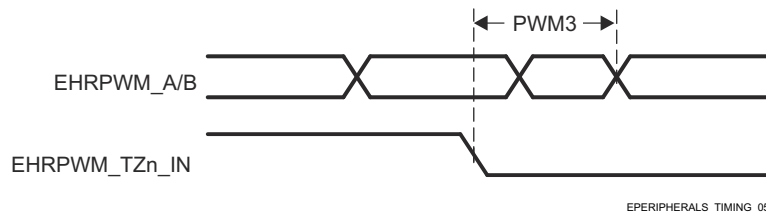
see 図 6-32, 図 6-33, and 図 6-34

| NO.  | PARAMETER        | DESCRIPTION                                                    | MIN                  | MAX | UNIT |
|------|------------------|----------------------------------------------------------------|----------------------|-----|------|
| PWM1 | $t_{w(PWM)}$     | Pulse duration, EHRPWM_A/B high/low                            | P - 3 <sup>(1)</sup> |     | ns   |
| PWM2 | $t_{w(SYNCO)}$   | Pulse duration, EHRPWM_SYNCO                                   | P - 3 <sup>(1)</sup> |     | ns   |
| PWM3 | $t_{d(TZ-PWM)}$  | Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low |                      | 11  | ns   |
| PWM4 | $t_{d(TZ-PWMZ)}$ | Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z            |                      | 11  | ns   |
| PWM5 | $t_{w(SOC)}$     | Pulse duration, EHRPWM_SOC/A/B output                          | P - 3 <sup>(1)</sup> |     | ns   |

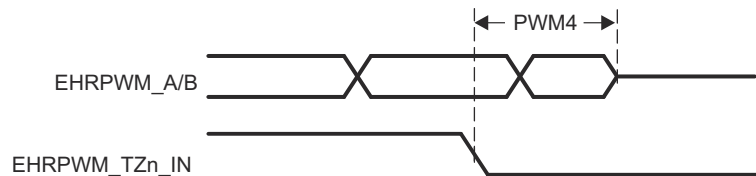
(1) P = sysclk period in ns.



**図 6-32. EHRPWM Switching Characteristics**



**図 6-33. EHRPWM\_TZn\_IN to EHRPWM\_A/B Forced Switching Characteristics**



**図 6-34. EHRPWM\_TZn\_IN to EHRPWM\_A/B Hi-Z Switching Characteristics**

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

### 6.10.5.5 EQEP

表 6-43, 表 6-44, 図 6-35, and 表 6-45 present timing conditions, requirements, and switching characteristics for EQEP.

**表 6-43. EQEP Timing Conditions**

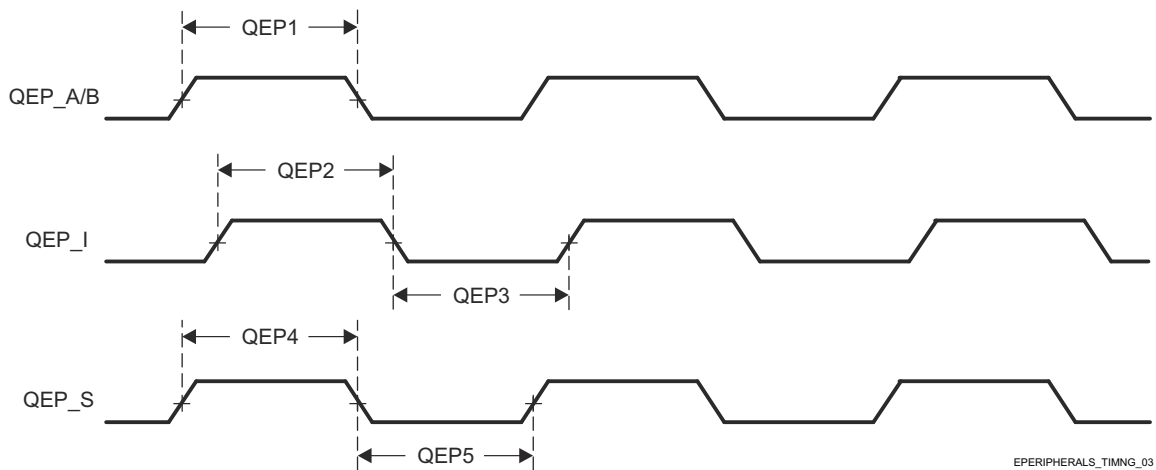
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

**表 6-44. EQEP Timing Requirements**

see 図 6-35

| NO.  | PARAMETER                           | DESCRIPTION                | MIN                   | MAX | UNIT |
|------|-------------------------------------|----------------------------|-----------------------|-----|------|
| QEP1 | t <sub>w</sub> (QEP)                | Pulse duration, QEP_A/B    | 2 + 2P <sup>(1)</sup> |     | ns   |
| QEP2 | t <sub>w</sub> (QEP <sub>I</sub> H) | Pulse duration, QEP_I high | 2 + 2P <sup>(1)</sup> |     | ns   |
| QEP3 | t <sub>w</sub> (QEP <sub>I</sub> L) | Pulse duration, QEP_I low  | 2 + 2P <sup>(1)</sup> |     | ns   |
| QEP4 | t <sub>w</sub> (QEP <sub>S</sub> H) | Pulse duration, QEP_S high | 2 + 2P <sup>(1)</sup> |     | ns   |
| QEP5 | t <sub>w</sub> (QEP <sub>S</sub> L) | Pulse duration, QEP_S low  | 2 + 2P <sup>(1)</sup> |     | ns   |

(1) P = sysclk period in ns



**図 6-35. EQEP Timing Requirements**

**表 6-45. EQEP Switching Characteristics**

| NO.  | PARAMETER                 | DESCRIPTION                                     | MIN | MAX | UNIT |
|------|---------------------------|-------------------------------------------------|-----|-----|------|
| QEP6 | t <sub>d</sub> (QEP-CNTR) | Delay time, external clock to counter increment |     | 24  | ns   |

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

### 6.10.5.6 FSI

表 6-46, 表 6-47, 図 6-36, 表 6-48, 図 6-37, 表 6-49, and 図 6-38 present timing conditions, requirements, and switching characteristics for FSI.

**表 6-46. FSI Timing Conditions**

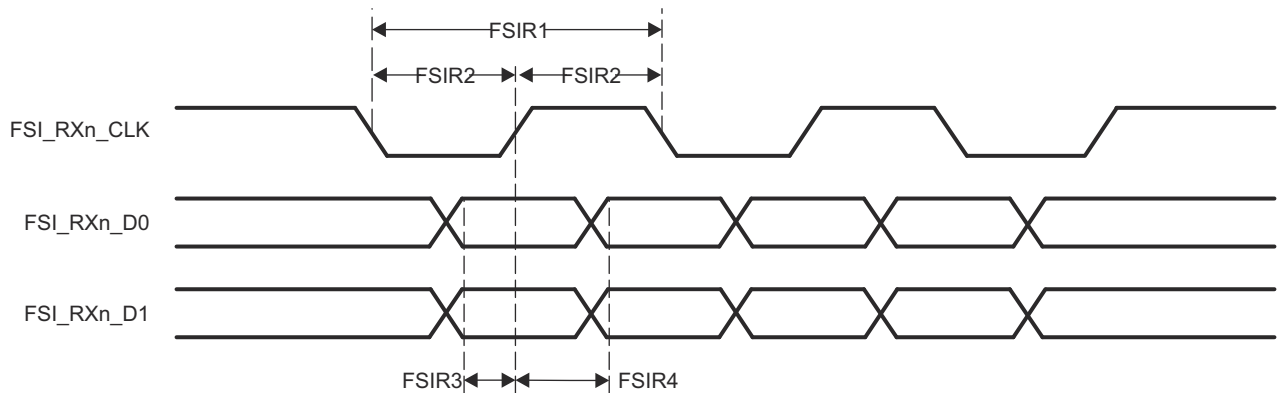
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.8 | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 1   | 7   | pF   |

**表 6-47. FSI Timing Requirements**

see 図 6-36

| NO.   |                               |                                                     | MIN                     | MAX                     | UNIT |
|-------|-------------------------------|-----------------------------------------------------|-------------------------|-------------------------|------|
| FSIR1 | t <sub>c</sub> (RX_CLK)       | Cycle time, FSI_RXn_CLK                             | 20                      |                         | ns   |
| FSIR2 | t <sub>w</sub> (RX_CLK)       | Pulse width, FSI_RXn_CLK low or FSI_RXn_CLK high    | 0.5P - 1 <sup>(1)</sup> | 0.5P + 1 <sup>(1)</sup> | ns   |
| FSIR3 | t <sub>su</sub> (RX_D-RX_CLK) | Setup time, FSI_RXn_D[1:0] valid before FSI_RXn_CLK | 3                       |                         | ns   |
| FSIR4 | t <sub>h</sub> (RX_CLK-RX_D)  | Hold time, FSI_RXn_D[1:0] valid after FSI_RXn_CLK   | 2.5                     |                         | ns   |

(1) P = FSI\_RXn\_CLK period in ns.



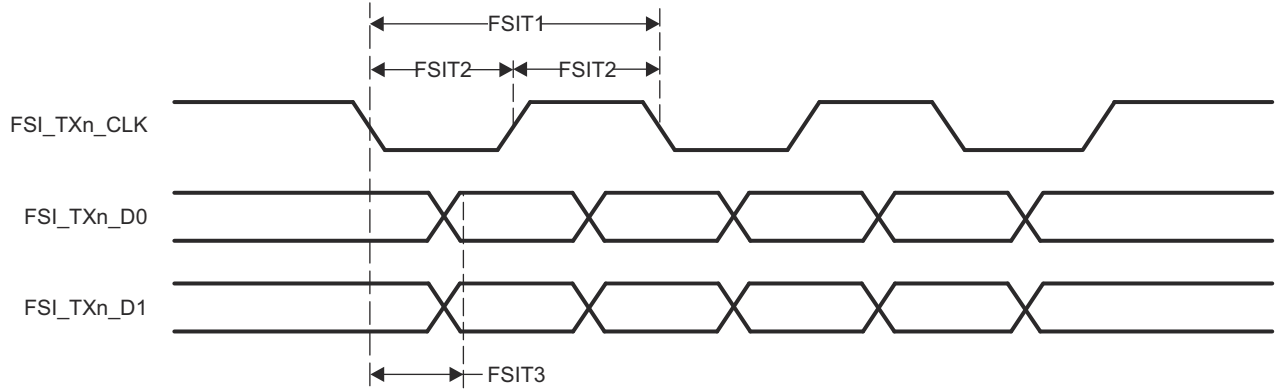
**図 6-36. FSI Timing Requirements**

**表 6-48. FSI Switching Characteristics - FSI Mode**

see 図 6-37

| NO.   | PARAMETER              |                                                                            | MODE     | MIN               | MAX                 | UNIT |
|-------|------------------------|----------------------------------------------------------------------------|----------|-------------------|---------------------|------|
| FSIT1 | $t_{c(TX\_CLK)}$       | Cycle time, FSI_TXn_CLK                                                    | FSI Mode | 20                |                     | ns   |
| FSIT2 | $t_{w(TX\_CLK)}$       | Pulse width, FSI_TXn_CLK low or FSI_TXn_CLK high                           | FSI Mode | $0.5p + 1^{(1)}$  | $0.5P - 1^{(1)}$    | ns   |
| FSIT3 | $t_{d(TX\_CLK-TX\_D)}$ | Delay time, FSI_TXn_D[1:0] valid after FSI_TXn_CLK high or FSI_TXn_CLK low | FSI Mode | $0.25P - 2^{(1)}$ | $0.25P + 2.5^{(1)}$ | ns   |

(1) P = FSI\_TXn\_CLK period in ns.



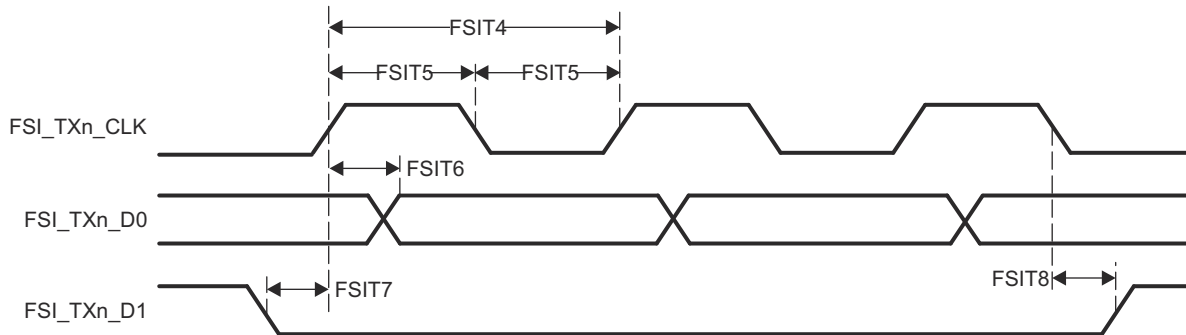
**図 6-37. FSI Switching Characteristics - FSI Mode**

**表 6-49. FSI Switching Characteristics - SPI Mode**

see 図 6-38

| NO.   | PARAMETER                |                                                  | MODE     | MIN              | MAX              | UNIT |
|-------|--------------------------|--------------------------------------------------|----------|------------------|------------------|------|
| FSIT4 | $t_{c(TX\_CLK)}$         | Cycle time, FSI_TXn_CLK                          | SPI Mode | 20               |                  | ns   |
| FSIT5 | $t_{w(TX\_CLK)}$         | Pulse width, FSI_TXn_CLK low or FSI_TXn_CLK high | SPI Mode | $0.5P + 1^{(1)}$ | $0.5P - 1^{(1)}$ | ns   |
| FSIT6 | $t_{d(TX\_CLKH-TX\_D0)}$ | Delay time, FSI_TXn_CLK high to FSI_TXn_D0 valid | SPI Mode |                  | 3                | ns   |
| FSIT7 | $t_{d(TX\_D1-TX\_CLK)}$  | Delay time, FSI_TXn_D1 low to FSI_TXn_CLK high   | SPI Mode | $P - 3^{(1)}$    |                  | ns   |
| FSIT8 | $t_{d(TX\_CLK-TX\_D1)}$  | Delay time, FSI_TXn_CLK low to FSI_TXn_D1 high   | SPI Mode | $P - 2^{(1)}$    |                  | ns   |

(1) P = FSI\_TXn\_CLK period in ns.



**図 6-38. FSI Switching Characteristics - SPI Mode**

For more information, see *Fast Serial Interface* section in *Peripherals* chapter in the device TRM.

### 6.10.5.7 GPIO

表 6-50, 表 6-51, and 表 6-52 present timing conditions, requirements, and switching characteristics for GPIO.

The device has three instances of the GPIO module.

- MCU\_GPIO0
- GPIO0
- GPIO1

#### 注

GPIO<sub>n</sub>\_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module and x represents one of the input/output signals associated with the module.

For additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**表 6-50. GPIO Timing Conditions**

| PARAMETER         |                         | BUFFER TYPE | MIN | MAX | UNIT |
|-------------------|-------------------------|-------------|-----|-----|------|
| INPUT CONDITIONS  |                         |             |     |     |      |
| SR <sub>I</sub>   | Input slew rate         | LVC MOS     | 0.2 | 6.6 | V/ns |
|                   |                         | I2C OD FS   | 0.2 | 0.8 | V/ns |
| OUTPUT CONDITIONS |                         |             |     |     |      |
| C <sub>L</sub>    | Output load capacitance | LVC MOS     | 3   | 10  | pF   |
|                   |                         | I2C OD FS   | 3   | 100 | pF   |

**表 6-51. GPIO Timing Requirements**

| NO.   | PARAMETER                | DESCRIPTION                       | MODE  | MIN                     | MAX | UNIT |
|-------|--------------------------|-----------------------------------|-------|-------------------------|-----|------|
| GPIO1 | t <sub>w</sub> (GPIO_IN) | Pulse width, GPIO <sub>n</sub> _x | 1.8 V | 2P + 2.6 <sup>(1)</sup> |     | ns   |
|       |                          |                                   | 3.3 V | 2P + 3.5 <sup>(1)</sup> |     | ns   |

(1) P = functional clock period in ns.

**表 6-52. GPIO Switching Characteristics**

| NO.   | PARAMETER                 | DESCRIPTION                       | BUFFER TYPE | MIN                         | MAX | UNIT |
|-------|---------------------------|-----------------------------------|-------------|-----------------------------|-----|------|
| GPIO2 | t <sub>w</sub> (GPIO_OUT) | Pulse width, GPIO <sub>n</sub> _x | LVC MOS     | 0.975P <sup>(1)</sup> - 3.6 |     | ns   |
|       |                           |                                   | I2C OD FS   | 160                         |     | ns   |

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

### 6.10.5.8 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 注

GPMC has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface is shown in [セクション 6.10.5.8.4](#).

[表 6-53](#) presents timing conditions for GPMC.

**表 6-53. GPMC Timing Conditions**

| PARAMETER                             |                                              |                          | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|--------------------------|------|-----|------|
| <b>INPUT CONDITIONS</b>               |                                              |                          |      |     |      |
| SR <sub>I</sub>                       | Input slew rate                              |                          | 1.65 | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |                          |      |     |      |
| C <sub>L</sub>                        | Output load capacitance                      |                          | 5    | 20  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |                          |      |     |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 133 MHz Synchronous Mode | 140  | 360 | ps   |
|                                       |                                              | All other modes          | 140  | 720 | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |                          |      | 200 | ps   |

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.8.1 GPMC and NOR Flash — Synchronous Mode

Hold time, input wait GPMC\_WAIT[j] valid after output clock GPMC\_CLK high (t<sub>h</sub>(clkH-waitV))

[表 6-54](#) and [表 6-55](#) present timing requirements and switching characteristics for GPMC and NOR Flash - Synchronous Mode.

**表 6-54. GPMC and NOR Flash Timing Requirements — Synchronous Mode**

see [図 6-39](#), [図 6-40](#), and [図 6-43](#)

| NO. | PARAMETER                 | DESCRIPTION                                                                                | MODE <sup>(5)</sup>                                            | MIN                                | MAX                                | UNIT |
|-----|---------------------------|--------------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------------------------|------------------------------------|------|
|     |                           |                                                                                            |                                                                | GPMC_FCLK = 100 MHz <sup>(2)</sup> | GPMC_FCLK = 133 MHz <sup>(2)</sup> |      |
| F12 | t <sub>su</sub> (dV-clkH) | Setup time, input data GPMC_AD[n:0] <sup>(1)</sup> valid before output clock GPMC_CLK high | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81                               | 1.12                               | ns   |
|     |                           |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06                               | 3.5                                | ns   |
| F13 | t <sub>h</sub> (clkH-dV)  | Hold time, input data GPMC_AD[n:0] <sup>(1)</sup> valid after output clock GPMC_CLK high   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 2.29                               | 2.29                               | ns   |
|     |                           |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 2.29                               | 2.29                               | ns   |

**表 6-54. GPMC and NOR Flash Timing Requirements — Synchronous Mode (続き)**

see 図 6-39, 図 6-40, and 図 6-43

| NO. | PARAMETER            | DESCRIPTION                                                                                    | MODE <sup>(5)</sup>                                            | MIN                                | MAX                                | UNIT |
|-----|----------------------|------------------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------------------------|------------------------------------|------|
|     |                      |                                                                                                |                                                                | GPMC_FCLK = 100 MHz <sup>(2)</sup> | GPMC_FCLK = 133 MHz <sup>(2)</sup> |      |
| F21 | $t_{su}(waitV-clkH)$ | Setup time, input wait GPMC_WAIT[j] <sup>(3) (4)</sup> valid before output clock GPMC_CLK high | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81                               | 1.12                               | ns   |
|     |                      |                                                                                                | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06                               | 3.5                                | ns   |
| F22 | $t_h(clkH-waitV)$    | Hold time, input wait GPMC_WAIT[j] <sup>(3) (4)</sup> valid after output clock GPMC_CLK high   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 2.29                               | 2.29                               | ns   |
|     |                      |                                                                                                | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 2.29                               | 2.29                               | ns   |

(1) Synchronous Mode supports 16-bit data bus up to 133 MHz and 32-bit data bus up to 100 MHz

(2) GPMC\_FCLK select

- gpmc\_fclk\_sel[1:0] = 2b01 to select the 100MHz GPMC\_FCLK
- gpmc\_fclk\_sel[1:0] = 2b00 to select the 133MHz GPMC\_FCLK

(3) In GPMC\_WAIT[j], j is equal to 0 or 1.

(4) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

(5) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC\_CLK frequency = GPMC\_FCLK frequency

For not\_div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:  
– GPMC\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

**表 6-55. GPMC and NOR Flash Switching Characteristics – Synchronous Mode**

see 図 6-39, 図 6-40, 図 6-41, 図 6-42, and 図 6-43

| NO.<br>(3) | PARAMETER     | DESCRIPTION                                        | MODE <sup>(17)</sup>                                       | MIN                             | MAX                             | UNIT |
|------------|---------------|----------------------------------------------------|------------------------------------------------------------|---------------------------------|---------------------------------|------|
|            |               |                                                    |                                                            | 100 MHz                         | 133 MHz                         |      |
| F0         | 1 / tc(clk)   | Period, output clock GPMC_CLK <sup>(16)</sup>      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 10.00                           | 7.52                            | ns   |
| F1         | $t_{w}(clkH)$ | Typical pulse duration, output clock GPMC_CLK high | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 0.475P<br>- 0.3 <sup>(15)</sup> | 0.475P<br>- 0.3 <sup>(15)</sup> | ns   |
| F1         | $t_{w}(clkL)$ | Typical pulse duration, output clock GPMC_CLK low  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 0.475P<br>- 0.3 <sup>(15)</sup> | 0.475P<br>- 0.3 <sup>(15)</sup> | ns   |

**表 6-55. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (続き)**

see [図 6-39](#), [図 6-40](#), [図 6-41](#), [図 6-42](#), and [図 6-43](#)

| NO.<br>(3) | PARAMETER                     | DESCRIPTION                                                                                                                                                                  | MODE <sup>(17)</sup>                                                          | MIN             | MAX      | MIN             | MAX      | UNIT |
|------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----------------|----------|-----------------|----------|------|
|            |                               |                                                                                                                                                                              |                                                                               | 100 MHz         |          | 133 MHz         |          |      |
| F2         | $t_{d(\text{clkH-csnV})}$     | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition <sup>(14)</sup>                                                                   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | F - 2.2<br>(6)  | F + 3.75 | F - 2.2<br>(6)  | F + 3.75 | ns   |
| F3         | $t_{d(\text{clkH-CSn[i]V})}$  | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid <sup>(14)</sup>                                                                      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | E - 2.2<br>(5)  | E + 3.18 | E - 2.2<br>(5)  | E + 4.5  | ns   |
| F4         | $t_{d(aV-\text{clk})}$        | Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge                                                                                            | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | B - 2.3<br>(3)  | B + 4.5  | B - 2.3<br>(3)  | B + 4.5  | ns   |
| F5         | $t_{d(\text{clkH-aIV})}$      | Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid                                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3            | 4.5      | -2.3            | 4.5      | ns   |
| F6         | $t_{d(\text{be[x]nV-clk})}$   | Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge                    | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | B - 2.3<br>(3)  | B + 1.9  | B - 2.3<br>(3)  | B + 1.9  | ns   |
| F7         | $t_{d(\text{clkH-be[x]nIV})}$ | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid <sup>(11)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | D - 2.3<br>(4)  | D + 1.9  | D - 2.3<br>(4)  | D + 1.9  | ns   |
| F7         | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(12)</sup>                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | D - 2.3<br>(4)  | D + 1.9  | D - 2.3<br>(4)  | D + 1.9  | ns   |
| F7         | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(13)</sup>                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | D - 2.3<br>(4)  | D + 1.9  | D - 2.3<br>(4)  | D + 1.9  | ns   |
| F8         | $t_{d(\text{clkH-advn})}$     | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition                                                      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | G - 2.3<br>(7)  | G + 4.5  | G - 2.3<br>(7)  | G + 4.5  | ns   |
| F9         | $t_{d(\text{clkH-advnIV})}$   | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | D - 2.3<br>(4)  | D + 4.5  | D - 2.3<br>(4)  | D + 4.5  | ns   |
| F10        | $t_{d(\text{clkH-oen})}$      | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | H - 2.3<br>(8)  | H + 3.5  | H - 2.3<br>(8)  | H + 3.5  | ns   |
| F11        | $t_{d(\text{clkH-oenIV})}$    | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid                                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | H - 2.3<br>(8)  | H + 3.5  | H - 2.3<br>(8)  | H + 3.5  | ns   |
| F14        | $t_{d(\text{clkH-wen})}$      | Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition                                                                                     | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | I - 2.3<br>(9)  | I + 4.5  | I - 2.3<br>(9)  | I + 4.5  | ns   |
| F15        | $t_{d(\text{clkH-do})}$       | Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[n:0] <sup>(1)</sup> transition <sup>(11)</sup>                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | J - 2.3<br>(10) | J + 2.7  | J - 2.3<br>(10) | J + 2.7  | ns   |

表 6-55. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (続き)

see 図 6-39, 図 6-40, 図 6-41, 図 6-42, and 図 6-43

| NO.<br>(3) | PARAMETER                          | DESCRIPTION                                                                                                                                 | MODE <sup>(17)</sup>                                       | MIN             | MAX     | MIN             | MAX     | UNIT |
|------------|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-----------------|---------|-----------------|---------|------|
|            |                                    |                                                                                                                                             |                                                            | 100 MHz         | 133 MHz | 133 MHz         | 133 MHz |      |
| F15        | $t_{d(\text{clkL}-\text{do})}$     | Delay time, GPMC_CLK falling edge to GPMC_AD[n:0] <sup>(1)</sup> data bus transition <sup>(12)</sup>                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.3<br>(10) | J + 2.7 | J - 2.3<br>(10) | J + 2.7 | ns   |
| F15        | $t_{d(\text{clkL}-\text{do})}$     | Delay time, GPMC_CLK falling edge to GPMC_AD[n:0] <sup>(1)</sup> data bus transition <sup>(13)</sup>                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.3<br>(10) | J + 2.7 | J - 2.3<br>(10) | J + 2.7 | ns   |
| F17        | $t_{d(\text{clkH}-\text{be}[x]n)}$ | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition <sup>(11)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.3<br>(10) | J + 1.9 | J - 2.3<br>(10) | J + 1.9 | ns   |
| F17        | $t_{d(\text{clkL}-\text{be}[x]n)}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(12)</sup>                                                    | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.3<br>(10) | J + 1.9 | J - 2.3<br>(10) | J + 1.9 | ns   |
| F17        | $t_{d(\text{clkL}-\text{be}[x]n)}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(13)</sup>                                                    | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.3<br>(10) | J + 1.9 | J - 2.3<br>(10) | J + 1.9 | ns   |
| F18        | $t_{w(\text{csnV})}$               | Pulse duration, output chip select GPMC_CSn[i] <sup>(14)</sup> low                                                                          | Read                                                       | A               |         | A               |         | ns   |
|            |                                    |                                                                                                                                             | Write                                                      | A               |         | A               |         | ns   |
| F19        | $t_{w(\text{be}[x]nV)}$            | Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low                     | Read                                                       | C               |         | C               |         | ns   |
|            |                                    |                                                                                                                                             | Write                                                      | C               |         | C               |         | ns   |
| F20        | $t_{w(\text{advnV})}$              | Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low                                                             | Read                                                       | K               |         | K               |         | ns   |
|            |                                    |                                                                                                                                             | Write                                                      | K               |         | K               |         | ns   |

- (1) Synchronous Mode supports 16-bit data bus up to 133 MHz and 32-bit data bus up to 100 MHz
- (2) For single read:  $A = (\text{CSRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$   
 For burst read:  $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$   
 For burst write:  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$   
 With n being the page burst access number.
- (3)  $B = \text{ClkActivationTime} \times \text{GPMC\_FCLK}^{(15)}$
- (4) For single read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$   
 For burst read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$   
 For burst write:  $D = (\text{WrCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$
- (5) For single read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$   
 For burst read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$   
 For burst write:  $E = (\text{CSWrOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(15)}$
- (6) For csn falling edge (CS activated):
- Case GPMCFCLKDIVIDER = 0:
    - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
  - Case GPMCFCLKDIVIDER = 1:
    - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
    - $F = (1 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
  - Case GPMCFCLKDIVIDER = 2:
    - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((CSOnTime - ClkActivationTime) is a multiple of 3)
    - $F = (1 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
    - $F = (2 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)
- (7) For ADV falling edge (ADV activated):
- Case GPMCFCLKDIVIDER = 0:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
  - Case GPMCFCLKDIVIDER = 1:

- $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
- $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
- Case GPMCFCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and WEOntime are odd) or (ClkActivationTime and WEOntime are even)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((WEOntime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((WEOntime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((WEOntime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$
- Case GPMCFCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(15)}$  if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(15)}$  if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10)  $J = \text{GPMC\_FCLK}^{(15)}$

(11) First transfer only for CLK DIV 1 mode.

(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(13) Half cycle of GPMC\_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC\_CLKOUT divide down from GPMC\_FCLK.

(14) In GPMC\_CS*n*[*j*], *i* is equal to 0, 1, 2 or 3. In GPMC\_WAIT[*j*], *j* is equal to 0 or 1.

(15)  $P = \text{GPMC\_CLK period in ns}$

(16) Related to the GPMC\_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC\_CONFIG1\_1 configuration register bit field GPMCFCLKDIVIDER.

(17) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_1 register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

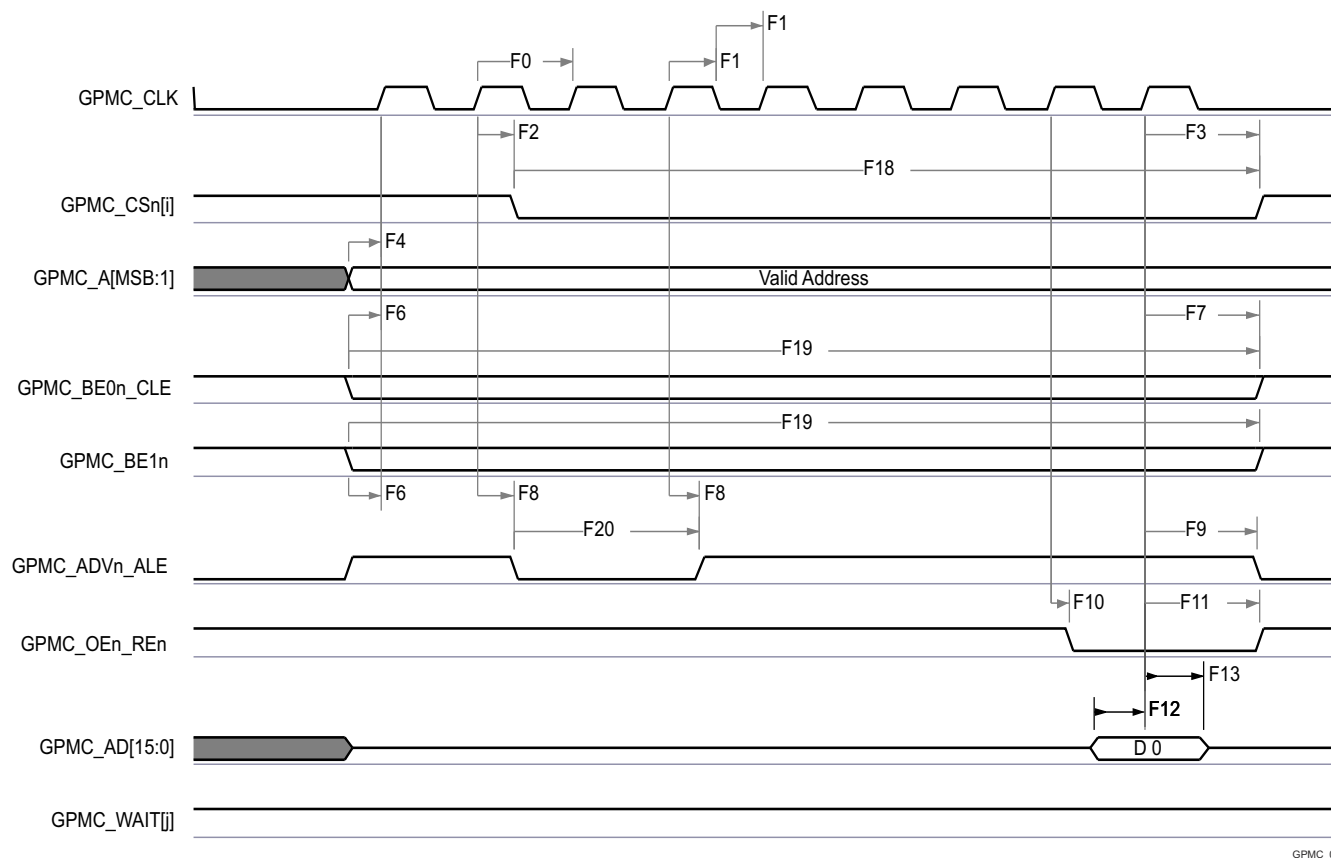
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_1 Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra\_delay:

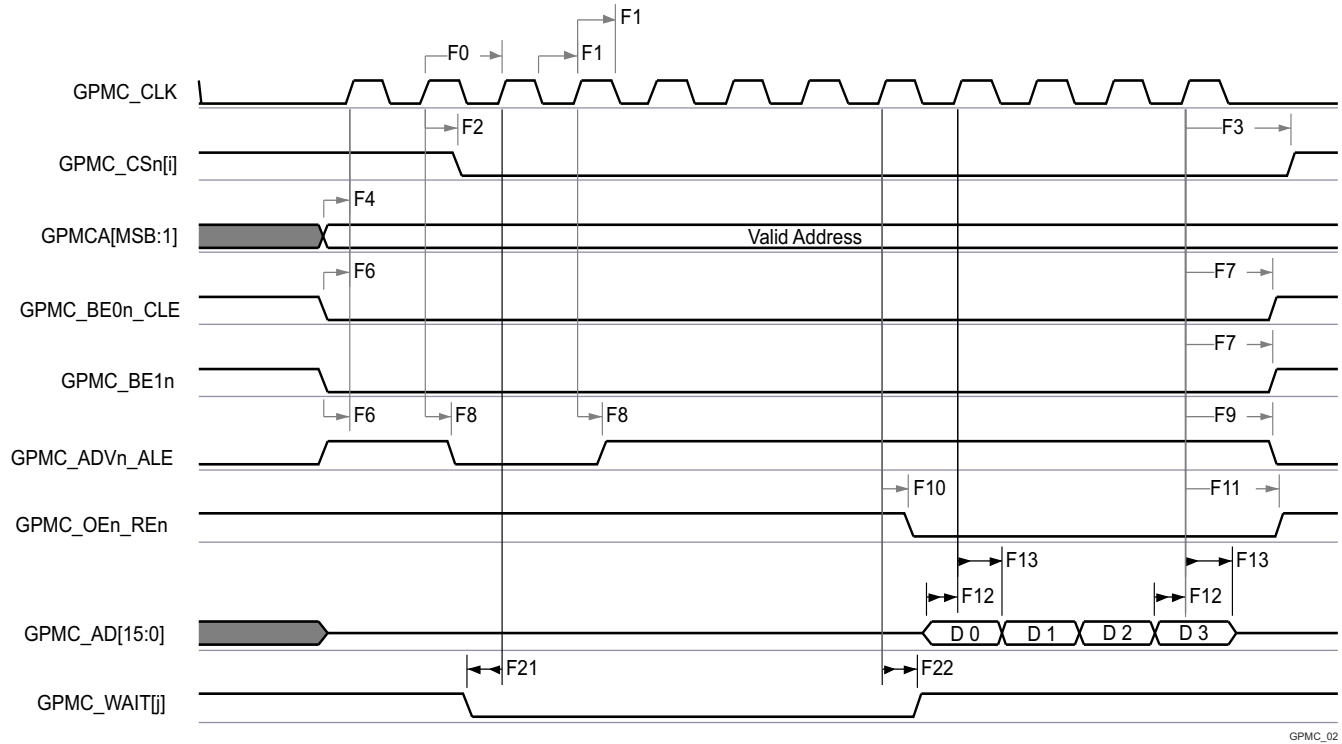
- GPMC\_CONFIG2\_1 Register: CSEXTRADELAY = 0h = CS*n* Timing control signal is not delayed
- GPMC\_CONFIG4\_1 Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC\_CONFIG4\_1 Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC\_CONFIG3\_1 Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
B. In GPMC\_WAIT[j], j is equal to 0 or 1.

6-39. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)

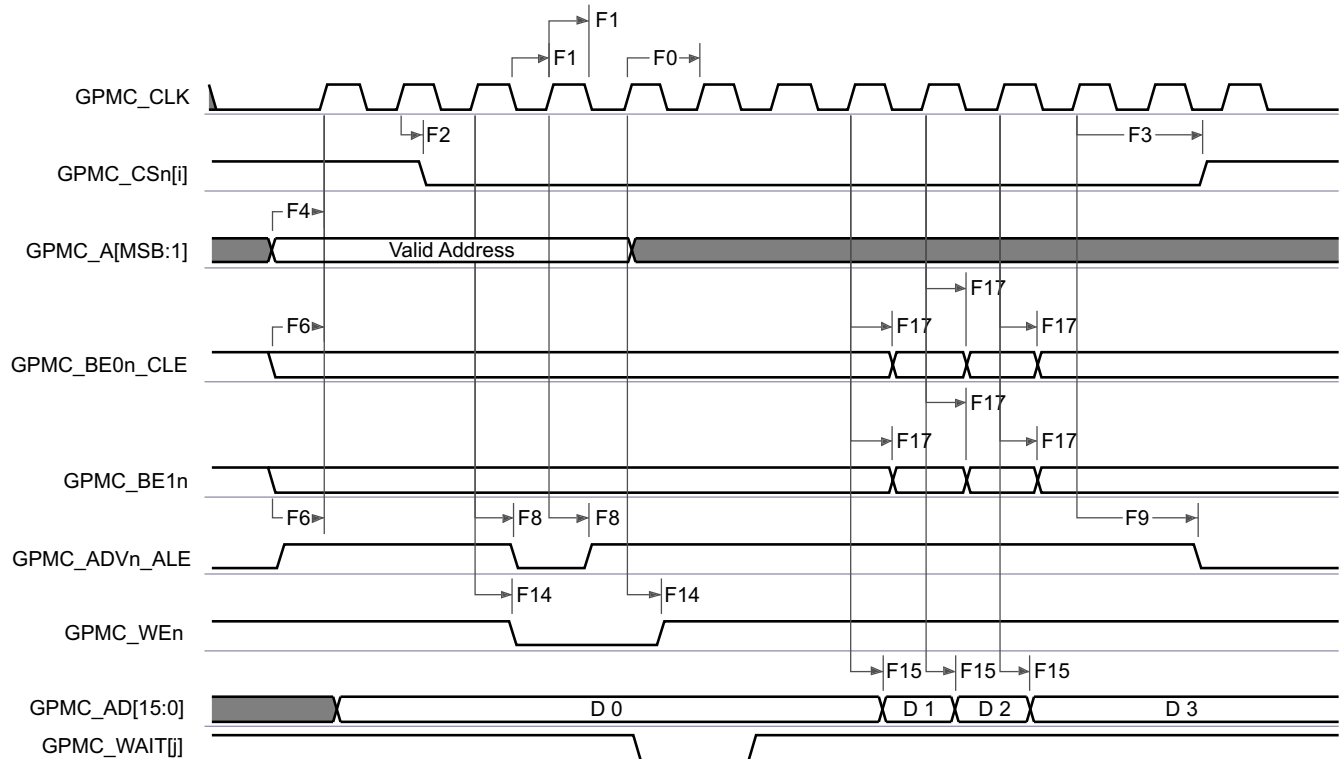
GPMC\_01



GPMC\_02

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**図 6-40. GPMC and NOR Flash — Synchronous Burst Read — 4x16-bit (GPMCFCLKDIVIDER = 0)**

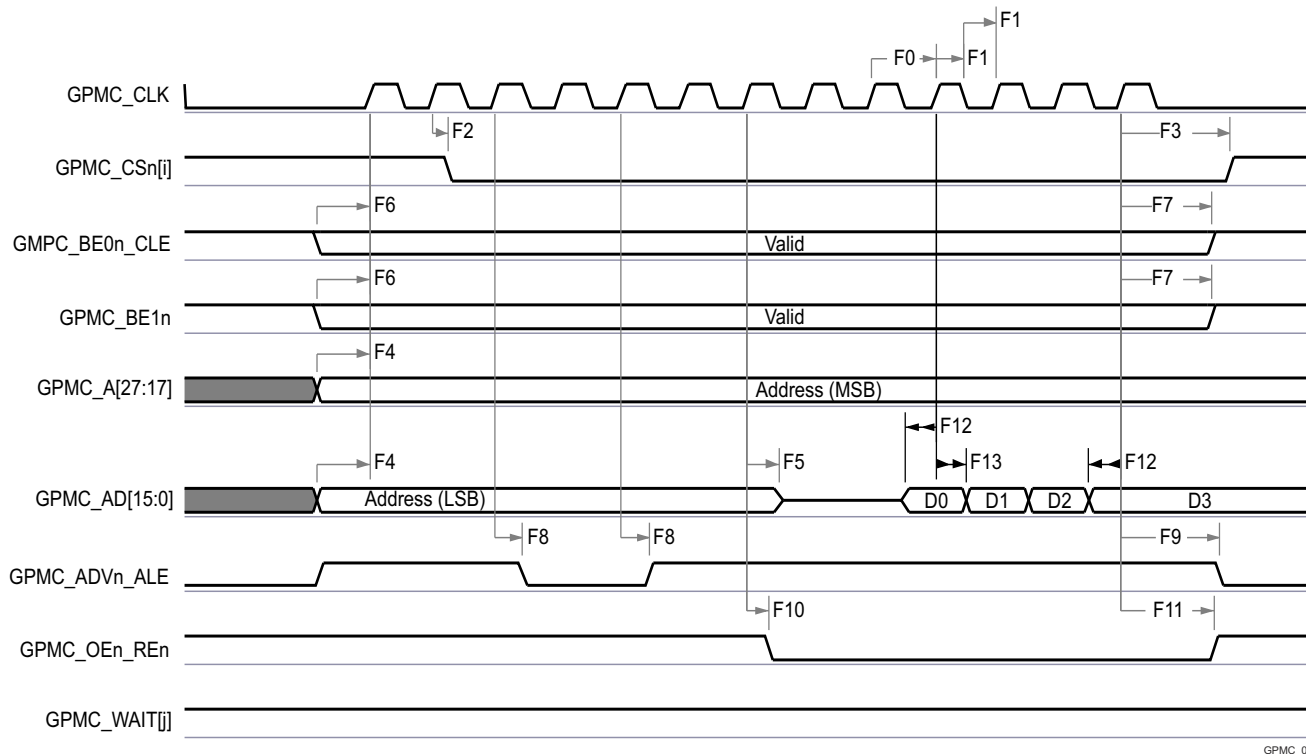


GPMC\_03

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**6-41. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**

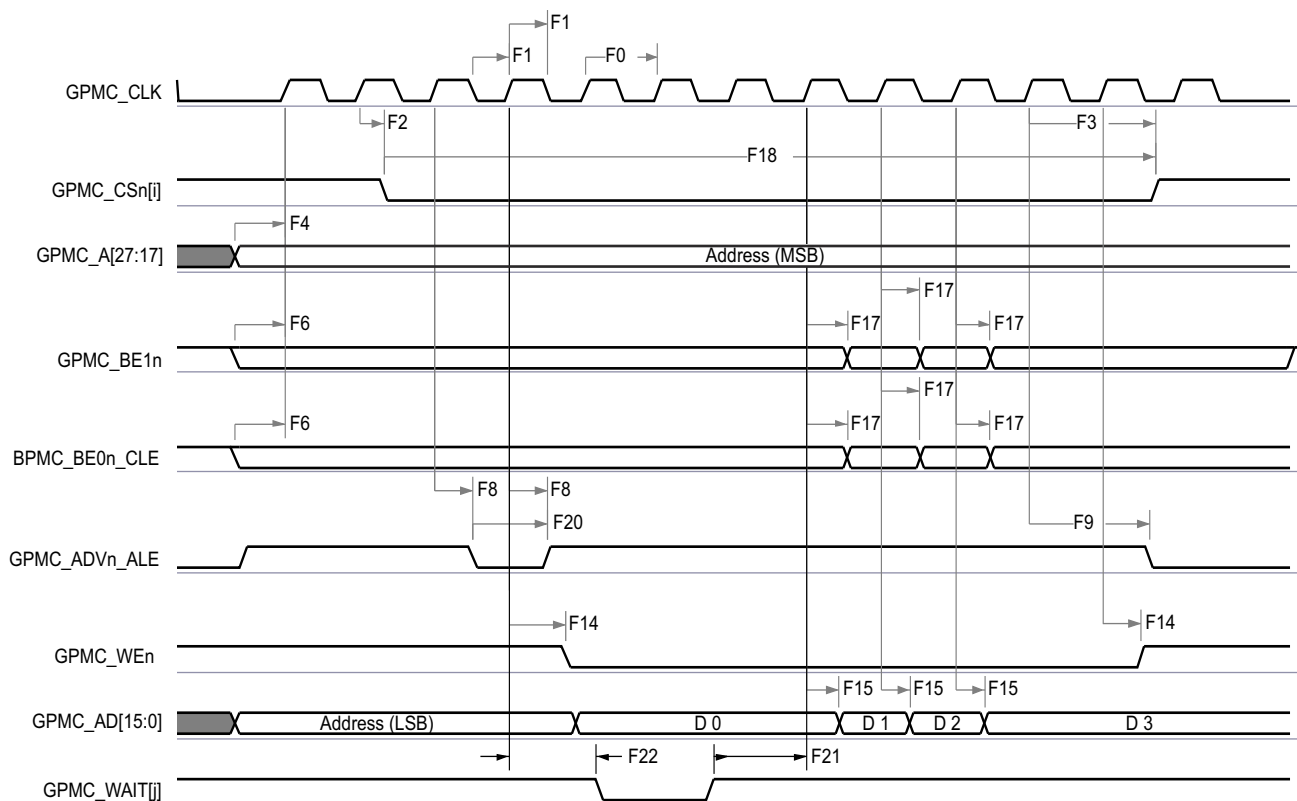


GPMC\_04

A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**6-42. GPMC and Multiplexed NOR Flash — Synchronous Burst Read**



GPMC\_05

- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3.  
 B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**図 6-43. GPMC and Multiplexed NOR Flash — Synchronous Burst Write**

### 6.10.5.8.2 GPMC and NOR Flash — Asynchronous Mode

表 6-56 and 表 6-57 present timing requirements and switching characteristics for GPMC and NOR Flash — Asynchronous Mode.

**表 6-56. GPMC and NOR Flash Timing Requirements – Asynchronous Mode**

see 図 6-44, 図 6-45, 図 6-46, and 図 6-48

| NO.                             | PARAMETER            | DESCRIPTION                           | MODE                                                       | MIN | MAX              | UNIT |
|---------------------------------|----------------------|---------------------------------------|------------------------------------------------------------|-----|------------------|------|
| FA5 <sup>(1)</sup>              | $t_{acc(d)}$         | Data access time                      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |     | H <sup>(4)</sup> | ns   |
| FA2 <sub>0</sub> <sup>(2)</sup> | $t_{acc1-pgmode(d)}$ | Page mode successive data access time | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |     | P <sup>(3)</sup> | ns   |
| FA2 <sub>1</sub> <sup>(1)</sup> | $t_{acc2-pgmode(d)}$ | Page mode first data access time      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |     | H <sup>(4)</sup> | ns   |

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (3)  $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(5)}$
- (4)  $H = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(5)}$
- (5) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

**表 6-57. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode**

see 図 6-44, 図 6-45, 図 6-46, 図 6-47, 図 6-48, and 図 6-49

| NO.  | PARAMETER             | DESCRIPTION                                                                                                                                                                   | MODE <sup>(15)</sup>                                       | MIN                     | MAX                     | UNIT |
|------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------|-------------------------|------|
|      |                       |                                                                                                                                                                               |                                                            | 133 MHz                 |                         |      |
| FA0  | $t_{w(be[x]nV)}$      | Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time                                                | Read                                                       | N <sup>(12)</sup>       |                         | ns   |
|      |                       |                                                                                                                                                                               | Write                                                      | N <sup>(12)</sup>       |                         |      |
| FA1  | $t_{w(csnV)}$         | Pulse duration, output chip select GPMC_CSn[i] <sup>(13)</sup> low                                                                                                            | Read                                                       | A <sup>(1)</sup>        |                         | ns   |
|      |                       |                                                                                                                                                                               | Write                                                      | A <sup>(1)</sup>        |                         |      |
| FA3  | $t_{d(csnV-advnIV)}$  | Delay time, output chip select GPMC_CSn[i] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE invalid                                       | Read                                                       | B - 2.1 <sup>(2)</sup>  | B + 2.1 <sup>(2)</sup>  | ns   |
|      |                       |                                                                                                                                                                               | Write                                                      | B - 2.1 <sup>(2)</sup>  | B + 2.1 <sup>(2)</sup>  |      |
| FA4  | $t_{d(csnV-oenIV)}$   | Delay time, output chip select GPMC_CSn[i] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Single read)                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C - 2.1 <sup>(3)</sup>  | C + 2.1 <sup>(3)</sup>  | ns   |
| FA9  | $t_{d(aV-csnV)}$      | Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[i] <sup>(13)</sup> valid                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.1 <sup>(9)</sup>  | J + 2.1 <sup>(9)</sup>  | ns   |
| FA10 | $t_{d(be[x]nV-csnV)}$ | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[i] <sup>(13)</sup> valid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.1 <sup>(9)</sup>  | J + 2.1 <sup>(9)</sup>  | ns   |
| FA12 | $t_{d(csnV-advnV)}$   | Delay time, output chip select GPMC_CSn[i] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE valid                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | K - 2.1 <sup>(10)</sup> | K + 2.1 <sup>(10)</sup> | ns   |
| FA13 | $t_{d(csnV-oenV)}$    | Delay time, output chip select GPMC_CSn[i] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | L - 2.1 <sup>(11)</sup> | L + 2.1 <sup>(11)</sup> | ns   |

**表 6-57. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode (続き)**

see [図 6-44](#), [図 6-45](#), [図 6-46](#), [図 6-47](#), [図 6-48](#), and [図 6-49](#)

| NO.  | PARAMETER                  | DESCRIPTION                                                                                                                  | MODE <sup>(15)</sup>                                       | MIN                    | MAX                    | UNIT |
|------|----------------------------|------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|------------------------|------------------------|------|
|      |                            |                                                                                                                              |                                                            | 133 MHz                |                        |      |
| FA16 | t <sub>w(aIV)</sub>        | Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses                              | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | G <sup>(7)</sup>       |                        | ns   |
| FA18 | t <sub>d(csnV-oenIV)</sub> | Delay time, output chip select GPMC_CS <i>n</i> [i] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Burst read) | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | I - 2.1 <sup>(8)</sup> | I + 2.1 <sup>(8)</sup> | ns   |
| FA20 | t <sub>w(aV)</sub>         | Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses                                               | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | D <sup>(4)</sup>       |                        | ns   |
| FA25 | t <sub>d(csnV-wenV)</sub>  | Delay time, output chip select GPMC_CS <i>n</i> [i] <sup>(13)</sup> valid to output write enable GPMC_WEn valid              | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | E - 2.1 <sup>(5)</sup> | E + 2.1 <sup>(5)</sup> | ns   |
| FA27 | t <sub>d(csnV-wenIV)</sub> | Delay time, output chip select GPMC_CS <i>n</i> [i] <sup>(13)</sup> valid to output write enable GPMC_WEn invalid            | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F - 2.1 <sup>(6)</sup> | F + 2.1 <sup>(6)</sup> | ns   |
| FA28 | t <sub>d(wenV-dV)</sub>    | Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid                                            | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                        | 2.1                    | ns   |
| FA29 | t <sub>d(dV-csnV)</sub>    | Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CS <i>n</i> [i] <sup>(13)</sup> valid                 | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J - 2.1 <sup>(9)</sup> | J + 2.1 <sup>(9)</sup> | ns   |
| FA37 | t <sub>d(oenV-aIV)</sub>   | Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end                                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                        | 2.1                    | ns   |

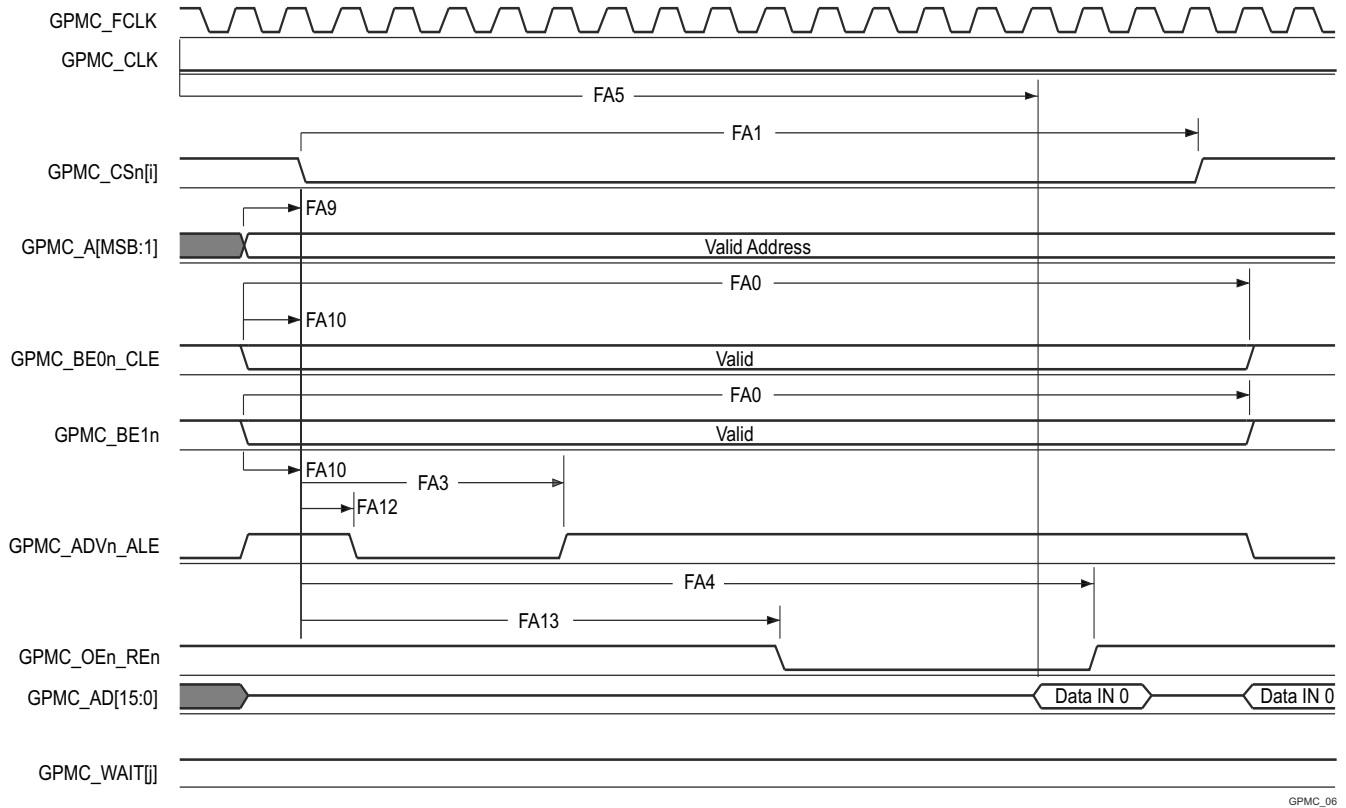
- (1) For single read:  $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 For single write:  $A = (CSWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 For burst read:  $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 For burst write:  $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 with n being the page burst access number
- (2) For reading:  $B = ((ADVrdOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
 For writing:  $B = ((ADVwrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (3)  $C = ((OEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (4)  $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (5)  $E = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (6)  $F = ((WEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (7)  $G = Cycle2CycleDelay \times GPMC\_FCLK^{(14)}$
- (8)  $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (9)  $J = (CSOnTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(14)}$
- (10)  $K = ((ADVOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (11)  $L = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (12) For single read:  $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 For single write:  $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 For burst read:  $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 For burst write:  $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (13) In GPMC\_CS*n*[i], i is equal to 0, 1, 2 or 3.
- (14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (15) For div\_by\_1\_mode:
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
 – GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

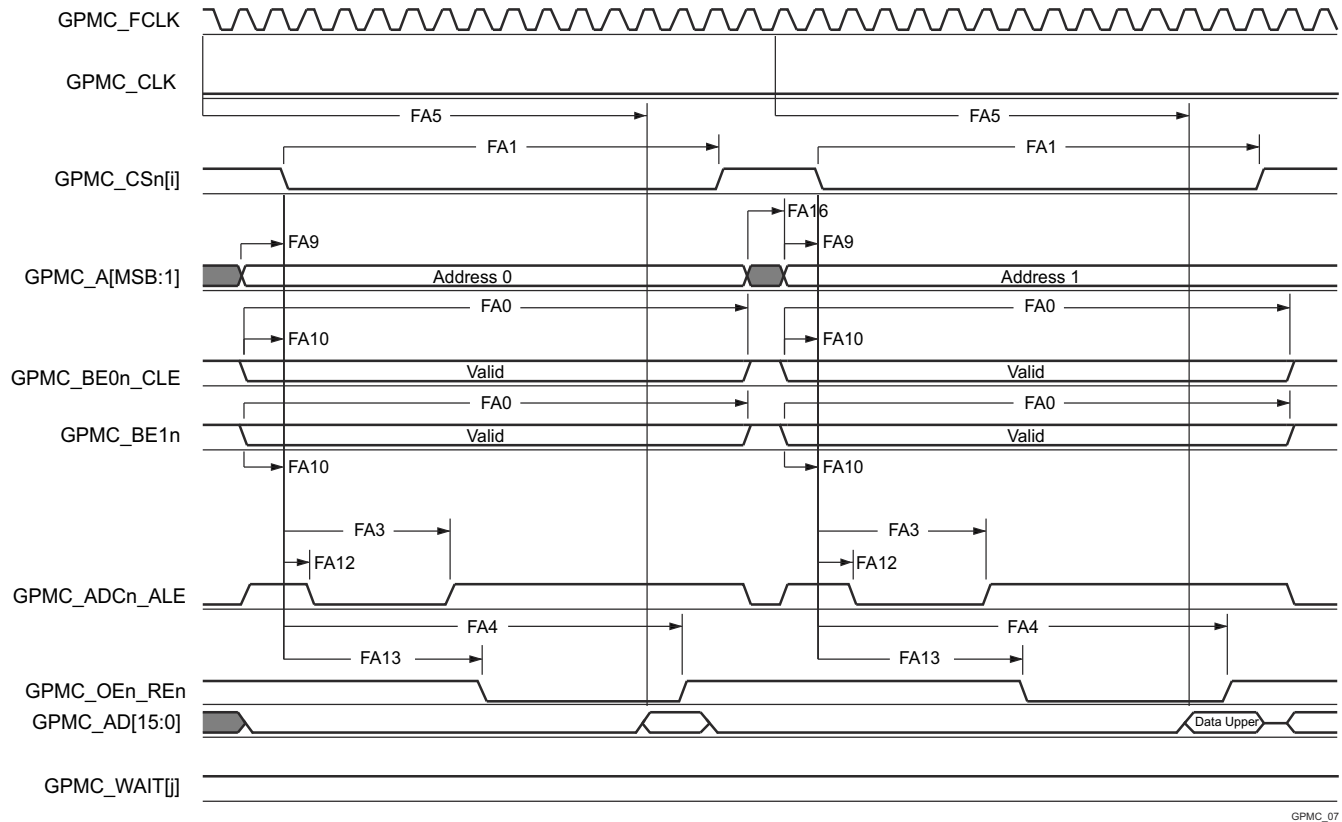
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



GPMC\_06

- In GPMC\_CS[n], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

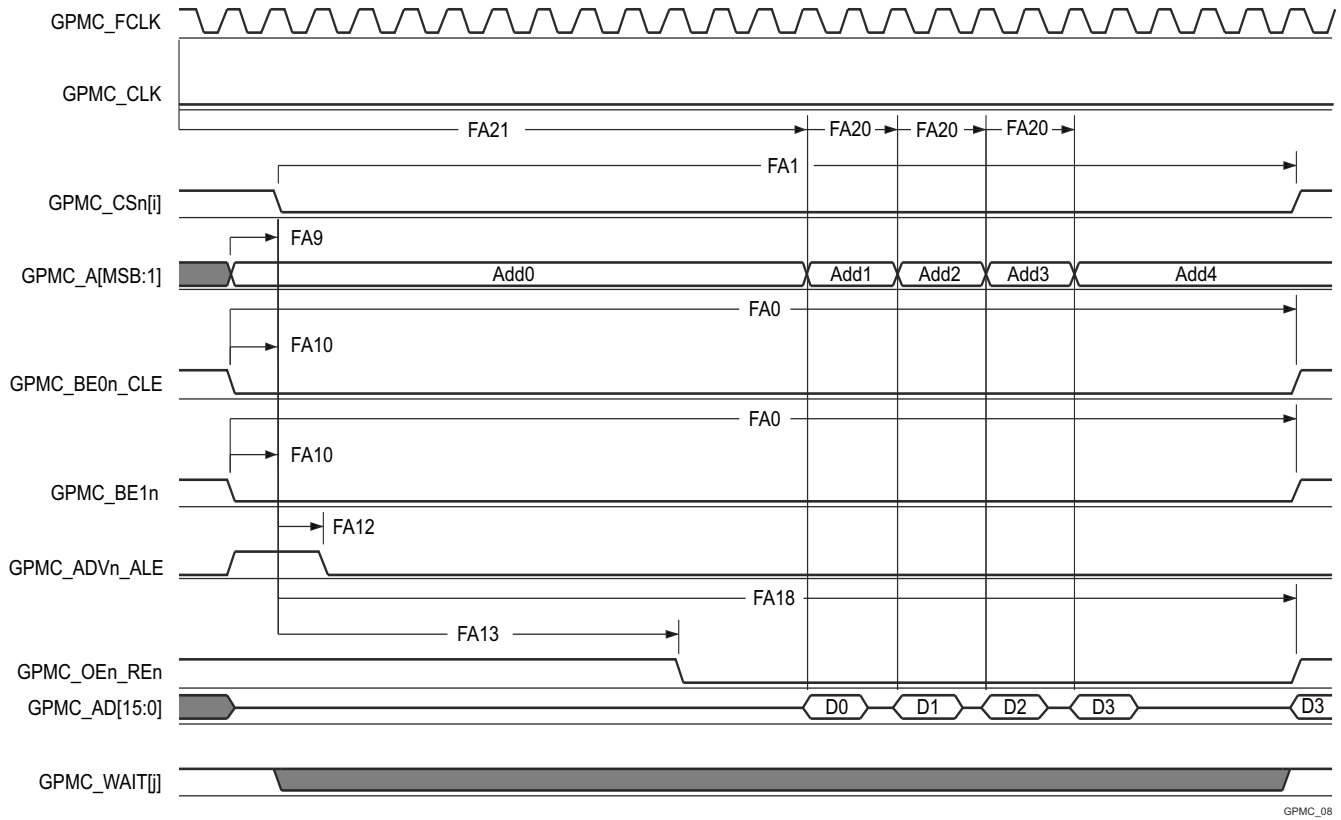
**図 6-44. GPMC and NOR Flash — Asynchronous Read — Single Word**



GPMC\_07

- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

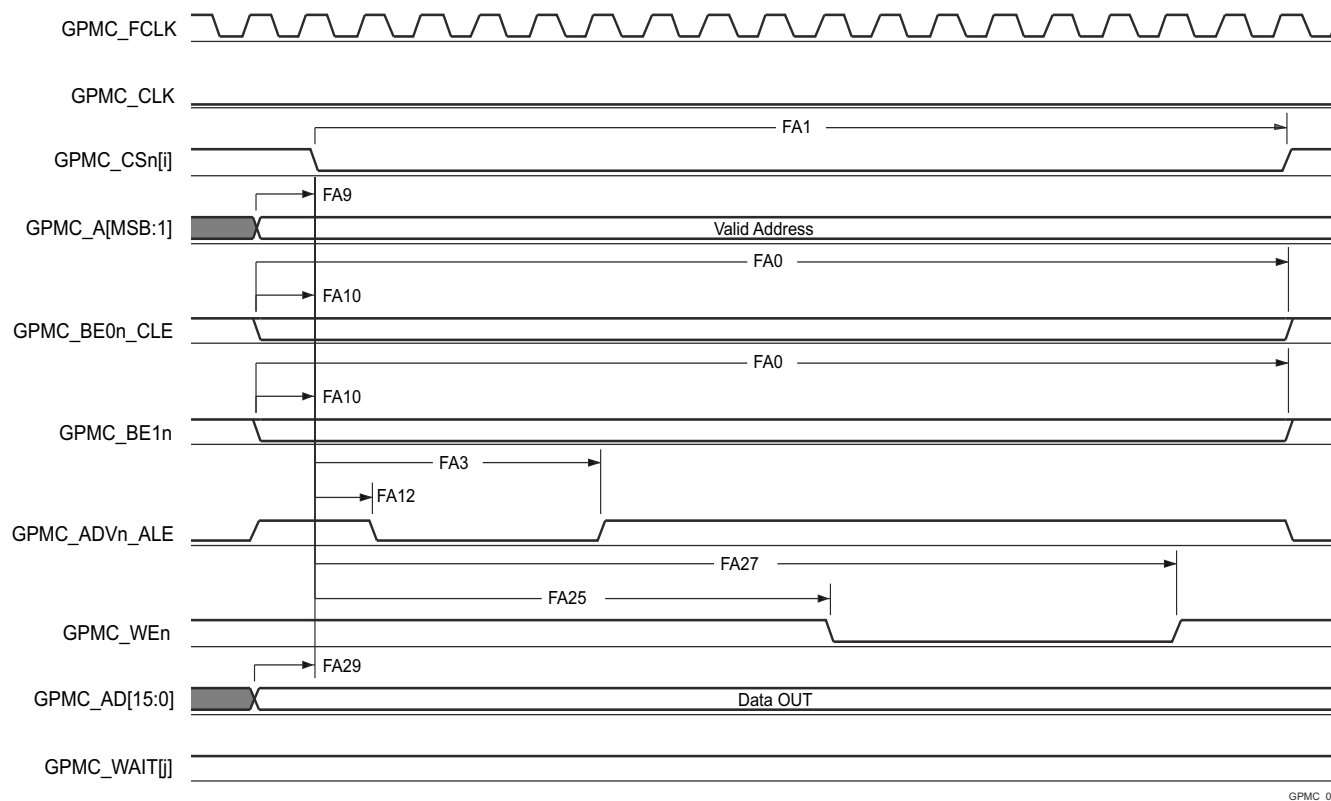
#### ✎ 6-45. GPMC and NOR Flash — Asynchronous Read — 32-Bit



GPMC\_08

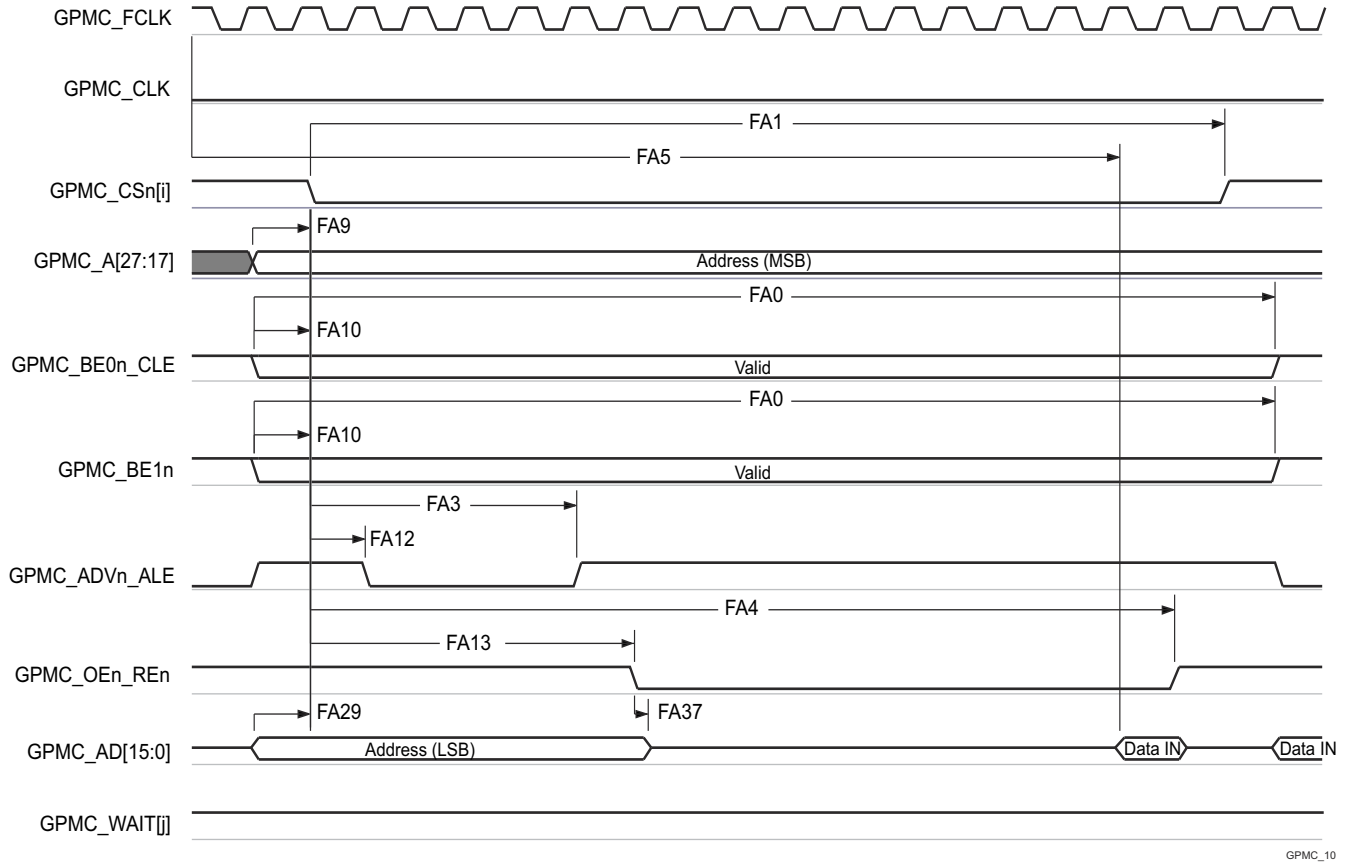
- In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**図 6-46. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16-Bit**



A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

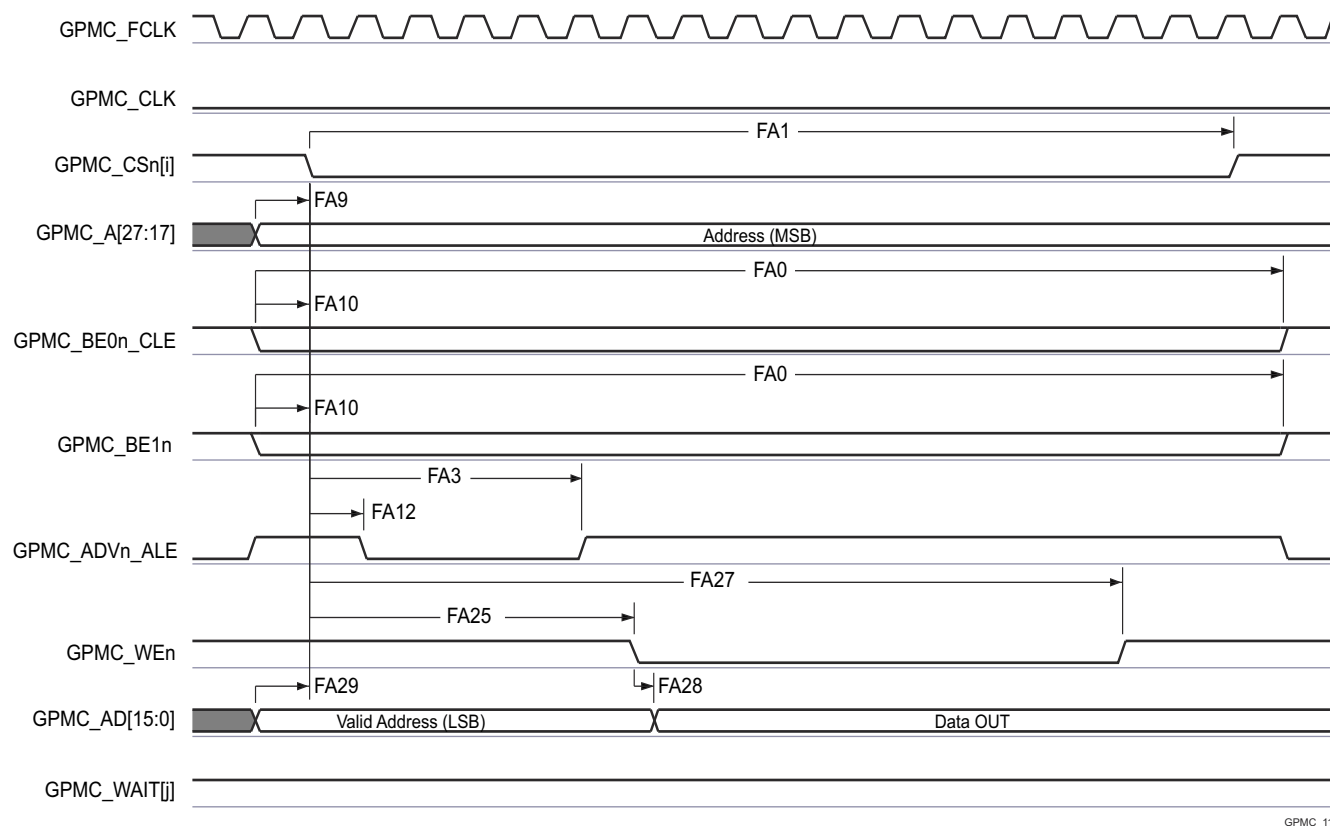
**図 6-47. GPMC and NOR Flash — Asynchronous Write — Single Word**



GPMC\_10

- In GPMC\_CS[n], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**图 6-48. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word**



A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

**图 6-49. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word**

### 6.10.5.8.3 GPMC and NAND Flash — Asynchronous Mode

表 6-58 and 表 6-59 present timing requirements and switching characteristics for GPMC and NAND Flash — Asynchronous Mode.

**表 6-58. GPMC and NAND Flash Timing Requirements – Asynchronous Mode**

see 図 6-52

| NO.                  | PARAMETER           | DESCRIPTION                                          | MODE <sup>(4)</sup>                                        | MIN     | MAX              | UNIT |
|----------------------|---------------------|------------------------------------------------------|------------------------------------------------------------|---------|------------------|------|
|                      |                     |                                                      |                                                            | 133 MHz |                  |      |
| GNF12 <sup>(1)</sup> | t <sub>acc(d)</sub> | Access time, input data GPMC_AD[15:0] <sup>(3)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |         | J <sup>(2)</sup> | ns   |

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2)  $J = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$ <sup>(3)</sup>

(3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHSIDIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

**表 6-59. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode**

see 図 6-50, 図 6-51, 図 6-52 and 図 6-53

| NO.  | PARAMETER                   |                                                                                                                             | MODE <sup>(4)</sup>                                        | MIN   | MAX   | UNIT |
|------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------|-------|------|
| GNF0 | t <sub>w(wenV)</sub>        | Pulse duration, output write enable GPMC_WEn valid                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | A     |       | ns   |
| GNF1 | t <sub>d(csnV-wenV)</sub>   | Delay time, output chip select GPMC_CS[n] <sup>(2)</sup> valid to output write enable GPMC_WEn valid                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | B - 2 | B + 2 | ns   |
| GNF2 | t <sub>w(cleH-wenV)</sub>   | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C - 2 | C + 2 | ns   |
| GNF3 | t <sub>w(wenV-dV)</sub>     | Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid                                           | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | D - 2 | D + 2 | ns   |
| GNF4 | t <sub>w(wenIV-dIV)</sub>   | Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid                                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | E - 2 | E + 2 | ns   |
| GNF5 | t <sub>w(wenIV-cleIV)</sub> | Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F - 2 | F + 2 | ns   |
| GNF6 | t <sub>w(wenIV-csnIV)</sub> | Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CS[n] <sup>(2)</sup> invalid                    | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | G - 2 | G + 2 | ns   |
| GNF7 | t <sub>w(aleH-wenV)</sub>   | Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C - 2 | C + 2 | ns   |

**表 6-59. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode (続き)**

see 図 6-50, 図 6-51, 図 6-52 and 図 6-53

| NO.   | PARAMETER              | MODE <sup>(4)</sup>                                                                                                       | MIN                                                        | MAX            | UNIT |
|-------|------------------------|---------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|----------------|------|
| GNF8  | $t_{w(wenIV-aleIV)}$   | Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F - 2    F + 2 | ns   |
| GNF9  | $t_{c(wen)}$           | Cycle time, write                                                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | H              | ns   |
| GNF10 | $t_{d(csnV-oenV)}$     | Delay time, output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(2)</sup> valid to output enable GPMC_OEn_REn valid     | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | I - 2    I + 2 | ns   |
| GNF13 | $t_{w(oenV)}$          | Pulse duration, output enable GPMC_OEn_REn valid                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | K              | ns   |
| GNF14 | $t_{c(oen)}$           | Cycle time, read                                                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | L              | ns   |
| GNF15 | $t_{w(oenIV-CSn[i]V)}$ | Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(2)</sup> invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | M - 2    M + 2 | ns   |

(1)  $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(3)}$ (2) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.

(3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC\_CLK frequency = GPMC\_FCLK frequency

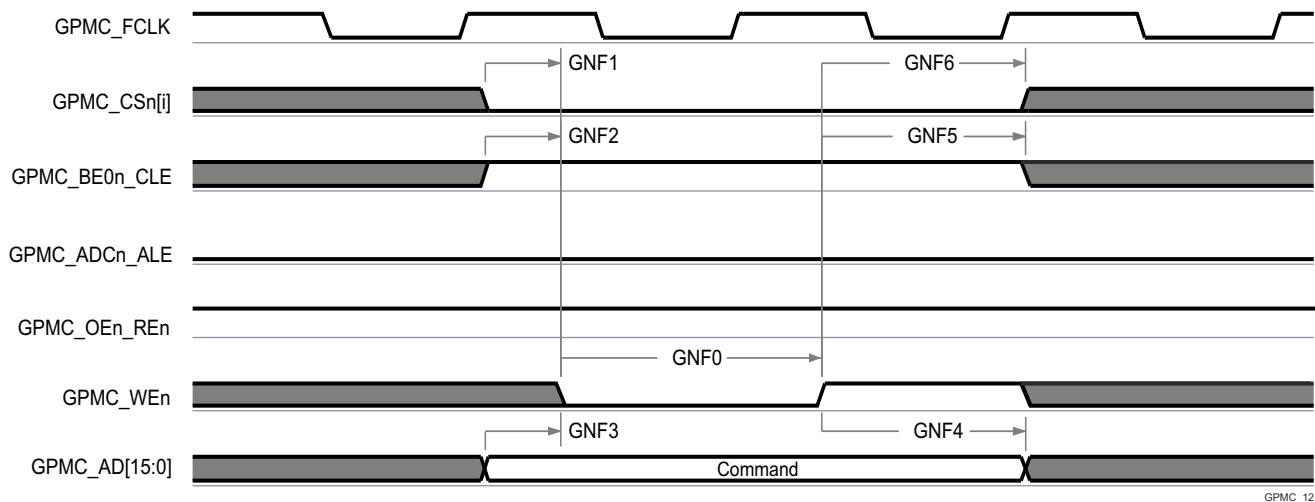
For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS

CLKOUT3 = 2000/15 = 133.33 MHz

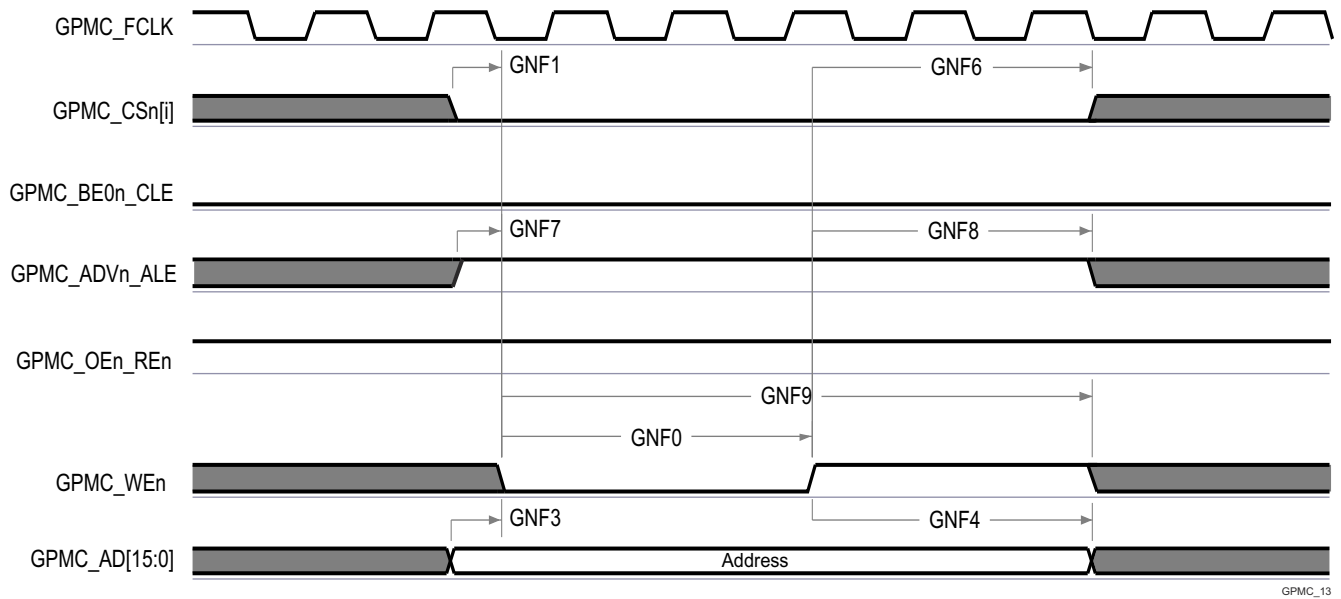
For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



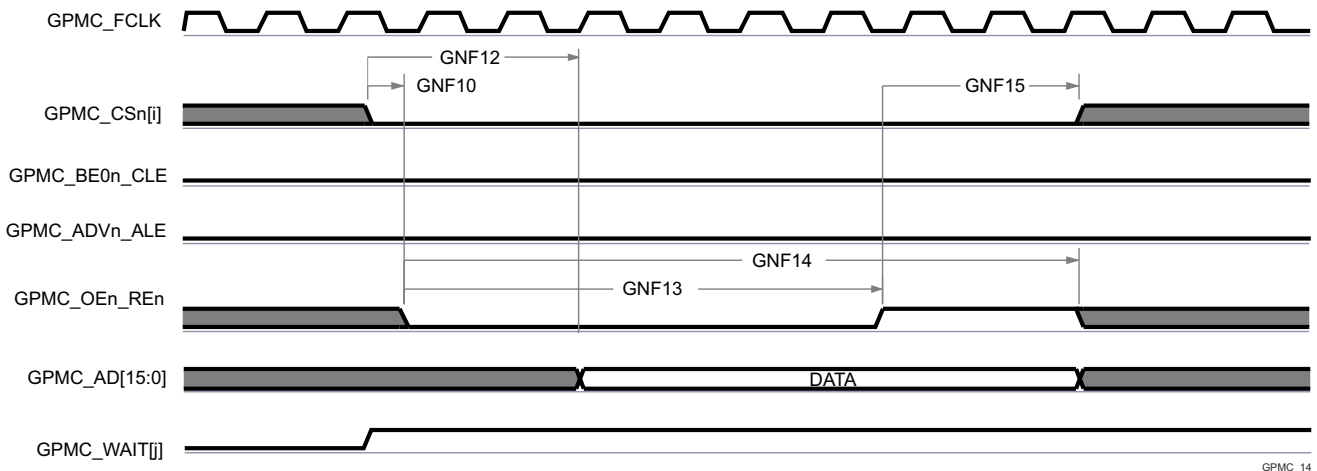
GPMC\_12

A. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.**図 6-50. GPMC and NAND Flash — Command Latch Cycle**



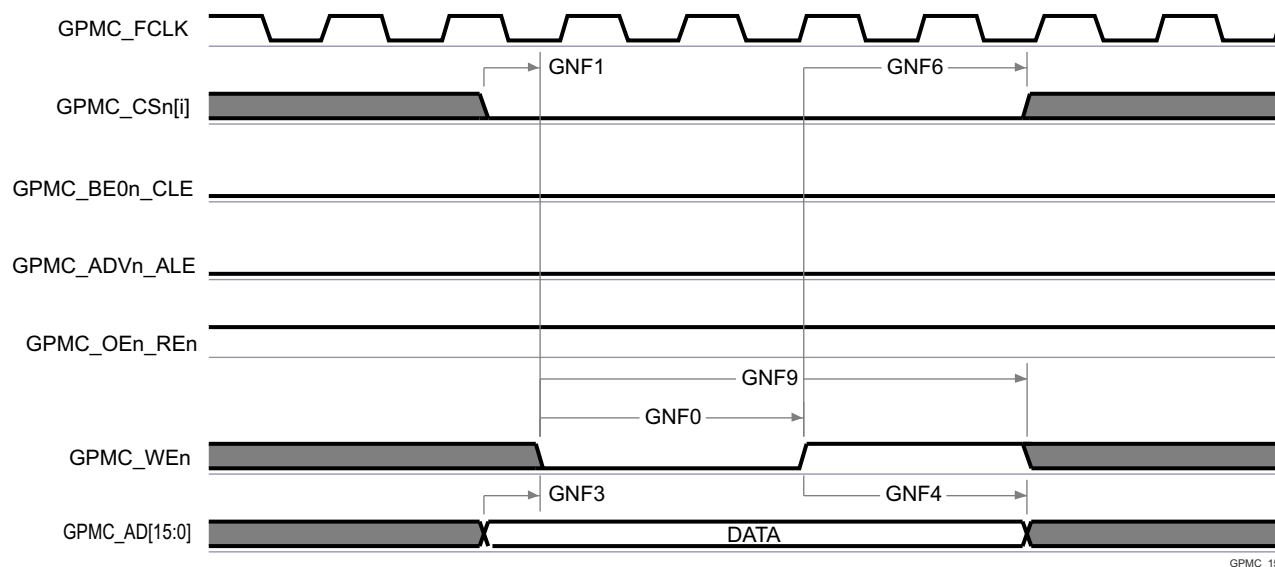
A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3.

**図 6-51. GPMC and NAND Flash — Address Latch Cycle**



- A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- B. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- C. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

**図 6-52. GPMC and NAND Flash — Data Read Cycle**



GPMC\_15

A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

**図 6-53. GPMC and NAND Flash — Data Write Cycle**

#### 6.10.5.8.4 GPMC0 IOSETs

表 6-60 defines valid pin combinations of each GPMC0 IOSET.

**表 6-60. GPMC0 IOSETs**

| SIGNALS        | IOSET1          |         | IOSET2          |         |
|----------------|-----------------|---------|-----------------|---------|
|                | BALL NAME       | MUXMODE | BALL NAME       | MUXMODE |
| GPMC0_AD0      | GPMC0_AD0       | 0       | GPMC0_AD0       | 0       |
| GPMC0_AD1      | GPMC0_AD1       | 0       | GPMC0_AD1       | 0       |
| GPMC0_AD2      | GPMC0_AD2       | 0       | GPMC0_AD2       | 0       |
| GPMC0_AD3      | GPMC0_AD3       | 0       | GPMC0_AD3       | 0       |
| GPMC0_AD4      | GPMC0_AD4       | 0       | GPMC0_AD4       | 0       |
| GPMC0_AD5      | GPMC0_AD5       | 0       | GPMC0_AD5       | 0       |
| GPMC0_AD6      | GPMC0_AD6       | 0       | GPMC0_AD6       | 0       |
| GPMC0_AD7      | GPMC0_AD7       | 0       | GPMC0_AD7       | 0       |
| GPMC0_AD8      | GPMC0_AD8       | 0       | GPMC0_AD8       | 0       |
| GPMC0_AD9      | GPMC0_AD9       | 0       | GPMC0_AD9       | 0       |
| GPMC0_AD10     | GPMC0_AD10      | 0       | GPMC0_AD10      | 0       |
| GPMC0_AD11     | GPMC0_AD11      | 0       | GPMC0_AD11      | 0       |
| GPMC0_AD12     | GPMC0_AD12      | 0       | GPMC0_AD12      | 0       |
| GPMC0_AD13     | GPMC0_AD13      | 0       | GPMC0_AD13      | 0       |
| GPMC0_AD14     | GPMC0_AD14      | 0       | GPMC0_AD14      | 0       |
| GPMC0_AD15     | GPMC0_AD15      | 0       | GPMC0_AD15      | 0       |
| GPMC0_CLK      | GPMC0_CLK       | 0       | GPMC0_CLK       | 0       |
| GPMC0_ADVn_ALE | GPMC0_ADVn_ALE  | 0       | GPMC0_ADVn_ALE  | 0       |
| GPMC0_OEn_REn  | GPMC0_OEn_REn   | 0       | GPMC0_OEn_REn   | 0       |
| GPMC0_WEn      | GPMC0_WEn       | 0       | GPMC0_WEn       | 0       |
| GPMC0_BE0n_CLE | GPMC0_BE0n_CLE  | 0       | GPMC0_BE0n_CLE  | 0       |
| GPMC0_BE1n     | GPMC0_BE1n      | 0       | GPMC0_BE1n      | 0       |
| GPMC0_WAIT0    | GPMC0_WAIT0     | 0       | GPMC0_WAIT0     | 0       |
| GPMC0_WAIT1    | GPMC0_WAIT1     | 0       | GPMC0_WAIT1     | 0       |
| GPMC0_WPn      | GPMC0_WPn       | 0       | GPMC0_WPn       | 0       |
| GPMC0_DIR      | GPMC0_DIR       | 0       | GPMC0_DIR       | 0       |
| GPMC0_CSn0     | GPMC0_CSn0      | 0       | GPMC0_CSn0      | 0       |
| GPMC0_CSn1     | GPMC0_CSn1      | 0       | GPMC0_CSn1      | 0       |
| GPMC0_CSn2     | GPMC0_CSn2      | 0       | GPMC0_CSn2      | 0       |
| GPMC0_CSn3     | GPMC0_CSn3      | 0       | GPMC0_CSn3      | 0       |
| GPMC0_AD16     | PRG1_PRU0_GPO0  | 8       | PRG1_PRU0_GPO0  | 8       |
| GPMC0_AD17     | PRG1_PRU0_GPO1  | 8       | PRG1_PRU0_GPO1  | 8       |
| GPMC0_AD18     | PRG1_PRU0_GPO2  | 8       | PRG1_PRU0_GPO2  | 8       |
| GPMC0_AD19     | PRG1_PRU0_GPO3  | 8       | PRG1_PRU0_GPO3  | 8       |
| GPMC0_AD20     | PRG1_PRU0_GPO4  | 8       | PRG1_PRU0_GPO4  | 8       |
| GPMC0_AD21     | PRG1_PRU0_GPO5  | 8       | PRG1_PRU0_GPO5  | 8       |
| GPMC0_AD22     | PRG1_PRU0_GPO6  | 8       | PRG1_PRU0_GPO6  | 8       |
| GPMC0_AD23     | PRG1_PRU0_GPO7  | 8       | PRG1_PRU0_GPO7  | 8       |
| GPMC0_AD24     | PRG1_PRU0_GPO8  | 8       | PRG1_PRU0_GPO8  | 8       |
| GPMC0_AD25     | PRG1_PRU0_GPO9  | 8       | PRG1_PRU0_GPO9  | 8       |
| GPMC0_AD26     | PRG1_PRU0_GPO10 | 8       | PRG1_PRU0_GPO10 | 8       |

表 6-60. GPMC0 IOSETs (続き)

| SIGNALS    | IOSET1                  |         | IOSET2                  |         |
|------------|-------------------------|---------|-------------------------|---------|
|            | BALL NAME               | MUXMODE | BALL NAME               | MUXMODE |
| GPMC0_AD27 | PRG1_PRU0_GPO11         | 8       | PRG1_PRU0_GPO11         | 8       |
| GPMC0_AD28 | PRG1_PRU0_GPO12         | 8       | PRG1_PRU0_GPO12         | 8       |
| GPMC0_AD29 | PRG1_PRU0_GPO13         | 8       | PRG1_PRU0_GPO13         | 8       |
| GPMC0_AD30 | PRG1_PRU0_GPO14         | 8       | PRG1_PRU0_GPO14         | 8       |
| GPMC0_AD31 | PRG1_PRU0_GPO15         | 8       | PRG1_PRU0_GPO15         | 8       |
| GPMC0_BE2n | PRG1_PRU0_GPO16         | 8       | PRG1_PRU0_GPO16         | 8       |
| GPMC0_A0   | PRG1_PRU0_GPO17         | 8       | PRG0_PRU0_GPO2          | 9       |
| GPMC0_A1   | PRG1_PRU0_GPO18         | 8       | PRG0_PRU0_GPO4          | 9       |
| GPMC0_A2   | PRG1_PRU0_GPO19         | 8       | PRG0_PRU0_GPO8          | 9       |
| GPMC0_A3   | PRG1_PRU1_GPO0          | 8       | PRG0_PRU0_GPO14         | 9       |
| GPMC0_A4   | PRG1_PRU1_GPO1          | 8       | PRG0_PRU0_GPO16         | 9       |
| GPMC0_A5   | PRG1_PRU1_GPO2          | 8       | PRG0_PRU0_GPO18         | 9       |
| GPMC0_A6   | PRG1_PRU1_GPO3          | 8       | PRG0_PRU0_GPO19         | 9       |
| GPMC0_A7   | PRG1_PRU1_GPO4          | 8       | PRG0_PRU1_GPO12         | 9       |
| GPMC0_A8   | PRG1_PRU1_GPO5          | 8       | PRG0_PRU1_GPO13         | 9       |
| GPMC0_A9   | PRG1_PRU1_GPO6          | 8       | PRG0_PRU1_GPO14         | 9       |
| GPMC0_A10  | PRG1_PRU1_GPO7          | 8       | PRG0_PRU1_GPO15         | 9       |
| GPMC0_A11  | PRG1_PRU1_GPO8          | 8       | PRG0_PRU1_GPO16         | 9       |
| GPMC0_A12  | PRG1_PRU1_GPO9          | 8       | PRG0_MDIO0_MDIO         | 9       |
| GPMC0_A13  | PRG1_PRU1_GPO10         | 8       | PRG0_MDIO0_MDC          | 9       |
| GPMC0_A14  | PRG1_PRU1_GPO11         | 8       | PRG0_PRU0_GPO12         | 9       |
| GPMC0_A15  | PRG1_PRU1_GPO12         | 8       | PRG0_PRU0_GPO13         | 9       |
| GPMC0_A16  | PRG1_PRU1_GPO13         | 8       | PRG0_PRU0_GPO15         | 9       |
| GPMC0_A17  | PRG1_PRU1_GPO14         | 8       | PRG0_PRU0_GPO17         | 9       |
| GPMC0_A18  | PRG1_PRU1_GPO15         | 8       | PRG0_PRU1_GPO3          | 9       |
| GPMC0_A19  | PRG1_PRU1_GPO16         | 8       | PRG0_PRU1_GPO6          | 9       |
| GPMC0_BE3n | PRG1_PRU1_GPO17         | 8       | PRG1_PRU1_GPO17         | 8       |
| GPMC0_A20  | GPMC0_CS <sub>n</sub> 3 | 4       | GPMC0_CS <sub>n</sub> 3 | 4       |
| GPMC0_A21  | GPMC0_WAIT1             | 4       | GPMC0_WAIT1             | 4       |
| GPMC0_A22  | GPMC0_WP <sub>n</sub>   | 4       | GPMC0_WP <sub>n</sub>   | 4       |

#### 6.10.5.9 I2C

The device contains six multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I<sup>2</sup>C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- MCU\_I2C1, I2C1, I2C2, and I2C3
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5 \text{ V})$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.
- MCU\_I2C0 and I2C0
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Hs-mode (up to 3.4 Mbit/s)
      - 1.8 V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3 V. So Hs-mode is limited to 1.8-V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8 V/ns (or 8E+7 V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.8 V/ns.
    - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5 \text{ V})$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

### 6.10.5.10 MCAN

表 6-61 and 表 6-62 presents timing conditions and switching characteristics for MCAN.

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 注

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

**表 6-61. MCAN Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 2   | 15  | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 5   | 20  | pF   |

**表 6-62. MCAN Switching Characteristics**

| NO.   | PARAMETER                | DESCRIPTION                                     | MIN | MAX | UNIT |
|-------|--------------------------|-------------------------------------------------|-----|-----|------|
| MCAN1 | t <sub>d</sub> (MCAN_TX) | Delay time, transmit shift register to MCANn_TX |     | 10  | ns   |
| MCAN2 | t <sub>d</sub> (MCAN_RX) | Delay time, MCANn_RX to receive shift register  |     | 10  | ns   |

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.11 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-63 presents timing conditions for MCSPI.

**表 6-63. MCSPI Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 2   | 8.5 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 6   | 12  | pF   |

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

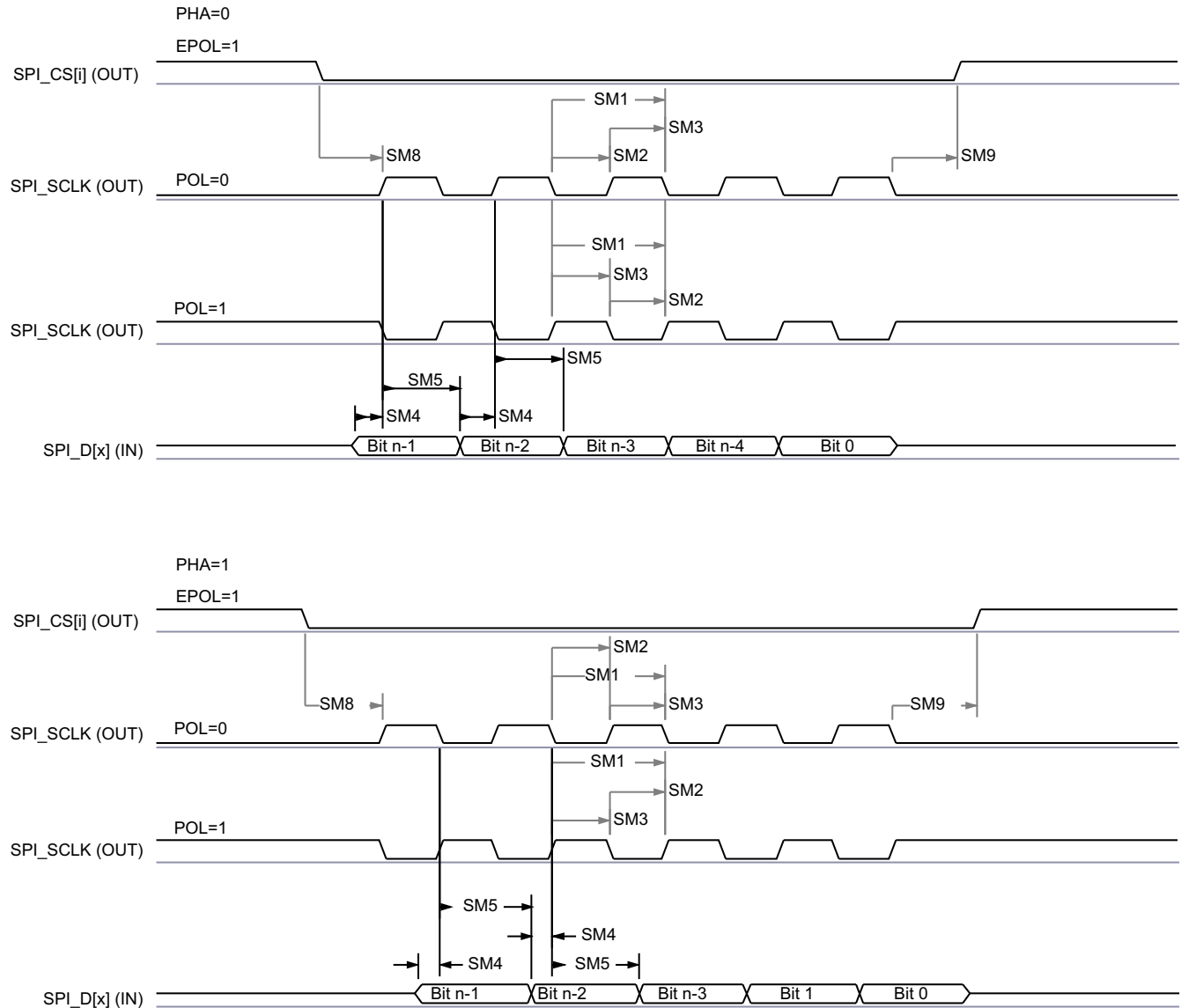
#### 6.10.5.11.1 MCSPI — Controller Mode

表 6-64, 図 6-54, 表 6-65, and 図 6-55 present timing requirements and switching characteristics for SPI – Controller Mode.

**表 6-64. MCSPI Timing Requirements – Controller Mode**

see 図 6-54

| NO. | PARAMETER             | DESCRIPTION                                             | MIN | MAX | UNIT |
|-----|-----------------------|---------------------------------------------------------|-----|-----|------|
| SM4 | $t_{su}(POCI-SPICLK)$ | Setup time, SPIn_D[x] valid before SPIn_CLK active edge | 2.8 |     | ns   |
| SM5 | $t_h(SPICLK-POCI)$    | Hold time, SPIn_D[x] valid after SPIn_CLK active edge   | 3   |     | ns   |



SPRSP08\_TIMING\_McSPI\_02

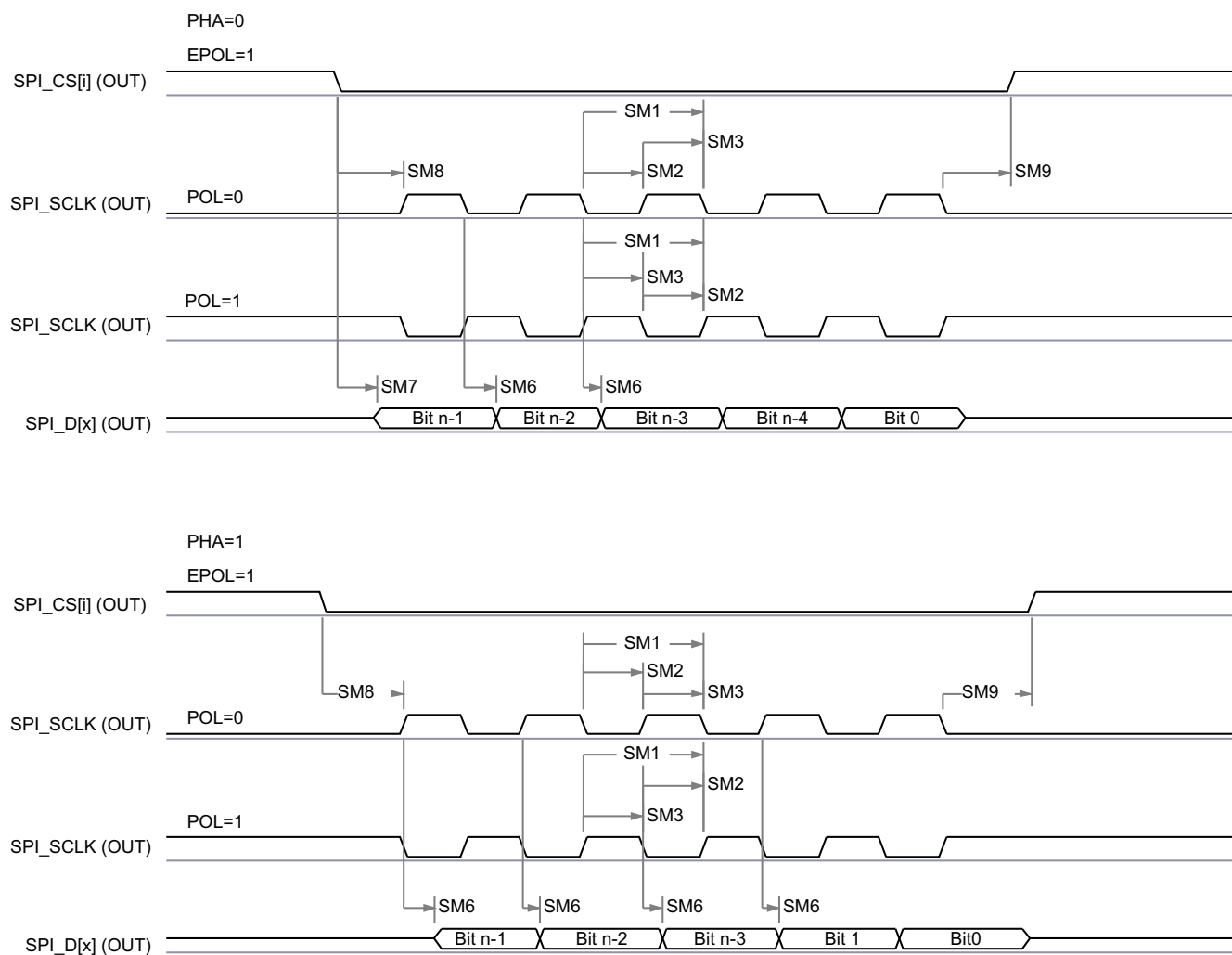
**図 6-54. MCSPI Controller Mode Receive Timing**

**表 6-65. MCSPI Switching Characteristics - Controller Mode**

see  6-55

| NO. | PARAMETER            |                                                     | MIN              | MAX                  | UNIT |
|-----|----------------------|-----------------------------------------------------|------------------|----------------------|------|
| SM1 | $t_{c(SPICLK)}$      | Cycle time, SPIn_CLK                                | 20               |                      | ns   |
| SM2 | $t_{w(SPICLK_L)}$    | Pulse duration, SPIn_CLK low                        | $0.5P - 1^{(1)}$ |                      | ns   |
| SM3 | $t_{w(SPICLK_H)}$    | Pulse duration, SPIn_CLK high                       | $0.5P - 1^{(1)}$ |                      | ns   |
| SM6 | $t_{d(SPICLK-PICO)}$ | Delay time, SPIn_CLK active edge to SPIn_D[x]       | -3               | 2.5                  | ns   |
| SM7 | $t_{d(CS-PICO)}$     | Delay time, SPIn_CSi active edge to SPIn_D[x]       | 5                |                      | ns   |
| SM8 | $t_{d(CS-SPICLK)}$   | Delay time, SPIn_CSi active to SPIn_CLK first edge  | PHA = 0          | B - 4 <sup>(2)</sup> | ns   |
|     |                      |                                                     | PHA = 1          | A - 4 <sup>(3)</sup> | ns   |
| SM9 | $t_{d(SPICLK-CS)}$   | Delay time, SPIn_CLK last edge to SPIn_CSi inactive | PHA = 0          | A - 4 <sup>(4)</sup> | ns   |
|     |                      |                                                     | PHA = 1          | B - 4 <sup>(5)</sup> | ns   |

- (1) P = SPI\_CLK period in ns.
- (2) T<sub>ref</sub> is the period of the McSPI functional clock in ns. Fratio is the divide ratio of McSPI functional clock frequency to SPIn\_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI\_CH(i)CONF register and the EXTCLK bit field in the MSPI\_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI\_CH(i)CONF register.
  - When Fratio = 1; B = (TCS(i) + 0.5) \* T<sub>ref</sub>.
  - When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) \* Fratio \* T<sub>ref</sub>.
  - When Fratio ≥ 3 and odd value; B = ((TCS(i) \* Fratio) + ((Fratio + 1) / 2)) \* T<sub>ref</sub>.
- (3) T<sub>ref</sub> is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn\_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI\_CH(i)CONF register and the EXTCLK bit field in the MSPI\_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI\_CH(i)CONF register.
  - When Fratio = 1; A = (TCS(i) + 1) \* T<sub>ref</sub>.
  - When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) \* Fratio \* T<sub>ref</sub>.
  - When Fratio ≥ 3 and odd value; A = ((TCS(i) \* Fratio) + ((Fratio - 1) / 2)) \* T<sub>ref</sub>.
- (4) T<sub>ref</sub> is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn\_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI\_CH(i)CONF register and the EXTCLK bit field in the MSPI\_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI\_CH(i)CONF register.
  - When Fratio = 1; A = (TCS(i) + 1) \* T<sub>ref</sub>.
  - When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) \* Fratio \* T<sub>ref</sub>.
  - When Fratio ≥ 3 and odd value; A = ((TCS(i) \* Fratio) + ((Fratio + 1) / 2)) \* T<sub>ref</sub>.
- (5) T<sub>ref</sub> is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn\_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI\_CH(i)CONF register and the EXTCLK bit field in the MSPI\_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI\_CH(i)CONF register.
  - When Fratio = 1; B = (TCS(i) + 0.5) \* T<sub>ref</sub>.
  - When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) \* Fratio \* T<sub>ref</sub>.
  - When Fratio ≥ 3 and odd value; B = ((TCS(i) \* Fratio) + ((Fratio - 1) / 2)) \* T<sub>ref</sub>.



SPRSP08\_TIMING\_McSPI\_01


**6-55. MCSPI Controller Mode Transmit Timing**

### 6.10.5.11.2 MCSPI — Peripheral Mode

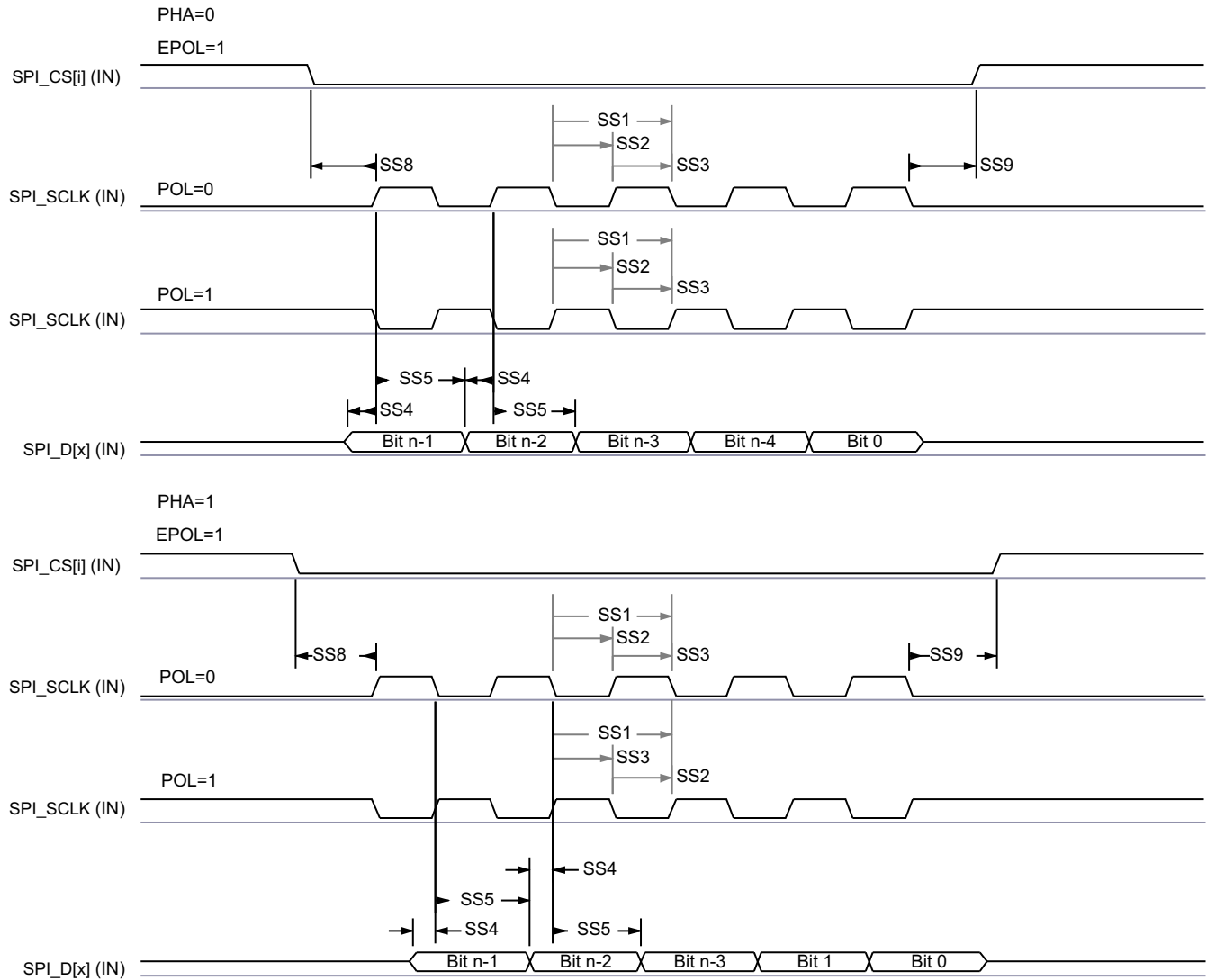
表 6-66, 図 6-56, 表 6-67, and 図 6-57 present timing requirements and switching characteristics for SPI – Peripheral Mode.

**表 6-66. MCSPI Timing Requirements – Peripheral Mode**

see 図 6-56

| NO. | PARAMETER             | DESCRIPTION                                             | MIN                  | MAX | UNIT |
|-----|-----------------------|---------------------------------------------------------|----------------------|-----|------|
| SS1 | $t_{c(SPICLK)}$       | Cycle time, SPIn_CLK                                    | 20                   |     | ns   |
| SS2 | $t_{w(SPICLK_L)}$     | Pulse duration, SPIn_CLK low                            | 0.45P <sup>(1)</sup> |     | ns   |
| SS3 | $t_{w(SPICLK_H)}$     | Pulse duration, SPIn_CLK high                           | 0.45P <sup>(1)</sup> |     | ns   |
| SS4 | $t_{su(PICO-SPICLK)}$ | Setup time, SPIn_D[x] valid before SPIn_CLK active edge | 5                    |     | ns   |
| SS5 | $t_{h(SPICLK-PICO)}$  | Hold time, SPIn_D[x] valid after SPIn_CLK active edge   | 5                    |     | ns   |
| SS8 | $t_{su(CS-SPICLK)}$   | Setup time, SPIn_CSi valid before SPIn_CLK first edge   | 5                    |     | ns   |
| SS9 | $t_{h(SPICLK-CS)}$    | Hold time, SPIn_CSi valid after SPIn_CLK last edge      | 5                    |     | ns   |

(1) P = SPIn\_CLK period in ns.



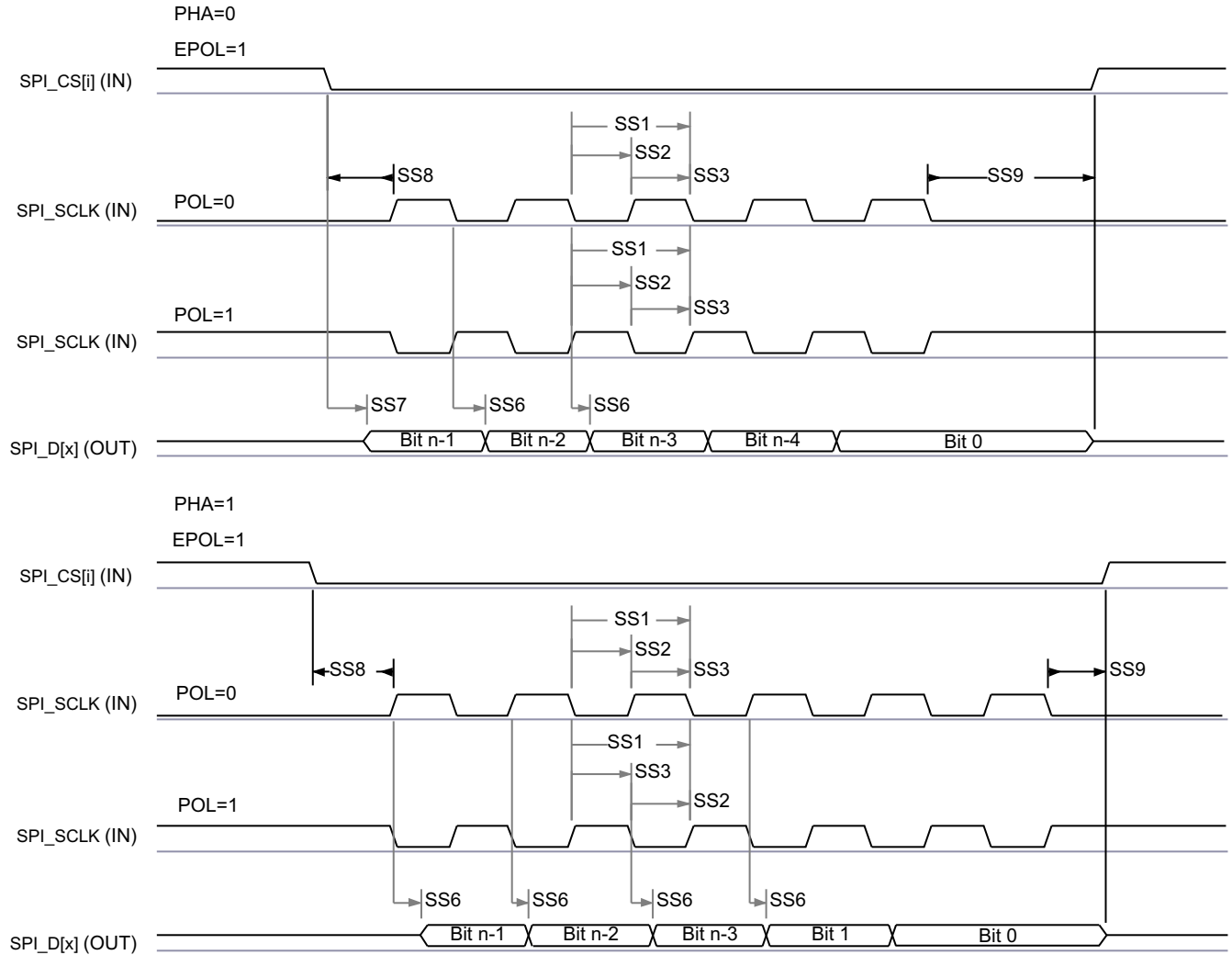
SPRSP08\_TIMING\_McSPI\_04


**6-56. SPI Peripheral Mode Receive Timing**

表 6-67. MCSPI Switching Characteristics – Peripheral Mode

see 図 6-57

| NO. | PARAMETER            | DESCRIPTION                                   | MIN   | MAX   | UNIT |
|-----|----------------------|-----------------------------------------------|-------|-------|------|
| SS6 | $t_{d(SPICLK-POCI)}$ | Delay time, SPIn_CLK active edge to SPIn_D[x] | 2     | 17.12 | ns   |
| SS7 | $t_{sk(CS-POCI)}$    | Delay time, SPIn_CSi active edge to SPIn_D[x] | 20.95 |       | ns   |



SPRSP08\_TIMING\_McSPI\_03

図 6-57. SPI Peripheral Mode Transmit Timing

### 6.10.5.12 MMCSd

The MMCSd Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSd Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSd interfaces, see the corresponding MMC0 and MMC1 subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 注

Some operating modes require software configuration of the MMC DLL delay settings, as shown in 表 6-68 and 表 6-77.

The modes which show a value of "Tuning" in the ITAPDLYSEL column of 表 6-68 and 表 6-77 require a tuning algorithm to be used for optimizing input timing. Refer to the MMCSd Programming Guide in the device TRM for more information on the tuning algorithm and configuration of input delays required to optimize input timing.

For more information, see *Multi-Media Card/Secure Digital (MMCSd) Interface* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.12.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and supports the following eMMC applications:

- Legacy speed
- High speed SDR
- High speed DDR
- HS200

表 6-68 presents the required DLL software configuration settings for MMC0 timing modes.

**表 6-68. MMC0 DLL Delay Mapping for all Timing Modes**

| REGISTER NAME        |                                          | MMCSd0_SS_PHY_CTRL_4_REG |                           |                          |                          |                         | MMCSd0_SS_PHY_CTRL_5_REG     |                      |                             |
|----------------------|------------------------------------------|--------------------------|---------------------------|--------------------------|--------------------------|-------------------------|------------------------------|----------------------|-----------------------------|
| BIT FIELD            |                                          | [31:24]                  | [20]                      | [15:12]                  | [8]                      | [4:0]                   | [17:16]                      | [10:8]               | [2:0]                       |
| BIT FIELD NAME       |                                          | STRBSEL                  | OTAPDLYENA                | OTAPDLYSEL               | ITAPDLYENA               | ITAPDLYSEL              | SELDLYTXCLK<br>SELDLYRXCLK   | FRQSEL               | CLKBUFSEL                   |
| MODE                 | DESCRIPTION                              | STROBE<br>DELAY          | OUTPUT<br>DELAY<br>ENABLE | OUTPUT<br>DELAY<br>VALUE | INPUT<br>DELAY<br>ENABLE | INPUT<br>DELAY<br>VALUE | DLL<br>DELAY CHAIN<br>SELECT | DLL REF<br>FREQUENCY | DELAY<br>BUFFER<br>DURATION |
| Legacy<br>SDR        | 8-bit PHY<br>operating 1.8 V,<br>25 MHz  | 0x0                      | 0x0                       | NA <sup>(1)</sup>        | 0x1                      | 0x10                    | 0x1                          | 0x0                  | 0x7                         |
| High<br>Speed<br>SDR | 8-bit PHY<br>operating 1.8 V,<br>50 MHz  | 0x0                      | 0x0                       | NA <sup>(1)</sup>        | 0x1                      | 0xA                     | 0x1                          | 0x0                  | 0x7                         |
| High<br>Speed<br>DDR | 8-bit PHY<br>operating 1.8 V,<br>50 MHz  | 0x0                      | 0x1                       | 0x6                      | 0x1                      | 0x3                     | 0x0                          | 0x4                  | 0x7                         |
| HS200                | 8-bit PHY<br>operating 1.8 V,<br>200 MHz | 0x0                      | 0x1                       | 0x7                      | 0x1                      | Tuning <sup>(2)</sup>   | 0x0                          | 0x0                  | 0x7                         |

(1) NA means Not Applicable

(2) Tuning means this mode requires a tuning algorithm to optimize input timing

表 6-69 presents timing conditions for MMC0.

**表 6-69. MMC0 Timing Conditions**

| PARAMETER                             |                                              |                               | MIN  | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|-------------------------------|------|------|------|
| INPUT CONDITIONS                      |                                              |                               |      |      |      |
| SR <sub>i</sub>                       | Input slew rate                              | Legacy SDR                    | 0.14 | 1.44 | V/ns |
|                                       |                                              | High Speed SDR                | 0.3  | 0.9  | V/ns |
|                                       |                                              | High Speed DDR (CMD)          | 0.3  | 0.9  | V/ns |
|                                       |                                              | High Speed DDR (DAT[7:0])     | 0.45 | 0.9  | V/ns |
| OUTPUT CONDITIONS                     |                                              |                               |      |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | Legacy SDR                    | 1    | 12   | pF   |
|                                       |                                              | High Speed SDR                | 1    | 12   | pF   |
|                                       |                                              | High Speed DDR                | 1    | 12   | pF   |
|                                       |                                              | HS200                         | 1    | 6    | pF   |
|                                       |                                              | PCB CONNECTIVITY REQUIREMENTS |      |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | All modes                     | 126  | 756  | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | Legacy SDR, High Speed SDR    |      | 100  | ps   |
|                                       |                                              | High Speed DDR, HS200         |      | 8    | ps   |

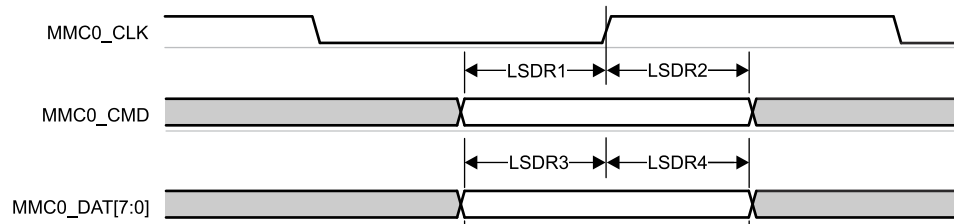
### 6.10.5.12.1.1 Legacy SDR Mode

表 6-70, 図 6-58, 表 6-71, and 図 6-59 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

**表 6-70. MMC0 Timing Requirements – Legacy SDR Mode**

see 図 6-58

| NO.   |                     |                                                             | MIN  | MAX | UNIT |
|-------|---------------------|-------------------------------------------------------------|------|-----|------|
| LSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 1.56 |     | ns   |
| LSDR2 | $t_h(clkH-cmdV)$    | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 5.44 |     | ns   |
| LSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 1.56 |     | ns   |
| LSDR4 | $t_h(clkH-dV)$      | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 5.44 |     | ns   |

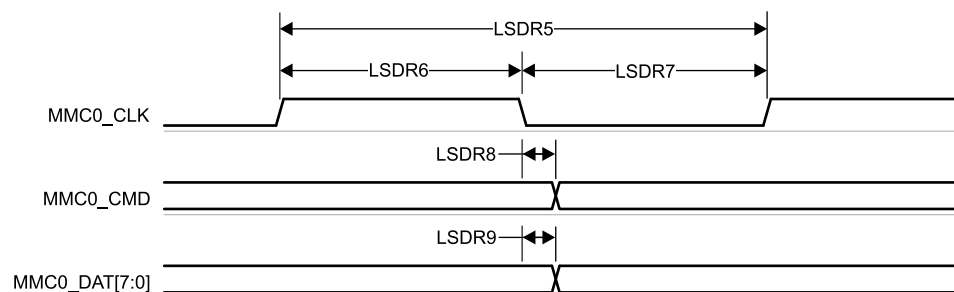


**図 6-58. MMC0 – Legacy SDR – Receive Mode**

**表 6-71. MMC0 Switching Characteristics – Legacy SDR Mode**

see 図 6-59

| NO.   |                  | PARAMETER                                                     | MIN  | MAX | UNIT |
|-------|------------------|---------------------------------------------------------------|------|-----|------|
|       | $f_{op(clk)}$    | Operating frequency, MMC0_CLK                                 |      | 25  | MHz  |
| LSDR5 | $t_c(clk)$       | Cycle time, MMC0_CLK                                          | 40   |     | ns   |
| LSDR6 | $t_w(clkH)$      | Pulse duration, MMC0_CLK high                                 | 18.7 |     | ns   |
| LSDR7 | $t_w(clkL)$      | Pulse duration, MMC0_CLK low                                  | 18.7 |     | ns   |
| LSDR8 | $t_d(clkL-cmdV)$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | -2.3 | 2.9 | ns   |
| LSDR9 | $t_d(clkL-dV)$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | -2.3 | 2.9 | ns   |



**図 6-59. MMC0 – Legacy SDR – Transmit Mode**

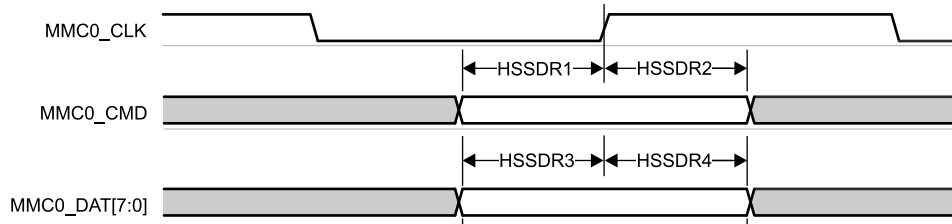
#### 6.10.5.12.1.2 High Speed SDR Mode

表 6-72, 図 6-60, 表 6-73, and 図 6-61 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

**表 6-72. MMC0 Timing Requirements – High Speed SDR Mode**

see 図 6-60

| NO.    |                     |                                                             | MIN  | MAX | UNIT |
|--------|---------------------|-------------------------------------------------------------|------|-----|------|
| HSSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 2.55 |     | ns   |
| HSSDR2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 2.67 |     | ns   |
| HSSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 2.55 |     | ns   |
| HSSDR4 | $t_{h(clkH-dV)}$    | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 2.67 |     | ns   |

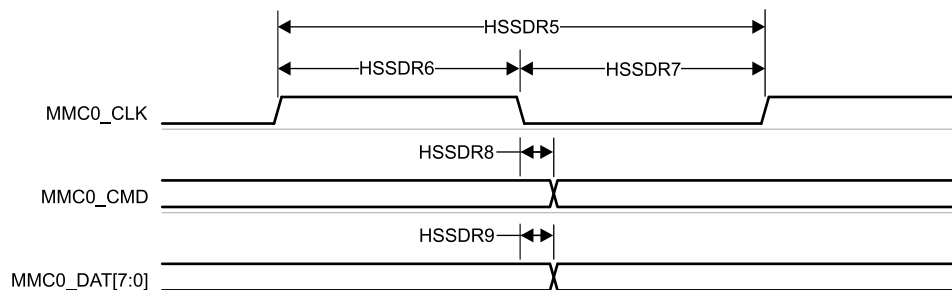


**図 6-60. MMC0 – High Speed SDR Mode – Receive Mode**

**表 6-73. MMC0 Switching Characteristics – High Speed SDR Mode**

see 図 6-61

| NO.    |                    | PARAMETER                                                     | MIN  | MAX | UNIT |
|--------|--------------------|---------------------------------------------------------------|------|-----|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC0_CLK                                 |      | 50  | MHz  |
| HSSDR5 | $t_{c(clk)}$       | Cycle time, MMC0_CLK                                          | 20   |     | ns   |
| HSSDR6 | $t_{w(clkH)}$      | Pulse duration, MMC0_CLK high                                 | 9.2  |     | ns   |
| HSSDR7 | $t_{w(clkL)}$      | Pulse duration, MMC0_CLK low                                  | 9.2  |     | ns   |
| HSSDR8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | -2.3 | 2.9 | ns   |
| HSSDR9 | $t_{d(clkL-dV)}$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | -2.3 | 2.9 | ns   |



**図 6-61. MMC0 – High Speed SDR Mode – Transmit Mode**

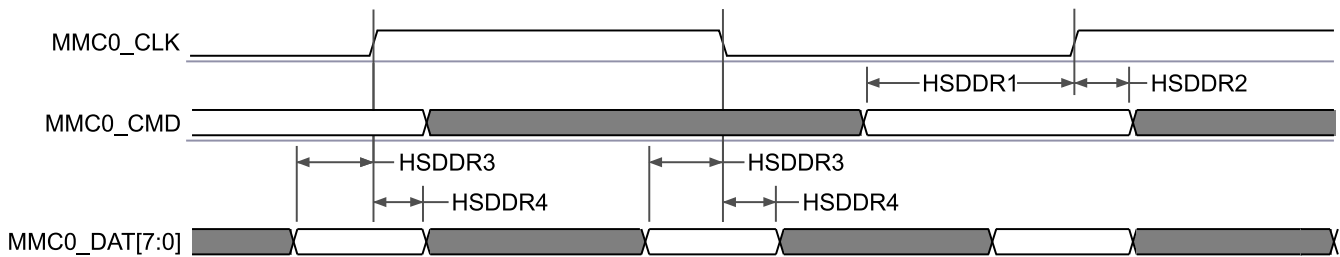
### 6.10.5.12.1.3 High Speed DDR Mode

表 6-74, 図 6-62, 表 6-75, and 図 6-63 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

**表 6-74. MMC0 Timing Requirements – High Speed DDR Mode**

see 図 6-62

| NO.    |                    |                                                            | MIN  | MAX | UNIT |
|--------|--------------------|------------------------------------------------------------|------|-----|------|
| HSDDR1 | $t_{su(cmdV-clk)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge     | 1.62 |     | ns   |
| HSDDR2 | $t_{h(clk-cmdV)}$  | Hold time, MMC0_CMD valid after MMC0_CLK rising edge       | 2.52 |     | ns   |
| HSDDR3 | $t_{su(dV-clk)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition | 0.83 |     | ns   |
| HSDDR4 | $t_{h(clk-dV)}$    | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition   | 1.76 |     | ns   |

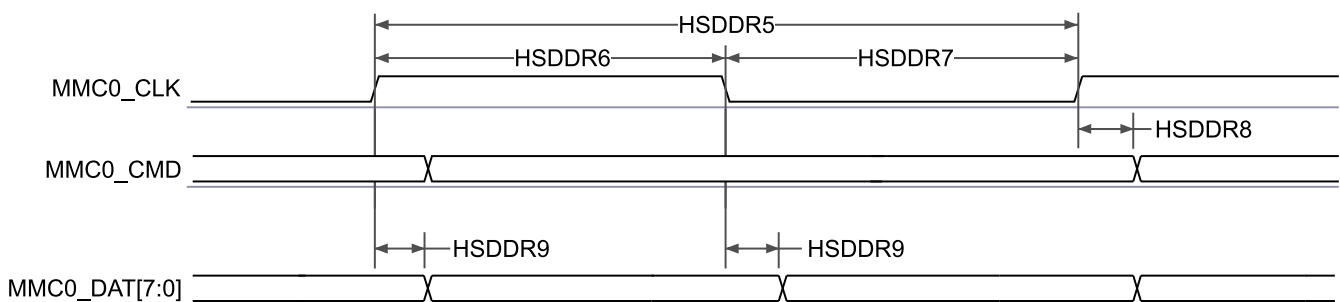


**図 6-62. MMC0 – High Speed DDR Mode – Receive Mode**

**表 6-75. MMC0 Switching Characteristics – High Speed DDR Mode**

see 図 6-63

| NO.    |                   | PARAMETER                                                   | MIN  | MAX  | UNIT |
|--------|-------------------|-------------------------------------------------------------|------|------|------|
|        | $f_{op(clk)}$     | Operating frequency, MMC0_CLK                               |      | 50   | MHz  |
| HSDDR5 | $t_{c(clk)}$      | Cycle time, MMC0_CLK                                        | 20   |      | ns   |
| HSDDR6 | $t_{w(clkH)}$     | Pulse duration, MMC0_CLK high                               | 9.2  |      | ns   |
| HSDDR7 | $t_{w(clkL)}$     | Pulse duration, MMC0_CLK low                                | 9.2  |      | ns   |
| HSDDR8 | $t_{d(clk-cmdV)}$ | Delay time, MMC0_CLK rising edge to MMC0_CMD transition     | 3.31 | 7.65 | ns   |
| HSDDR9 | $t_{d(clk-dV)}$   | Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition | 2.81 | 6.94 | ns   |



**図 6-63. MMC0 – High Speed DDR Mode – Transmit Mode**

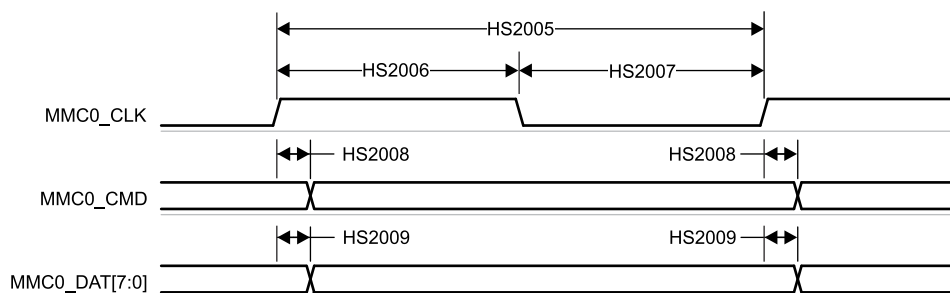
#### 6.10.5.12.1.4 HS200 Mode

表 6-76 and 図 6-64 present switching characteristics for MMC0 – HS200 Mode.

**表 6-76. MMC0 Switching Characteristics – HS200 Mode**

see 図 6-64

| NO.    | PARAMETER          |                                                              | MIN  | MAX  | UNIT |
|--------|--------------------|--------------------------------------------------------------|------|------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC0_CLK                                |      | 200  | MHz  |
| HS2005 | $t_{c(clk)}$       | Cycle time, MMC0_CLK                                         | 5    |      | ns   |
| HS2006 | $t_{w(clkH)}$      | Pulse duration, MMC0_CLK high                                | 2.08 |      | ns   |
| HS2007 | $t_{w(clkL)}$      | Pulse duration, MMC0_CLK low                                 | 2.08 |      | ns   |
| HS2008 | $t_{d(clkL-cmdV)}$ | Delay time, MMC0_CLK rising edge to MMC0_CMD transition      | 0.99 | 3.28 | ns   |
| HS2009 | $t_{d(clkL-dV)}$   | Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition | 0.99 | 3.28 | ns   |



**図 6-64. MMC0 – HS200 Mode – Transmit Mode**

### 6.10.5.12.2 MMC1 - SD/SDIO Interface

MMC1 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS-I SDR12
- UHS-I SDR25
- UHS-I SDR50
- UHS-I SDR104
- UHS-I DDR50

表 6-77 presents the required DLL software configuration settings for MMC1 timing modes.

**表 6-77. MMC1 DLL Delay Mapping for all Timing Modes**

| REGISTER NAME  |                                    | MMCSD1_SS_PHY_CTRL_4_REG |                |                          |                         | MMCSD1_SS_PHY_CTRL_5_REG    |
|----------------|------------------------------------|--------------------------|----------------|--------------------------|-------------------------|-----------------------------|
| BIT FIELD      |                                    | [20]                     | [15:12]        | [8]                      | [4:0]                   | [2:0]                       |
| BIT FIELD NAME |                                    | OTAPDLYENA               | OTAPDLYSEL     | ITAPDLYENA               | ITAPDLYSEL              | CLKBUFSEL                   |
| MODE           | DESCRIPTION                        | DELAY<br>ENABLE          | DELAY<br>VALUE | INPUT<br>DELAY<br>ENABLE | INPUT<br>DELAY<br>VALUE | DELAY<br>BUFFER<br>DURATION |
| Default Speed  | 4-bit PHY operating 3.3 V, 25 MHz  | 0x1                      | 0x0            | 0x1                      | 0x0                     | 0x7                         |
| High Speed     | 4-bit PHY operating 3.3 V, 50 MHz  | 0x1                      | 0x0            | 0x1                      | 0x0                     | 0x7                         |
| UHS-I SDR12    | 4-bit PHY operating 1.8 V, 25 MHz  | 0x1                      | 0xF            | 0x1                      | 0x0                     | 0x7                         |
| UHS-I SDR25    | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                      | 0xF            | 0x1                      | 0x0                     | 0x7                         |
| UHS-I SDR50    | 4-bit PHY operating 1.8 V, 100 MHz | 0x1                      | 0xC            | 0x1                      | Tuning <sup>(1)</sup>   | 0x7                         |
| UHS-I DDR50    | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                      | 0x9            | 0x1                      | Tuning <sup>(1)</sup>   | 0x7                         |
| UHS-I SDR104   | 4-bit PHY operating 1.8 V, 200 MHz | 0x1                      | 0x6            | 0x1                      | Tuning <sup>(1)</sup>   | 0x7                         |

(1) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

表 6-78 presents timing conditions for MMC1.

**表 6-78. MMC1 Timing Conditions**

| PARAMETER                             |                                              |                           | MIN  | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|---------------------------|------|------|------|
| Input Conditions                      |                                              |                           |      |      |      |
| SR <sub>I</sub>                       | Input slew rate                              | Default Speed, High Speed | 0.69 | 2.06 | V/ns |
|                                       |                                              | UHS-I SDR12, UHS-I SDR25  | 0.34 | 1.34 | V/ns |
|                                       |                                              | UHS-I DDR50               | 1    | 2    | V/ns |
| Output Conditions                     |                                              |                           |      |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | UHS-I DDR50               | 3    | 10   | pF   |
|                                       |                                              | All other modes           | 1    | 10   | pF   |
| PCB Connectivity Requirements         |                                              |                           |      |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | UHS-I DDR50               | 240  | 1134 | ps   |
|                                       |                                              | All other modes           | 126  | 1386 | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | UHS-I DDR50, UHS-I SDR104 |      | 20   | ps   |
|                                       |                                              | All other modes           |      | 100  | ps   |

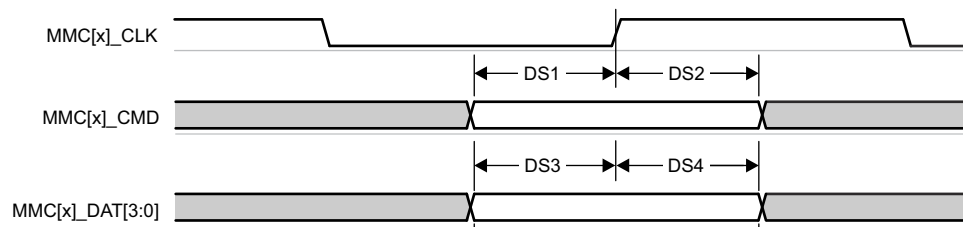
#### 6.10.5.12.2.1 Default Speed Mode

表 6-79, 図 6-65, 表 6-80, and 図 6-66 present timing requirements and switching characteristics for MMC1 – Default Speed Mode.

**表 6-79. Timing Requirements for MMC1 – Default Speed Mode**

see 図 6-65

| NO. |                     |                                                             | MIN  | MAX | UNIT |
|-----|---------------------|-------------------------------------------------------------|------|-----|------|
| DS1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC1_CMD valid before MMCi_CLK rising edge      | 2.15 |     | ns   |
| DS2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC1_CMD valid after MMC1_CLK rising edge        | 1.67 |     | ns   |
| DS3 | $t_{su(dV-clkH)}$   | Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge | 2.15 |     | ns   |
| DS4 | $t_{h(clkH-dV)}$    | Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge   | 1.67 |     | ns   |

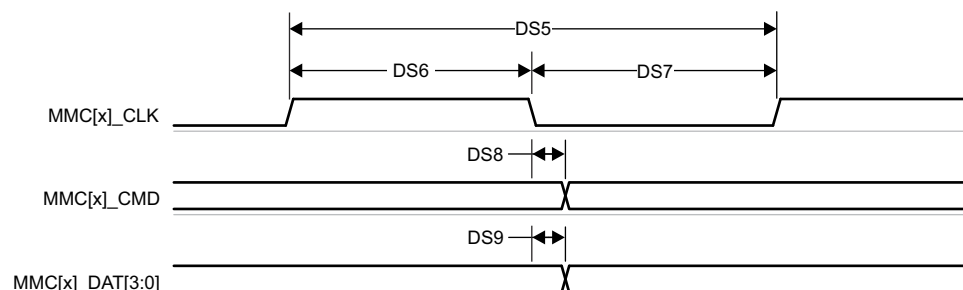


**図 6-65. MMC1 – Default Speed – Receive Mode**

**表 6-80. Switching Characteristics for MMC1 – Default Speed Mode**

see 図 6-66

| NO. |                    | PARAMETER                                                     | MIN  | MAX | UNIT |
|-----|--------------------|---------------------------------------------------------------|------|-----|------|
|     | $f_{op(clk)}$      | Operating frequency, MMC1_CLK                                 |      | 25  | MHz  |
| DS5 | $t_{c(clk)}$       | Cycle time, MMC1_CLK                                          | 40   |     | ns   |
| DS6 | $t_{w(clkH)}$      | Pulse duration, MMC1_CLK high                                 | 18.7 |     | ns   |
| DS7 | $t_{w(clkL)}$      | Pulse duration, MMC1_CLK low                                  | 18.7 |     | ns   |
| DS8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC1_CLK falling edge to MMC1_CMD transition      | -1.8 | 1.8 | ns   |
| DS9 | $t_{d(clkL-dV)}$   | Delay time, MMC1_CLK falling edge to MMC1_DAT[3:0] transition | -1.8 | 1.8 | ns   |



**図 6-66. MMC1 – Default Speed – Transmit Mode**

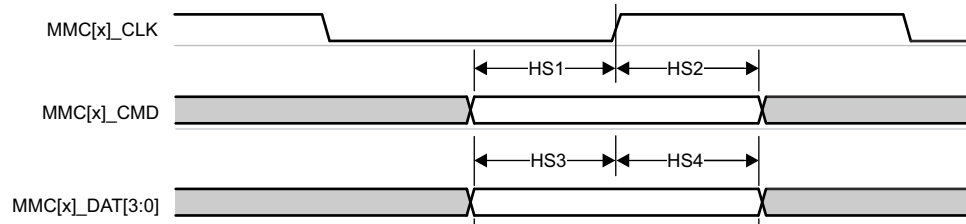
#### 6.10.5.12.2.2 High Speed Mode

表 6-81, 図 6-67, 表 6-82, and 図 6-68 present timing requirements and switching characteristics for MMC1 – High Speed Mode.

**表 6-81. Timing Requirements for MMC1 – High Speed Mode**

see 図 6-67

| NO. |                     |                                                             | MIN  | MAX | UNIT |
|-----|---------------------|-------------------------------------------------------------|------|-----|------|
| HS1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC1_CMD valid before MMC1_CLK rising edge      | 2.15 |     | ns   |
| HS2 | $t_h(clkH-cmdV)$    | Hold time, MMC1_CMD valid after MMC1_CLK rising edge        | 1.67 |     | ns   |
| HS3 | $t_{su(dV-clkH)}$   | Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge | 2.15 |     | ns   |
| HS4 | $t_h(clkH-dV)$      | Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge   | 1.67 |     | ns   |

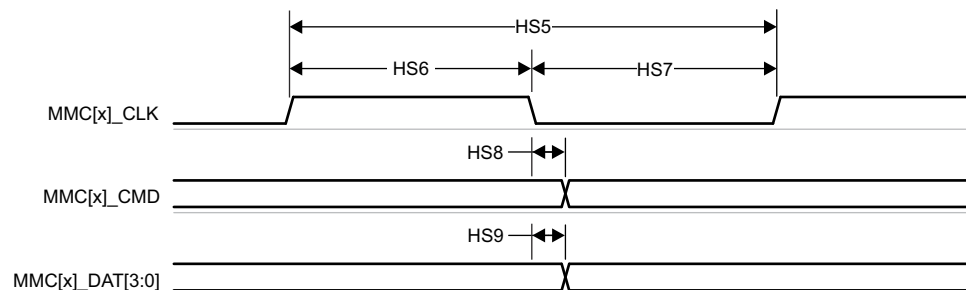


**図 6-67. MMC1 – High Speed – Receive Mode**

**表 6-82. Switching Characteristics for MMC1 – High Speed Mode**

see 図 6-68

| NO. |                  | PARAMETER                                                     | MIN  | MAX | UNIT |
|-----|------------------|---------------------------------------------------------------|------|-----|------|
|     | $f_{op(clk)}$    | Operating frequency, MMC1_CLK                                 |      | 50  | MHz  |
| HS5 | $t_c(clk)$       | Cycle time, MMC1_CLK                                          | 20   |     | ns   |
| HS6 | $t_w(clkH)$      | Pulse duration, MMC1_CLK high                                 | 9.2  |     | ns   |
| HS7 | $t_w(clkL)$      | Pulse duration, MMC1_CLK low                                  | 9.2  |     | ns   |
| HS8 | $t_d(clkL-cmdV)$ | Delay time, MMC1_CLK falling edge to MMC1_CMD transition      | -1.8 | 1.8 | ns   |
| HS9 | $t_d(clkL-dV)$   | Delay time, MMC1_CLK falling edge to MMC1_DAT[3:0] transition | -1.8 | 1.8 | ns   |



**図 6-68. MMC1 – High Speed – Transmit Mode**

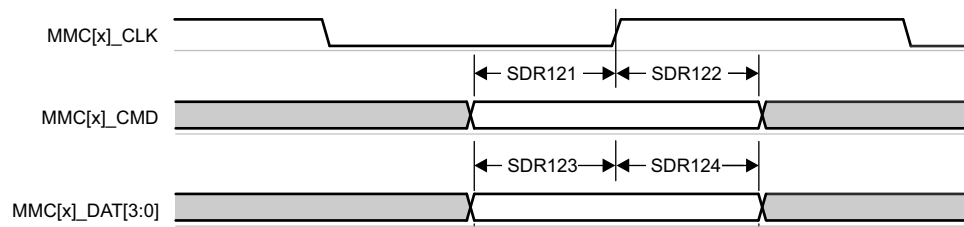
### 6.10.5.12.2.3 UHS-I SDR12 Mode

表 6-83, 図 6-69, 表 6-84, and 図 6-70 present timing requirements and switching characteristics for MMC1 – UHS-I SDR12 Mode.

**表 6-83. Timing Requirements for MMC1 – UHS-I SDR12 Mode**

see 図 6-69

| NO.    |                     |                                                             | MIN  | MAX | UNIT |
|--------|---------------------|-------------------------------------------------------------|------|-----|------|
| SDR121 | $t_{su(cmdV-clkH)}$ | Setup time, MMC1_CMD valid before MMC1_CLK rising edge      | 2.35 |     | ns   |
| SDR122 | $t_{h(clkH-cmdV)}$  | Hold time, MMC1_CMD valid after MMC1_CLK rising edge        | 1.67 |     | ns   |
| SDR123 | $t_{su(dV-clkH)}$   | Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge | 2.35 |     | ns   |
| SDR124 | $t_{h(clkH-dV)}$    | Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge   | 1.67 |     | ns   |

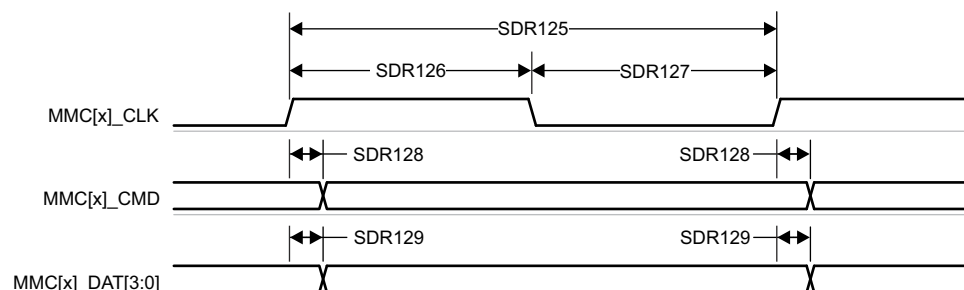


**図 6-69. MMC1 – UHS-I SDR12 – Receive Mode**

**表 6-84. Switching Characteristics for MMC1 – UHS-I SDR12 Mode**

see 図 6-70

| NO.    |                    | PARAMETER                                                    | MIN  | MAX | UNIT |
|--------|--------------------|--------------------------------------------------------------|------|-----|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC1_CLK                                |      | 25  | MHz  |
| SDR125 | $t_{c(clk)}$       | Cycle time, MMC1_CLK                                         | 40   |     | ns   |
| SDR126 | $t_{w(clkH)}$      | Pulse duration, MMC1_CLK high                                | 18.7 |     | ns   |
| SDR127 | $t_{w(clkL)}$      | Pulse duration, MMC1_CLK low                                 | 18.7 |     | ns   |
| SDR128 | $t_{d(clkL-cmdV)}$ | Delay time, MMC1_CLK rising edge to MMC1_CMD transition      | 1.2  | 8   | ns   |
| SDR129 | $t_{d(clkL-dV)}$   | Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition | 1.2  | 8   | ns   |



**図 6-70. MMC1 – UHS-I SDR12 – Transmit Mode**

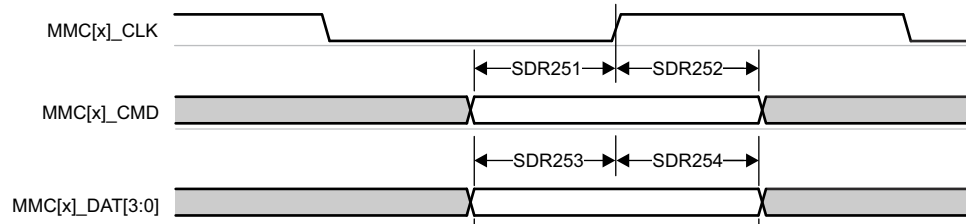
#### 6.10.5.12.2.4 UHS-I SDR25 Mode

表 6-85, 図 6-71, 表 6-86, and 図 6-72 present timing requirements and switching characteristics for MMC1 – UHS-I SDR25 Mode.

**表 6-85. Timing Requirements for MMC1 – UHS-I SDR25 Mode**

see 図 6-71

| NO.    |                     |                                                             | MIN  | MAX | UNIT |
|--------|---------------------|-------------------------------------------------------------|------|-----|------|
| SDR251 | $t_{su(cmdV-clkH)}$ | Setup time, MMC1_CMD valid before MMC1_CLK rising edge      | 1.95 |     | ns   |
| SDR252 | $t_{h(clkH-cmdV)}$  | Hold time, MMC1_CMD valid after MMC1_CLK rising edge        | 1.67 |     | ns   |
| SDR253 | $t_{su(dV-clkH)}$   | Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge | 1.95 |     | ns   |
| SDR254 | $t_{h(clkH-dV)}$    | Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge   | 1.67 |     | ns   |

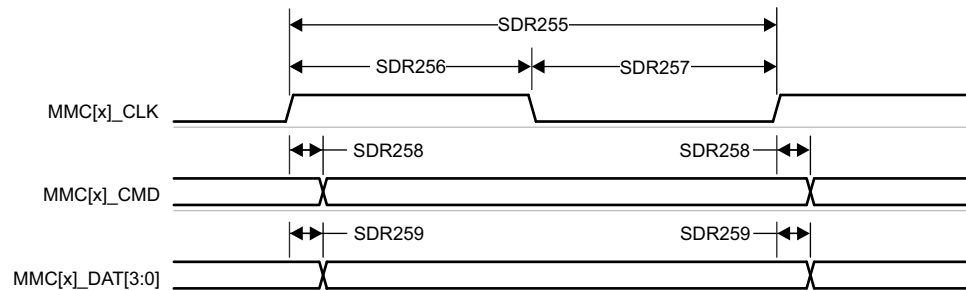


**図 6-71. MMC1 – UHS-I SDR25 – Receive Mode**

**表 6-86. Switching Characteristics for MMC1 – UHS-I SDR25 Mode**

see 図 6-72

| NO.    |                    | PARAMETER                                                    | MIN | MAX | UNIT |
|--------|--------------------|--------------------------------------------------------------|-----|-----|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC1_CLK                                |     | 50  | MHz  |
| SDR255 | $t_{c(clk)}$       | Cycle time, MMC1_CLK                                         | 20  |     | ns   |
| SDR256 | $t_{w(clkH)}$      | Pulse duration, MMC1_CLK high                                | 9.2 |     | ns   |
| SDR257 | $t_{w(clkL)}$      | Pulse duration, MMC1_CLK low                                 | 9.2 |     | ns   |
| SDR258 | $t_{d(clkL-cmdV)}$ | Delay time, MMC1_CLK rising edge to MMC1_CMD transition      | 2.4 | 8   | ns   |
| SDR259 | $t_{d(clkL-dV)}$   | Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition | 2.4 | 8   | ns   |



**図 6-72. MMC1 – UHS-I SDR25 – Transmit Mode**

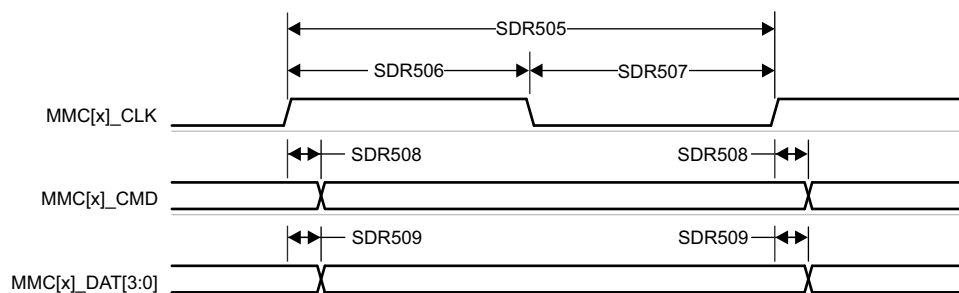
### 6.10.5.12.2.5 UHS-I SDR50 Mode

表 6-87, and 図 6-73 presents switching characteristics for MMC1 – UHS-I SDR50 Mode.

**表 6-87. Switching Characteristics for MMC1 – UHS-I SDR50 Mode**

see 図 6-73

| NO.    | PARAMETER          |                                                              | MIN  | MAX  | UNIT |
|--------|--------------------|--------------------------------------------------------------|------|------|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC1_CLK                                |      | 100  | MHz  |
| SDR505 | $t_{c}(clk)$       | Cycle time, MMC1_CLK                                         | 10   |      | ns   |
| SDR506 | $t_{w}(clkH)$      | Pulse duration, MMC1_CLK high                                | 4.45 |      | ns   |
| SDR507 | $t_{w}(clkL)$      | Pulse duration, MMC1_CLK low                                 | 4.45 |      | ns   |
| SDR508 | $t_{d}(clkL-cmdV)$ | Delay time, MMC1_CLK rising edge to MMC1_CMD transition      | 1.2  | 6.35 | ns   |
| SDR509 | $t_{d}(clkL-dV)$   | Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition | 1.2  | 6.35 | ns   |



**図 6-73. MMC1 – UHS-I SDR50 – Transmit Mode**

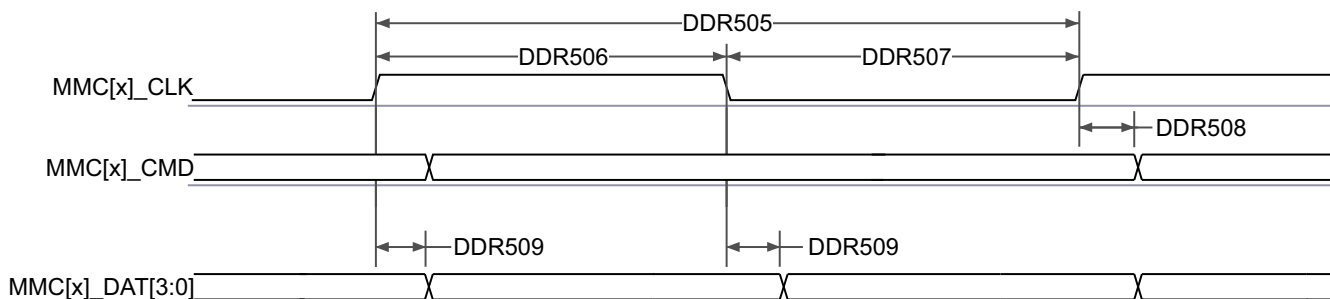
#### 6.10.5.12.2.6 UHS-I DDR50 Mode

表 6-88, and 図 6-74 present switching characteristics for MMC1 – UHS-I DDR50 Mode.

**表 6-88. Switching Characteristics for MMC1 – UHS-I DDR50 Mode**

see 図 6-74

| NO.    | PARAMETER         |                                                             | MIN | MAX  | UNIT |
|--------|-------------------|-------------------------------------------------------------|-----|------|------|
|        | $f_{op(clk)}$     | Operating frequency, MMC1_CLK                               |     | 50   | MHz  |
| DDR505 | $t_{c(clk)}$      | Cycle time, MMC1_CLK                                        | 20  |      | ns   |
| DDR506 | $t_{w(clkH)}$     | Pulse duration, MMC1_CLK high                               | 9.2 |      | ns   |
| DDR507 | $t_{w(clkL)}$     | Pulse duration, MMC1_CLK low                                | 9.2 |      | ns   |
| DDR508 | $t_{d(clk-cmdV)}$ | Delay time, MMC1_CLK rising edge to MMC1_CMD transition     | 1.2 | 6.35 | ns   |
| DDR509 | $t_{d(clk-dV)}$   | Delay time, MMC1_CLK transition to MMC1_DAT[3:0] transition | 1.2 | 6.35 | ns   |



**図 6-74. MMC1 – UHS-I DDR50 – Transmit Mode**

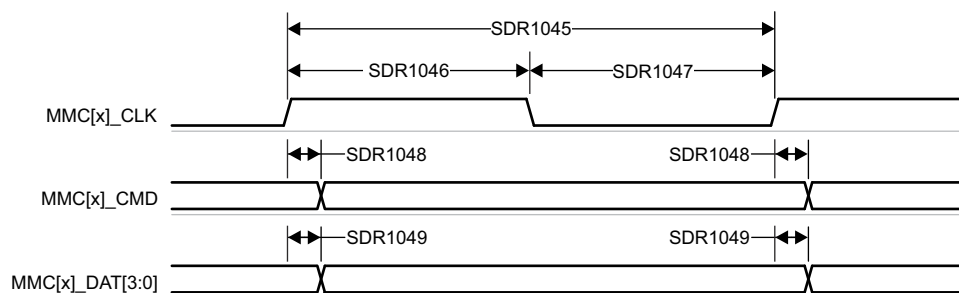
### 6.10.5.12.2.7 UHS-I SDR104 Mode

表 6-89, and 図 6-75 present switching characteristics for MMC1 – UHS-I SDR104 Mode.

**表 6-89. Switching Characteristics for MMC1 – UHS-I SDR104 Mode**

see 図 6-75

| NO.     | PARAMETER          |                                                              | MIN  | MAX | UNIT |
|---------|--------------------|--------------------------------------------------------------|------|-----|------|
|         | $f_{op(clk)}$      | Operating frequency, MMC1_CLK                                |      | 200 | MHz  |
| SDR1045 | $t_{c(clk)}$       | Cycle time, MMC1_CLK                                         | 5    |     | ns   |
| SDR1046 | $t_{w(clkH)}$      | Pulse duration, MMC1_CLK high                                | 2.12 |     | ns   |
| SDR1047 | $t_{w(clkL)}$      | Pulse duration, MMC1_CLK low                                 | 2.12 |     | ns   |
| SDR1048 | $t_{d(clkL-cmdV)}$ | Delay time, MMC1_CLK rising edge to MMC1_CMD transition      | 1.08 | 3.2 | ns   |
| SDR1049 | $t_{d(clkL-dV)}$   | Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition | 1.08 | 3.2 | ns   |



**図 6-75. MMC1 – UHS-I SDR104 – Transmit Mode**

### 6.10.5.13 CPTS

表 6-90, 表 6-91, 図 6-76, 表 6-92, and 図 6-77 present timing conditions, requirements, and switching characteristics for CPTS.

**表 6-90. CPTS Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 10  | pF   |

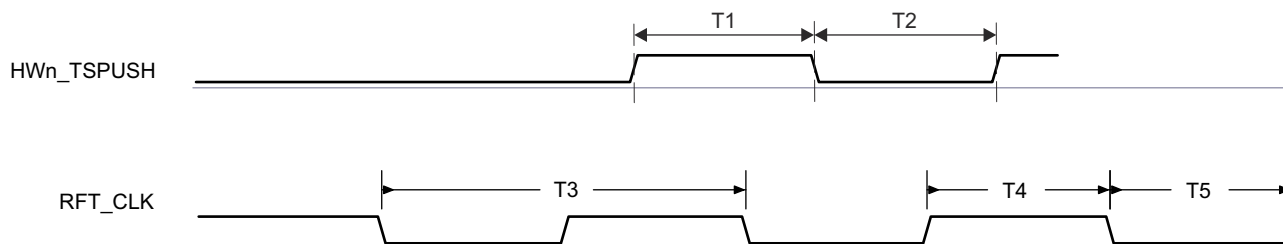
**表 6-91. CPTS Timing Requirements**

see 図 6-76

| NO. | PARAMETER                  | DESCRIPTION                    | MIN                    | MAX | UNIT |
|-----|----------------------------|--------------------------------|------------------------|-----|------|
| T1  | t <sub>w</sub> (HWTSPUSHH) | Pulse duration, HWnTSPUSH high | 12P <sup>(1)</sup> + 2 |     | ns   |
| T2  | t <sub>w</sub> (HWTSPUSHL) | Pulse duration, HWnTSPUSH low  | 12P <sup>(1)</sup> + 2 |     | ns   |
| T3  | t <sub>c</sub> (RFT_CLK)   | Cycle time, RFT_CLK            | 5                      | 8   | ns   |
| T4  | t <sub>w</sub> (RFT_CLKH)  | Pulse duration, RFT_CLK high   | 0.45T <sup>(2)</sup>   |     | ns   |
| T5  | t <sub>w</sub> (RFT_CLKL)  | Pulse duration, RFT_CLK low    | 0.45T <sup>(2)</sup>   |     | ns   |

(1) P = functional clock period in ns.

(2) T = RFT\_CLK period in ns.



**図 6-76. CPTS Timing Requirements**

表 6-92. CPTS Switching Characteristics

see 図 6-77

| NO. | PARAMETER            | DESCRIPTION                    | SOURCE  | MIN             | MAX | UNIT |
|-----|----------------------|--------------------------------|---------|-----------------|-----|------|
| T6  | $t_{w(TS\_COMP)}$    | Pulse duration, TS_COMP high   |         | $36P^{(1)} - 2$ |     | ns   |
| T7  | $t_{w(TS\_COMPL)}$   | Pulse duration, TS_COMP low    |         | $36P^{(1)} - 2$ |     | ns   |
| T8  | $t_{w(TS\_SYNCH)}$   | Pulse duration, TS_SYNC high   |         | $36P^{(1)} - 2$ |     | ns   |
| T9  | $t_{w(TS\_SYNCL)}$   | Pulse duration, TS_SYNC low    |         | $36P^{(1)} - 2$ |     | ns   |
| T10 | $t_{w(SYNCH\_OUTH)}$ | Pulse duration, SYNCn_OUT high | TS_SYNC | $36P^{(1)} - 2$ |     | ns   |
|     |                      |                                | GENF    | $5P^{(1)} - 2$  |     | ns   |
| T11 | $t_{w(SYNCH\_OUTL)}$ | Pulse duration, SYNCn_OUT low  | TS_SYNC | $36P^{(1)} - 2$ |     | ns   |
|     |                      |                                | GENF    | $5P^{(1)} - 2$  |     | ns   |

(1) P = functional clock period in ns.

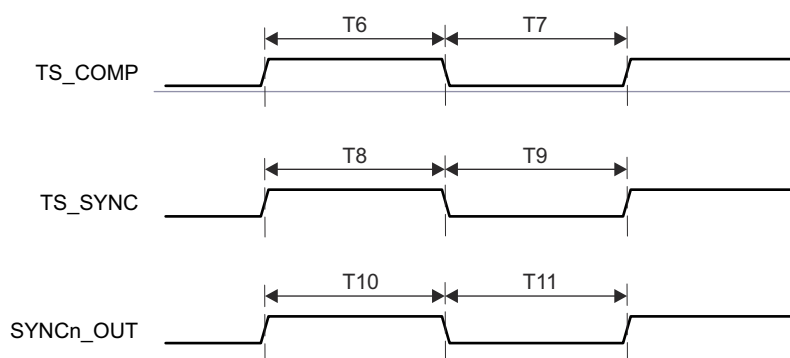


図 6-77. CPTS Switching Characteristics

For more information, see *Data Movement Architecture (DMA)* chapter in the device TRM.

#### 6.10.5.14 OSPI

OSPI0 offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI0\_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI0\_CLK for Double Data Rate (DDR) transfers. PHY mode supports four clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI0\_LBCLKO looped back into the PHY from the OSPI0\_LBCLKO pin as the PHY receive data capture clock. External Board Loopback - uses OSPI0\_LBCLKO looped back into the PHY from the OSPI0\_DQS pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI0\_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200 MHz, which produces an OSPI0\_CLK rate up to 50 MHz for SDR mode or 25 MHz for DDR mode.

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

セクション 6.10.5.14.1 defines timing requirements and switching characteristics associated with PHY mode and セクション 6.10.5.14.2 defines timing requirements and switching characteristics associated with Tap mode.

表 6-93 presents timing conditions for OSPI0.

**表 6-93. OSPI0 Timing Conditions**

| PARAMETER                             |                                                                                     | MODE                                                          | MIN                    | MAX                    | UNIT |
|---------------------------------------|-------------------------------------------------------------------------------------|---------------------------------------------------------------|------------------------|------------------------|------|
| <b>INPUT CONDITIONS</b>               |                                                                                     |                                                               |                        |                        |      |
| SR <sub>I</sub>                       | Input slew rate                                                                     |                                                               | 1                      | 6                      | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                                                                     |                                                               |                        |                        |      |
| C <sub>L</sub>                        | Output load capacitance                                                             |                                                               | 3                      | 10                     | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                                                                     |                                                               |                        |                        |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of OSPI0_CLK trace                                                | No Loopback<br>Internal PHY Loopback<br>Internal Pad Loopback |                        | 450                    | ps   |
|                                       | Propagation delay of OSPI0_LBCLKO trace                                             | External Board Loopback                                       | 2L <sup>(1)</sup> - 30 | 2L <sup>(1)</sup> + 30 | ps   |
|                                       | Propagation delay of OSPI0_DQS trace                                                | DQS                                                           | L <sup>(1)</sup> - 30  | L <sup>(1)</sup> + 30  | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[3:0] relative to OSPI0_CLK | All modes                                                     |                        | 60                     | ps   |

(1) L = Propagation delay of OSPI0\_CLK trace

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.14.1 OSPI0 PHY Mode

##### 6.10.5.14.1.1 OSPI0 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

表 6-94 defines DLL delays required for OSPI0 with Data Training. 表 6-95, 図 6-78, 表 6-96, and 図 6-79 present timing requirements and switching characteristics for OSPI0 with Data Training.

**表 6-94. OSPI0 DLL Delay Mapping for PHY Data Training**

| MODE      | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|-----------|--------------------------------------|-------------|
| Transmit  |                                      |             |
| All modes | PHY_CONFIG_TX_DLL_DELAY_FLD,         | (1)         |
| Receive   |                                      |             |
| All modes | PHY_CONFIG_RX_DLL_DELAY_FLD          | (2)         |

(1) Transmit DLL delay value determined by training software

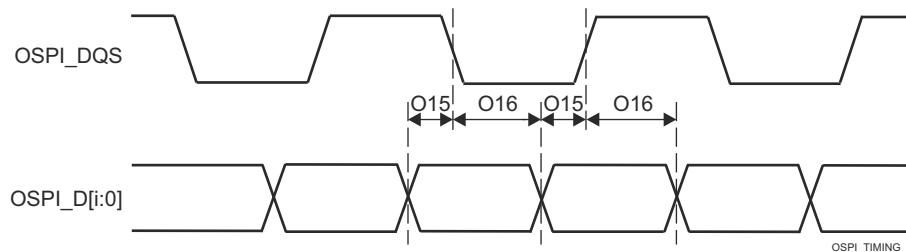
(2) Receive DLL delay value determined by training software

**表 6-95. OSPI0 Timing Requirements – PHY Data Training**

see 図 6-78

| NO. |                   |                                                             | MODE         | MIN | MAX | UNIT |
|-----|-------------------|-------------------------------------------------------------|--------------|-----|-----|------|
| O15 | $t_{su}(D-LBCLK)$ | Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge | DDR with DQS | (1) |     | ns   |
| O16 | $t_h(LBCLK-D)$    | Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge   | DDR with DQS | (1) |     | ns   |

(1) Minimum setup and hold time requirements for OSPI0\_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window.



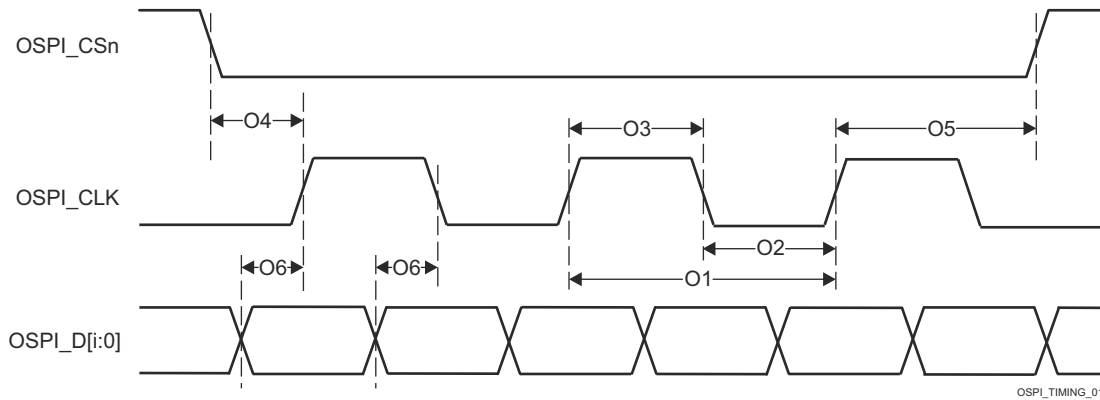
**図 6-78. OSPI0 Timing Requirements – PHY Data Training, DDR with DQS**

**表 6-96. OSPI Switching Characteristics – PHY Data Training**

See 図 6-79

| NO. | PARAMETER               |                                                                   | MODE      | MIN                                                             | MAX                                                             | UNIT |
|-----|-------------------------|-------------------------------------------------------------------|-----------|-----------------------------------------------------------------|-----------------------------------------------------------------|------|
| O1  | $t_{c(\text{CLK})}$     | Cycle time, OSPI0_CLK                                             | 1.8V, DDR | 6.02                                                            | 7.52                                                            | ns   |
|     |                         |                                                                   | 3.3V, DDR | 7.52                                                            | 7.52                                                            | ns   |
| O2  | $t_{w(\text{CLKL})}$    | Pulse duration, OSPI0_CLK low                                     | DDR       | $((0.475P^{(1)}) - 0.3)$                                        |                                                                 | ns   |
| O3  | $t_{w(\text{CLKH})}$    | Pulse duration, OSPI0_CLK high                                    | DDR       | $((0.475P^{(1)}) - 0.3)$                                        |                                                                 | ns   |
| O4  | $t_{d(\text{CSn-CLK})}$ | Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge   | DDR       | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) + (0.04TD^{(5)}) - 1)$ | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + (0.11TD^{(5)}) + 1)$ | ns   |
| O5  | $t_{d(\text{CLK-CSn})}$ | Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge | DDR       | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - (0.04TD^{(5)}) - 1)$ | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) - (0.11TD^{(5)}) + 1)$ | ns   |
| O6  | $t_{d(\text{CLK-D})}$   | Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition      | DDR       | (6)                                                             | (6)                                                             | ns   |

- (1) P = SCLK cycle time in ns = OSPI0\_CLK cycle time in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = reference clock cycle time in ns  
(5) TD = PHY\_CONFIG\_TX\_DLL\_DELAY\_FLD  
(6) Minimum and maximum delay times for OSPI0\_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window.



**図 6-79. OSPI0 Switching Characteristics – PHY DDR Data Training**

#### 6.10.5.14.1.2 OSPI0 Without Data Training

注

Timing parameters defined in this section are only applicable when data training is not implemented and DLL delays are configured as described in 表 6-97 and 表 6-100.

##### 6.10.5.14.1.2.1 OSPI0 PHY SDR Timing

表 6-97 defines DLL delays required for OSPI0 PHY SDR Mode. 表 6-98, 図 6-80, 図 6-81, 表 6-99, and 図 6-82 present timing requirements and switching characteristics for OSPI0 PHY SDR Mode.

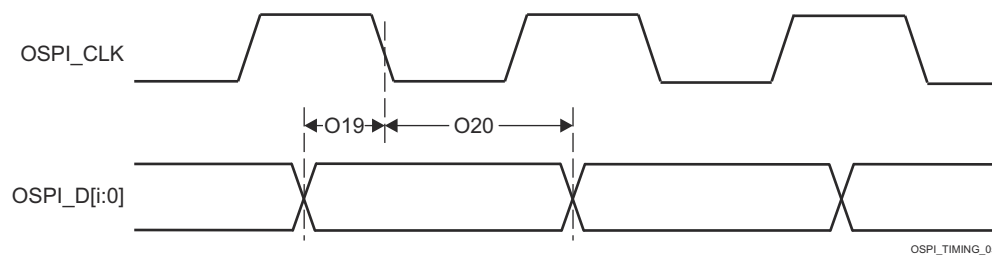
**表 6-97. OSPI0 DLL Delay Mapping for PHY SDR Timing Modes**

| MODE      | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|-----------|--------------------------------------|-------------|
| Transmit  |                                      |             |
| All modes | PHY_CONFIG_TX_DLL_DELAY_FLD,         | 0x0         |
| Receive   |                                      |             |
| All modes | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x0         |

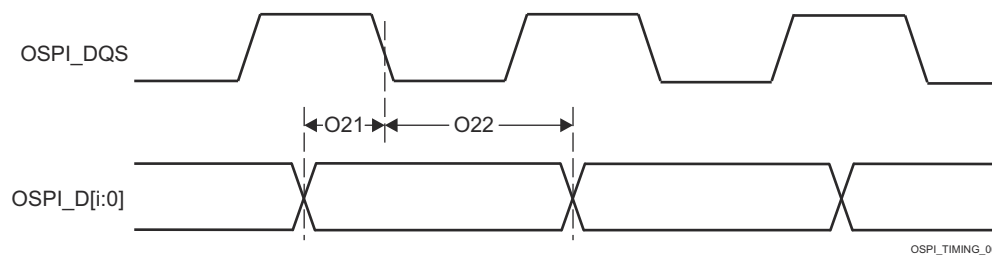
**表 6-98. OSPI0 Timing Requirements – PHY SDR Mode**

see 図 6-80 and 図 6-81

| NO. |                   |                                                             | MODE                                   | MIN  | MAX | UNIT |
|-----|-------------------|-------------------------------------------------------------|----------------------------------------|------|-----|------|
| O19 | $t_{su(D-CLK)}$   | Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge | 1.8V, SDR with Internal PHY Loopback   | 4.8  |     | ns   |
|     |                   |                                                             | 3.3V, SDR with Internal PHY Loopback   | 5.19 |     | ns   |
| O20 | $t_h(CLK-D)$      | Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge   | 1.8V, SDR with Internal PHY Loopback   | -0.5 |     | ns   |
|     |                   |                                                             | 3.3V, SDR with Internal PHY Loopback   | -0.5 |     | ns   |
| O21 | $t_{su(D-LBCLK)}$ | Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge | 1.8V, SDR with External Board Loopback | 0.6  |     | ns   |
|     |                   |                                                             | 3.3V, SDR with External Board Loopback | 0.9  |     | ns   |
| O22 | $t_h(LBCLK-D)$    | Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge   | 1.8V, SDR with External Board Loopback | 1.7  |     | ns   |
|     |                   |                                                             | 3.3V, SDR with External Board Loopback | 2.0  |     | ns   |



**図 6-80. OSPI0 Timing Requirements – PHY SDR with Internal PHY Loopback**



**図 6-81. OSPI0 Timing Requirements – PHY SDR with External Board Loopback**

## 表 6-99. OSPI0 Switching Characteristics – PHY SDR Mode

see 図 6-82

| NO. | PARAMETER               | MODE | MIN                                            | MAX                                            | UNIT |
|-----|-------------------------|------|------------------------------------------------|------------------------------------------------|------|
| O7  | $t_{c(\text{CLK})}$     | 1.8V | 7                                              |                                                | ns   |
|     |                         | 3.3V | 6.03                                           |                                                | ns   |
| O8  | $t_{w(\text{CLKL})}$    |      | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O9  | $t_{w(\text{CLKH})}$    |      | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O10 | $t_{d(\text{CSn-CLK})}$ |      | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)} - 1))$ | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)} + 1))$ | ns   |
| O11 | $t_{d(\text{CLK-CSn})}$ |      | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)} - 1))$ | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)} + 1))$ | ns   |
| O12 | $t_{d(\text{CLK-D})}$   | 1.8V | -1.16                                          | 1.25                                           | ns   |
|     |                         | 3.3V | -1.33                                          | 1.51                                           | ns   |

- (1) P = SCLK cycle time in ns = OSPI0\_CLK cycle time in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = reference clock cycle time in ns

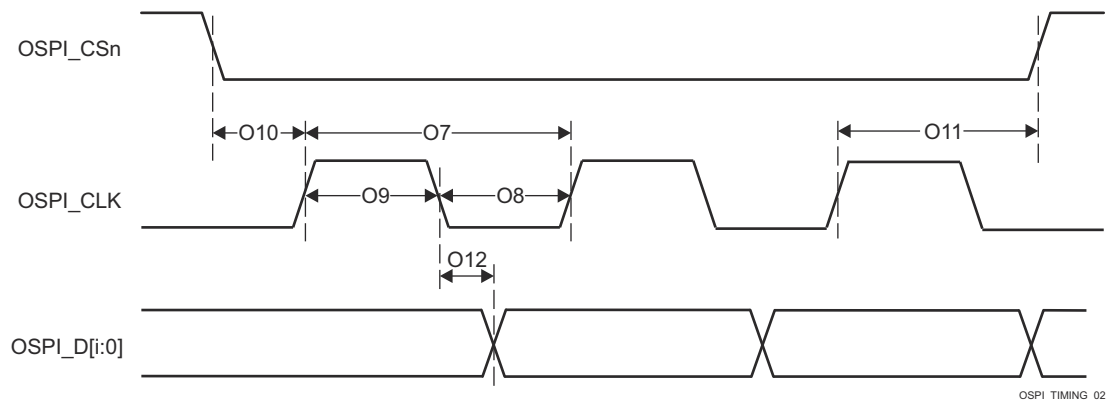


図 6-82. OSPI0 Switching Characteristics – PHY SDR

#### 6.10.5.14.1.2.2 OSPI0 PHY DDR Timing

表 6-100 defines DLL delays required for OSPI0 PHY DDR Mode. 表 6-101, 図 6-83, 表 6-102, and 図 6-84 present timing requirements and switching characteristics for OSPI0 PHY DDR Mode.

**表 6-100. OSPI0 DLL Delay Mapping for PHY DDR Timing Modes**

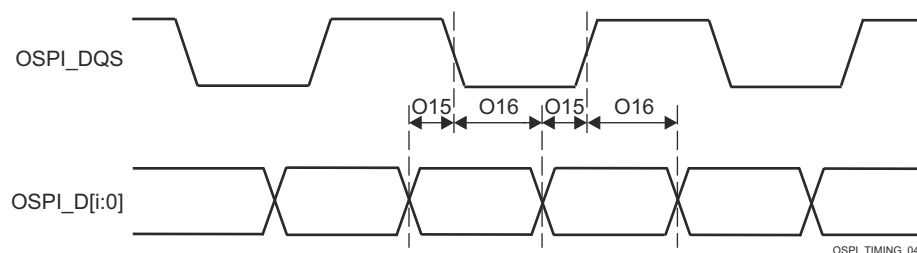
| MODE            | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|-----------------|--------------------------------------|-------------|
| Transmit        |                                      |             |
| 1.8V            | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x3E        |
| 3.3V            | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x3B        |
| Receive         |                                      |             |
| 1.8V, DQS       | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x15        |
| 3.3V, DQS       | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x3A        |
| All other modes | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x0         |

**表 6-101. OSPI0 Timing Requirements – PHY DDR Mode**

see 図 6-83

| NO. |                   |                                                             | MODE                                   | MIN                 | MAX | UNIT |
|-----|-------------------|-------------------------------------------------------------|----------------------------------------|---------------------|-----|------|
| O15 | $t_{su(D-LBCLK)}$ | Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge | 1.8V, DDR with External Board Loopback | 0.53                |     | ns   |
|     |                   |                                                             | 1.8V, DDR with DQS                     | -0.46               |     | ns   |
|     |                   |                                                             | 3.3V, DDR with External Board Loopback | 1.23                |     | ns   |
|     |                   |                                                             | 3.3V, DDR with DQS                     | -0.66               |     | ns   |
| O16 | $t_{h(LBCLK-D)}$  | Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge   | 1.8V, DDR with External Board Loopback | 1.24 <sup>(1)</sup> |     | ns   |
|     |                   |                                                             | 1.8V, DDR with DQS                     | 3.59                |     | ns   |
|     |                   |                                                             | 3.3V, DDR with External Board Loopback | 1.44 <sup>(1)</sup> |     | ns   |
|     |                   |                                                             | 3.3V, DDR with DQS                     | 7.92                |     | ns   |

- (1) This Hold time requirement is larger than the Hold time provided by a typical OSPI/QSPI/SPI device. Therefore, the trace length between the SoC and attached OSPI/QSPI/SPI device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI0\_LBCLKO to OSPI0\_DQS) may need to be shortened to compensate.



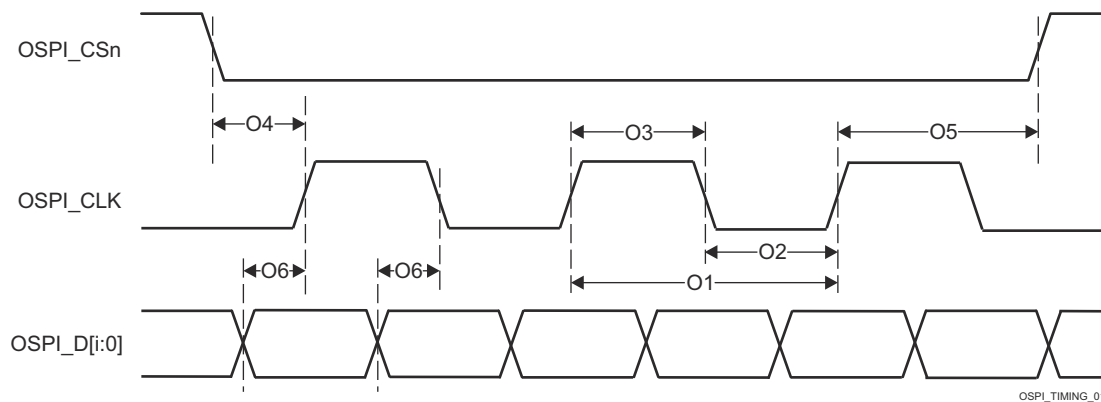
**図 6-83. OSPI0 Timing Requirements – PHY DDR with External Board Loopback or DQS**

**表 6-102. OSPI0 Switching Characteristics – PHY DDR Mode**

see 図 6-84

| NO. | PARAMETER                                                                          | MODE | MIN                                            | MAX                                            | UNIT |
|-----|------------------------------------------------------------------------------------|------|------------------------------------------------|------------------------------------------------|------|
| O1  | $t_{c(CLK)}$ Cycle time, OSPI0_CLK                                                 |      | 19                                             |                                                | ns   |
| O2  | $t_{w(CLKL)}$ Pulse duration, OSPI0_CLK low                                        |      | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O3  | $t_{w(CLKH)}$ Pulse duration, OSPI0_CLK high                                       |      | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O4  | $t_{d(CSn-CLK)}$ Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge   |      | $((0.475P^{(1)}) - (0.975M^{(2)}R^{(4)}))$     | $((0.525P^{(1)}) - (1.025M^{(2)}R^{(4)}) + 7)$ | ns   |
| O5  | $t_{d(CLK-CSn)}$ Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge |      | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - 7)$ | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}))$     | ns   |
| O6  | $t_{d(CLK-D)}$ Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition        | 1.8V | -7.71                                          | -1.56                                          | ns   |
|     |                                                                                    | 3.3V | -7.71                                          | -1.56                                          | ns   |

- (1) P = SCLK cycle time in ns = OSPI0\_CLK cycle time in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = reference clock cycle time in ns



**図 6-84. OSPI0 Switching Characteristics – PHY DDR**

## 6.10.5.14.2 OSPI0 Tap Mode

### 6.10.5.14.2.1 OSPI0 Tap SDR Timing

表 6-103, 図 6-85, 表 6-104, and 図 6-86 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

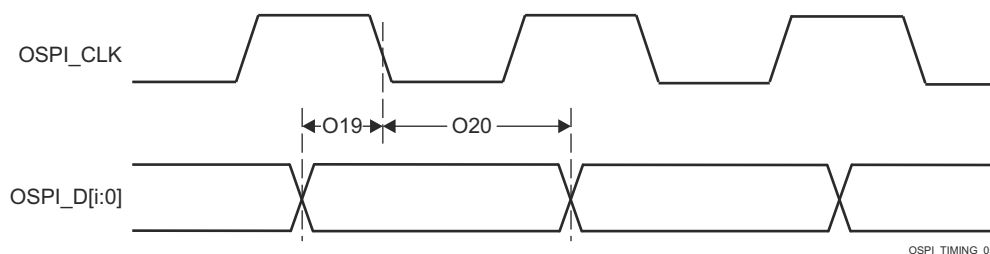
**表 6-103. OSPI0 Timing Requirements – Tap SDR Mode**

see 図 6-85

| NO. |                 | MODE                                                        | MIN                                | MAX | UNIT |
|-----|-----------------|-------------------------------------------------------------|------------------------------------|-----|------|
| O19 | $t_{su(D-CLK)}$ | Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge | (15.4 - $(0.975T^{(1)}R^{(2)})$ )  |     | ns   |
| O20 | $t_{h(CLK-D)}$  | Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge   | (- 4.3 + $(0.975T^{(1)}R^{(2)})$ ) |     | ns   |

(1) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DELAY\_FLD]

(2) R = reference clock cycle time in ns



**図 6-85. OSPI0 Timing Requirements – Tap SDR, No Loopback**

**表 6-104. OSPI0 Switching Characteristics – Tap SDR Mode**

see 図 6-86

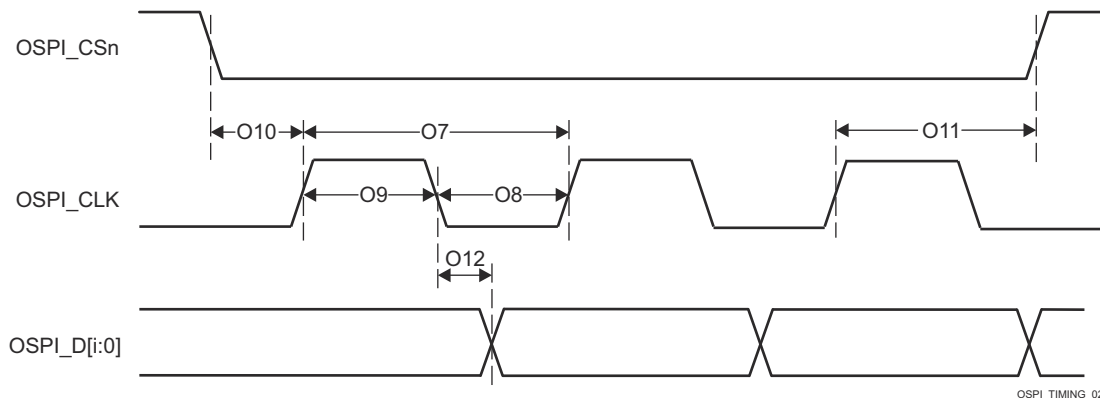
| NO. | PARAMETER        | MODE                                                              | MIN                                            | MAX                                            | UNIT |
|-----|------------------|-------------------------------------------------------------------|------------------------------------------------|------------------------------------------------|------|
| O7  | $t_{c(CLK)}$     | Cycle time, OSPI0_CLK                                             | 20                                             |                                                | ns   |
| O8  | $t_{w(CLKL)}$    | Pulse duration, OSPI0_CLK low                                     | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O9  | $t_{w(CLKH)}$    | Pulse duration, OSPI0_CLK high                                    | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O10 | $t_{d(CSn-CLK)}$ | Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge   | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) - 1)$ | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + 1)$ | ns   |
| O11 | $t_{d(CLK-CSn)}$ | Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - 1)$ | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) + 1)$ | ns   |
| O12 | $t_{d(CLK-D)}$   | Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition      | - 4.25                                         | 7.25                                           | ns   |

(1) P = SCLK cycle time in ns = OSPI0\_CLK cycle time in ns

(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]

(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]

(4) R = reference clock cycle time in ns



**図 6-86. OSPI0 Switching Characteristics – Tap SDR, No Loopback**

#### 6.10.5.14.2.2 OSPI0 Tap DDR Timing

表 6-105, 図 6-87, 表 6-106, and 図 6-88 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

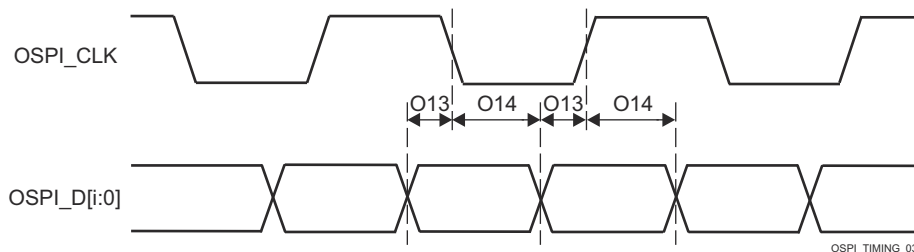
**表 6-105. OSPI0 Timing Requirements – Tap DDR Mode**

see 図 6-87

| NO. |                 |                                                             | MODE        | MIN                                                  | MAX | UNIT |
|-----|-----------------|-------------------------------------------------------------|-------------|------------------------------------------------------|-----|------|
| O13 | $t_{su(D-CLK)}$ | Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge | No Loopback | (17.04 - (0.975T <sup>(1)</sup> R <sup>(2)</sup> ))  |     | ns   |
| O14 | $t_{h(CLK-D)}$  | Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge   | No Loopback | (- 3.16 + (0.975T <sup>(1)</sup> R <sup>(2)</sup> )) |     | ns   |

(1) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DELAY\_FLD]

(2) R = reference clock cycle time in ns



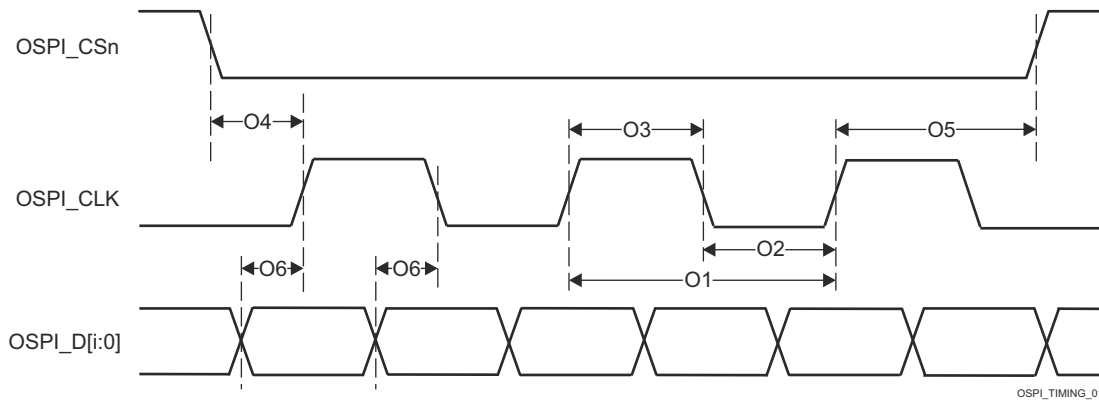
**図 6-87. OSPI0 Timing Requirements – Tap DDR, No Loopback**

**表 6-106. OSPI0 Switching Characteristics – Tap DDR Mode**

see 図 6-88

| NO. | PARAMETER        | MODE                                                              | MIN                                                      | MAX                                                     | UNIT |
|-----|------------------|-------------------------------------------------------------------|----------------------------------------------------------|---------------------------------------------------------|------|
| O1  | $t_{c(CLK)}$     | Cycle time, OSPI0_CLK                                             | 40                                                       |                                                         | ns   |
| O2  | $t_{w(CLKL)}$    | Pulse duration, OSPI0_CLK low                                     | $((0.475P^{(1)}) - 0.3)$                                 |                                                         | ns   |
| O3  | $t_{w(CLKH)}$    | Pulse duration, OSPI0_CLK high                                    | $((0.475P^{(1)}) - 0.3)$                                 |                                                         | ns   |
| O4  | $t_{d(CSn-CLK)}$ | Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge   | $((0.475P^{(1)}) + ((0.975M^{(2)}R^{(5)}) - 1))$         | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(5)}) + 1)$          | ns   |
| O5  | $t_{d(CLK-CSn)}$ | Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(5)}) - 1)$           | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(5)}) + 1)$          | ns   |
| O6  | $t_{d(CLK-D)}$   | Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition      | $(-5.04 + (0.975(T^{(4)} + 1)R^{(5)}) - (0.525P^{(1)}))$ | $(3.64 + (1.025(T^{(4)} + 1)R^{(5)}) - (0.475P^{(1)}))$ | ns   |

- (1) P = SCLK cycle time in ns = OSPI0\_CLK cycle time in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DDR\_READ\_DELAY\_FLD]  
(5) R = reference clock cycle time in ns



**図 6-88. OSPI0 Switching Characteristics – Tap DDR, No Loopback**

#### 6.10.5.15 PCIe

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express (PCIe), see the *SERDES0 Signal Descriptions* and the corresponding subsection within *Detailed Description*.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter of the device TRM.

#### 6.10.5.16 PRU\_ICSSG

The device has integrated two identical Programmable Real-Time Unit Subsystem and Industrial Communication Subsystems - Gigabit (PRU\_ICSSG), PRU\_ICSSG0 and PRU\_ICSSG1. The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores in the device.

For more details about features and additional description information on the device PRU\_ICSSG, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

注

The PRU\_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU\_ICSSG chapter in the device TRM.

##### 6.10.5.16.1 PRU\_ICSSG Programmable Real-Time Unit (PRU)

注

The PRU\_ICSSG PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the *PRU Module Interface* section in the device TRM.

**表 6-107. PRU\_ICSSG PRU Timing Conditions**

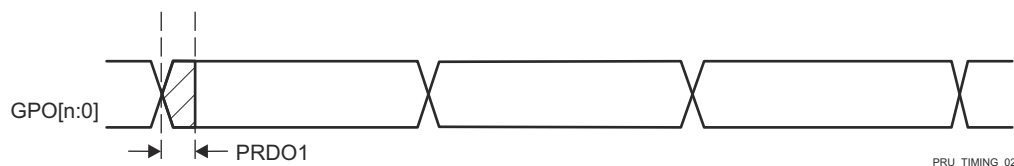
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 30  | pF   |

##### 6.10.5.16.1.1 PRU\_ICSSG PRU Direct Output Mode Timing

**表 6-108. PRU\_ICSSG PRU Switching Characteristics – Direct Output Mode**

see [図 6-89](#)

| NO.   | PARAMETER                 | DESCRIPTION      | MIN | MAX | UNIT |
|-------|---------------------------|------------------|-----|-----|------|
| PRDO1 | t <sub>sk</sub> (GPO-GPO) | Skew, GPO to GPO |     | 2   | ns   |



A. n in GPO[n:0] = 19.

**図 6-89. PRU\_ICSSG PRU Direct Output Timing**

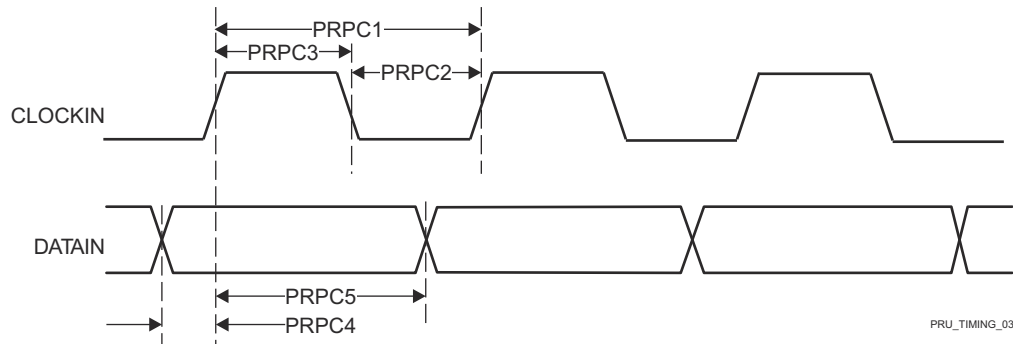
#### 6.10.5.16.1.2 PRU\_ICSSG PRU Parallel Capture Mode Timing

**表 6-109. PRU\_ICSSG PRU Timing Requirements – Parallel Capture Mode**

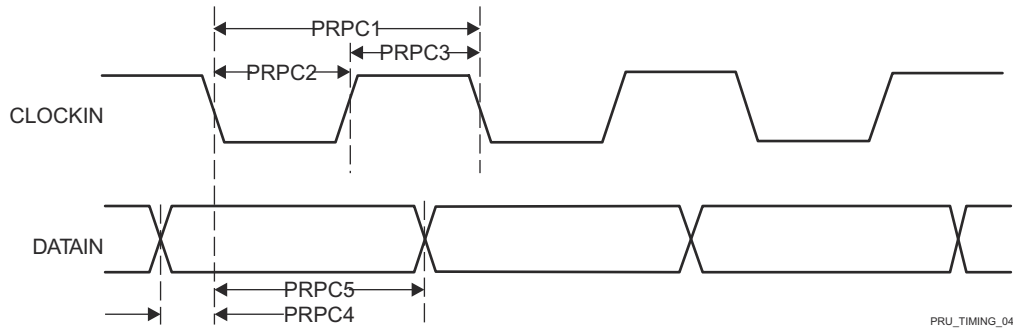
see 図 6-90 and 図 6-91

| NO.   | PARAMETER              | DESCRIPTION                                         | MIN                  | MAX | UNIT |
|-------|------------------------|-----------------------------------------------------|----------------------|-----|------|
| PRPC1 | $t_{c(CLOCK)}$         | Cycle time, CLOCKIN                                 | 20                   |     | ns   |
| PRPC2 | $t_{w(CLOCKL)}$        | Pulse duration, CLOCKIN low                         | 0.45P <sup>(1)</sup> |     | ns   |
| PRPC3 | $t_{w(CLOCKH)}$        | Pulse duration, CLOCKIN high                        | 0.45P <sup>(1)</sup> |     | ns   |
| PRPC4 | $t_{su(DATAIN-CLOCK)}$ | Setup time, DATAIN valid before CLOCKIN active edge | 4                    |     | ns   |
| PRPC5 | $t_{h(CLOCK-DATAIN)}$  | Hold time, DATAIN valid after CLOCKIN active edge   | 0                    |     | ns   |

(1) P = CLOCKIN cycle time in ns



**図 6-90. PRU\_ICSSG PRU Parallel Capture Timing Requirements – Rising Edge Mode**



**図 6-91. PRU\_ICSSG PRU Parallel Capture Timing Requirements – Falling Edge Mode**

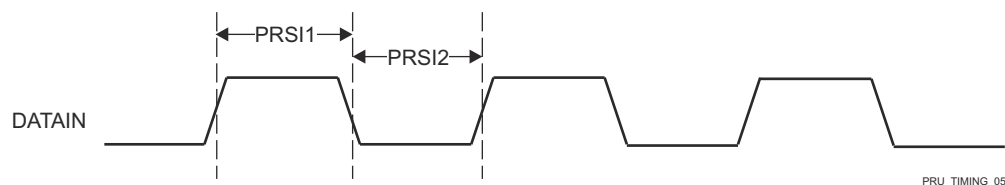
### 6.10.5.16.1.3 PRU\_ICSSG PRU Shift Mode Timing

**表 6-110. PRU\_ICSSG PRU Timing Requirements – Shift In Mode**

see [図 6-92](#)

| NO.   | PARAMETER        | DESCRIPTION                 | MIN            | MAX | UNIT |
|-------|------------------|-----------------------------|----------------|-----|------|
| PRSI1 | $t_{w(DATAINH)}$ | Pulse duration, DATAIN high | $2P^{(1)} + 2$ |     | ns   |
| PRSI2 | $t_{w(DATAINL)}$ | Pulse duration, DATAIN low  | $2P^{(1)} + 2$ |     | ns   |

- (1) P = Internal shift in clock period, defined by PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 bit fields in the ICSSG\_GPCFGn\_REG register. PRUn represents the respective PRU0 or PRU1 instance.



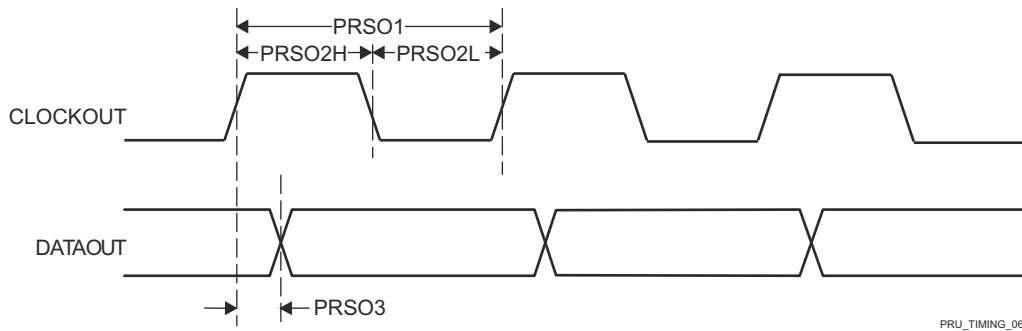
**図 6-92. PRU\_ICSSG PRU Shift In Timing**

**表 6-111. PRU\_ICSSG PRU Switching Characteristics – Shift Out Mode**

see 図 6-93

| NO.    | PARAMETER                        | DESCRIPTION                           | MIN                         | MAX | UNIT |
|--------|----------------------------------|---------------------------------------|-----------------------------|-----|------|
| PRSO1  | $t_{c}(\text{CLOCKOUT})$         | Cycle time, CLOCKOUT                  | 10                          |     | ns   |
| PRSO2L | $t_{w}(\text{CLOCKOUTL})$        | Pulse duration, CLOCKOUT low          | $0.475P^{(1)}Z^{(2)} - 0.3$ |     | ns   |
| PRSO2H | $t_{w}(\text{CLOCKOUTH})$        | Pulse duration, CLOCKOUT high         | $0.475P^{(1)}Y^{(3)} - 0.3$ |     | ns   |
| PRSO3  | $t_{d}(\text{CLOCKOUT-DATAOUT})$ | Delay time, CLOCKOUT to DATAOUT valid | -1                          | 4   | ns   |

- (1) P = Software programmable shift out clock period, defined by PRUn\_GPO\_DIV0 and PRUn\_GPO\_DIV1 bit fields in the ICSSG\_GPCFGn\_REG register, where PRUn represents the respective PRU0 or PRU1 instance.
- (2) The Z parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.
- If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are INTEGERS -or- if PRUn\_GPI\_DIV0 is a NON-INTEGER and PRUn\_GPI\_DIV1 is an EVEN INTEGER then, Z equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1})$ .
  - If PRUn\_GPI\_DIV0 is a NON-INTEGER and PRUn\_GPI\_DIV1 is an ODD INTEGER then, Z equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1} + 0.5)$ .
  - If PRUn\_GPI\_DIV0 is an INTEGER and PRUn\_GPI\_DIV1 is a NON-INTEGER then, Z equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1} + 0.5 * \text{PRUn\_GPI\_DIV0})$ .
  - If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are NON-INTEGERS then, Z equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1} + 0.25 * \text{PRUn\_GPI\_DIV0})$ .
- (3) The Y parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.
- If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are INTEGERS -or- if PRUn\_GPI\_DIV0 is a NON-INTEGER and PRUn\_GPI\_DIV1 is an EVEN INTEGER then, Y equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1})$ .
  - If PRUn\_GPI\_DIV0 is a NON-INTEGER and PRUn\_GPI\_DIV1 is an ODD INTEGER then, Y equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1} - 0.5)$ .
  - If PRUn\_GPI\_DIV0 is an INTEGER and PRUn\_GPI\_DIV1 is a NON-INTEGER then, Y equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1} - 0.5 * \text{PRUn\_GPI\_DIV0})$ .
  - If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are NON-INTEGERS then, Y1 equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1} - 0.25 * \text{PRUn\_GPI\_DIV0})$  and Y2 equals  $(\text{PRUn\_GPI\_DIV0} * \text{PRUn\_GPI\_DIV1} + 0.25 * \text{PRUn\_GPI\_DIV0})$ , where Y1 is the first high pulse and Y2 is the second high pulse.



**図 6-93. PRU\_ICSSG PRU Shift Out Timing**

#### 6.10.5.16.1.4 PRU\_ICSSG PRU Sigma Delta and Peripheral Interface

**表 6-112. PRU\_ICSSG PRU Sigma Delta and Peripheral Interface Timing Conditions**

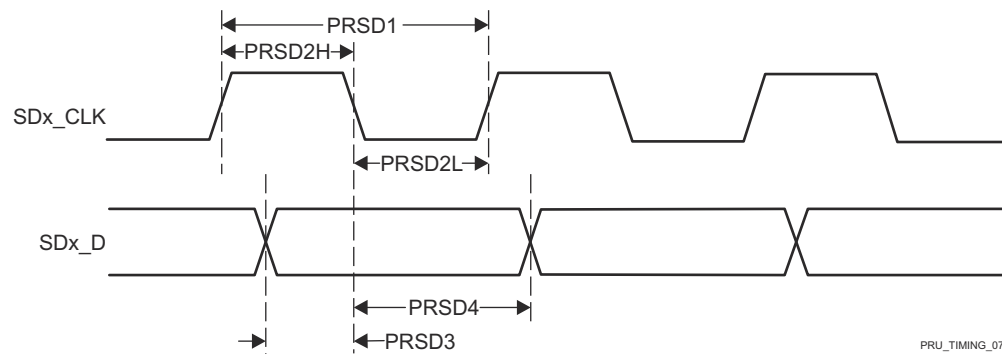
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 18  | pF   |

#### 6.10.5.16.1.4.1 PRU\_ICSSG PRU Sigma Delta and Peripheral Interface Timing

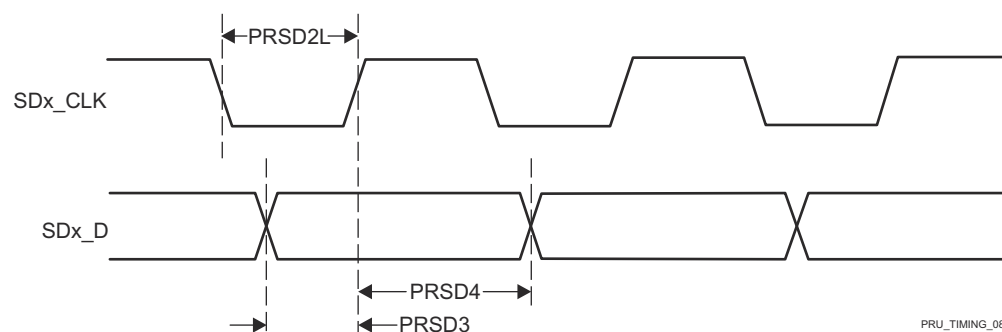
**表 6-113. PRU\_ICSSG PRU Timing Requirements – Sigma Delta Mode**

see 図 6-94 and 図 6-95

| NO.    | PARAMETER                     | DESCRIPTION                                        | MIN | MAX | UNIT |
|--------|-------------------------------|----------------------------------------------------|-----|-----|------|
| PRSD1  | t <sub>c</sub> (SD_CLK)       | Cycle time, SDx_CLK                                | 40  |     | ns   |
| PRSD2L | t <sub>w</sub> (SD_CLKL)      | Pulse duration, SDx_CLK low                        | 20  |     | ns   |
| PRSD2H | t <sub>w</sub> (SD_CLKH)      | Pulse duration, SDx_CLK high                       | 20  |     | ns   |
| PRSD3  | t <sub>su</sub> (SD_D-SD_CLK) | Setup time, SDx_D valid before SDx_CLK active edge | 10  |     | ns   |
| PRSD4  | t <sub>h</sub> (SD_CLK-SD_D)  | Hold time, SDx_D valid before SDx_CLK active edge  | 5   |     | ns   |



**図 6-94. PRU\_ICSSG PRU SD\_CLK Falling Active Edge**



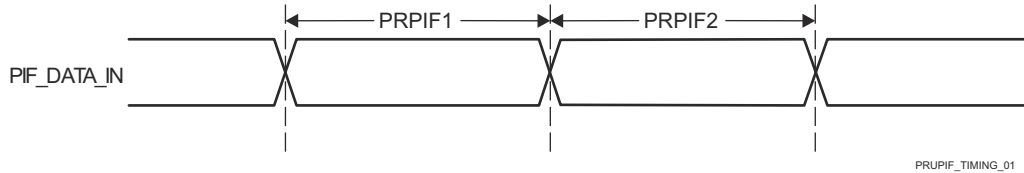
**図 6-95. PRU\_ICSSG PRU SD\_CLK Rising Active Edge**

**表 6-114. PRU\_ICSSG PRU Timing Requirements – Peripheral Interface Mode**

see 図 6-96

| NO.    | PARAMETER               | DESCRIPTION                      | MIN                                 | MAX | UNIT |
|--------|-------------------------|----------------------------------|-------------------------------------|-----|------|
| PRPIF1 | $t_{w(PIF\_DATA\_INH)}$ | Pulse duration, PIF_DATA_IN high | $2 + 0.475 \cdot (4 \cdot P)^{(1)}$ |     | ns   |
| PRPIF2 | $t_{w(PIF\_DATA\_INL)}$ | Pulse duration, PIF_DATA_IN low  | $2 + 0.475 \cdot (4 \cdot P)^{(1)}$ |     | ns   |

(1)  $P = 1x$  (or TX) clock period in ns, defined by PRUn\_ED\_TX\_DIV\_FACTOR and PRUn\_ED\_TX\_DIV\_FACTOR\_FRAC in the ICSSG\_PRUn\_ED\_TX\_CFG\_REG register. PRUn represents the respective PRU0 or PRU1 instance.



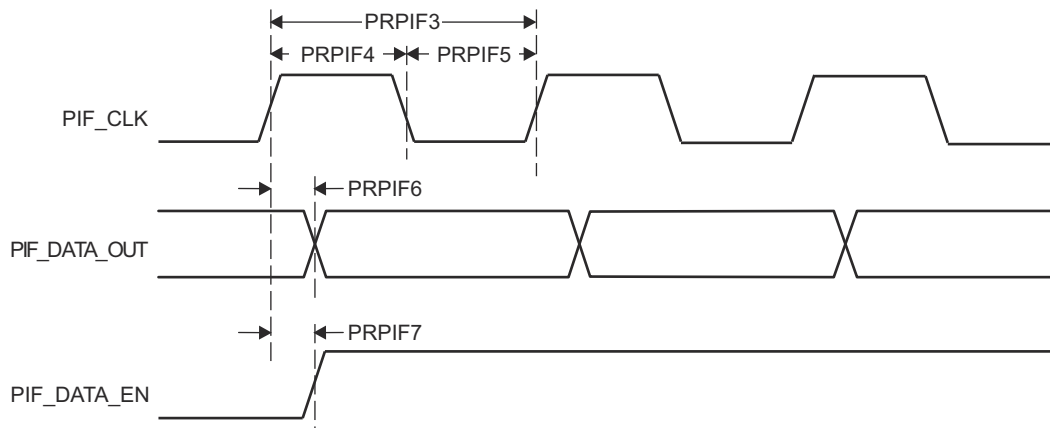
**図 6-96. PRU\_ICSSG PRU Peripheral Interface Timing Requirements**

**表 6-115. PRU\_ICSSG PRU Switching Characteristics – Peripheral Interface Mode**

see 図 6-97

| NO.    | PARAMETER                      | DESCRIPTION                              | MIN                   | MAX | UNIT |
|--------|--------------------------------|------------------------------------------|-----------------------|-----|------|
| PRPIF3 | $t_c(PIF\_CLK)$                | Cycle time, PIF_CLK                      | 30                    |     | ns   |
| PRPIF4 | $t_{w(PIF\_CLKH)}$             | Pulse duration, PIF_CLK high             | $0.475 \cdot P^{(1)}$ |     | ns   |
| PRPIF5 | $t_{w(PIF\_CLKL)}$             | Pulse duration, PIF_CLK low              | $0.475 \cdot P^{(1)}$ |     | ns   |
| PRPIF6 | $t_d(PIF\_CLK-PIF\_DATA\_OUT)$ | Delay time, PIF_CLK fall to PIF_DATA_OUT | -5                    | 5   | ns   |
| PRPIF7 | $t_d(PIF\_CLK-PIF\_DATA\_EN)$  | Delay time, PIF_CLK fall to PIF_DATA_EN  | -5                    | 5   | ns   |

(1)  $P = 1x$  (or TX) clock period in ns, defined by PRUn\_ED\_TX\_DIV\_FACTOR and PRUn\_ED\_TX\_DIV\_FACTOR\_FRAC in the ICSSG\_PRUn\_ED\_TX\_CFG\_REG register. PRUn represents the respective PRU0 or PRU1 instance.



**図 6-97. PRU\_ICSSG PRU Peripheral Interface Switching Characteristics**

6.10.5.16.2 PRU\_ICSSG Pulse Width Modulation (PWM)

表 6-116. PRU\_ICSSG PWM Timing Conditions

| PARAMETER         |                         | MIN | MAX | UNIT |
|-------------------|-------------------------|-----|-----|------|
| INPUT CONDITIONS  |                         |     |     |      |
| SR <sub>I</sub>   | Input slew rate         | 1   | 4   | V/ns |
| OUTPUT CONDITIONS |                         |     |     |      |
| C <sub>L</sub>    | Output load capacitance | 2   | 7   | pF   |

6.10.5.16.2.1 PRU\_ICSSG PWM Timing

表 6-117. PRU\_ICSSG PWM Switching Characteristics

see [図 6-98](#)

| NO.    | PARAMETER                     | DESCRIPTION          | MIN | MAX | UNIT |
|--------|-------------------------------|----------------------|-----|-----|------|
| PRPWM1 | t <sub>sk</sub> (PWM_A-PWM_B) | Skew, PWM_A to PWM_B |     | 5   | ns   |

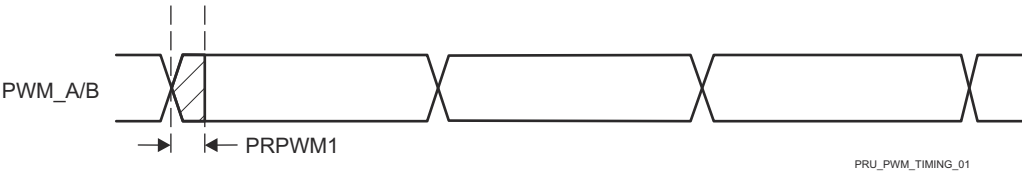


図 6-98. PRU\_ICSSG PWM Timing

### 6.10.5.16.3 PRU\_ICSSG Industrial Ethernet Peripheral (IEP)

表 6-118. PRU\_ICSSG IEP Timing Conditions

| PARAMETER                |                         |                                | MIN | MAX | UNIT |
|--------------------------|-------------------------|--------------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |                                |     |     |      |
| SR <sub>I</sub>          | Input slew rate         |                                | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |                                |     |     |      |
| C <sub>L</sub>           | Output load capacitance | EDC_SYNC_OUTx<br>EDIO_OUTVALID | 2   | 7   | pF   |
|                          |                         | EDIO_DATA_OUT                  | 3   | 10  | pF   |

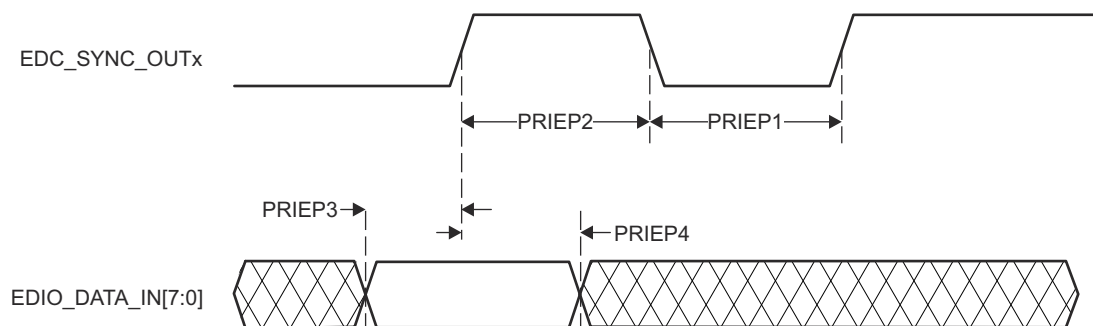
#### 6.10.5.16.3.1 PRU\_ICSSG IEP Timing

表 6-119. PRU\_ICSSG IEP Timing Requirements – Input Validated with SYNC

see 図 6-99

| NO.    | PARAMETER                                        | DESCRIPTION                                                     | MIN                    | MAX | UNIT |
|--------|--------------------------------------------------|-----------------------------------------------------------------|------------------------|-----|------|
| PRIEP1 | t <sub>w</sub> (EDC_SYNC_OUTxL)                  | Pulse duration, EDC_SYNC_OUTx low                               | 20P <sup>(1)</sup> - 2 |     | ns   |
| PRIEP2 | t <sub>w</sub> (EDC_SYNC_OUTxH)                  | Pulse duration, EDC_SYNC_OUTx high                              | 20P <sup>(1)</sup> - 2 |     | ns   |
| PRIEP3 | t <sub>su</sub> (EDIO_DATA_IN-<br>EDC_SYNC_OUTx) | Setup time, EDIO_DATA_IN valid before EDC_SYNC_OUTx active edge | 20                     |     | ns   |
| PRIEP4 | t <sub>h</sub> (EDC_SYNC_OUTx-<br>EDIO_DATA_IN)  | Hold time, EDIO_DATA_IN valid after EDC_SYNC_OUTx active edge   | 20                     |     | ns   |

(1) P = PRU\_ICSSG IEP clock source period in ns.



PRU\_IEP\_TIMING\_01

図 6-99. PRU\_ICSSG IEP SYNC Timing Requirements

**表 6-120. PRU\_ICSSG IEP Switching Characteristics – Digital IOs**

see 図 6-100

| NO.    | PARAMETER                               | DESCRIPTION                                | MIN             | MAX         | UNIT |
|--------|-----------------------------------------|--------------------------------------------|-----------------|-------------|------|
| IEPIO1 | $t_{w(EDIO\_OUTVALIDL)}$                | Pulse duration, EDIO_OUTVALID low          | $14P^{(1)} - 2$ |             | ns   |
| IEPIO2 | $t_{w(EDIO\_OUTVALIDH)}$                | Pulse duration, EDIO_OUTVALID high         | $32P^{(1)} - 2$ |             | ns   |
| IEPIO3 | $t_{d(EDIO\_OUTVALID-EDIO\_DATA\_OUT)}$ | Delay time, EDIO_OUTVALID to EDIO_DATA_OUT | 0               | $18P^{(1)}$ | ns   |
| IEPIO4 | $t_{sk(EDIO\_DATA\_OUT)}$               | EDIO_DATA_OUT skew                         |                 | 5           | ns   |

(1) P = PRU\_ICSSG IEP clock source period in ns.



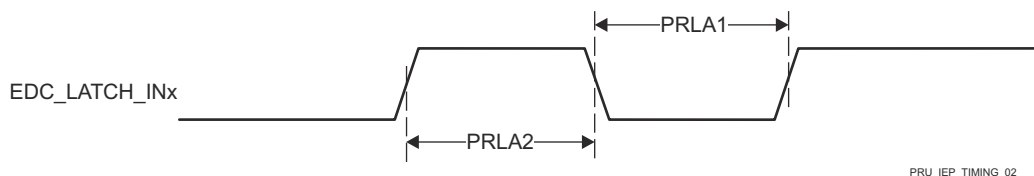
**図 6-100. PRU\_ICSSG IEP Digital IOs Timing Requirements**

**表 6-121. PRU\_ICSSG IEP Timing Requirements – LATCH\_INx**

see 図 6-101

| NO.   | PARAMETER                 | DESCRIPTION                        | MIN            | MAX | UNIT |
|-------|---------------------------|------------------------------------|----------------|-----|------|
| PRLA1 | $t_{w(EDC\_LATCH\_INxL)}$ | Pulse duration, EDC_LATCH_INx low  | $3P^{(1)} + 2$ |     | ns   |
| PRLA2 | $t_{w(EDC\_LATCH\_INxH)}$ | Pulse duration, EDC_LATCH_INx high | $3P^{(1)} + 2$ |     | ns   |

(1) P = PRU\_ICSSG IEP clock source period in ns.



**図 6-101. PRU\_ICSSG IEP LATCH\_INx Timing Requirements**

#### 6.10.5.16.4 PRU\_ICSSG Universal Asynchronous Receiver Transmitter (UART)

**表 6-122. PRU\_ICSSG UART Timing Conditions**

| PARAMETER                |                         | MIN | MAX               | UNIT |
|--------------------------|-------------------------|-----|-------------------|------|
| <b>INPUT CONDITIONS</b>  |                         |     |                   |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 5                 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |                   |      |
| C <sub>L</sub>           | Output load capacitance | 1   | 30 <sup>(1)</sup> | pF   |

- (1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

##### 6.10.5.16.4.1 PRU\_ICSSG UART Timing

**表 6-123. PRU\_ICSSG UART Timing Requirements**

see 図 6-102

| NO. | PARAMETER             | DESCRIPTION                               | MIN                         | MAX                         | UNIT |
|-----|-----------------------|-------------------------------------------|-----------------------------|-----------------------------|------|
| 1   | t <sub>w</sub> (RXD)  | Pulse width, receive data bit high or low | 0.95U <sup>(1)</sup><br>(2) | 1.05U <sup>(1)</sup><br>(2) | ns   |
| 2   | t <sub>w</sub> (RXDS) | Pulse width, receive start bit low        | 0.95U <sup>(1)</sup><br>(2) |                             | ns   |

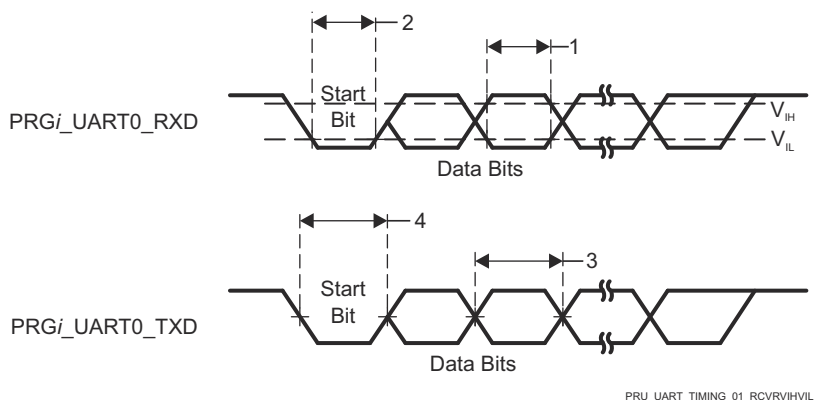
- (1) U = UART baud time in ns = 1/programmed baud rate.  
(2) This value defines the data valid time, where the input voltage is required to be above V<sub>IH</sub> or below V<sub>IL</sub>.

**表 6-124. PRU\_ICSSG UART Switching Characteristics**

see 図 6-102

| NO. | PARAMETER             | DESCRIPTION                                | MIN                  | MAX                  | UNIT |
|-----|-----------------------|--------------------------------------------|----------------------|----------------------|------|
|     | f(baud)               | Programmed baud rate                       |                      | 12                   | Mbps |
| 3   | t <sub>w</sub> (TXD)  | Pulse width, transmit data bit high or low | U <sup>(1)</sup> - 2 | U <sup>(1)</sup> + 2 | ns   |
| 4   | t <sub>w</sub> (TXDS) | Pulse width, transmit start bit low        | U <sup>(1)</sup> - 2 | U <sup>(1)</sup> + 2 | ns   |

- (1) U = UART baud time in ns = 1/actual baud rate, where the actual baud rate is defined in the UART Baud Rate Settings table of the device TRM.



**図 6-102. PRU\_ICSSG UART Timing Requirements and Switching Characteristics**

#### 6.10.5.16.5 PRU\_ICSSG Enhanced Capture Peripheral (ECAP)

表 6-125. PRU\_ICSSG ECAP Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

#### 6.10.5.16.5.1 PRU\_ICSSG ECAP Timing

表 6-126. PRU\_ICSSG ECAP Timing Requirements

see 図 6-103

| NO.   | PARAMETER              | DESCRIPTION                          | MIN                   | MAX | UNIT |
|-------|------------------------|--------------------------------------|-----------------------|-----|------|
| PREP1 | t <sub>w</sub> (CAP)   | Pulse Duration, CAP (asynchronous)   | 2P <sup>(1)</sup> + 2 |     | ns   |
| PREP2 | t <sub>w</sub> (SYNCl) | Pulse Duration, SYNCl (asynchronous) | 2P <sup>(1)</sup> + 2 |     | ns   |

(1) P = CORE\_CLK period in ns.

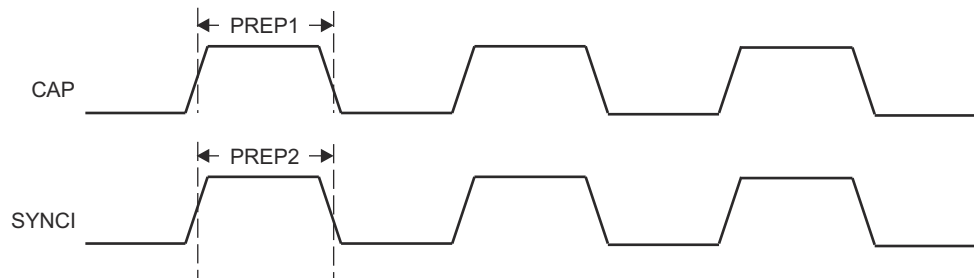


図 6-103. PRU\_ICSSG ECAP Timing

表 6-127. PRU\_ICSSG ECAP Switching Characteristics

see 図 6-104

| NO.   | PARAMETER              | DESCRIPTION                          | MIN                   | MAX | UNIT |
|-------|------------------------|--------------------------------------|-----------------------|-----|------|
| PREP3 | t <sub>w</sub> (APWM)  | Pulse Duration, APWM high/low        | 2P <sup>(1)</sup> - 2 |     | ns   |
| PREP4 | t <sub>w</sub> (SYNCO) | Pulse Duration, SYNCO (asynchronous) | P <sup>(1)</sup> - 2  |     | ns   |

(1) P = CORE\_CLK period in ns.

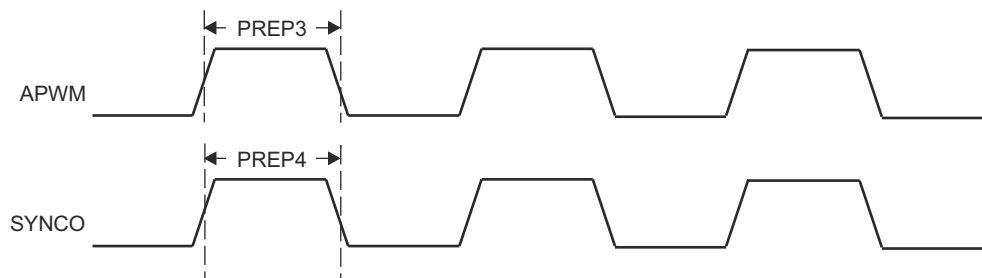


図 6-104. PRU\_ICSSG ECAP Switching Characteristics

#### 6.10.5.16.6 PRU\_ICSSG RGMII, MII\_RT, and Switch

For more information, see *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in *Processors and Accelerators* chapter in the device TRM.

##### 6.10.5.16.6.1 PRU\_ICSSG MDIO Timing

表 6-128, 表 6-129, 表 6-130, and 図 6-105 present timing conditions, requirements, and switching characteristics for PRU\_ICSSG MDIO.

**表 6-128. PRU\_ICSSG MDIO Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 10  | 470 | pF   |

**表 6-129. PRU\_ICSSG MDIO Timing Requirements**

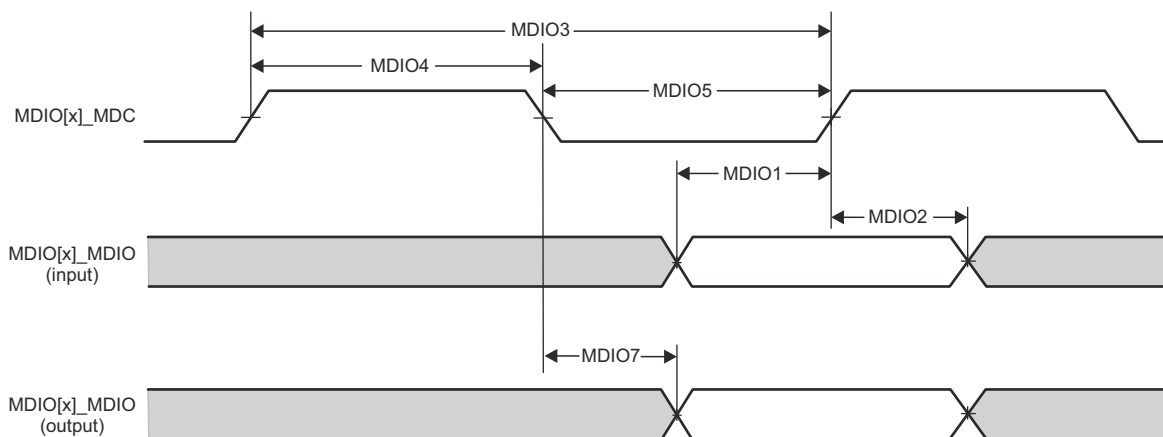
see 図 6-105

| NO.   | PARAMETER                  |                                                        | MIN | MAX | UNIT |
|-------|----------------------------|--------------------------------------------------------|-----|-----|------|
| MDIO1 | t <sub>su</sub> (MDIO_MDC) | Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high | 90  |     | ns   |
| MDIO2 | t <sub>h</sub> (MDC_MDIO)  | Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high   | 0   |     | ns   |

**表 6-130. PRU\_ICSSG MDIO Switching Characteristics**

see 図 6-105

| NO.   | PARAMETER                 |                                                   | MIN  | MAX | UNIT |
|-------|---------------------------|---------------------------------------------------|------|-----|------|
| MDIO3 | t <sub>c</sub> (MDC)      | Cycle time, MDIO[x]_MDC                           | 400  |     | ns   |
| MDIO4 | t <sub>w</sub> (MDCH)     | Pulse Duration, MDIO[x]_MDC high                  | 160  |     | ns   |
| MDIO5 | t <sub>w</sub> (MDCL)     | Pulse Duration, MDIO[x]_MDC low                   | 160  |     | ns   |
| MDIO7 | t <sub>d</sub> (MDC_MDIO) | Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid | -150 | 150 | ns   |



CPSW2G\_MDIO\_TIMING\_01

**図 6-105. PRU\_ICSSG MDIO Timing Requirements and Switching Characteristics**

## 6.10.5.16.6.2 PRU\_ICSSG MII Timing

## 注

In order to ensure the MII\_G\_RT I/O timing values published in the device data sheet, the PRU\_ICSSG ICSSGn\_CORE\_CLK (where n = 0 to 1) core clock must be configured for 200 MHz, 225 MHz, or 250 MHz and the TX\_CLK\_DELAYn (where n = 0 or 1) bit field in the ICSSG\_TXCFG0/1 register must be set to 0h (default value).

表 6-131, 表 6-132, 図 6-106, 表 6-133, 図 6-107, 表 6-134, 図 6-108, 表 6-135, and 図 6-109 present timing conditions, requirements, and switching characteristics for PRU\_ICSSG MII.

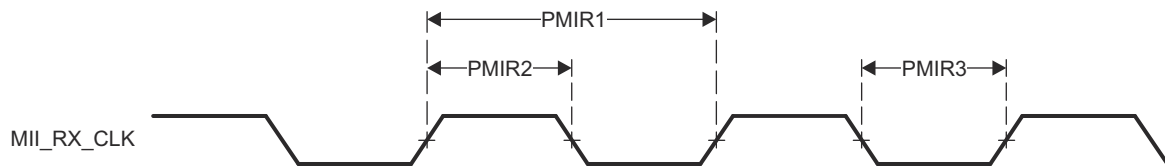
表 6-131. PRU\_ICSSG MII Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 20  | pF   |

表 6-132. PRU\_ICSSG MII Timing Requirements – MII[x]\_RX\_CLK

see 図 6-106

| NO.   | PARAMETER                | DESCRIPTION                        | MODE     | MIN    | MAX    | UNIT |
|-------|--------------------------|------------------------------------|----------|--------|--------|------|
| PMIR1 | t <sub>c</sub> (RX_CLK)  | Cycle time, MII[x]_RX_CLK          | 10 Mbps  | 399.96 | 400.04 | ns   |
|       |                          |                                    | 100 Mbps | 39.996 | 40.004 | ns   |
| PMIR2 | t <sub>w</sub> (RX_CLKH) | Pulse Duration, MII[x]_RX_CLK High | 10 Mbps  | 140    | 260    | ns   |
|       |                          |                                    | 100 Mbps | 14     | 26     | ns   |
| PMIR3 | t <sub>w</sub> (RX_CLKL) | Pulse Duration, MII[x]_RX_CLK Low  | 10 Mbps  | 140    | 260    | ns   |
|       |                          |                                    | 100 Mbps | 14     | 26     | ns   |



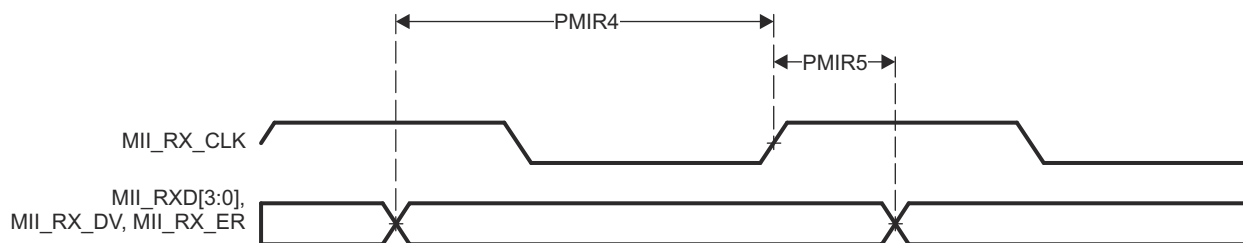
PRU\_MII\_RT\_TIMING\_04

図 6-106. PRU\_ICSSG MII[x]\_RX\_CLK Timing

**表 6-133. PRU\_ICSSG MII Timing Requirements – MII[x]\_RXD[3:0], MII[x]\_RX\_DV, and MII[x]\_RX\_ER**

see 図 6-107

| NO.   | PARAMETER                | DESCRIPTION                                            | MODE     | MIN | MAX | UNIT |
|-------|--------------------------|--------------------------------------------------------|----------|-----|-----|------|
| PMIR4 | $t_{su}(RXD-RX\_CLK)$    | Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK | 10 Mbps  | 8   |     | ns   |
|       | $t_{su}(RX\_DV-RX\_CLK)$ | Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
|       | $t_{su}(RX\_ER-RX\_CLK)$ | Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
|       | $t_{su}(RXD-RX\_CLK)$    | Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK | 100 Mbps | 8   |     | ns   |
|       | $t_{su}(RX\_DV-RX\_CLK)$ | Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
|       | $t_{su}(RX\_ER-RX\_CLK)$ | Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
| PMIR5 | $t_h(RX\_CLK-RXD)$       | Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK   | 10 Mbps  | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_DV)$    | Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_ER)$    | Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RXD)$       | Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK   | 100 Mbps | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_DV)$    | Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_ER)$    | Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK      |          | 8   |     | ns   |

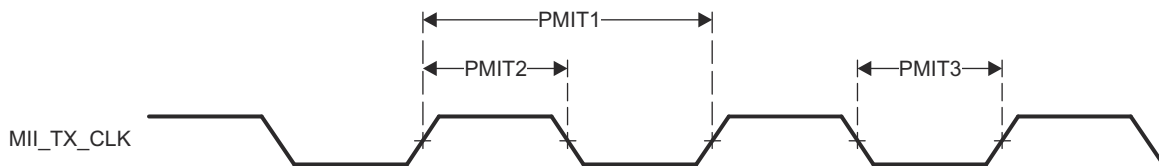


**図 6-107. PRU\_ICSSG MII[x]\_RXD[3:0], MII[x]\_RX\_DV, and MII[x]\_RX\_ER Timing**

**表 6-134. PRU\_ICSSG MII Timing Requirements – MII[x]\_TX\_CLK**

see 図 6-108

| NO.   | PARAMETER       | DESCRIPTION                        | MODE     | MIN    | MAX    | UNIT |
|-------|-----------------|------------------------------------|----------|--------|--------|------|
| PMIT1 | $t_c(TX\_CLK)$  | Cycle time, MII[x]_TX_CLK          | 10 Mbps  | 399.96 | 400.04 | ns   |
|       |                 |                                    | 100 Mbps | 39.996 | 40.004 | ns   |
| PMIT2 | $t_w(TX\_CLKH)$ | Pulse Duration, MII[x]_TX_CLK High | 10 Mbps  | 140    | 260    | ns   |
|       |                 |                                    | 100 Mbps | 14     | 26     | ns   |
| PMIT3 | $t_w(TX\_CLKL)$ | Pulse Duration, MII[x]_TX_CLK Low  | 10 Mbps  | 140    | 260    | ns   |
|       |                 |                                    | 100 Mbps | 14     | 26     | ns   |

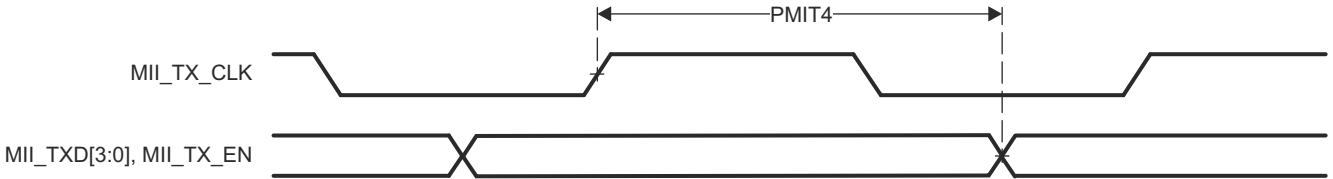


**図 6-108. PRU\_ICSSG MII[x]\_TX\_CLK Timing**

表 6-135. PRU\_ICSSG MII Switching Characteristics – MII[x]\_TXD[3:0] and MII[x]\_TX\_EN

see  6-109

| NO.   | PARAMETER             | DESCRIPTION                                             | MODE     | MIN | MAX | UNIT |
|-------|-----------------------|---------------------------------------------------------|----------|-----|-----|------|
| PMIT4 | $t_d(TX\_CLK-TXD)$    | Delay time, MII[x]_TX_CLK High to MII[x]_TXD[3:0] valid | 10 Mbps  | 0   | 25  | ns   |
|       | $t_d(TX\_CLK-TX\_EN)$ | Delay time, MII[x]_TX_CLK to MII[x]_TX_EN valid         |          | 0   | 25  | ns   |
|       | $t_d(TX\_CLK-TXD)$    | Delay time, MII[x]_TX_CLK High to MII[x]_TXD[3:0] valid | 100 Mbps | 0   | 25  | ns   |
|       | $t_d(TX\_CLK-TX\_EN)$ | Delay time, MII[x]_TX_CLK to MII[x]_TX_EN valid         |          | 0   | 25  | ns   |



 6-109. PRU\_ICSSG MII[x]\_TXD[3:0], MII[x]\_TX\_EN Timing

### 6.10.5.16.6.3 PRU\_ICSSG RGMII Timing

表 6-136, 表 6-137, 表 6-138, 図 6-110, 表 6-139, 表 6-140, and 図 6-111 present timing conditions, requirements, and switching characteristics for PRU\_ICSSG RGMII.

**表 6-136. PRU\_ICSSG RGMII Timing Conditions**

| PARAMETER                             |                                              |                                                       | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|-------------------------------------------------------|------|-----|------|
| INPUT CONDITIONS                      |                                              |                                                       |      |     |      |
| SR <sub>I</sub>                       | Input slew rate                              | VDD = 1.8V                                            | 1.44 | 5   | V/ns |
|                                       |                                              | VDD = 3.3V                                            | 2.65 | 5   | V/ns |
| OUTPUT CONDITIONS                     |                                              |                                                       |      |     |      |
| C <sub>L</sub>                        | Output load capacitance                      |                                                       | 2    | 20  | pF   |
| PCB CONNECTIVITY REQUIREMENTS         |                                              |                                                       |      |     |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | RGMII[x]_RXC,<br>RGMII[x]_RD[3:0],<br>RGMII[x]_RX_CTL |      | 50  | ps   |
|                                       |                                              | RGMII[x]_TXC,<br>RGMII[x]_TD[3:0],<br>RGMII[x]_TX_CTL |      | 50  | ps   |

**表 6-137. PRU\_ICSSG RGMII Timing Requirements – RGMII[x]\_RXC**

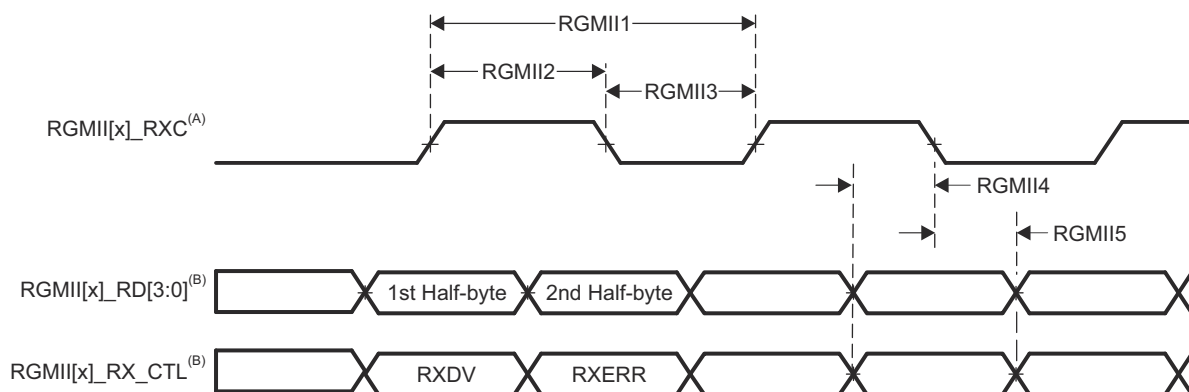
see 図 6-110

| NO.    | PARAMETER     | DESCRIPTION                       | MODE      | MIN | MAX | UNIT |
|--------|---------------|-----------------------------------|-----------|-----|-----|------|
| RGMII1 | $t_{c(RXC)}$  | Cycle time, RGMII[x]_RXC          | 10 Mbps   | 360 | 440 | ns   |
|        |               |                                   | 100 Mbps  | 36  | 44  | ns   |
|        |               |                                   | 1000 Mbps | 7.2 | 8.8 | ns   |
| RGMII2 | $t_{w(RXCH)}$ | Pulse duration, RGMII[x]_RXC high | 10 Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100 Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000 Mbps | 3.6 | 4.4 | ns   |
| RGMII3 | $t_{w(RXCL)}$ | Pulse duration, RGMII[x]_RXC low  | 10 Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100 Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000 Mbps | 3.6 | 4.4 | ns   |

**表 6-138. PRU\_ICSSG RGMII Timing Requirements – RGMII[x]\_RD[3:0] and RGMII[x]\_RX\_CTL**

see 図 6-110

| NO.    | PARAMETER             | DESCRIPTION                                                    | MODE      | MIN | MAX | UNIT |
|--------|-----------------------|----------------------------------------------------------------|-----------|-----|-----|------|
| RGMII4 | $t_{su(RD-RXC)}$      | Setup time, RGMII[x]_RD[3:0] valid before RXC high/low         | 10 Mbps   | 1   |     | ns   |
|        |                       |                                                                | 100 Mbps  | 1   |     | ns   |
|        |                       |                                                                | 1000 Mbps | 1   |     | ns   |
|        | $t_{su(RX\_CTL-RXC)}$ | Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low | 10 Mbps   | 1   |     | ns   |
|        |                       |                                                                | 100 Mbps  | 1   |     | ns   |
|        |                       |                                                                | 1000 Mbps | 1   |     | ns   |
| RGMII5 | $t_h(RXC-RD)$         | Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low  | 10 Mbps   | 1   |     | ns   |
|        |                       |                                                                | 100 Mbps  | 1   |     | ns   |
|        |                       |                                                                | 1000 Mbps | 1   |     | ns   |
|        | $t_h(RXC-RX\_CTL)$    | Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low   | 10 Mbps   | 1   |     | ns   |
|        |                       |                                                                | 100 Mbps  | 1   |     | ns   |
|        |                       |                                                                | 1000 Mbps | 1   |     | ns   |



- A. RGMII[x]\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII[x]\_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_RXC and data bits 7-4 on the falling edge of RGMII[x]\_RXC. Similarly, RGMII[x]\_RX\_CTL carries RXDV on rising edge of RGMII[x]\_RXC and RXERR on falling edge of RGMII[x]\_RXC.

**図 6-110. PRU\_ICSSG RGMII[x]\_RXC, RGMII[x]\_RD[3:0], RGMII[x]\_RX\_CTL Timing Requirements - RGMII Mode**

**表 6-139. PRU\_ICSSG RGMII Switching Characteristics – RGMII[x]\_TXC**

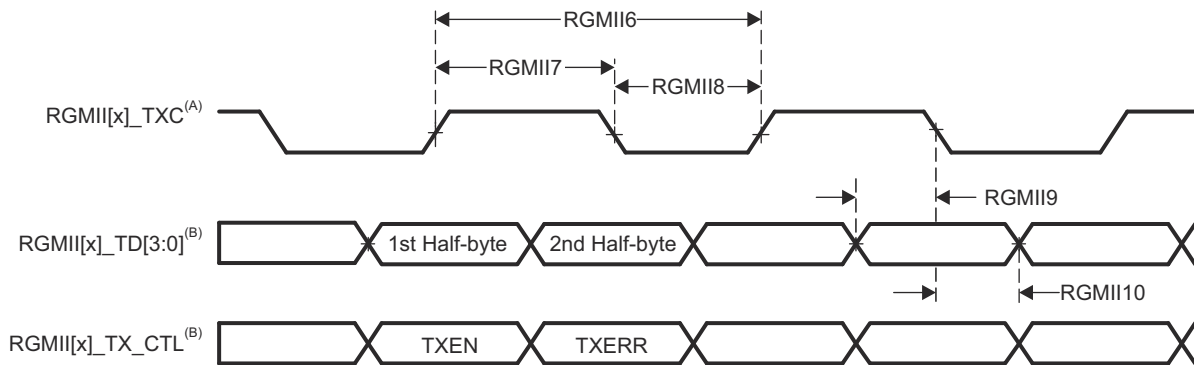
see 図 6-111

| NO.    | PARAMETER     | DESCRIPTION                       | MODE      | MIN | MAX | UNIT |
|--------|---------------|-----------------------------------|-----------|-----|-----|------|
| RGMII6 | $t_{c(TXC)}$  | Cycle time, RGMII[x]_TXC          | 10 Mbps   | 360 | 440 | ns   |
|        |               |                                   | 100 Mbps  | 36  | 44  | ns   |
|        |               |                                   | 1000 Mbps | 7.2 | 8.8 | ns   |
| RGMII7 | $t_{w(TXCH)}$ | Pulse duration, RGMII[x]_TXC high | 10 Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100 Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000 Mbps | 3.6 | 4.4 | ns   |
| RGMII8 | $t_{w(TXCL)}$ | Pulse duration, RGMII[x]_TXC low  | 10 Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100 Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000 Mbps | 3.6 | 4.4 | ns   |

**表 6-140. PRU\_ICSSG RGMII Switching Characteristics – RGMII[x]\_TD[3:0] and RGMII[x]\_TX\_CTL**

see 図 6-111

| NO.     | PARAMETER              | DESCRIPTION                                                           | MODE      | MIN | MAX | UNIT |
|---------|------------------------|-----------------------------------------------------------------------|-----------|-----|-----|------|
| RGMII9  | $t_{osu(TD-TXC)}$      | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low    | 10 Mbps   | 1.2 |     | ns   |
|         |                        |                                                                       | 100 Mbps  | 1.2 |     | ns   |
|         |                        |                                                                       | 1000 Mbps | 1.2 |     | ns   |
|         | $t_{osu(TX\_CTL-TXC)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low     | 10 Mbps   | 1.2 |     | ns   |
|         |                        |                                                                       | 100 Mbps  | 1.2 |     | ns   |
|         |                        |                                                                       | 1000 Mbps | 1.2 |     | ns   |
| RGMII10 | $t_{oh(TXC-TD)}$       | Output setup time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low | 10 Mbps   | 1.2 |     | ns   |
|         |                        |                                                                       | 100 Mbps  | 1.2 |     | ns   |
|         |                        |                                                                       | 1000 Mbps | 1.2 |     | ns   |
|         | $t_{oh(TXC-TX\_CTL)}$  | Output setup time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low  | 10 Mbps   | 1.2 |     | ns   |
|         |                        |                                                                       | 100 Mbps  | 1.2 |     | ns   |
|         |                        |                                                                       | 1000 Mbps | 1.2 |     | ns   |



- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII[x]\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_TXC and data bits 7-4 on the falling edge of RGMII[x]\_TXC. Similarly, RGMII[x]\_TX\_CTL carries TXEN on rising edge of RGMII[x]\_TXC and TXERR on falling edge of RGMII[x]\_TXC.

**図 6-111. PRU\_ICSSG RGMII[x]\_TXC, RGMII[x]\_TD[3:0], and RGMII[x]\_TX\_CTL Switching Characteristics - RGMII Mode**

### 6.10.5.17 Timers

For more details about features and additional description information on the device Timers, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**表 6-141. Timer Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 10  | pF   |

**表 6-142. Timer Input Timing Requirements**

see 図 6-112

| NO. | PARAMETER             | DESCRIPTION          | MODE    | MIN                   | MAX | UNIT |
|-----|-----------------------|----------------------|---------|-----------------------|-----|------|
| T1  | t <sub>w(TINPH)</sub> | Pulse duration, high | CAPTURE | 2 + 4P <sup>(1)</sup> |     | ns   |
| T2  | t <sub>w(TINPL)</sub> | Pulse duration, low  | CAPTURE | 2 + 4P <sup>(1)</sup> |     | ns   |

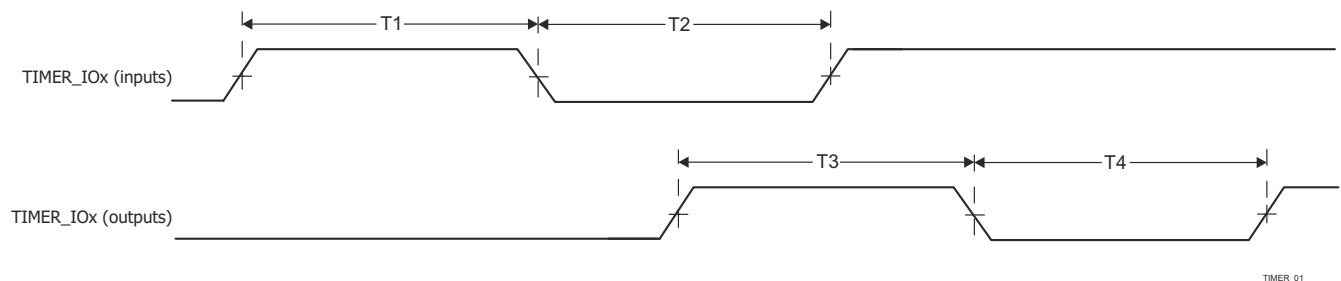
(1) P = functional clock period in ns.

**表 6-143. Timer Output Switching Characteristics**

see 図 6-112

| NO. | PARAMETER             | DESCRIPTION          | MODE | MIN                    | MAX | UNIT |
|-----|-----------------------|----------------------|------|------------------------|-----|------|
| T3  | t <sub>w(TOUTH)</sub> | Pulse duration, high | PWM  | -2 + 4P <sup>(1)</sup> |     | ns   |
| T4  | t <sub>w(TOUTL)</sub> | Pulse duration, low  | PWM  | -2 + 4P <sup>(1)</sup> |     | ns   |

(1) P = functional clock period in ns.



**図 6-112. Timer Timing Requirements and Switching Characteristics**

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

### 6.10.5.18 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**表 6-144. UART Timing Conditions**

| PARAMETER                |                         | MIN | MAX               | UNIT |
|--------------------------|-------------------------|-----|-------------------|------|
| <b>INPUT CONDITIONS</b>  |                         |     |                   |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 5                 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |                   |      |
| C <sub>L</sub>           | Output load capacitance | 1   | 30 <sup>(1)</sup> | pF   |

- (1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

**表 6-145. UART Timing Requirements**

see 図 6-113

| NO. | PARAMETER            | DESCRIPTION                               | MIN                         | MAX                         | UNIT |
|-----|----------------------|-------------------------------------------|-----------------------------|-----------------------------|------|
| 1   | t <sub>w(RXD)</sub>  | Pulse width, receive data bit high or low | 0.95U <sup>(1)</sup><br>(2) | 1.05U <sup>(1)</sup><br>(2) | ns   |
| 2   | t <sub>w(RXDS)</sub> | Pulse width, receive start bit low        | 0.95U <sup>(1)</sup><br>(2) |                             | ns   |

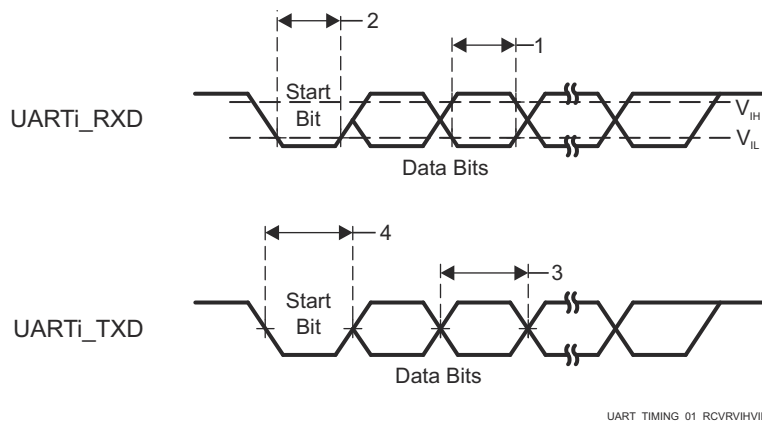
- (1) U = UART baud time in ns = 1/programmed baud rate.  
(2) This value defines the data valid time, where the input voltage is required to be above V<sub>IH</sub> or below V<sub>IL</sub>.

**表 6-146. UART Switching Characteristics**

see 図 6-113

| NO. | PARAMETER            | DESCRIPTION                                  | MIN                    | MAX                    | UNIT |
|-----|----------------------|----------------------------------------------|------------------------|------------------------|------|
|     | f <sub>(baud)</sub>  | Programmable baud rate for Main Domain UARTs |                        | 12                     | Mbps |
|     |                      | Programmable baud rate for MCU Domain UARTs  |                        | 3.7                    | Mbps |
| 3   | t <sub>w(TXD)</sub>  | Pulse width, transmit data bit high or low   | U <sup>(1)</sup> - 2.2 | U <sup>(1)</sup> + 2.2 | ns   |
| 4   | t <sub>w(TXDS)</sub> | Pulse width, transmit start bit low          | U <sup>(1)</sup> - 2.2 |                        | ns   |

- (1) U = UART baud time in ns = 1/programmed baud rate.



**図 6-113. UART Timing Requirements and Switching Characteristics**

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.19 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the *SERDES0 Signal Descriptions* and the corresponding subsection within *Detailed Description*.

## 6.10.6 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

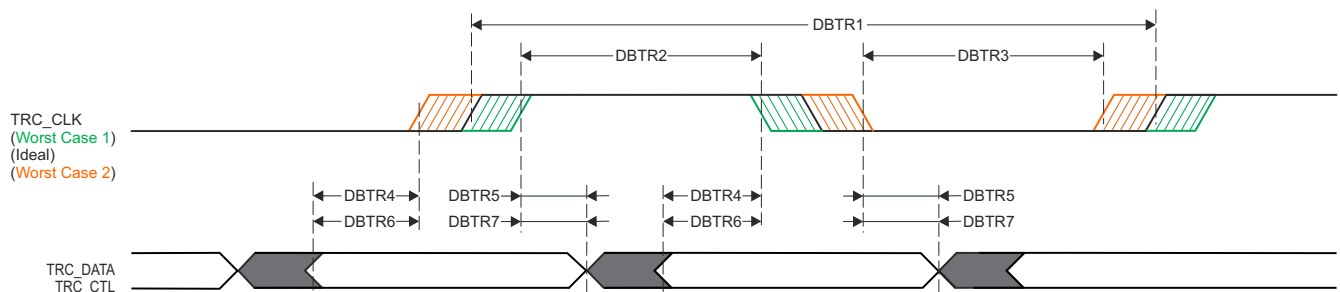
### 6.10.6.1 Trace

**表 6-147. Trace Timing Conditions**

| PARAMETER                            |                                              |                | MIN | MAX | UNIT |
|--------------------------------------|----------------------------------------------|----------------|-----|-----|------|
| <b>OUTPUT CONDITIONS</b>             |                                              |                |     |     |      |
| $C_L$                                | Output load capacitance                      |                | 2   | 5   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                              |                |     |     |      |
| $t_d$ (Trace Mismatch)               | Propagation delay mismatch across all traces | VDDSHV3 = 1.8V |     | 200 | ps   |
|                                      |                                              | VDDSHV3 = 3.3V |     | 100 | ps   |

**表 6-148. Trace Switching Characteristics**

| NO.       | PARAMETER                            |                                                    | MIN  | MAX | UNIT |
|-----------|--------------------------------------|----------------------------------------------------|------|-----|------|
| 1.8V Mode |                                      |                                                    |      |     |      |
| DBTR1     | t <sub>c</sub> (TRC_CLK)             | Cycle time, TRC_CLK                                | 6.50 |     | ns   |
| DBTR2     | t <sub>w</sub> (TRC_CLKH)            | Pulse width, TRC_CLK high                          | 2.50 |     | ns   |
| DBTR3     | t <sub>w</sub> (TRC_CLKL)            | Pulse width, TRC_CLK low                           | 2.50 |     | ns   |
| DBTR4     | t <sub>osu</sub> (TRC_DATAV-TRC_CLK) | Output setup time, TRC_DATA valid to TRC_CLK edge  | 0.81 |     | ns   |
| DBTR5     | t <sub>oh</sub> (TRC_CLK-TRC_DATAI)  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 0.81 |     | ns   |
| DBTR6     | t <sub>osu</sub> (TRC_CTLV-TRC_CLK)  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 0.81 |     | ns   |
| DBTR7     | t <sub>oh</sub> (TRC_CLK-TRC_CTLI)   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 0.81 |     | ns   |
| 3.3V Mode |                                      |                                                    |      |     |      |
| DBTR1     | t <sub>c</sub> (TRC_CLK)             | Cycle time, TRC_CLK                                | 8.67 |     | ns   |
| DBTR2     | t <sub>w</sub> (TRC_CLKH)            | Pulse width, TRC_CLK high                          | 3.58 |     | ns   |
| DBTR3     | t <sub>w</sub> (TRC_CLKL)            | Pulse width, TRC_CLK low                           | 3.58 |     | ns   |
| DBTR4     | t <sub>osu</sub> (TRC_DATAV-TRC_CLK) | Output setup time, TRC_DATA valid to TRC_CLK edge  | 1.08 |     | ns   |
| DBTR5     | t <sub>oh</sub> (TRC_CLK-TRC_DATAI)  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 1.08 |     | ns   |
| DBTR6     | t <sub>osu</sub> (TRC_CTLV-TRC_CLK)  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 1.08 |     | ns   |
| DBTR7     | t <sub>oh</sub> (TRC_CLK-TRC_CTLI)   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 1.08 |     | ns   |



SPRSP08\_Debug\_01

**図 6-114. Trace Switching Characteristics**

## 6.10.6.2 JTAG

表 6-149. JTAG Timing Conditions

| PARAMETER                             |                                              | MIN  | MAX                 | UNIT |
|---------------------------------------|----------------------------------------------|------|---------------------|------|
| <b>INPUT CONDITIONS</b>               |                                              |      |                     |      |
| SR <sub>I</sub>                       | Input slew rate                              | 0.5  | 2.0                 | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |      |                     |      |
| C <sub>L</sub>                        | Output load capacitance                      | 5    | 15                  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |      |                     |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 83.5 | 1000 <sup>(1)</sup> | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |      | 100                 | ps   |

- (1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

表 6-150. JTAG Timing Requirements

see 図 6-115

| NO. |                           |                                                  | MIN                 | MAX | UNIT |
|-----|---------------------------|--------------------------------------------------|---------------------|-----|------|
| J1  | t <sub>c</sub> (TCK)      | Cycle time minimum, TCK                          | 45.5 <sup>(1)</sup> |     | ns   |
| J2  | t <sub>w</sub> (TCKH)     | Pulse width minimum, TCK high                    | 0.4P <sup>(2)</sup> |     | ns   |
| J3  | t <sub>w</sub> (TCKL)     | Pulse width minimum, TCK low                     | 0.4P <sup>(2)</sup> |     | ns   |
| J4  | t <sub>su</sub> (TDI-TCK) | Input setup time minimum, TDI valid to TCK high  | 4                   |     | ns   |
|     | t <sub>su</sub> (TMS-TCK) | Input setup time minimum, TMS valid to TCK high  | 4                   |     | ns   |
| J5  | t <sub>h</sub> (TCK-TDI)  | Input hold time minimum, TDI valid from TCK high | 2                   |     | ns   |
|     | t <sub>h</sub> (TCK-TMS)  | Input hold time minimum, TMS valid from TCK high | 2                   |     | ns   |

- (1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristics for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 2.2 ns relative to the rising edge of TCK
  - TDI and TMS output delay in the range of -16.1 ns to 14.1 ns relative to the falling edge of TCK
- (2) P = TCK cycle time in ns

表 6-151. JTAG Switching Characteristics

see 図 6-115

| NO. |                            | PARAMETER                                  | MIN | MAX | UNIT |
|-----|----------------------------|--------------------------------------------|-----|-----|------|
| J6  | t <sub>d</sub> (TCKL-TDOI) | Delay time minimum, TCK low to TDO invalid | 0   |     | ns   |
| J7  | t <sub>d</sub> (TCKL-TDOV) | Delay time maximum, TCK low to TDO valid   |     | 14  | ns   |

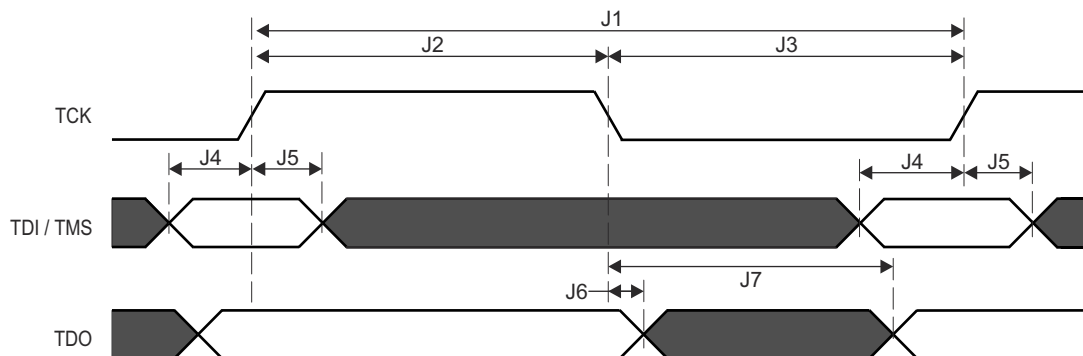


図 6-115. JTAG Timing Requirements and Switching Characteristics

## 7 Detailed Description

### 7.1 Overview

AM64x is an extension of the Sitara™ industrial-grade family of heterogeneous Arm processors. AM64x is built for industrial applications, such as motor drives and programmable logic controllers (PLCs), which require a unique combination of real-time processing and communications with applications processing. AM64x combines two instances of Sitara's gigabit TSN-enabled PRU-ICSSG, up to two Arm Cortex-A53 cores, up to four Cortex-R5F MCUs, and a Cortex-M4F MCU domain.

AM64x is architected to provide real-time performance through the high-performance R5Fs, Tightly-Coupled Memory banks, configurable SRAM partitioning, and low-latency paths to and from peripherals for rapid data movement in and out of the SoC. This deterministic architecture allows for AM64x to handle the tight control loops found in servo drives, while the peripherals like FSI, GPMC, PWMs, sigma delta decimation filters, and absolute encoder interfaces help enable a number of different architectures found in these systems.

The Cortex-A53s provide the powerful computing elements necessary for Linux applications. Linux, and Real-time (RT) Linux, is provided through TI's Processor SDK Linux which stays updated to the latest Long Term Support (LTS) Linux kernel, bootloader and Yocto file system on an annual basis. AM64x helps bridge the Linux world with the real-time world by enabling isolation between Linux applications and real-time streams through configurable memory partitioning. The Cortex-A53s can be assigned to work strictly out of DDR for Linux, and the internal SRAM can be broken up into various sizes for the Cortex-R5Fs to use together or independently.

The PRU\_ICSSG in AM64x provides the flexible industrial communications capability necessary to run gigabit TSN, EtherCAT, PROFINET, EtherNet/IP, and various other protocols. In addition, the PRU\_ICSSG also enables additional interfaces in the SoC including sigma delta decimation filter modules and absolute encoder interfaces.

Functional safety features can be enabled through the MCU domain with an integrated Cortex-M4F and dedicated peripheral set which can all be shared or isolated from the rest of the SoC. AM64x also supports secure boot.

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#### 注

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

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## 7.2 Processor Subsystems

### 7.2.1 Arm Cortex-A53 Subsystem

The A53SS module supports the following features:

- Dual Core A53 Cluster
  - Full ARM v8-A Architecture Compliant
- AArch32 and AArch64 Execution States
- All exception levels EL0-3
- A32 Instruction Set (Previously ARM instruction set)
- T32 instruction set (previously Thumb instruction set)
- A64 Instruction Set
  - Advanced SIMD and Floating Point Extensions (NEON)
  - ARMv8 Cryptography Extensions
  - ARMv8 Cryptography Extensions
  - ARM GICv3 architecture
  - In-order pipeline with symmetric dual-issue of most instructions
  - Harvard L1 with system MMU
- 32 KB Instruction Cache
- 32 KB Data Cache
  - 256KB Shared L2 Cache
  - Generic Timer(s)
  - Debug
- 128-Bit VBUSM Initiator Interfaces (for axi\_r and axi\_r channels)
- 128-Bit VBUSM Target Interface (for Accelerator Coherency Port)
- 64-bit Grey-coded system input time
- 48-bit Grey-coded debug input time
- 32-bit VBUSP Target Interface for Debug
- Integrated PBIST Controller with BISTOR

For more information, see *Dual-A53 MPU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

### 7.2.2 Arm Cortex-R5F Subsystem (R5FSS)

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for dual/single-core operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC.

#### 注

The Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating Point Unit (FPU) extension.

For more information, see *Dual-R5F Subsystem (R5FSS)* section in *Processors and Accelerators* chapter in the device TRM.

### 7.2.3 Arm Cortex-M4F (M4FSS)

The M4FSS module on the AM64x device provides a safety channel (secondary channel - working in conjunction with an external microcontroller)- or- a general purpose MCU.

The M4FSS module supports the following features:

- Cortex M4F With MPU
- ARMv7-M architecture
- Support for Nested Vectored Interrupt Controller (NVIC) with 64 inputs

- Ability to executed code from internal or external memories
- 192 KB of SRAM (I-Code)
- 64 KB of SRAM (D-Code)
- External access to internal memories if allowed
- Debug Support Including:
  - DAP based Debug to the CPU Core
  - Full Debug Features of CPU Core are enabled
  - Standard ITM trace
  - CTM Cross Trigger
  - ETM Trace Support
- Fault Detection and Correction
  - SECEDED ECC protection on I-CODE
  - SECEDED ECC protection on D-CODE
  - Fault Error Interrupt Output

For more information, see *Arm Cortex M4F Subsystem (M4FSS)* section in *Processors and Accelerators* chapter in the device TRM.

## 7.3 Accelerators and Coprocessors

### 7.3.1 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU\_ICSSG)

The PRU\_ICSSG module supports the following main features:

- 3x PRUs
  - General-Purpose PRU (PRU)
  - Real-Time PRU(RTU\_PRU)
  - Transmit PRU (TX\_PRU)
- 2x Ethernet MII\_G\_RT configurable connection to PRUs
  - Up to 2x RGMII ports
  - Up to 2x MII ports
  - RX Classifier
- 2x Industrial Ethernet Peripheral (IEP) to manage and generate industrial Ethernet functions
- 2x Industrial Ethernet 64-bit timers, each with 10 capture and 16 compare events, along with slow and fast compensation.
- 1x MDIO
- 1x UART, with a dedicated 192-MHz clock input
- Supports up to 4 sets of 3-phased motor control, with 12 primary and 12 complimentary programmable PWM outputs.
- Supports up to 9 safety events with optional external trip I/O per PWM set with hardware glitch filter.
- 1x Enhanced Capture Module (ECAP)
- 1x Interrupt Controller (INTC)
  - 160 input events supported – 96 external, 64 internal
- Flexible power management support
- Integrated switched central resource with programmable priority
- All memories support ECC

For more information, see *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in *Processors and Accelerators* chapter in the device TRM.

## 7.4 Other Subsystems

### 7.4.1 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers accessed via a standard non-coherent bus fabric. The PDMA module is intended to be located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (UDMA-P + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

There are five PDMA modules in the device.

For more information, see *PDMA Controller* section in *DMA Controllers* chapter in the device TRM.

## **7.4.2 Peripherals**

### **7.4.2.1 ADC**

The analog-to-digital converter (ADC) module is a single-channel general purpose analog-to-digital converter with an 8-input analog multiplexer, which supports 12-bit conversion samples from an analog front end (AFE).

There is one ADC module in the device.

For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

### **7.4.2.2 DCC**

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programmed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

The device has seven instances of DCC modules.

For more information, see *Dual Clock Comparator (DCC)* section in *Peripherals* chapter in the device TRM.

### **7.4.2.3 Dual Data Rate (DDR) External Memory Interface (DDRSS)**

Integrated in MAIN domain: one instance of DDR Subsystem (DDRSS) is used as an interface to external RAM devices which can be utilized for storing program or data. DDRSS provides the following main features:

- Support of DDR4 / LPDDR4 memory types
- 16-bit memory bus interface with in-line ECC
- System bus interface: little Endian only with 128-bit data width
- Configuration bus Interface: little Endian only with 32-bit data width
- Support of dual rank configuration
- Support of automatic idle power saving mode when no or low activity is detected
- Class of Service (CoS) - three latency classes supported
- Prioritized refresh scheduling
- Statistical counters for performance management

For more information, see *DDR Subsystem (DDRSS)* section in *Peripherals* chapter in the device TRM.

### **7.4.2.4 ECAP**

This section describes the Enhanced Capture (ECAP) module for the device.

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

### **7.4.2.5 EPWM**

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWM\_x instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

Additionally, the EPWM integration allows this synchronization scheme to be extended to the capture peripheral modules (ECAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

The device has six instances of EPWM modules.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.6 ELM

The Error Location Module (ELM) is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

The General-Purpose Memory Controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The ELM extracts error addresses from these syndrome polynomials.

For more information, see *Error Location Module (ELM)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.7 ESM

The Error Signaling Module (ESM) aggregates safety-related events and/or errors from throughout the device into one location. The module can signal both low and high priority interrupts to a processor to deal with a safety event and/or manipulate an I/O error pin to signal external hardware that an error has occurred. This allows an external controller to reset the device or keep the system in safe, known state.

For more information, see *Error Signaling Module (ESM)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.8 GPIO

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.9 EQEP

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a

reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vice versa.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel can be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 KHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.10 General-Purpose Memory Controller (GPMC)

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.11 I2C

The Inter-IC Bus (I2C) interface is implemented using the mshsi2c module. This peripheral implements the multi-controller I2C bus, which allows serial transfer of 8-bit data to and from other I2C controller and target devices, through a two-wire interface.

The I2C module supports the following main features:

- Compliant with Philips I2C specification version 2.1
- Supported Speeds:
  - Standard mode (up to 100 K bits/s)
  - Fast mode (up to 400 K bits/s)
  - High-speed mode (up to 3.4 M bits/s), I2C0 and MCU\_I2C0 only
- Multi-controller transmitter and target receiver mode
- Multi-controller receiver and target transmitter mode
- Combined controller transmit/receive and receive/transmit modes
- 7-bit and 10-bit device addressing modes
- Built-in 32-byte FIFO for buffered read or write
- Programmable multi-target channel (responds to 4 separates addresses)
- Programmable clock generation
- Support for asynchronous wake-up
- One interrupt line

For more information, see *Inter-Integrated Circuit (I2C) Interface* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.12 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The device supports 2 MCAN modules

For more information, see *Modular Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.13 MCRC Controller

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

For more information, see *MCRC Controller* section in *Interprocessor Communication* chapter in the device TRM.

#### 7.4.2.14 MCSPI

The MCSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

There are total of seven MCSPI modules in the device.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.15 MMCSD

There are two Multi-Media Card/Secure Digital (MMCSD) modules inside the device - MMCSD0 and MMCSD1. Each MMCSD module includes one MMCSD Host Controller, where MMCSD0 is associated with MMC0 and MMCSD1 is associated with MMC1.

The MMCSD Host Controller supports:

- One controller with 8-bit wide data bus
- One controller with 4-bit wide data bus
- Support of eMMC5.1 Host Specification (JESD84-B51)
- Support of SD Host Controller Standard Specification - SDIO 3.00
- Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3
- eMMC Electrical Standard 5.1 (JESD84-B51)
- Multi-Media card features:
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR: 1.8 V, 8/4/1-bit bus width, 0-25 MHz, 25/12.5/3.125 MB/s
  - High Speed SDR: 1.8 V, 8/4/1-bit bus width, 0-50 MHz, 50/25/6.25 MB/s
  - High Speed DDR: 1.8 V, 8/4-bit bus width, 0-50 MHz, 100/50 MB/s
  - HS200 SDR: 1.8 V, 0-200 MHz, 8/4-bit bus width, 200/100 MB/s
- SD card support: SDIO, SDR12, SDR25, SDR50, DDR50
- System bus interface: CBA 4.0 VBUSM initiator port with 64-bit data width and 64-bit address, little Endian only
- Configuration bus interface: CBA 4.0 VBUSM with 32-bit data width, 32-bit aligned accesses only, linear incrementing addressing mode, little Endian only

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.16 OSPI

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.17 Peripheral Component Interconnect Express (PCIe)

The PCIe subsystem supports the following main features:

- Dual mode – root port (RP) or end point (EP) modes.
- 1-lane configuration with up to 5.0GT/lane.
- 62.5/125 MHz operation on PIPE interface for Gen1/Gen2 respectively
- Constant 32-bit PIPE width for Gen1/Gen2 modes
- Maximum outbound payload size of 128 bytes
- Maximum inbound payload size of 128 bytes
- Maximum remote read request size of 4K bytes
- Maximum number of nonposted outstanding transactions: 8 on each VBUSM interface.
- Four virtual channels (4VC)
- Resizable BAR capability
- SRIS support
- Power Management
  - L1 Power Management Substate support
  - D1 support
  - L1 Power Shutoff support
- Legacy, MSI, and MSI-X interrupt support
- 32 outbound address translation regions
- Precision time measurement (PTM)

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.18 Serializer/Deserializer (SerDes) PHY

Integrated in the MAIN domain is one instance of high-speed differential interface implemented with Serializer/Deserializer (SerDes) Multi-protocol Multi-link PHY with the following main blocks:

- Single-lane SerDes PHY with common module for peripheral and Tx clocking handling
- Physical coding sub-block for data translation from/to the parallel interface, as well as data encoding/decoding and symbol alignment
- MUX module for device interface multiplexing into a single SerDes lane (Tx and Rx)
- A wrapper for sending control and reporting status signals from the SerDes and muxes

For more information, see *Serializer/Deserializer (SerDes)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.19 Real Time Interrupt (RTI/WWDT)

This section describes the Real Time Interrupt (RTI) modules with Windowed Watchdog Timer (WWDT) functionality for the device.

For more information, see *Real Time Interrupt (RTI/WWDT) Module* section in *Peripherals* chapter of the device TRM.

#### 7.4.2.20 Dual Mode Timer (DMTIMER)

The Dual Mode Timer (DMTIMER) module supports the following main features:

- Interrupts generated on overflow, compare, and capture events
- Free running 32-bit upward counter
- Supported operating modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- Programmable divider clock source ( $2^n$  with  $n=[0:8]$ )
- Dedicated input trigger for capture mode, and dedicated output trigger/PWM (pulse width modulation) signal
- On the fly read/write register (while counting)
- Generate 1-ms tick with 32768-Hz functional clock

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.21 UART

The UART module supports the following main features:

- 16C750 compatibility
- Baud rate from 300 bps up to 12 Mbps (MCU\_UART0 and MCU\_UART1 limited to 3.7 Mbps)
- Auto-baud between 1200 bps and 115.2 Kbps
- Software/hardware flow control
  - Programmable Xon/Xoff characters
  - Programmable Auto-RTS and Auto CTS
- Programmable serial interface characteristics
  - 5-, 6-, 7-, 8-bit characters
  - Even, odd, mark (always 1), space (always 0), or no parity (non-parity bit frame) bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
- Optional multi-drop transmission
- Configurable time-guard feature
- False start bit detection
- Line break generation and detection
- Modem control functions on UART0 (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities
- RS-485 External transceiver auto flow control support

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

#### 7.4.2.22 Universal Serial Bus Subsystem (USBSS)

The Universal Serial Bus Subsystem (USBSS) module supports the following main features:

General USB interface:

- Compliant with USB 3.1 specification
- Compliant with xHCI 1.1 specification
- Port configurable as:
  - USB host:
    - SuperSpeed Gen 1 (5 Gbps)
    - High-speed (480 Mbps)

- Full-speed (12 Mbps)
- Low-speed (1.5 Mbps)
- USB device/peripheral:
  - High-speed (480 Mbps)
  - Full-speed (12Mbps)
- USB Dual-Role device

USB Host mode features:

- 64 slots
- Up to 96 periodic simultaneous endpoints
- 256 primary streams
- MSI
- Root hub

For more information, see *Universal Serial Bus (USB) Subsystem* section in *Peripherals* chapter in the device TRM.

## 8 Applications, Implementation, and Layout

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Device Connection and Layout Fundamentals

#### 8.1.1 Power Supply

##### 8.1.1.1 Power Supply Designs

The [TPS65220](#) or [TPS65219](#) Power Management IC (PMIC) is recommended for an integrated power solution. This cost and space optimized solution is designed to power the device and its principal peripherals. For the full application note and related operational details, refer to [Powering the AM64x with the TPS65220 or TPS65219 PMIC](#).

- Full device performance entitlement of TPS6522053 as validated on TI Evaluation boards
- Factory programmed configurations support power rail load steps, supply voltage accuracies and maximum load currents with margins
- Factory programmed configurations support LPDDR4 and DDR4 memory
- Meets all power supply sequencing requirements, refer to [Power Supply Sequencing](#)

### 注

AM64x also supports discrete power supply topologies and customized power designs to meet various system requirements.

##### 8.1.1.2 Power Distribution Network Implementation Guidance

The [Sitara Processor Power Distribution Networks: Implementation and Analysis](#) provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI *only* supports designs that follow the board design guidelines contained in the application report.

#### 8.1.2 External Oscillator

For more information about External Oscillators, see the [Clock Specifications](#) section.

#### 8.1.3 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the [XDS Target Connection Guide](#).

For recommendations on JTAG, EMU, and TRACE routing, see the [Emulation and Trace Headers Technical Reference Manual](#)

#### 8.1.4 Unused Pins

For more information about Unused Pins, see the [Pin Connectivity Requirements](#) section.

## 8.2 Peripheral- and Interface-Specific Design Information

### 8.2.1 DDR Board Design and Layout Guidelines

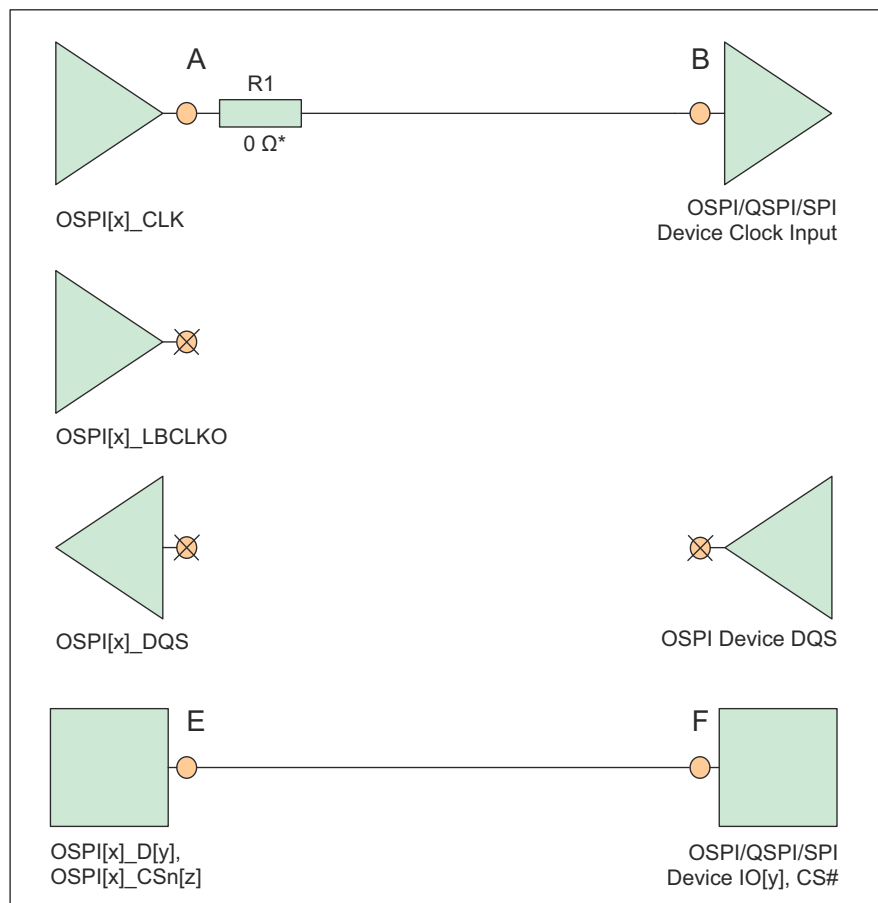
The goal of the [AM64x\AM243x DDR Board Design and Layout Guidelines](#) is to make the DDR system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4 or LPDDR4 memories that follow the guidelines in this document.

## 8.2.2 OSPI/QSPI/SPI Board Design and Layout Guidelines

The following section details the PCB routing guidelines that must be observed when connecting OSPI, QSPI, or SPI devices.

### 8.2.2.1 No Loopback, Internal PHY Loopback, and Internal Pad Loopback

- The OSPI[x]\_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The signal propagation delay from the OSPI[x]\_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B) must be  $\leq 450$  ps ( $\sim 7$ cm as stripline or  $\sim 8$ cm as microstrip)
- The signal propagation delay of each OSPI[x]\_D[y] and OSPI[x]\_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]\_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50  $\Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 8-1](#)
- Propagation delays and matching:
  - (A to B)  $\leq 450$  ps
  - (E to F, or F to E) = ((A to B)  $\pm 60$  ps)



\* 0  $\Omega$  resistor (R1), located as close as possible to the OSPI[x]\_CLK pin, is placeholder for fine tuning, if needed.

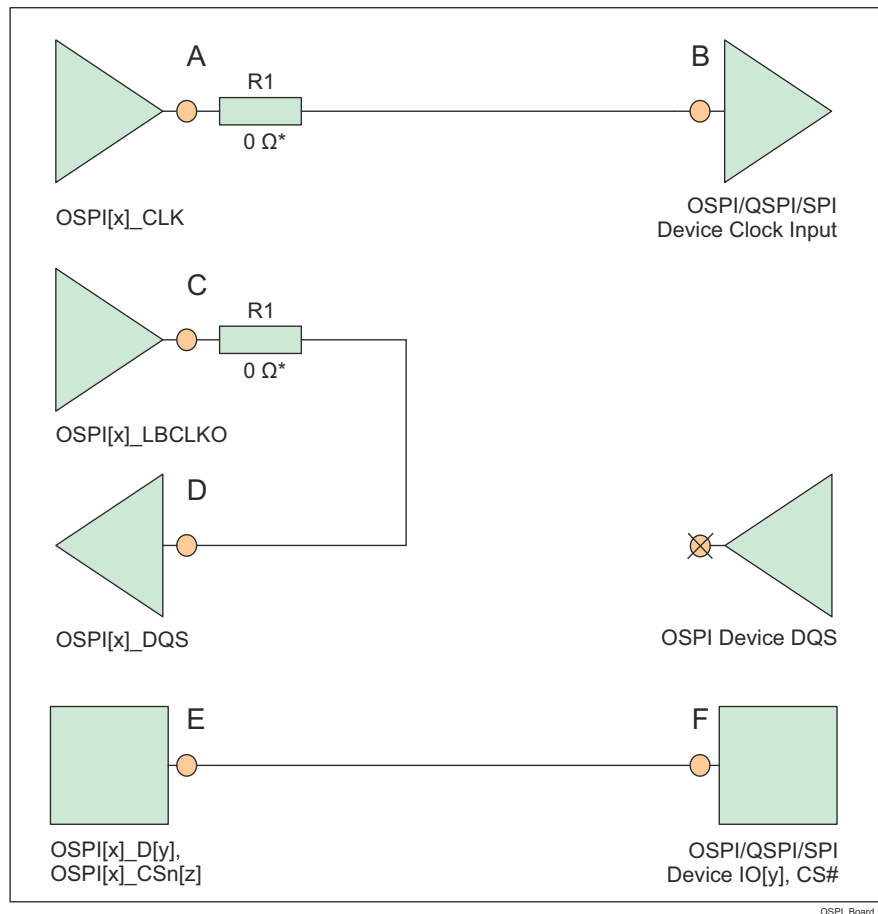
**Figure 8-1. OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback**

### 8.2.2.2 External Board Loopback

- The OSPI[x]\_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The OSPI[x]\_LBCLKO output pin must be looped back to the OSPI[x]\_DQS input pin
- The signal propagation delay of the OSPI[x]\_LBCLKO pin to the OSPI[x]\_DQS pin (C to D) must be approximately twice the propagation delay of the OSPI[x]\_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]\_D[y] and OSPI[x]\_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]\_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50  $\Omega$  PCB routing is recommended along with series terminations, as shown in [図 8-2](#)
- Propagation delays and matching:
  - (C to D) =  $2 \times ((A \text{ to } B) \pm 30 \text{ ps})$ , see the exception note below.
  - (E to F, or F to E) =  $((A \text{ to } B) \pm 60 \text{ ps})$

#### 注

The External Board Loopback hold time requirement (defined by parameter number O16 in [表 6-101](#), *OSPI0 Timing Requirements - PHY DDR Mode*) may be larger than the hold time provided by a typical OSPI/QSPI/SPI device. In this case, the propagation delay of OSPI[x]\_LBCLKO pin to the OSPI[x]\_DQS pin (C to D) can be reduced to provide additional hold time.

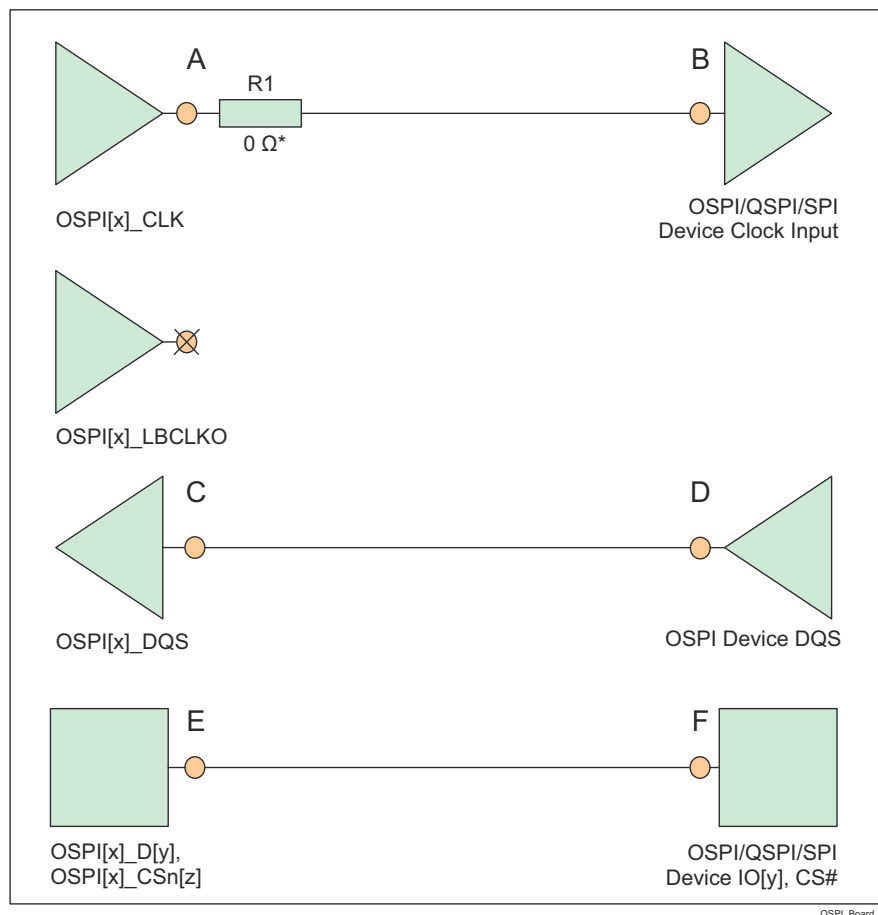


\* 0  $\Omega$  resistor (R1), located as close as possible to the OSPI[x]\_CLK and OSPI[x]\_LBCLKO pins, is a placeholder for fine tuning, if needed.

**図 8-2. OSPI Connectivity Schematic for External Board Loopback**

### 8.2.2.3 DQS (only available in Octal SPI devices)

- The OSPI[x]\_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The DQS pin of the attached OSPI/QSPI/SPI device must be connected to OSPI[x]\_DQS pin
- The signal propagation delay from the attached OSPI/QSPI/SPI device DQS pin to the OSPI[x]\_DQS pin (D to C) must be approximately equal to the signal propagation delay from the OSPI[x]\_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]\_D[y] and OSPI[x]\_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]\_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50  $\Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 8-3](#)
- Propagation delays and matching:
  - (D to C) = ((A to B)  $\pm$  30 ps)
  - (E to F, or F to E) = ((A to B)  $\pm$  60 ps)



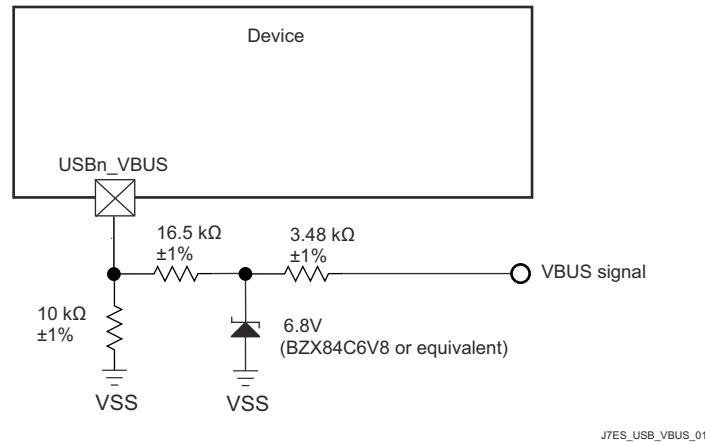
\* 0  $\Omega$  resistor (R1), located as close as possible to the OSPI[x]\_CLK pin, is a placeholder for fine tuning, if needed.

**図 8-3. OSPI Connectivity Schematic for DQS**

### 8.2.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the [Figure 8-4](#)), which limits the voltage applied to the actual device pin (USBn\_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of Zener diode at 5 V should be less than 100 nA.



**Figure 8-4. USB VBUS Detect Voltage Divider / Clamp Circuit**

The USB0\_VBUS pin can be considered to be fail-safe because the external circuit in [Figure 8-4](#) limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

### 8.2.4 System Power Supply Monitor Design Guidelines

The VMON\_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system and can be connected to the VMON\_VSYS pin via an external resistor divider circuit. This system supply is monitored by comparing the external voltage divider output voltage to an internal voltage reference, where a power fail event is triggered when the voltage applied to VMON\_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit.

When building the resistor divider circuit the designer must understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON\_VSYS input threshold which has a nominal value of 0.45 V, with a variation of  $\pm 3\%$ . Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON\_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON\_VSYS input leakage current can be in the range of 10 nA to 2.5  $\mu$ A when applying 0.45 V.

#### 注

The resistor voltage divider shall be designed such that the output voltage never exceeds the maximum value defined in the *Recommended Operating Conditions* section, during normal operating conditions.

Figure 8-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

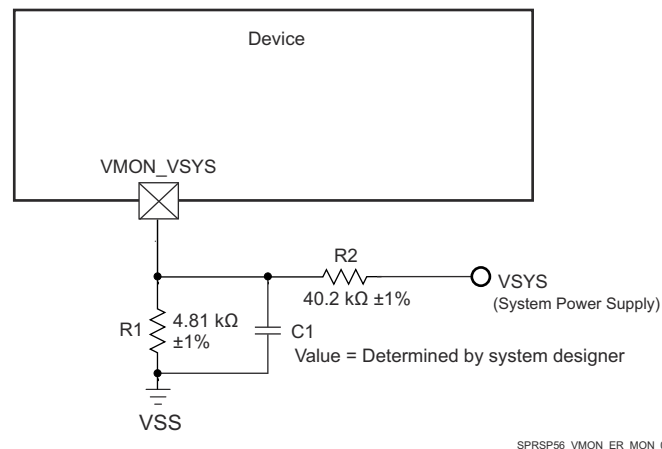
For this example, the designer must understand which variables effect the maximum trigger threshold when selecting resistor values. A device which has a VMON\_VSYS input threshold of  $0.45\text{ V} + 3\%$  needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but the contribution to the maximum trigger point is not obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON\_VSYS pin is  $2.5\text{ }\mu\text{A}$ . When implementing a resistor divider where  $R1 = 4.81\text{ k}\Omega$  and  $R2 = 40.2\text{ k}\Omega$ , the result is a maximum trigger threshold of 4.517 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of  $0.45\text{ V} - 3\%$  when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.013 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.013 V to 4.517 V. Approximately 250 mV of this range is introduced by VMON\_VSYS input threshold accuracy of  $\pm 3\%$ , approximately 150 mV of this range is introduced by resistor tolerance of  $\pm 1\%$ , and approximately 100 mV of this range is introduced by loading error when VMON\_VSYS input leakage current is  $2.5\text{ }\mu\text{A}$ .

The resistor values selected in this example produces approximately  $100\text{ }\mu\text{A}$  of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above can be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer must also consider implementing a noise filter on the voltage divider output since VMON\_VSYS has minimum hysteresis and a high-bandwidth response to transients. This can be done by installing a capacitor across R1 as shown in Figure 8-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.



**Figure 8-5. System Supply Monitor Voltage Divider Circuit**

VMON\_1P8\_MCU and VMON\_1P8\_SOC pins provide a way to monitor external 1.8 V power supplies. These pins must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

VMON\_3P3\_MCU and VMON\_3P3\_SOC pins provide a way to monitor external 3.3 V power supplies. These pins must be connected directly to their respective power source. An internal resistor divider with software

control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

### **8.2.5 High Speed Differential Signal Routing Guidance**

The [High Speed Interface Layout Guidelines](#) provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application note.

### **8.2.6 Thermal Solution Guidance**

The [Thermal Design Guide for DSP and ARM Application Processors](#) provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application note.

## 8.3 Clock Routing Guidelines

### 8.3.1 Oscillator Routing

When designing the printed-circuit board:

- Place all crystal circuit components as close as possible to the respective device pins.
- Route the crystal circuit traces on the outer layer of the PCB and minimize trace lengths to reduce parasitic capacitance and minimize crosstalk from other signals.
- Place a continuous ground plane on the adjacent layer of the PCB such that it is under all crystal circuit components and crystal circuit traces.
- Route a ground guard around the crystal circuit components to shield it from any adjacent signals routed on the same layer as the crystal circuit traces. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Route a ground guard between the MCU\_OSC0\_XI and MCU\_OSC0\_XO signals to shield the MCU\_OSC0\_XI signal from the MCU\_OSC0\_XO signal. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Connect all crystal circuit ground connections and ground guard connections directly to the adjacent layer ground plane, and the device VSS ground plane if they are implemented separately on different layers of the PCB.

注

Implementing a ground guard between the MCU\_OSC0\_XI and MCU\_OSC0\_XO signals is critical to minimize shunt capacitance between the two signals. Routing these two signals adjacent to each other without a ground guard between them will effectively reduce the gain of the oscillator amplifier, which reduces its ability to start oscillation.

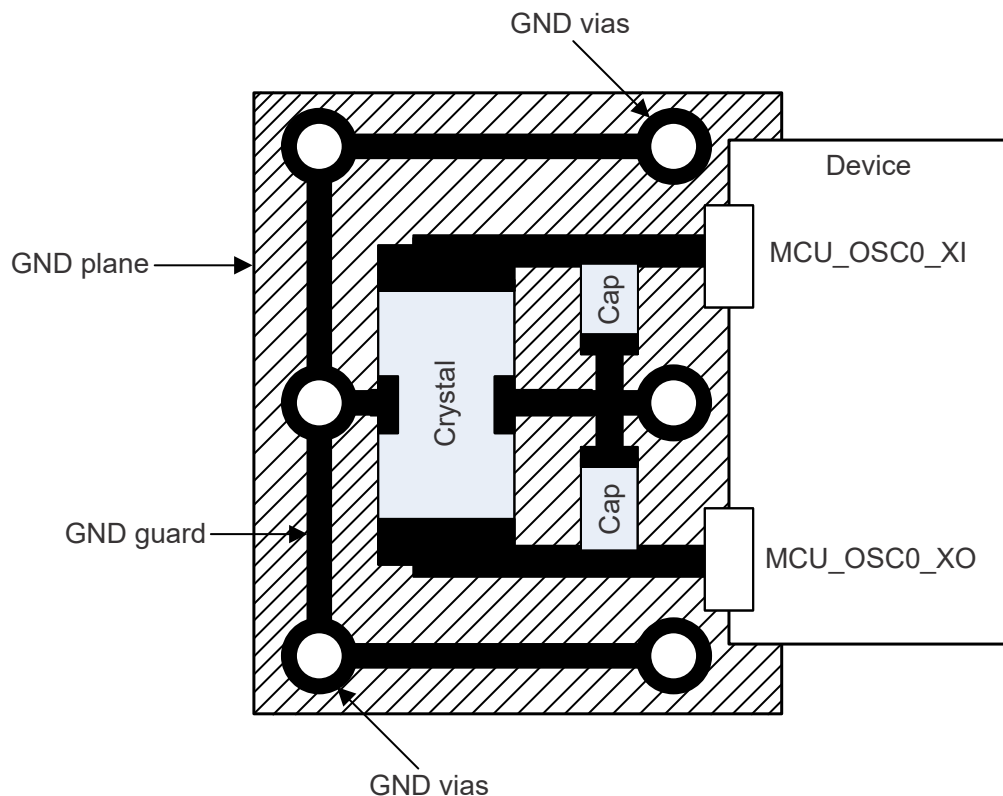


図 8-6. MCU\_OSC0 PCB requirements

## 9 Device and Documentation Support

### 9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all embedded processor devices and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM6442BSFFHAALV). Texas Instruments recommends two of three possible prefix designators for related support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the device's final electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null (BLANK)** Production version of the silicon die that is fully qualified and meets final electrical specifications.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM64x devices in the ALV package type, see the Package Option Addendum at the end of this document, the TI website ([ti.com](http://ti.com)), or contact your TI sales representative.

### 9.1.1 Standard Package Symbolization

注

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

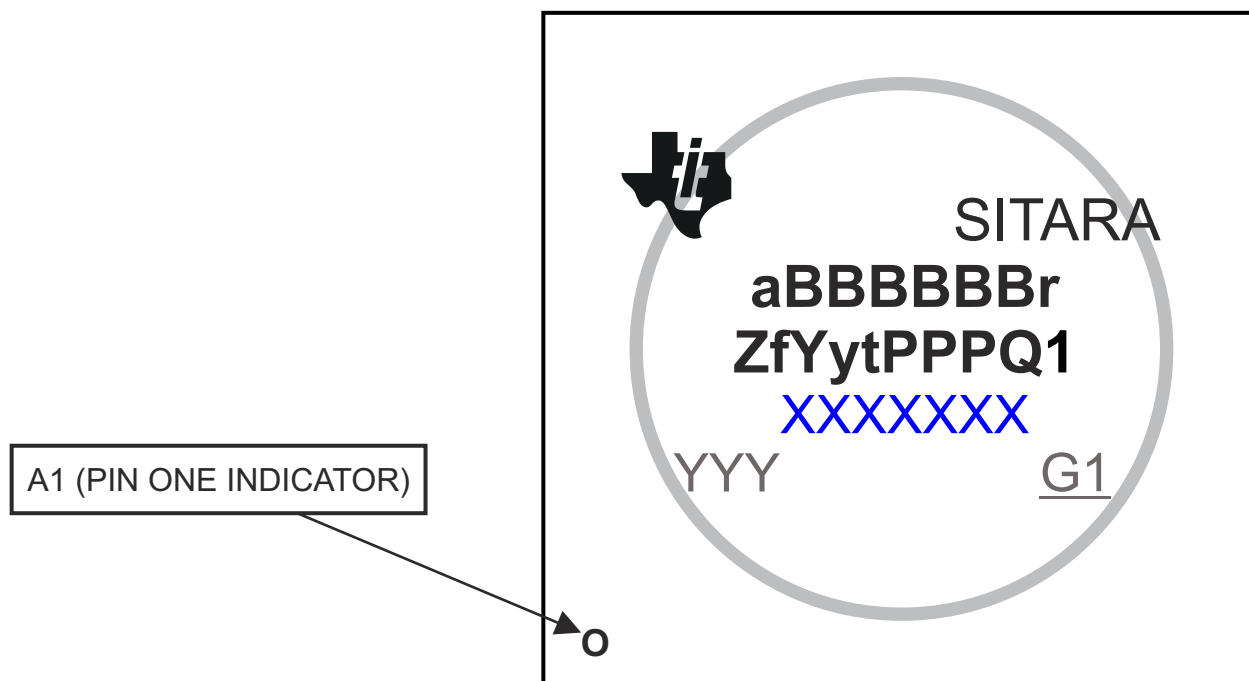


図 9-1. Printed Device Reference

## 9.1.2 Device Naming Convention

**表 9-1. Nomenclature Description**

| FIELD PARAMETER | FIELD DESCRIPTION                | VALUE  | DESCRIPTION                                                                                                                                                                                                                                                           |
|-----------------|----------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| a               | Device evolution stage           | X      | Prototype                                                                                                                                                                                                                                                             |
|                 |                                  | P      | Preproduction (production test flow, no reliability data)                                                                                                                                                                                                             |
|                 |                                  | BLANK  | Production                                                                                                                                                                                                                                                            |
| BBBBBB          | Base production part number      | AM6442 | See 表 4-1, <i>Device Comparison</i>                                                                                                                                                                                                                                   |
|                 |                                  | AM6441 |                                                                                                                                                                                                                                                                       |
|                 |                                  | AM6422 |                                                                                                                                                                                                                                                                       |
|                 |                                  | AM6421 |                                                                                                                                                                                                                                                                       |
|                 |                                  | AM6412 |                                                                                                                                                                                                                                                                       |
|                 |                                  | AM6411 |                                                                                                                                                                                                                                                                       |
| r               | Device revision                  | A      | Silicon Revision (SR) 1.0                                                                                                                                                                                                                                             |
|                 |                                  | B      | SR 2.0                                                                                                                                                                                                                                                                |
| Z               | Device Speed Grades              | S      | See 表 6-1, <i>Speed Grade Maximum Frequency</i>                                                                                                                                                                                                                       |
|                 |                                  | K      |                                                                                                                                                                                                                                                                       |
| f               | Features (see 表 4-1)             | C      | All PRU_ICSSG features are enabled except for industrial communication support. PRU_ICSSG industrial communication interfaces include Ethernet networking (MII/RGMII, MDIO), Sigma-Delta (SD) decimation, and three channel peripheral interface (EnDat 2.2 and BiSS) |
|                 |                                  | D      | Features supported by C, plus PRU_ICSSG industrial communication is enabled                                                                                                                                                                                           |
|                 |                                  | E      | Features supported by D, plus EtherCAT HW Accelerator and CAN-FD are enabled                                                                                                                                                                                          |
|                 |                                  | F      | Features supported by E, plus Pre-integrated Stacks are enabled                                                                                                                                                                                                       |
| Y               | Functional Safety                | G      | Non-Functional Safety                                                                                                                                                                                                                                                 |
|                 |                                  | F      | Functional Safety                                                                                                                                                                                                                                                     |
| y               | Security                         | G      | Non-Secure                                                                                                                                                                                                                                                            |
|                 |                                  | H      | Secure                                                                                                                                                                                                                                                                |
| t               | Temperature <sup>(1)</sup>       | A      | –40°C to 105°C - Extended Industrial (see セクション 6.4, <i>Recommended Operating Conditions</i> )                                                                                                                                                                        |
|                 |                                  | I      | –40°C to 125°C - Automotive (see セクション 6.4, <i>Recommended Operation Conditions</i> )                                                                                                                                                                                 |
| PPP             | Package Designator               | ALV    | ALV FCBGA-N441 (17.2 mm × 17.2 mm) Package                                                                                                                                                                                                                            |
| Q1              | Automotive Designator            | Q1     | Automotive Qualified (AEC - Q100)                                                                                                                                                                                                                                     |
|                 |                                  | BLANK  | Standard                                                                                                                                                                                                                                                              |
| XXXXXXX         | Lot Trace Code (LTC)             |        |                                                                                                                                                                                                                                                                       |
| YYY             | Production Code; For TI use only |        |                                                                                                                                                                                                                                                                       |
| O               | Pin one designator               |        |                                                                                                                                                                                                                                                                       |
| G1              | ECAT—Green package designator    |        |                                                                                                                                                                                                                                                                       |

(1) Applies to device max junction temperature.

### 注

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

## 9.2 Tools and Software

The following Development Tools support development for TI's Embedded Processing platforms:

### Development Tools

**Code Composer Studio™ Integrated Development Environment** Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. The tool includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

**SysConfig-PinMux Tool** The SysConfig-PinMux Tool is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool generates output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements. The **Cloud-based SysConfig-PinMux Tool** is also available.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [ti.com](http://ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 9.3 Documentation Support

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

The following documents describe the AM64x devices.

### Technical Reference Manual

**AM64x/AM243x Processors Silicon Revision 1.0 Technical Reference Manual** Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM64x family of devices.

### Errata

**AM64x/AM243x Processors Silicon Revision 1.0 Silicon Errata** Describes the known exceptions to the functional specifications for the device.

## 9.4 サポート・リソース

**テキサス・インスツルメンツ E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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## 9.5 Trademarks

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PCI-Express® is a registered trademark of PCI-SIG.  
EtherCAT® is a registered trademark of Beckhoff Automation GmbH.  
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## 9.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.7 用語集

### テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

### Changes from November 1, 2023 to April 21, 2024 (from Revision F (OCTOBER 2023) to Revision G (APRIL 2024))

#### Page

|                                                                                                                                                                                                                                                                     |     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| • グローバル:「改訂履歴」セクションをドキュメントの末尾に移動.....                                                                                                                                                                                                                               | 1   |
| • (特長): 取得した機能安全準拠認証を含むように「機能安全」の箇条書き項目を更新 / 変更.....                                                                                                                                                                                                                | 1   |
| • (Related Products): Deleted sentence containing the reference to lockstep because the feature is not applicable.....                                                                                                                                              | 9   |
| • (Speed Grade Maximum Frequency): Changed the Maximum Frequency for ICSSG in K speed grade devices from 250MHz to 333MHz.....                                                                                                                                      | 103 |
| • (SDIO Electrical Characteristics): Changed VDDSHV5 power rail name, where applicable, used to define the $V_{IL}/V_{ILSS}/V_{IH}/V_{IHSS}/V_{OL}/V_{OH}$ parameter values by referencing a generic power rail name (VDD), and added an associated table note..... | 106 |

## 11 Mechanical, Packaging, and Orderable Information

### 11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要なお知らせと免責事項

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## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| <a href="#">AM6411BKCGHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6411B<br>KCGHAALV<br>709 |
| AM6411BKCGHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6411B<br>KCGHAALV<br>709 |
| <a href="#">AM6411BSCGHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6411B<br>SCGHAALV<br>709 |
| AM6411BSCGHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6411B<br>SCGHAALV<br>709 |
| <a href="#">AM6411BSCGHIALVR</a> | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6411B<br>SCGHIALV<br>709 |
| AM6411BSCGHIALVR.B               | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6411B<br>SCGHIALV<br>709 |
| <a href="#">AM6412BKCGHAALVR</a> | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6412B<br>KCGHAALV<br>709 |
| AM6412BKCGHAALVR.B               | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6412B<br>KCGHAALV<br>709 |
| <a href="#">AM6412BSCGHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6412B<br>SCGHAALV<br>709 |
| AM6412BSCGHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6412B<br>SCGHAALV<br>709 |
| <a href="#">AM6421BSDGHAALVR</a> | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SDGHAALV<br>709 |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier    | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|----------------------------------|---------------|----------------------|-------------------|--------------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| AM6421BSDGHAALVR.B               | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R          | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SDGHAALV<br>709 |
| <a href="#">AM6421BSEFHAALVR</a> | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R          | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SEFHAALV<br>709 |
| AM6421BSEFHAALVR.B               | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R          | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SEFHAALV<br>709 |
| <a href="#">AM6421BSFFHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC<br>TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SFFHAALV<br>709 |
| AM6421BSFFHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC<br>TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SFFHAALV<br>709 |
| <a href="#">AM6421BSFGHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC<br>TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SFGHAALV<br>709 |
| AM6421BSFGHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC<br>TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6421B<br>SFGHAALV<br>709 |
| <a href="#">AM6422BSDFHAALVR</a> | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R          | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6422B<br>SDFHAALV<br>709 |
| AM6422BSDFHAALVR.B               | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R          | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6422B<br>SDFHAALV<br>709 |
| <a href="#">AM6422BSDGHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC<br>TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6422B<br>SDGHAALV<br>709 |
| AM6422BSDGHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC<br>TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6422B<br>SDGHAALV<br>709 |
| <a href="#">AM6441BSEFHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC<br>TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6441B<br>SEFHAALV<br>709 |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| AM6441BSEFHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6441B<br>SEFHAALV<br>709 |
| <a href="#">AM6441BSEGHAALVR</a> | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6441B<br>SEGHAALV<br>709 |
| AM6441BSEGHAALVR.B               | Active        | Production           | FCBGA (ALV)   441 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6441B<br>SEGHAALV<br>709 |
| <a href="#">AM6441BSFFHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6441B<br>SFFHAALV<br>709 |
| AM6441BSFFHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6441B<br>SFFHAALV<br>709 |
| <a href="#">AM6442BSDGHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SDGHAALV<br>709 |
| AM6442BSDGHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SDGHAALV<br>709 |
| <a href="#">AM6442BSEFHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SEFHAALV<br>709 |
| AM6442BSEFHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SEFHAALV<br>709 |
| <a href="#">AM6442BSEGHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SEGHAALV<br>709 |
| AM6442BSEGHAALV.B                | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SEGHAALV<br>709 |
| <a href="#">AM6442BSFFHAALV</a>  | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SFFHAALV<br>709 |

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|---------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| AM6442BSFFHAALV.B               | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SFFHAALV<br>709 |
| <a href="#">AM6442BSFGHAALV</a> | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SFGHAALV<br>709 |
| AM6442BSFGHAALV.B               | Active        | Production           | FCBGA (ALV)   441 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6442B<br>SFGHAALV<br>709 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

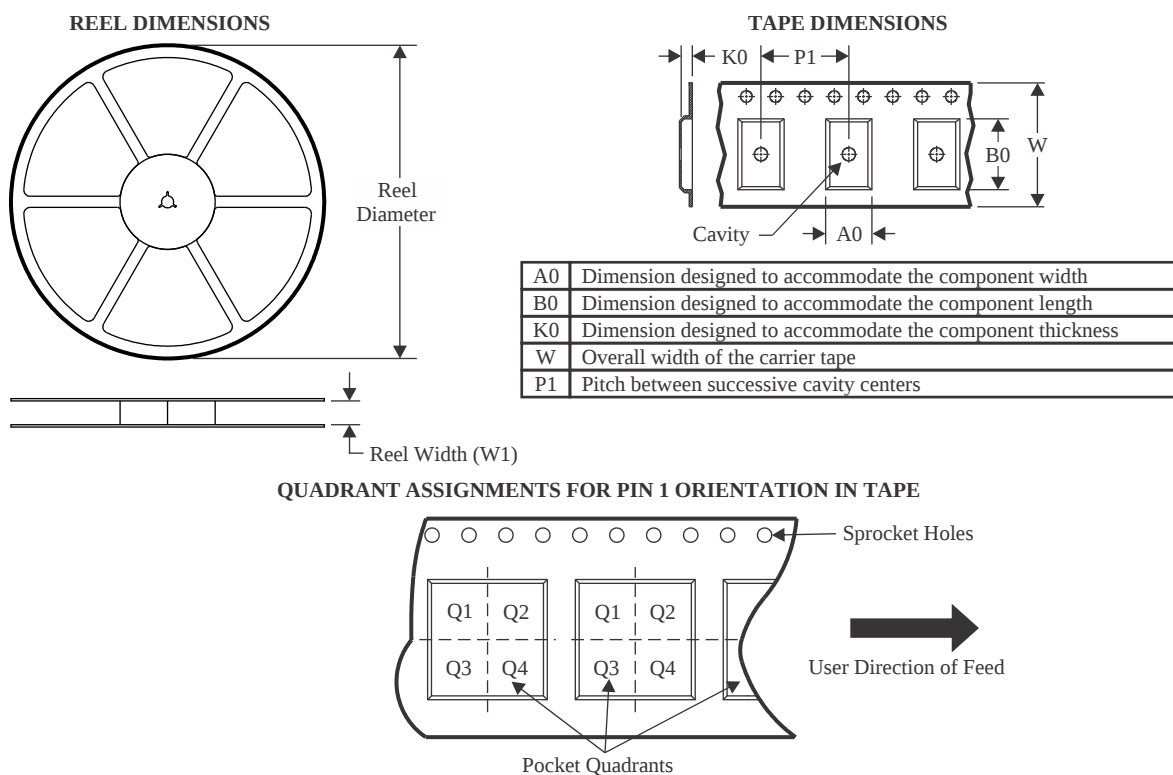
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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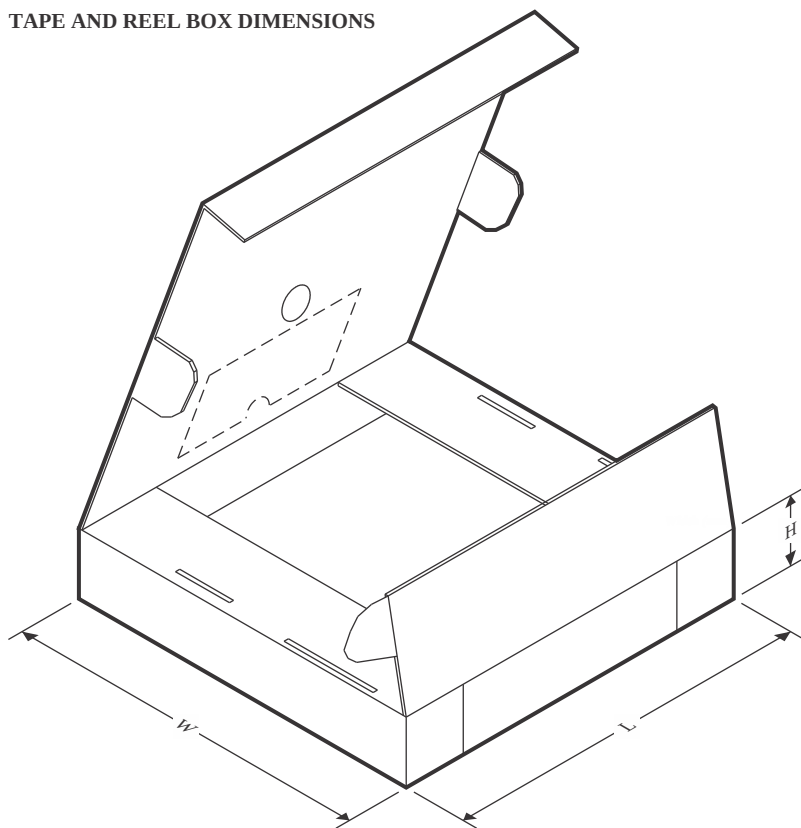
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AM6411BSCGHIALVR | FCBGA        | ALV             | 441  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |
| AM6412BCKGHAALVR | FCBGA        | ALV             | 441  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |
| AM6421BSDGHAALVR | FCBGA        | ALV             | 441  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |
| AM6421BSEFHAALVR | FCBGA        | ALV             | 441  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |
| AM6422BSDFHAALVR | FCBGA        | ALV             | 441  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |
| AM6441BSEGHAALVR | FCBGA        | ALV             | 441  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |

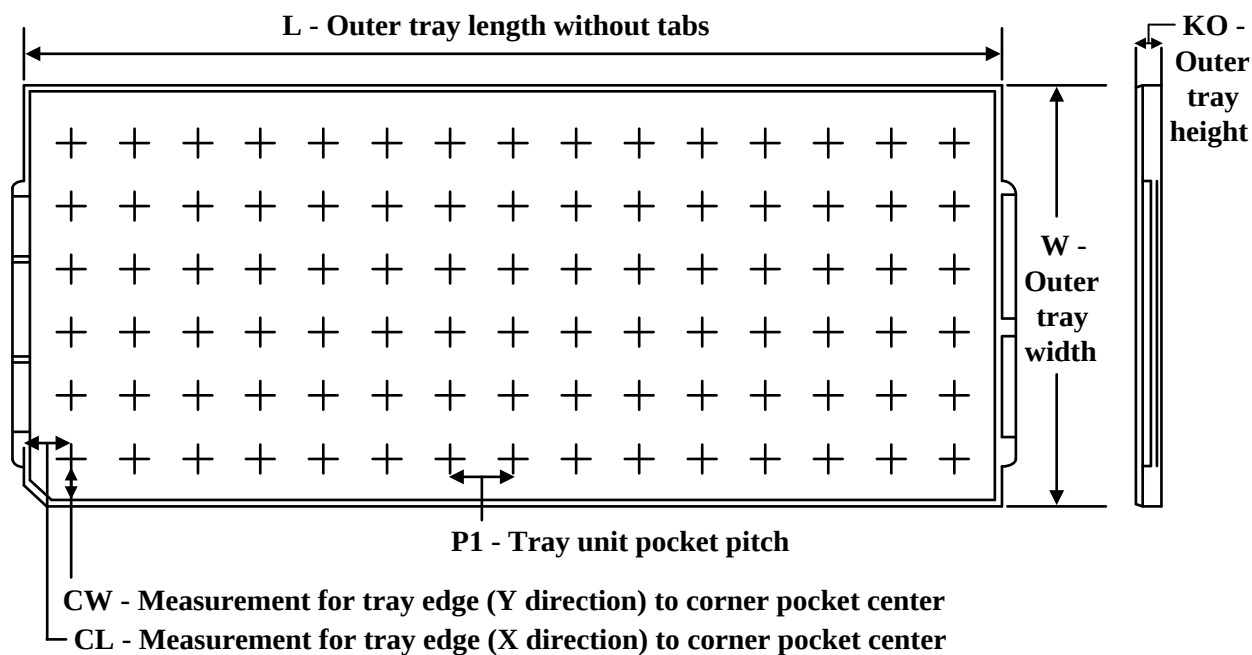
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| AM6411BSCGHIALVR | FCBGA        | ALV             | 441  | 500 | 336.6       | 336.6      | 41.3        |
| AM6412BKCGHAALVR | FCBGA        | ALV             | 441  | 500 | 336.6       | 336.6      | 41.3        |
| AM6421BSDGHAALVR | FCBGA        | ALV             | 441  | 500 | 336.6       | 336.6      | 41.3        |
| AM6421BSEFHAALVR | FCBGA        | ALV             | 441  | 500 | 336.6       | 336.6      | 41.3        |
| AM6422BSDFHAALVR | FCBGA        | ALV             | 441  | 500 | 336.6       | 336.6      | 41.3        |
| AM6441BSEGHAALVR | FCBGA        | ALV             | 441  | 500 | 336.6       | 336.6      | 41.3        |

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|-------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| AM6411BKCGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6411BKCGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6411BSCGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6411BSCGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6412BSCGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6412BSCGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6421BSFFHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6421BSFFHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6421BSFGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6421BSFGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6422BSDGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6422BSDGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6441BSEFHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6441BSEFHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6441BSFFHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6441BSFFHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSDGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |

| Device            | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|-------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| AM6442BSDGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSEFHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSEFHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSEGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSEGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSFFHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSFFHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSFGHAALV   | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |
| AM6442BSFGHAALV.B | ALV          | FCBGA        | 441  | 84  | 6 x 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.55   |



**FCBGA - 2.657 mm max height**

**Top View:**

- Overall width: 17.1
- Overall height: 17.3
- Inner width: 10.8
- Inner height: 12.8
- Feature callouts: BALL A1 CORNER, PIN 1 ID (OPTIONAL), 0.1 C (surface finish), 0.2 C (surface finish).

**Side View:**

- Seating Plane
- Dimensions: 2.652, 2.332, 0.662, 0.5 TYP, 0.3
- Feature callouts: 0.15 C (surface finish), 1.45

**Pin Grid View:**

- Grid size: 21 pins by 21 pins (441 pins total)
- Pin pitch: 0.25 (M), 0.1 (M)
- Grid dimensions: 16 TYP (width), 16 TYP (height)
- Feature callouts: 0.8 TYP, 0.6 TYP, 0.6 TYP, 0.8 TYP, 0.25 (M), 0.1 (M), 0.55, 0.45

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

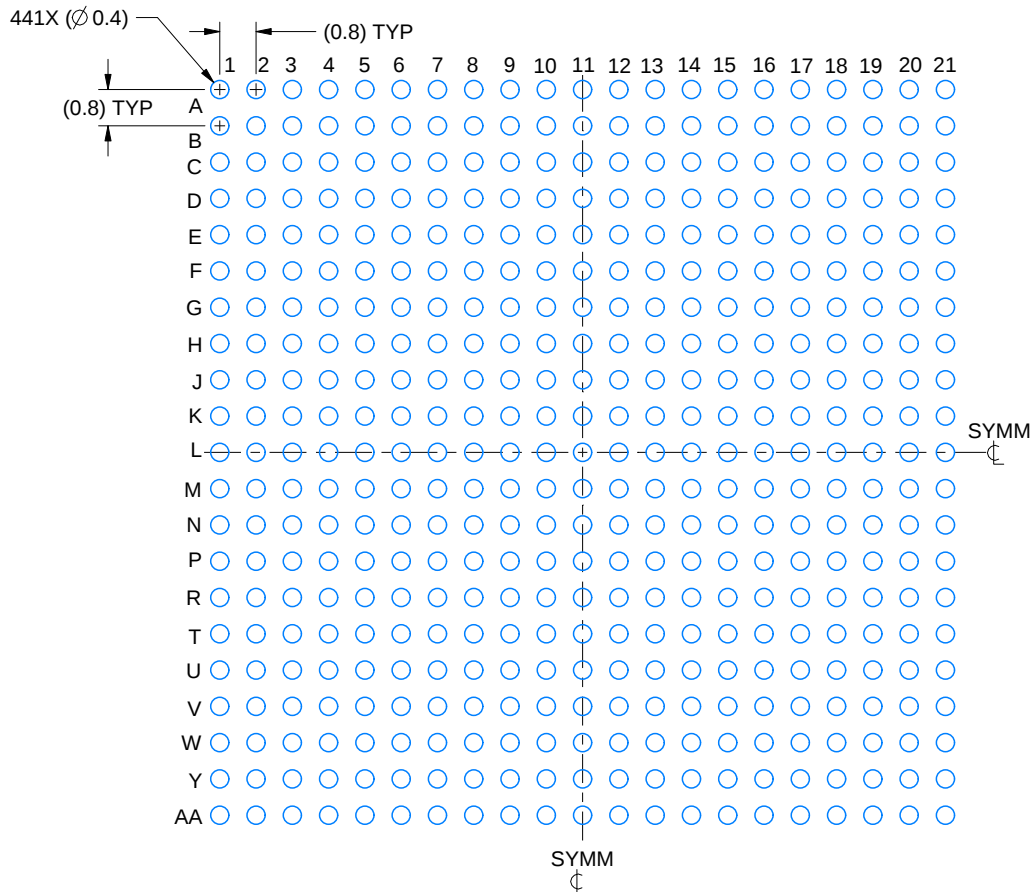
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

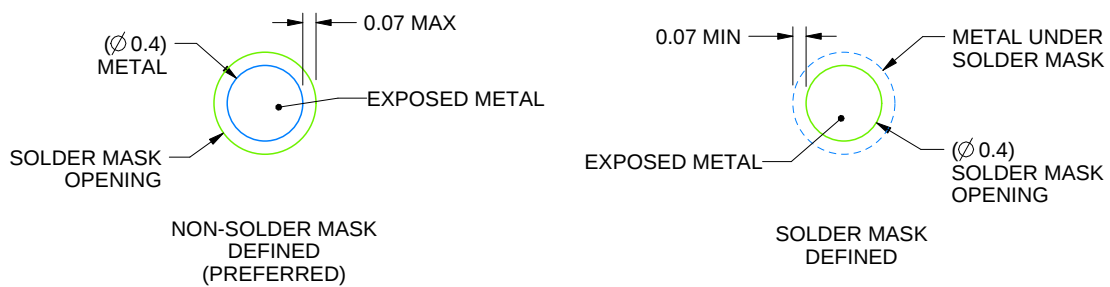
ALV0441A

FCBGA - 2.657 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4225999/A 06/2020

NOTES: (continued)

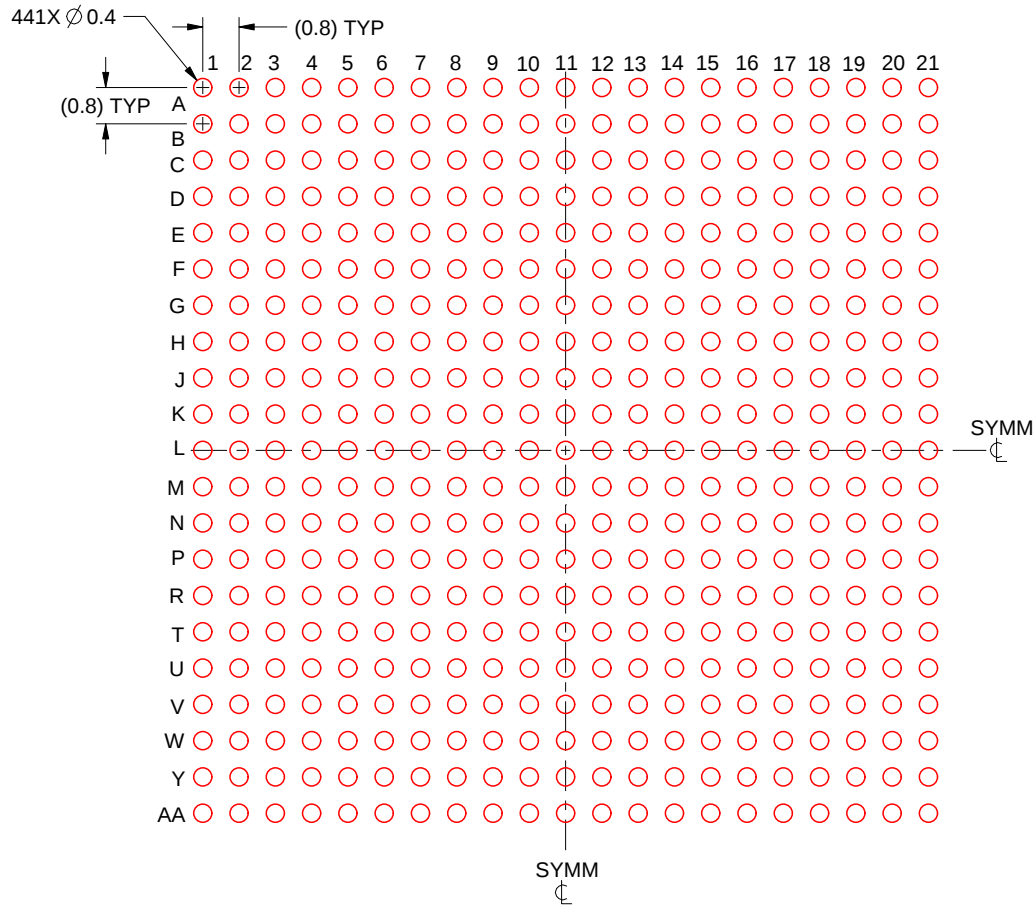
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ALV0441A

FCBGA - 2.657 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
 BASED ON 0.15 mm THICK STENCIL  
 SCALE: 6X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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