AM26LV31E 低電圧高速クワッド差動ライン ドライバ ±15kV IEC ESD 保護機能搭載

1 特長

- 規格 TIA/EIA-422-B および ITU 勧告 V.11 適合またはそれを上回る性能
- 3.3V 単一電源で動作
- RS422 バス ピン用 ESD 保護機能
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2、接触放電
  - ±15kV IEC 61000-4-2、気中放電
- 最高 32MHz のスイッチング速度
- 伝搬遅延時間:8ns (標準値)
- パルス スキュー時間:500ps (標準値)
- 大出力電流:±30mA
- 制御された立ち上がりおよび立ち下がり時間:5ns (標準値)
- 100Ω 負荷での
  差動出力電圧:2.6V (標準値)
- 3.3V 電源で 5V ロジック入力を許容
- I_{off} により部分的パワーダウン モードでの動作をサポート
- ドライバ出力の短絡保護回路
- グリッチ フリーのパワーアップ / パワーダウン保護機能
- パッケージ オプション:SO、SOIC、TSSOP、VQFN

2 アプリケーション

- モーター ドライブ
- 宇宙 / 航空 / 防衛
- 医療、ヘルスケア、フィットネス
- ワイヤレス インフラ
- ファクトリ オートメーション / 制御

3 概要

AM26LV31E は、3 ステート出力のクワッド差動ライン ドライバです。このドライバは ±15kV ESD (HBM および IEC61000-4-2、気中放電) および ±8kV ESD (IEC61000-4-2、接触放電) の保護を備えています。このデバイスは、低い電源電圧で TIA/EIA-422-B および ITU 勧告 V.11 のドライバ要件を満たすように設計されています。

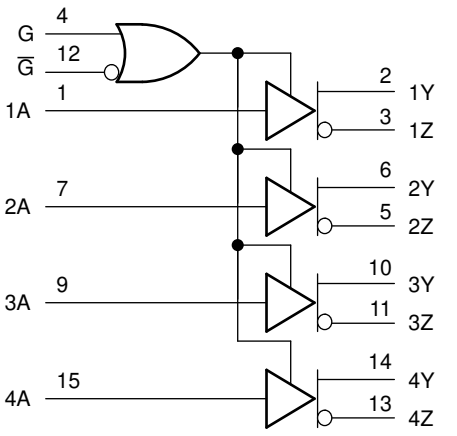
このデバイスは、最高 32MHz のスイッチング速度で平衡化されたバス転送に最適化されています。出力には、ツイストペア伝送ラインなど平衡化されたラインを駆動するための、非常に大きな電流能力があり、電源オフ時には高インピーダンスになります。

AM26LV31EI は、-40℃～+85℃で動作特性が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
AM26LV31E	SOIC (D、16)	9.9mm × 6mm
	SO (NS、16)	10.2mm × 7.8mm
	TSSOP (PW、16)	5mm × 6.4mm
	VQFN (RGY) (16)	4mm × 3.5mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



ロジック図

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4 Pin Configuration and Functions

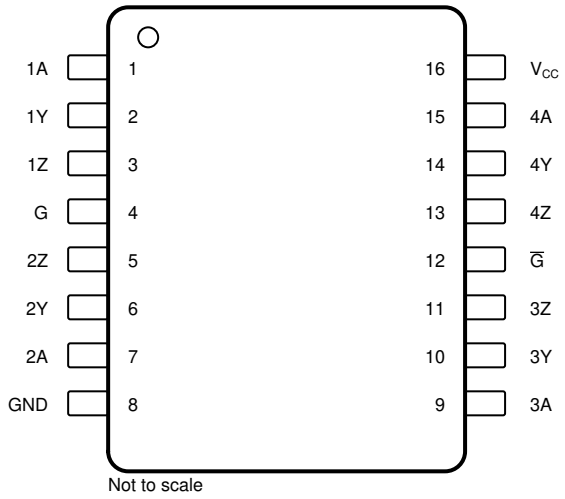


図 4-1. D, NS, or PW Package 16-Pin SOIC, SO, TSSOP (Top View)

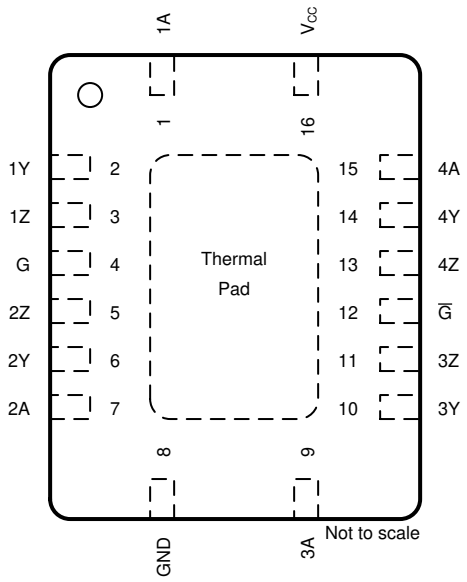


図 4-2. RGY Package 16-Pin VQFN With Thermal Pad (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	1	I	Logic data input to RS422 driver 1
1Y	2	O	RS-422 data line for driver 1
1Z	3	O	RS-422 data line for driver 1
2A	7	I	Logic data input to RS422 driver 2
2Y	6	O	RS-422 data line for driver 2
2Z	5	O	RS-422 data line for driver 2
3A	9	I	Logic data input to RS422 driver 3
3Y	10	O	RS-422 data line for driver 3
3Z	11	O	RS-422 data line for driver 3
4A	15	I	Logic data input to RS422 driver 4
4Y	14	O	RS-422 data line for driver 4
4Z	13	O	RS-422 data line for driver 4
G	4	I	Driver enable (active high)
$\overline{G}$	12	I	Driver enable (active low)
GND	8	—	Device ground pin
V_{CC}	16	—	Power input (5V)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	6	V
V_I	Input voltage		–0.5	6	V
V_O	Output voltage		–0.5	6	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–20	mA
I_O	Continuous output current			±150	mA
	Continuous current through V_{CC} or GND			±200	mA
T_J	Operating virtual junction temperature			150	°C
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±15000	V
			All pins except 2, 3, 5, 6, 10, 11, 13, and 14	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		IEC 61000-4-2 contact discharge	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±8000	
		IEC 61000-4-2 air-gap discharge	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±15000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage	0		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–30	mA
I_{OL}	Low-level output current			30	mA
T_A	Operating free-air temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC[1]		AM26LV31E				UNIT
		D (SOIC)	PW (TSSOP)	NS (SO)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	107.5	88.5	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	38.4	46.2	46.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	53.7	50.7	24.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	3.2	13.5	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	53.1	50.3	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	8.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = –20mA	2.4	3		V
V_{OL}	Low-level output voltage	V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0mA	2		4	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100Ω (see 図 6-1)	2	2.6		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage	R_L = 100Ω (see 図 6-1)			±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100Ω (see 図 6-1)		1.5	2	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage	R_L = 100Ω (see 図 6-1)			±0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0, V_O = –0.25V or 5.5V			±100	µA
I_{OZ}	High-impedance state output current	V_O = –0.25V or 5.5V, G = 0.8V or $\overline{G}$ = 2V			±100	µA
I_I	Input current	V_{CC} = 0 or 3.6V, V_I = 0 or 5.5V			±10	µA
I_{OS}	Short-circuit output current	V_O = V_{CC} or GND[2]	–30		–150	mA
I_{CC}	Supply current (total package)	V_I = V_{CC} or GND, No load, enable			100	µA
C_{pd}	Power dissipation capacitance	No load[3]		160		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.
(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(3) C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

5.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	See 図 6-2	4	8	12	ns
t_{PLH}	Propagation delay time, low- to high-level output		4	8	12	ns
t_t	Transition time (t_r or t_f)	See 図 6-2		5	10	ns
t_{PZH}	Output-enable time to high level	See 図 6-3		10	20	ns
t_{PZL}	Output-enable time to low level	See #none#		10	20	ns
t_{PHZ}	Output-disable time from high level	See 図 6-3		10	20	ns
t_{PLZ}	Output-disable time from low level	See #none#		10	20	ns
$t_{sk(p)}$	Pulse skew	See 図 6-2 (2) (3)		0.5	1.5	ns
$t_{sk(o)}$	Skew limit (pin to pin)				1.5	ns
$t_{sk(lim)}$	Skew limit (device to device)				3	ns
$f_{(max)}$	Maximum operating frequency	See 図 6-2		32		MHz

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

5.7 Typical Characteristics

図 5-1 and 図 5-2 show typical I_{CC} values at various frequencies/data rates for various termination conditions.

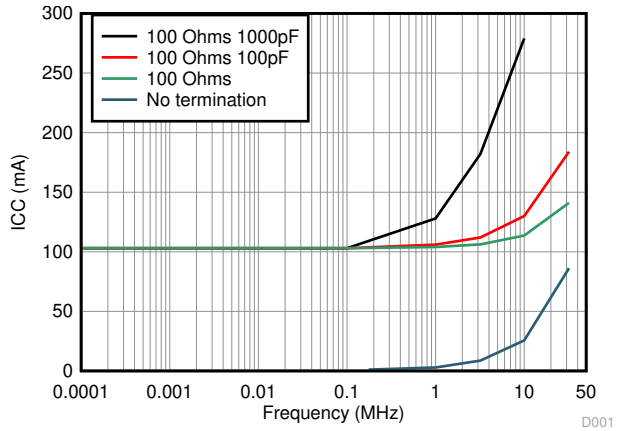


図 5-1. I_{CC} vs. Frequency

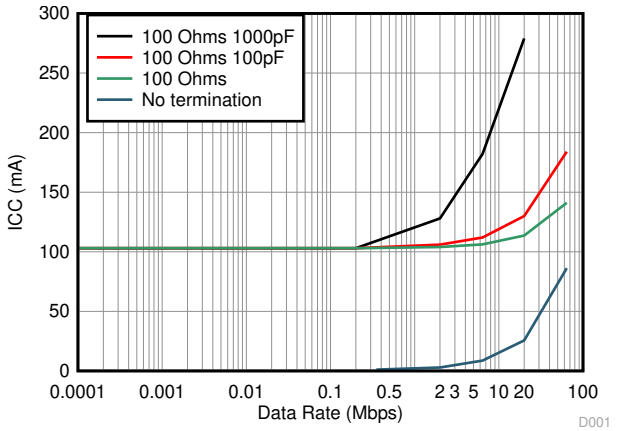


図 5-2. I_{CC} vs. Data Rate

6 Parameter Measurement Information

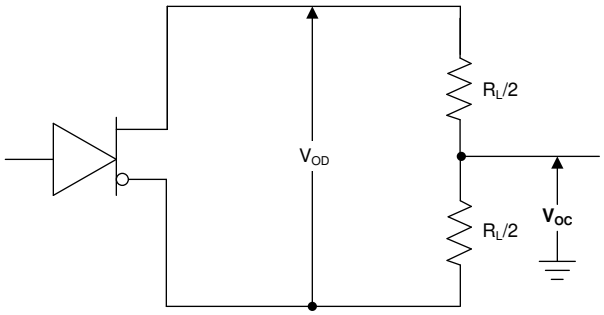
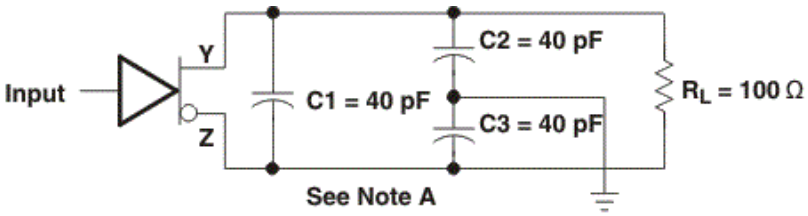
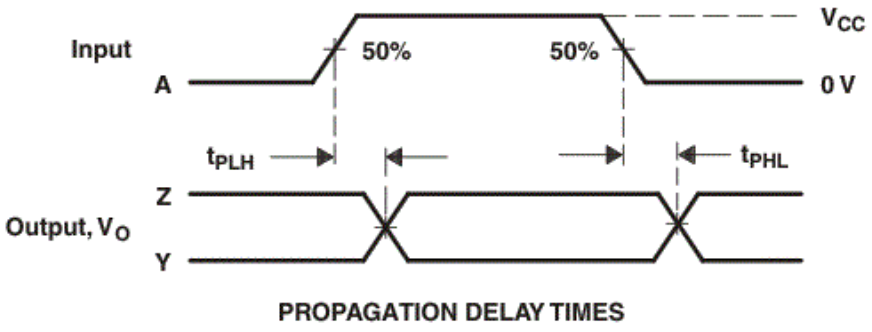
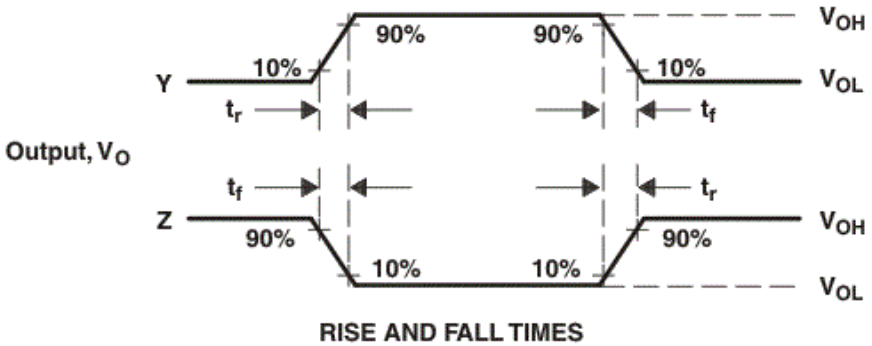


図 6-1. Test Circuit, V_{OD} and V_{OC}





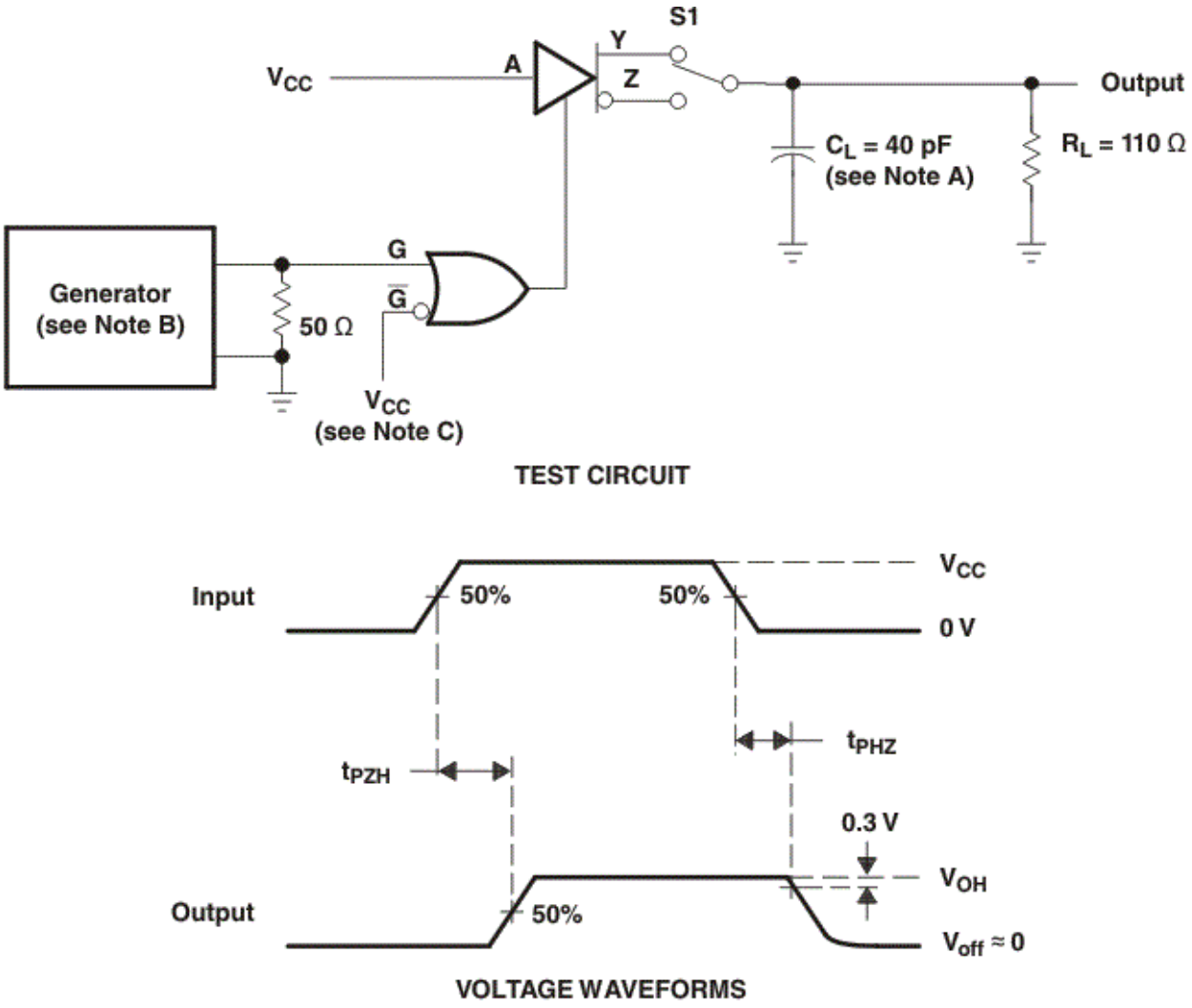
PROPAGATION DELAY TIMES



RISE AND FALL TIMES

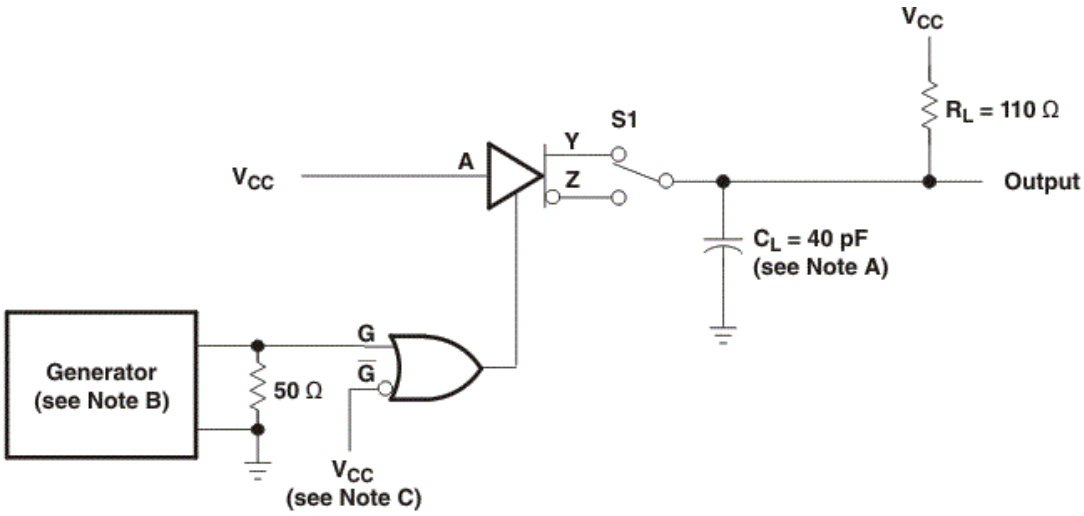
A. C_L includes probe and stray capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 10MHz, 50% duty cycle, t_r and t_f ≤ 10ns.

図 6-2. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

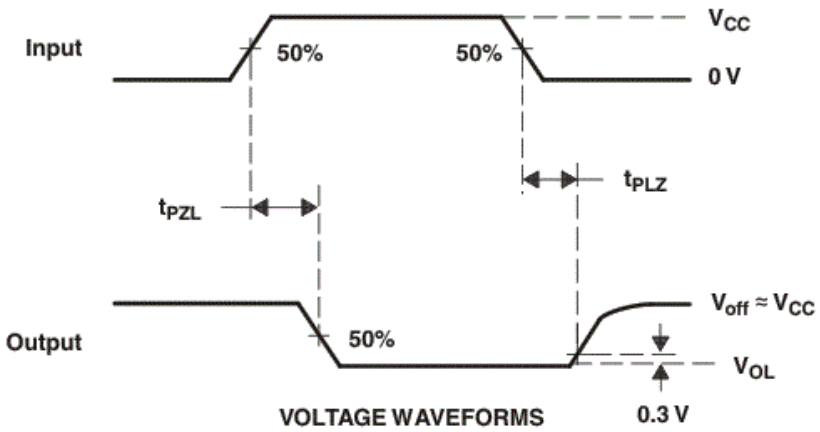


A. C_L includes probe and stray capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle, t_r and t_f ≤ 2ns.
C. To test the active-low enable $\overline{G}$ ground G and apply inverted waveform to $\overline{G}$.

図 6-3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and stray capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle, t_r and t_f ≤ 2ns.
C. To test the active-low enable $\overline{G}$ ground G and apply inverted waveform to $\overline{G}$.

7 Detailed Description

7.1 Overview

The AM26LV31E is a quadruple differential line driver with 3-state outputs. The device is designed to meet TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply voltage. The high current capability of the outputs allow for driving balanced lines, such as twisted-pair transmission lines, and proved a high impedance in the power-off condition. The AM26LV31E is optimized for balanced-bus transmission line at switching rates up to 32MHz.

From a single 3.3V power supply, the device operates four 3-state differential line drivers with integrated active high and active low enables for precise control. The device is capable of accepting 5V logic inputs with a 3.3V supply. The driver is designed to handle loads of a minimum of ±30mA of sink or source current.

7.2 Functional Block Diagram

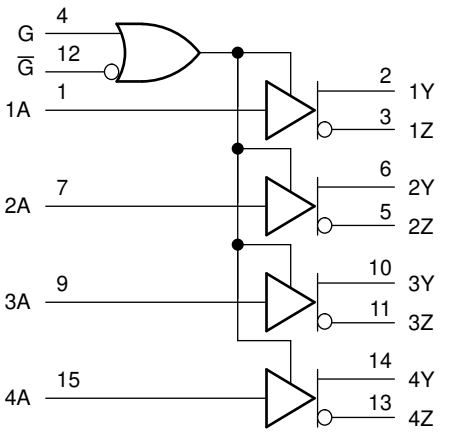


図 7-1. Logic Diagram

7.3 Feature Description

7.3.1 Complementary Out-Enable Inputs

The AM26LV31E transmitter outputs can be configured using the G and $\overline{G}$ logic inputs. The transmitter outputs are enabled when either G is set to logic HIGH or $\overline{G}$ is set to logic LOW. The reverse disables the outputs (G = LOW, $\overline{G}$ = HIGH). See 表 7-1 for the complete truth table.

7.3.2 High Output Impedance for Specific Driver Enable Inputs

When the AM26LV31E transmitter outputs are disabled using G and $\overline{G}$ logic inputs, the outputs are set to a high impedance state.

7.4 Device Functional Modes

表 7-1 lists the functional modes of the AM26LV31E.

表 7-1. Function Table

INPUT A (1)	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

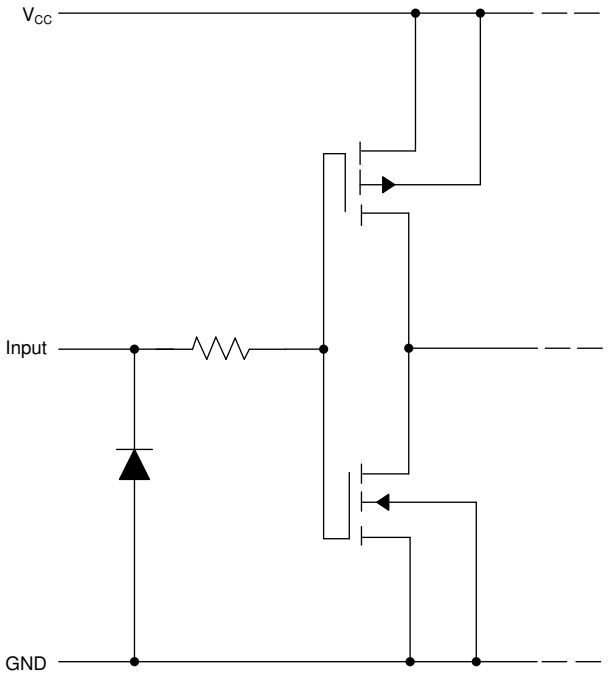


図 7-2. Equivalent of Each Input (A, G, or $\overline{G}$) Schematic

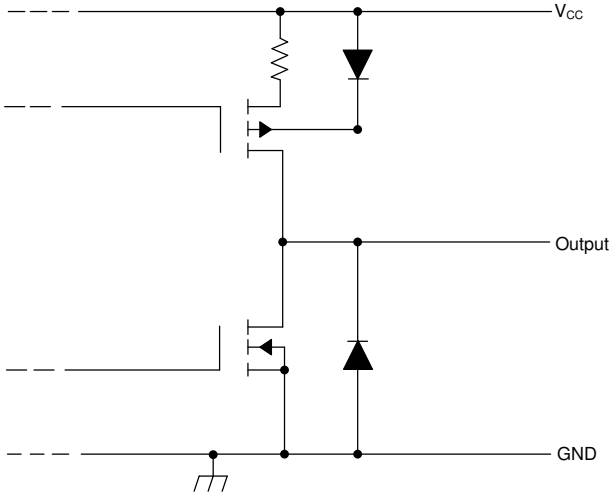


図 7-3. Typical of Each Driver Output Schematic

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31E and AM26LV32E, respectively, were tested at room temperature with a 3.3V supply voltage. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

8.2 Typical Application

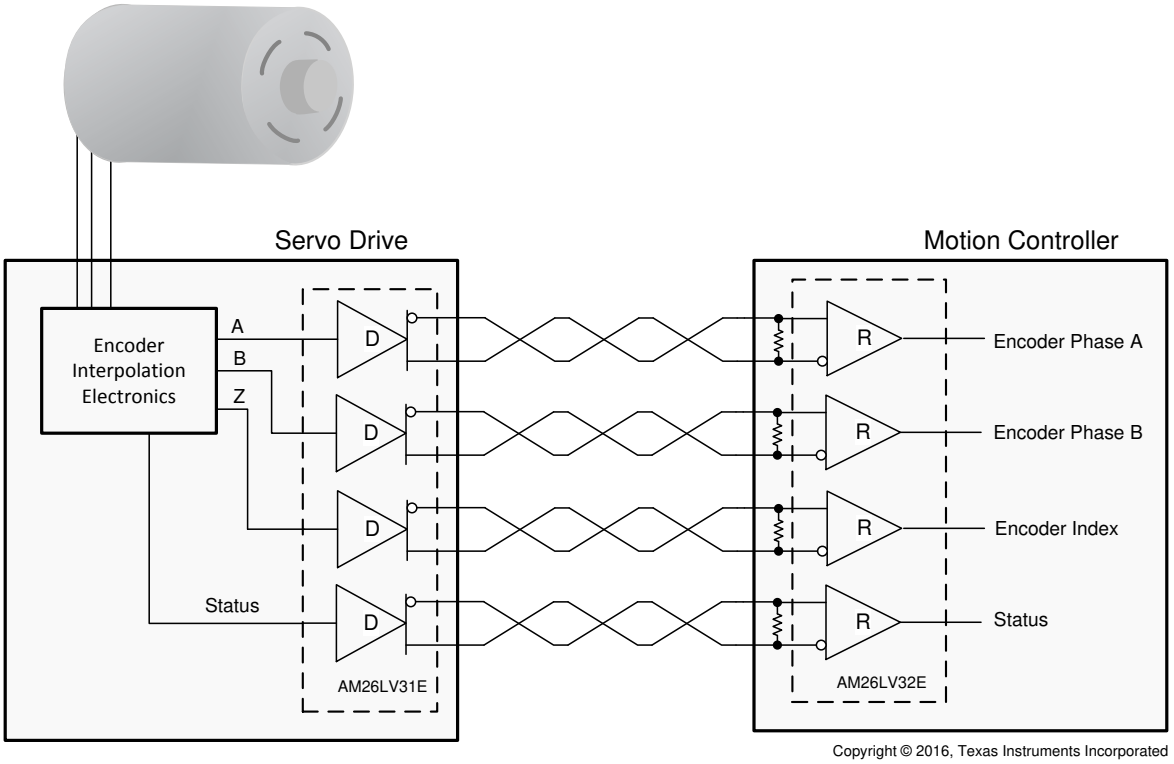


図 8-1. Encoder Application

8.2.1 Design Requirements

This example requires the following:

- 3.3V power source
- RS-485 bus operating at speed compatible with cable length
- Connector that ensures the correct polarity for port pins

8.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200mV on the A-B port, if the drive is in high impedance state (see *Failsafe in RS-485 data buses*, SLYT080).

8.2.3 Application Curve

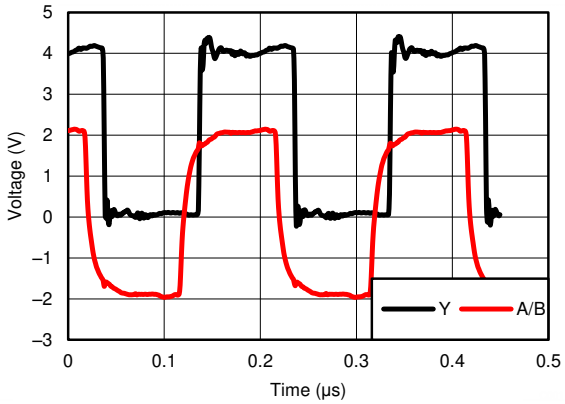


図 8-2. Differential 120Ω Terminated Output Waveforms (Cat 5E Cable)

8.3 Power Supply Recommendations

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can often propagate into analog circuitry through the power supply of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

8.4.2 Layout Example

For all Y and Z outputs, make sure the traces are impedance matched to cable used.

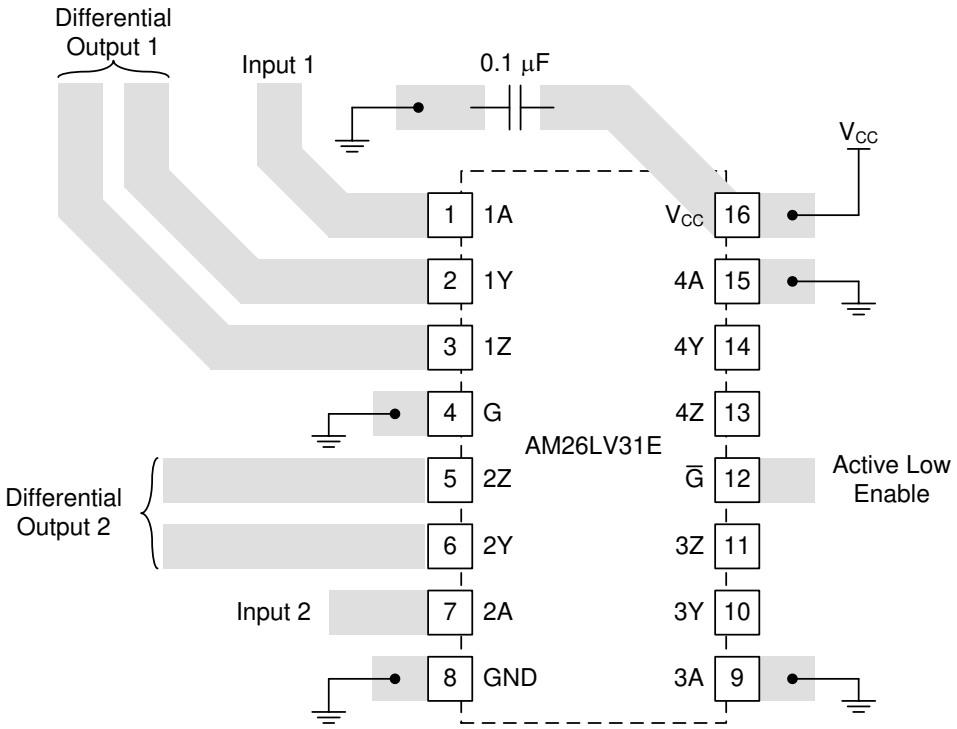


図 8-3. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

Failsafe in RS-485 data buses, SLYT080

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (September 2016) to Revision C (July 2023)	Page
• 「製品情報」表を「パッケージ情報」表に変更	1
• Changed the *Thermal Information* table	5
• Changed the note in 図 6-3	7

Changes from Revision A (May 2008) to Revision B (September 2016)	Page
• 「アプリケーション」セクション、「熱に関する情報」表、「機能説明」セクション、「デバイスの機能モード」セ、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「注文情報」表を削除 (このデータシートの末尾にある「メカニカル、パッケージ、および注文情報」を参照)	1
• Changed *ESD PROTECTION* to *ESD Ratings* table	4
• Changed $R_{\theta JA}$ for PW package from 108°C/W: to 99.5°C/W	5
• Changed $R_{\theta JA}$ for NS package from 64°C/W: to 74.5°C/W	5

- Changed $R_{\theta JA}$ for RGY package from 39°C/W: to 39.3°C/W..... 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26LV31EIDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI
AM26LV31EIDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI
AM26LV31EIDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI
AM26LV31EINSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV31EI
AM26LV31EINSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV31EI
AM26LV31EINSRG4.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV31EI
AM26LV31EIPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31
AM26LV31EIPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31
AM26LV31EIPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31
AM26LV31EIRGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31
AM26LV31EIRGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31
AM26LV31EIRGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AM26LV31E :

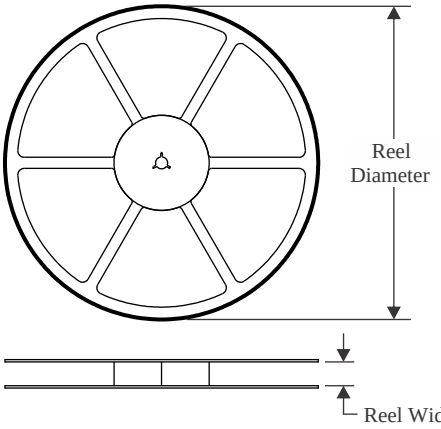
- Enhanced Product : AM26LV31E-EP

NOTE: Qualified Version Definitions:

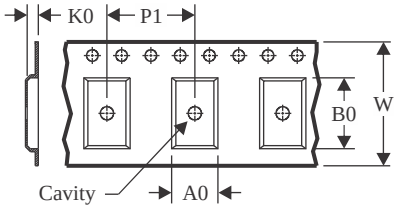
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

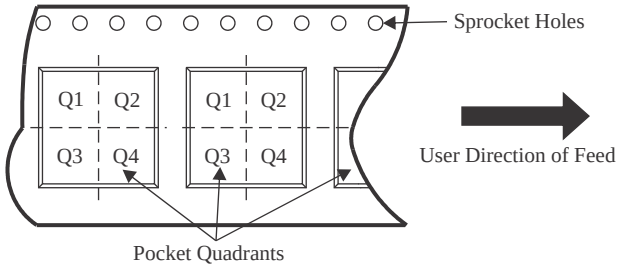


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

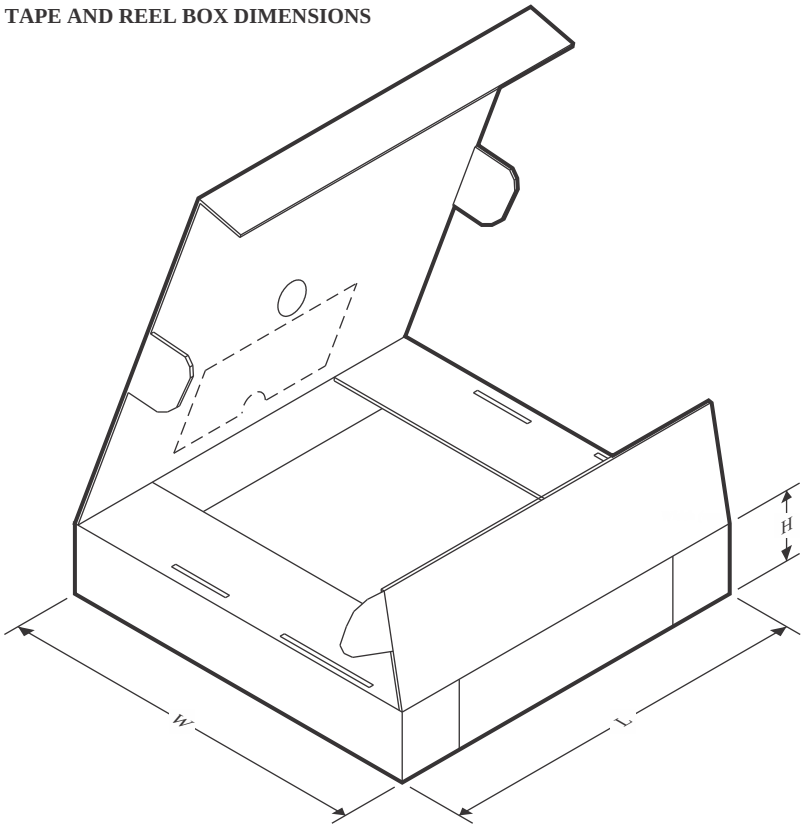
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31EINSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31EINSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV31EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV31EIRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

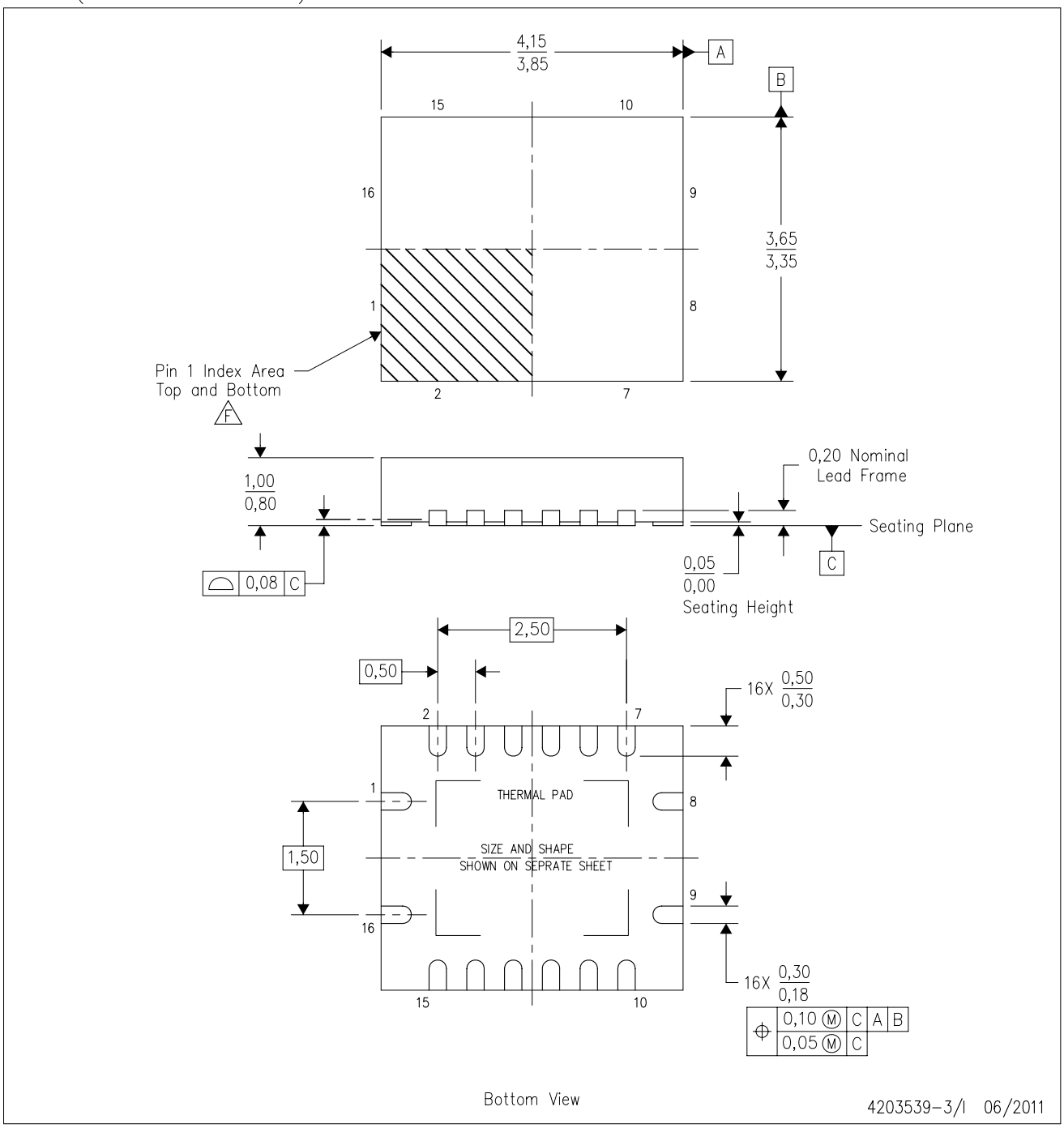
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

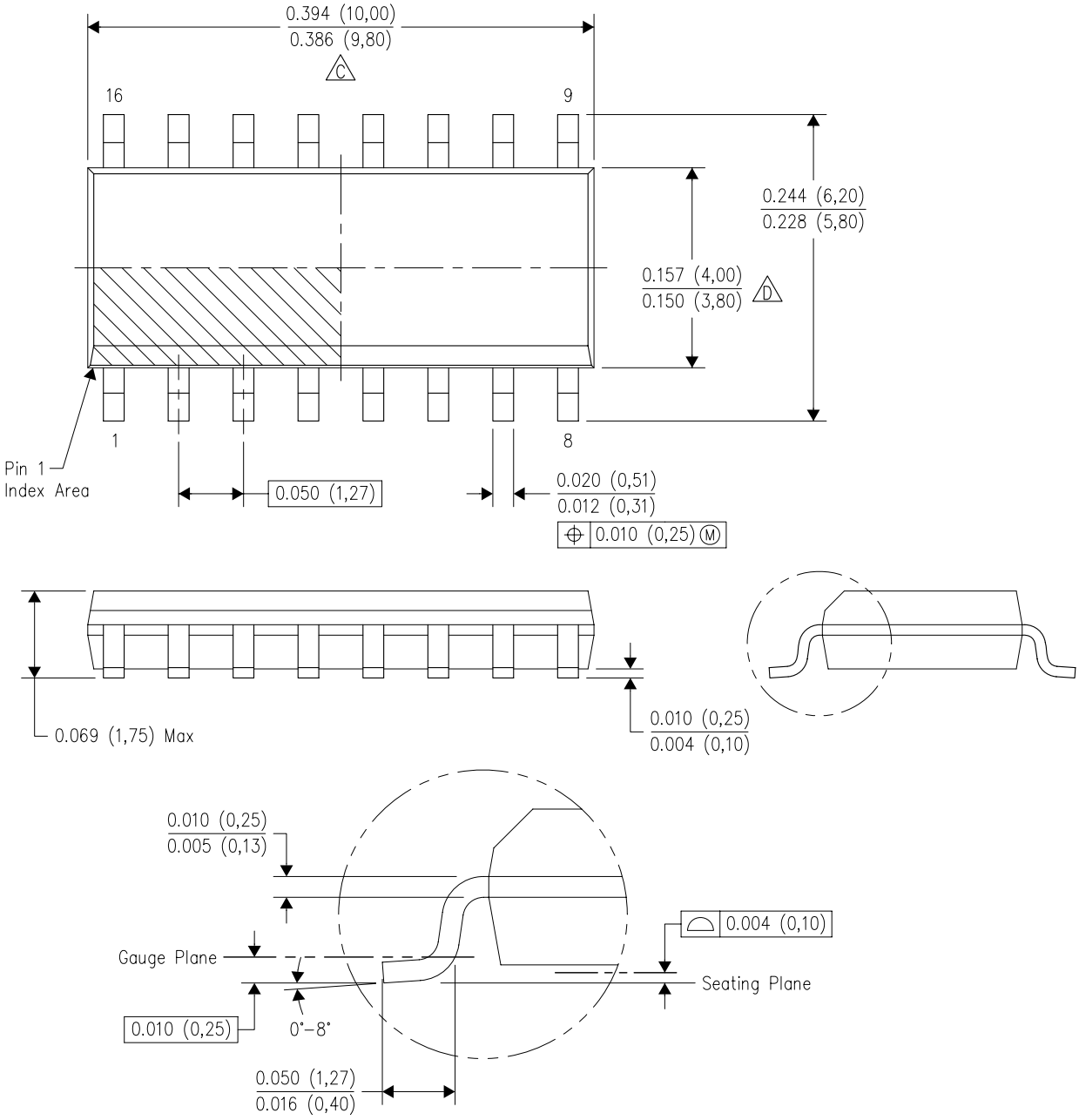
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31EIDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV31EINSR	SOP	NS	16	2000	367.0	367.0	38.0
AM26LV31EINSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26LV31EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26LV31EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
AM26LV31EIRGYR	VQFN	RGY	16	3000	360.0	360.0	36.0

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



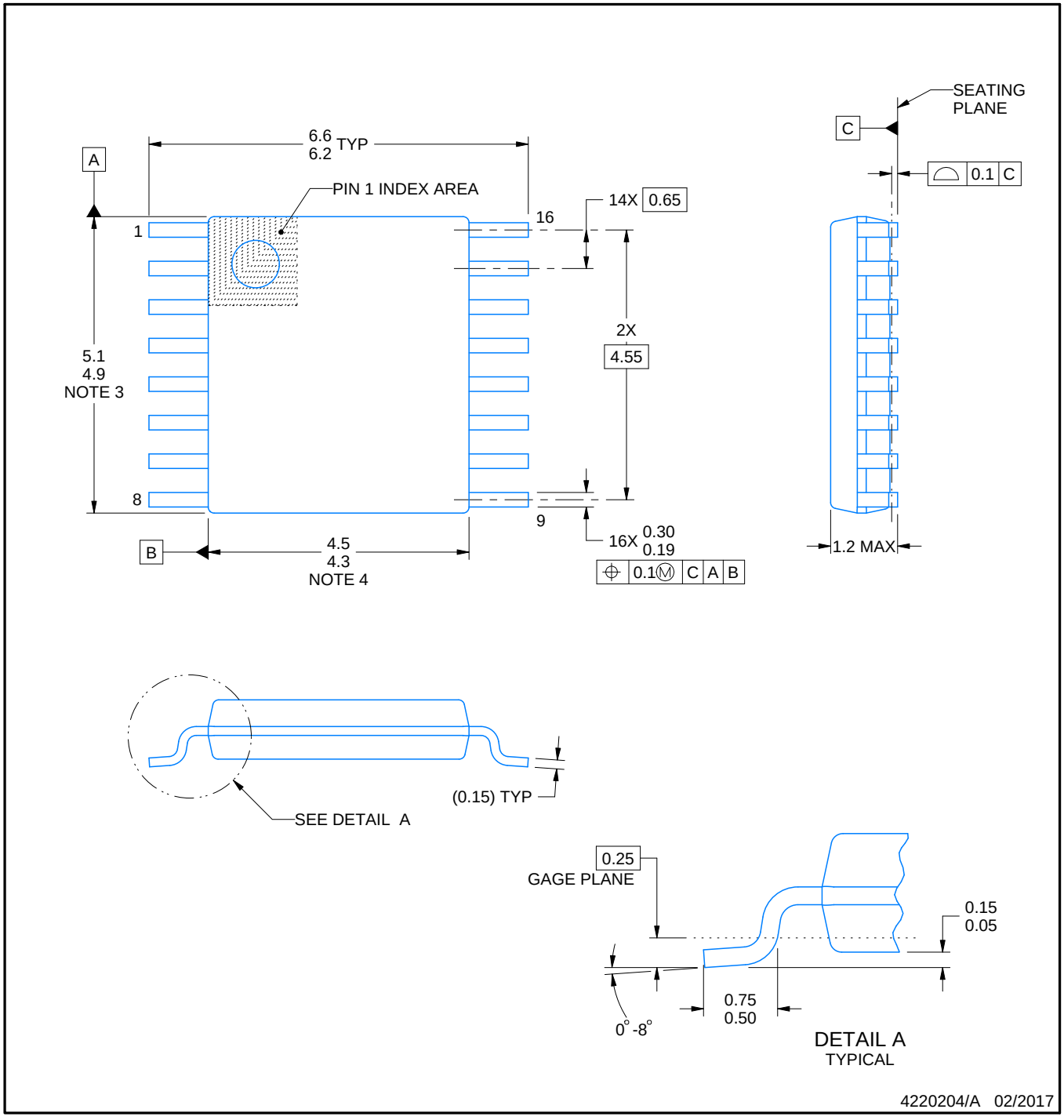
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

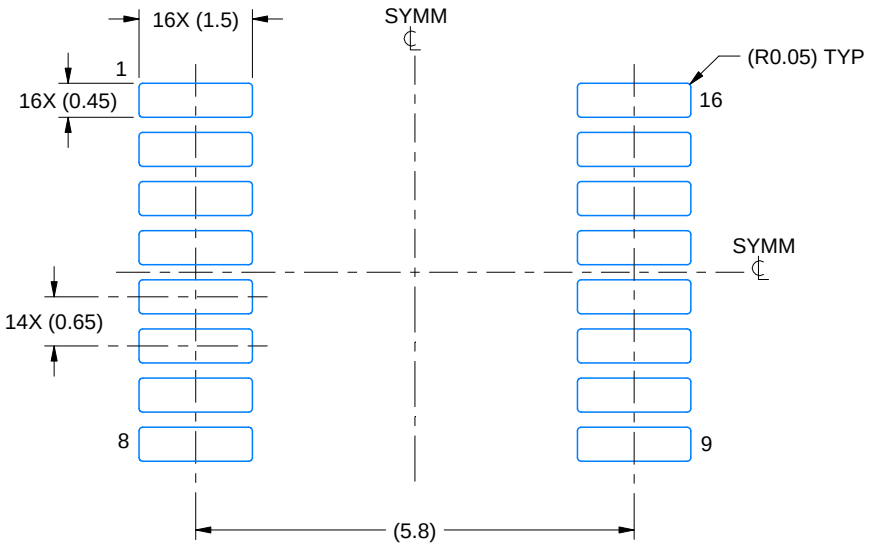
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

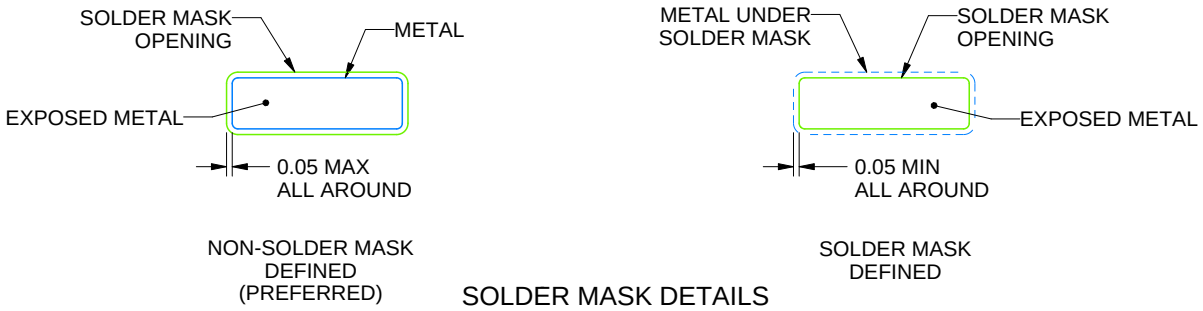


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

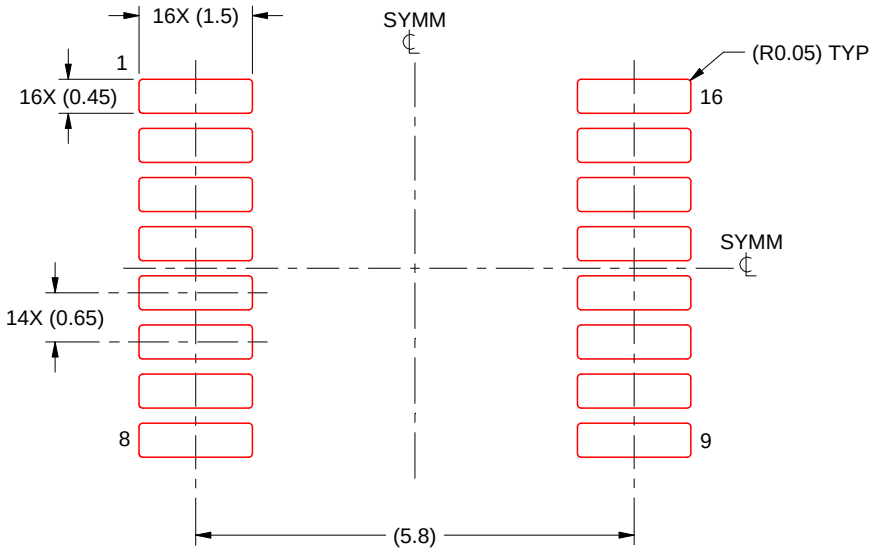


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

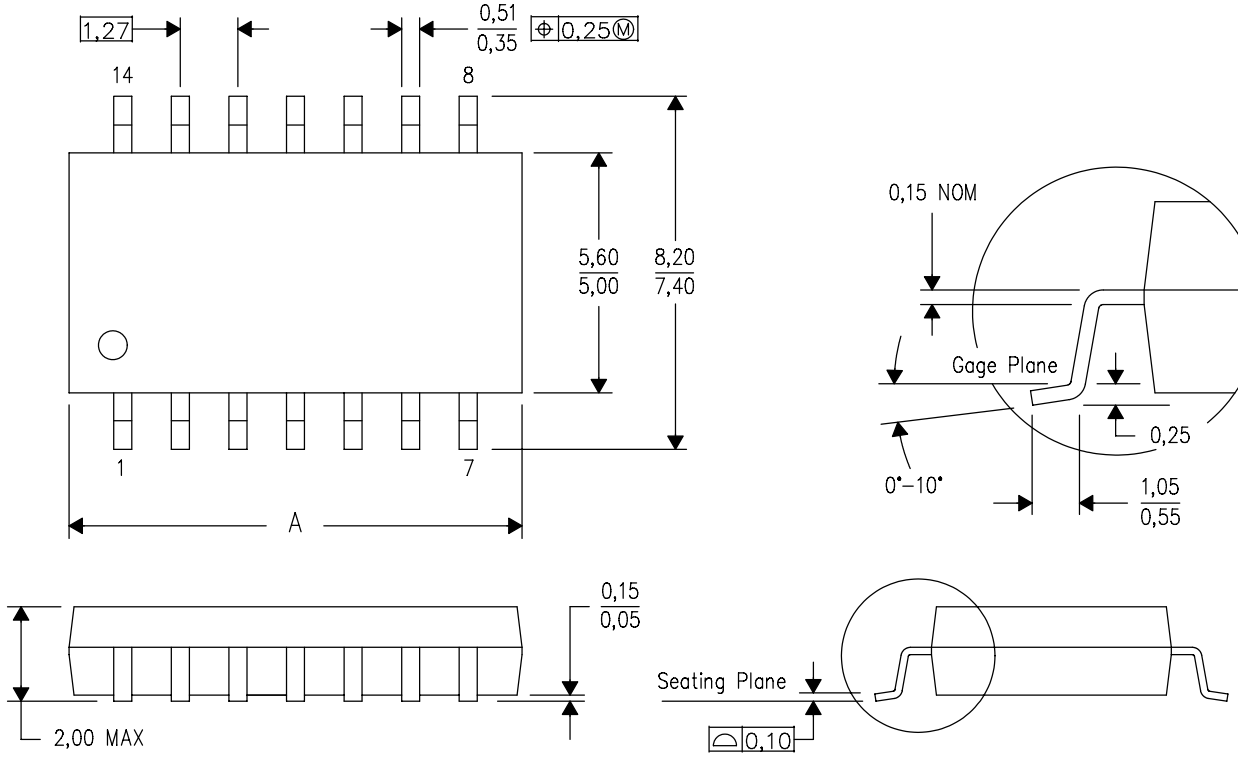
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

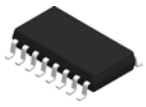
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

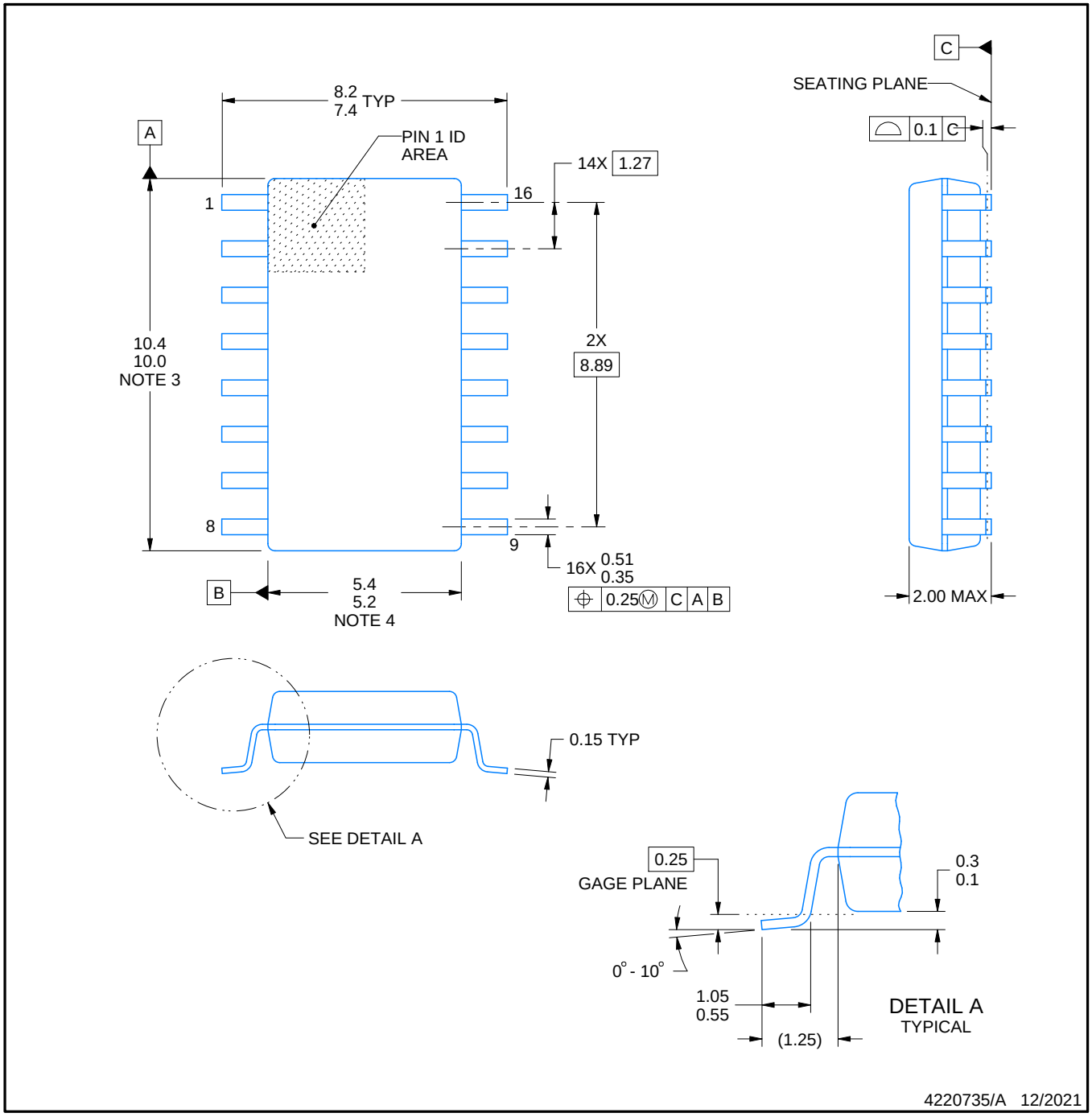


PACKAGE OUTLINE

NS0016A

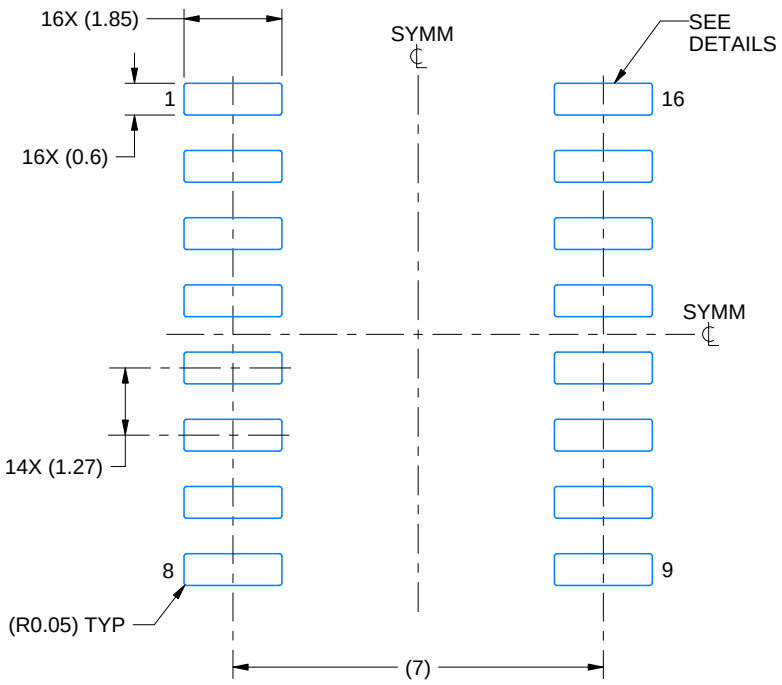
SOP - 2.00 mm max height

SOP

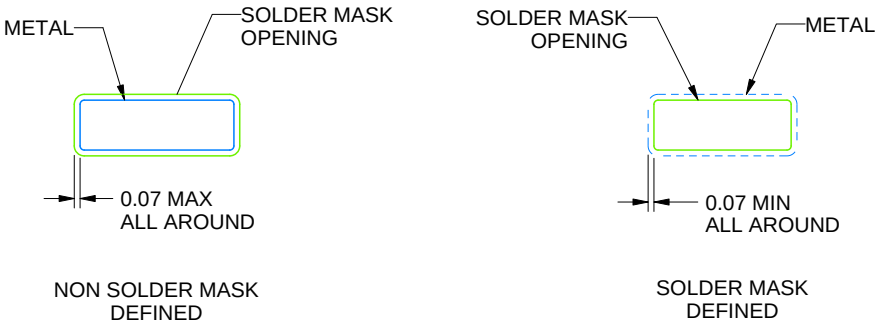


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

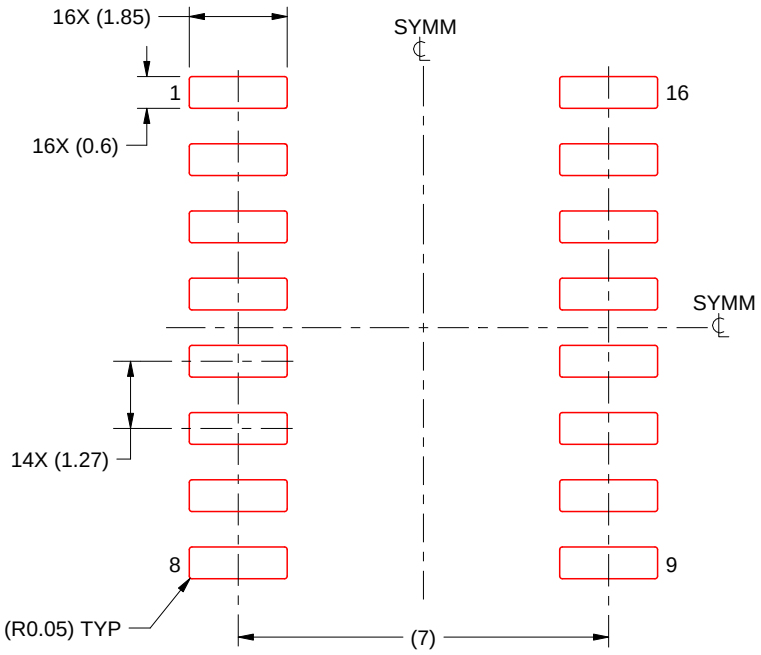
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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