# AFE7954 クワッド RF サンプリング 12GSPS D/A コンバータ (DAC)

## 1 特長

- データシート全体のご請求
- クワッド RF サンプリング 12GSPS DAC
- 最大 RF 信号帯域幅:
  - 4TX:1200MHz または
  - 2TX:2400MHz
- RF 周波数範囲:600MHz～12GHz
- デジタル・ステップ・アッテネータ (DSA):
  - TX:40dB レンジ、0.125dB ステップ
- シングルまたはデュアル・バンド DUC
- TX に対応する 16 個の NCO
- DAC の内部 PLL / VCO、または DAC サンプル・レートでの外部クロックを選択可能
- SerDes データ・インターフェイス:
  - JESD204B、JESD204C 適合
  - 最高 29.5Gbps を発揮する 8 つの SerDes トランシーバ
  - サブクラス 1 のマルチデバイス同期
- パッケージ:17mm × 17mm FCBGA、0.8mm ピッチ

## 2 アプリケーション

- レーダー
- 追尾フロント・エンド
- 防衛無線
- 戦術通信網
- ワイヤレス通信テスト

## 3 概要

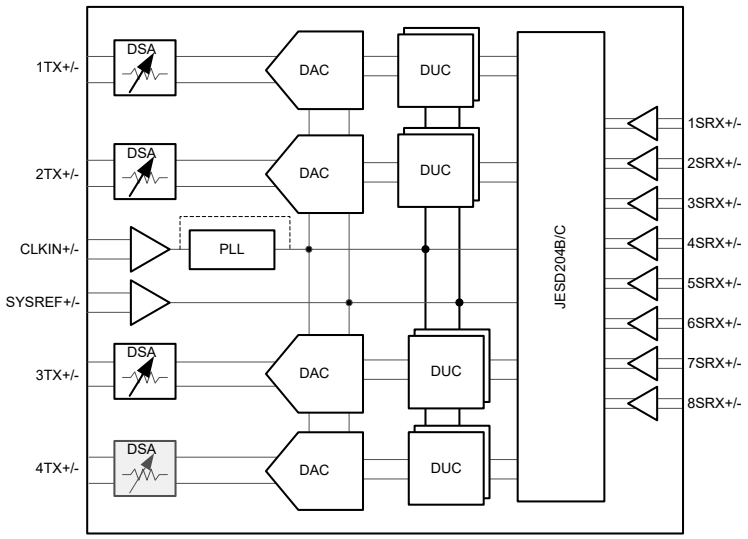
AFE7954 は、高性能、広帯域幅のクワッド・チャネル RF サンプリング DAC です。このデバイスは、最大 12GHz で動作するため、追加の周波数変換段を必要とせず、L、S、C、X バンドの周波数範囲について直接 RF サンプリングが可能です。こうした密度と柔軟性の向上により、多くのチャネル数を持つマルチミッション・システムが可能になります。

信号パスは、4 個の DAC (TX) で最大 1200MHz の信号帯域幅、または 2 個の DAC で 2400MHz を実現する、補間およびデジタル昇圧変換オプションをサポートしています。DUC の出力は、2 次ナイキスト動作を拡張する混在モード出力方式で 12GSPS の DAC (D/A コンバータ) を駆動します。DAC 出力は、40dB レンジ、1dB アナログ・ステップ、0.125dB デジタル・ステップの可変ゲイン・アンプ (TX DSA) を内蔵しています。

**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ・サイズ (2) |
|---|---|---|
| AFE7954 | FC-BGA | 17mm × 17mm |

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。




**機能ブロック図**

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## 4 概要 (続き)

各レシーバ・チェーンは、3GSPS の ADC (A/D コンバータ) に接続された 25dB レンジの DSA (デジタル・ステップ・アッテネータ) を備えています。各レシーバ・チャネルは、外部または内部の自律的な AGC (自動ゲイン制御) を補助するためのアナログ・ピーク電力検出器とさまざまなデジタル電力検出器、およびデバイスの信頼性を確保するための RF 過負荷検出器を備えています。柔軟なデシメーション・オプションによりデータ帯域幅を最適化でき、FB パスなしの 4 つの RX では最高 1200MHz、2 つの FB パス付き (それぞれ 1200MHz の帯域幅) では最高 600MHz が得られます。

## 5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|---|---|---|
| July 2023 | * | Initial Release |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage Range | DVDD0P9, VDDT0P9 | –0.3 | 1.2 | V |
| | VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML | –0.3 | 1.4 | V |
| | VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8 | –0.5 | 2.1 | V |
| Pin Volatge Range | {1/2/3/4}TXOUT+/- | –0.5 | VDDTX1P8+0.3 | V |
| | REFCLK+/-, SYSREF+/- | –0.3 | 1.4 | V |
| | {1:8}SRX+/- | –0.3 | 1.4 | V |
| | GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1 | –0.5 | VDD1P8GPIO + 0.3 | V |
| | IFORCE, VSENSE | –0.3 | VDDCLK1P8 + 0.3 | V |
| | SRDAMUX1, SRDAMUX2 | –0.3 | VDDA1P8+0.3 | V |
| Peak Input Current | any input | | 20 | mA |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 1000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins | 150 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| DVDD0P9, VDDT0P9 | Supply voltage 0.9V | 0.9 | 0.925 | 0.95 | V |
| VDD1P2{RX/TXCLK/TXENC/FB/PLL/ PLLCLKREF/FBCML/RXCML} | Supply voltage 1.2V | 1.15 | 1.2 | 1.25 | V |
| VDD1P8{RX/RXCLK/TX/TXDAC/ TXENC/PLL/PLLVCO/FB/FBCLK/ GPIO}, VDDA1P8 | Supply voltage 1.8V | 1.75 | 1.8 | 1.85 | V |
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating Junction Temperature | | | 110(1) | °C |
| | Maximum Operating Junction Temperature | 125 | | | °C |

(1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to SBAA403 application note for additional details

## 6.4 Thermal Information AFE79xx

| THERMAL METRIC(1) | | 17mmx17mm FC-BGA 400 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 16.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.42 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 4.85 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.12 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 4.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Transmitter Electrical Characteristics

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{DAC}$ = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $DAC_{RES}$ | DAC resolution | | | 14 | | bits |
| $f_{RFout}$ | RF output frequency range | $f_{DAC}$ = 12 GSPS, 1st Nyquist | 600 | | 6000 | MHz |
| | | $f_{DAC}$ = 12 GSPS, 2nd Nyquist | 6000 | | 12000 | |
| | | $f_{DAC}$ = 9 GSPS, 1st Nyquist | 600 | | 4500 | |
| | | $f_{DAC}$ = 9 GSPS, 2nd Nyquist | 4500 | | 9000 | |
| | | $f_{DAC}$ = 6 GSPS, 1st Nyquist | 600 | | 3000 | |
| | | $f_{DAC}$ =6 GSPS, 2nd Nyquist | 3000 | | 6000 | |
| $P_{max\_FS}$ | Max Full Scale Output Power, max gain 1 tone, at device pins | $f_{out}$ = 850 MHz, $f_{DAC}$ = 5898.24 MSPS, -0.5dBFS | | 4.2 | | dBm |
| | | $f_{out}$ = 1800 MHz, $f_{DAC}$ = 5898.24 MSPS, -0.5dBFS | | 4.6 | | dBm |
| | | $f_{out}$ = 2600 MHz, $f_{DAC}$ = 8847.36 MSPS, -0.5dBFS | | 4.0 | | dBm |
| | | $f_{out}$ = 3500 MHz, -0.5dBFS | | 3.9 | | dBm |
| | | $f_{out}$ = 4900 MHz, -0.5dBFS | | 3.1 | | dBm |
| | | $f_{out}$ = 3500 MHz, $f_{DAC}$ = 5898.24 MSPS, -0.5dBFS, straight mode | | 1.0 | | dBm |
| | | $f_{out}$ = 4900 MHz, $f_{DAC}$ = 5898.24 MSPS, -0.5dBFS, straight mode | | 0.1 | | dBm |
| | | $f_{out}$ = 4900 MHz, $f_{DAC}$ = 8847.36 MSPS, -0.5dBFS, straight mode | | -0.7 | | dBm |
| | | $f_{out}$ = 8100 MHz, -0.1dBFS, mixed mode | | -2.8 | | dBm |
| | | $f_{out}$ = 9600 MHz, -0.1dBFS, mixed mode | | -4.3 | | dBm |
| $R_{TERM}$ | Output termination resistor | Default setting | | 50 | | Ω |
| $ATT_{range}$ | DSA Attenuation range | | | 40 | | dB |
| $ATT_{step}$ | DSA Analog Attenuation step | | | 1.0 | | dB |
| | DSA Attenuation step accuracy (DNL) | 0 < Atten < 40dB, before calibration | | ±0.2 | | dB |
| | DSA Attenuation step accuracy (DNL) | 0 < Atten < 40dB, after calibration | | ±0.1 | | dB |
| $ATT_{phase-err}$ | DSA Gain Steps Phase accuracy, any 8dB range | $f_{out}$ = 850MHz(2) | | ±1 | | deg |
| | | $f_{out}$ = 1800MHz(2) | | ±1 | | deg |
| | | $f_{out}$ =2600MHz(2) | | ±1 | | deg |
| | | $f_{out}$ = 3500MHz(2) | | ±1 | | |
| | | $f_{out}$ = 4900MHz(2) | | ±1 | | deg |
| | | $f_{out}$ = 8100MHz(2) | | ±2 | | deg |
| | | $f_{out}$ = 9600MHz(2) | | ±2 | | deg |
| $G_{flat}$ | Gain flatness | any 20MHz | | 0.1 | | dB |
| | | 600MHz BW, $F_{out}$ < 4.9G | | 1.2 | | |

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{DAC}$ = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| IMD3 | 3rd Order Intermodulation distortion, 2 tones at $f_{IF}$±10 MHz | $f_{out}$ = 850MHz, -7dBFS each tone | | -66 | | dBc |
| | | $f_{out}$ = 1800MHz, -7dBFS each tone | | -63 | | dBc |
| | | $f_{out}$ = 2600MHz, -7dBFS each tone | | -62 | | dBc |
| | | $f_{out}$ = 3500MHz, -7dBFS each tone | | -61 | | dBc |
| | | $f_{out}$ = 4900MHz, -7dBFS each tone | | -57 | | dBc |
| | | $f_{out}$ = 8100MHz, -7dBFS each tone | | -55 | | dBc |
| | | $f_{out}$ = 9600MHz, -7dBFS each tone | | -52 | | dBc |
| | | $f_{out}$ = 850MHz, -13dBFS each tone | | -74.4 | | dBc |
| | | $f_{out}$ = 1800MHz, -13dBFS each tone | | -71.1 | | dBc |
| | | $f_{out}$ = 2600MHz, -13dBFS each tone | | -73 | | dBc |
| | | $f_{out}$ = 3500MHz, -13dBFS each tone | | -72 | | dBc |
| | | $f_{out}$ = 4900MHz, -13dBFS each tone | | -67.8 | | dBc |
| | | $f_{out}$ = 8100MHz, -13dBFS each tone | | -64 | | dBc |
| | | $f_{out}$ = 9600MHz, -13dBFS each tone | | -68 | | dBc |
| SFDR | Spurious Free Dynamic Range (within Nyquist zone) | $f_{out}$ = 850 MHz | | 50.8 | | dBc |
| | | $f_{out}$ = 1800 MHz | | 51.9 | | dBc |
| | | $f_{out}$ = 2600 MHz | | 42 | | dBc |
| | | $f_{out}$ = 3500 MHz | | 44 | | dBc |
| | | $f_{out}$= 4900 MHz | | 46.1 | | dBc |
| $f_S/2 - f_{OUT}$ | Interleaving Image | $f_{DAC}$ = 5898.24MSPS, interleave mode | | -51.9 | | dBc |
| | | $f_{DAC}$ = 8847.36 MSPS, interleave mode | | -46.0 | | dBc |
| | | $f_{DAC}$ = 11796.48MSPS, interleave mode | | -41 | | dBc |
| HD2 | 2nd Harmonic Distortion (within Nyquist zone) | $f_{out}$ = 850 MHz | | -49 | | dBc |
| | | $f_{out}$ = 1800 MHz | | -53 | | dBc |
| | | $f_{out}$ = 2600 MHz | | -50 | | dBc |
| | | $f_{out}$ = 3500 MHz | | -48 | | dBc |
| | | $f_{out}$= 4900 MHz | | -47 | | dBc |
| | | $f_{out}$= 8100 MHz | | -50 | | dBc |
| | | $f_{out}$= 9600 MHz | | -53 | | dBc |
| | | $f_{out}$ = 850 MHz, $A_{OUT}$=-12dBFS | | -60 | | dBc |
| | | $f_{out}$ = 1800 MHz, $A_{OUT}$=-12dBFS | | -64 | | dBc |
| | | $f_{out}$ = 2600 MHz, $A_{OUT}$=-12dBFS | | -45 | | dBc |
| | | $f_{out}$ = 3500 MHz, $A_{OUT}$=-12dBFS | | -57 | | dBc |
| | | $f_{out}$= 4900 MHz, $A_{OUT}$=-12dBFS | | -58 | | dBc |
| | | $f_{out}$= 8100 MHz, $A_{OUT}$=-12dBFS | | -60 | | dBc |
| | | $f_{out}$= 9600 MHz, $A_{OUT}$=-12dBFS | | -62 | | dBc |

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{DAC}$ = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| HD3 | 3rd Harmonic Distortion (within Nyquist zone) | $f_{out}$ = 850 MHz | | -62 | | dBc |
| | | $f_{out}$ = 1800 MHz | | -55 | | dBc |
| | | $f_{out}$ = 2600 MHz | | -57 | | dBc |
| | | $f_{out}$ = 3500 MHz | | -60 | | dBc |
| | | $f_{out}$= 4900 MHz | | -54 | | dBc |
| | | $f_{out}$= 8100 MHz | | -54 | | dBc |
| | | $f_{out}$= 9600 MHz | | -56 | | dBc |
| | | $f_{out}$ = 850 MHz, $A_{OUT}$=-12dBFS | | -80 | | dBc |
| | | $f_{out}$ = 1800 MHz, $A_{OUT}$=-12dBFS | | -79 | | dBc |
| | | $f_{out}$ = 2600 MHz, $A_{OUT}$=-12dBFS | | -77 | | dBc |
| | | $f_{out}$ = 3500 MHz, $A_{OUT}$=-12dBFS | | -77 | | dBc |
| | | $f_{out}$= 4900 MHz, $A_{OUT}$=-12dBFS | | -78 | | dBc |
| | | $f_{out}$= 8100 MHz, $A_{OUT}$=-12dBFS | | -82 | | dBc |
| | | $f_{out}$= 9600 MHz, $A_{OUT}$=-12dBFS | | -80 | | dBc |
| HDn, n >= 4 | Harmonic Distortion n >= 4 (within Nyquist zone) | $f_{out}$ = 850 MHz | | -81 | | dBc |
| | | $f_{out}$ = 1800 MHz | | -88 | | dBc |
| | | $f_{out}$ = 2600 MHz | | -86 | | dBc |
| | | $f_{out}$ = 3500 MHz | | -79 | | dBc |
| | | $f_{out}$= 4900 MHz | | -86 | | dBc |
| | | $f_{out}$= 8100 MHz | | -87 | | dBc |
| | | $f_{out}$= 9600 MHz | | -85 | | dBc |
| | | $f_{out}$ = 850 MHz, $A_{OUT}$=-12dBFS | | -93 | | dBc |
| | | $f_{out}$ = 1800 MHz, $A_{OUT}$=-12dBFS | | -98 | | dBc |
| | | $f_{out}$ = 2600 MHz, $A_{OUT}$=-12dBFS | | -84 | | dBc |
| | | $f_{out}$ = 3500 MHz, $A_{OUT}$=-12dBFS | | -87 | | dBc |
| | | $f_{out}$= 4900 MHz, $A_{OUT}$=-12dBFS | | -87 | | dBc |
| | | $f_{out}$= 8100 MHz, $A_{OUT}$=-12dBFS | | -87 | | dBc |
| | | $f_{out}$= 9600 MHz, $A_{OUT}$=-12dBFS | | -87 | | dBc |
| SFDR +/- 250 MHz | Spurious Free Dynamic Range within +/- 250 MHz | $f_{out}$ = 850 MHz | | 68.5 | | dBc |
| | | $f_{out}$ = 1800 MHz | | 79.4 | | dBc |
| | | $f_{out}$ = 2600 MHz | | 77 | | dBc |
| | | $f_{out}$ = 3500 MHz | | 75 | | dBc |
| | | $f_{out}$= 4900 MHz | | 76 | | dBc |
| | | $f_{out}$= 8100 MHz | | 61 | | dBc |
| | | $f_{out}$= 9600 MHz | | 64 | | dBc |
| $f_S/4$ | Fixed Spur | $f_{DAC}$ = 5898.24MSPS | | -64 | | dBFS |
| | | $f_{DAC}$ = 8847.36MSPS | | -75 | | dBFS |
| | | $f_{DAC}$ = 11796.48MSPS | | -67 | | dBFS |
| $f_S/2$ | Fixed Spur | $f_{DAC}$ = 5898.24MSPS | | -49 | | dBFS |
| | | $f_{DAC}$ = 8847.36MSPS | | -48 | | dBFS |
| | | $f_{DAC}$ = 11796.48 MSPS | | -48 | | dBFS |

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{DAC}$ = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 3*$f_S$/4 | Fixed Spur | 2nd Nyquist, $f_{DAC}$ = 5898.24MSPS | | -76 | | dBFS |
| | | 2nd Nyquist, $f_{DAC}$ = 8847.36MSPS | | -89 | | dBFS |
| | | 2nd Nyquist, $f_{DAC}$ = 11796.48MSPS | | -63 | | dBFS |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{out}$ = 0.85 GHz | Atten=0dB, Pout=-13dBFs | | -68.5 | | dBc |
| | | Atten=20dB,Pout=-13dBFs | | -67.2 | | dBc |
| | | Atten=28dB,Pout=-13dBFs | | -64.5 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -53.9 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{out}$ = 1.8425 GHz | Atten=0dB,Pout=-13dBFs | | -70.7 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -68.3 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -62.9 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -52.0 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{out}$ = 2.6 GHz | Atten=0dB, Pout=-13dBFs | | -71 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -68 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -62 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -51.3 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{out}$ = 3.5 GHz | Atten=0dB, Pout=-13dBFs | | -70 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -67 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -60 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -49.8 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{out}$ = 4.9 GHz | Atten=0dB, Pout=-13dBFs | | -68.8 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -65.9 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -60.6 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -49.5 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{out}$ = 2.6 GHz | Atten=0dB, Pout=-13dBFs | | -65 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -62 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -55 | | dBc |
| | | Atten=39dB,Pout=-13dBFs | | -44.3 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{out}$ = 3.5 GHz | Atten=0dB, Pout=-13dBFs | | -64 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -59 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -52 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -41.1 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{out}$ = 4.9 GHz | Atten=0dB, Pout=-13dBFs | | -64.1 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -60.4 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -53.5 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -42.5 | | dBc |
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{out}$ = 8.1 GHz | Atten=0dB, Pout=-13dBFs | | -58 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -53 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -46 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -36 | | dBc |

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{DAC}$ = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $ACPR_{1xcarr}$ | ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{out}$ = 9.6 GHz | Atten=0dB, Pout=-13dBFs | | -57 | | dBc |
| | | Atten=20dB, Pout=-13dBFs | | -50 | | dBc |
| | | Atten=28dB, Pout=-13dBFs | | -42 | | dBc |
| | | Atten=39dB, Pout=-13dBFs | | -31 | | dBc |
| EVM | Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise | $F_{out}$ =0.85 GHz, $P_{OUT}$=-13dBFs | | 0.2 | | % |
| | | $F_{out}$ =1.8425 GHz, $P_{OUT}$=-13dBFs | | 0.3 | | % |
| | | $F_{out}$ =2.6 GHz, $P_{OUT}$=-13dBFs | | 0.28 | | % |
| | | $F_{out}$ =3.5 GHz, $P_{OUT}$=-13dBFs | | 0.38 | | % |
| | | $F_{out}$ =4.9 GHz, $P_{OUT}$=-13dBFs | | 0.4 | | % |
| $NSD_{dBFS}$ | Noise Spectral Density 20MHz offset $f_{OUT}$ = 0.85 GHz | Atten=0dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -157.6 | | dBFS/Hz |
| | | Atten=20dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -153.3 | | dBFS/Hz |
| | | Atten=28dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -147.9 | | dBFS/Hz |
| | | Atten=39dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -136.9 | | dBFS/Hz |
| $NSD_{dBFS}$ | Noise Spectral Density 20MHz offset $f_{OUT}$ = 1.8 GHz | Atten=0dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -158.4 | | dBFS/Hz |
| | | Atten=20dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -152.2 | | dBFS/Hz |
| | | Atten=28dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -145.6 | | dBFS/Hz |
| | | Atten=39dB, $f_{DAC}$ = 5898.24MSPS, Pout=-13dBFs | | -134.6 | | dBFS/Hz |
| $NSD_{dBFS}$ | Noise Spectral Density 20MHz offset $f_{OUT}$ = 2.6 GHz | Atten=0dB, $f_{DAC}$ = 8847.36MSPS, Pout=-13dBFs | | -157 | | dBFS/Hz |
| | | Atten=20dB, $f_{DAC}$ = 8847.36MSPS, Pout=-13dBFs | | -151 | | dBFS/Hz |
| | | Atten=28dB, $f_{DAC}$ = 8847.36MSPS, Pout=-13dBFs | | -144 | | dBFS/Hz |
| | | Atten=39dB, $f_{DAC}$ = 8847.36MSPS, Pout=-13dBFs | | -133.0 | | dBFS/Hz |
| $NSD_{dBFS}$ | Noise Spectral Density 20MHz offset $F_{out}$ =3.5 GHz | Atten=0dB, Pout=-13dBFs | | -158 | | dBFS/Hz |
| | | Atten=20dB, Pout=-13dBFs | | -150 | | dBFS/Hz |
| | | Atten=28dB, Pout=-13dBFs | | -143 | | dBFS/Hz |
| | | Atten=39dB, Pout=-13dBFs | | -131.8 | | dBFS/Hz |

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{DAC}$ = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $NSD_{dBFS}$ | Noise Spectral Density 20MHz offset $F_{out}$ =4.9 GHz | Atten=0dB, Pout=-13dBFs | | -155.5 | | dBFS/Hz |
| | | Atten=20dB, Pout=-13dBFs | | -147.8 | | dBFS/Hz |
| | | Atten=28dB, Pout=-13dBFs | | -140.8 | | dBFS/Hz |
| | | Atten=39dB, Pout=-13dBFs | | -129.6 | | dBFS/Hz |
| $NSD_{dBFS}$ | Noise Spectral Density 50MHz offset $F_{out}$ =8.1 GHz | Atten=0dB, Pout=-13dBFs | | -153 | | dBFS/Hz |
| | | Atten=20dB, Pout=-13dBFs | | -147 | | dBFS/Hz |
| | | Atten=28dB, Pout=-13dBFs | | -140 | | dBFS/Hz |
| | | Atten=39dB, Pout=-13dBFs | | -129 | | dBFS/Hz |
| $NSD_{dBFS}$ | Noise Spectral Density 50MHz offset $F_{out}$ =9.6 GHz | Atten=0dB, Pout=-13dBFs | | -152 | | dBFS/Hz |
| | | Atten=20dB, Pout=-13dBFs | | -147 | | dBFS/Hz |
| | | Atten=28dB, Pout=-13dBFs | | -140 | | dBFS/Hz |
| | | Atten=39dB, Pout=-13dBFs | | -129 | | dBFS/Hz |
| S22 | Output Return Loss, <6GHz, +/- fc * 10% | with matching | | -17 | | dB |
| | Output Return Loss, >8GHz, +/- fc * 10% | with matching | | -10 | | dB |
| Isolation | Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT(1) | $f_{out}$ = 900 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -49 | | dB |
| | | $f_{out}$ = 1850 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -59 | | dB |
| | | $f_{out}$ = 2600 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -65 | | dB |
| | | $f_{out}$ = 3500 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -66 | | dB |
| | | $f_{out}$= 4900 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -60 | | dB |
| | | $f_{out}$ = 900 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -90 | | dB |
| | | $f_{out}$ = 1850 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -91 | | dB |
| | | $f_{out}$ = 2600 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -93 | | dB |
| | | $f_{out}$ = 3500 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -94 | | dB |
| | | $f_{out}$= 4900 MHz, $f_{DAC}$ = 8847.36MSPS, straight mode | | -83 | | dB |

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{DAC}$ = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $PN_{TXADD}$ | Additive Phase Noise External Clock Mode(3) | $f_{out}$ = 9.6GHz, $f_{OFFSET}$ = 100Hz | | -88 | | dBc/Hz |
| | | $f_{out}$ = 9.6GHz, $f_{OFFSET}$ = 1kHz | | -102 | | dBc/Hz |
| | | $f_{out}$ = 9.6GHz, $f_{OFFSET}$ = 10kHz | | -110 | | dBc/Hz |
| | | $f_{out}$ = 9.6GHz, $f_{OFFSET}$ = 100kHz | | -123 | | dBc/Hz |
| | | $f_{out}$ = 9.6GHz, $f_{OFFSET}$ = 1MHz | | -136 | | dBc/Hz |
| | | $f_{out}$ = 9.6GHz, $f_{OFFSET}$ = 10MHz | | -143 | | dBc/Hz |
| | | $f_{out}$ = 9.6GHz, $f_{OFFSET}$ = 100MHz | | -146 | | dBc/Hz |

(1) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
(2) After DSA calibration procedure
(3) Single side band, input clock phase noise subtracted.

## 6.6 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to $f_{VCO}$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{VCO1}$ | VCO1 min frequency | | | | 7.2 | GHz |
| | VCO1 max frequency | | 7.68 | | | GHz |
| $f_{VCO2}$ | VCO2 min frequency | | | | 8.8 | GHz |
| | VCO2 max frequency | | 9.1 | | | GHz |
| $f_{VCO3}$ | VCO3 min frequency | | | | 9.7 | GHz |
| | VCO3 max frequency | | 10.24 | | | GHz |
| $f_{VCO4}$ | VCO4 min frequency | | | | 11.6 | GHz |
| | VCO4 max frequency | | 12.08 | | | GHz |
| $DIV_{DAC}$ | DAC sample rate divider | | | 1, 2 or 3 | | |
| $DIV_{FBADC}$ | ADC sample rate divider from DAC sample rate | | | 1, 2, 3, 4, 6 or 8 | | |
| $DIV_{RXADC}$ | ADC sample rate divider | | | 1, 2, 3, 4, 6 or 8 | | |
| $PN_{VCO}$ | Closed Loop Phase Noise $F_{PLL}$ = 11.79848 GHz $F_{REF}$=491.52MHz | 600kHz | | -113 | | dBc/Hz |
| | | 800kHz | | -116 | | dBc/Hz |
| | | 1MHz | | -119 | | dBc/Hz |
| | | 1.8MHz | | -125 | | dBc/Hz |
| | | 5MHz | | -133 | | dBc/Hz |
| | | 50MHz | | –141 | | dBc/Hz |
| | Closed Loop Phase Noise $F_{PLL}$=8.84736 GHz $F_{REF}$=491.52MHz | 600kHz | | -114 | | dBc/Hz |
| | | 800kHz | | –118 | | dBc/Hz |
| | | 1MHz | | –120 | | dBc/Hz |
| | | 1.8MHz | | –127 | | dBc/Hz |
| | | 5MHz | | –135 | | dBc/Hz |
| | | 50MHz | | –142 | | dBc/Hz |
| | Closed Loop Phase Noise $F_{PLL}$= 9.8403 GHz $F_{REF}$=491.52MHz | 600kHz | | –113 | | dBc/Hz |
| | | 800kHz | | –116 | | dBc/Hz |
| | | 1MHz | | –119 | | dBc/Hz |
| | | 1.8MHz | | –125 | | dBc/Hz |
| | | 5MHz | | –134 | | dBc/Hz |
| | | 50MHz | | –140 | | dBc/Hz |
| | Closed Loop Phase Noise $F_{PLL}$= 7.86432GHz $F_{REF}$=491.52MHz | 600kHz | | –116 | | dBc/Hz |
| | | 800kHz | | –119 | | dBc/Hz |
| | | 1MHz | | –122 | | dBc/Hz |
| | | 1.8MHz | | –127 | | dBc/Hz |
| | | 5MHz | | –136 | | dBc/Hz |
| | | 50MHz | | –143 | | dBc/Hz |
| $F_{rms}$ | Clock PLL integrated phase error(1) | $f_{PLL}$=11.79848 GHz, [1KHz, 100MHz] | | -43.4 | | dBc/Hz |
| | | $f_{PLL}$=8.8536 GHz, [1KHz, 100MHz] | | -47.6 | | dBc/Hz |
| | | $f_{PLL}$=9.8304 GHz, [1KHz, 100MHz] | | -46.2 | | dBc/Hz |
| $f_{PFD}$ | PFD frequency | | 100 | | 500 | MHz |
| $PN_{pll\_flat}$ | Normalized PLL flat Noise | $f_{VCO}$ = 11796.48MHz | | –226.5 | | dBc/Hz |
| $F_{REF}$ | Input Clock frequency | | 0.1 | | 12 | GHz |

## 6.6 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to $f_{VCO}$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{SS}$ | Input Clock level | | 0.6 | | 1.8 | Vppdiff |
| Coupling | | | | AC Coupling Only | | |
| | REFCLK input impedance(2) | Parallel resistance | | 100 | | Ω |
| | | Parallel capacitance | | 0.5 | | pF |

(1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

## 6.7 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CML SerDes Inputs [8:1]SRX+/-** | | | | | | |
| $V_{SRDIFF}$ | SerDes Receiver Input Amplitude | differential | 100 | | 1200 | mVpp |
| $V_{SRCOM}$ | SerDes Input Common Mode | | 0.4 | 0.5 | 0.6 | V |
| $Z_{SRdiff}$ | SerDes Internal Differential Termination(1) | | | 100 | | Ω |
| $F_{SerDes}$ | SerDes Bit Rate | Full rate mode | 19 | | 29.5 | Gbps |
| | | Half rate mode | 9.5 | | 16.25 | Gbps |
| | | Quarter rate mode | 4.75 | | 8.125 | Gbps |
| | Insertion Loss Tolerance(2) | Serdes supply = 1.8V | | 25 | | dB |
| TJ | Total Jitter Tolerance | | | | 0.42 | UI |
| **CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1** | | | | | | |
| $V_{IH}$ | High-Level Input Voltage | | 0.6×VDD1 P8GPIO | | | V |
| $V_{IL}$ | Low-Level Input Voltage | | | | 0.4×VDD1 P8GPIO | V |
| $I_{IH}$ | High-Level Input Current | | –250 | | 250 | µA |
| $I_{IL}$ | Low-Level Input Current | | –250 | | 250 | µA |
| $C_L$ | CMOS input capacitance | | | 2 | | pF |
| $V_{OH}$ | High-Level Ouput Voltage | | VDD1P8G PIO–0.2 | | | V |
| $V_{OL}$ | Low-Level Output Voltage | | | | 0.2 | V |
| **Differential Inputs: SYSREF+/- Mode A** | | | | | | |
| $Clock_{MODE}$ | | | | PLL Clock Mode Only | | |
| $F_{SYSREFMAX}$ | SYSREF Input Frequency Maximum | | | 40 | | MHz |
| $V_{SWINGSRMAX}$ | SYSREF Input Swing Maximum | | | 1.8 | | Vppdiff(3) |
| $V_{SWINGSRMIN}$ | SYSREF Input Swing Minimum | $f_{REF}$ < 500MHz | | 0.3 | | Vppdiff(3) |
| $V_{SWINGSRMIN}$ | SYSREF Input Swing Minimum | $f_{REF}$ > 500MHz | | 0.6 | | Vppdiff(3) |
| $V_{COMSRMAX}$ | SYSREF Input Common Mode Voltage Maximum | | | 0.8 | | V |
| $V_{COMSRMIN}$ | SYSREF Input Common Mode Voltage Minimum | | | 0.6 | | V |
| $Z_T$ | Input termination | differential | | 100 (1) | | Ω |
| $C_L$ | Input capacitance | Each pin to GND | | 0.5 | | pF |
| **LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-** | | | | | | |
| $V_{ICOM}$ | Input Common Voltage | | | 1.2 | | V |
| $V_{ID}$ | Differential Input Voltage swing | | | 450 | | Vppdiff(3) |
| $Z_T$ | Input termination | differential | | 100 | | Ω |
| **LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-** | | | | | | |
| $V_{OCOM}$ | Output Common Voltage | | | 1.2 | | V |
| $V_{OD}$ | Differential Output Voltage swing | | | 500 | | Vppdiff(3) |
| $Z_T$ | Internal Termination | | | 100 | | Ω |

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Loss tolerance is bump to bump from STX to SRX

(3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

## 6.8 Power Supply Electrical Characteristics

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, $f_{DAC}$ = 9000MSPS interleave mode; $f_{ADC}$ = 3000MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 20Gbps; unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VDD1P8}$ | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX | Mode 1: 4TX<br>TX Dual Band: 96x Int, TX Rate 125 MSPS<br>$f_{DAC}$ = 12 GSPS, $f_{TX}$ = 1.85 + 2.15 GHz<br>JESD: 8/10 coding, 20Gbps<br>TX: 2-16-16-1 | | 564 | | mA |
| | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 | | | 274 | | mA |
| | Group 3C: VDD1P8PLL + VDD1P8PLLVCO | | | 71 | | mA |
| $I_{VDD1P2}$ | Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF | | | 953 | | mA |
| $I_{VDD0P9}$ | Group 1A: DVDD0P9 + VDDT0P9 | | | 1747 | | mA |
| $P_{diss}$ | Power Dissipation | | | 4396 | | mW |
| $I_{VDD1P8}$ | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX | Mode 2: 4TX<br>TX Single Band: 24x Int, TX Rate 500 MSPS<br>$f_{DAC}$ = 12 GSPS, $f_{TX}$ = 2.75 GHz<br>JESD: 8/10 coding, 20Gbps<br>TX: 4-8-4-1 | | 570 | | mA |
| | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 | | | 382 | | mA |
| | Group 3C: VDD1P8PLL + VDD1P8PLLVCO | | | 72 | | mA |
| $I_{VDD1P2}$ | Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF | | | 967 | | mA |
| $I_{VDD0P9}$ | Group 1A: DVDD0P9 + VDDT0P9 | | | 2172 | | mA |
| $P_{diss}$ | Power Dissipation | | | 5011 | | mW |
| $I_{VDD1P8}$ | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX | Mode 3: 4TX<br>TX Single Band: 12x Int, TX Rate 1 GSPS<br>fDAC = 12 GSPS, fTX = 2.75 GHz<br>JESD: 8/10 coding, 20Gbps<br>TX: 8-8-2-1 | | 571 | | mA |
| | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 | | | 495 | | mA |
| | Group 3C: VDD1P8PLL + VDD1P8PLLVCO | | | 72 | | mA |
| $I_{VDD1P2}$ | Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF | | | 969 | | mA |
| $I_{VDD0P9}$ | Group 1A: DVDD0P9 + VDDT0P9 | | | 2465 | | mA |
| $P_{diss}$ | Power Dissipation | | | 5490 | | mW |

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, $f_{DAC}$ = 9000MSPS interleave mode; $f_{ADC}$ = 3000MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 20Gbps; unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VDD1P8}$ | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX | Mode 4: 4TX<br>TX Single Band: 8x Int, TX Rate 1500 MSPS<br>fDAC = 12 GSPS, fTX = 2.75 GHz<br>JESD: 64/66 coding, 24.75Gbps<br>TX: 8-8-2-1 | | 569 | | mA |
| | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 | | | 521 | | mA |
| | Group 3C: VDD1P8PLL + VDD1P8PLLVCO | | | 73 | | mA |
| $I_{VDD1P2}$ | Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF | | | 981 | | mA |
| $I_{VDD0P9}$ | Group 1A: DVDD0P9 + VDDT0P9 | | | 2719 | | mA |
| $P_{diss}$ | Power Dissipation | | | 5786 | | mW |
| $I_{VDD1P8}$ | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX | Mode 5: 2TX<br>TX Single Band: 4x Int, TX Rate 3000 MSPS<br>fDAC = 12 GSPS, fTX = 2.75 GHz<br>JESD: 64/66 coding, 24.75Gbps<br>TX: 8-4-1-1 | | 297 | | mA |
| | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 | | | 446 | | mA |
| | Group 3C: VDD1P8PLL + VDD1P8PLLVCO | | | 72 | | mA |
| $I_{VDD1P2}$ | Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF | | | 544 | | mA |
| $I_{VDD0P9}$ | Group 1A: DVDD0P9 + VDDT0P9 | | | 1575 | | mA |
| $P_{diss}$ | Power Dissipation | | | 3577 | | mW |
| $I_{VDD1P8}$ | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX | Mode 6: Same as Mode 5 in Sleep mode with Sleep pin pulled high. | | 96 | | mA |
| $I_{VDD1P8}$ | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 | | | 330 | | mA |
| $I_{VDD1P8}$ | Group 3C: VDD1P8PLL + VDD1P8PLLVCO | | | 16 | | mA |
| $I_{VDD1P2}$ | Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF | | | 48 | | mA |
| $I_{VDD0P9}$ | Group 1A: DVDD0P9 + VDDT0P9 | | | 302 | | mA |
| $P_{diss}$ | Power Dissipation | | | 1132 | | mW |

## 6.9 Timing Requirements

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, $f_{DAC}$ = 8847.36MSPS; $f_{ADC}$ = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Timing: SYSREF+/-** | | | | | |
| $t_{s(SYSREF)}$ | Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/- | | 50 | | ps |
| $t_{h(SYSREF)}$ | Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/- | | 50 | | ps |
| **Timing: Serial ports** | | | | | |
| $t_{s(SENB)}$ | Setup Time, SENB to Rising Edge of SCLK | | | 15 | ns |
| $t_{h(SENB)}$ | Hold Time, SENB after last Rising Edge of SCLK (1) | | | 5 + $t_{SCLK}$ | ns |
| $t_{s(SDIO)}$ | Setup Time, SDIO valid to Rising Edge of SCLK | | | 15 | ns |
| $t_{h(SDIO)}$ | Hold Time, SDIO valid after Rising Edge of SCLK | | | 5 | ns |
| $t_{(SCLK)\_W}$ | Minimum SCLK period: registers write | | | 25 | ns |
| $t_{(SCLK)\_R}$ | Minimum SCLK period: registers read | | | 50 | ns |
| $t_{d(data\_out)}$ | Minimum Data Output delay after Falling Edge of SCLK | | | 0 | ns |
| | Maximum Data Output delay after Falling Edge of SCLK | | | 15 | ns |
| $t_{RESET}$ | Minimum RESETZ Pulse Width | | 1 | | ms |

(1) SDEN\\ need to be held one more extra clock cycle with the last SCLK edge

## 6.10 Switching Characteristics

Typical values at $T_A$ = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, $f_{DAC}$ = 8847.36MSPS; $f_{ADC}$ = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TX Channel Latency** | | | | | | |
| | SerDes Receiver Analog Delay | Full rate | | 2.8 | | ns |
| $t_{JESDTX}$ | JESD to TX output Latency | LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C) | | 152 | | interface clock cycles(1) |
| | | LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C) | | 176 | | |
| | | LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C) | | 124 | | |
| | | LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C) | | 97 | | |

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

# 7 Device and Documentation Support

## 7.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 7.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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## 7.3 Trademarks

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## 7.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 7.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| AFE7954IABJ | Active | Production | FCBGA (ABJ) \| 400 | 90 \| JEDEC TRAY (5+1) | Yes | SNAGCU \| SNAGCU | Level-3-260C-168 HR | -40 to 85 | AFE7954I |
| AFE7954IABJ.B | Active | Production | FCBGA (ABJ) \| 400 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Call TI | -40 to 85 | |
| AFE7954IALK | Active | Production | FCBGA (ALK) \| 400 | 90 \| JEDEC TRAY (5+1) | No | Call TI | Level-3-220C-168 HR | -40 to 85 | AFE7954 SNPB |
| AFE7954IALK.B | Active | Production | FCBGA (ALK) \| 400 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Call TI | -40 to 85 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

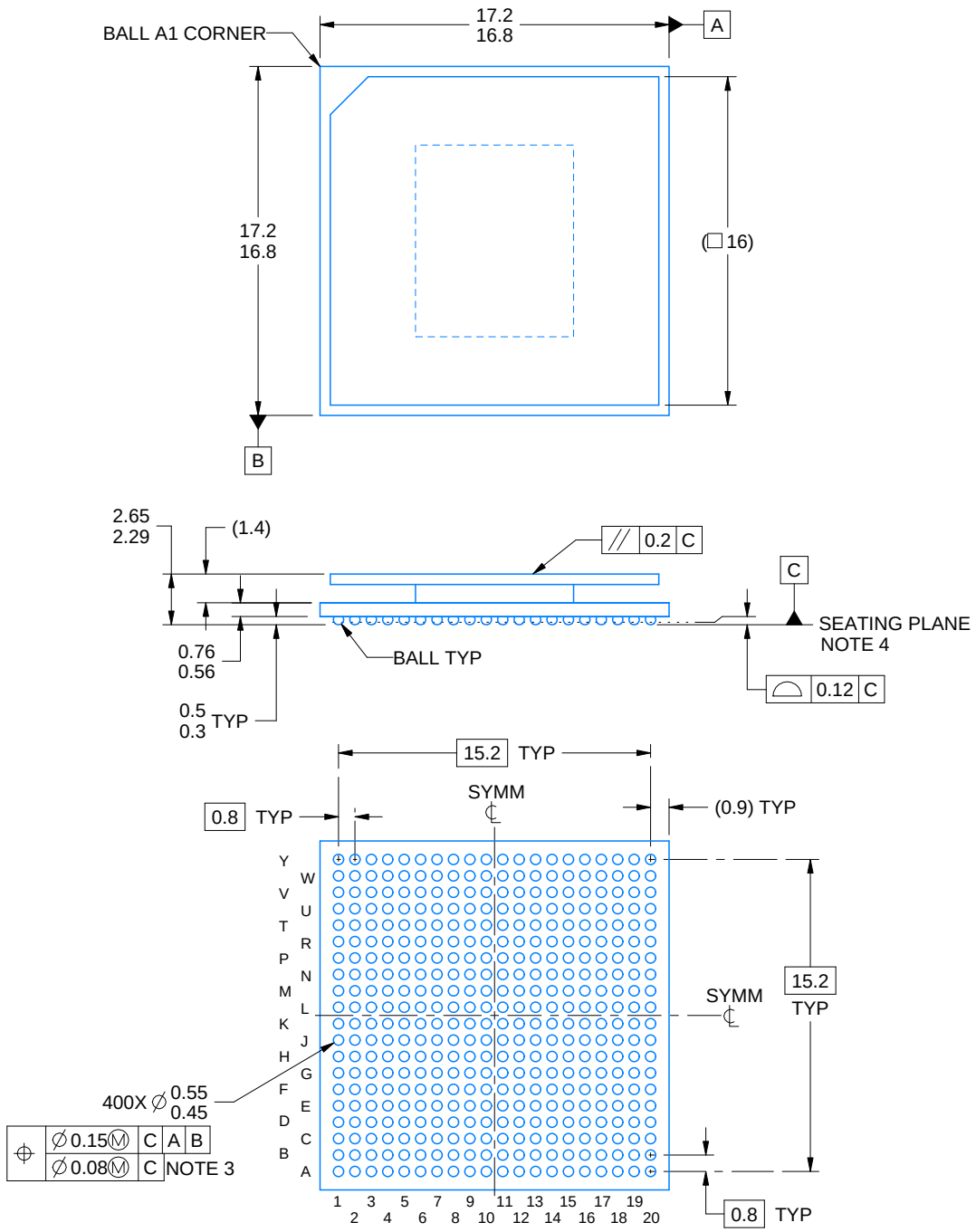
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# PACKAGE OUTLINE

## ABJ0400A

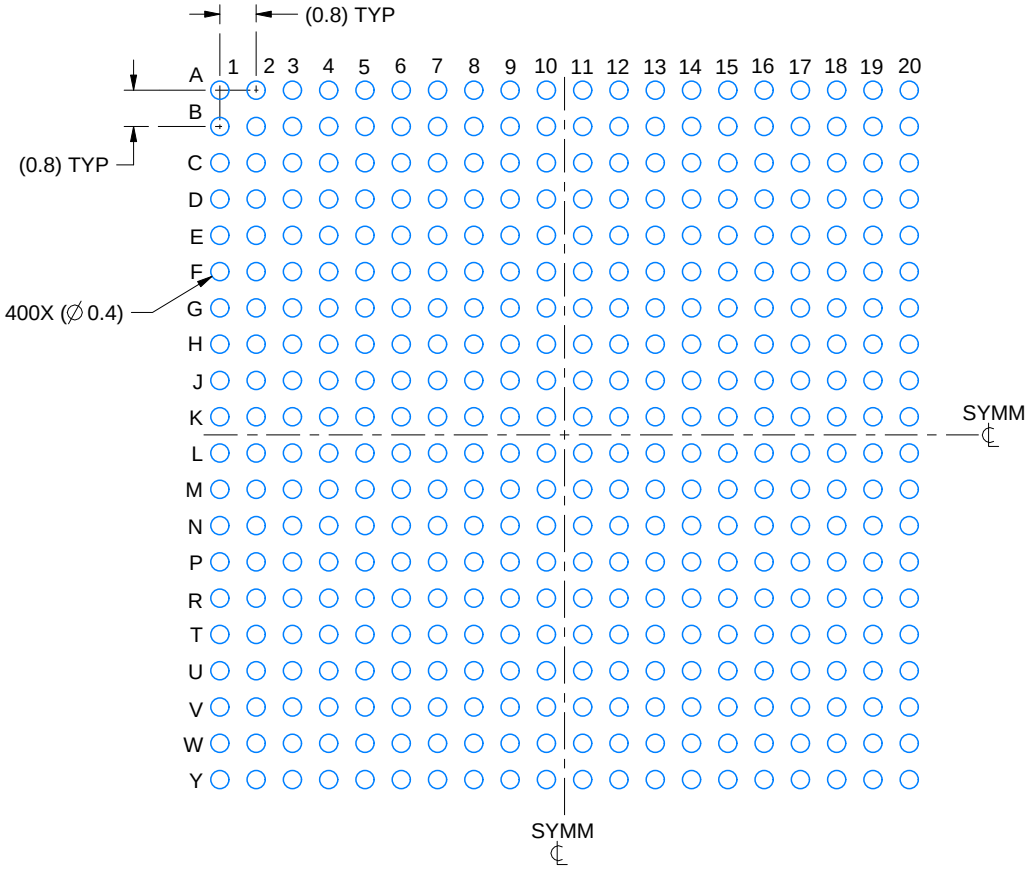
## FCBGA - 2.65 mm max height

BALL GRID ARRAY

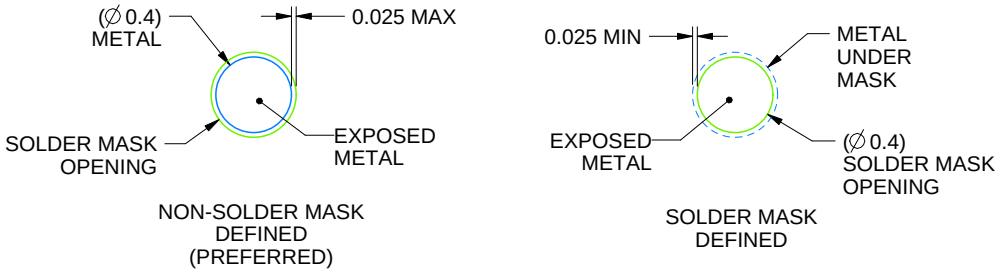



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

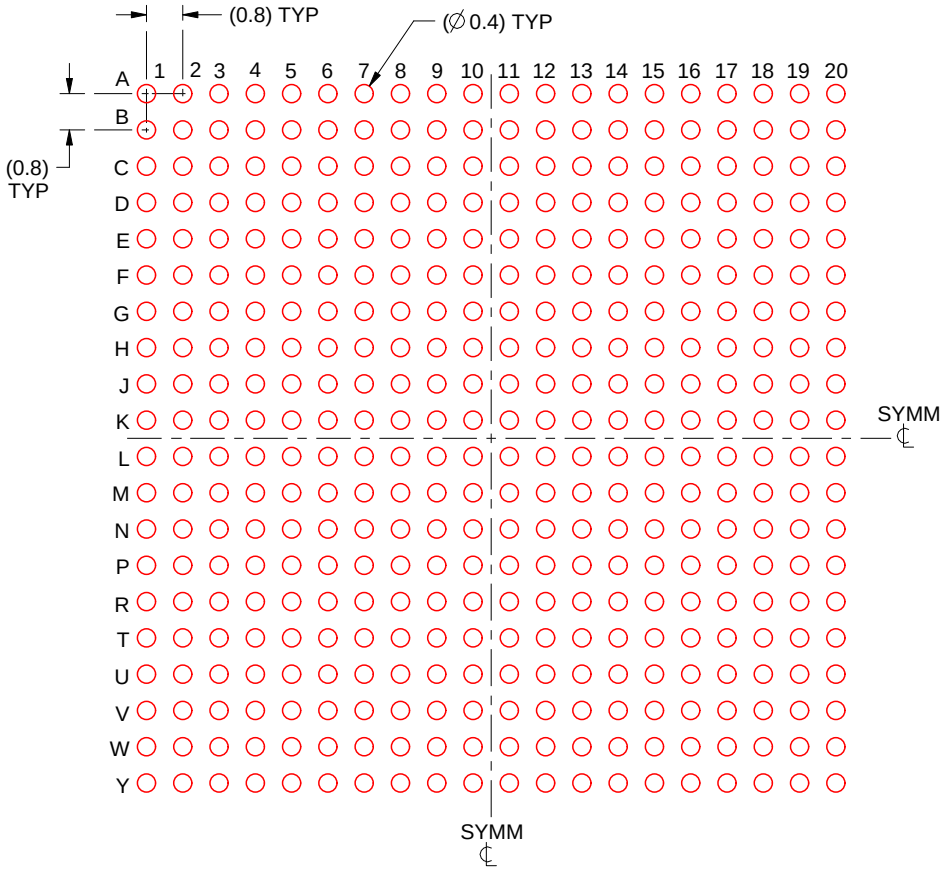



SOLDER MASK DETAILS
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).




SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4221311/D 03/2023

NOTES: (continued)

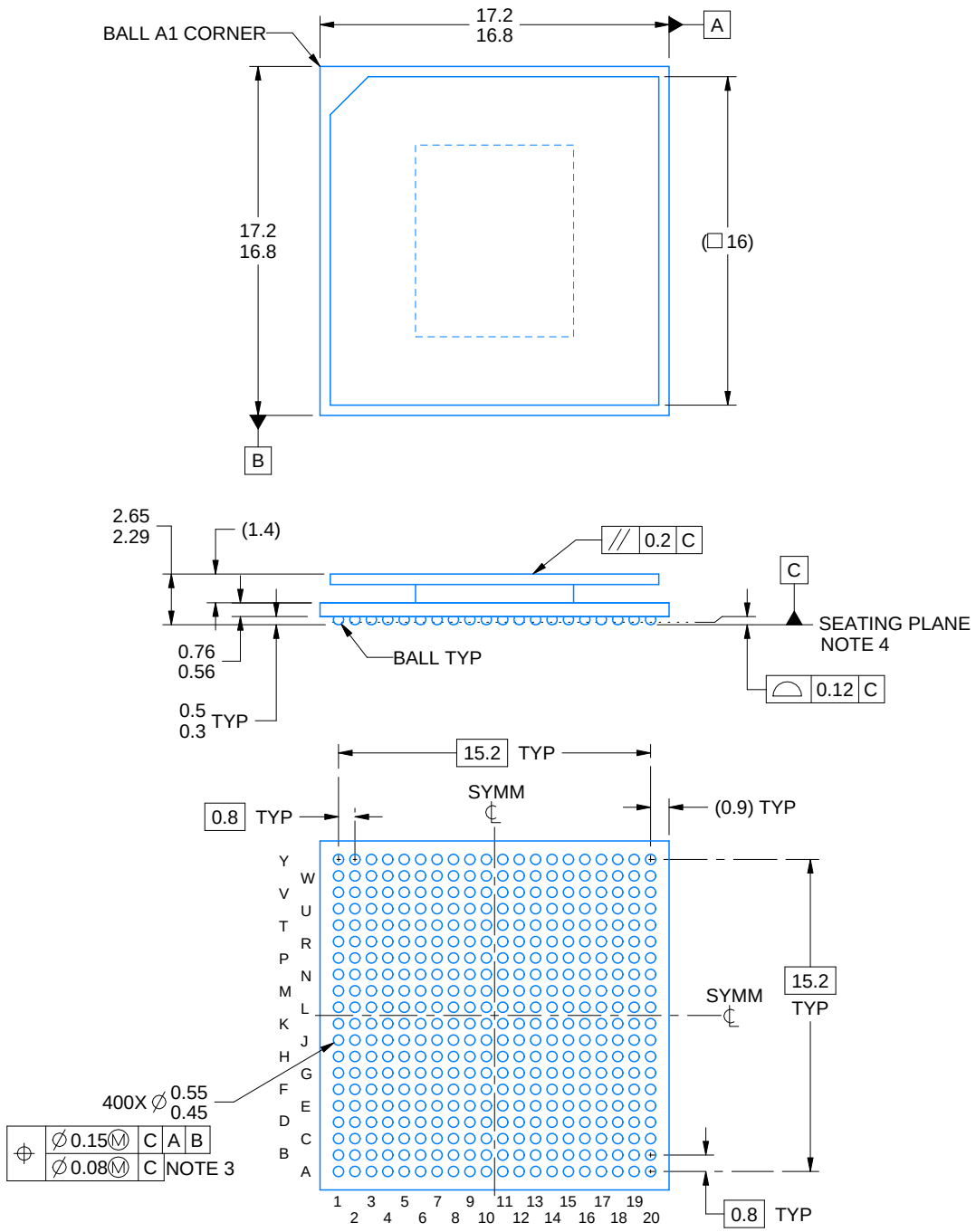
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# ALK0400A

# PACKAGE OUTLINE

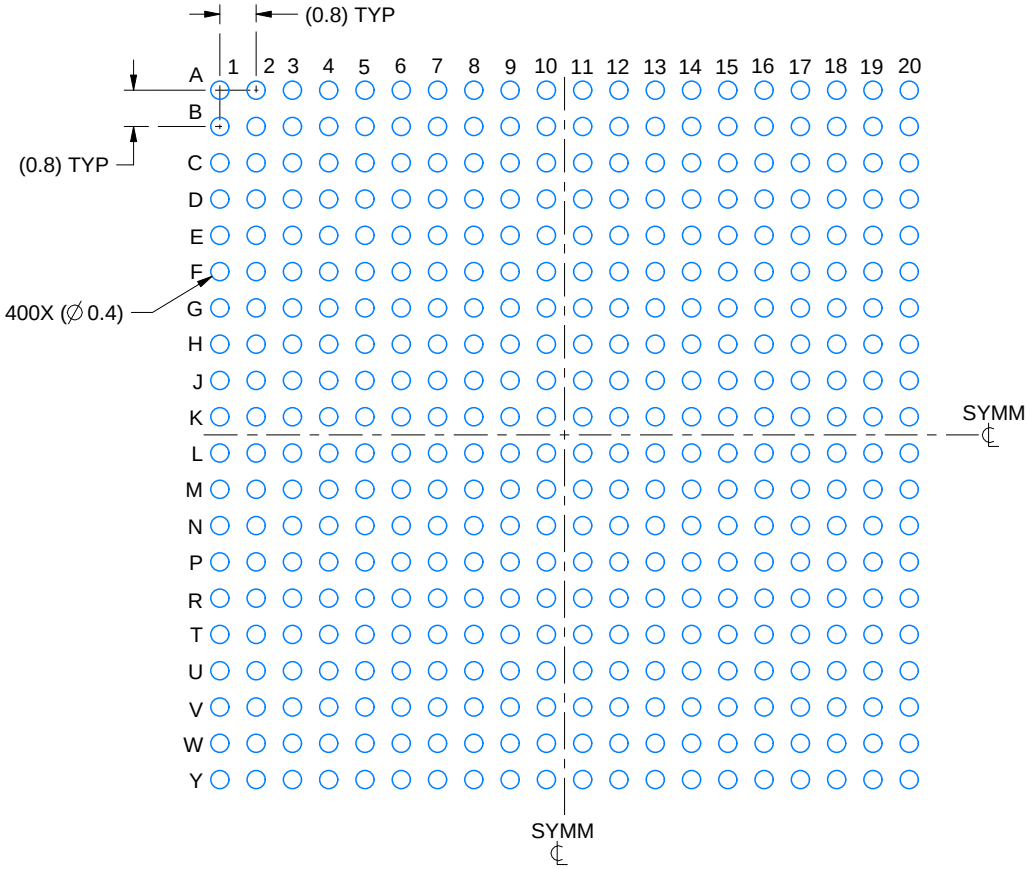
## FCBGA - 2.65 mm max height

BALL GRID ARRAY

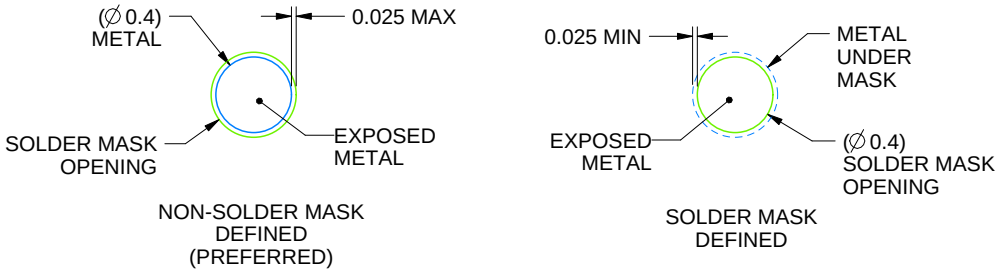



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

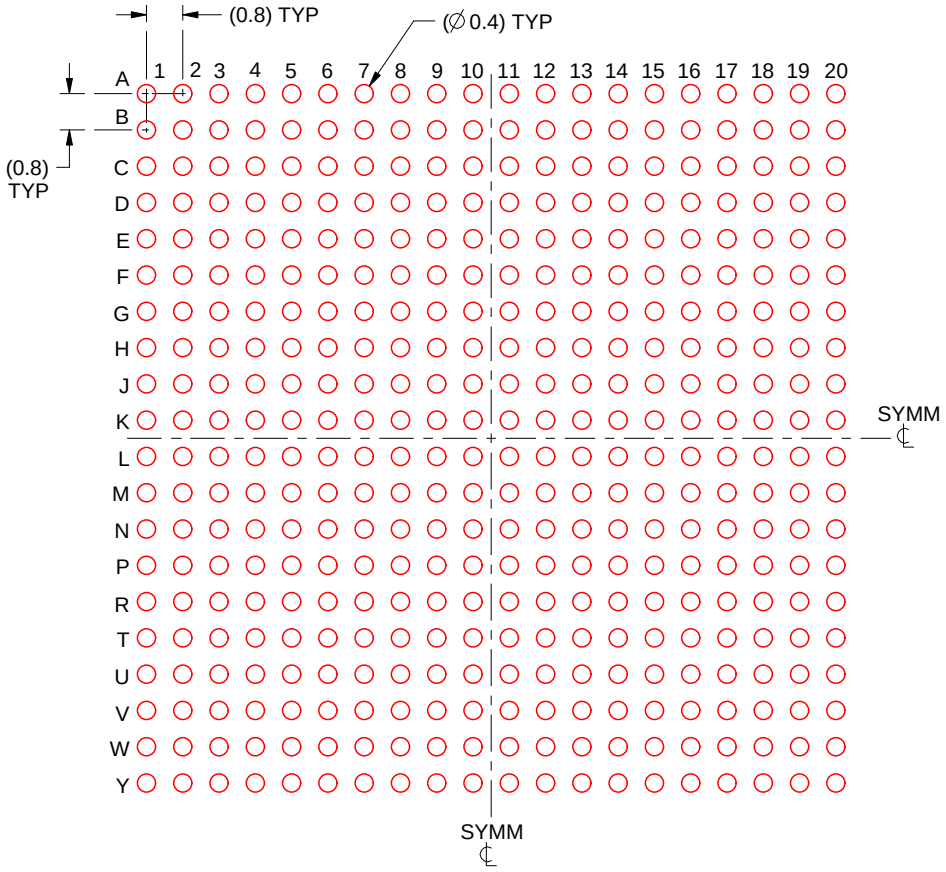



SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).




SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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