参考資料

AFE7951 12GSPS DAC と 3GSPS ADC 搭載、4T4R RF サンプリング AFE

1 特長

- データシート全体のご請求
- クワッド RF サンプリング 12GSPS 送信 DAC
- クワッド RF サンプリング 3GSPS 受信 ADC
- 最大 RF 信号帯域幅:400MHz
- RF 周波数範囲:600MHz～12GHz
- デジタル・ステップ・アッテネータ (DSA):
  - TX:40dB レンジ、0.125dB ステップ
  - RX:25dB レンジ、0.5dB ステップ
- シングルまたはデュアル・バンドの DUC と DDC
- TX または RX ごとに 16 個の NCO
- DAC もしくは ADC クロック用の内部 PLL もしくは VCO、または DAC もしくは ADC サンプル・レートでの外部クロックを選択可能
- SerDes データ・インターフェイス:
  - JESD204B、JESD204C 適合
  - 8 つの SerDes トランシーバ (最高 29.5Gbps)
  - サブクラス 1 のマルチデバイス同期
- パッケージ:17mm × 17mm FCBGA、0.8mm ピッチ

2 アプリケーション

- レーダー
- 追尾フロント・エンド
- 防衛無線
- 戦術通信網
- ワイヤレス通信テスト

3 概要

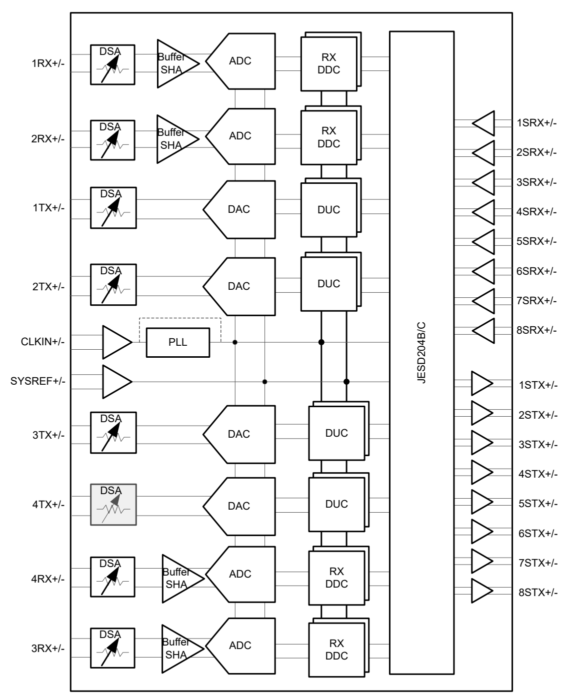
AFE7951 は、高性能で広帯域のマルチチャネル・トランシーバで、4 つの RF サンプリング・トランスミッタ・チェーンと 4 つの RF サンプリング・レシーバ・チェーンを内蔵しています。このデバイスは、最大 12GHz で動作するため、追加の周波数変換段を必要とせず、L、S、C、X バンドの周波数範囲について直接 RF サンプリングが可能です。密度と柔軟性の向上により、多くのチャネル数を持つマルチミッション・システムが可能になります。

TX 信号パスは、TX チャネルあたり最大 400MHz の信号帯域幅を実現する補間およびデジタル・アップ・コンバージョン・オプションをサポートしています。DUC の出力は、2 次ナイキスト動作を拡張する混在モード出力方式で 12GSPS の DAC (D/A コンバータ) を駆動します。DAC 出力は、40dB レンジ、1dB アナログ・ステップ、0.125dB デジタル・ステップの可変ゲイン・アンプ (TX DSA) を内蔵しています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AFE7951	FC-BGA	17mm × 17mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

Table of Contents

4 概要 (続き)

各レシーバ・チェーンは、3GSPS の ADC (A/D コンバータ) に接続された 25dB レンジの DSA (デジタル・ステップ・アッテネータ) を備えています。各レシーバ・チャネルは、外部または内部の自律的な AGC (自動ゲイン制御) を補助するためのアナログ・ピーク電力検出器とさまざまなデジタル電力検出器、およびデバイスの信頼性を確保するための RF 過負荷検出器を備えています。柔軟なデシメーション・オプションにより信号帯域幅を RX チャネルごとには最高 400MHz で最適化できます。

5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
May 2023	*	Initial Release

6 Pin Configuration and Functions

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	VDD1P2 TXCLK	2TXOUT+	2TXOUT-	VDD1P2 TXCLK	VDD1P8TX	1TXOUT-	1TXOUT+	VDD1P8TX	VSSTX	VDD1P2 PLLCLK REF	VDD1P8 PLLVCO	VSSTX	VDD1P8TX	3TXOUT+	3TXOUT-	VDD1P8TX	VDD1P2 TXCLK	4TXOUT-	4TXOUT+	VDD1P2 TXCLK	20
19	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTX	VSSTX	PLL_LDOUT	SYSREF+	SYSREF-	VSSPLL	VSSTX	VSSTX	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	19
18	VSSFBCLK	VSSFBCLK	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSPLL CLKREF	VDD1P2 PLLCLK REF	VDD1P2 PLLCLK REF	VSSPLL CLKREF	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSFBCLK	VSSFBCLK	18
17	VDD1P8 FBCLK	VSSFB	VSSTX	VDD1P2 TXENC	VSSTXENC	VSSTX	VDD1P8 TXDAC	VDD1P8 TXDAC	VSS PLLRXCML	REFCLK+	REFCLK-	VSS PLLRXCML	VDD1P8 TXDAC	VDD1P8 TXDAC	VSSTX	VSSTXENC	VDD1P2 TXENC	VSSTX	VSSFB	VDD1P8 FBCLK	17
16	NC	VSSFB	VDD1P8FB	VDD1P2FB	VSSTXENC	GTR_7_SPIB2SEN	GTR_17_SPIB1CLK	GTR_14_SPIB1SEN	VSSPLL FBCML	VDD1P8PLL	VDD1P8PLL	VSSPLL FBCML	GTL_7_ALARM1	GTL_15_GPIO3	GTL_18_SPIASDO	VSSTXENC	VDD1P2FB	VDD1P8FB	VSSFB	NC	16
15	NC	VSSFB	VDD1P8FB	VDD1P2FB	VDD1P2FB	GTR_15_RESETZ	GTR_13_TRST	GTR_3_TXTDD1	GTR_9_SPIB2SDO	VDD1P2 PLLRXCML	VDD1P2 PLLFBCML	GTL_3_AUX0	GTL_2_ALARM2	GTL_4_SPIACLK	GTL_6_RXTDD2	VDD1P2FB	VDD1P2FB	VDD1P8FB	VSSFB	NC	15
14	VDD1P8 FBCLK	VSSFB	VSSFB	VDD1P2FB	VDD1P2RX	GTR_5_TDO	GTR_18_TDI	GTR_4_TCLK	GTR_2_SPIB2CLK	GTR_8_FBTDD1	GTL_8_AUX1	GTL_9_AUX2	GTL_17_SPIASDIO	GTL_1_SPEEP	GTL_5_SPIASEN	VDD1P2RX	VDD1P2FB	VSSFB	VSSFB	VDD1P8 FBCLK	14
13	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_0_RXGSWAP	GTR_6_SPIB2_SDIO	GND_ESD	DVDD0P9	DVDD0P9	GND_ESD	GTL_0_GPIO2	GTL_11_AUX3	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	13
12	1RXIN+	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_11_SPIB1_SDO	GTR_1_GPIO1	DGND	DVDD0P9	DVDD0P9	DGND	GTL_13_AUX4	GTL_12_BIST1	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	3RXIN+	12
11	1RXIN-	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P2RX	VDD1P2RX	GTR_10_TMS	GTR_12_SPIB1_SDIO	DGND	DVDD0P9	DVDD0P9	DGND	GTL_14_AUX5	GTL_10_BIST0	VDD1P2RX	VDD1P2RX	VDD1P8RX	VDD1P8RX	VSSRX	3RXIN-	11
10	VDD1P2RX	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_6_RXBLNB	GBR_5_FSPIDB	DGND	DVDD0P9	DVDD0P9	DGND	GBL_5_GPIO15	GBL_6_GPIO16	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRX	VDD1P2RX	10
9	VDD1P8 RXCLK	VSSRXCLK	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_9_SYNCB_OUT0-	GBR_7_SYNCB_OUT0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_7_SYNCB_OUT1+	GBL_9_SYNCB_OUT1-	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRXCLK	VDD1P8 RXCLK	9
8	2RXIN-	VSSRX	VSSRXCLK	GND_ESD	GBR_10_FSPICLKA	VDD1P8RX	GBR_13_GPIO8	GBR_8_SYNCB_IN0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_8_SYNCB_IN1+	GBL_13_GPIO19	VDD1P8RX	GBL_10_GPIO17	GND_ESD	VSSRXCLK	VSSRX	4RXIN-	8
7	2RXIN+	VSSRX	VSSRXCLK	GND_ESD	GBR_11_RXTDD1	GBR_14_FSPIDA	GBR_12_GPIO7	GBR_17_SYNCB_IN0-	DGND	DVDD0P9	DVDD0P9	DGND	GBL_17_SYNCB_IN1-	GBL_12_FSPICLKD	GBL_14_FSPIDD	GBL_11_GPIO18	GND_ESD	VSSRXCLK	VSSRX	4RXIN+	7
6	VDD1P8 RXCLK	VSSRXCLK	GBR_0_GPIO4	GBR_19_GPIO12	GBR_16_GPIO10	GBR_1_GPIO5	GBR_15_GPIO9	VDD1P8 GPIO	DGND	DVDD0P9	DVDD0P9	DGND	VDD1P8 GPIO	GBL_15_FSPIDC	GBL_1_FBTDD2	GBL_16_RXCLNB	GBL_19_GPIO20	GBL_0_GPIO13	VSSRXCLK	VDD1P8 RXCLK	6
5	VSSRXCLK	VSSRXCLK	GBR_18_GPIO11	GBR_2_RXALNB	GBR_4_GPIO6	GBR_3_FSPICLKB	IFORCE	VSSGPIO	DGND	DVDD0P9	DVDD0P9	DGND	VSSGPIO	VSENSE	GBL_3_GPIO14	GBL_4_RXDLNB	GBL_2_FSPICLKC	GBL_18_TXTDD2	VSSRXCLK	VSSRXCLK	5
4	VSST	VSST	1STX+	VDDT0P9	2STX+	VDDA1P8	3STX-	VDDA1P8	4STX-	VSST	VSST	5STX-	VDDA1P8	6STX-	VDDA1P8	7STX+	VDDT0P9	8STX+	VSST	VSST	4
3	1SRX+	VSST	1STX-	VDDT0P9	2STX-	VDDA1P8	3STX+	VDDA1P8	4STX+	SERDES_AMUX1	SERDES_AMUX2	5STX+	VDDA1P8	6STX+	VDDA1P8	7STX-	VDDT0P9	8STX-	VSST	8SRX+	3
2	1SRX-	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	DVDD0P9	DVDD0P9	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	8SRX-	2
1	VSST	2SRX+	2SRX-	VSST	3SRX+	3SRX-	VSST	4SRX+	4SRX-	VSST	VSST	5SRX-	5SRX+	VSST	6SRX-	6SRX+	VSST	7SRX-	7SRX+	VSST	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

TX Outputs
RX Inputs
Clock Inputs
Serdes Receivers
Serdes Transmitters
MISC Analog
GPIO
0.9V Supplies
1.2V Supplies
1.8V Supplies
GROUND

図 6-1. FCBGA Package, 400-Pin (Top View)

表 6-1. Pin Functions

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
RF INTERFACES			
RXNC	A15, A16, Y15, Y16	I	Do not connect.
1RXIN–	A11	I	Receiver Channel 1 RF input: negative terminal. Unused RX inputs can be left open.
1RXIN+	A12	I	Receiver Channel 1 RF input: positive terminal. Unused RX inputs can be left open.
2RXIN–	A8	I	Receiver Channel 2 RF input: negative terminal. Unused RX inputs can be left open.

表 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[1]	DESCRIPTION
2RXIN+	A7	I	Receiver Channel 2 RF input: positive terminal. Unused RX inputs can be left open.
3RXIN–	Y11	I	Receiver Channel 3 RF input: negative terminal.
3RXIN+	Y12	I	Receiver Channel 3 RF input: positive terminal. Unused RX inputs can be left open.
4RXIN–	Y8	I	Receiver Channel 4 RF input: negative terminal. Unused RX inputs can be left open.
4RXIN+	Y7	I	Receiver Channel 4 RF input: positive terminal. Unused RX inputs can be left open.
1TXOUT–	F20	O	Transmitter Channel 1 RF output: negative terminal. Connect to 1.8 V when not used.
1TXOUT+	G20	O	Transmitter Channel 1 RF output: positive terminal. Connect to 1.8 V when not used.
2TXOUT–	C20	O	Transmitter Channel 2 RF output: negative terminal. Connect to 1.8 V when not used.
2TXOUT+	B20	O	Transmitter Channel 2 RF output: positive terminal. Connect to 1.8 V when not used.
3TXOUT–	R20	O	Transmitter Channel 3 RF output: negative terminal. Connect to 1.8 V when not used.
3TXOUT+	P20	O	Transmitter Channel 3 RF output: positive terminal. Connect to 1.8 V when not used.
4TXOUT–	V20	O	Transmitter Channel 4 RF output: negative terminal. Connect to 1.8 V when not used.
4TXOUT+	W20	O	Transmitter Channel 4 RF output: positive terminal. Connect to 1.8 V when not used.
DIFFERENTIAL CLOCKS INPUTS			
REFCLK–	L17	I	Reference Clock Inputs: negative terminal
REFCLK+	K17	I	Reference Clock Inputs: positive terminal
SYSREF–	L19	I	SYSREEF inputs: negative terminals
SYSREF+	K19	I	SYSREEF inputs: positive terminals
SerDes CML INTERFACE			
1SRX–	A2	I	CML SerDes Interface Lane 1 input: negative terminal. Unused Serdes inputs can be left open.
1SRX+	A3	I	CML SerDes Interface Lane 1 input: positive terminal. Unused Serdes inputs can be left open.
2SRX–	C1	I	CML SerDes Interface Lane 2 input: negative terminal. Unused Serdes inputs can be left open.
2SRX+	B1	I	CML SerDes Interface Lane 2 input: positive terminal. Unused Serdes inputs can be left open.
3SRX–	F1	I	CML SerDes Interface Lane 3 input: negative terminal
3SRX+	E1	I	CML SerDes Interface Lane 3 input: positive terminal. Unused Serdes inputs can be left open.
4SRX–	J1	I	CML SerDes Interface Lane 4 input: negative terminal
4SRX+	H1	I	CML SerDes Interface Lane 4 input: positive terminal
5SRX–	M1	I	CML SerDes Interface Lane 5 input: negative terminal. Unused Serdes inputs can be left open.
5SRX+	N1	I	CML SerDes Interface Lane 5 input: positive terminal
6SRX–	R1	I	CML SerDes Interface Lane 6 input: negative terminal
6SRX+	T1	I	CML SerDes Interface Lane 6 input: positive terminal. Unused Serdes inputs can be left open.

表 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
7SRX–	V1	I	CML SerDes Interface Lane 7 input: negative terminal
7SRX+	W1	I	CML SerDes Interface Lane 7 input: positive terminal. Unused Serdes inputs can be left open.
8SRX–	Y2	I	CML SerDes Interface Lane 8 input: negative terminal
8SRX+	Y3	I	CML SerDes Interface Lane 8 input: positive terminal. Unused Serdes inputs can be left open.
1STX–	C3	O	CML SerDes Interface Lane 1 output: negative terminal. Unused Serdes outputs can be left open.
1STX+	C4	O	CML SerDes Interface Lane 1 output: positive terminal. Unused Serdes outputs can be left open.
2STX–	E3	O	CML SerDes Interface Lane 2 output: negative terminal. Unused Serdes outputs can be left open.
2STX+	E4	O	CML SerDes Interface Lane 2 output: positive terminal. Unused Serdes outputs can be left open.
3STX–	G4	O	CML SerDes Interface Lane 3 output: negative terminal. Unused Serdes outputs can be left open.
3STX+	G3	O	CML SerDes Interface Lane 3 output: positive terminal. Unused Serdes outputs can be left open.
4STX–	J4	O	CML SerDes Interface Lane 4 output: negative terminal. Unused Serdes outputs can be left open.
4STX+	J3	O	CML SerDes Interface Lane 4 output: positive terminal. Unused Serdes outputs can be left open.
5STX–	M4	O	CML SerDes Interface Lane 5 output: negative terminal. Unused Serdes outputs can be left open.
5STX+	M3	O	CML SerDes Interface Lane 5 output: positive terminal. Unused Serdes outputs can be left open.
6STX–	P4	O	CML SerDes Interface Lane 6 output: negative terminal. Unused Serdes outputs can be left open.
6STX+	P3	O	CML SerDes Interface Lane 6 output: positive terminal. Unused Serdes outputs can be left open.
7STX–	T3	O	CML SerDes Interface Lane 7 output: negative terminal. Unused Serdes outputs can be left open.
7STX+	T4	O	CML SerDes Interface Lane 7 output: positive terminal. Unused Serdes outputs can be left open.
8STX–	V3	O	CML SerDes Interface Lane 8 output: negative terminal. Unused Serdes outputs can be left open.
8STX+	V4	O	CML SerDes Interface Lane 8 output: positive terminal. Unused Serdes outputs can be left open.
GPIO FUNCTIONS			
GBL_0_GPIO13	V6	I/O	GPIO.
GBL_1_FBTDD2	R6	I/O	Default location of FB TDD2 input signal.
GBL_2_FSPICLKC	U5	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_3_GPIO14	R5	I/O	GPIO.
GBL_4_RXDLNB	T5	I/O	Default location of RX channel D AGC LNA Bypass output signal.
GBL_5_GPIO15	N10	I/O	GPIO.
GBL_6_GPIO16	P10	I/O	GPIO.

表 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
GBL_7_SYNCB_OUT1+	N9	I/O	Default location of JESD Sync\ 1 output differential positive terminal.
GBL_8_SYNCB_IN1+	N8	I/O	Default location of JESD Sync\ 1 input differential positive terminal.
GBL_9_SYNCB_OUT1–	P9	I/O	Default location of JESD Sync\ 1 output differential negative terminal.
GBL_10_GPIO17	T8	I/O	GPIO.
GBL_11_GPIO18	T7	I/O	GPIO.
GBL_12_FSPICLKD	P7	I/O	Default and recommended location of FSPI D clock (FSPI for factory use only, available as generic GPIO).
GBL_13_GPIO19	P8	I/O	GPIO.
GBL_14_FSPIDD	R7	I/O	Default and recommended location of FSPI D data (FSPI for factory use only, available as generic GPIO).
GBL_15_FSPIDC	P6	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_16_RXCLNB	T6	I/O	Default location of RX channel C AGC LNA Bypass output signal.
GBL_17_SYNCB_IN1–	N7	I/O	Default location of JESD Sync\ 1 input differential negative terminal.
GBL_18_TXTDD2	V5	I/O	Default location of TX TDD2 input signal.
GBL_19_GPIO20	U6	I/O	GPIO.
GBR_0_GPIO4	C6	I/O	GPIO.
GBR_1_GPIO5	F6	I/O	GPIO.
GBR_2_RXALNB	D5	I/O	Default location of RX channel A AGC LNA Bypass output signal.
GBR_3_FSPICLKB	F5	I/O	Default and recommended location of FSPI B clock (FSPI for factory use only, available as generic GPIO).
GBR_4_GPIO6	E5	I/O	GPIO.
GBR_5_FSPIDB	H10	I/O	Default and recommended location of FSPI B data (FSPI for factory use only, available as generic GPIO).
GBR_6_RXBLNB	G10	I/O	Default location of RX channel B AGC LNA Bypass output signal.
GBR_7_SYNCB_OUT0+	H9	I/O	Default location of JESD Sync\ 0 output differential positive terminal.
GBR_8_SYNCB_IN0+	H8	I/O	Default location of JESD Sync\ 0 input differential positive terminal.
GBR_9_SYNCB_OUT0–	G9	I/O	Default location of JESD Sync\ 0 output differential negative terminal.
GBR_10_FSPICLKA	E8	I/O	Default location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_11_RXTDD1	E7	I/O	Default location of RX TDD1 input signal.
GBR_12_GPIO7	G7	I/O	GPIO.
GBR_13_GPIO8	G8	I/O	GPIO.
GBR_14_FSPIDA	F7	I/O	Default and recommended location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_15_GPIO9	G6	I/O	GPIO.
GBR_16_GPIO10	E6	I/O	GPIO.
GBR_17_SYNCB_IN0–	H7	I/O	Default location of JESD Sync\ 0 input differential negative terminal.
GBR_18_GPIO11	C5	I/O	GPIO.

表 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
GBR_19_GPIO12	D6	I/O	GPIO.
GTL_0_GPIO2	N13	I/O	GPIO.
GTL_1_SLEEP	P14	I/O	Default location of Sleep input signal.
GTL_2_ALARM2	N15	I/O	Default location of Alarm 2 output signal.
GTL_3_AUX0	M15	I/O	GPIO or auxiliary low-speed ADC input 0
GTL_4_SPIACLK	P15	I/O	Fixed Location of SPI A Clock.
GTL_5_SPIASEN	R14	I/O	Fixed Location of SPI A Send Enable.
GTL_6_RXTDD2	R15	I/O	Default location of RX TDD2 input signal.
GTL_7_ALARM1	N16	I/O	Default location of Alarm 1 output signal.
GTL_8_AUX1	L14	I/O	GPIO or auxiliary low-speed ADC input 1.
GTL_9_AUX2	M14	I/O	GPIO or auxiliary low-speed ADC input 2.
GTL_10_BIST0	P11	I/O	Fixed Location for BIST0 Function. Set low when using JTAG, set high for normal operation.
GTL_11_AUX3	P13	I/O	GPIO or auxiliary low-speed ADC input 3.
GTL_12_BIST1	P12	I/O	Fixed Location for BIST1 Function. Set high when using JTAG, set low for normal operation.
GTL_13_AUX4	N12	I/O	GPIO or auxiliary low-speed ADC input 4.
GTL_14_AUX5	N11	I/O	GPIO or auxiliary low-speed ADC input 5.
GTL_15_GPIO3	P16	I/O	GPIO.
GTL_17_SPIASDIO	N14	I/O	Fixed Location of SPI A Serial Data Input (3- and 4-wire mode) or Output (3 wire mode only).
GTL_18_SPIASDO	R16	I/O	Fixed Location of SPI A Serial Data Output in 4-wire mode.
GTR_0_RXGSWAP	G13	I/O	Default location of RX gain swap input.
GTR_1_GPIO1	H12	I/O	GPIO.
GTR_2_SPIB2CLK	J14	I/O	Default and recommended location of SPI B2 clock.
GTR_3_TXTDD1	H15	I/O	Default location of TX TDD1 input signal.
GTR_4_TCLK	H14	I/O	Fixed location for JTAG Test Clock.
GTR_5_TDO	F14	I/O	Fixed location for JTAG Test Data Out.
GTR_6_SPIB2_SDIO	H13	I/O	Default and recommended location of SPI B2 serial data input/output.
GTR_7_SPIB2SEN	F16	I/O	Default and recommended location of SPI B2 enable input.
GTR_8_FBTDD1	K14	I/O	Default location of FB TDD1 input signal.
GTR_9_SPIB2SDO	J15	I/O	Default and recommended location of SPI B2 serial data output (4-wire mode)
GTR_10_TMS	G11	I/O	Fixed location for JTAG Test Mode Select.
GTR_11_SPIB1_SDO	G12	I/O	Default and recommended location of SPI B1 serial data output (4-wire mode).
GTR_12_SPIB_SDIO	H11	I/O	Default and recommended location of SPI B1 serial data input/output.
GTR_13_TRST	G15	I/O	Fixed location for JTAG Test Reset. Must be pulled low when the JTAG port is not used.
GTR_14_SPIB1SEN	H16	I/O	Default and recommended location of SPI B1 enable input.
GTR_15_RESETZ	F15	I/O	Fixed Location for reset function. Chip Reset to default register settings.
GTR_17_SPIB1CLK	G16	I/O	Default and recommended location of SPI B1 clock.
GTR_18_TDI	G14	I/O	Fixed location for JTAG Test Data Input.
POWER SUPPLIES			

表 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE(1)	DESCRIPTION
DVDD	K2, K5, K6, K7, K8, K9, K10, K11, K12, K13, L2, L5, L6, L7, L8, L9, L10, L11, L12, L13	—	0.9-V digital power supply
VDD1P2FB	D14, D15, D16, E15, U14, U15, U16, T15	—	1.2-V supply for FB ADCs.
VDD1P8FB	C15, C16, V15, V16	—	1.8-V supply for FB ADC.
VDD1P8FBCLK	A14, A17, Y17, Y14	—	1.8-V supply for FB ADC clock.
VDD1P2PLLCLKREF	K20, K18, L18	—	1.2-V supply for PLL.
VDDPLL1P2FBCML	L15	—	1.2-V supply for PLL clock distribution to FB ADC.
VDDPLL1P2RXCML	K15	—	1.2-V supply for clock distribution to RX ADC.
VDD1P8PLL	K16, L16	—	1.8-V supply for PLL.
VDD1P8PLLVCO	L20	—	1.8-V supply for PLL/VCO. This is a sensitive net and requires extra care in layout.
VDD1P2RX	A10, A13, E11, E12, E13, E14,F11, F12, F13, R11, R12, R13, T11, T12, T13, T14, Y10, Y13	—	1.2-V supply for RX ADCs.
VDD1P8RX	C9, C10, C11, D9, D10, D11, E9, E10, F8, F9, F10, R8, R9, R10, T9, T10, U9, U10, U11, V9, V10, V11	—	1.8-V supply for RX ADCs.
VDD1P8RXCLK	A6, A9, Y6, Y9	—	1.8-V supply for RX ADC clocks.
VDD1P2TXENC	D17, U17	—	1.2-V supply for DAC encoder.
VDD1P2TXCLK	A20, D20, U20, Y20	—	1.2-V supply for DAC clock.
VDD1P8TX	E20, H20, N20, T20	—	1.8-V supply for DAC.
VDD1P8TXDAC	G17, H17, N17, P17	—	1.8-V supply for DAC.
VDD1P8GPIO	H6, N6	—	1.8-V supply for GPIO.
VDDA1P8	F3, F4, H3, H4, R3, R4, N3, N4	—	SerDes analog 1.8-V power supply.
VDDT0P9	D3, D4, U3, U4	—	SerDes digital 0.9-V power supply.
GROUNDS			
DGND	J5, J6, J7, J8, J9, J10, J11, J12, M5, M6, M7, M8, M9, M10, M11, M12	—	Digital core ground
VSSGPIO	H5, N5	—	GPIO ground.
VSSFB	B14, B15, B16, B17, C14, V14, W14, W15, W16, W17	—	Ground for FB ADC supply.
VSSFBCLK	A18, B18, W18, Y18	—	Ground for FB ADC 1.8-V clock supply.
GND_ESD	D7, D8, J13, M13, U7, U8	—	Ground for ESD protection circuits.
VSSRX	B7, B8, B10, B11, B12, C12, D12, B13, C13, D13, W7, W8, W10, W11, W13, U12, V12, W12, U13, V13	—	Ground for RX ADC.
VSSRXCLK	A5, B5, B6, B9, C7, C8, W5, W6, W9, Y5, V7, V8	—	Ground for RX ADC clocks.
VSSTX	B19, C17, C18, C19, D18, E18, E19, F17, F18, F19, G18, G19, H18, H19, J20, M20, N18, N19, P18, P19, R17, R18, R19, T18, T19, U18, V17, V18, V19, W19	—	Ground for TX DAC.
VSSTXENC	E16, E17, T16, T17	—	Ground for TX DAC encoder.

表 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
VSSTXCLK	A19, D19, U19, Y19	—	Ground for TX DAC clock.
VSSPLL	M19	—	Ground for PLL.
VSSPLLFBCML	J16, M16	—	Ground for FB ADC clock.
VSSPLLCLKREF	J18, M18	—	Ground for CLKREF PLL.
VSSPLLRXCML	J17, M17	—	Ground for RX ADC clock.
VSST	A1, A4, B2, B3, B4, C2, D1, D2, E2, F2, G1, G2, H2, J2, K1, K4, L1, L4, M2, N2, P1, P2, R2, T2, U1, U2, V2, W2, W3, W4, Y1, Y4	—	SerDes ground.
OTHERS			
IFORCE	G5	—	Reserved for TI use only. Do not connect.
PLL_LDOUT	J19	—	External decoupling ball for PLL LDO. Connect with 100-nF capacitor to GND.
SerDes_AMUX1	K3	—	Analog test pin for SerDes lane 1-4, can be left floating
SerDes_AMUX2	L3	—	Analog test pin for SerDes lane 5-8, can be left floating
VSENSE	P5	—	Process test: sense voltage (TI use only). Do not connect.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	–0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	–0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	–0.5	2.1	V
Pin Volatge Range	{1/2/3/4}RXIN+/-	–0.5	VDDRX1P8+0.3	V
	{1/2/3/4}TXOUT+/-	–0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	–0.3	1.4	V
	{1:8}SRX+/-	–0.3	1.4	V
	{1:8}STX+/-	–0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, $\overline{\text{RESET}}$, BISTB0, BISTB1	–0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	–0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	–0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/ PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/ TXENC/PLL/PLLVCO/FB/FBCLK/ GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating Junction Temperature			110[(1)]	°C
	Maximum Operating Junction Temperature	125			°C

(1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to SBAA403 application note for additional details

7.4 Thermal Information AFE79xx

THERMAL METRIC[(1)]		17mmx17mm FC-BGA	UNIT
		400 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.85	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Transmitter Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC_{RES}	DAC resolution			14		bits
f_{RFout}	RF output frequency range	f_{DAC} = 12 GSPS, 1st Nyquist	600		6000	MHz
		f_{DAC} = 12 GSPS, 2nd Nyquist	6000		12000	
		f_{DAC} = 9 GSPS, 1st Nyquist	600		4500	
		f_{DAC} = 9 GSPS, 2nd Nyquist	4500		9000	
		f_{DAC} = 6 GSPS, 1st Nyquist	600		3000	
		f_{DAC} =6 GSPS, 2nd Nyquist	3000		6000	
P_{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.2		dBm
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.6		dBm
		f_{out} = 2600 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f_{out} = 3500 MHz, -0.5dBFS		3.9		dBm
		fout = 4900 MHz, -0.5dBFS		3.1		dBm
		f_{out} = 3500 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
		f_{out} = 4900 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
		f_{out} = 4900 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
		f_{out} = 8100 MHz, -0.1dBFS, mixed mode		-2.8		dBm
		f_{out} = 9600 MHz, -0.1dBFS, mixed mode		-4.3		dBm
R_{TERM}	Output termination resistor	Default setting		50		Ω
ATT_{range}	DSA Attenuation range			40		dB
ATT_{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		±0.1		dB
$ATT_{phase-err}$	DSA Gain Steps Phase accuracy, any 8dB range	f_{out} = 850MHz(2)		±1		deg
		f_{out} = 1800MHz(2)		±1		deg
		f_{out} =2600MHz(2)		±1		deg
		f_{out} = 3500MHz(2)		±1		
		f_{out} = 4900MHz(2)		±1		deg
		f_{out} = 8100MHz(2)		±2		deg
		f_{out} = 9600MHz(2)		±2		deg
G_{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F_{out} < 4.9G		1.2		

7.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at f_{IF}±10 MHz	f_{out} = 850MHz, -7dBFS each tone		-66		dBc
		f_{out} = 1800MHz, -7dBFS each tone		-63		dBc
		f_{out} = 2600MHz, -7dBFS each tone		-62		dBc
		f_{out} = 3500MHz, -7dBFS each tone		-61		dBc
		f_{out} = 4900MHz, -7dBFS each tone		-57		dBc
		f_{out} = 8100MHz, -7dBFS each tone		-55		dBc
		f_{out} = 9600MHz, -7dBFS each tone		-52		dBc
		f_{out} = 850MHz, -13dBFS each tone		-74.4		dBc
		f_{out} = 1800MHz, -13dBFS each tone		-71.1		dBc
		f_{out} = 2600MHz, -13dBFS each tone		-73		dBc
		f_{out} = 3500MHz, -13dBFS each tone		-72		dBc
		f_{out} = 4900MHz, -13dBFS each tone		-67.8		dBc
		f_{out} = 8100MHz, -13dBFS each tone		-64		dBc
		f_{out} = 9600MHz, -13dBFS each tone		-68		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	f_{out} = 850 MHz		50.8		dBc
		f_{out} = 1800 MHz		51.9		dBc
		f_{out} = 2600 MHz		42		dBc
		f_{out} = 3500 MHz		44		dBc
		f_{out}= 4900 MHz		46.1		dBc
$f_S/2$ - f_{OUT}	Interleaving Image	f_{DAC} = 5898.24MSPS, interleave mode		-51.9		dBc
		f_{DAC} = 8847.36 MSPS, interleave mode		-46.0		dBc
		f_{DAC} = 11796.48MSPS, interleave mode		-41		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	f_{out} = 850 MHz		-49		dBc
		f_{out} = 1800 MHz		-53		dBc
		f_{out} = 2600 MHz		-50		dBc
		f_{out} = 3500 MHz		-48		dBc
		f_{out}= 4900 MHz		-47		dBc
		f_{out}= 8100 MHz		-50		dBc
		f_{out}= 9600 MHz		-53		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-60		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-64		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-45		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-57		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-58		dBc
		f_{out}= 8100 MHz, A_{OUT}=-12dBFS		-60		dBc
		f_{out}= 9600 MHz, A_{OUT}=-12dBFS		-62		dBc

7.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	f_{out} = 850 MHz		-62		dBc
		f_{out} = 1800 MHz		-55		dBc
		f_{out} = 2600 MHz		-57		dBc
		f_{out} = 3500 MHz		-60		dBc
		f_{out}= 4900 MHz		-54		dBc
		f_{out}= 8100 MHz		-54		dBc
		f_{out}= 9600 MHz		-56		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-80		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-77		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-77		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-78		dBc
		f_{out}= 8100 MHz, A_{OUT}=-12dBFS		-82		dBc
		f_{out}= 9600 MHz, A_{OUT}=-12dBFS		-80		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	f_{out} = 850 MHz		-81		dBc
		f_{out} = 1800 MHz		-88		dBc
		f_{out} = 2600 MHz		-86		dBc
		f_{out} = 3500 MHz		-79		dBc
		f_{out}= 4900 MHz		-86		dBc
		f_{out}= 8100 MHz		-87		dBc
		f_{out}= 9600 MHz		-85		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-93		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-98		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out}= 8100 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out}= 9600 MHz, A_{OUT}=-12dBFS		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	f_{out} = 850 MHz		68.5		dBc
		f_{out} = 1800 MHz		79.4		dBc
		f_{out} = 2600 MHz		77		dBc
		f_{out} = 3500 MHz		75		dBc
		f_{out}= 4900 MHz		76		dBc
		f_{out}= 8100 MHz		61		dBc
		f_{out}= 9600 MHz		64		dBc
$f_S/4$	Fixed Spur	f_{DAC} = 5898.24MSPS		-64		dBFS
		f_{DAC} = 8847.36MSPS		-75		dBFS
		f_{DAC} = 11796.48MSPS		-67		dBFS
$f_S/2$	Fixed Spur	f_{DAC} = 5898.24MSPS		-49		dBFS
		f_{DAC} = 8847.36MSPS		-48		dBFS
		f_{DAC} = 11796.48 MSPS		-48		dBFS

7.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3*f_S/4	Fixed Spur	2nd Nyquist, f_{DAC} = 5898.24MSPS		-76		dBFS
		2nd Nyquist, f_{DAC} = 8847.36MSPS		-89		dBFS
		2nd Nyquist, f_{DAC} = 11796.48MSPS		-63		dBFS
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 0.85 GHz	Atten=0dB, Pout=-13dBFs		-68.5		dBc
		Atten=20dB,Pout=-13dBFs		-67.2		dBc
		Atten=28dB,Pout=-13dBFs		-64.5		dBc
		Atten=39dB, Pout=-13dBFs		-53.9		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 1.8425 GHz	Atten=0dB,Pout=-13dBFs		-70.7		dBc
		Atten=20dB, Pout=-13dBFs		-68.3		dBc
		Atten=28dB, Pout=-13dBFs		-62.9		dBc
		Atten=39dB, Pout=-13dBFs		-52.0		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, Pout=-13dBFs		-71		dBc
		Atten=20dB, Pout=-13dBFs		-68		dBc
		Atten=28dB, Pout=-13dBFs		-62		dBc
		Atten=39dB, Pout=-13dBFs		-51.3		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, Pout=-13dBFs		-70		dBc
		Atten=20dB, Pout=-13dBFs		-67		dBc
		Atten=28dB, Pout=-13dBFs		-60		dBc
		Atten=39dB, Pout=-13dBFs		-49.8		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, Pout=-13dBFs		-68.8		dBc
		Atten=20dB, Pout=-13dBFs		-65.9		dBc
		Atten=28dB, Pout=-13dBFs		-60.6		dBc
		Atten=39dB, Pout=-13dBFs		-49.5		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, Pout=-13dBFs		-65		dBc
		Atten=20dB, Pout=-13dBFs		-62		dBc
		Atten=20dB, Pout=-13dBFs		-55		dBc
		Atten=39dB,Pout=-13dBFs		-44.3		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, Pout=-13dBFs		-64		dBc
		Atten=20dB, Pout=-13dBFs		-59		dBc
		Atten=28dB, Pout=-13dBFs		-52		dBc
		Atten=39dB, Pout=-13dBFs		-41.1		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, Pout=-13dBFs		-64.1		dBc
		Atten=20dB, Pout=-13dBFs		-60.4		dBc
		Atten=28dB, Pout=-13dBFs		-53.5		dBc
		Atten=39dB, Pout=-13dBFs		-42.5		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 8.1 GHz	Atten=0dB, Pout=-13dBFs		-58		dBc
		Atten=20dB, Pout=-13dBFs		-53		dBc
		Atten=28dB, Pout=-13dBFs		-46		dBc
		Atten=39dB, Pout=-13dBFs		-36		dBc

7.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 9.6 GHz	Atten=0dB, Pout=-13dBFs		-57		dBc
		Atten=20dB, Pout=-13dBFs		-50		dBc
		Atten=28dB, Pout=-13dBFs		-42		dBc
		Atten=39dB, Pout=-13dBFs		-31		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	F_{out} =0.85 GHz, P_{OUT}=-13dBFs		0.2		%
		F_{out} =1.8425 GHz, P_{OUT}=-13dBFs		0.3		%
		F_{out} =2.6 GHz, P_{OUT}=-13dBFs		0.28		%
		F_{out} =3.5 GHz, P_{OUT}=-13dBFs		0.38		%
		F_{out} =4.9 GHz, P_{OUT}=-13dBFs		0.4		%
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 0.85 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-157.6		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-153.3		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-147.9		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-136.9		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 1.8 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-158.4		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-152.2		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-145.6		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-134.6		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 2.6 GHz	Atten=0dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-157		dBFS/Hz
		Atten=20dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-151		dBFS/Hz
		Atten=28dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-144		dBFS/Hz
		Atten=39dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-133.0		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =3.5 GHz	Atten=0dB, Pout=-13dBFs		-158		dBFS/Hz
		Atten=20dB, Pout=-13dBFs		-150		dBFS/Hz
		Atten=28dB, Pout=-13dBFs		-143		dBFS/Hz
		Atten=39dB, Pout=-13dBFs		-131.8		dBFS/Hz

7.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =4.9 GHz	Atten=0dB, Pout=-13dBFs		-155.5		dBFS/Hz
		Atten=20dB, Pout=-13dBFs		-147.8		dBFS/Hz
		Atten=28dB, Pout=-13dBFs		-140.8		dBFS/Hz
		Atten=39dB, Pout=-13dBFs		-129.6		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 50MHz offset F_{out} =8.1 GHz	Atten=0dB, Pout=-13dBFs		-153		dBFS/Hz
		Atten=20dB, Pout=-13dBFs		-147		dBFS/Hz
		Atten=28dB, Pout=-13dBFs		-140		dBFS/Hz
		Atten=39dB, Pout=-13dBFs		-129		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 50MHz offset F_{out} =9.6 GHz	Atten=0dB, Pout=-13dBFs		-152		dBFS/Hz
		Atten=20dB, Pout=-13dBFs		-147		dBFS/Hz
		Atten=28dB, Pout=-13dBFs		-140		dBFS/Hz
		Atten=39dB, Pout=-13dBFs		-129		dBFS/Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-10		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT(1)	f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-49		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-59		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-65		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-66		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-60		dB
		f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-90		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-91		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-93		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-94		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-83		dB

7.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN_{TXADD}	Additive Phase Noise External Clock Mode(3)	f_{out} = 9.6GHz, f_{OFFSET} = 100Hz		-88		dBc/Hz
		f_{out} = 9.6GHz, f_{OFFSET} = 1kHz		-102		dBc/Hz
		f_{out} = 9.6GHz, f_{OFFSET} = 10kHz		-110		dBc/Hz
		f_{out} = 9.6GHz, f_{OFFSET} = 100kHz		-123		dBc/Hz
		f_{out} = 9.6GHz, f_{OFFSET} = 1MHz		-136		dBc/Hz
		f_{out} = 9.6GHz, f_{OFFSET} = 10MHz		-143		dBc/Hz
		f_{out} = 9.6GHz, f_{OFFSET} = 100MHz		-146		dBc/Hz

(1) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
(2) After DSA calibration procedure
(3) Single side band, input clock phase noise subtracted.

7.6 RF ADC Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC_{RES}	ADC resolution			14		bits
F_{RFin}	RF input frequency range		600		12000	MHz
$P_{FS\_CW,min}$	Min Full scale input power, at device pins (1)	f_{IN} = 830 MHz, DSA=0dB		-2.9		dBm
		f_{IN} = 1760 MHz, DSA=0dB		-2.8		dBm
		f_{IN} = 2610 MHz, DSA=0dB		-1.8		dBm
		f_{IN} = 3610 MHz, DSA=0dB		-0.4		dBm
		f_{IN} = 4910 MHz, DSA=0dB		0.1		dBm
		f_{IN} = 8150 MHz, DSA=0dB		2.1		dBm
		f_{IN} = 9610 MHz, DSA=0dB		4.3		dBm
$P_{FS\_CW,MAX}$	MAX Full scale input power - reliability limited, at device pins	f_{IN} = 830 MHz, DSA = 20dB		16.7		dBm
		f_{IN} = 1760 MHz, DSA = 20dB		17.0		dBm
		f_{IN} = 2610 MHz, DSA = 20dB		18		dBm
		f_{IN} = 3610 MHz, DSA = 20dB		18.5		dBm
		f_{IN} = 4910 MHz, DSA = 20dB		19.3		dBm
		f_{IN} = 8150 MHz, DSA = 20dB		21.3		dBm
		f_{IN} = 9610 MHz, DSA = 20dB		23.5		dBm
S11	Input Return Loss	with matching network		-12.0		dB
ATT_{range}	DSA Attenuation range			25.0		dB
ATT_{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F_{in}=3610MHz, after calibration		±0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=3610MHz, after calibration		±0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=4910MHz, after calibration		±1.8		deg
NSD	Noise Density (small signal)	f_{IN} = 830 MHz, DSA = 3dB(3)		-155.2		dBFS/Hz
		f_{IN} = 1760 MHz, DSA = 3dB(3)		-155.0		dBFS/Hz
		f_{IN} = 2610 MHz, DSA = 3dB(3)		-154.4		dBFS/Hz
		f_{IN} = 3610 MHz, DSA = 3dB(3)		-154.1		dBFS/Hz
		f_{IN} = 4910 MHz, DSA = 3dB(3)		-155.1		dBFS/Hz
		f_{IN} = 8150 MHz, DSA = 3dB(3)		-150		dBFS/Hz
		f_{IN} = 9610 MHz, DSA = 3dB(3)		-151		dBFS/Hz
		f_{IN} = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f_{IN} = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f_{IN} = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f_{IN} = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f_{IN} = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f_{IN} = 8150 MHz, 3<=Atten<=25		-152.5		dBFS/Hz
		f_{IN} = 9610 MHz, 3<=Atten<=25		-152.5		dBFS/Hz

7.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF_{min}	Noise Figure min DSA Atten=0 - 3dB	f_{IN} = 830 MHz		19.1		dB
		f_{IN} = 1760 MHz		19.0		dB
		f_{IN} = 2610 MHz		20.9		dB
		f_{IN} = 3610 MHz		22.8		dB
		f_{IN} = 4910 MHz		22.4		dB
		f_{IN} = 8150 MHz		27.3		dB
		f_{IN} = 9610 MHz		30		dB
NF	Noise Figure DSA Atten=4dB	f_{IN} = 830 MHz(4)		20.0		dB
		f_{IN} = 1760 MHz(4)		20.6		dB
		f_{IN} = 2610 MHz(4)		21.9		dB
		f_{IN} = 3610 MHz(4)		23.5		dB
		f_{IN} = 4910 MHz(4)		22.3		dB
		f_{IN} = 8150 MHz(4)		27.9		dB
		f_{IN} = 9610 MHz(4)		30.7		dB
NF_{max}	Noise Figure DSA Atten=20dB	f_{IN} = 830 MHz		34.7		dB
		f_{IN} = 1760 MHz		35.2		dB
		f_{IN} = 2610 MHz		36.0		dB
		f_{IN} = 3610 MHz		37.3		dB
		f_{IN} = 4910 MHz		37.6		dB
		f_{IN} = 8150 MHz		42.8		dB
		f_{IN} = 9610 MHz		45		dB
IMD3	3^{rd} order intermodulation 2 tones at at f_{IN} ± 10MHz -7dBFS each tone	f_{IN} = 840 MHz, 3<=Atten<=12		-82.4		dBc
		f_{IN} = 1770 MHz, 3<=Atten<=12		-84.1		dBc
		f_{IN} = 2610 MHz, 3<=Atten<=12		-74		dBc
		f_{IN} = 3610 MHz, 3<=Atten<=12		-77		dBc
		f_{IN} = 4920 MHz, 3<=Atten<=12		-75.9		dBc
		f_{IN} = 8150 MHz, 3<=Atten<=12, 25MHz tone spacing		-55		dBc
		f_{IN} = 9610 MHz, 3<=Atten<=12, 25MHz tone spacing		-60		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, A_{IN} = -3 dBFS	f_{IN} = 830 MHz		88.2		dBFS
		f_{IN} = 1760 MHz		80.6		dBFS
		f_{IN} = 2610 MHz		88		dBFS
		f_{IN} = 3610 MHz		84		dBFS
		f_{IN} = 4910 MHz		78.9		dBFS
		f_{IN} = 8150 MHz		78		dBFS
		f_{IN} = 9610 MHz		71		dBFS

7.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion A_{IN} = -3 dBFS[(2)] [(5)]	f_{IN} = 830 MHz		-85.5		dBFS
		f_{IN} = 1760 MHz		-90.5		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-87		dBFS
		f_{IN} = 4910 MHz		-84.2		dBFS
		f_{IN} = 8150 MHz		-70		dBFS
		f_{IN} = 9610 MHz		-70		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -3 dBFS[(5)]	f_{IN} = 830 MHz		-80.2		dBFS
		f_{IN} = 1760 MHz		-85.3		dBFS
		f_{IN} = 2610 MHz		-86		dBFS
		f_{IN} = 3610 MHz		-78		dBFS
		f_{IN} = 4910 MHz		-75.4		dBFS
		f_{IN} = 8150 MHz		-70		dBFS
		f_{IN} = 9610 MHz		-70		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -3 dBFS[(5)]	f_{IN} = 830 MHz		-88.2		dBFS
		f_{IN} = 1760 MHz		-80.6		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-84		dBFS
		f_{IN} = 4910 MHz		-81.7		dBFS
		f_{IN} = 8150 MHz		-78		dBFS
		f_{IN} = 9610 MHz		-71		dBFS
SFDR	Spurious Free Dynamic Range A_{IN} = -13 dBFS 0<=Atten<=16	f_{IN} = 830 MHz		89.2		dBFS
		f_{IN} = 1760 MHz		88.8		dBFS
		f_{IN} = 2610 MHz		95		dBFS
		f_{IN} = 3610 MHz		90		dBFS
		f_{IN} = 4910 MHz		89.8		dBFS
		f_{IN} = 8150 MHz		83		dBFS
		f_{IN} = 9610 MHz		80		dBFS
HD2	2nd Harmonic Distortion A_{IN} = -13 dBFS 0<=Atten<=16[(5)]	f_{IN} = 830 MHz, with board trim		-79.0		dBFS
		f_{IN} = 1760 MHz, with board trim		-101.6		dBFS
		f_{IN} = 2610 MHz, with board trim		-100		dBFS
		f_{IN} = 3610 MHz, with board trim		-101		dBFS
		f_{IN} = 4910 MHz, with board trim		-99.1		dBFS
		f_{IN} = 8150 MHz, with board trim		-107		dBFS
		f_{IN} = 9610 MHz, with board trim		-107		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -13 dBFS 0<=Atten<=16[(5)]	f_{IN} = 830 MHz		-95.4		dBFS
		f_{IN} = 1760 MHz		-95.2		dBFS
		f_{IN} = 2610 MHz		-98		dBFS
		f_{IN} = 3610 MHz		-97		dBFS
		f_{IN} = 4910 MHz		-94		dBFS
		f_{IN} = 8150 MHz		-100		dBFS
		f_{IN} = 9610 MHz		-102		dBFS

7.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -13 dBFS 0<=Atten<=16[5]	f_{IN} = 830 MHz		-89.2		dBFS
		f_{IN} = 1760 MHz		-88.8		dBFS
		f_{IN} = 2610 MHz		-95		dBFS
		f_{IN} = 3610 MHz		-90		dBFS
		f_{IN} = 4910 MHz		-90		dBFS
		f_{IN} = 8150 MHz		-83		dBFS
		f_{IN} = 9610 MHz		-80		dBFS
RX-RX Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN	f_{IN} = 830 MHz		-76.6		dBc
		f_{IN} = 1760 MHz		-70.9		dBc
		f_{IN} = 2610 MHz		-73.5		dBc
		f_{IN} = 3610 MHz		-76.9		dBc
		f_{IN} = 4910 MHz		-65.3		dBc
		f_{IN} = 8150 MHz		-64		dBc
TX-RX Isolation	Far Channel: 2TXOUT to 1RXIN 4TXOUT to 3RXIN	f_{IN} = 830 MHz		-85.9		dBc
		f_{IN} = 1760 MHz		-86.9		dBc
		f_{IN} = 2610 MHz		-91		dBc
		f_{IN} = 3610 MHz		-83		dBc
		f_{IN} = 4910 MHz		-81.9		dBc
		f_{IN} = 8150 MHz		-68		dBc
		f_{IN} = 9610 MHz		-68		dBc

(1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
(2) NLE correction of HD2
(3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
(4) NF increase 1dB per DSA 1dB above DSA = 3dB
(5) DDC Bypass (TI only test mode)

7.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.1			GHz
f_{VCO3}	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.08			GHz
DIV_{DAC}	DAC sample rate divider			1, 2 or 3		
DIV_{FBADC}	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
DIV_{RXADC}	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise F_{PLL} = 11.79848 GHz F_{REF}=491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		–141		dBc/Hz
	Closed Loop Phase Noise F_{PLL}=8.84736 GHz F_{REF}=491.52MHz	600kHz		-114		dBc/Hz
		800kHz		–118		dBc/Hz
		1MHz		–120		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–135		dBc/Hz
		50MHz		–142		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 9.8403 GHz F_{REF}=491.52MHz	600kHz		–113		dBc/Hz
		800kHz		–116		dBc/Hz
		1MHz		–119		dBc/Hz
		1.8MHz		–125		dBc/Hz
		5MHz		–134		dBc/Hz
		50MHz		–140		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 7.86432GHz F_{REF}=491.52MHz	600kHz		–116		dBc/Hz
		800kHz		–119		dBc/Hz
		1MHz		–122		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–136		dBc/Hz
		50MHz		–143		dBc/Hz
F_{rms}	Clock PLL integrated phase error[(1)]	f_{PLL}=11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f_{PLL}=8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f_{PLL}=9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
PN_{pll_flat}	Normalized PLL flat Noise	f_{VCO} = 11796.48MHz		–226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz

7.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SS}	Input Clock level		0.6		1.8	Vppdiff
Coupling				AC Coupling Only		
	REFCLK input impedance(2)	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

7.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V_{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V_{SRCOM}	SerDes Input Common Mode		0.4	0.5	0.6	V
Z_{SRdiff}	SerDes Internal Differential Termination(1)			100		Ω
F_{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance(2)	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V_{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V_{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z_{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V_{IH}	High-Level Input Voltage		0.6×VDD1P8GPIO			V
V_{IL}	Low-Level Input Voltage				0.4×VDD1P8GPIO	V
I_{IH}	High-Level Input Current		–250		250	µA
I_{IL}	Low-Level Input Current		–250		250	µA
C_L	CMOS input capacitance			2		pF
V_{OH}	High-Level Ouput Voltage		VDD1P8GPIO–0.2			V
V_{OL}	Low-Level Output Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
$Clock_{MODE}$				PLL Clock Mode Only		
$F_{SYSREFMAX}$	SYSREF Input Frequency Maximum			40		MHz
$V_{SWINGSRMAX}$	SYSREF Input Swing Maximum			1.8		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} < 500MHz		0.3		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} > 500MHz		0.6		Vppdiff(3)
$V_{COMSRMAX}$	SYSREF Input Common Mode Voltage Maximum			0.8		V
$V_{COMSRMIN}$	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z_T	Input termination	differential		100 (1)		Ω
C_L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V_{ICOM}	Input Common Voltage			1.2		V
V_{ID}	Differential Input Voltage swing			450		Vppdiff(3)

7.8 Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_T	Input termination	differential		100		Ω
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V
V_{OD}	Differential Output Voltage swing			500		Vppdiff(3)
Z_T	Internal Termination			100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Loss tolerance is bump to bump from STX to SRX
(3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

7.9 Power Supply Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, f_{DAC} = 9000MSPS interleave mode; f_{ADC} = 3000MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T4R - TDD with TX 75%, RX 25% TX Dual Band: 72x Int, TX Rate 125 MSPS RX Dual Band: 24x Dec, RX Rate 125 MSPS f_{DAC} = 9000MSPS, f_{OUT}=f_{IN}= 1.9, 2.6 GHz f_{ADC} = 3000MSPS JESD: 8/10 coding, 20Gbps TX: 2-16-16-1, RX: 2-16-16-1		765		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			395		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			69		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1151		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2001		mA
P_{diss}	Power Dissipation			5446		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4T4R - FDD TX Dual Band: 96x Int, TX Rate 125 MSPS RX Dual Band: RX 24x, RX Rate 125 MSPS f_{DAC} = 12 GSPS, f_{TX} = 1.85 + 2.15 GHz f_{ADC} = 3 GSPS, f_{RX} = 1.75 + 1.88 GHz JESD: 8/10 coding, 20Gbps TX: 2-16-16-1, RX: 2-16-16-1		1338		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			506		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			2109		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3311		mA
P_{diss}	Power Dissipation			9041		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R - FDD TX Single Band: 96x Int, TX Rate 125 MSPS RX Single Band: RX 24x, RX Rate 125 MSPS f_{DAC} = 12 GSPS, f_{TX} = 1.85 + 2.15 GHz f_{ADC} = 3 GSPS, f_{RX} = 1.75 + 1.88 GHz JESD: 8/10 coding, 20Gbps TX: 1-8-16-1, RX: 1-8-16-1		1332		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			496		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			2099		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2950		mA
P_{diss}	Power Dissipation			8667		mW

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, f_{DAC} = 9000MSPS interleave mode; f_{ADC} = 3000MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R - FDD TX Single Band: 24x Int, TX Rate 500 MSPS RX Single Band: RX 6x, RX Rate 500 MSPS f_{DAC} = 12 GSPS, f_{TX} = 1.85 + 2.15 GHz f_{ADC} = 3 GSPS, f_{RX} = 1.75 + 1.88 GHz JESD: 8/10 coding, 20Gbps TX: 4-8-4-1, RX: 4-8-4-1		1331		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			648		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			2096		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3269		mA
P_{diss}	Power Dissipation			9230		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: same configuration as Mode 4 Sleep Mode. SLEEP pin is pull high.		98		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			330		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			16		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			48		mA
	Group 1A: DVDD0P9 + VDDT0P9			305		mA
	Power Dissipation			1140		mW

7.10 Timing Requirements

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{s(SYSREF)}$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{h(SYSREF)}$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{s(SENB)}$	Setup Time, SENB to Rising Edge of SCLK			15	ns
$t_{h(SENB)}$	Hold Time, SENB after last Rising Edge of SCLK [1]			5 + t_{SCLK}	ns
$t_{s(SDIO)}$	Setup Time, SDIO valid to Rising Edge of SCLK			15	ns
$t_{h(SDIO)}$	Hold Time, SDIO valid after Rising Edge of SCLK			5	ns
$t_{(SCLK)\_W}$	Minimum SCLK period: registers write			25	ns
$t_{(SCLK)\_R}$	Minimum SCLK period: registers read			50	ns
$t_{d(data\_out)}$	Minimum Data Output delay after Falling Edge of SCLK			0	ns
	Maximum Data Output delay after Falling Edge of SCLK			15	ns
t_{RESET}	Minimum $\overline{RESET}$ Pulse Width		1		ms

(1) SDEN\\ need to be held one more extra clock cycle with the last SCLK edge

7.11 Switching Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

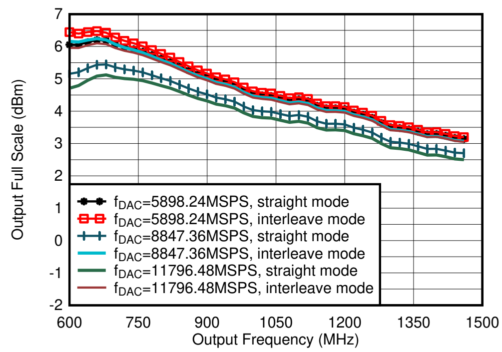
<table>
<tr><th colspan="2">PARAMETER</th><th>TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td colspan="7">TX Channel Latency</td></tr>
<tr><td></td><td>SerDes Receiver Analog Delay</td><td>Full rate</td><td></td><td>2.8</td><td></td><td>ns</td></tr>
<tr><td rowspan="4">t_{JESDTX}</td><td rowspan="4">JESD to TX output Latency</td><td>LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)</td><td></td><td>152</td><td></td><td rowspan="4">interface clock cycles(1)</td></tr>
<tr><td>LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)</td><td></td><td>176</td><td></td></tr>
<tr><td>LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)</td><td></td><td>124</td><td></td></tr>
<tr><td>LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)</td><td></td><td>97</td><td></td></tr>
<tr><td colspan="7">RX Channel Latency</td></tr>
<tr><td></td><td>SerDes Transmitter Analog Delay</td><td></td><td></td><td>3.6</td><td></td><td>ns</td></tr>
<tr><td rowspan="3">t_{JESDRX}</td><td rowspan="3">RX input to JESD output Latency</td><td>LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)</td><td></td><td>92</td><td></td><td rowspan="3">interface clock cycles(1)</td></tr>
<tr><td>LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)</td><td></td><td>108</td><td></td></tr>
<tr><td>LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)</td><td></td><td>153</td><td></td></tr>
<tr><td colspan="7">FB Channel Latency</td></tr>
<tr><td></td><td>SerDes Transmitter Analog Delay</td><td></td><td></td><td>3.6</td><td></td><td>ns</td></tr>
<tr><td rowspan="2">t_{JESDFB}</td><td rowspan="2">FB input to JESD output Latency</td><td>LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation</td><td></td><td>151</td><td></td><td rowspan="2">interface clock cycles(1)</td></tr>
<tr><td>LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation</td><td></td><td>177</td><td></td></tr>
</table>

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

7.12 Typical Characteristics

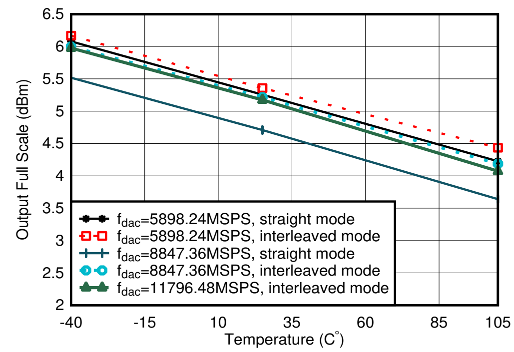
7.12.1 TX Typical Characteristics 800 MHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



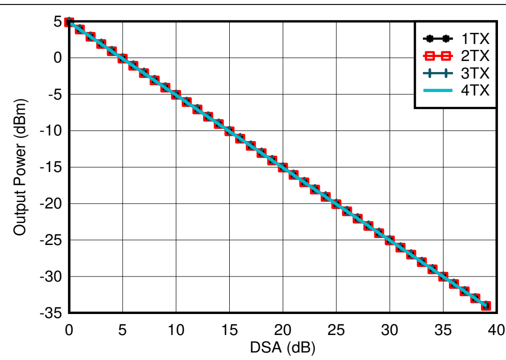
including PCB and cable losses, A_{out} = -0.5d FBS, DSA = 0, 0.8 GHz matching

図 7-1. TX Output Fullscale vs Output Frequency



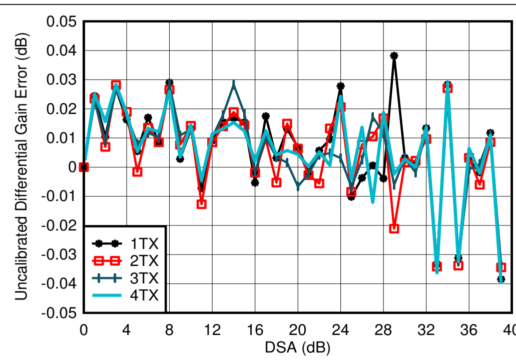
including PCB and cable losses, A_{out} = -0.5d FBS, DSA = 0, 0.8 GHz matching

図 7-2. TX Output Fullscale vs Temperature



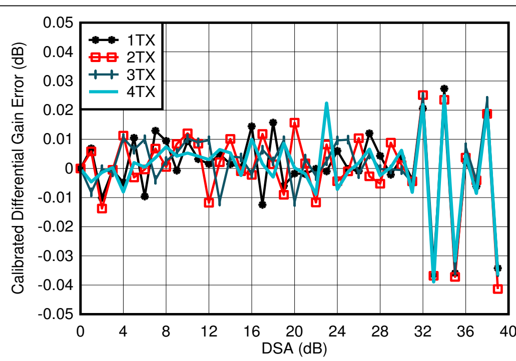
f_{DAC} = 11796.48 MSPS, interleave mode, A_{out} = -0.5 dFBS, matching 0.8 GHz

図 7-3. TX Output Power vs DSA Setting and Channel at 0.85 GHz



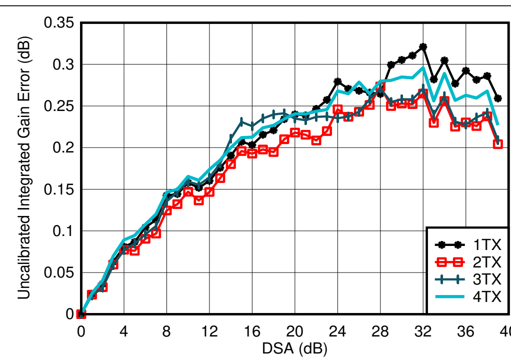
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-4. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-5. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz

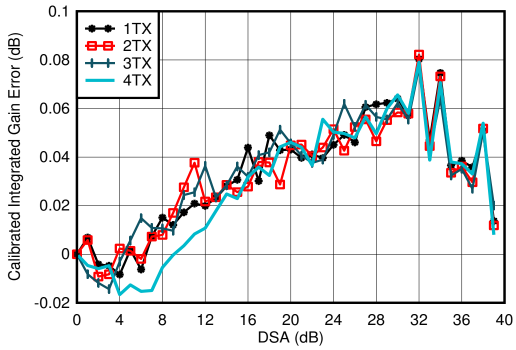


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Settings

図 7-6. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

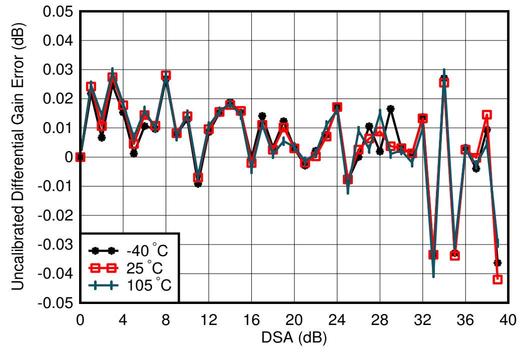
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



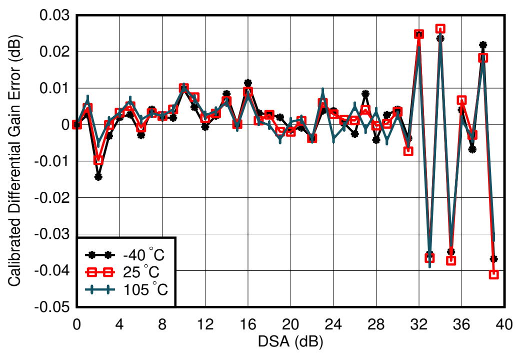
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 7-7. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



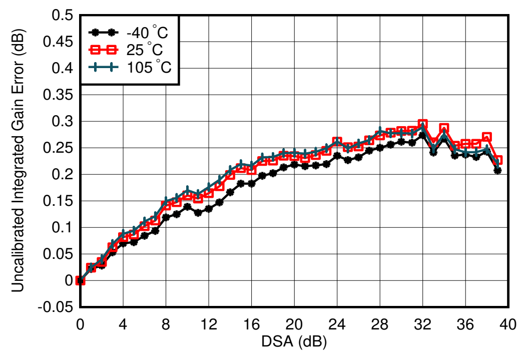
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-8. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



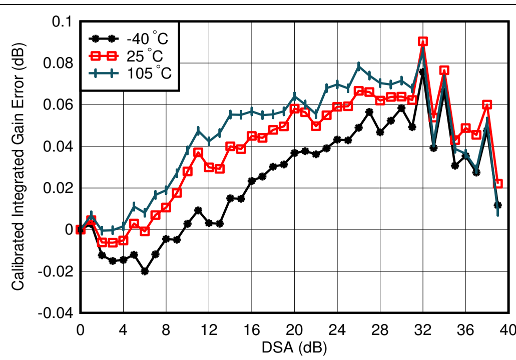
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-9. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



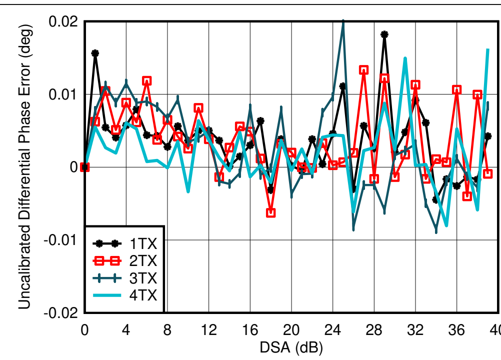
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 7-10. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 7-11. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

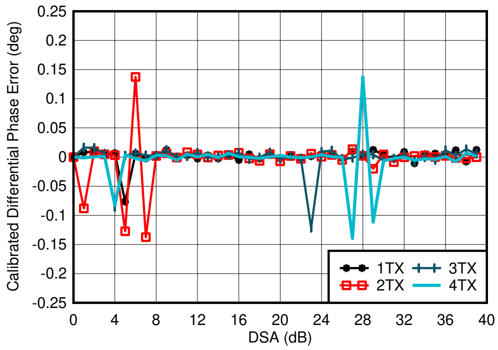


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-12. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

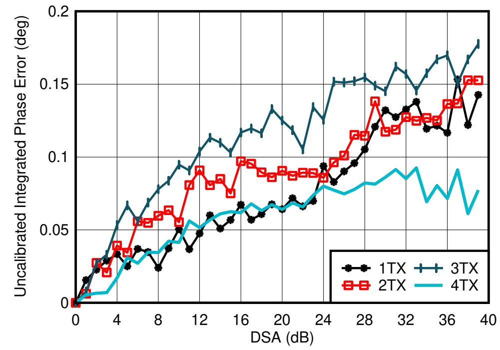
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



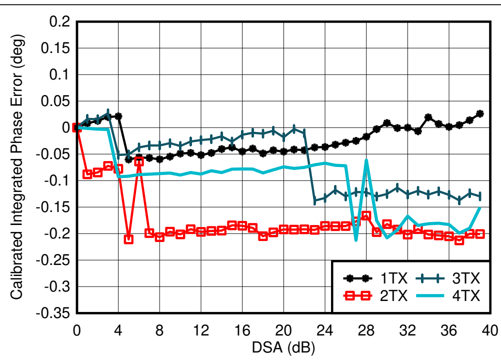
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 7-13. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



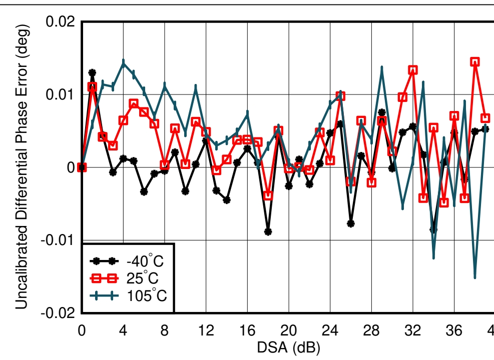
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 7-14. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 7-15. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

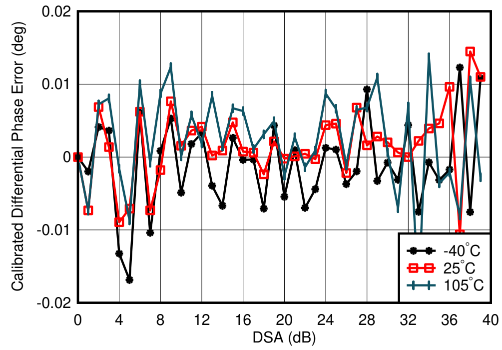


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

図 7-16. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz

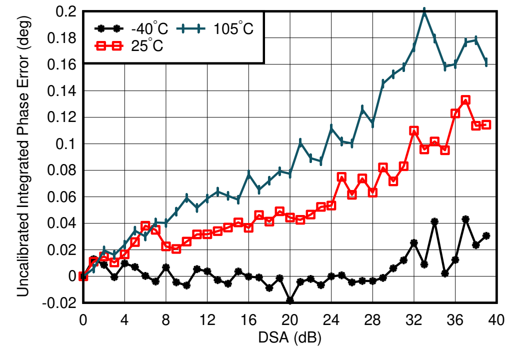
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



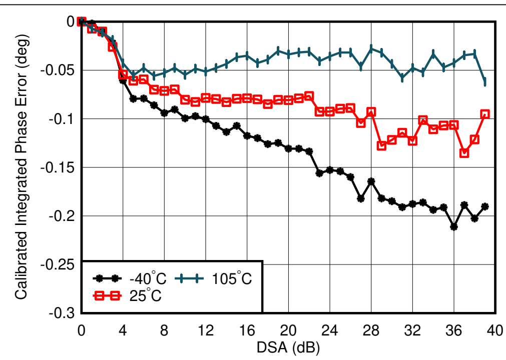
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

図 7-17. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



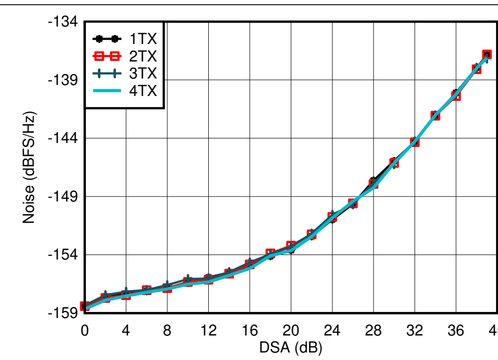
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 7-18. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



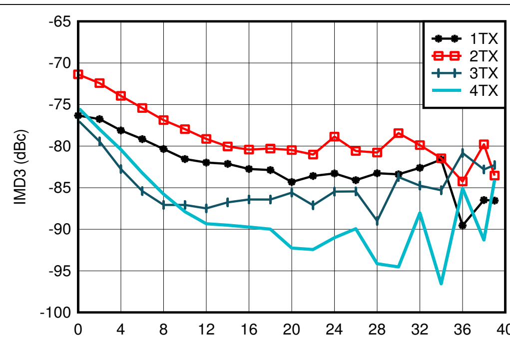
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 7-19. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



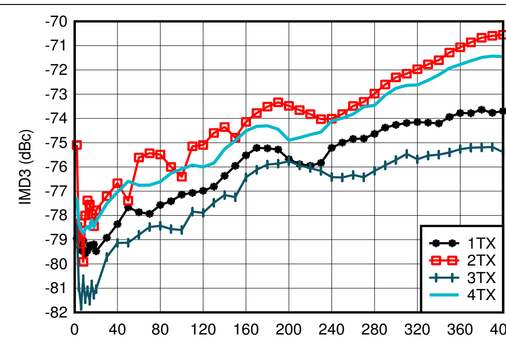
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz, P_{OUT} = –13 dBFS

図 7-20. TX Output Noise vs Channel and Attenuation at 0.85 GHz



f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 7-21. TX IMD3 vs DSA Setting at 0.85 GHz

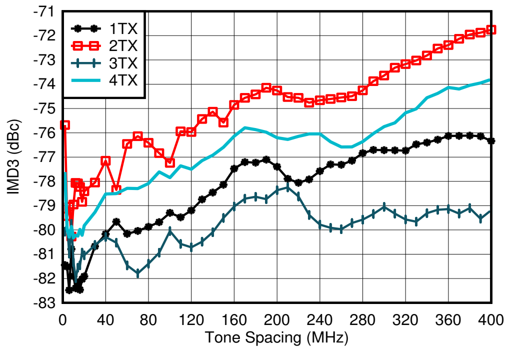


f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 7-22. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz

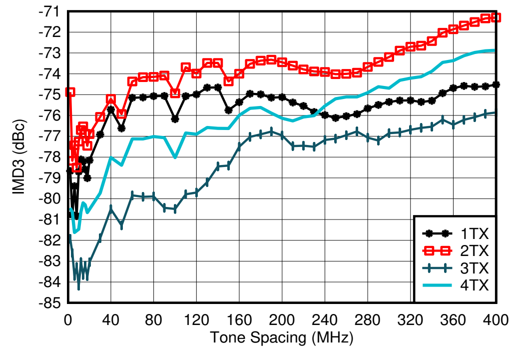
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



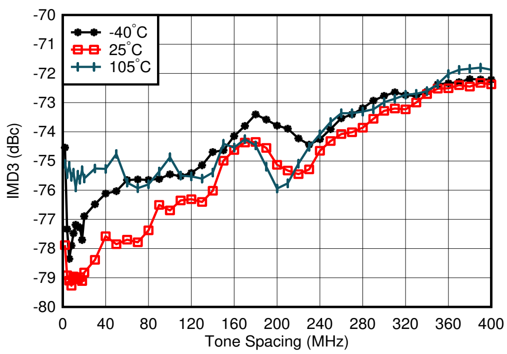
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 7-23. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



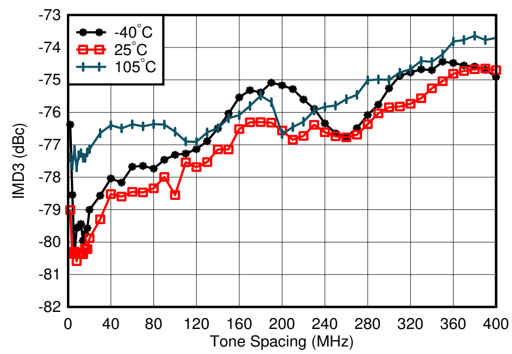
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 7-24. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



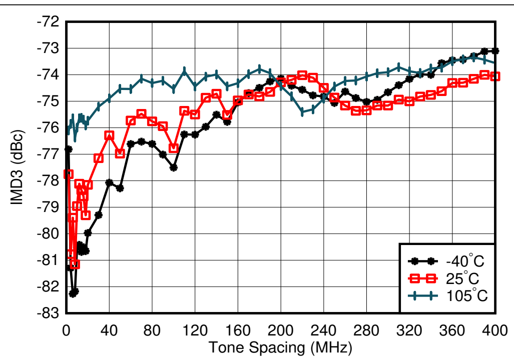
f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 7-25. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



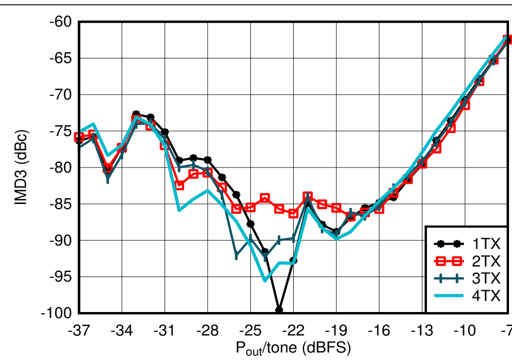
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 7-26. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



f_{DAC} = 11796.48 MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 7-27. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

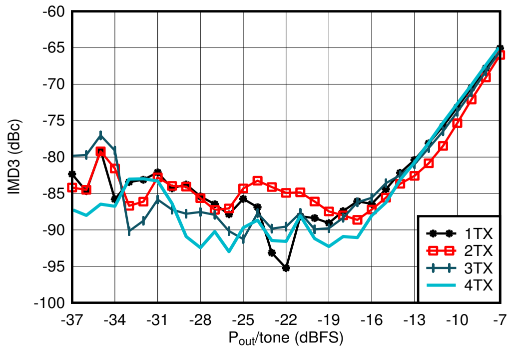


f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 7-28. TX IMD3 vs Digital Level at 0.85 GHz

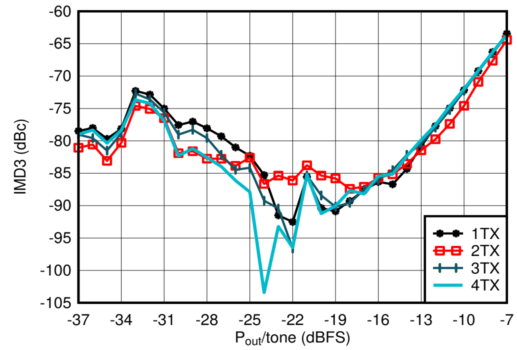
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



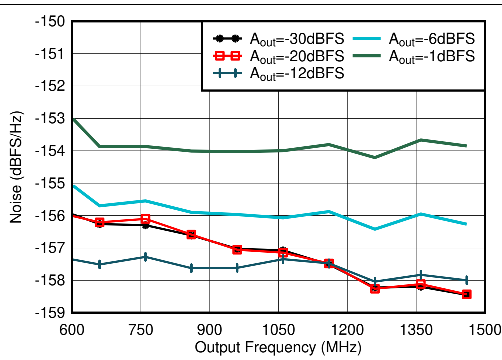
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 7-29. TX IMD3 vs Digital Level at 0.85 GHz



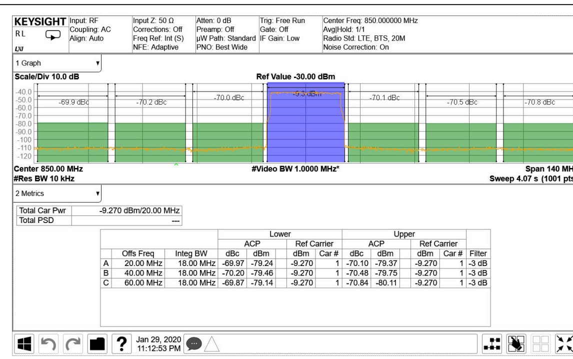
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 7-30. TX IMD3 vs Digital Level at 0.85 GHz



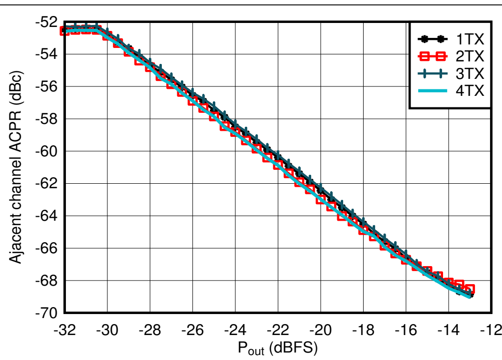
Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset, DSA = 0dB

図 7-31. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz



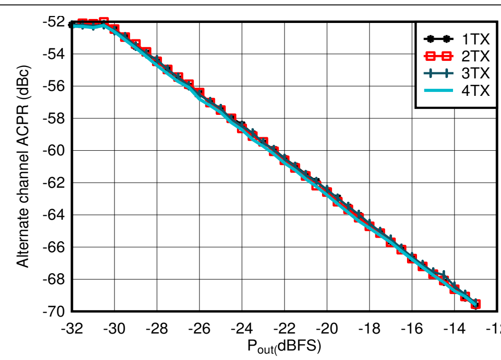
TM1.1, P_{OUT_RMS} = –13 dBFS

図 7-32. TX 20-MHz LTE Output Spectrum at 0.85 GHz



Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-33. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz

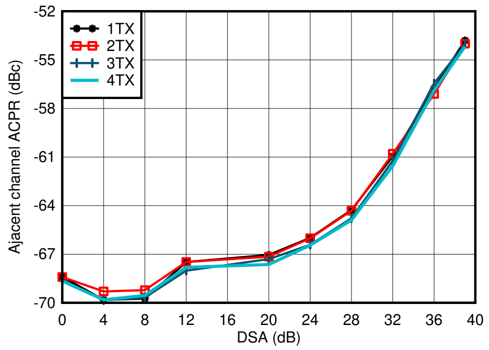


Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-34. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz

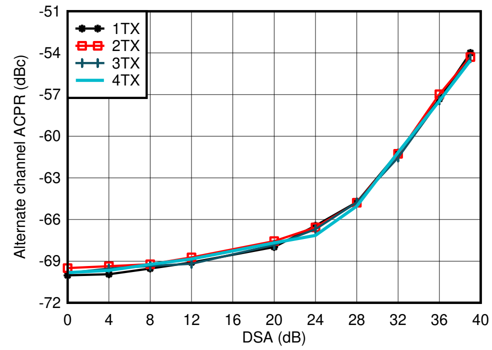
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



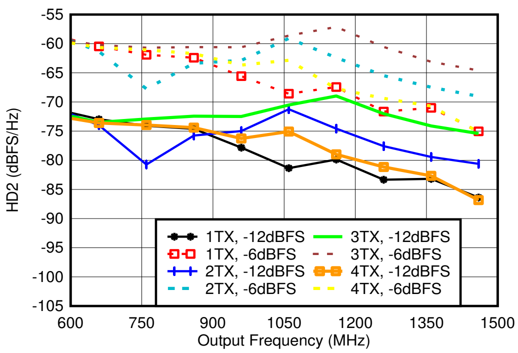
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-35. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz



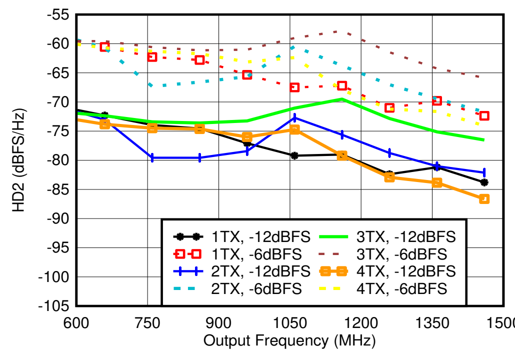
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-36. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz



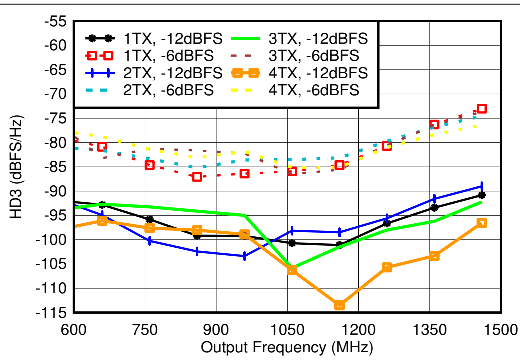
Matching at 0.8 GHz, f_{DAC} = 5898.24 GSPS, straight mode

図 7-37. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



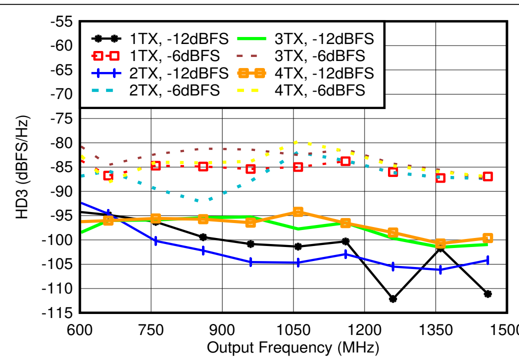
Matching at 0.8 GHz, f_{DAC} = 8847.36GSPS, straight mode

図 7-38. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



Matching at 0.8 GHz, f_{DAC} = 5898.24 MSPS, straight mode, normalized to output power at harmonic frequency

図 7-39. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz

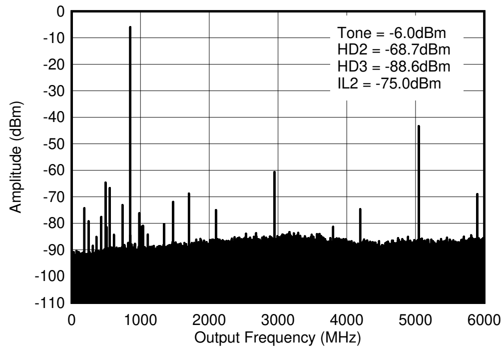


Matching at 0.8 GHz, f_{DAC} = 8847.36 MSPS, straight mode, normalized to output power at harmonic frequency

図 7-40. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz

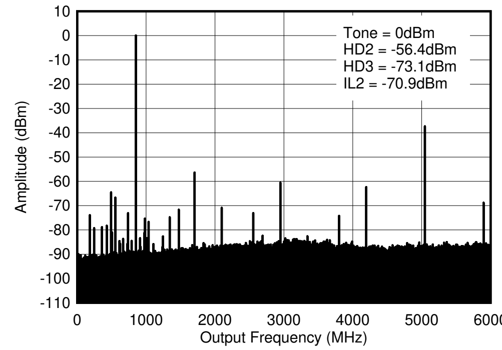
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



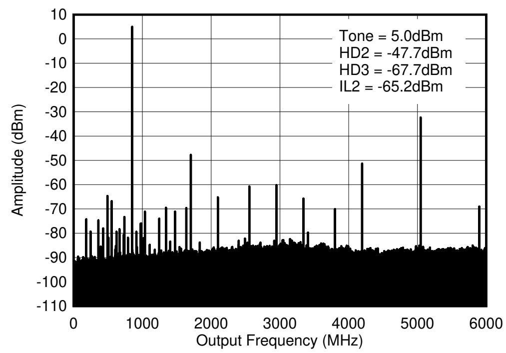
f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 7-41. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 7-42. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

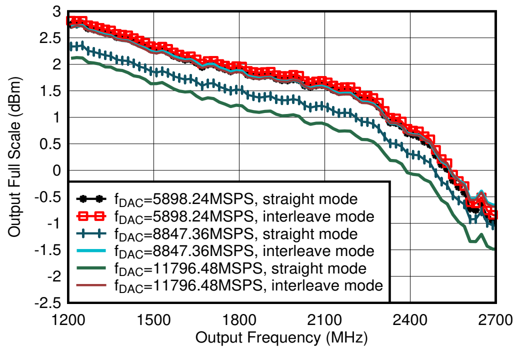


f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 7-43. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

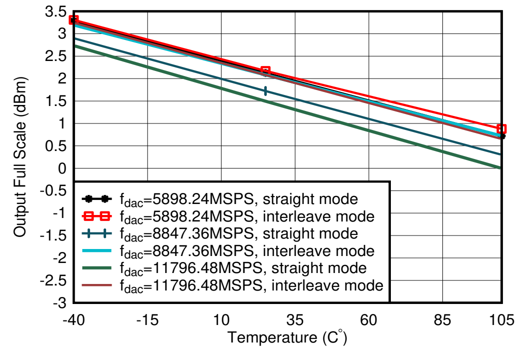
7.12.2 TX Typical Characteristics at 1.8 GHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



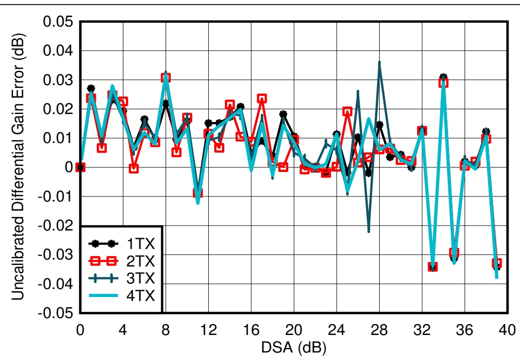
including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 1.8 GHz matching

図 7-44. TX Output Fullscale vs Output Frequency



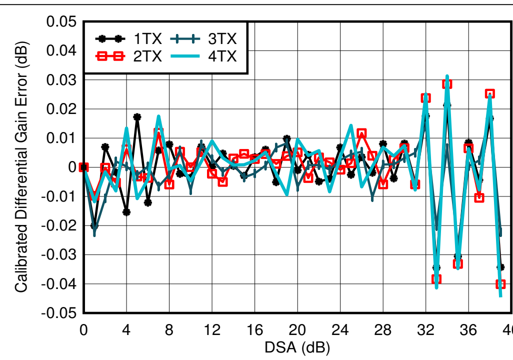
A_{out} = -0.5 dFBS, matching 1.8 GHz

図 7-45. TX Output Power vs Temperature at 1.8 GHz



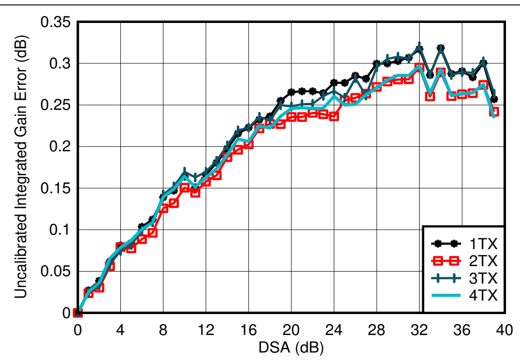
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-46. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



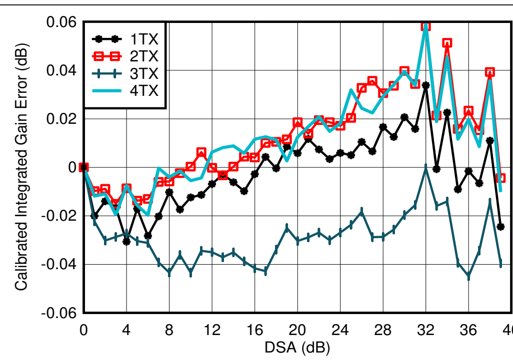
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-47. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-48. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

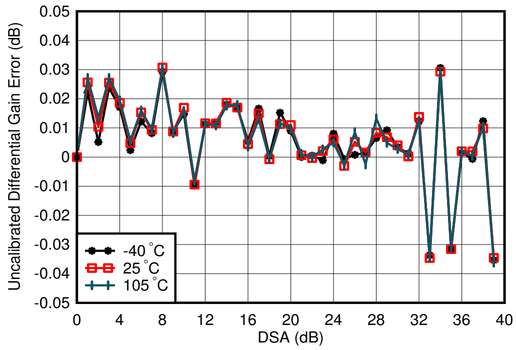


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-49. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

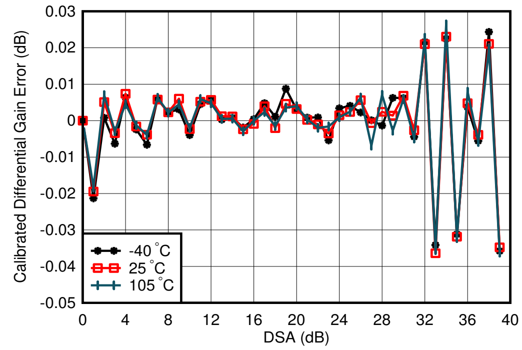
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



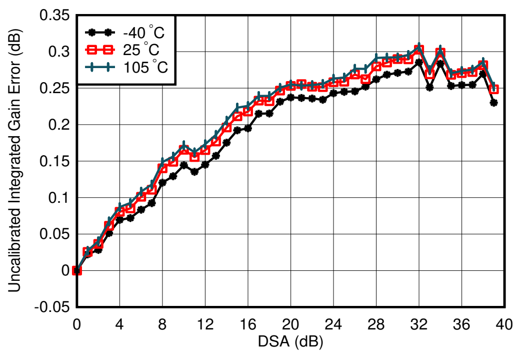
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-50. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



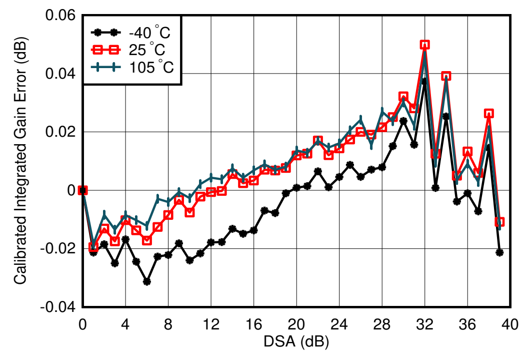
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-51. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-52. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz

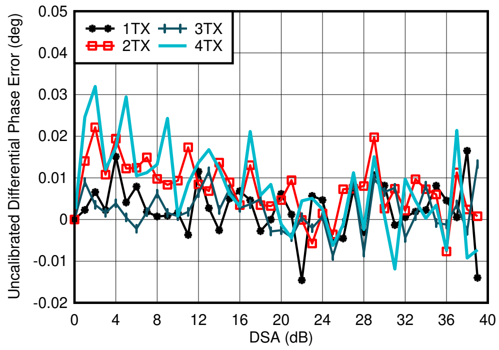


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-53. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz

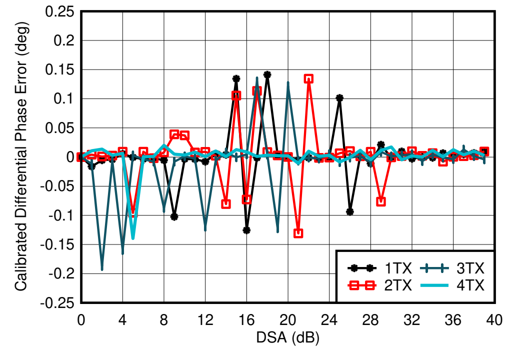
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



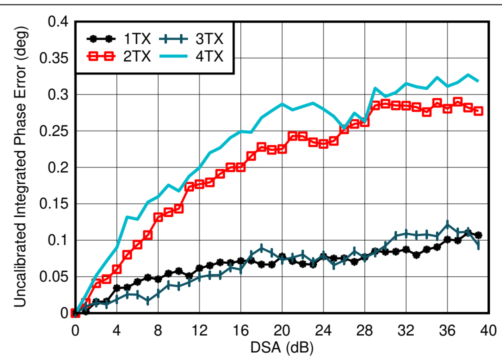
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-54. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz



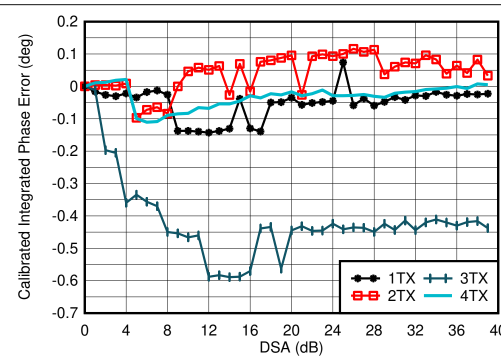
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 7-55. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-56. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz

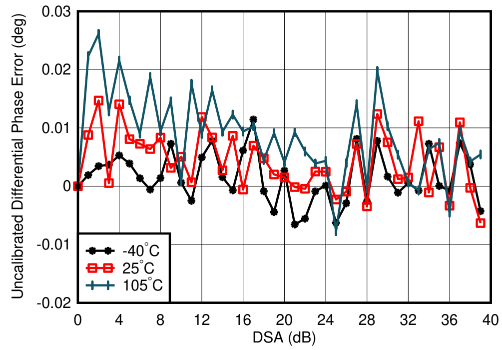


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-57. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz

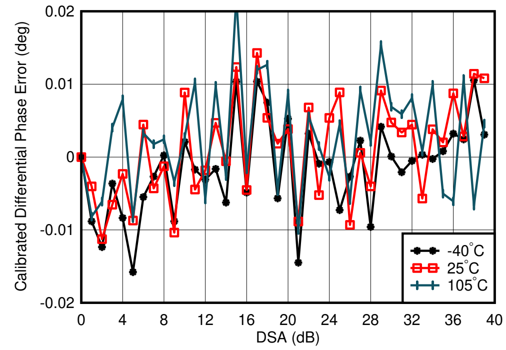
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



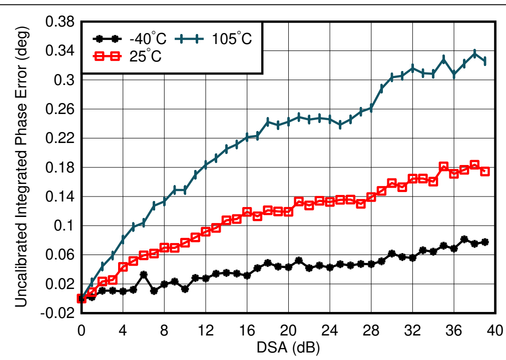
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-58. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz



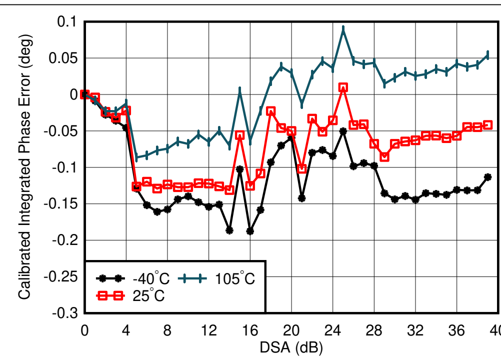
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-59. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz



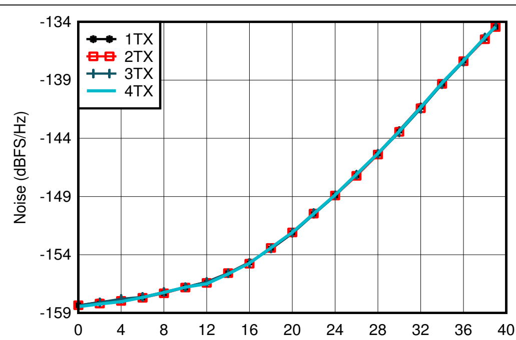
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-60. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



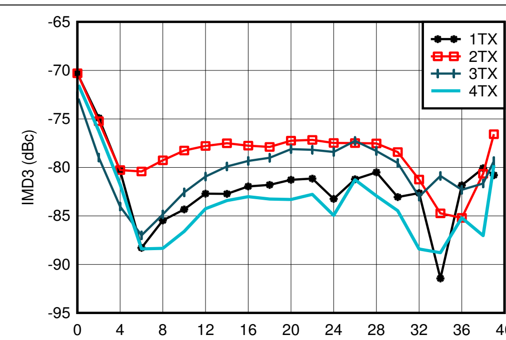
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-61. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 1.8 GHz, P_{OUT} = –13 dBFS

図 7-62. TX Output Noise vs Channel and Attenuation at 1.8 GHz

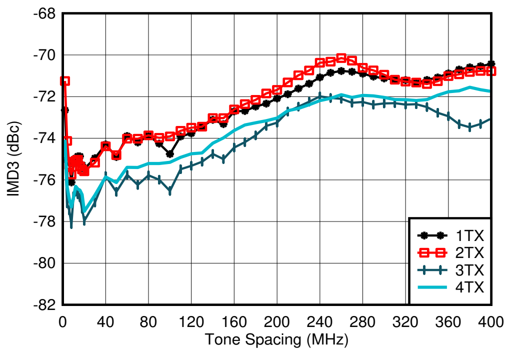


f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 1.8 GHz, matching at 1.8 GHz, –13 dBFS each tone

図 7-63. TX IMD3 vs DSA Setting at 1.8 GHz

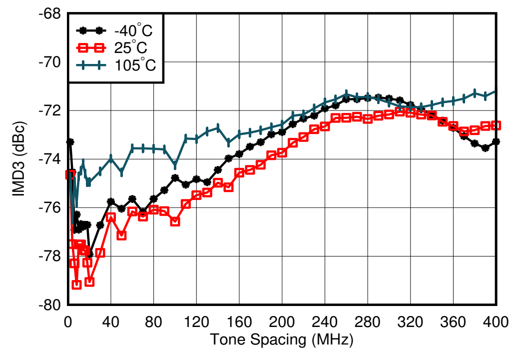
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



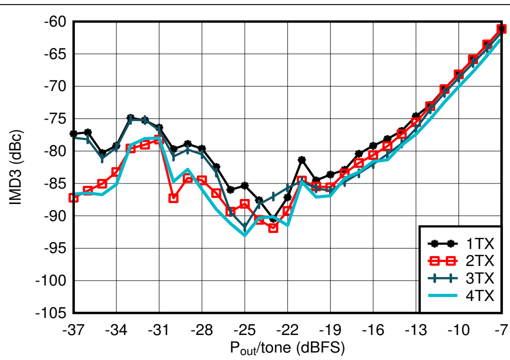
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 1.8 GHz, matching at 1.8 GHz, –13 dBFS each tone

図 7-64. TX IMD3 vs Tone Spacing and Channel at 1.8 GHz



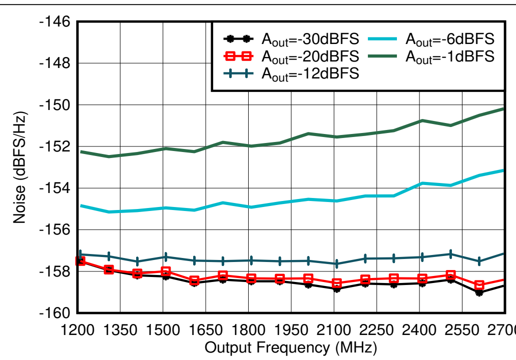
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 1.8 GHz, matching at 1.8 GHz, –13 dBFS each tone, worst channel

図 7-65. TX IMD3 vs Tone Spacing and Temperature at 1.8 GHz



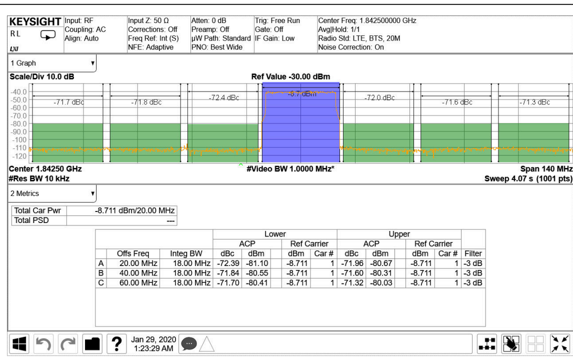
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 1.8 GHz, $f_{SPACING}$ = 20 MHz, matching at 1.8 GHz

図 7-66. TX IMD3 vs Digital Level at 1.8 GHz



Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648 GSPS, interleave mode, 40-MHz offset

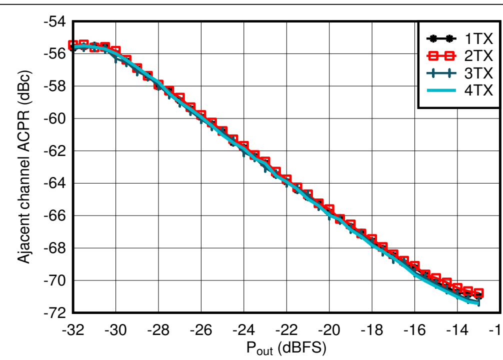
図 7-67. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



			Lower				Upper				
			ACP		Ref Carrier		ACP		Ref Carrier		
	Offs Freq	Integ BW	dBc	dBm	dBm	Car #	dBc	dBm	dBm	Car #	Filter
A	20.00 MHz	18.00 MHz	-72.39	-81.10	-8.711	1	-71.96	-80.67	-8.711	1	-3 dB
B	40.00 MHz	18.00 MHz	-71.84	-80.55	-8.711	1	-71.60	-80.31	-8.711	1	-3 dB
C	60.00 MHz	18.00 MHz	-71.70	-80.41	-8.711	1	-71.32	-80.03	-8.711	1	-3 dB

TM1.1, P_{OUT_RMS} = –13 dBFS

図 7-68. TX 20-MHz LTE Output Spectrum at 1.8425 GHz

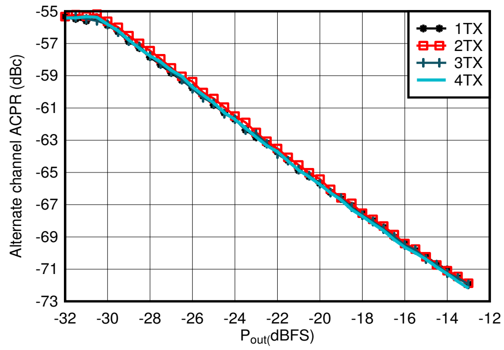


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-69. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz

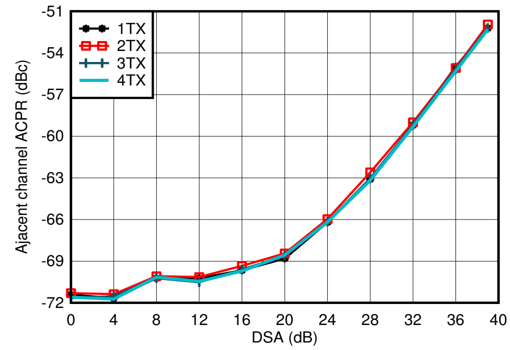
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



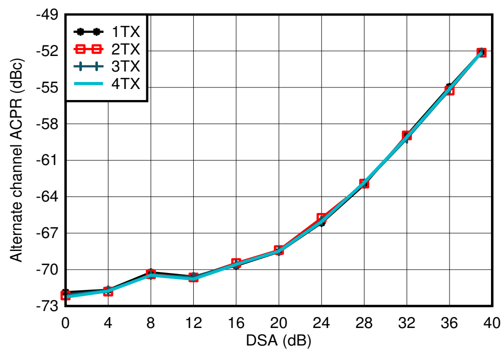
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-70. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz



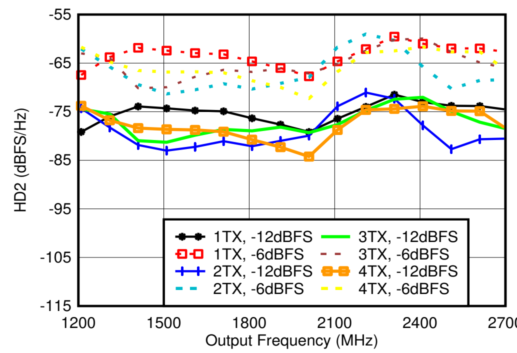
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-71. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz



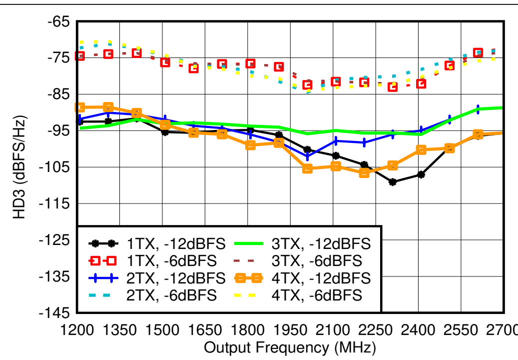
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-72. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz



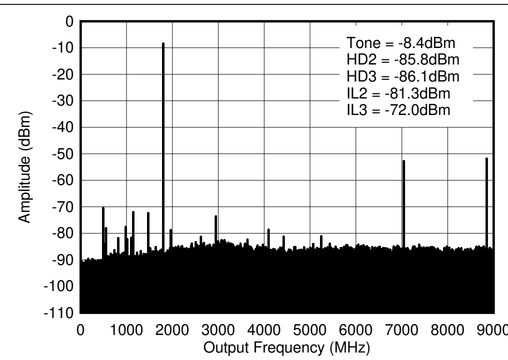
Matching at 1.8 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 7-73. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



Matching at 1.8 GHz, f_{DAC} = 11.7964 8GSPS, interleave mode, normalized to output power at harmonic frequency

図 7-74. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz

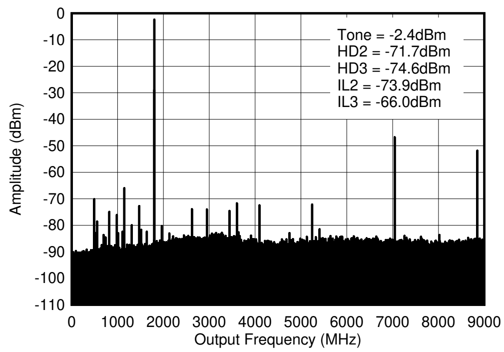


f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 7-75. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

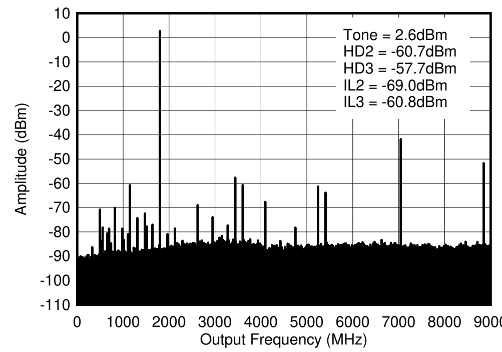
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 7-76. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

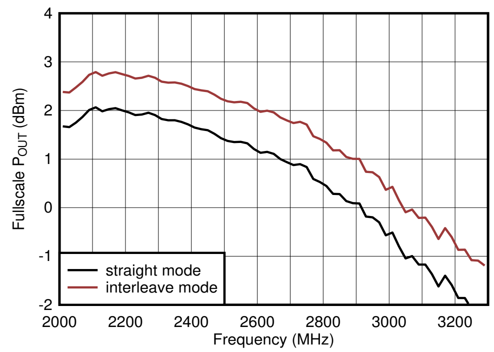


f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 7-77. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

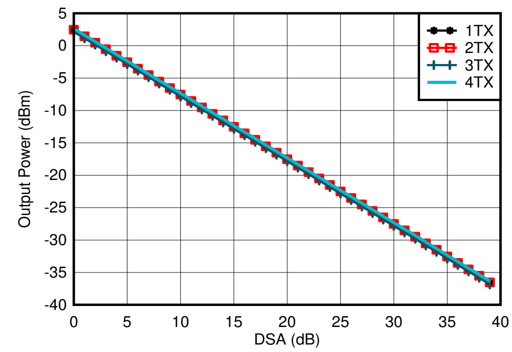
7.12.3 TX Typical Characteristics at 2.6 GHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



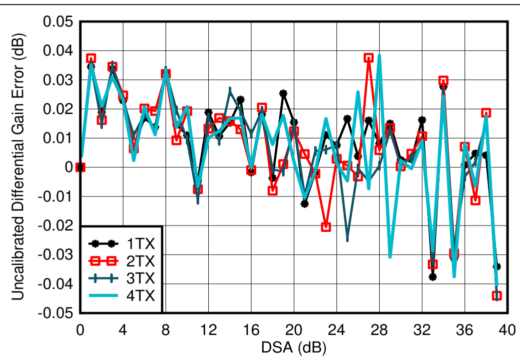
Including PCB and cable losses, A_{out} = -0.5d BFS, DSA = 0, 2.6 GHz matching

図 7-78. TX Full Scale vs RF Frequency at 11796.48 MSPS



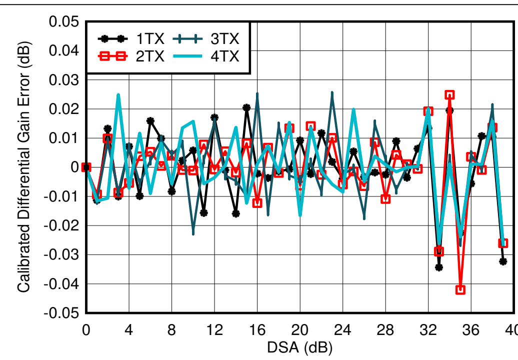
f_{DAC} = 8847.36 MSPS, A_{out} = -0.5 dBFS, matching 2.6 GHz

図 7-79. TX Output Power vs DSA Setting and Channel at 2.6 GHz



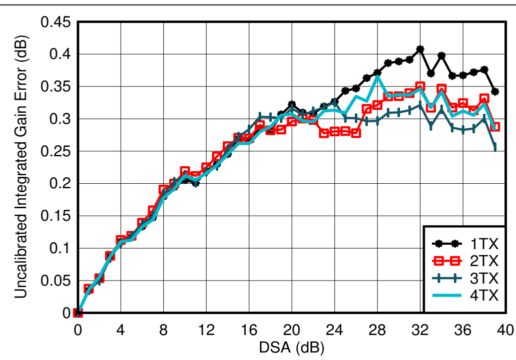
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-80. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



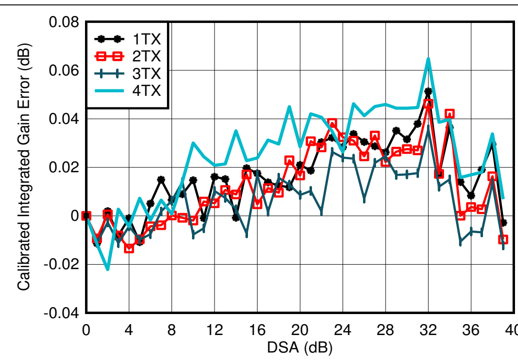
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-81. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-82. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

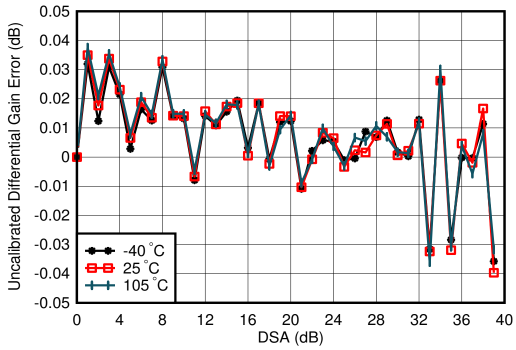


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-83. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

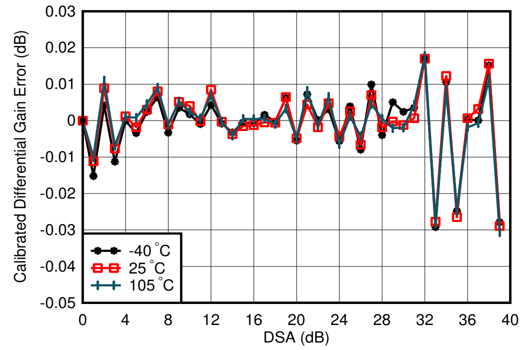
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



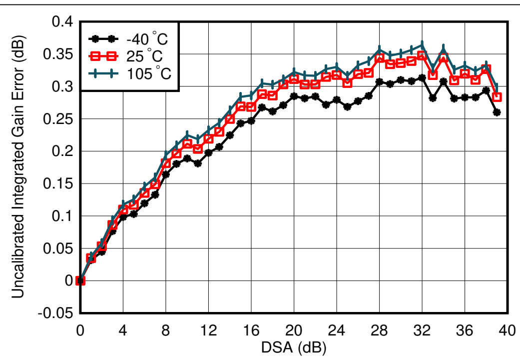
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-84. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



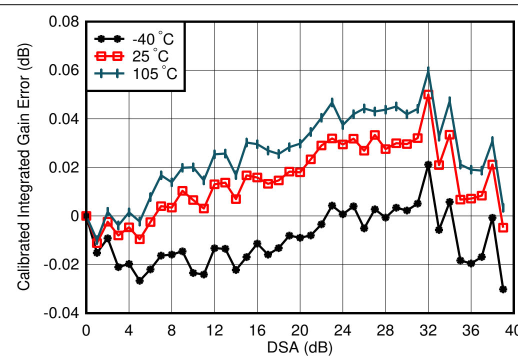
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-85. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-86. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

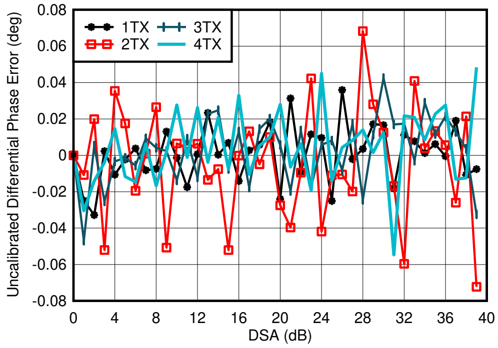


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-87. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

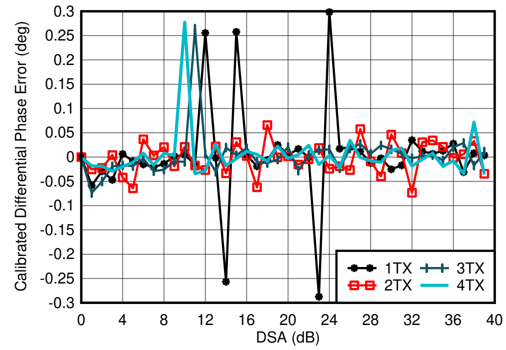
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



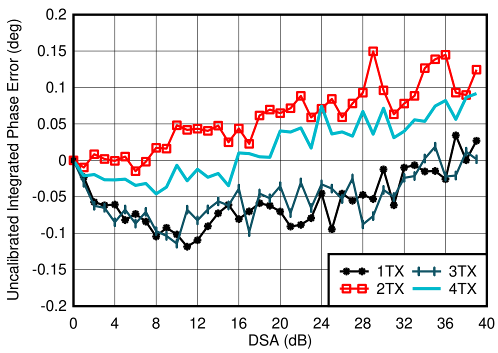
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-88. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



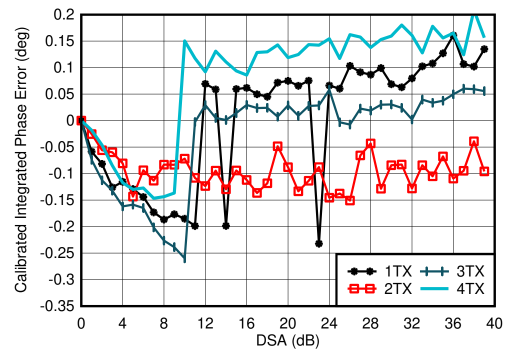
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 7-89. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-90. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

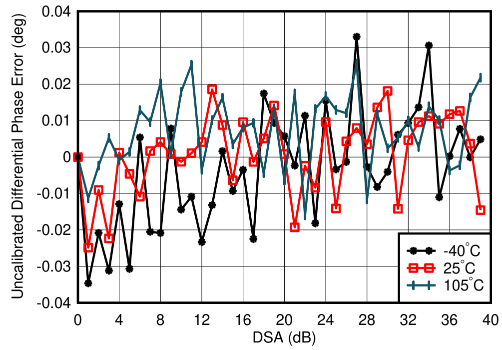


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-91. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

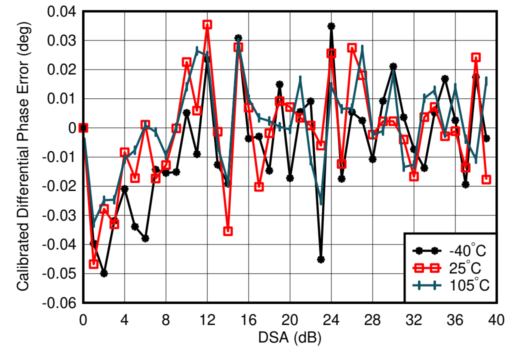
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



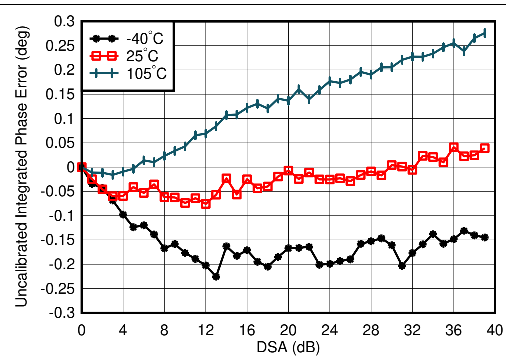
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-92. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



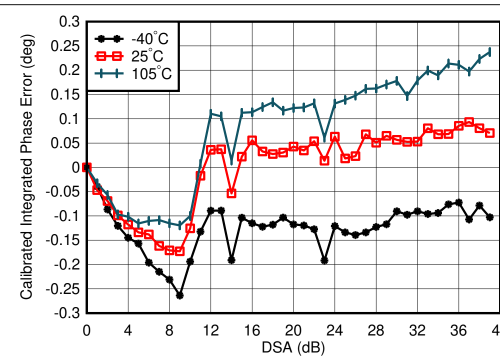
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-93. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



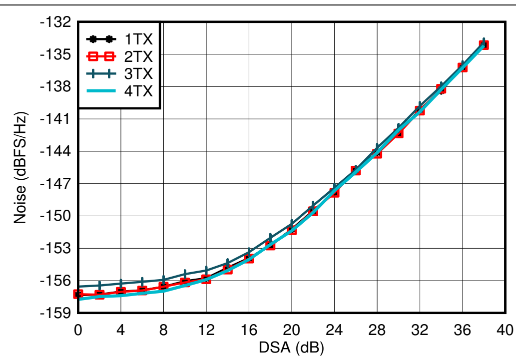
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-94. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



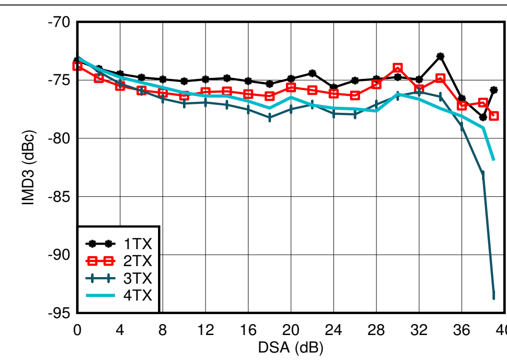
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-95. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, P_{OUT} = –13 dBFS

図 7-96. TX Output Noise vs Channel and Attenuation at 2.6 GHz

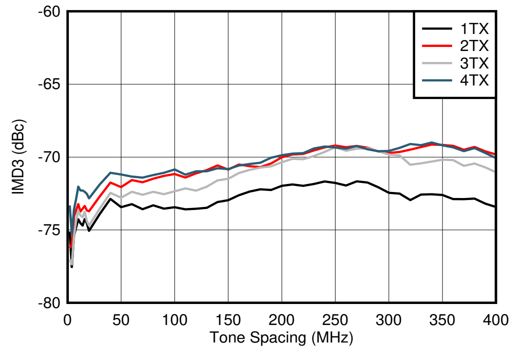


f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 7-97. TX IMD3 vs DSA Setting at 2.6 GHz

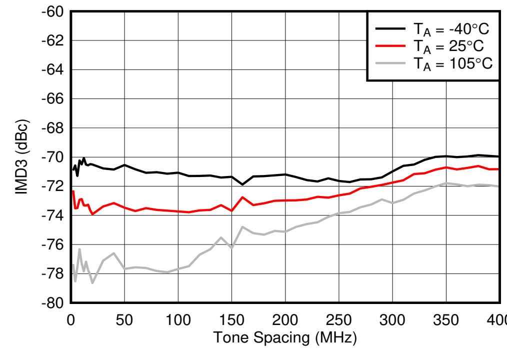
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



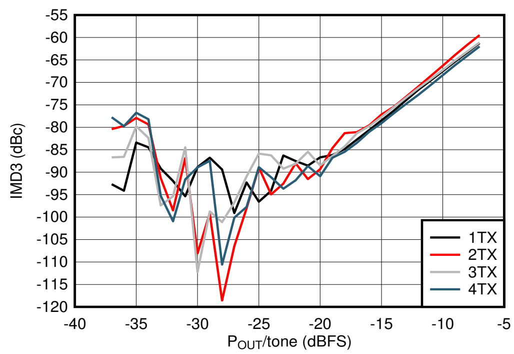
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 7-98. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



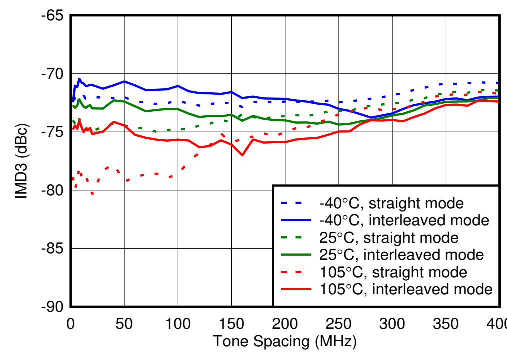
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone, worst channel.

図 7-99. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



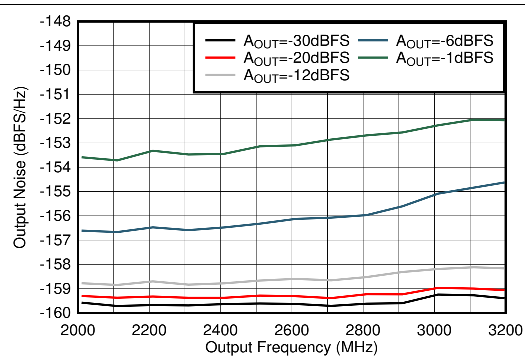
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, $f_{SPACING}$ = 20 MHz, matching at 2.6 GHz

図 7-100. TX IMD3 vs Digital Level at 2.6 GHz



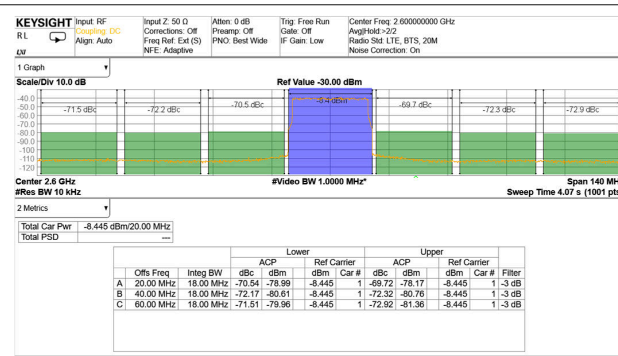
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 7-101. TX IMD3 vs Tone Spacing and Temperature



Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648 GSPS, interleave mode, 40-MHz offset

図 7-102. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz

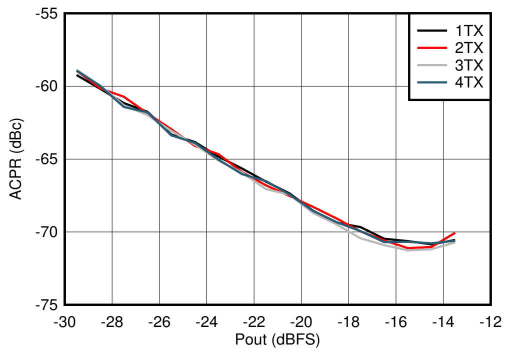


TM1.1, P_{OUT_RMS} = –13 dBFS

図 7-103. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)

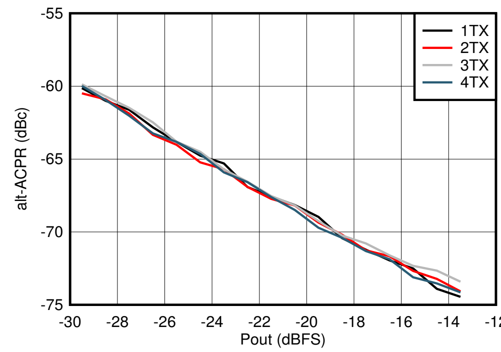
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



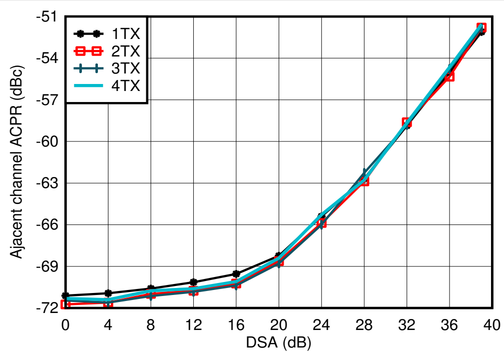
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-104. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



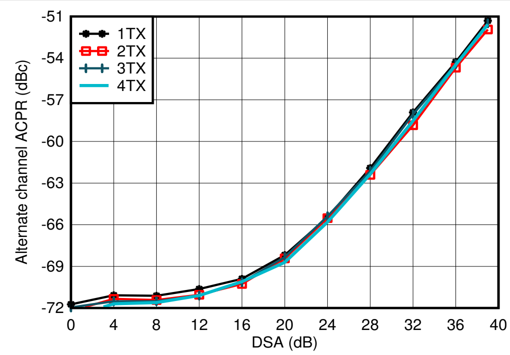
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-105. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



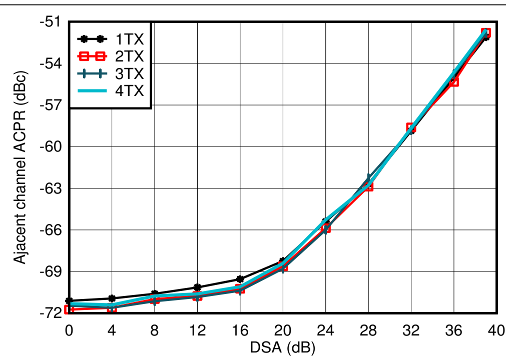
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-106. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



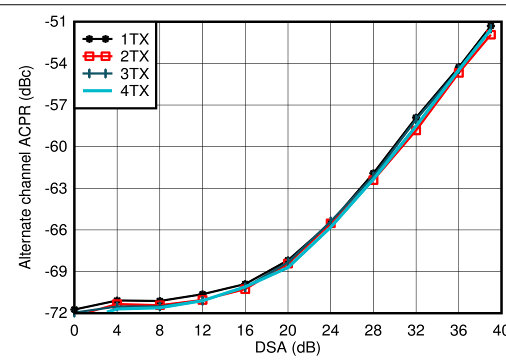
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-107. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-108. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

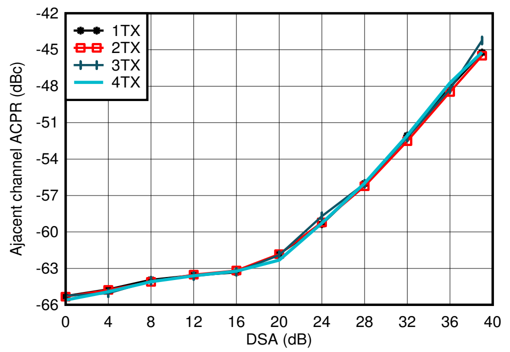


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-109. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz

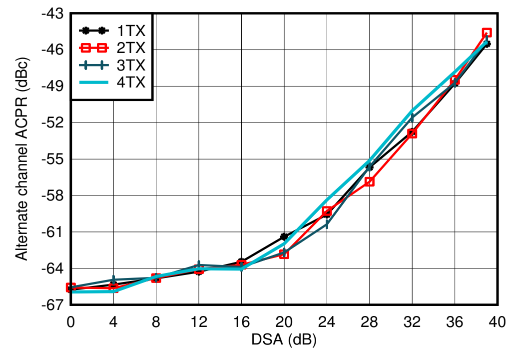
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



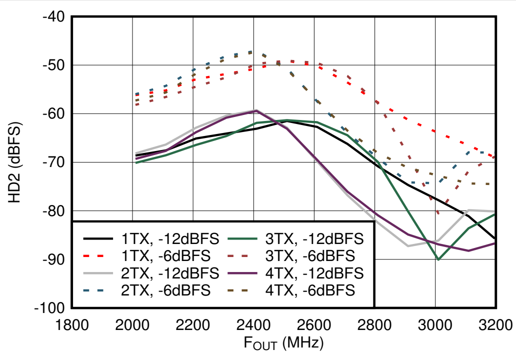
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 7-110. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



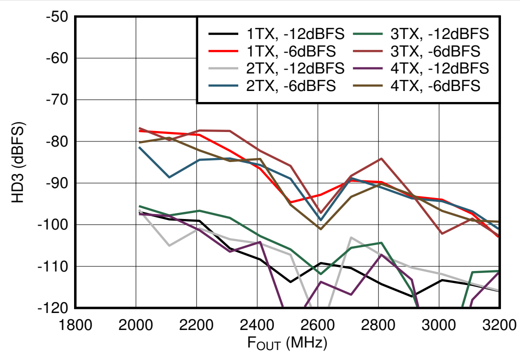
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 7-111. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



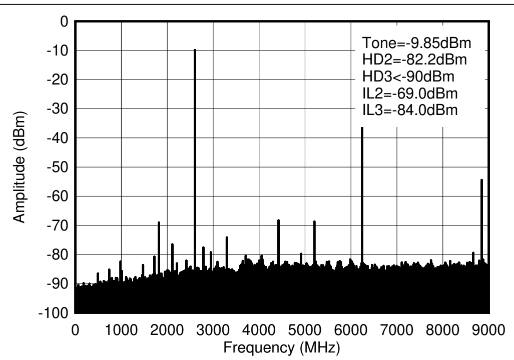
Matching at 2.6 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

図 7-112. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz



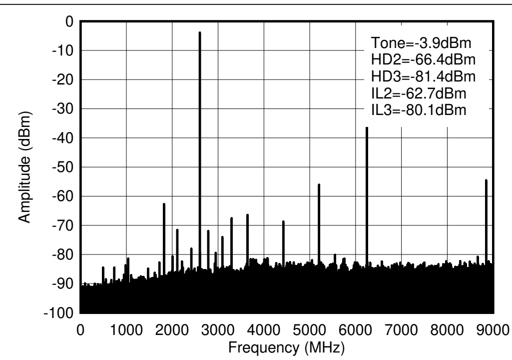
Matching at 2.6 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 7-113. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 7-114. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

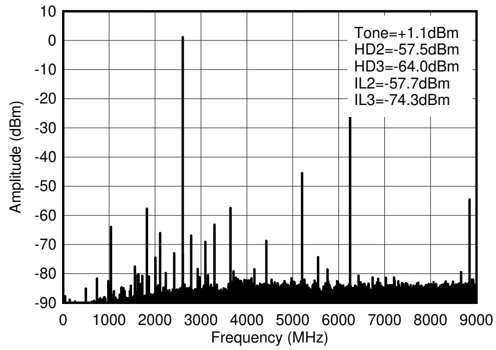


f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 7-115. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

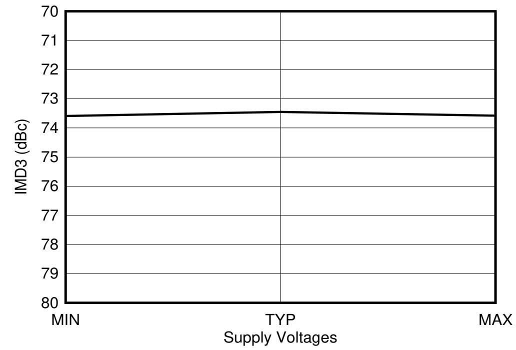
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 7-116. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

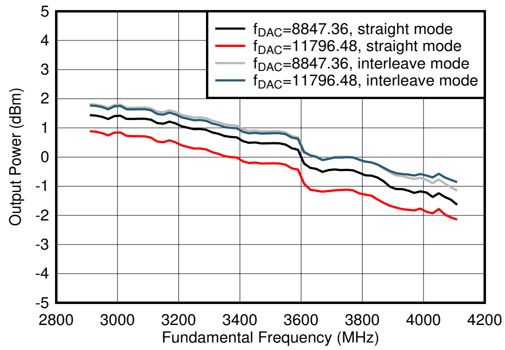


f_{DAC} = 11796.48 MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

図 7-117. TX IMD3 vs Supply Voltage at 2.6 GHz

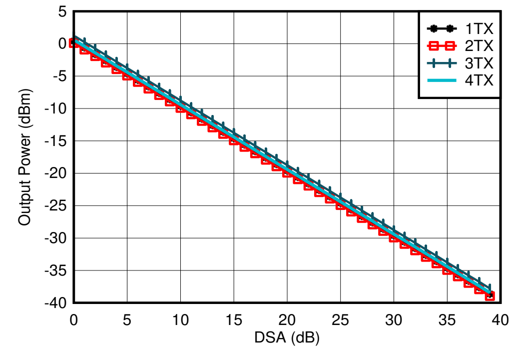
7.12.4 TX Typical Characteristics at 3.5 GHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



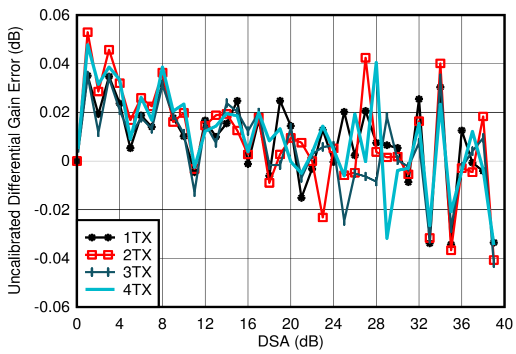
A_{out} = -0.5 dFBS, 3.5 GHz Matching, included PCB and cable losses

図 7-118. TX Output Power vs Frequency



A_{out} = -0.5 dFBS, 3.5 GHz Matching, included PCB and cable losses

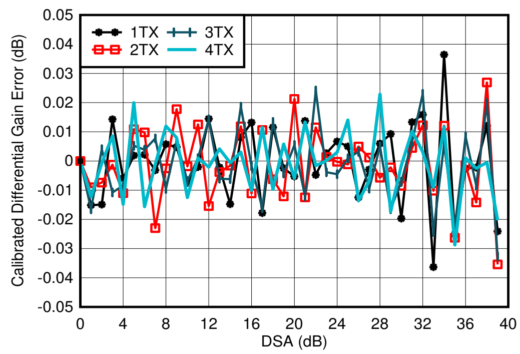
図 7-119. TX Output Power vs DSA Setting at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

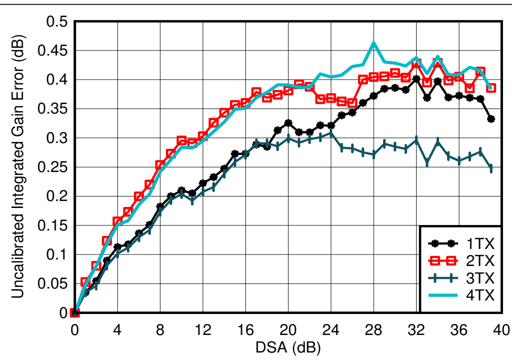
図 7-120. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

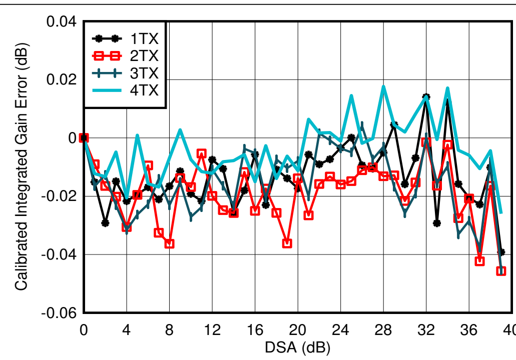
図 7-121. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-122. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz



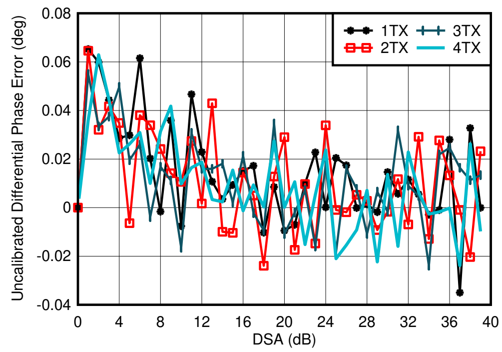
3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-123. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

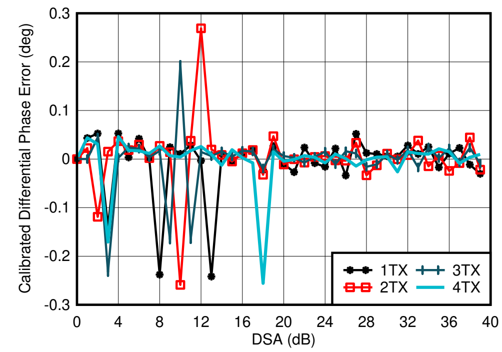
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



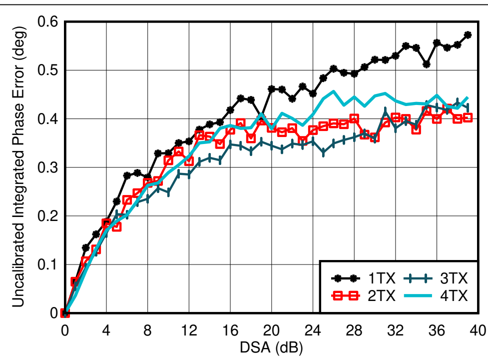
3.5 GHz Matching, included PCB and cable losses

図 7-124. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



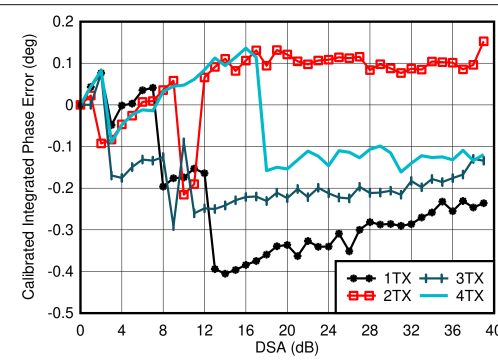
3.5 GHz Matching, included PCB and cable losses
Phase DNL spike may occur at any DSA setting.

図 7-125. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



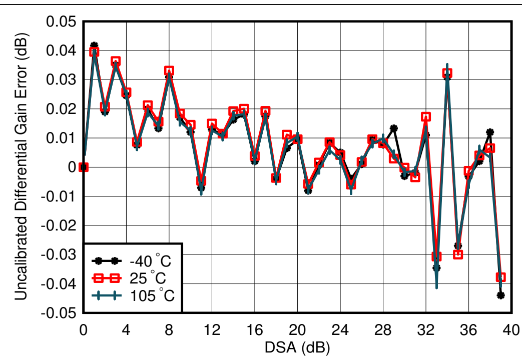
3.5 GHz Matching, included PCB and cable losses

図 7-126. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



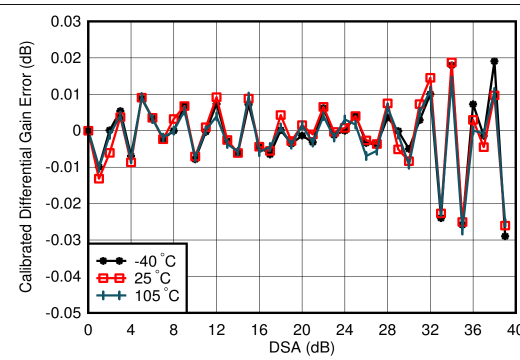
3.5 GHz Matching, included PCB and cable losses

図 7-127. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, 1TX

図 7-128. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

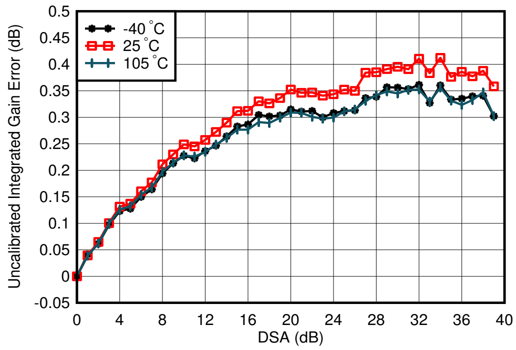


3.5 GHz Matching, 1TX, Calibrated at 25°C

図 7-129. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

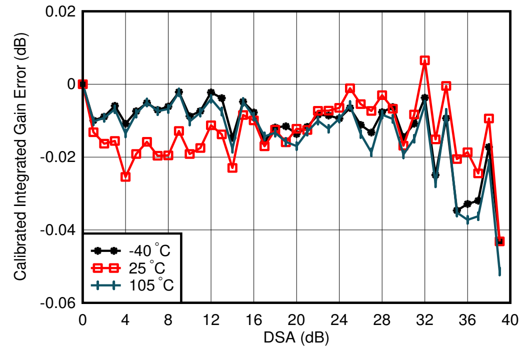
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



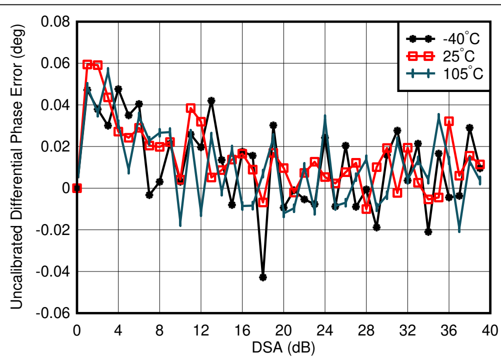
3.5 GHz Matching, 1TX

図 7-130. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

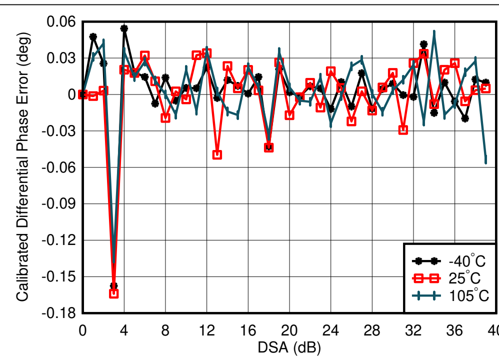
図 7-131. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

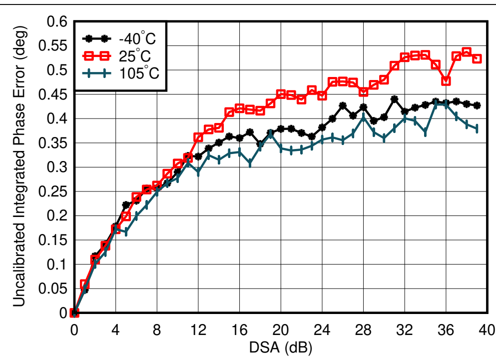
図 7-132. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

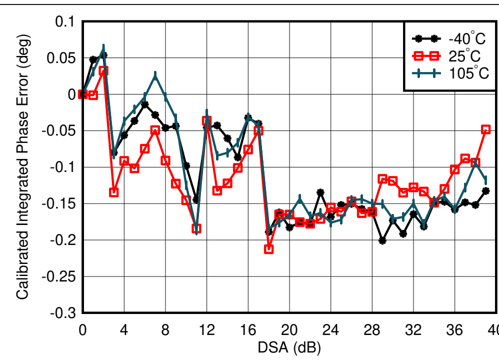
図 7-133. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

図 7-134. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



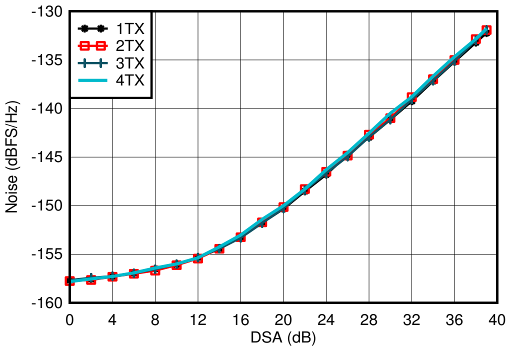
3.5 GHz Matching, 1TX, Calibrated at 25°C

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-135. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz

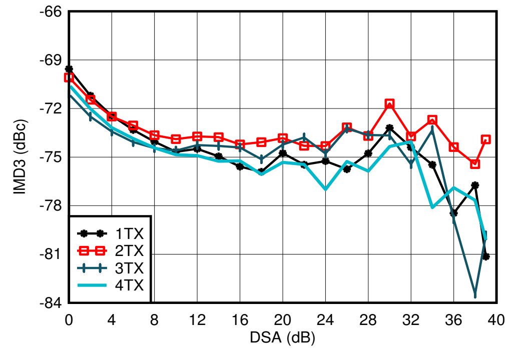
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



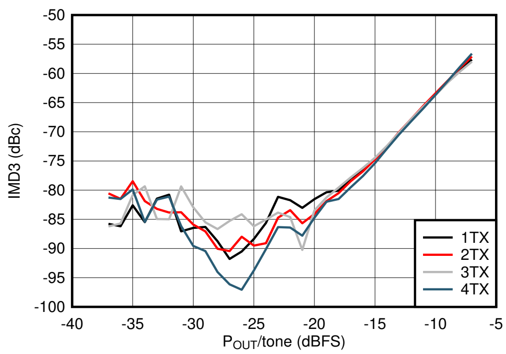
A. f_{DAC}=11796.48MSPS, interleave mode, matching at 3.5GHz, A_{out} = –13 dBFS.

図 7-136. TX NSD vs DSA Setting at 3.5 GHz



20-MHz tone spacing, 3.5 GHz Matching, –13 dBFS each tone, included PCB and cable losses

図 7-137. TX IMD3 vs DSA Setting at 3.5 GHz

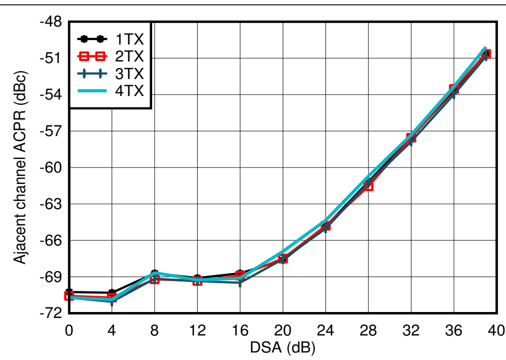


20-MHz tone spacing, 3.5 GHz Matching

図 7-138. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz

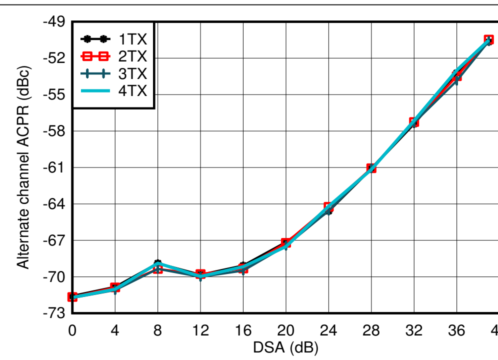
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 7-139. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 7-140. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz

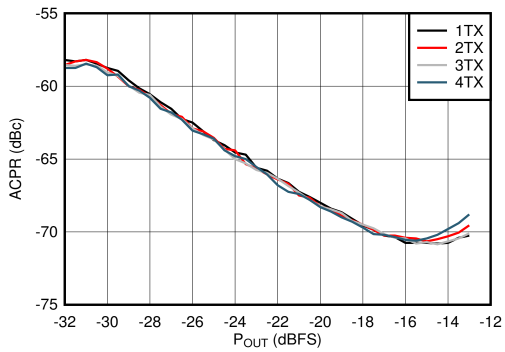


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 7-141. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz

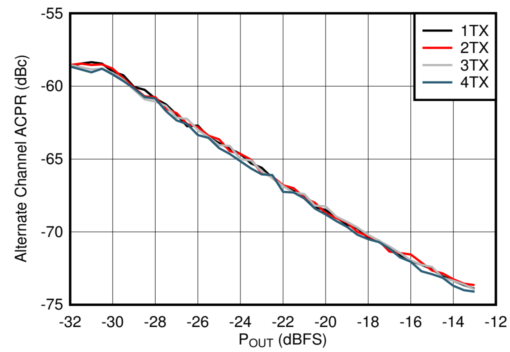
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



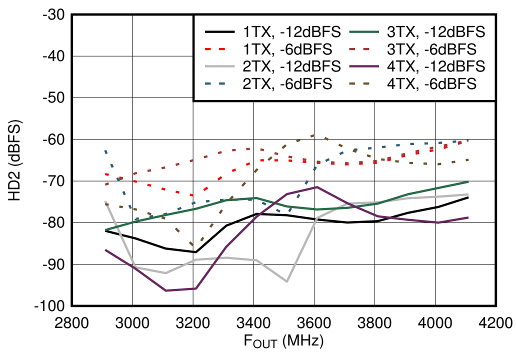
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 7-142. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



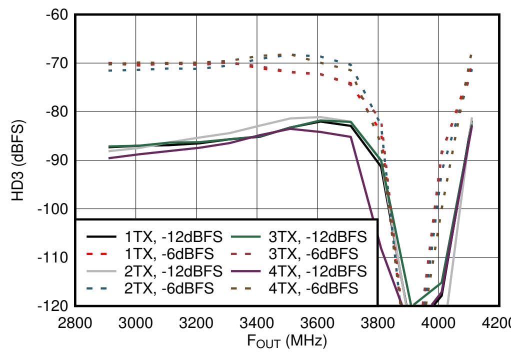
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 7-143. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



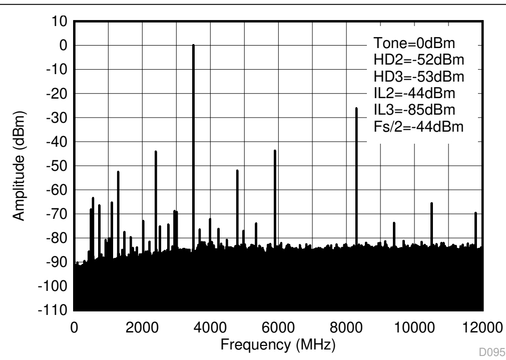
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 7-144. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



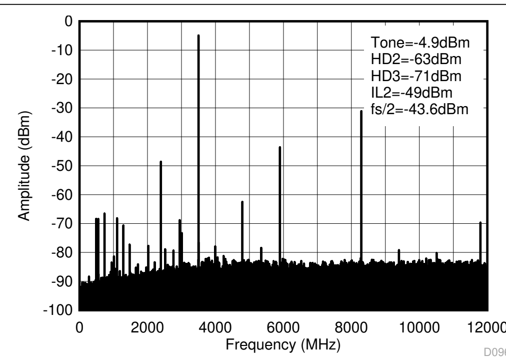
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

図 7-145. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 7-146. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})

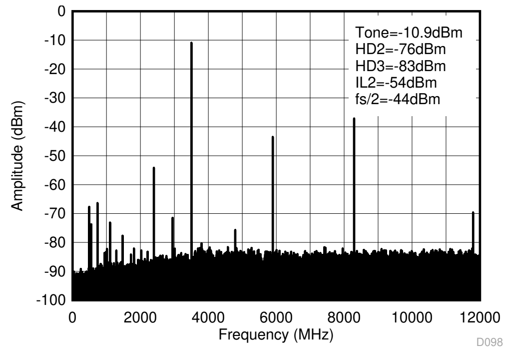


Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 7-147. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})

7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled

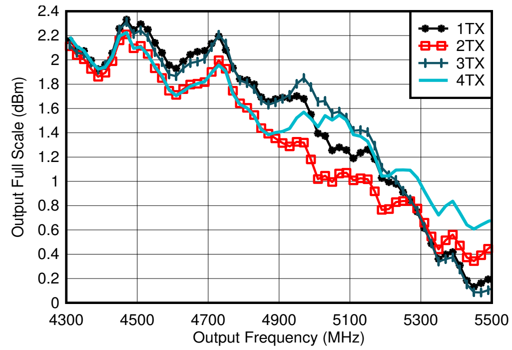


Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 7-148. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})

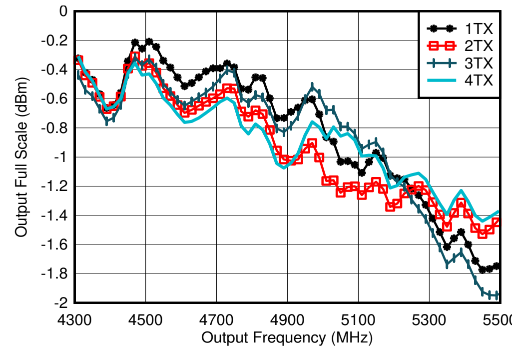
7.12.5 TX Typical Characteristics at 4.9 GHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



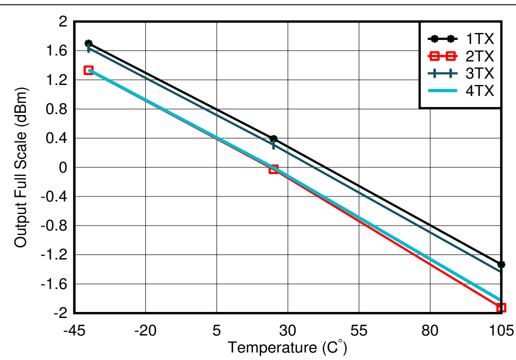
Excluding PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 4.9 GHz matching

図 7-149. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS



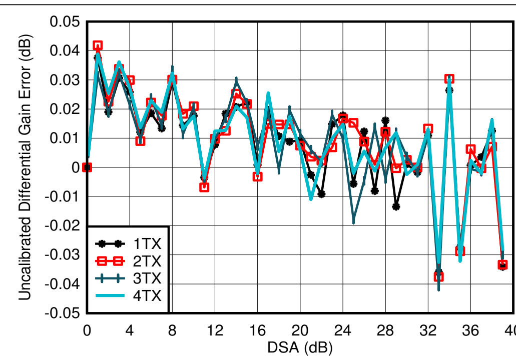
Excluding PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 4.9 GHz matching

図 7-150. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Straight Mode, 2nd Nyquist Zone



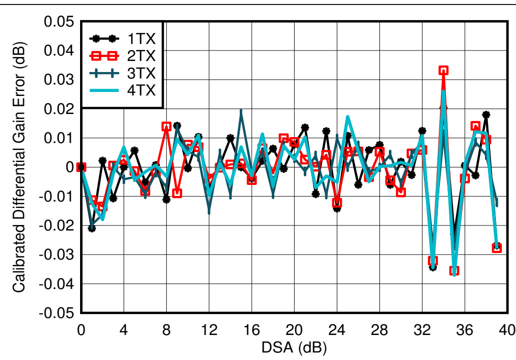
f_{DAC} = 11796.48 MSPS, A_{out} = -0.5 dFBS, matching 4.9 GHz

図 7-151. TX Output Power vs DSA Setting and Channel at 4.9 GHz



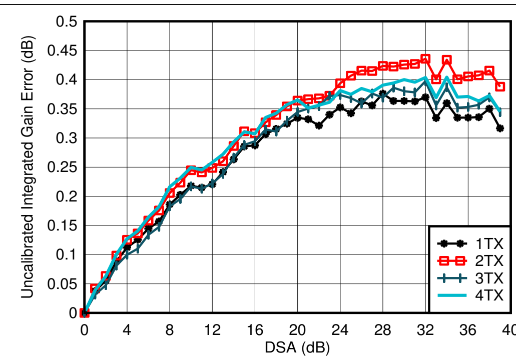
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-152. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-153. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

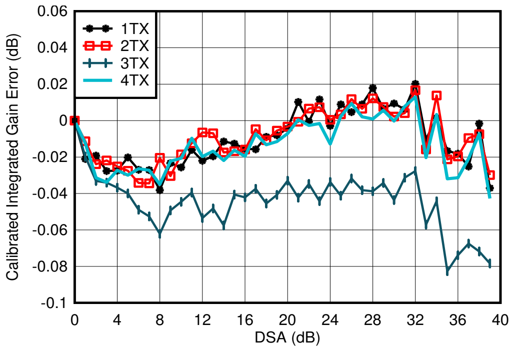


f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-154. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz

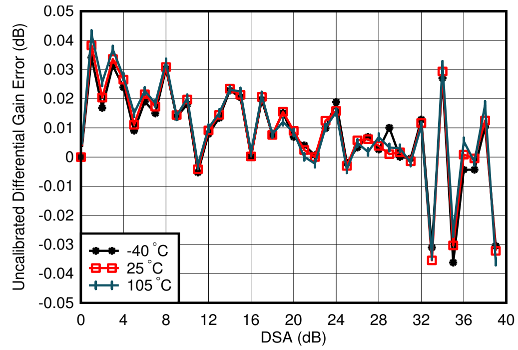
7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



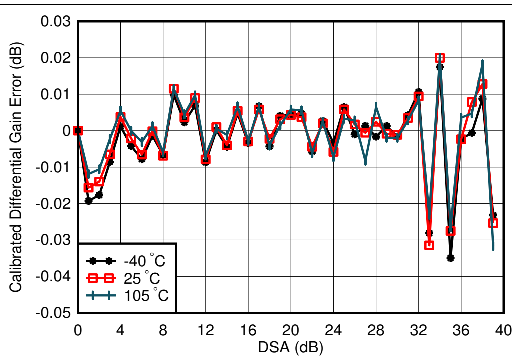
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-155. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



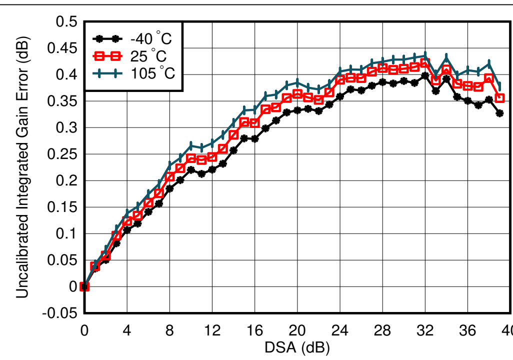
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-156. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 7-157. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

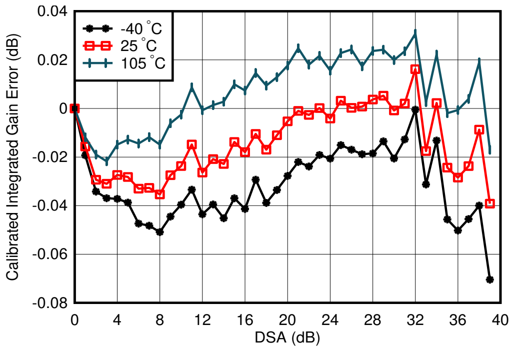


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-158. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz

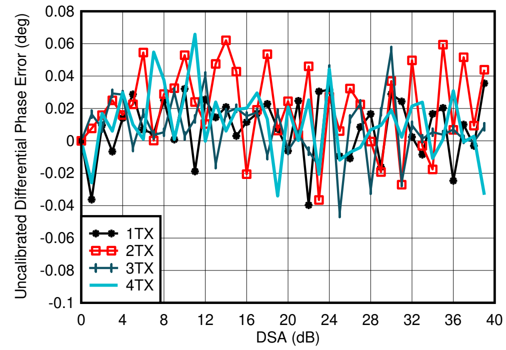
7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



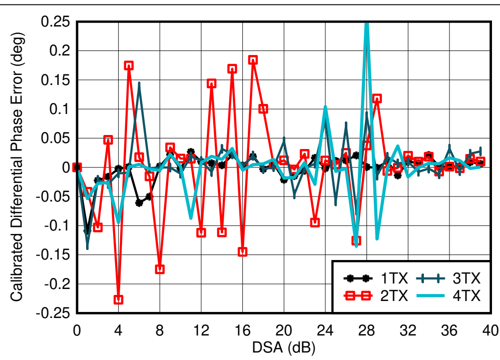
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 7-159. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



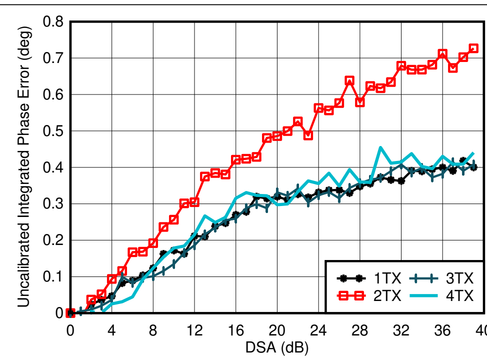
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-160. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 7-161. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

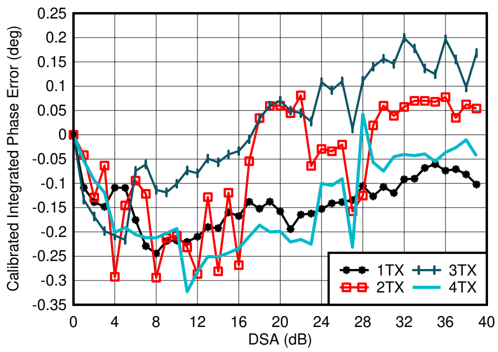


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-162. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz

7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

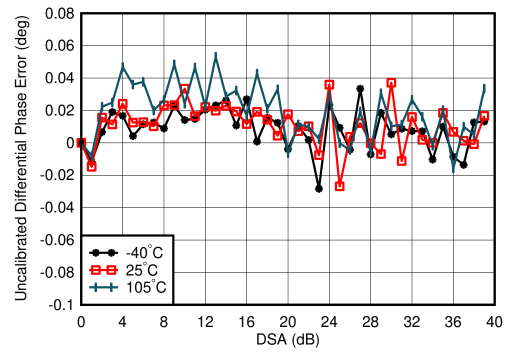
Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

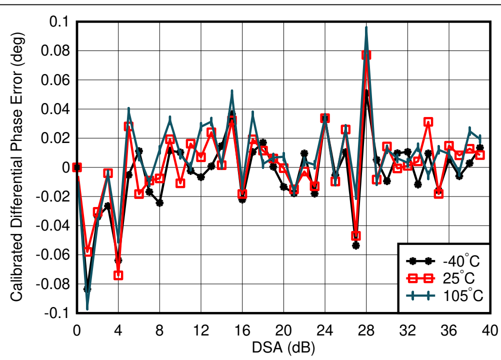
図 7-163. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

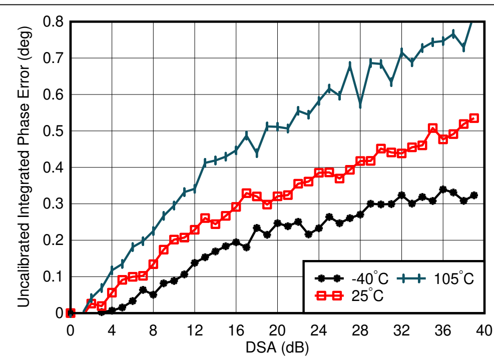
図 7-164. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 7-165. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



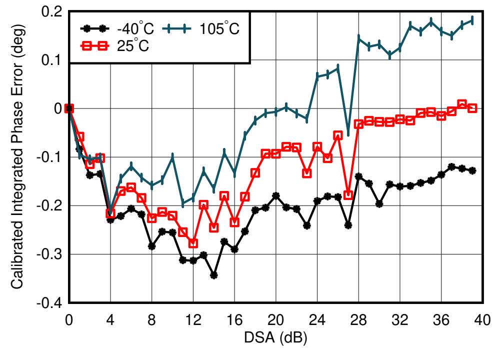
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-166. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz

7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

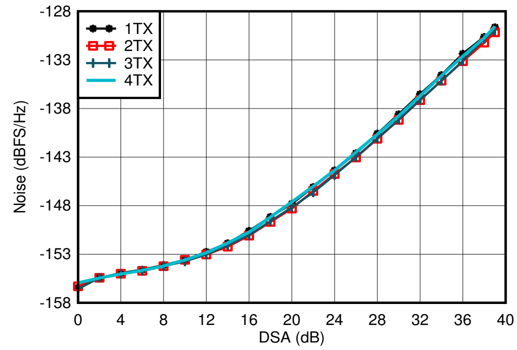
Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, channel with the median variation over DSA setting at 25°C

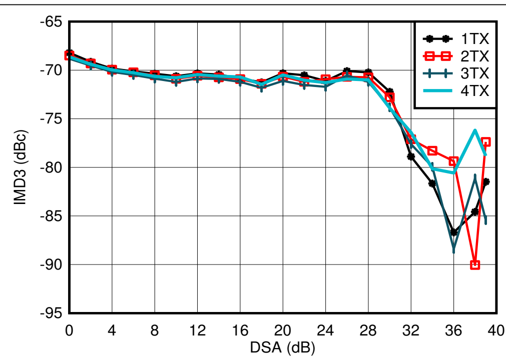
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-167. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



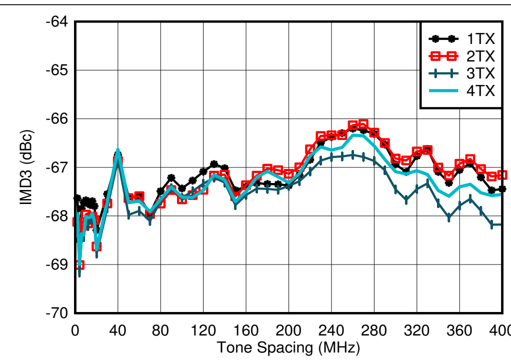
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, P_{OUT} = –13 dBFS

図 7-168. TX Output Noise vs Channel and Attenuation at 2.6 GHz



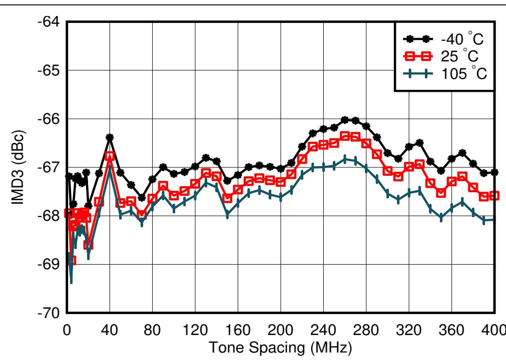
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, -13 dBFS each tone

図 7-169. TX IMD3 vs DSA Setting at 4.9 GHz



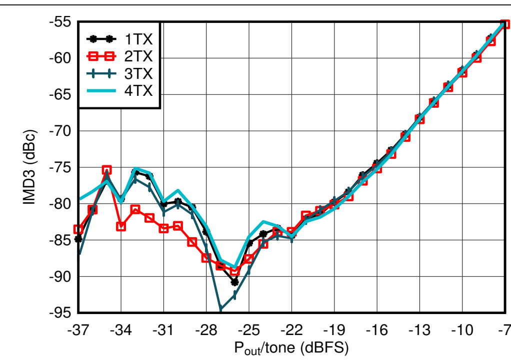
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, –13 dBFS each tone

図 7-170. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, –13 dBFS each tone, worst channel

図 7-171. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz

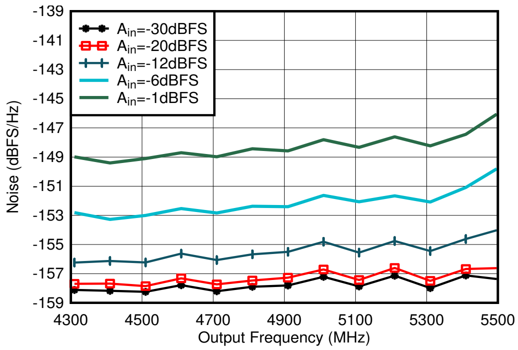


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, $f_{SPACING}$ = 20 MHz

図 7-172. TX IMD3 vs Digital Level at 4.9 GHz

7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled

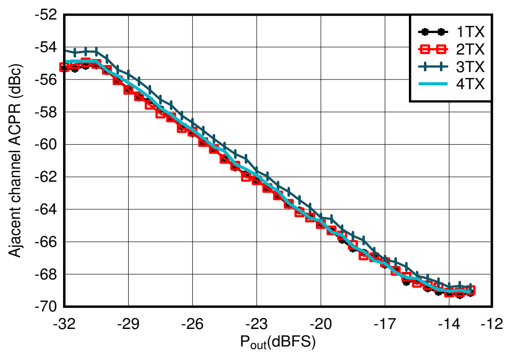


Matching at 4.9 GHz, Single tone, f_{DAC} = 11.7964 8GSPS, interleave mode, 40-MHz offset, DSA=0dB

図 7-173. TX Single Tone Output Noise vs Frequency and Amplitude at 4.9 GHz

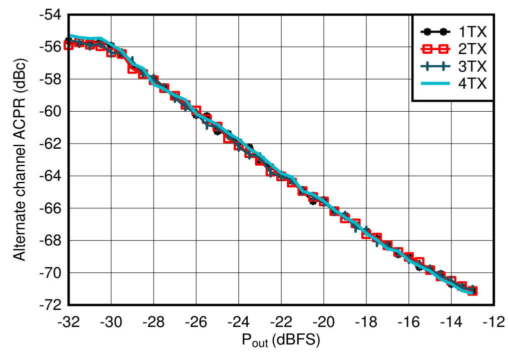
TM1.1, P_{OUT_RMS} = –13 dBFS

図 7-174. TX 20-MHz LTE Output Spectrum at 4.9 GHz



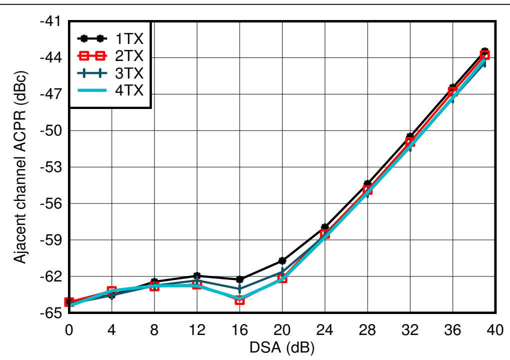
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-175. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



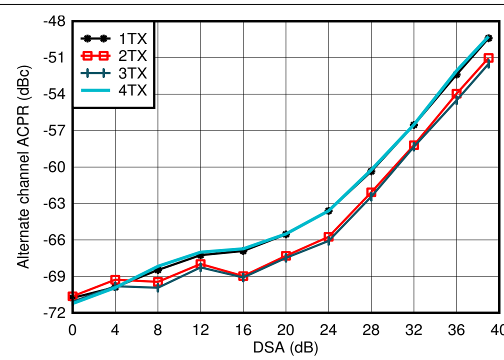
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-176. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-177. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz

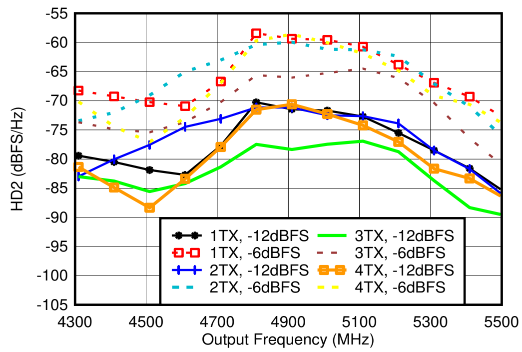


Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 7-178. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz

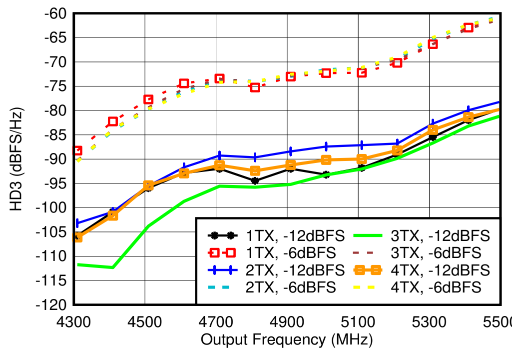
7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



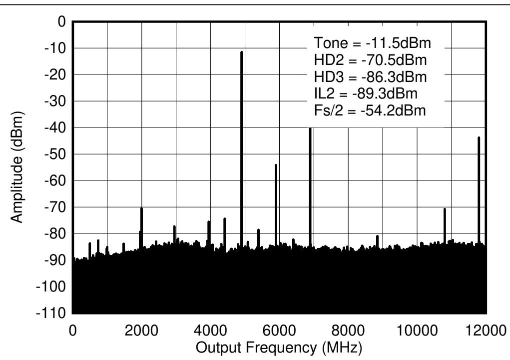
Matching at 4.9 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

図 7-179. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz



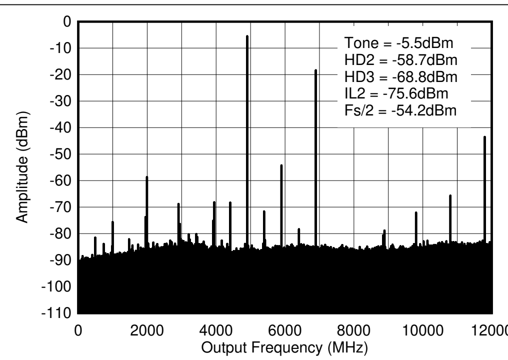
Matching at 4.9 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

図 7-180. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz



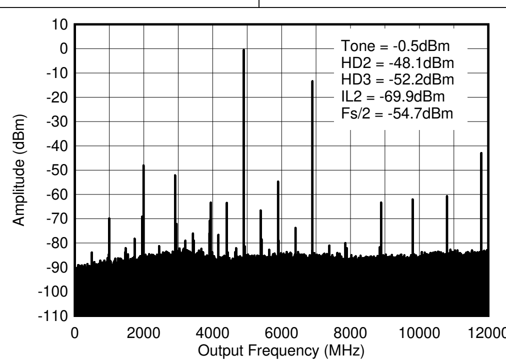
f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 7-181. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 7-182. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})

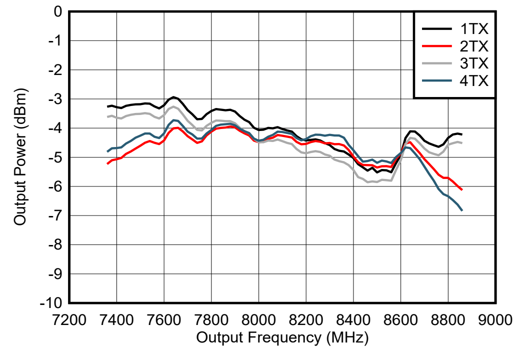


f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 7-183. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})

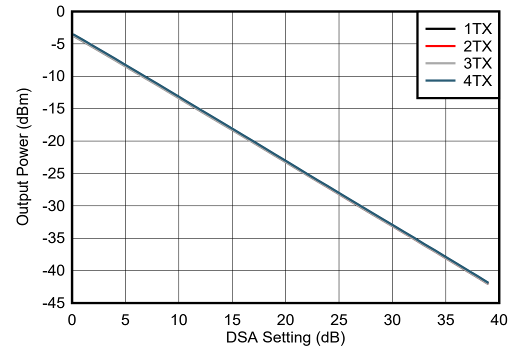
7.12.6 TX Typical Characteristics at 8.1 GHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



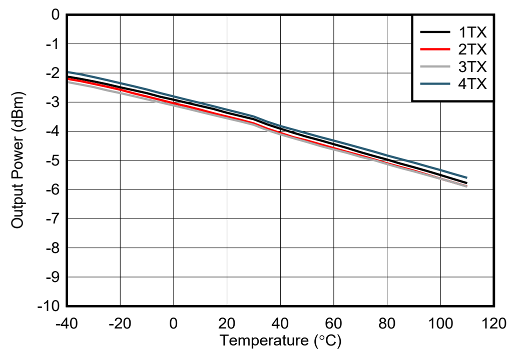
includes PCB and cable losses.

図 7-184. TX Output Power vs Frequency at 8.11 GHz



includes PCB and cable losses.

図 7-185. TX Output Power vs DSA Setting at 8.11 GHz



includes PCB and cable losses.

図 7-186. TX Output Power vs Temperature at 8.11 GHz

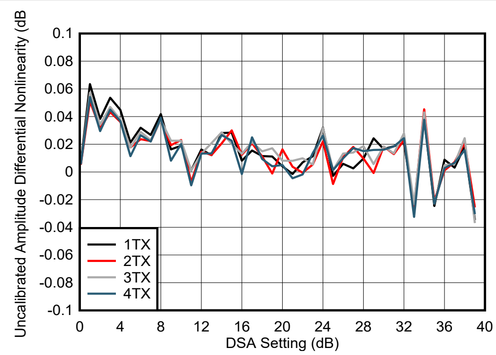


図 7-187. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz

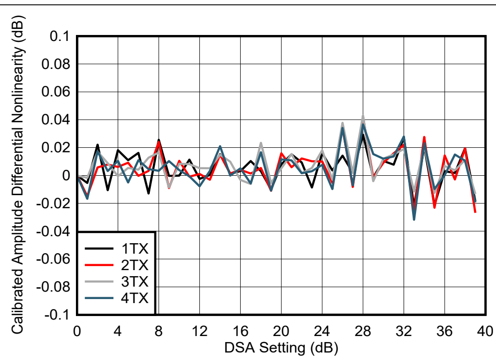


図 7-188. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

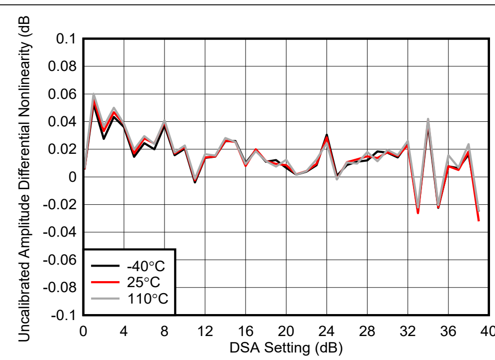


図 7-189. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

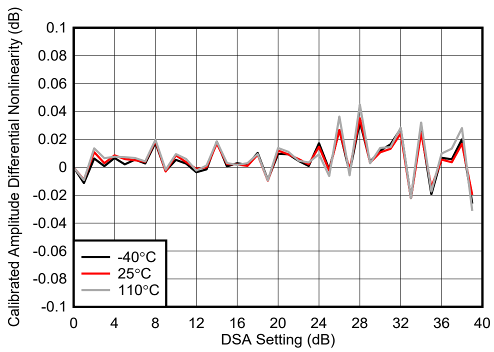


図 7-190. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

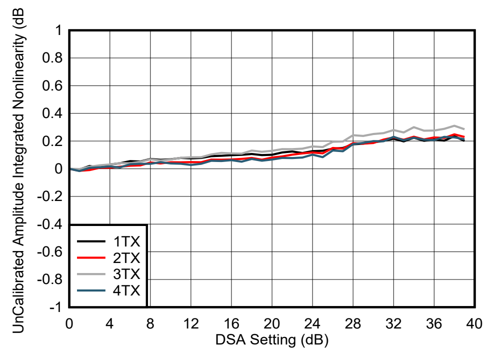


図 7-191. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

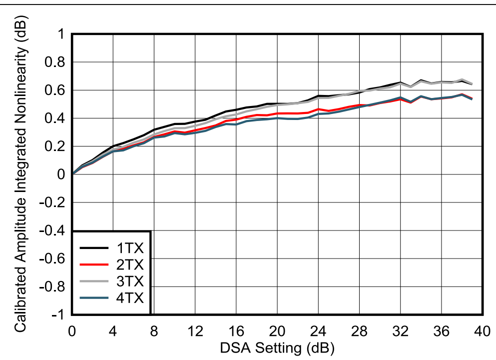


図 7-192. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

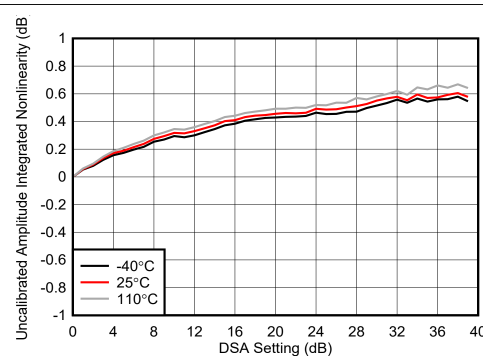


図 7-193. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

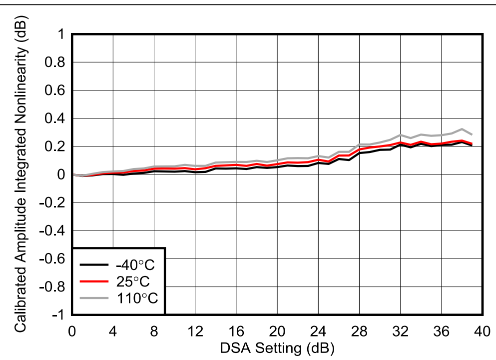


図 7-194. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

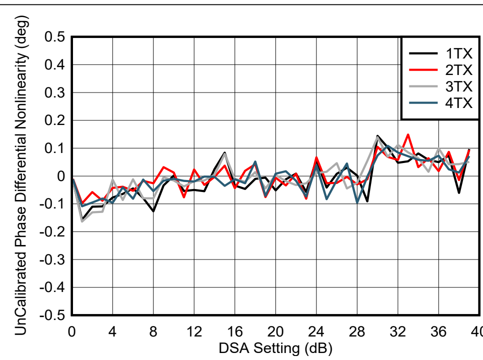


図 7-195. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

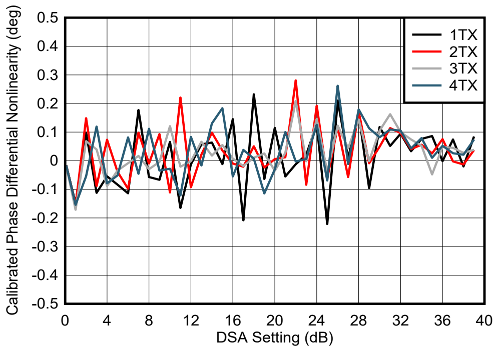


図 7-196. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

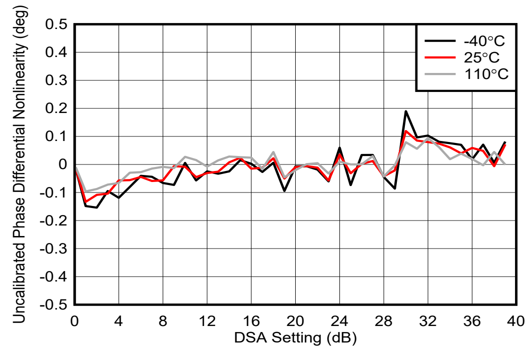


図 7-197. TX DSA Uncalibrated Phase Differntial Nonlinearity at 8.11 GHz

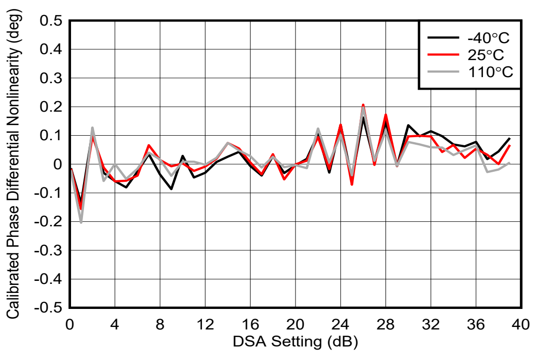


図 7-198. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

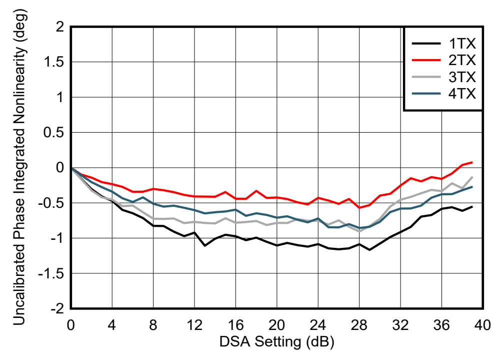


図 7-199. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz

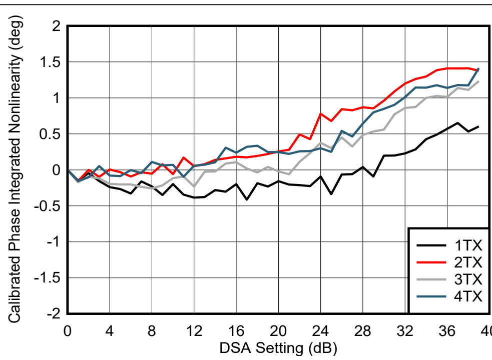


図 7-200. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz

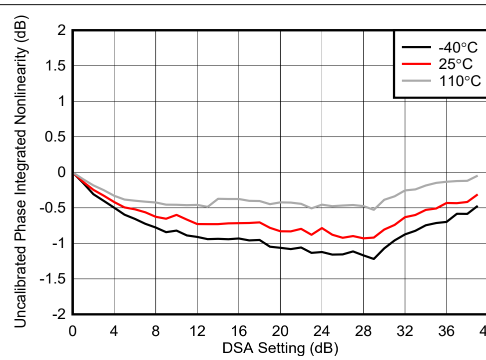


図 7-201. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

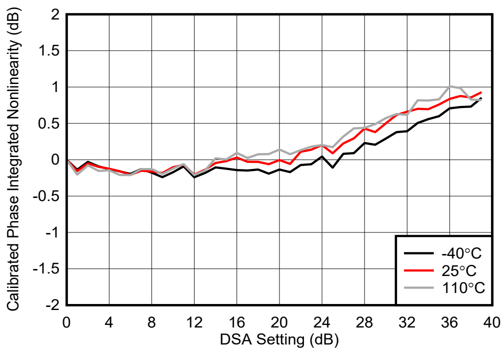
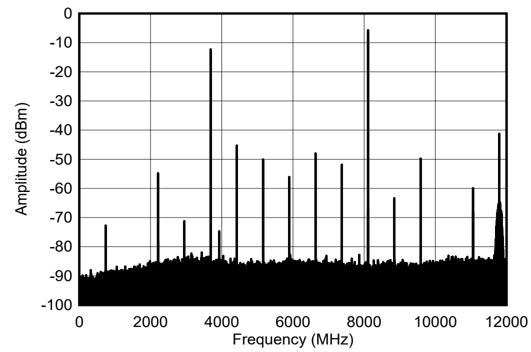
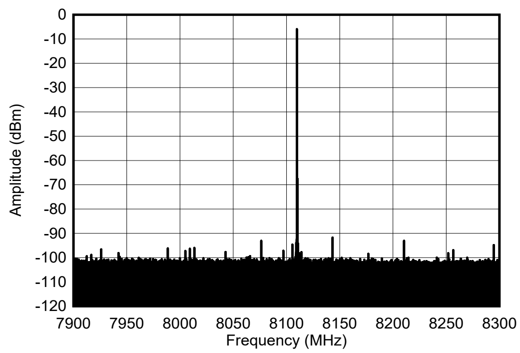


図 7-202. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz



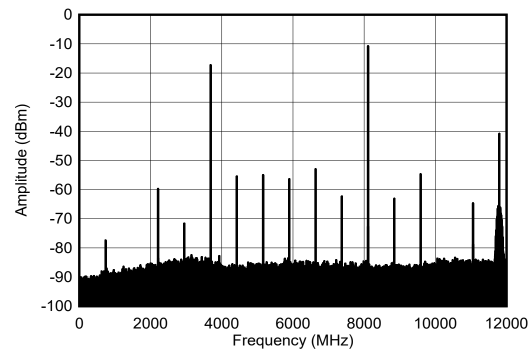
-1 dBFS

図 7-203. TX Single Tone Output Spectrum at 8.11 GHz



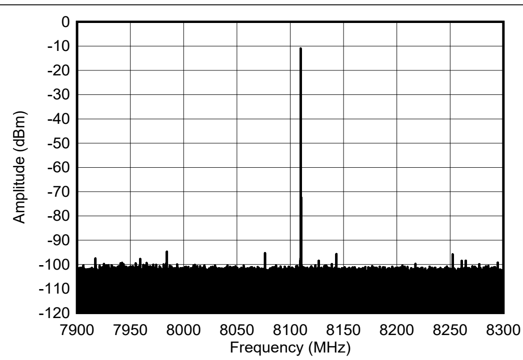
-1 dBFS

図 7-204. TX Single Tone Output Spectrum at 8.11 GHz



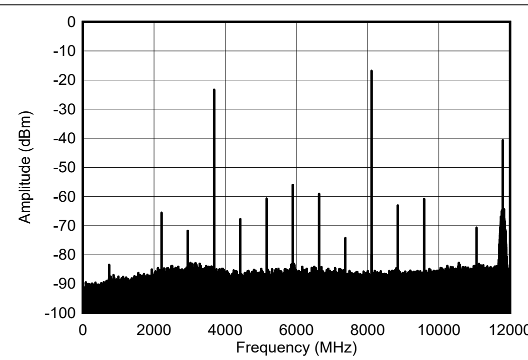
-6 dBFS

図 7-205. TX Single Tone Output Spectrum at 8.11 GHz



-6 dBFS

図 7-206. TX Single Tone Output Spectrum at 8.11 GHz

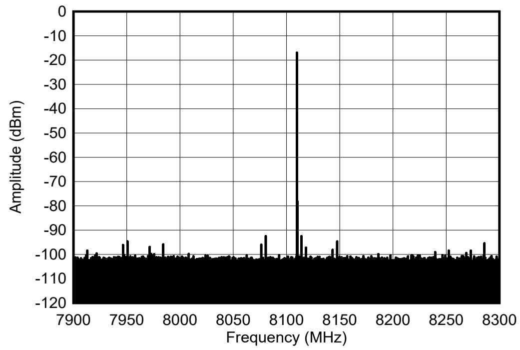


-12 dBFS

図 7-207. TX Single Tone Output Spectrum at 8.11 GHz

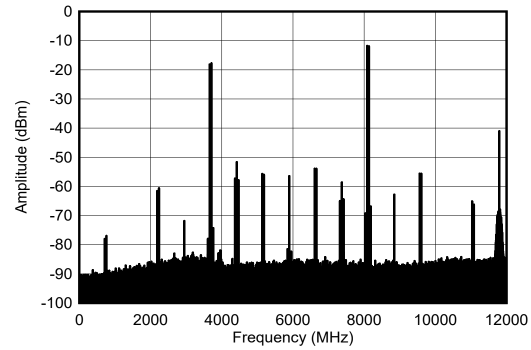
7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



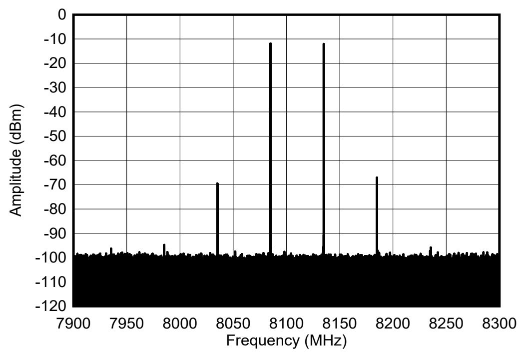
-12 dBFS

図 7-208. TX Single Tone Output Spectrum at 8.11 GHz



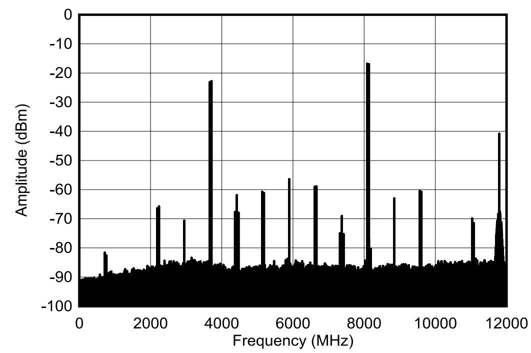
50 MHz tone spacing, -7 dBFS each tone

図 7-209. TX Dual Tone Output Spectrum at 8.11 GHz



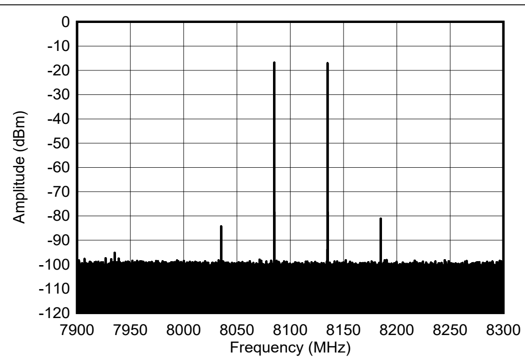
50 MHz tone spacing, -7d BFS each tone

図 7-210. TX Dual Tone Output Spectrum at 8.11 GHz



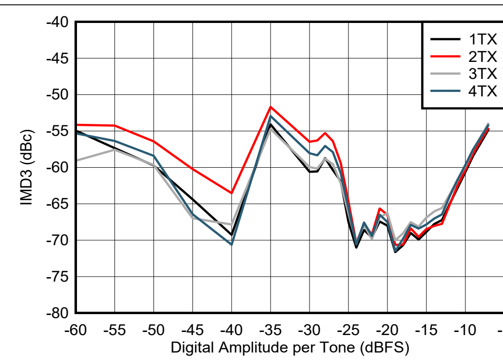
50 MHz tone spacing, -12 dBFS each tone

図 7-211. TX Dual Tone Output Spectrum at 8.11 GHz



50MHz tone spacing, -12dBFS each tone

図 7-212. TX Dual Tone Output Spectrum at 8.11 GHz

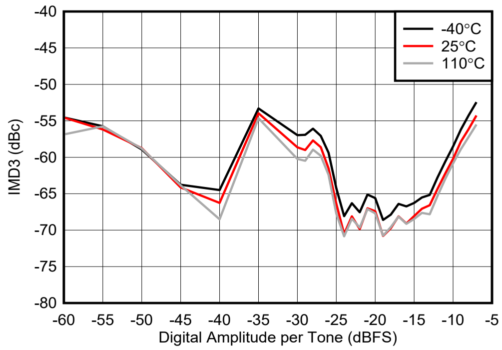


-7 dBFS each tone, 50 MHz tone spacing

図 7-213. TX IMD3 vs Digital Amplitude at 8.11 GHz

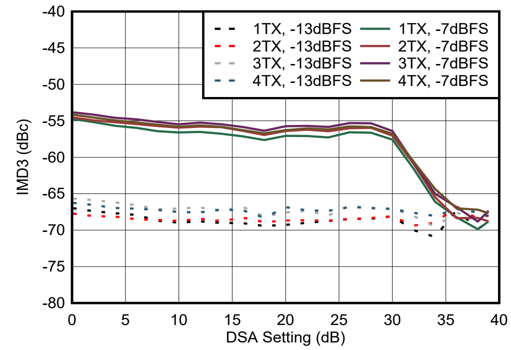
7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



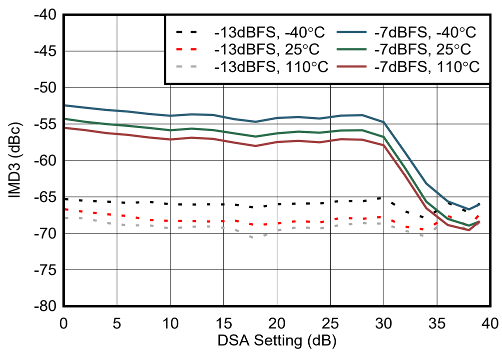
-7 dBFS each tone, 50 MHz tone spacing

図 7-214. TX IMD3 vs Digital Amplitude at 8.11 GHz



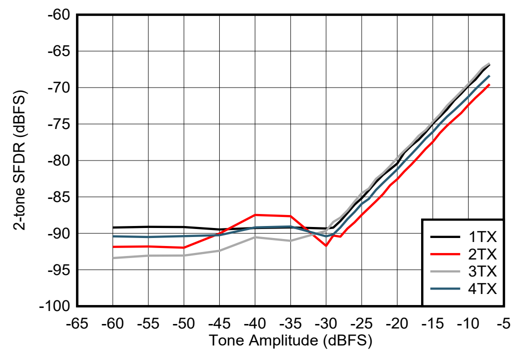
50 MHz tone spacing

図 7-215. TX IMD3 vs DSA Setting at 8.11 GHz



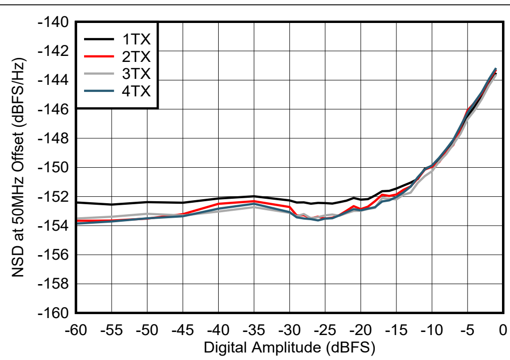
50 MHz tone spacing

図 7-216. TX IMD3 vs DSA Setting at 8.11 GHz



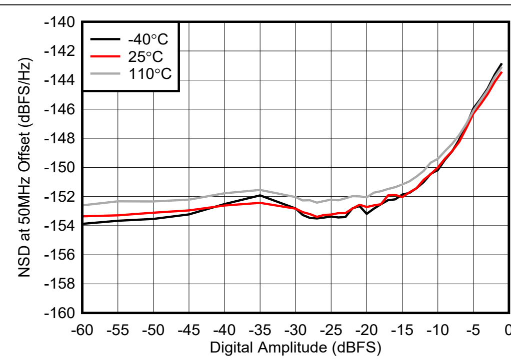
50 MHz tone spacing

図 7-217. TX 2-Tone SFDR vs Digital Amplitude at 8.11 GHz



50 MHz offset

図 7-218. TX NSD vs Digital Amplitude at 8.11 GHz

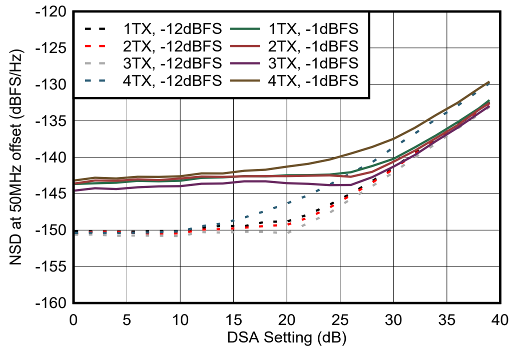


50 MHz offset

図 7-219. TX NSD vs Digital Amplitude at 8.11 GHz

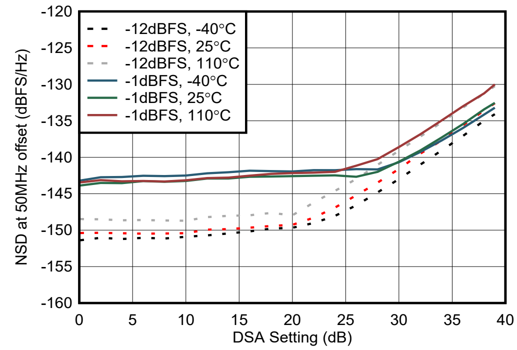
7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



50 MHz offset

図 7-220. TX NSD vs DSA Setting at 8.11 GHz



50 MHz offset

図 7-221. TX NSD vs DSA Setting at 8.11 GHz

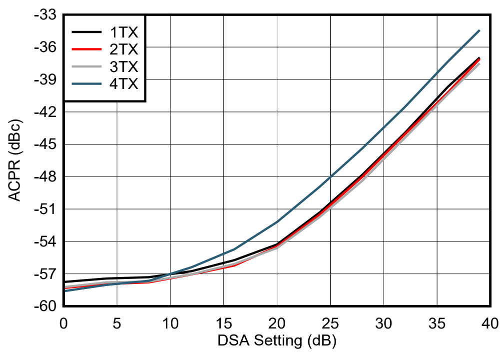


図 7-222. TX NR100MHz ACPR vs DSA Setting 8.11 GHz

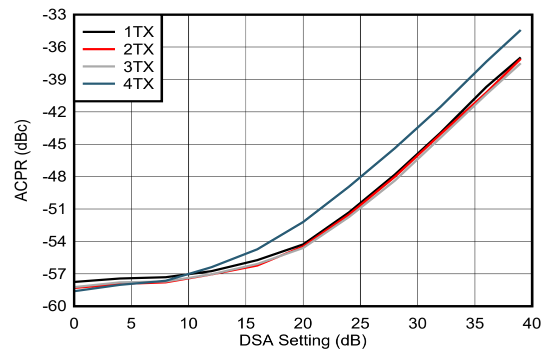


図 7-223. TX NR100MHz alt-ACPR vs DSA Setting 8.11 GHz

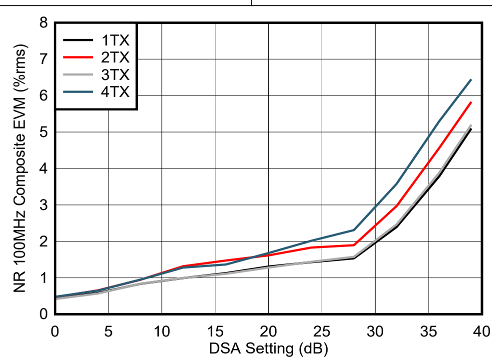
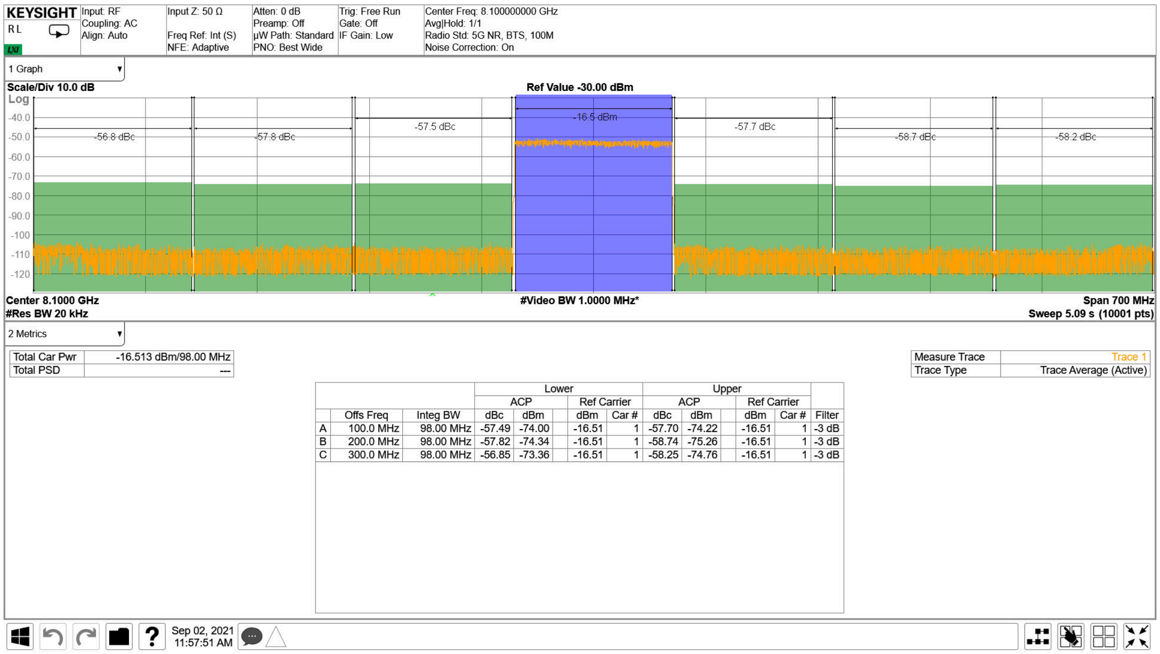


図 7-224. TX NR100MHz EVM vs DSA Setting 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



			Lower				Upper				
			ACP		Ref Carrier		ACP		Ref Carrier		
	Offs Freq	Integ BW	dBc	dBm	dBm	Car #	dBc	dBm	dBm	Car #	Filter
A	100.0 MHz	98.00 MHz	-57.49	-74.00	-16.51	1	-57.70	-74.22	-16.51	1	-3 dB
B	200.0 MHz	98.00 MHz	-57.82	-74.34	-16.51	1	-58.74	-75.26	-16.51	1	-3 dB
C	300.0 MHz	98.00 MHz	-56.85	-73.36	-16.51	1	-58.25	-74.76	-16.51	1	-3 dB

図 7-225. TX 100 MHz NR Output Spectrum at 8.11 GHz

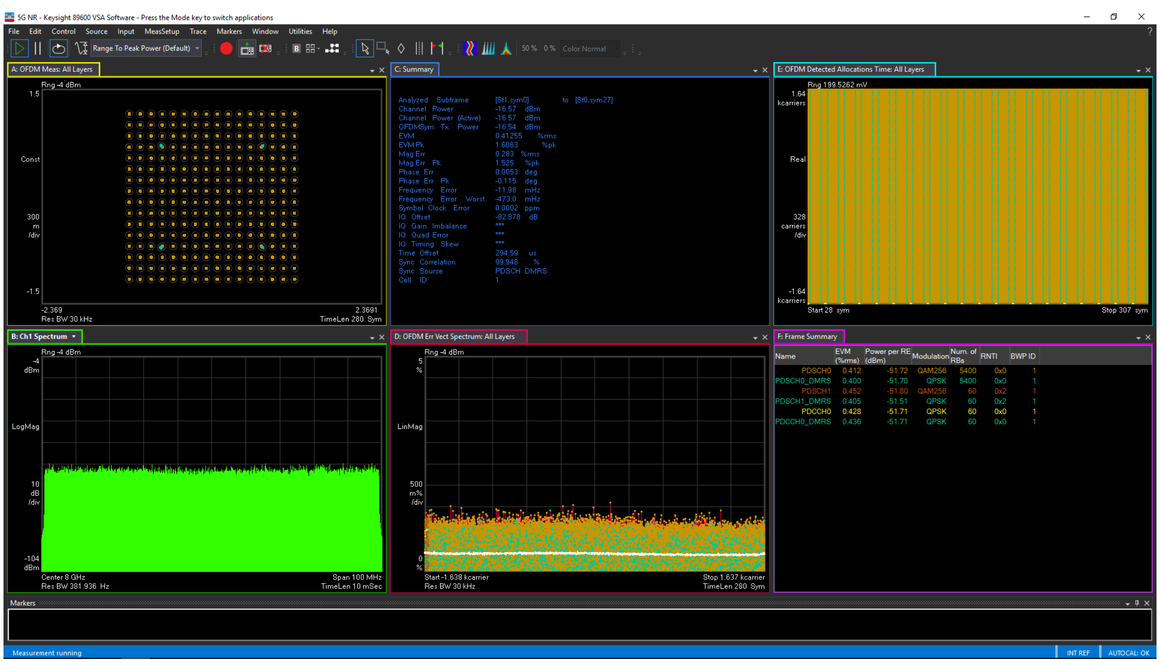


図 7-226. TX 100 MHz NR EVM at 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 491.52 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

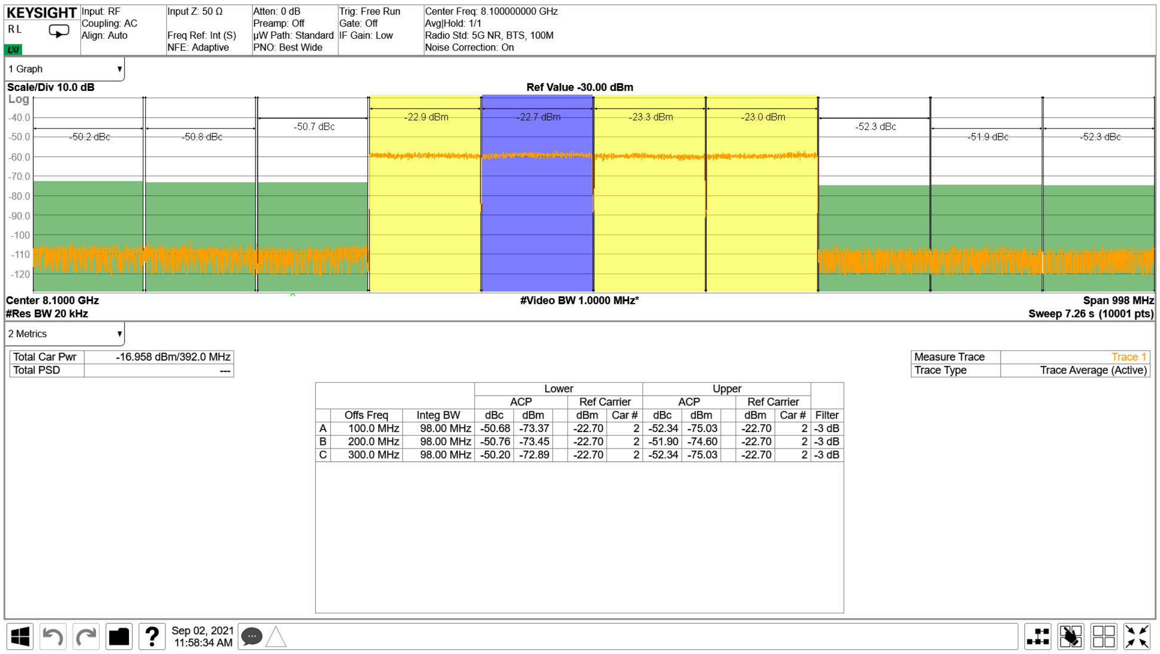


図 7-227. TX 4x100 MHz NR Output Spectrum 8.11 GHz

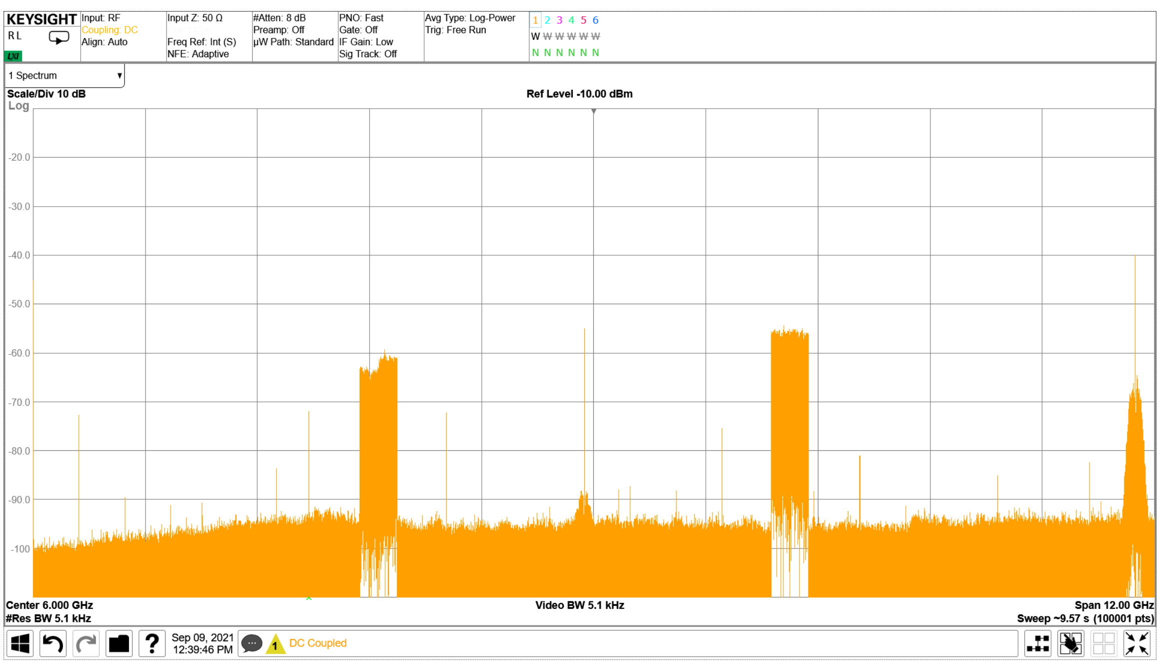
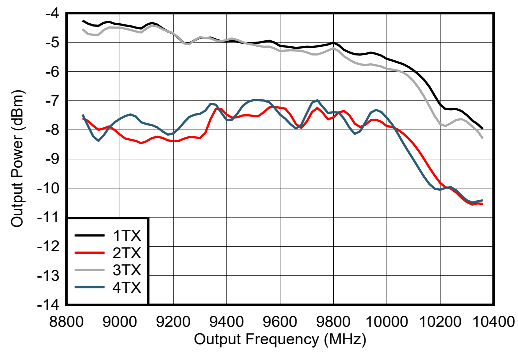


図 7-228. TX 4x100 MHz NR Output Spectrum 8.11 GHz

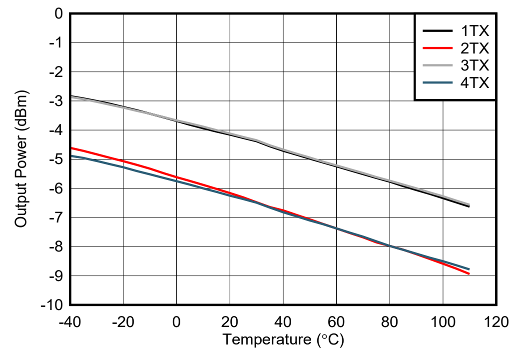
7.12.7 TX Typical Characteristics at 9.6 GHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



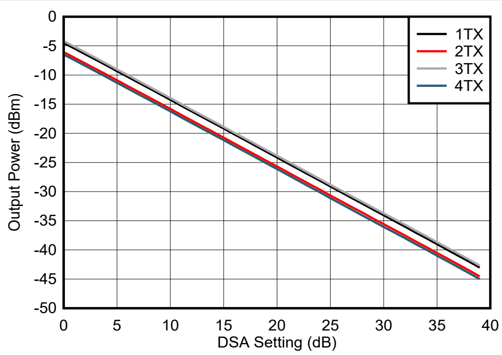
Includes PCB and cable losses.

図 7-229. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

図 7-230. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

図 7-231. TX Output Power vs DSA Setting at 9.6 1GHz

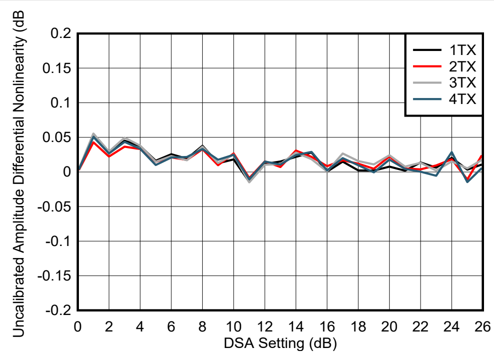


図 7-232. TX DSA Uncalibrated Amplitude Differential Nonlinearity

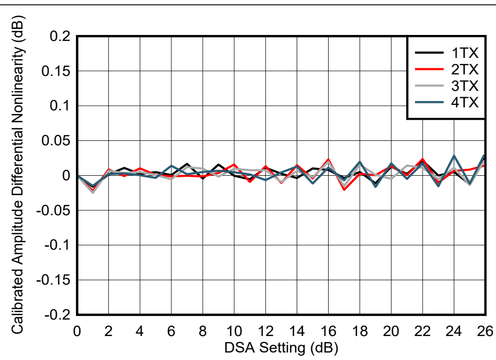


図 7-233. TX DSA Calibrated Amplitude Differential Nonlinearity

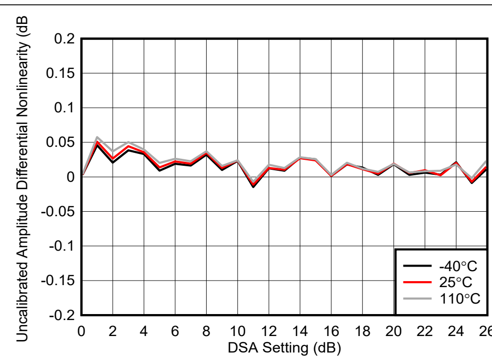


図 7-234. TX DSA Uncalibrated Amplitude Differential Nonlinearity

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

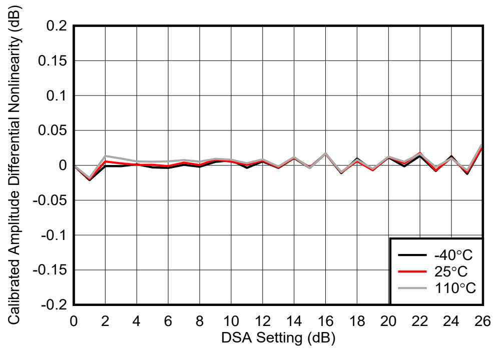


図 7-235. TX DSA Calibrated Amplitude Differential Nonlinearity

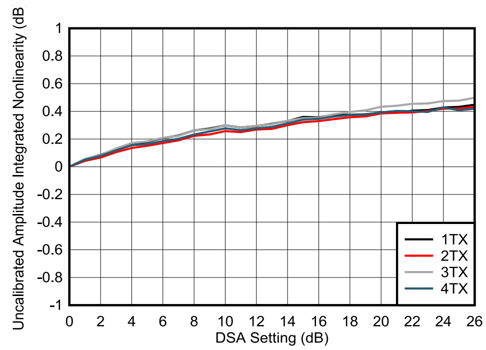


図 7-236. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

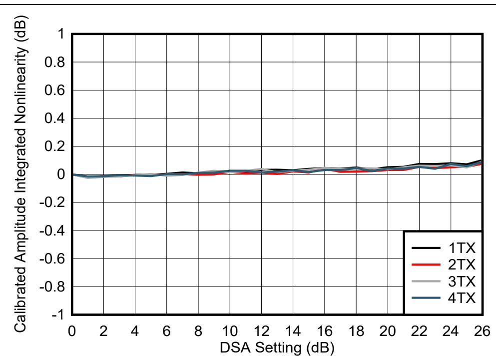


図 7-237. TX DSA Calibrated Amplitude Integrated Nonlinearity

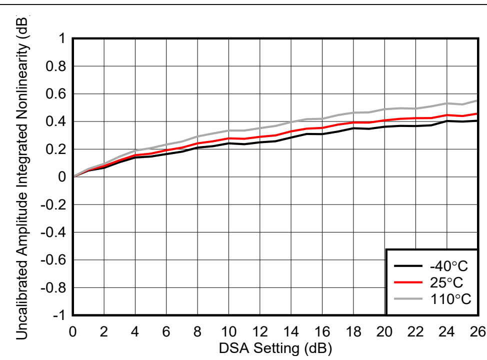


図 7-238. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

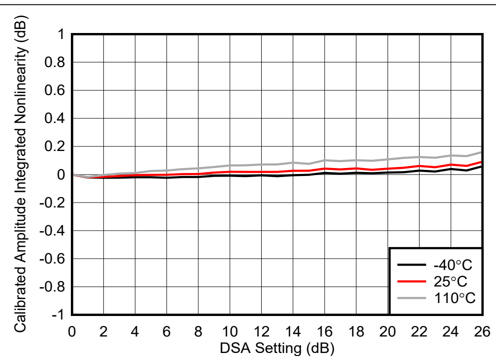


図 7-239. TX DSA Calibrated Amplitude Integrated Nonlinearity

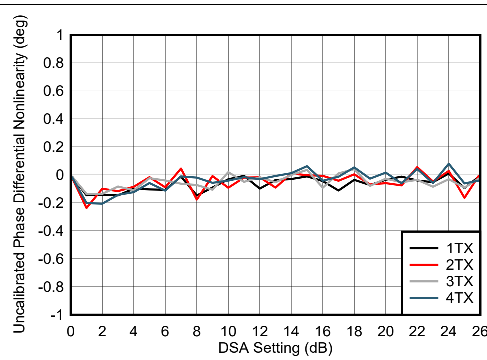


図 7-240. TX DSA Uncalibrated Phase Differential Nonlinearity

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

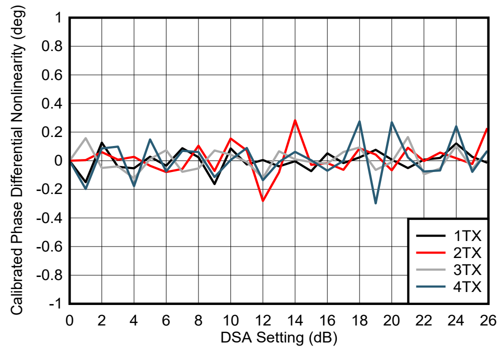


図 7-241. TX DSA Calibrated Phase Differential Nonlinearity

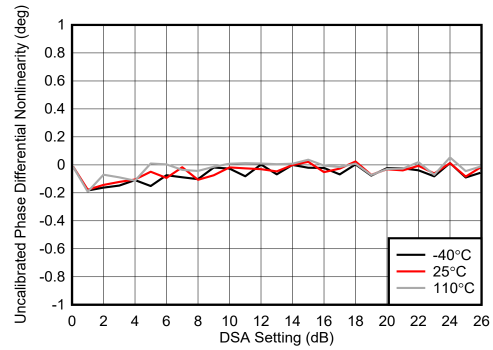


図 7-242. TX DSA Uncalibrated Phase Differential Nonlinearity

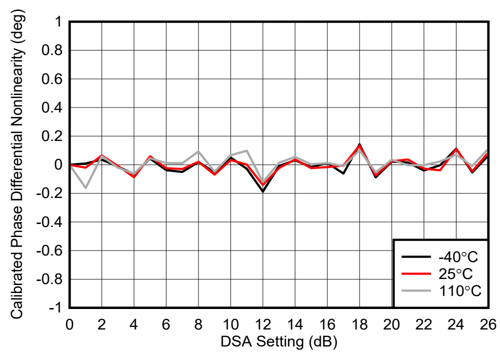


図 7-243. TX DSA Calibrated Phase Differential Nonlinearity

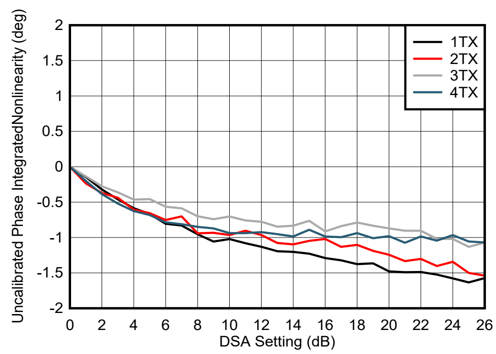


図 7-244. TX DSA Uncalibrated Phase Integrated Nonlinearity

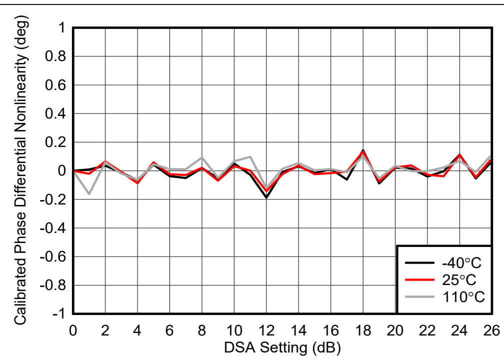


図 7-245. TX DSA Calibrated Phase Integrated Nonlinearity

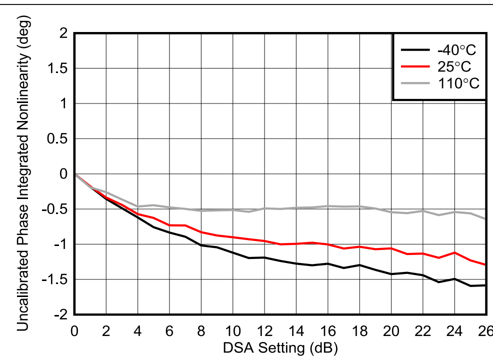


図 7-246. TX DSA Uncalibrated Phase Integrated Nonlinearity

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

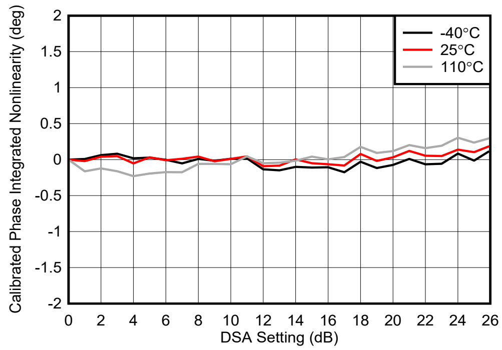
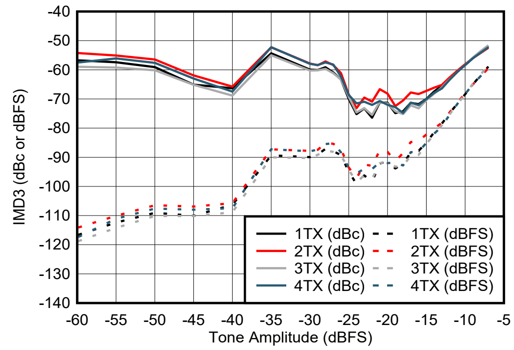
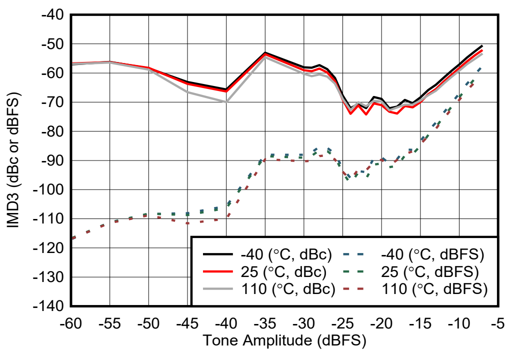


図 7-247. TX DSA Calibrated Amplitude Integrated Nonlinearity



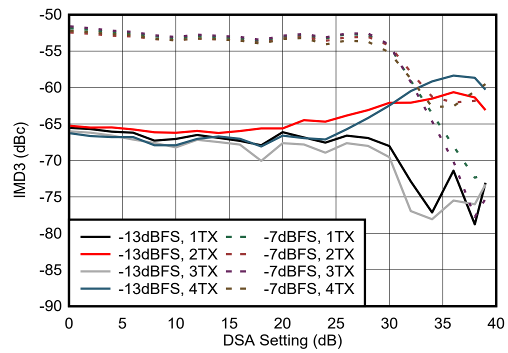
50 MHz tone spacing

図 7-248. TX IMD3 vs Digital Amplitude at 9.61 GHz



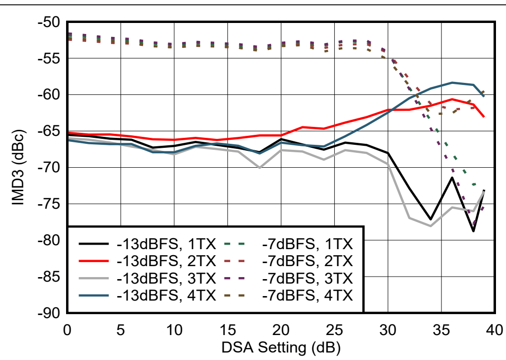
50 MHz tone spacing

図 7-249. TX IMD3 vs Digital Amplitude at 9.61 GHz



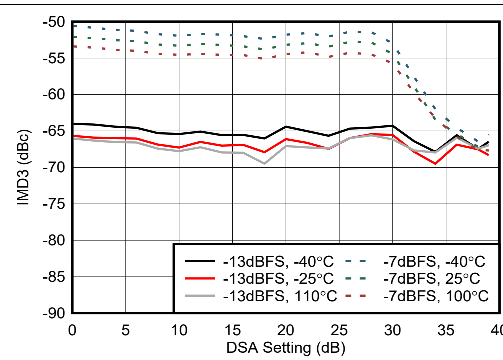
50 MHz tone spacing

図 7-250. TX IMD3 vs DSA Setting at 9.61 GHz



50 MHz tone spacing

図 7-251. TX IMD3 vs DSA Setting at 9.61 GHz



50 MHz tone spacing

図 7-252. TX IMD3 vs DSA Setting at 9.61 GHz

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

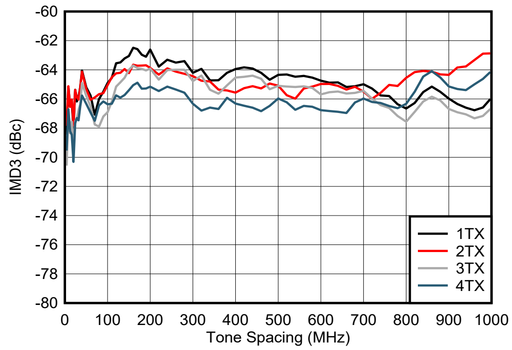


図 7-253. TX IMD3 vs Tone Spacing at 9.61 GHz

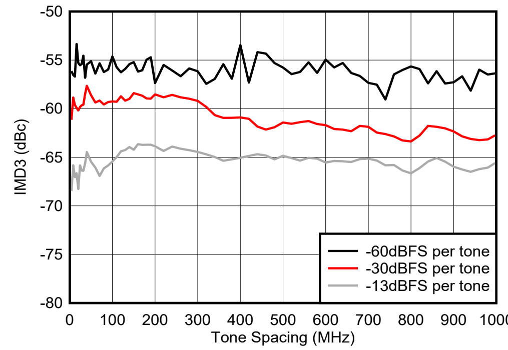


図 7-254. TX IMD3 vs Tone Spacing at 9.61 GHz

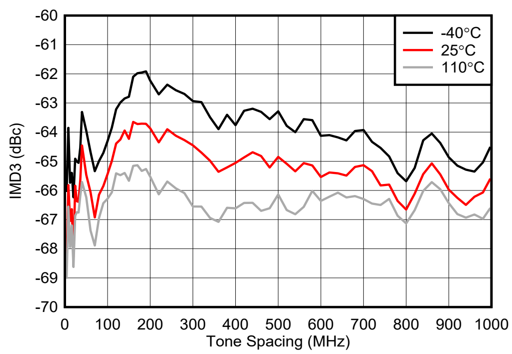


図 7-255. TX IMD3 vs Tone Spacing at 9.61 GHz

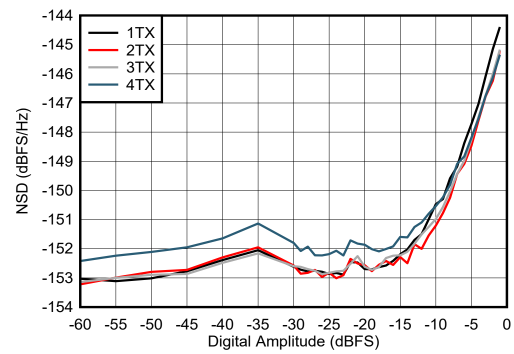


図 7-256. TX NSD vs Digital Amplitude at 9.61 GHz

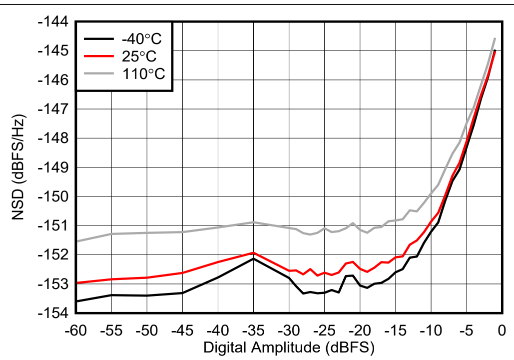


図 7-257. TX NSD vs Digital Amplitude at 9.61 GHz

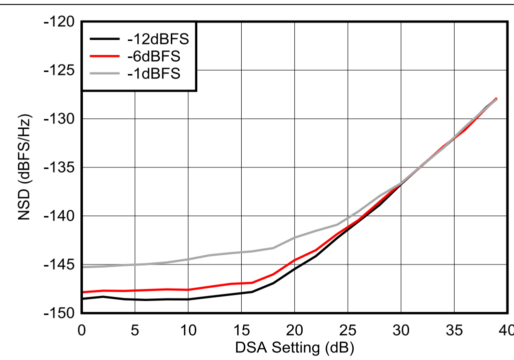


図 7-258. TX NSD vs DSA Setting at 9.61 GHz

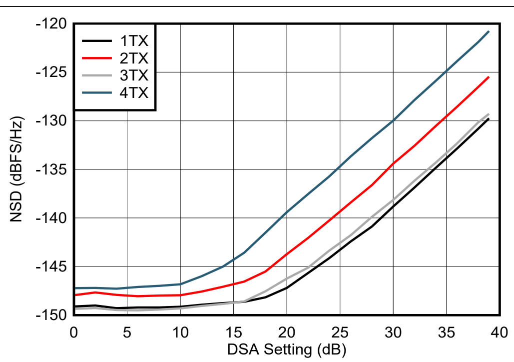


図 7-259. TX NSD vs DSA Setting at 9.61 GHz

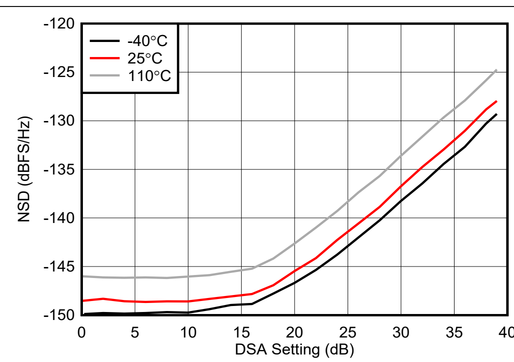
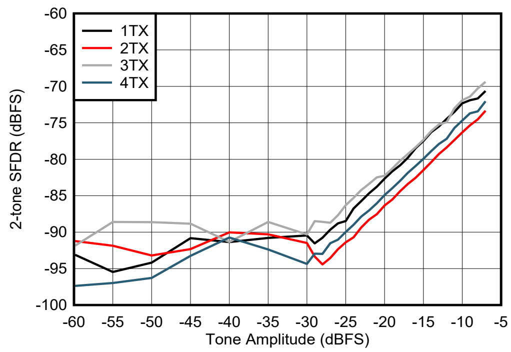


図 7-260. TX NSD vs DSA Setting at 9.61 GHz

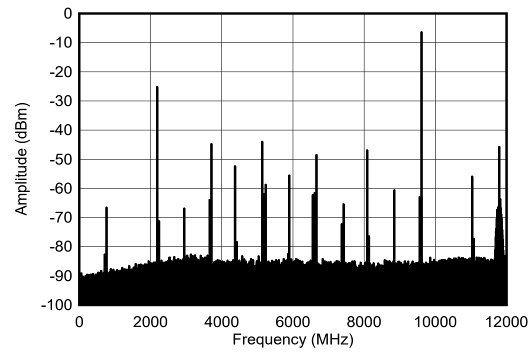
7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



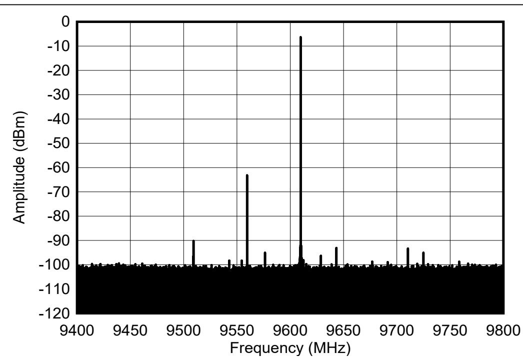
50MHz tone spacing

図 7-261. TX 2-tone SFDR vs Digital Amplitude at 9.61 GHz



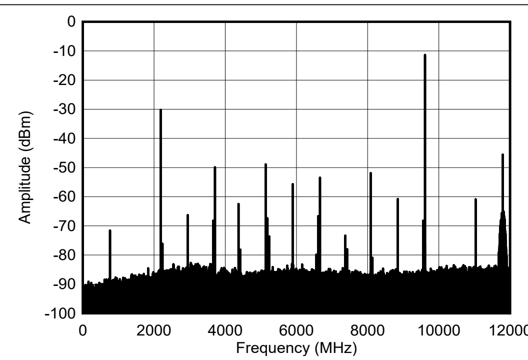
Includes PCB and cable losses.

図 7-262. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (wideband)



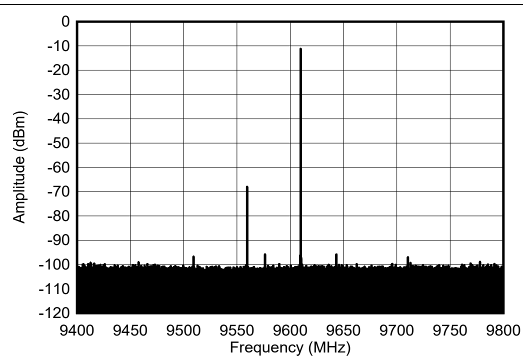
Includes PCB and cable losses.

図 7-263. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (400 MHz BW)



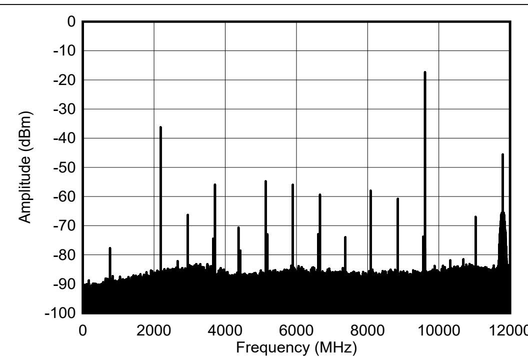
Includes PCB and cable losses.

図 7-264. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (wideband)



Includes PCB and cable losses.

図 7-265. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (400 MHz BW)

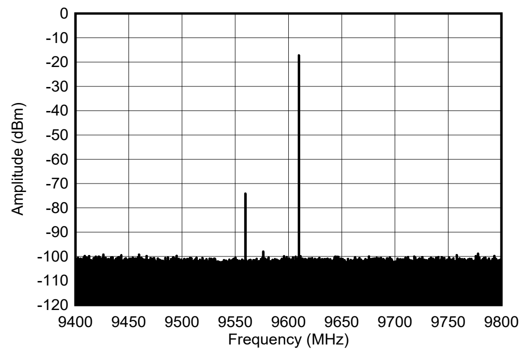


Includes PCB and cable losses.

図 7-266. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (wideband)

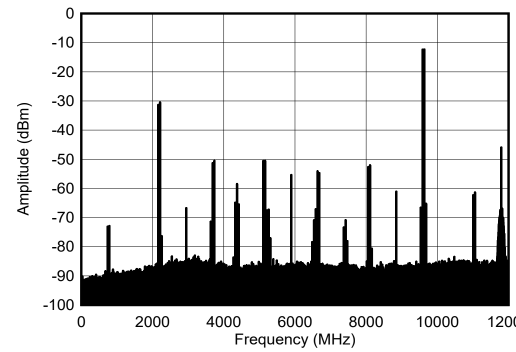
7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



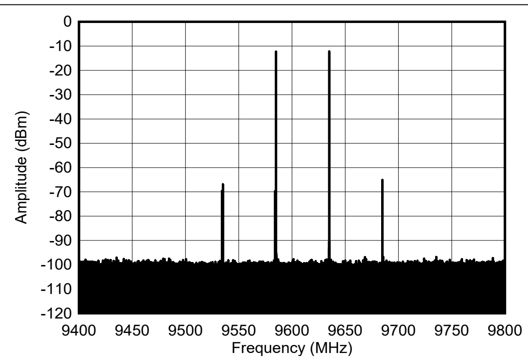
Includes PCB and cable losses.

図 7-267. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (400 MHz BW)



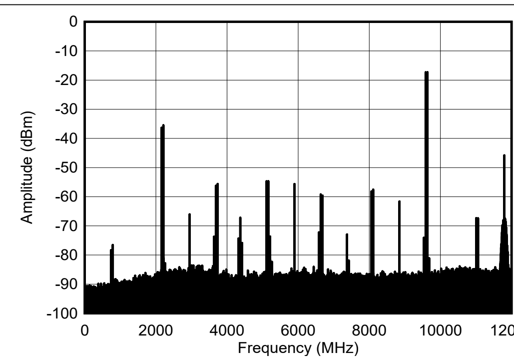
Includes PCB and cable losses, 50 MHz tone spacing.

図 7-268. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (wideband)



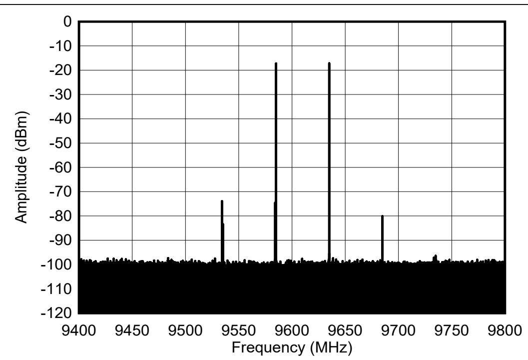
Includes PCB and cable losses, 50 MHz tone spacing.

図 7-269. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (400 MHz BW)



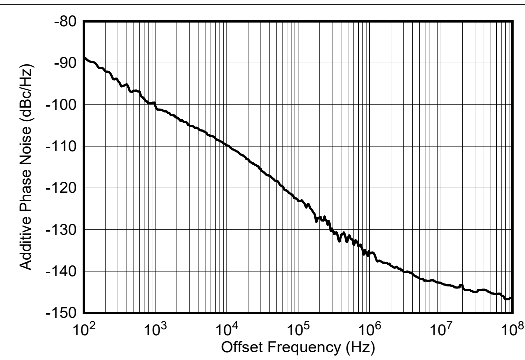
Includes PCB and cable losses, 50MHz tone spacing.

図 7-270. TX 2-Tone Spectrum at 9.61 GHz and -12 dBFS (wideband)



Includes PCB and cable losses, 50 MHz tone spacing.

図 7-271. TX 2-Tone Spectrum at 9.61 GHz and -12 dBFS (400 MHz BW)



Single sideband, external clock mode, input clock phase noise removed

図 7-272. TX Additive Phase Noise vs Offset Frequency at 9.61 GHz

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

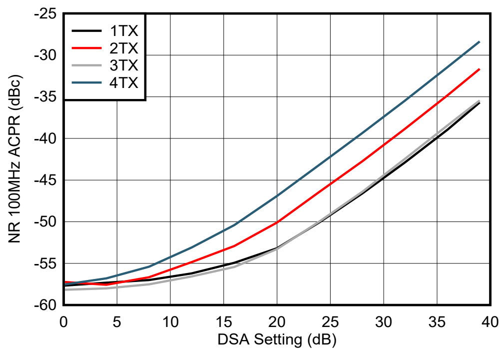


図 7-273. TX NR100MHz ACPR vs DSA Setting at 9.61 GHz

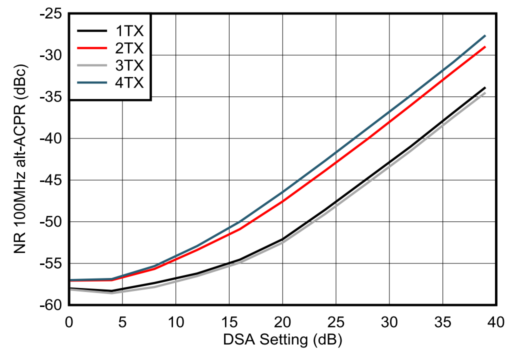


図 7-274. TX NR100MHz alt-ACPR vs DSA Setting at 9.61 GHz

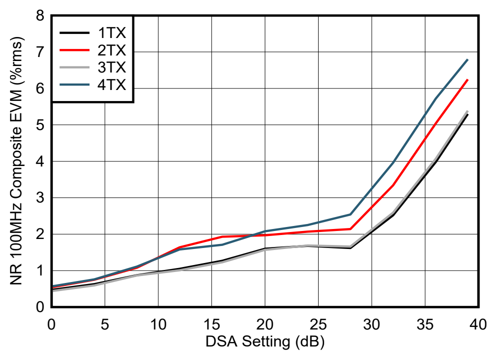
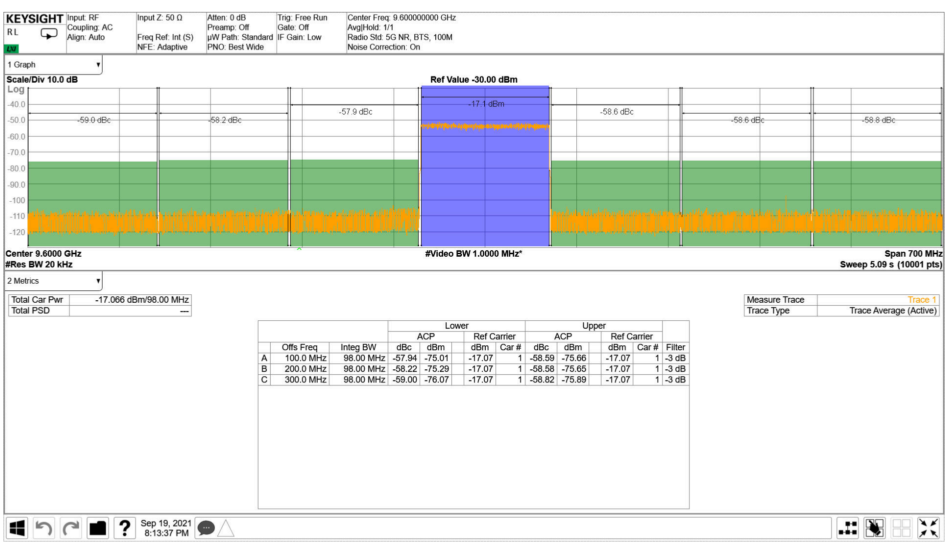


図 7-275. TX NR100MHz EVM vs DSA Setting at 9.61 GHz



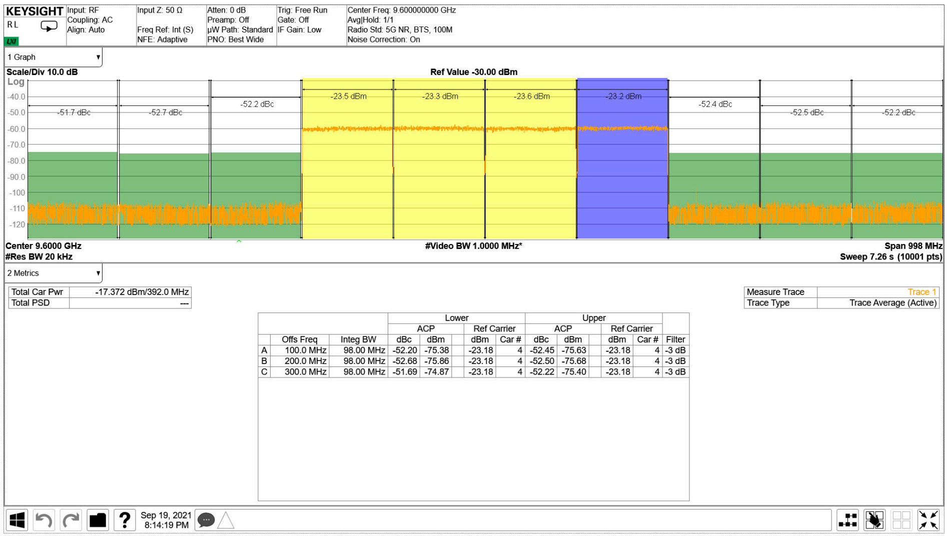
	Offs Freq	Integ BW	Lower ACP dBc	Lower ACP dBm	Lower Ref Carrier dBm	Car #	Upper ACP dBc	Upper ACP dBm	Upper Ref Carrier dBm	Car #	Filter
A	100.0 MHz	98.00 MHz	-57.94	-75.01	-17.07	1	-58.59	-75.66	-17.07	1	-3 dB
B	200.0 MHz	98.00 MHz	-58.22	-75.29	-17.07	1	-58.58	-75.65	-17.07	1	-3 dB
C	300.0 MHz	98.00 MHz	-59.00	-76.07	-17.07	1	-58.82	-75.89	-17.07	1	-3 dB

Includes PCB and cable losses.

図 7-276. TX NR100 MHz Output Spectrum at 9.61 GHz

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 1474.56 MHz, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

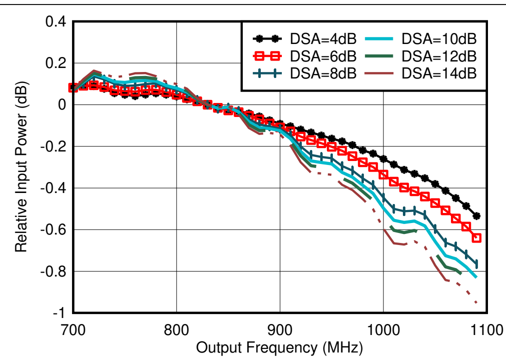


Includes PCB and cable losses.

図 7-277. TX 4xNR100 MHz Output Spectrum at 9.61 GHz

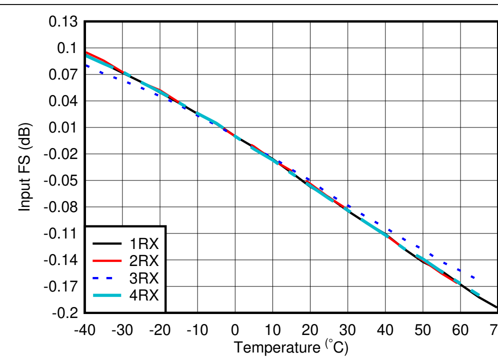
7.12.8 RX Typical Characteristics at 800 MHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching, normalized to 830 MHz

図 7-278. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 830 MHz

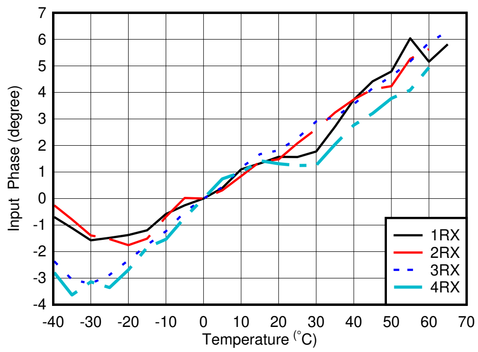


With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

図 7-279. RX Input Fullscale vs Temperature and Channel at 800 MHz

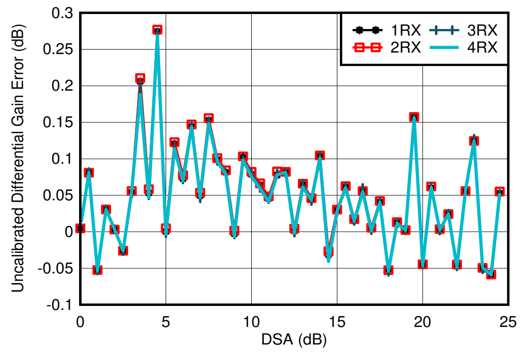
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching, normalized to phase at 25°C

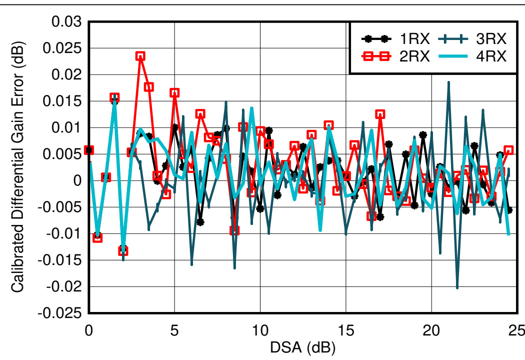
図 7-280. RX Input Phase vs Temperature and DSA at f_{OUT} = 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

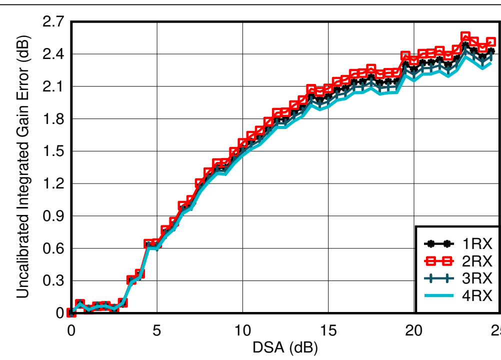
図 7-281. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

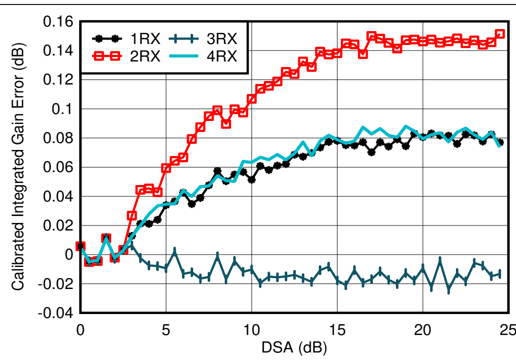
図 7-282. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

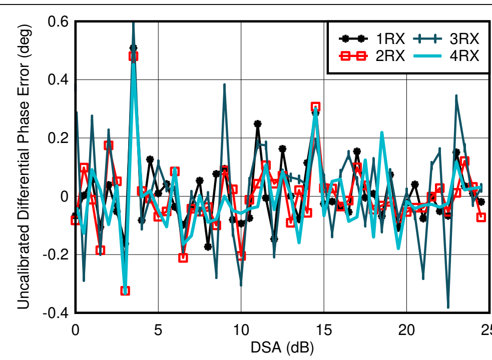
図 7-283. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 7-284. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



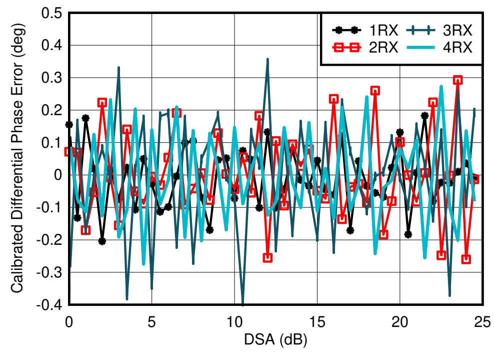
With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 7-285. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz

7.12.8 RX Typical Characteristics at 800 MHz (continued)

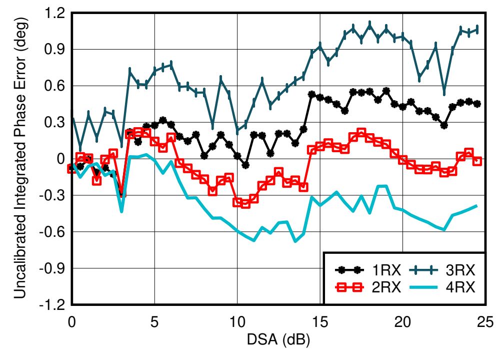
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

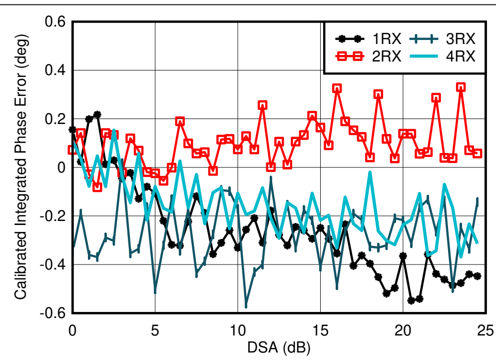
図 7-286. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

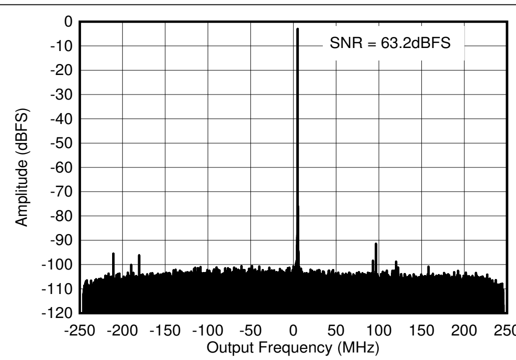
図 7-287. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

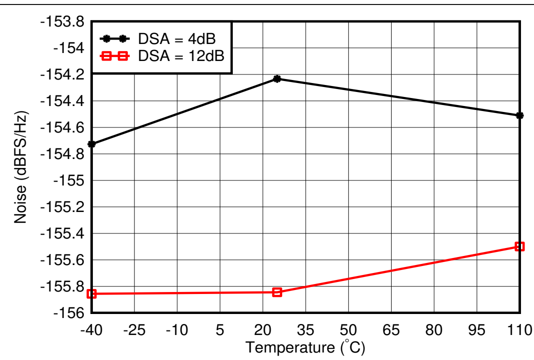
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-288. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



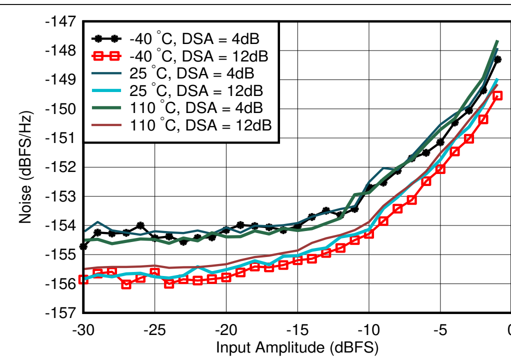
With 0.8 GHz matching, f_{IN} = 840 MHz, A_{IN}= –3 dBFS

図 7-289. RX Output FFT at 0.8 GHz



With 0.8 GHz matching, 12.5-MHz offset from tone

図 7-290. RX Noise Spectral Density vs Temperature at 0.8 GHz

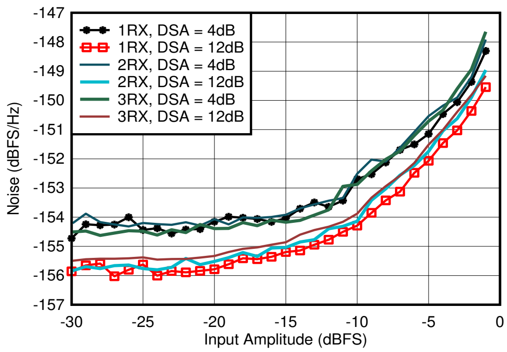


With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 7-291. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz

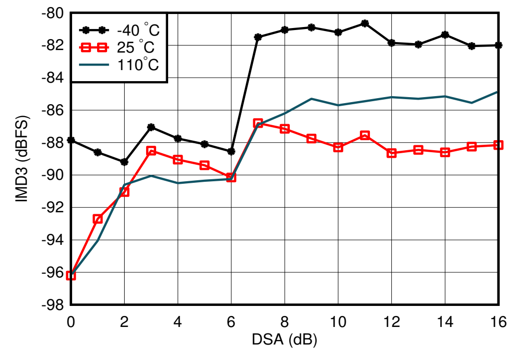
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



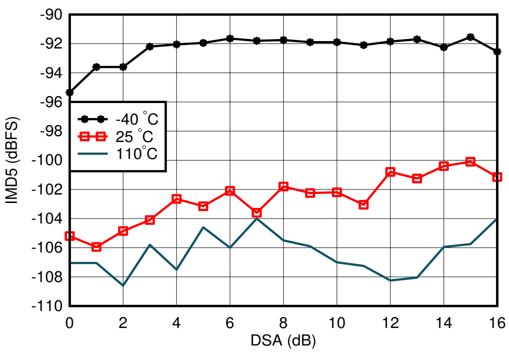
With 0.8 GHz matching, 12.5-MHz offset from tone

図 7-292. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



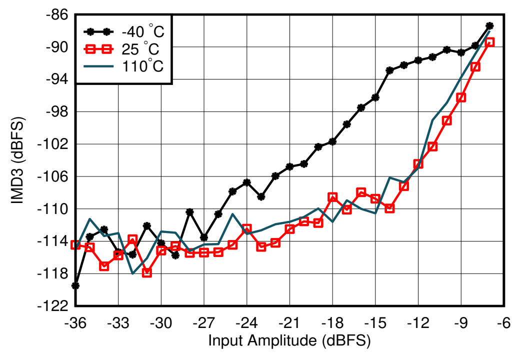
A. With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 7-293. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz



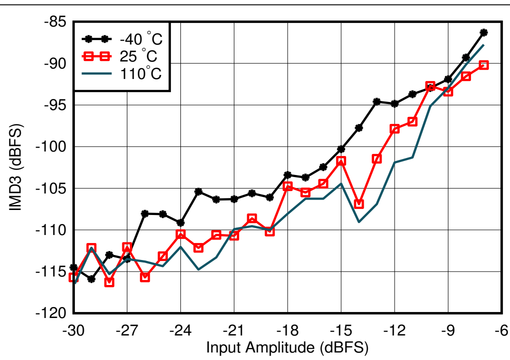
With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 7-294. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



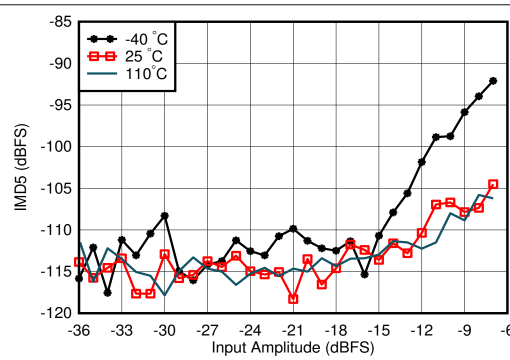
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 7-295. RX IMD3 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 7-296. RX IMD3 vs Input Level and Temperature at 0.8 GHz

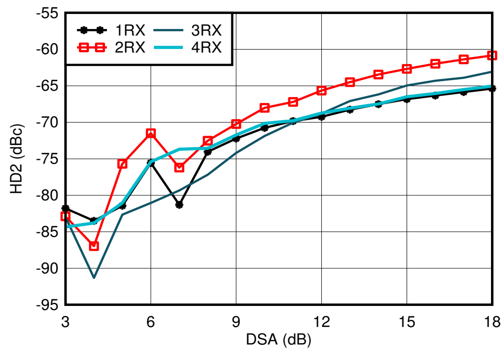


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 7-297. RX IMD5 vs Input Level and Temperature at 0.8 GHz

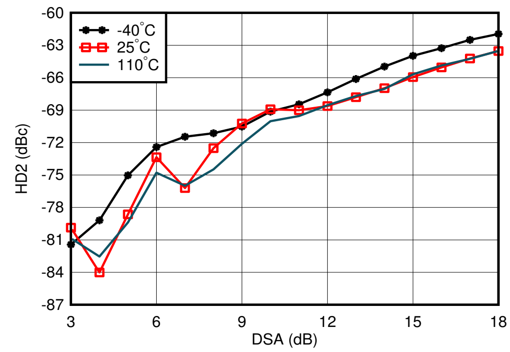
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



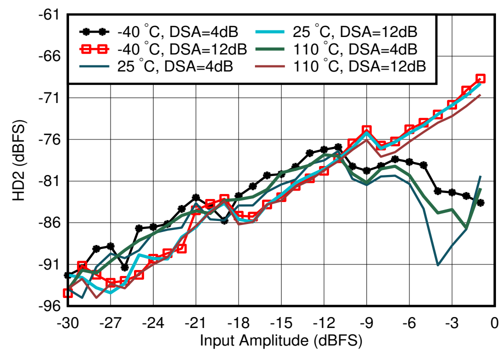
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-298. RX HD2 vs DSA Setting and Channel at 0.8 GHz



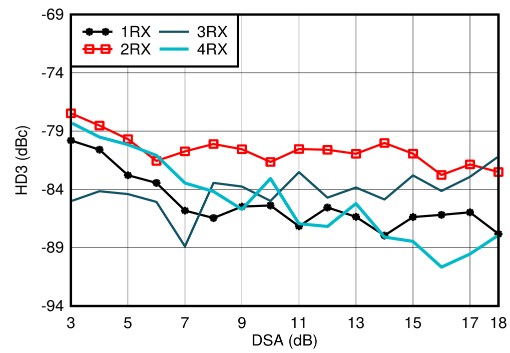
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-299. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



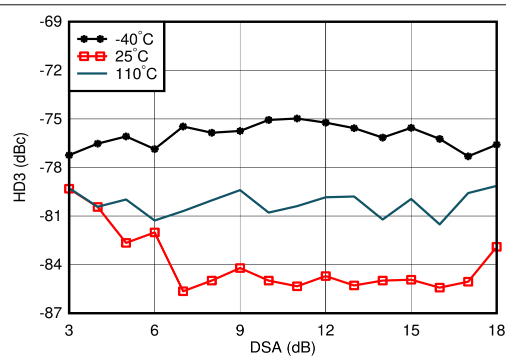
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-300. RX HD2 vs Input Level and Temperature at 0.8 GHz



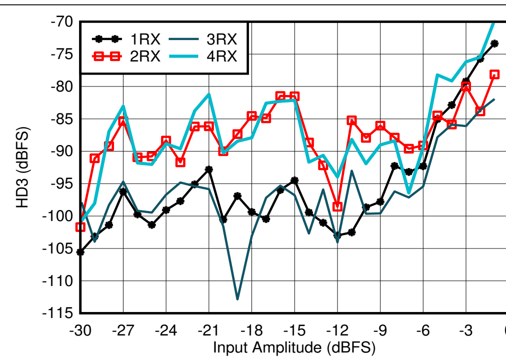
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-301. RX HD3 vs DSA Setting and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-302. RX HD3 vs DSA Setting and Temperature at 0.8 GHz

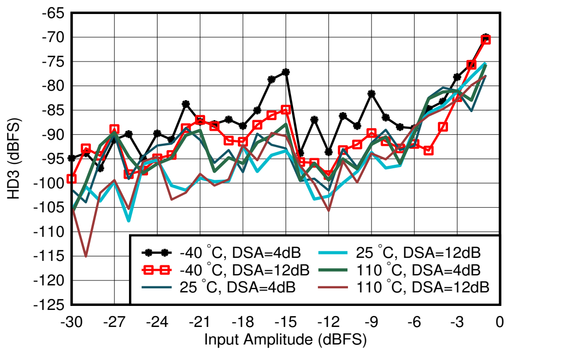


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-303. RX HD3 vs Input Level and Channel at 0.8 GHz

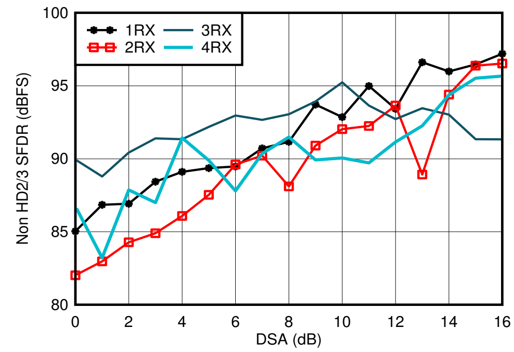
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



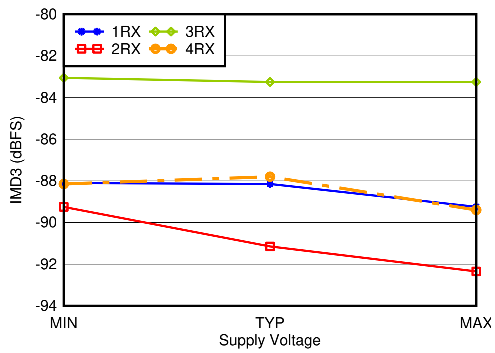
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-304. RX HD3 vs Input Level and Temperature at 0.8 GHz



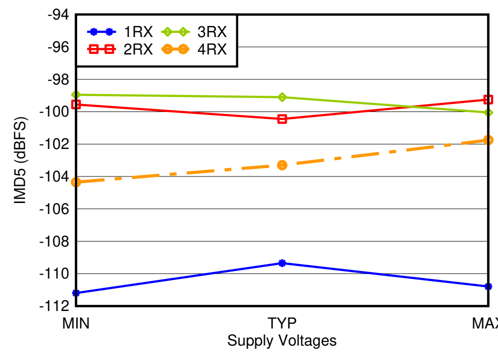
With 0.8 GHz matching

図 7-305. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



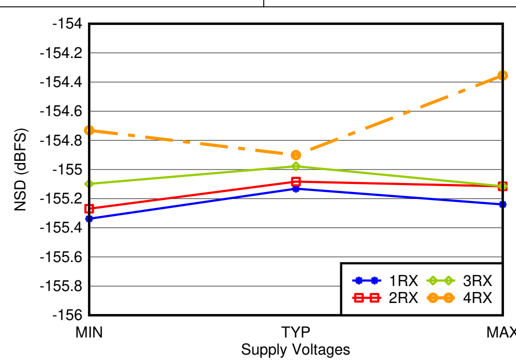
With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-306. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-307. RX IMD5 vs Supply and Channel at 0.8 GHz

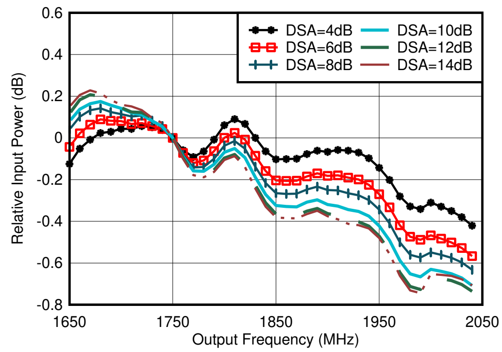


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-308. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

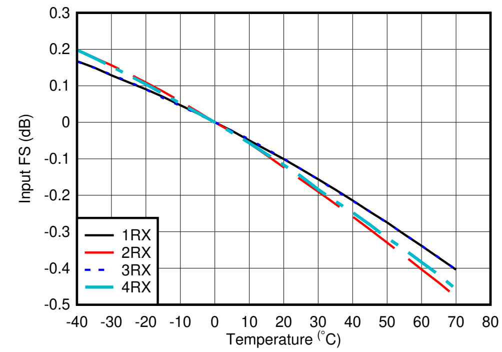
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



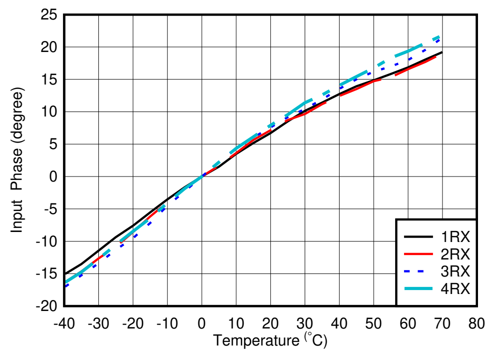
With 1.8 GHz matching, normalized to 1.75 GHz

図 7-309. RX In-Band Gain Flatness, f_{IN} = 1750 MHz



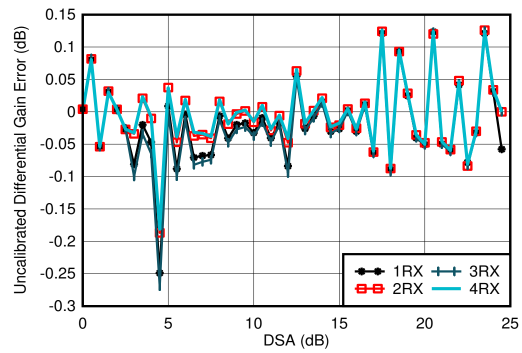
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

図 7-310. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at 25°C

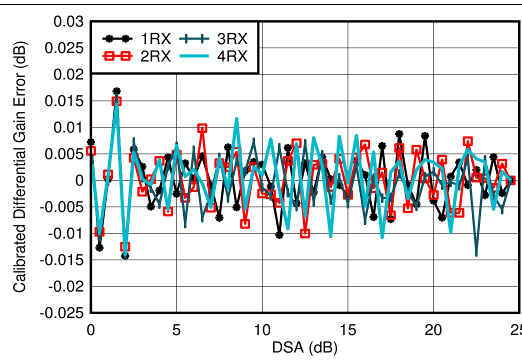
図 7-311. RX Input Phase vs Temperature and DSA at f_{IN} = 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

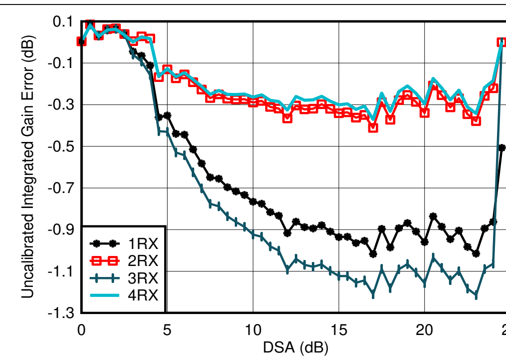
図 7-312. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 7-313. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



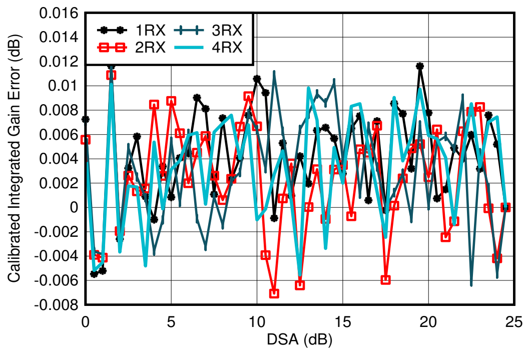
With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 7-314. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

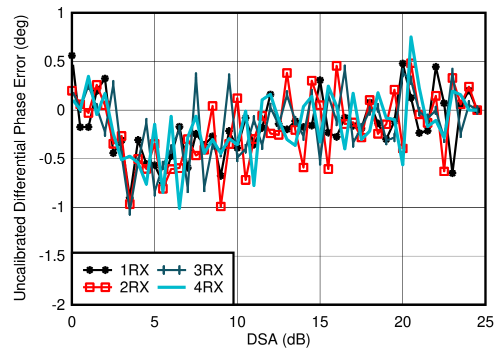
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

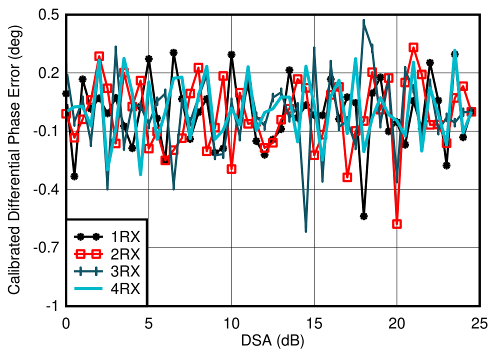
図 7-315. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

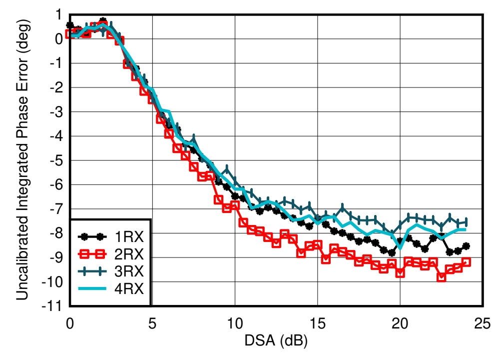
図 7-316. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

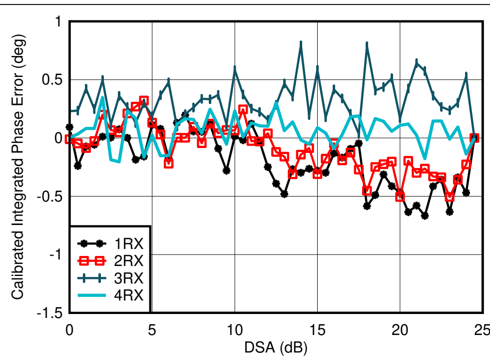
図 7-317. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

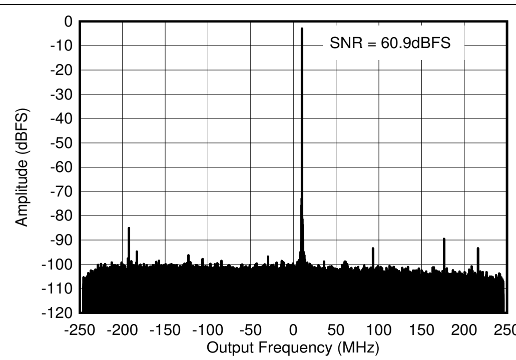
図 7-318. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-319. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

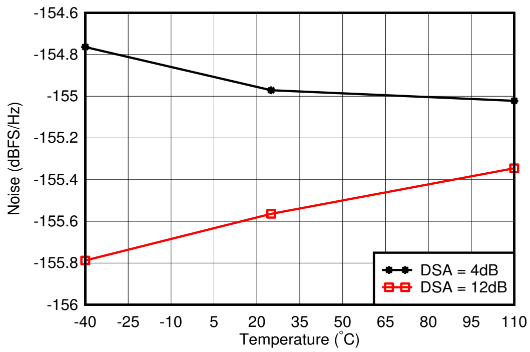


With 1.8 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 7-320. RX Output FFT at 1.75 GHz

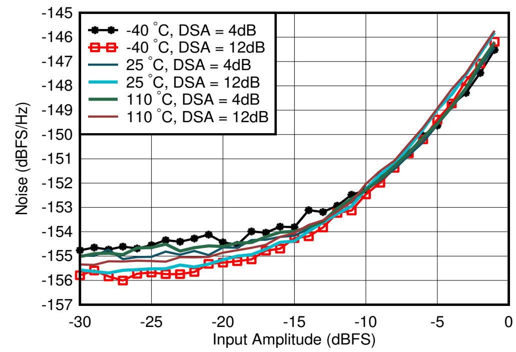
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



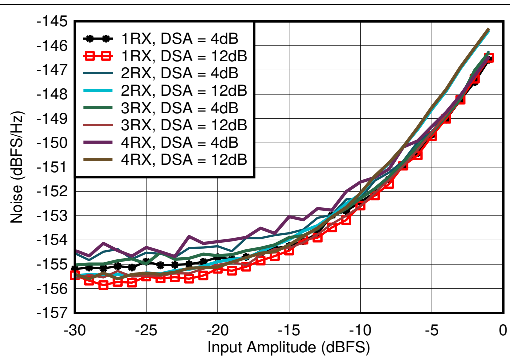
With 1.8 GHz matching, 12.5-MHz offset from tone

図 7-321. RX Noise Spectral Density vs Temperature at 1.75 GHz



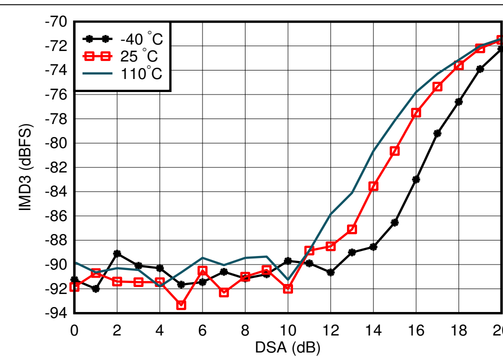
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 7-322. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



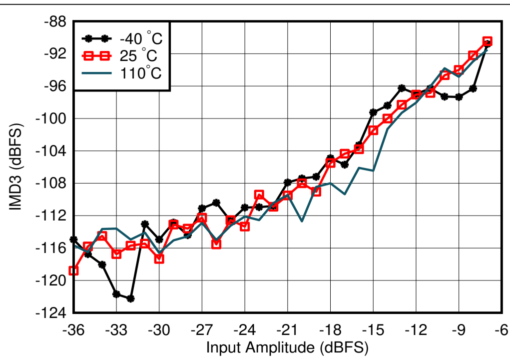
With 1.8 GHz matching, 12.5-MHz offset from tone

図 7-323. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



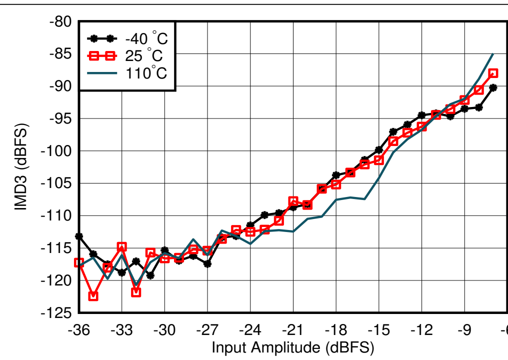
With 1.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 7-324. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 7-325. RX IMD3 vs Input Level and Temperature at 1.75 GHz

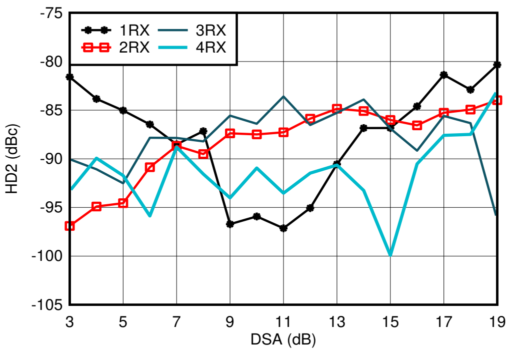


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 7-326. RX IMD3 vs Input Level and Temperature at 1.75 GHz

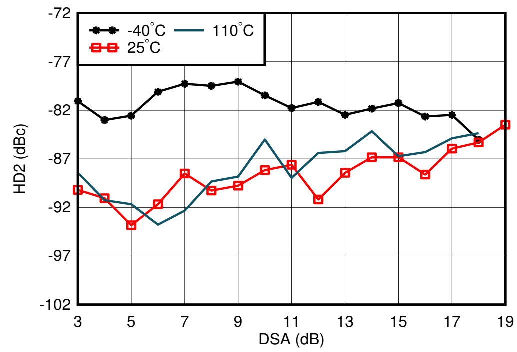
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



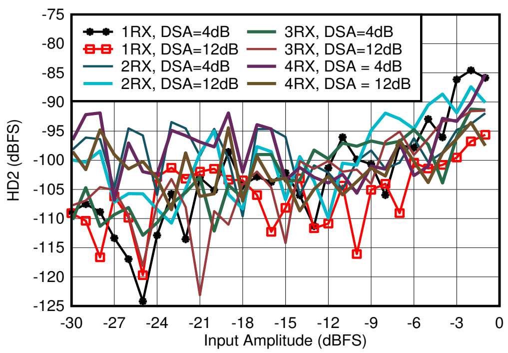
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-327. RX HD2 vs DSA Setting and Channel at 1.9 GHz



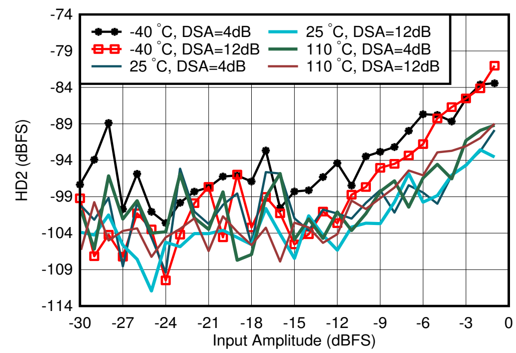
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-328. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



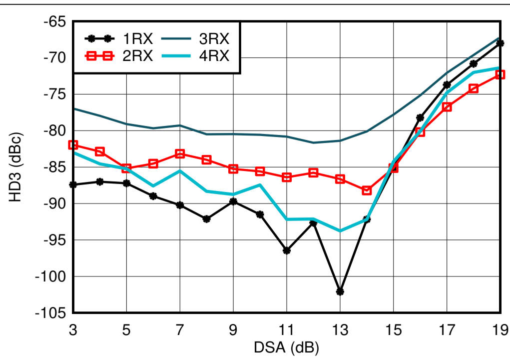
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-329. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



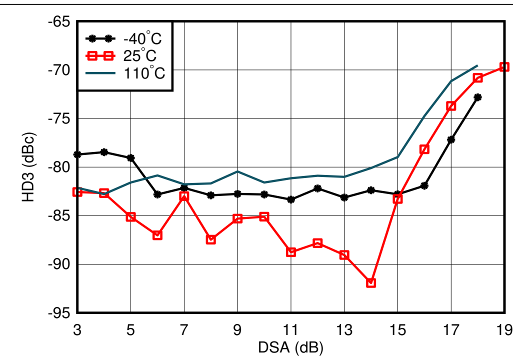
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-330. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz



With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

図 7-331. RX HD3 vs DSA Setting and Channel at 1.9 GHz

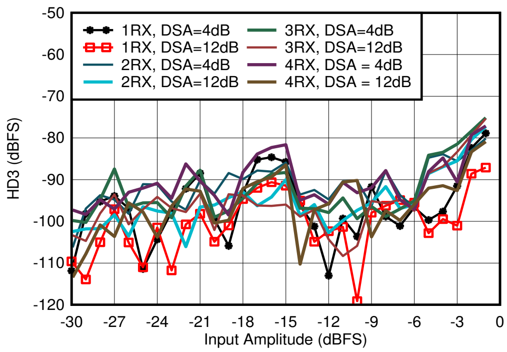


With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

図 7-332. RX HD3 vs DSA Setting and Temperature at 1.9 GHz

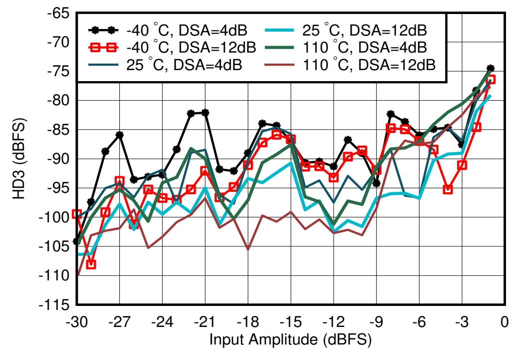
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



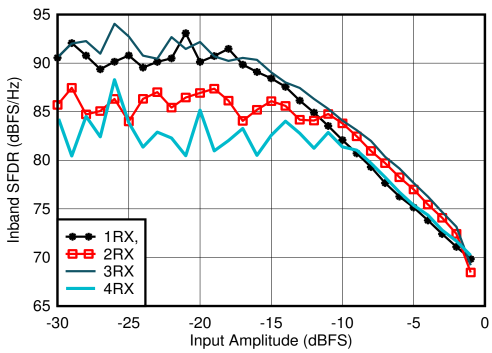
With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

図 7-333. RX HD3 vs Input Level and Channel at 1.9 GHz



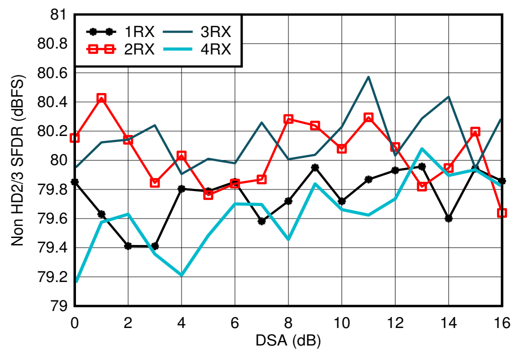
With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

図 7-334. RX HD3 vs Input Level and Temperature at 1.9 GHz



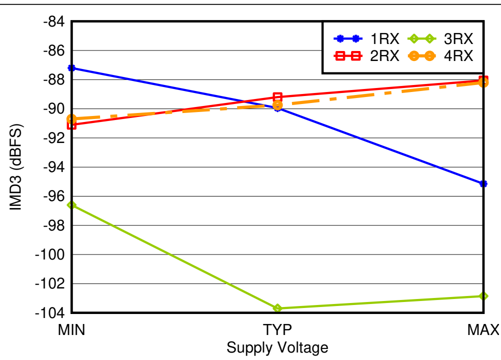
With 1.8 GHz matching, decimated by 3

図 7-335. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75 GHz



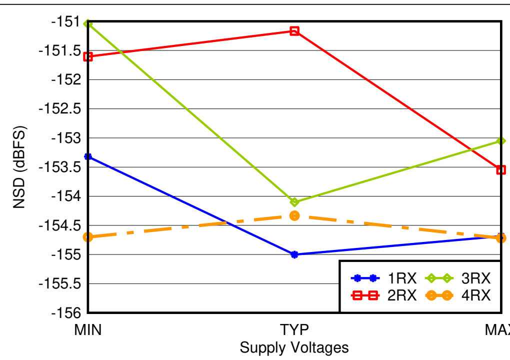
With 1.8 GHz matching

図 7-336. RX Non-HD2/3 vs DSA Setting at 1.75 GHz



With 1.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-337. RX IMD3 vs Supply and Channel at 1.75 GHz

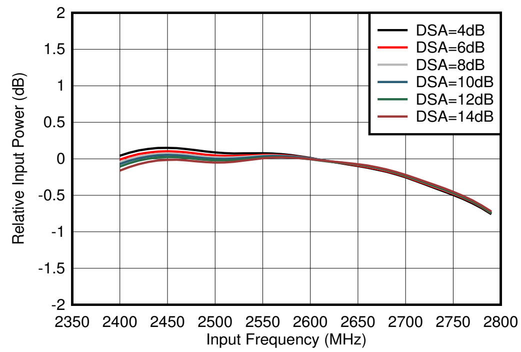


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-338. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

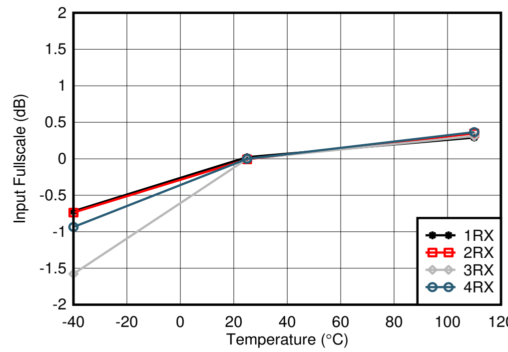
7.12.10 RX Typical Characteristics at 2.6 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



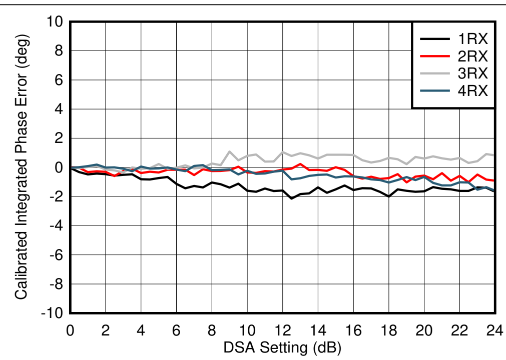
With matching, normalized to power at 2.6 GHz for each DSA setting

図 7-339. RX Inband Gain Flatness, f_{IN} = 2600 MHz



With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

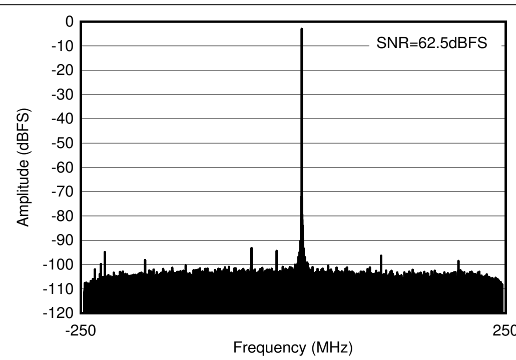
図 7-340. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



With 2.6 GHz matching

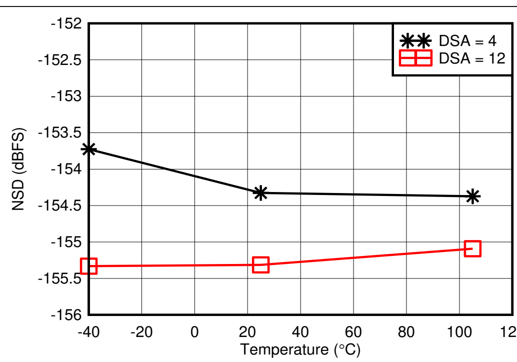
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-341. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



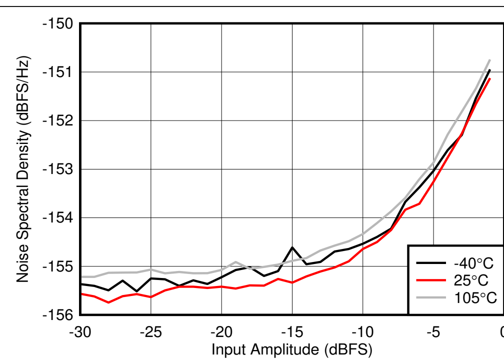
With 2.6 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 7-342. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

図 7-343. RX Noise Spectral Density vs Temperature at 2.6 GHz

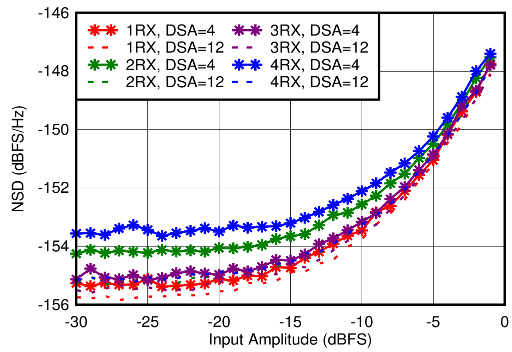


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 7-344. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

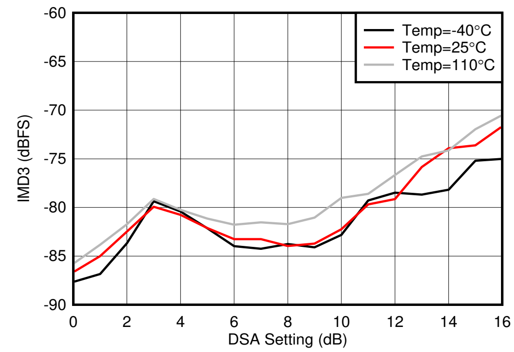
7.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



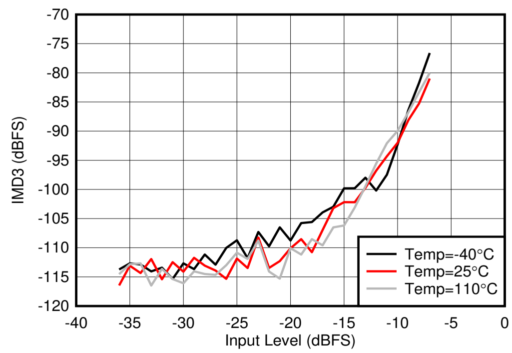
With 2.6 GHz matching, 12.5-MHz offset from tone

図 7-345. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



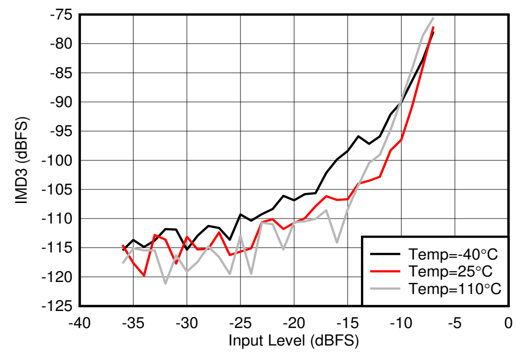
With 2.6 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 7-346. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



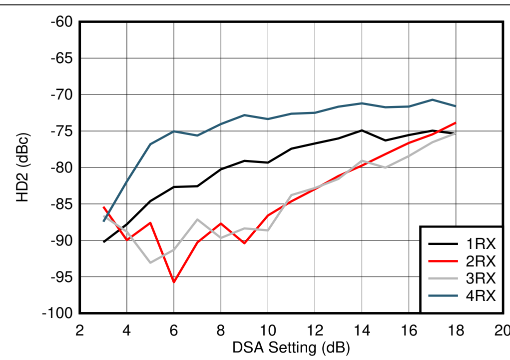
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 7-347. RX IMD3 vs Input Level and Temperature at 2.6 GHz



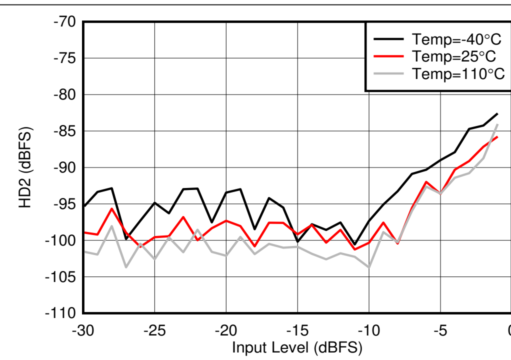
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 7-348. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-349. RX HD2 vs DSA Setting and Channel at 2.6 GHz

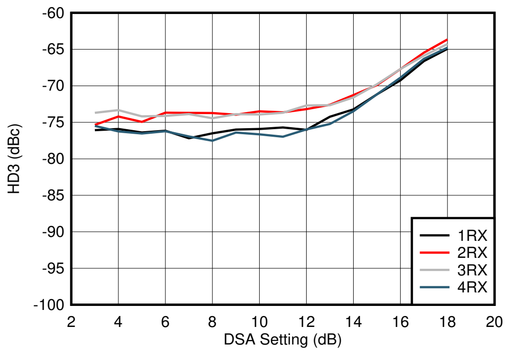


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-350. RX HD2 vs Input Level and Temperature at 2.6 GHz

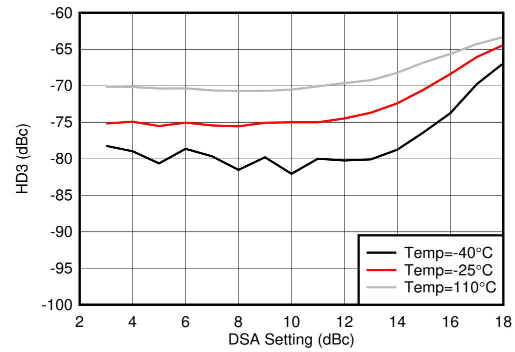
7.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



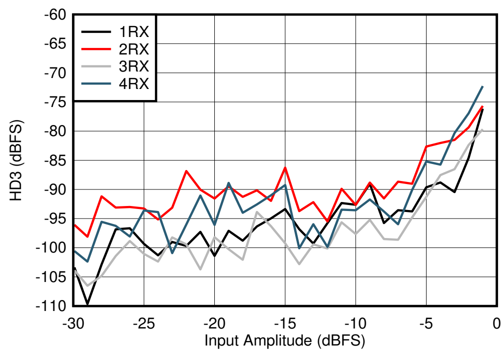
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-351. RX HD3 vs DSA Setting and Channel at 2.6 GHz



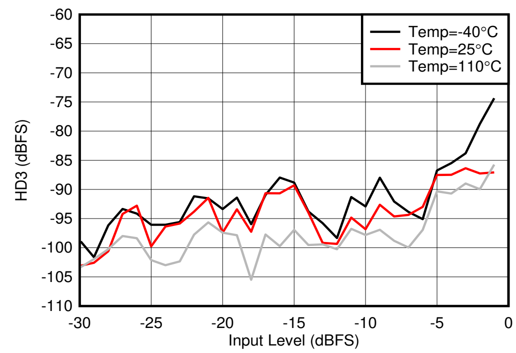
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-352. RX HD3 vs DSA Setting and Temperature at 2.6 GHz



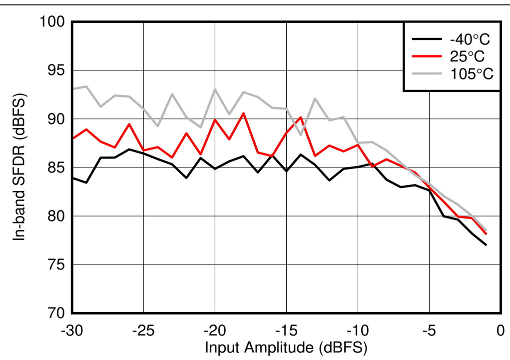
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-353. RX HD3 vs Input Level and Channel at 2.6 GHz



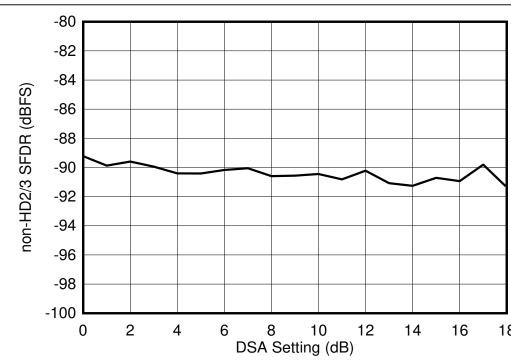
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-354. RX HD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, decimate by 4

図 7-355. RX In-Band SFDR (±300 MHz) vs Input Amplitude and Temperature at 2.6 GHz

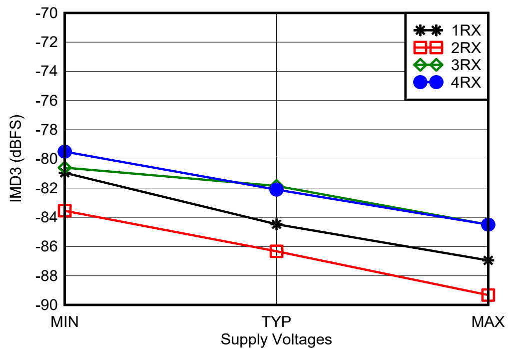


With 2.6 GHz matching

図 7-356. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

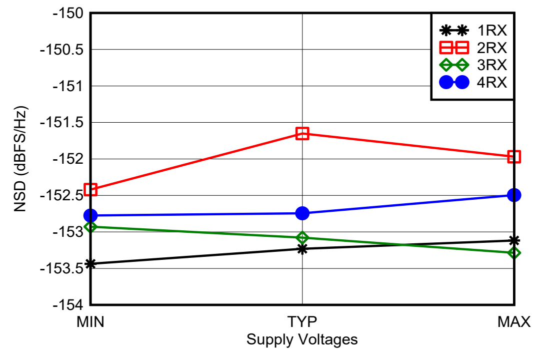
7.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 2.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-357. RX IMD3 vs Supply and Channel at 2.6 GHz

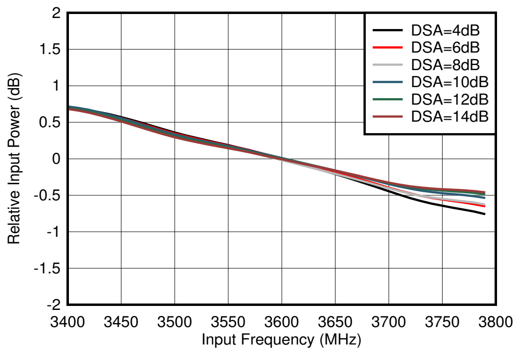


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-358. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

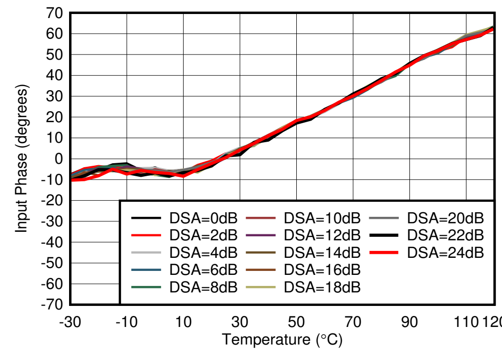
7.12.11 RX Typical Characteristics at 3.5 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



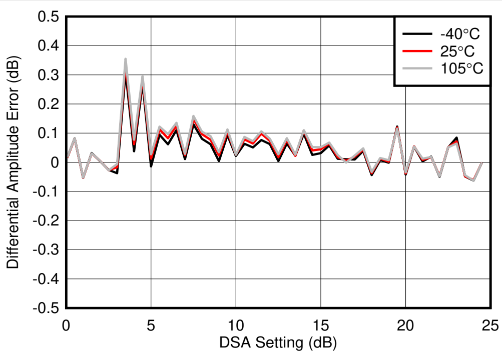
With 3.6 GHz matching, normalized to 3.6 GHz

図 7-359. RX In-Band Gain Flatness, f_{IN} = 3600 MHz



With 3.6 GHz matching, normalized to phase at 25°C

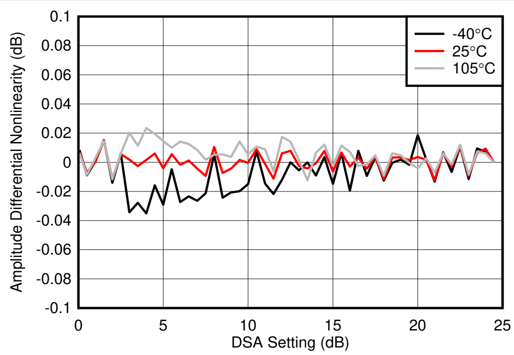
図 7-360. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

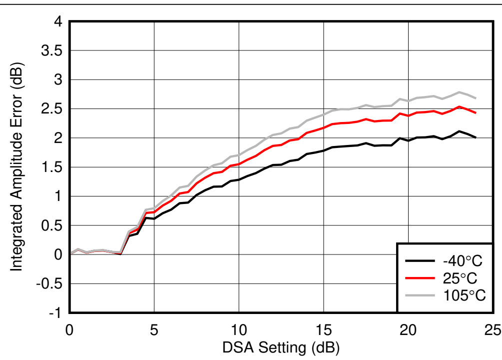
図 7-361. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

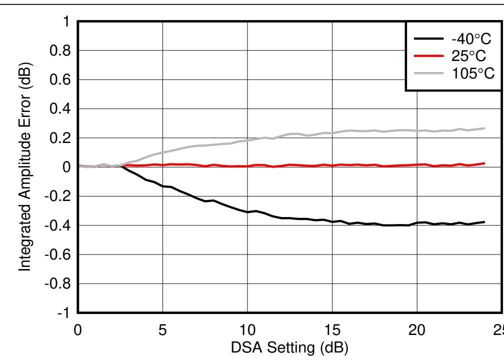
図 7-362. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 7-363. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



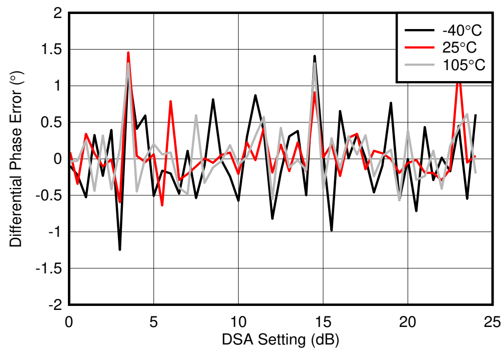
With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 7-364. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

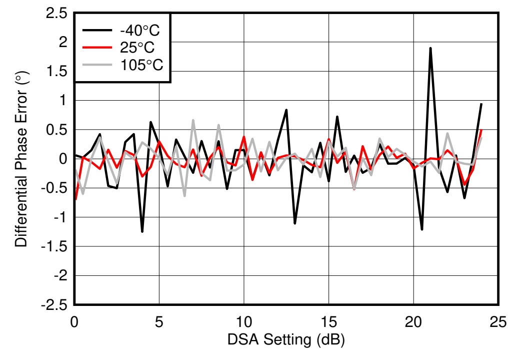
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 3.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

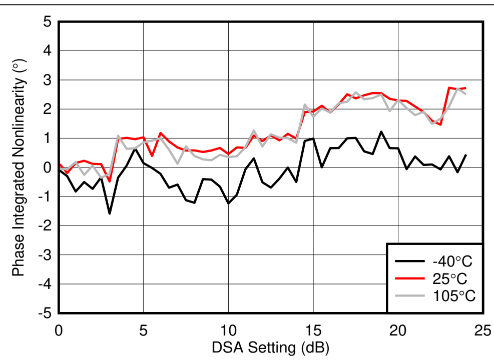
図 7-365. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

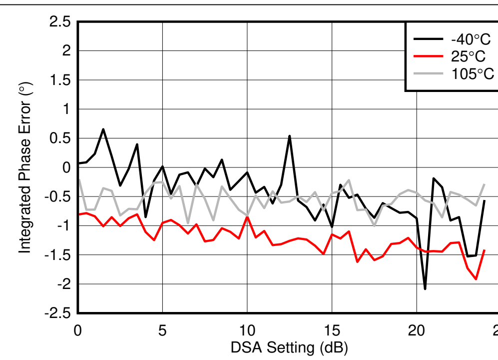
図 7-366. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

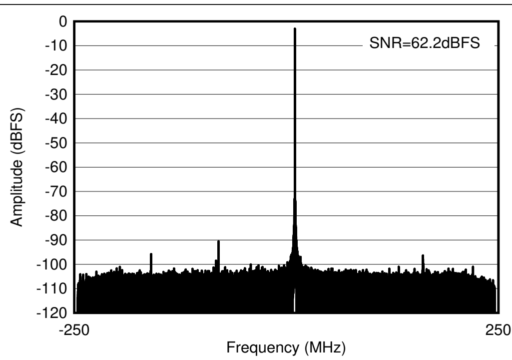
図 7-367. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

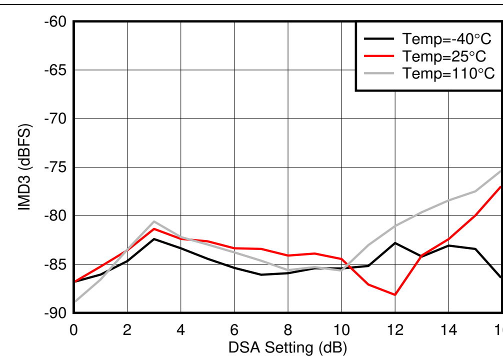
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-368. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching , f_{IN} = 3610 MHz, A_{IN} = –3 dBFS

図 7-369. RX Output FFT at 3.6 GHz

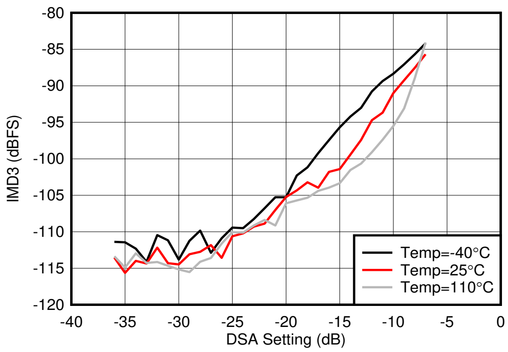


With 3.5 GHz matching, each tone at –7 dBFS, 20-MHz tone spacing

図 7-370. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

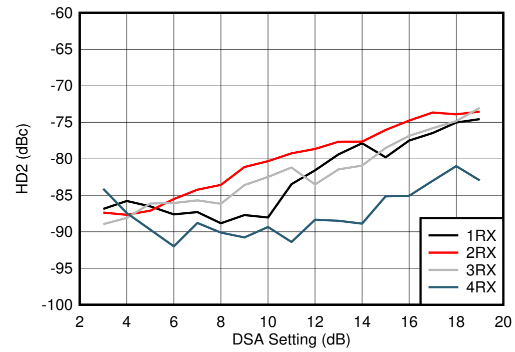
7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



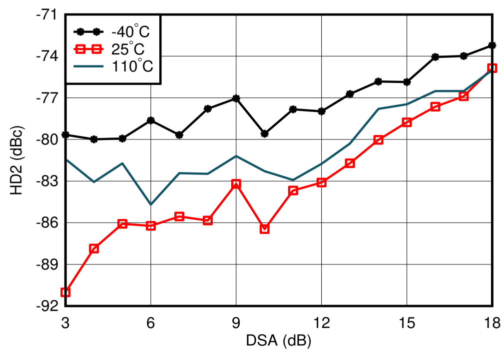
With 3.5 GHz matching, 20-MHz tone spacing

図 7-371. RX IMD3 vs Input Level and Temperature at 3.6 GHz



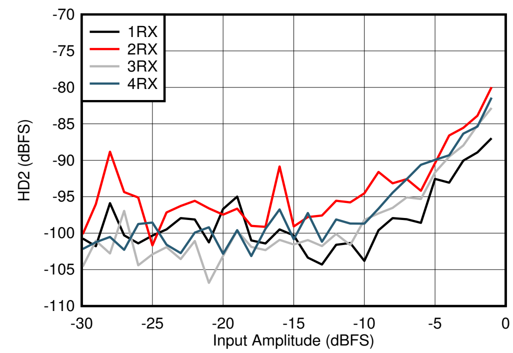
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-372. RX HD2 vs DSA Setting and Channel at 3.6 GHz



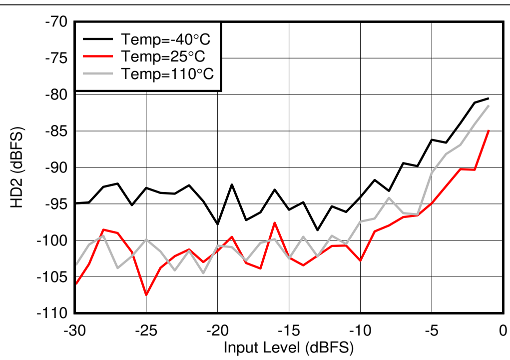
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-373. RX HD2 vs DSA Setting and Temperature at 3.6 GHz



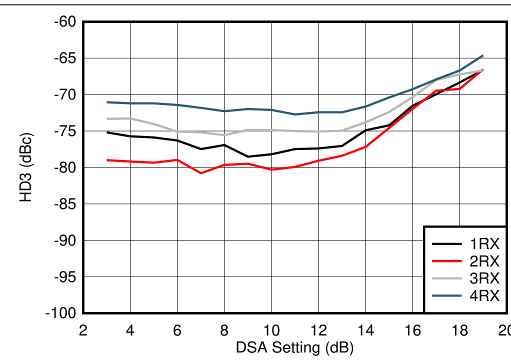
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-374. RX HD2 vs Input Level and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-375. RX HD2 vs Input Level and Temperature at 3.6 GHz

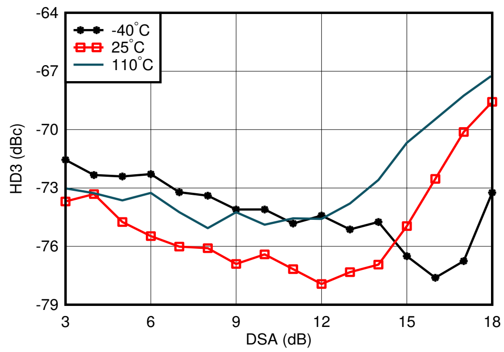


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-376. RX HD3 vs DSA Setting and Channel at 3.6 GHz

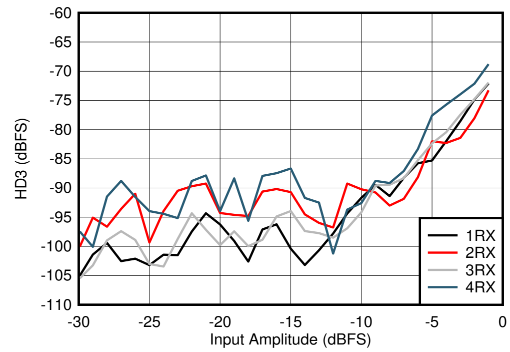
7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



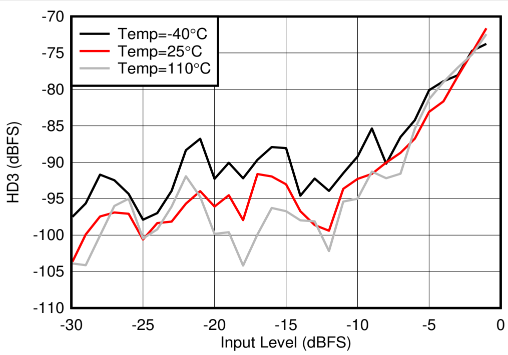
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-377. RX HD3 vs DSA Setting and Temperature at 3.6 GHz



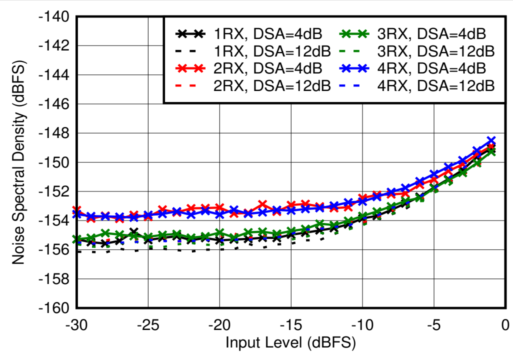
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-378. RX HD3 vs Input Level and Channel at 3.6 GHz



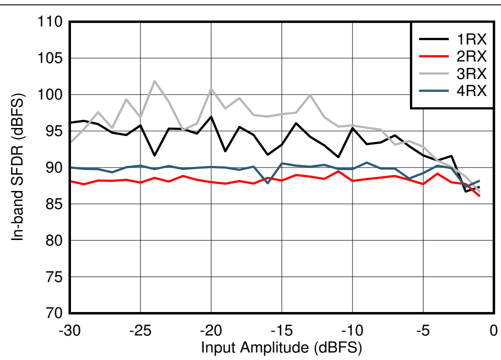
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-379. RX HD3 vs Input Level and Temperature at 3.6 GHz



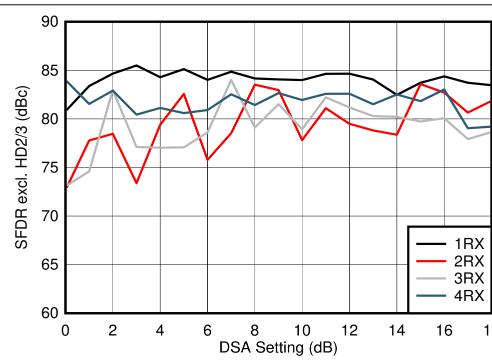
With 3.5 GHz matching, 12.5-MHz offset from tone

図 7-380. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



With 3.5 GHz matching

図 7-381. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz

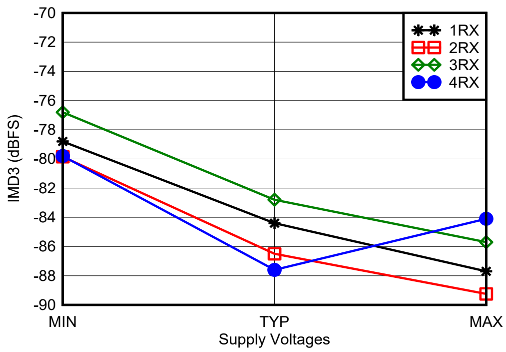


With 3.5 GHz matching

図 7-382. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz

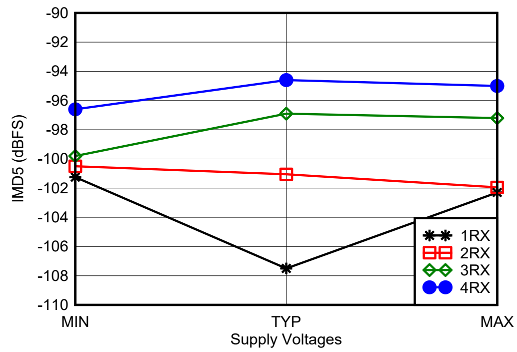
7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



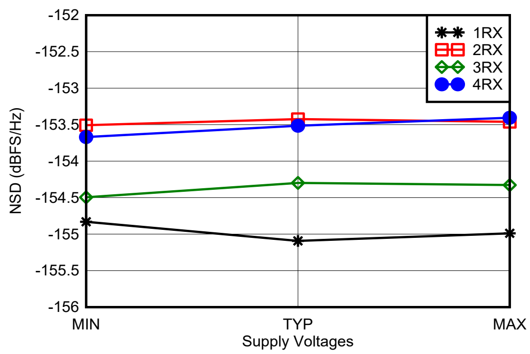
With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-383. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-384. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

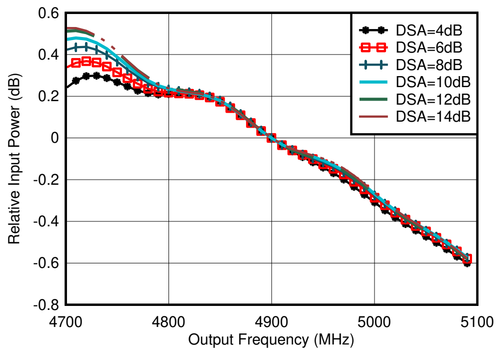


With 3.6 GHz matching, tone at –20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-385. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

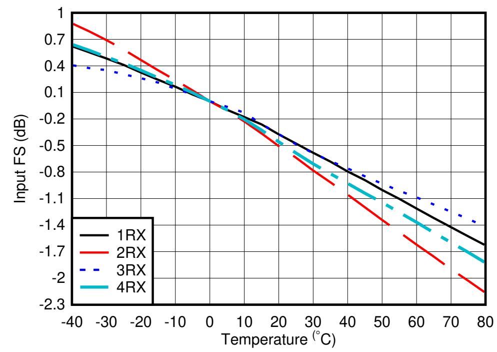
7.12.12 RX Typical Characteristics at 4.9 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



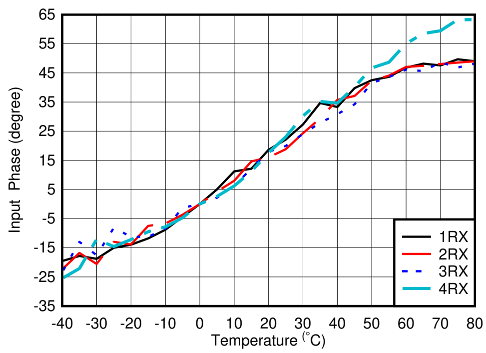
With matching, normalized to power at 4.9 GHz for each DSA setting

図 7-386. RX Inband Gain Flatness, f_{IN} = 4900 MHz



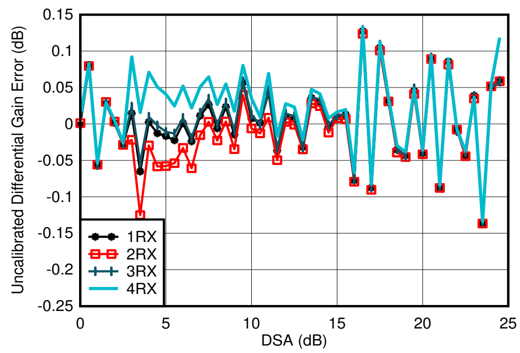
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

図 7-387. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

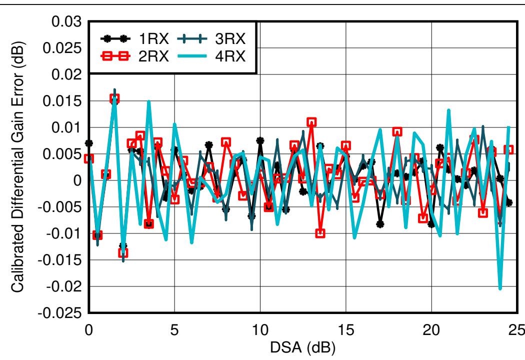
図 7-388. RX Input Phase vs Temperature and DSA at f_{OUT} = 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

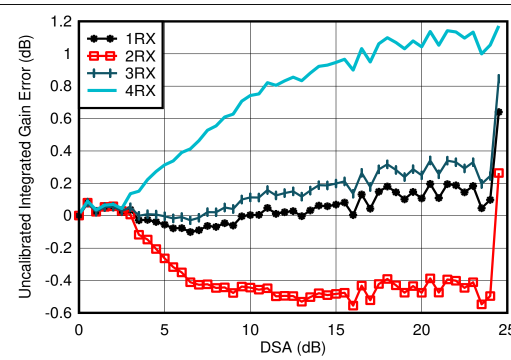
図 7-389. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 7-390. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



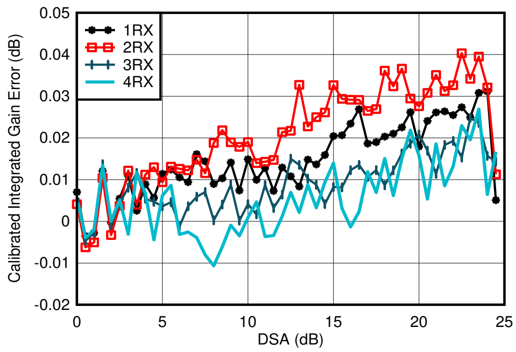
With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 7-391. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

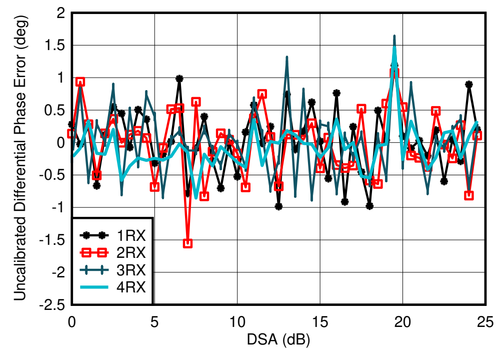
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

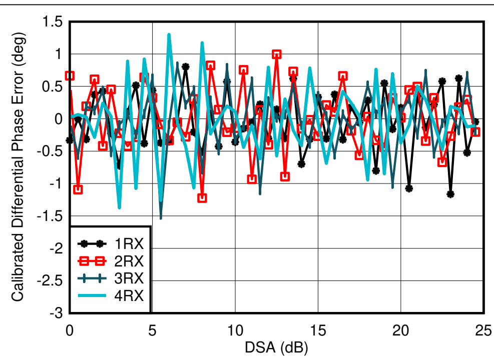
図 7-392. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

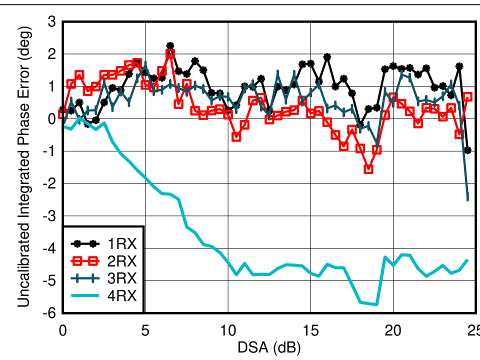
図 7-393. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

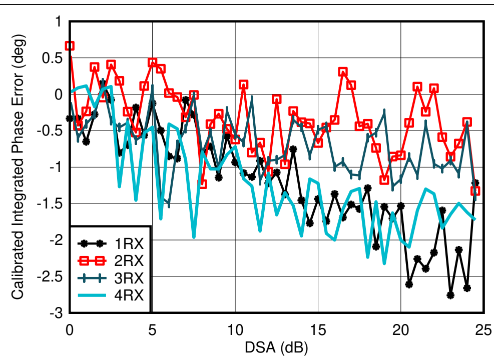
図 7-394. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

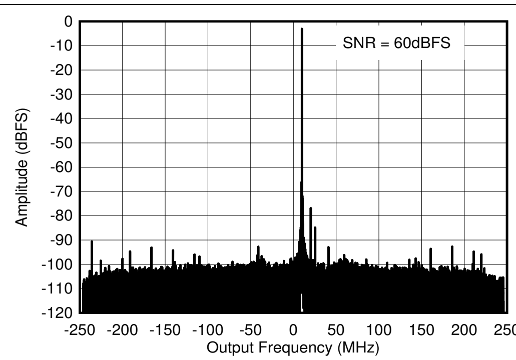
図 7-395. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 7-396. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

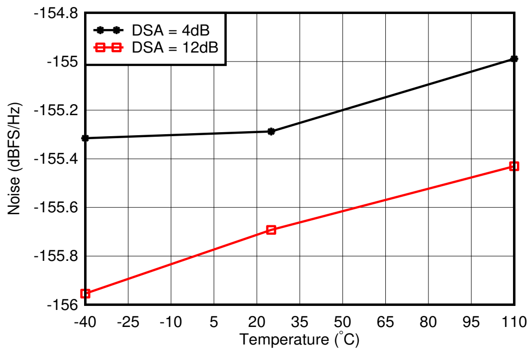


With 4.9 GHz matching, f_{IN} = 4910 MHz, A_{IN}= –3 dBFS

図 7-397. RX Output FFT at 4.9 GHz

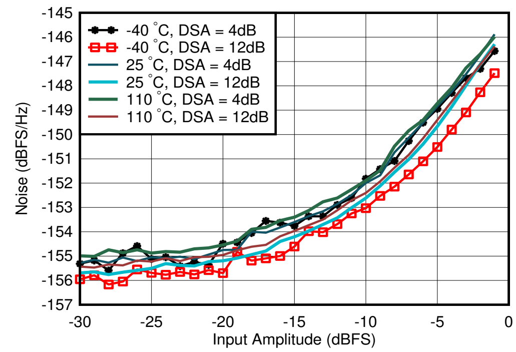
7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



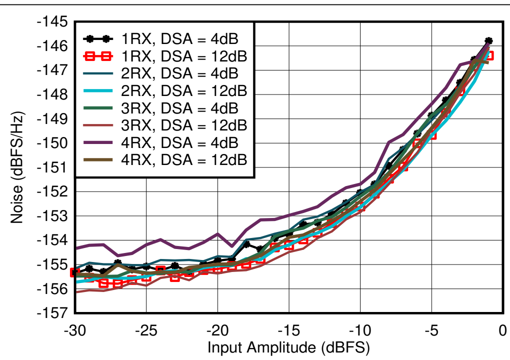
With 4.9 GHz matching, 12.5-MHz offset from tone

図 7-398. RX Noise Spectral Density vs Temperature at 4.9 GHz



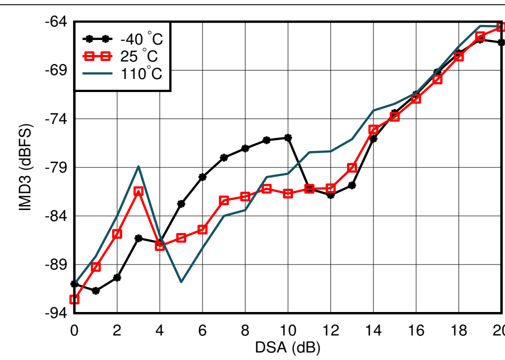
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 7-399. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



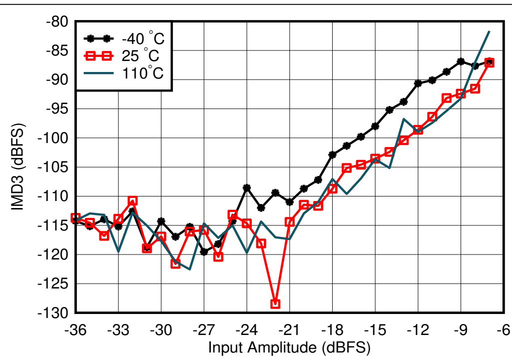
With 4.9 GHz matching, 12.5-MHz offset from tone

図 7-400. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz



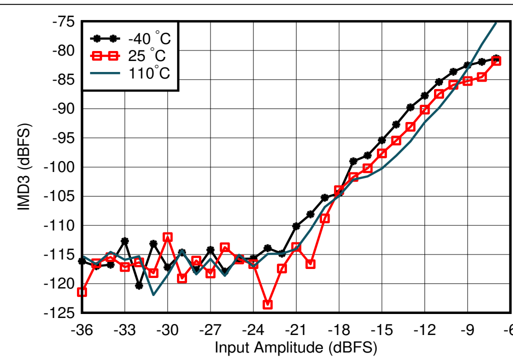
With 4.9 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 7-401. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 7-402. RX IMD3 vs Input Level and Temperature at 4.9 GHz

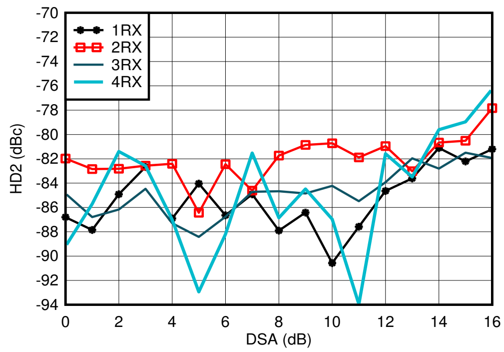


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 7-403. RX IMD3 vs Input Level and Temperature at 4.9 GHz

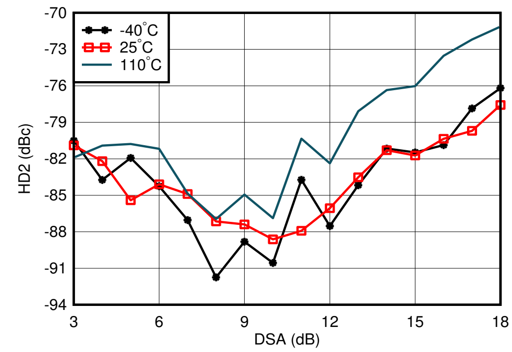
7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



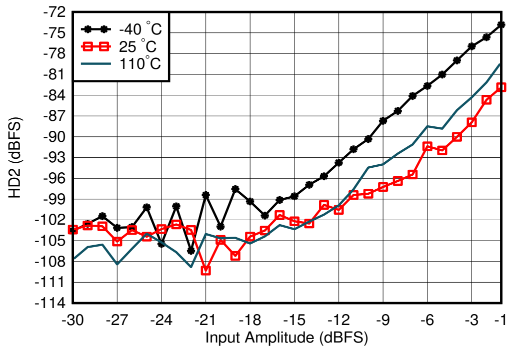
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-404. RX HD2 vs DSA Setting and Channel at 4.9 GHz



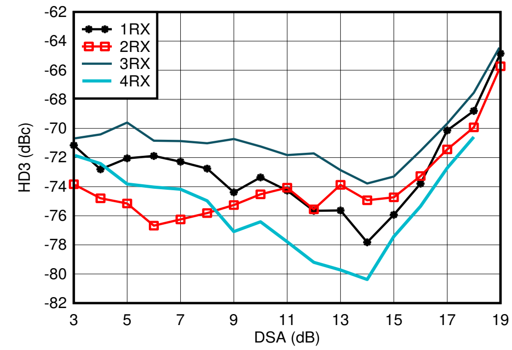
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-405. RX HD2 vs DSA and Temperature at 4.9 GHz



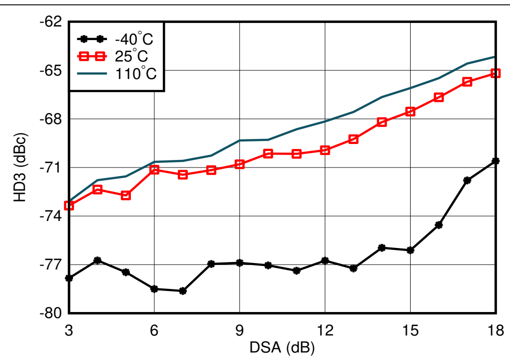
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 7-406. RX HD2 vs Input Level and Temperature at 4.9 GHz



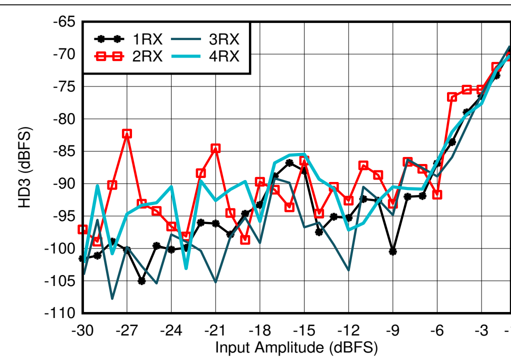
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-407. RX HD3 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-408. RX HD3 vs DSA Setting and Temperature at 4.9 GHz

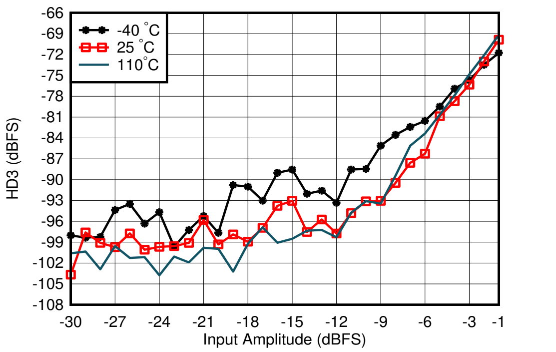


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-409. RX HD3 vs Input Level and Channel at 4.9 GHz

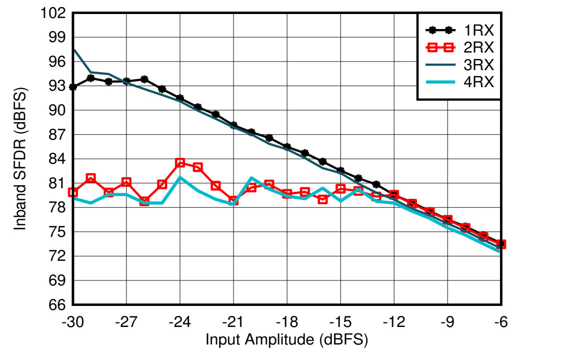
7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



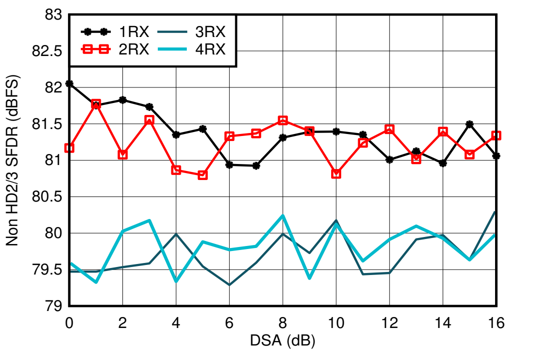
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 7-410. RX HD3 vs Input Level and Temperature at 4.9 GHz



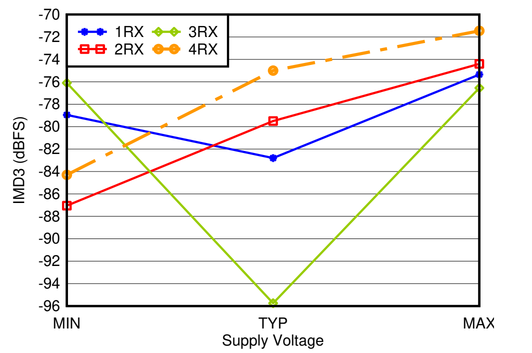
With 4.9 GHz matching, decimate by 3

図 7-411. RX In-Band SFDR (±400 MHz) vs Input Amplitude and Channel at 4.9 GHz



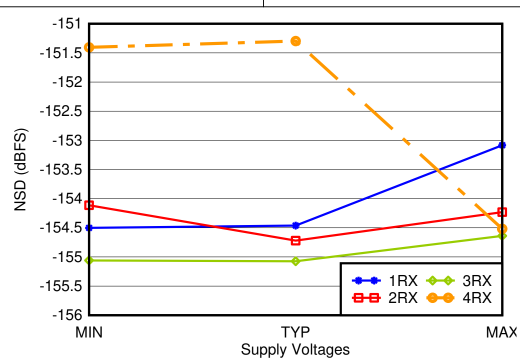
With 4.9 GHz matching

図 7-412. RX Non-HD2/3 vs DSA Setting at 4.9 GHz



With 4.9 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-413. RX IMD3 vs Supply and Channel at 4.9 GHz

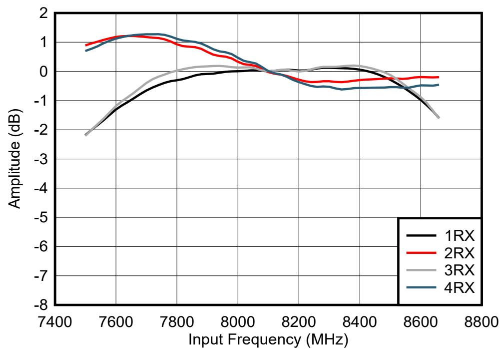


With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 7-414. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

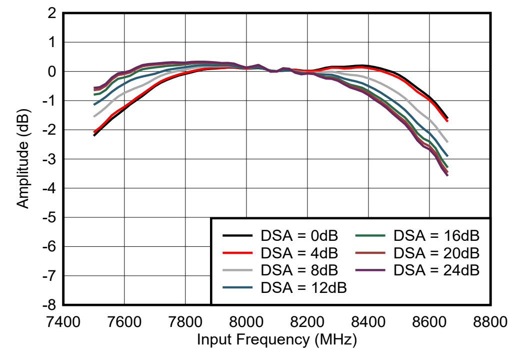
7.12.13 RX Typical Characteristics at 8.1 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 8.1 GHz matching.



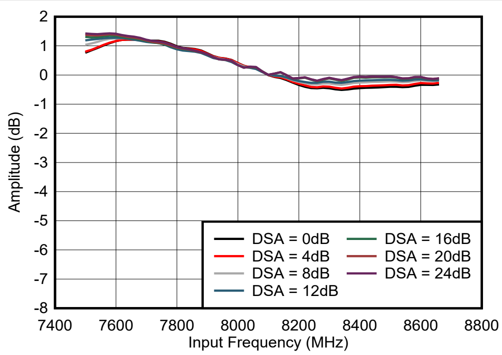
Normalized to 8.11GHz

図 7-415. RX Amplitude vs Frequency and Channel



1RX and 3RX, Normalized to 8.11 GHz

図 7-416. RX Amplitude vs Frequency and DSA Setting



2RX and 4RX, Normalized to 8.11 GHz

図 7-417. RX Amplitude vs Frequency and DSA Setting

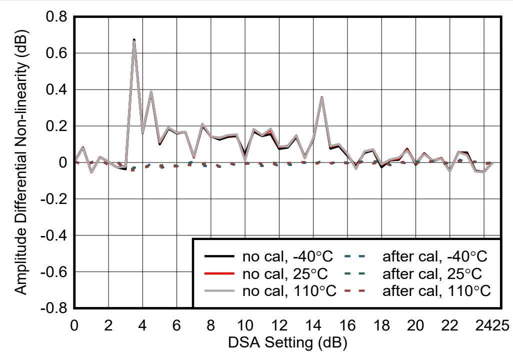


図 7-418. RX Amplitude Differential Nonlinearity at 8.11 GHz

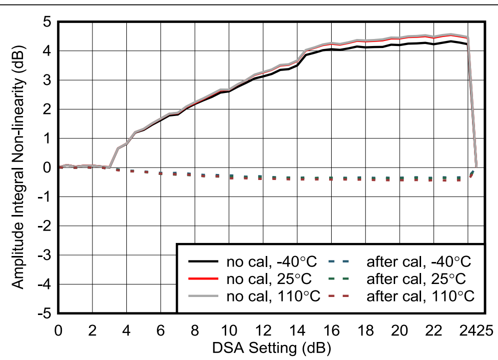


図 7-419. RX Amplitude Integrated Nonlinearity at 8.11 GHz

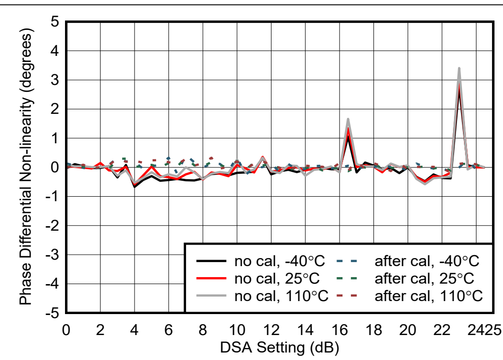


図 7-420. RX Phase Differential Nonlinearity at 8.11 GHz

7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 8.1 GHz matching.

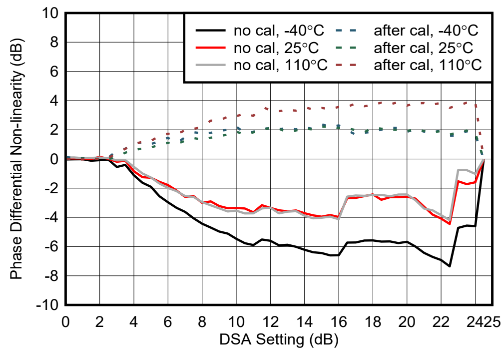
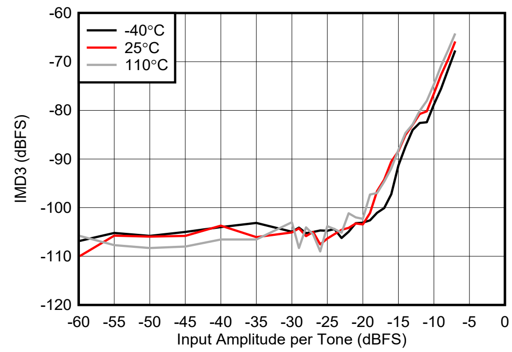
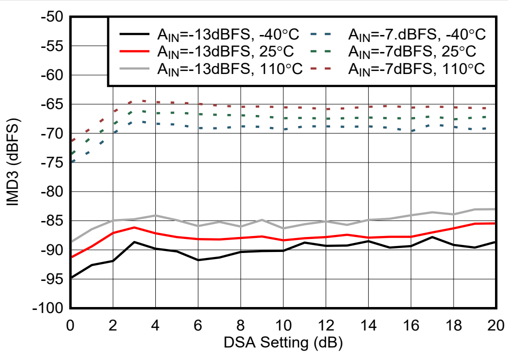


図 7-421. RX Phase Differential Nonlinearity at 8.11 GHz



50MHz tone spacing

図 7-422. RX IMD3 vs Input Amplitude at 8.11 GHz



50 MHz tone spacing

図 7-423. RX IMD3 vs DSA Setting at 8.11 GHz

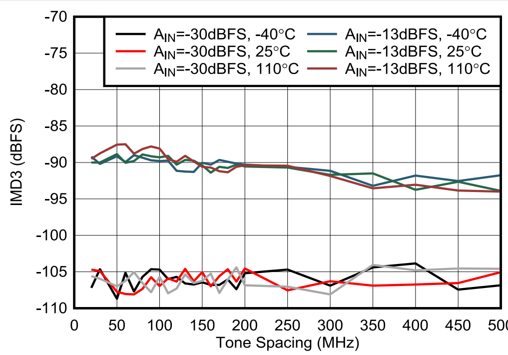


図 7-424. RX IMD3 vs Tone Spacing at 8.11 GHz

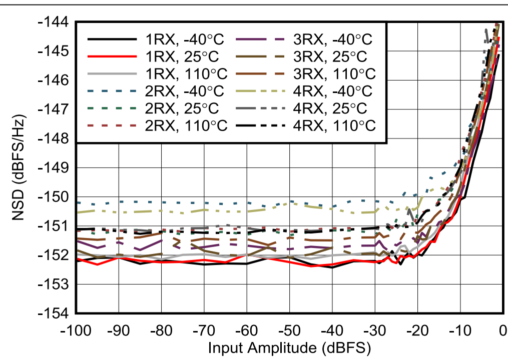


図 7-425. RX NSD vs Digital Amplitude at 8.11 GHz

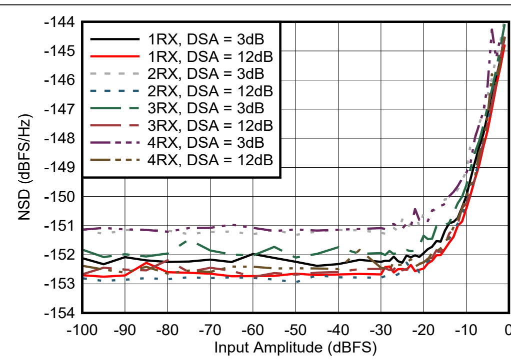


図 7-426. RX NSD vs Digital Amplitude at 8.11 GHz

7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 8.1 GHz matching.

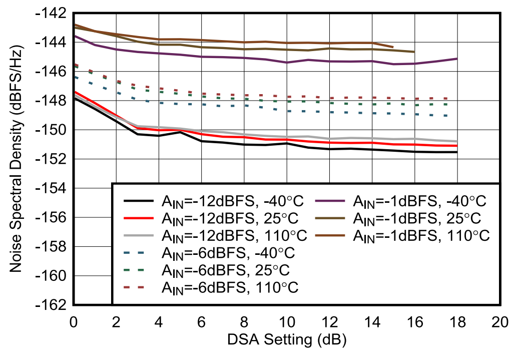
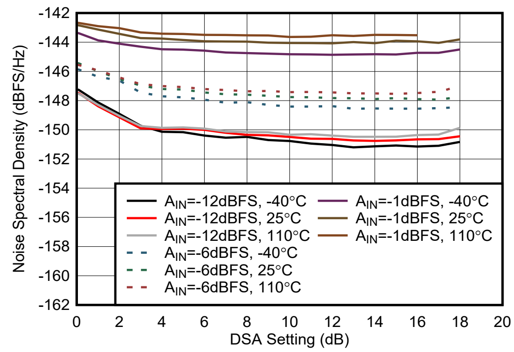


図 7-427. RX NSD vs DSA Setting at 8.11 GHz



External clock mode

図 7-428. RX NSD vs DSA Setting at 8.11 GHz

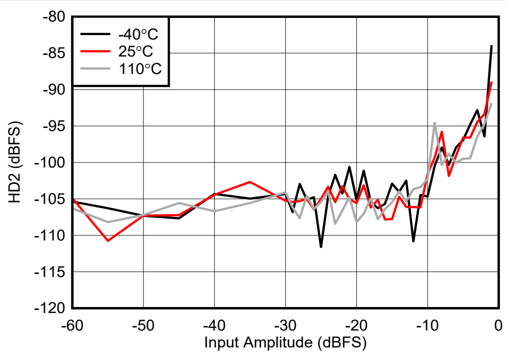


図 7-429. RX HD2 vs Digital Amplitude at 8.11 GHz

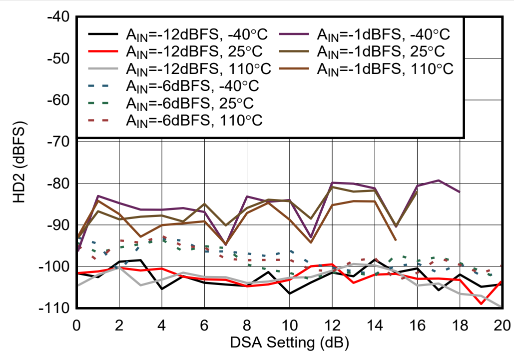


図 7-430. RX HD2 vs DSA Setting at 8.11 GHz

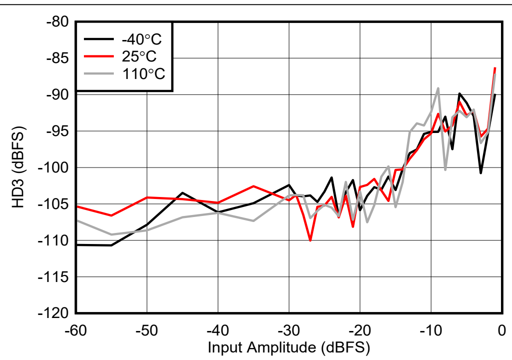


図 7-431. RX HD3 vs Digital Amplitude at 8.11 GHz

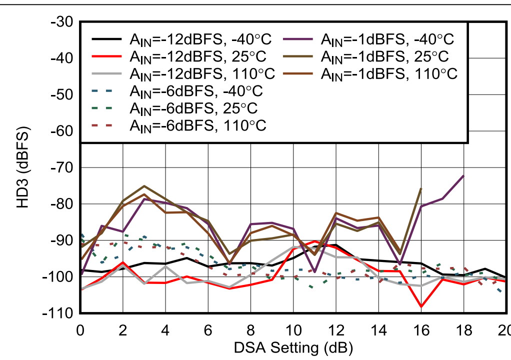
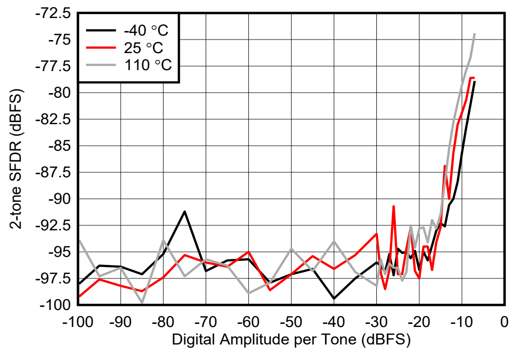


図 7-432. RX HD3 vs DSA Setting at 8.11 GHz

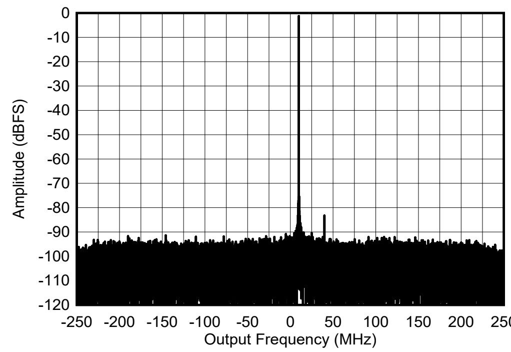
7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 8.1 GHz matching.



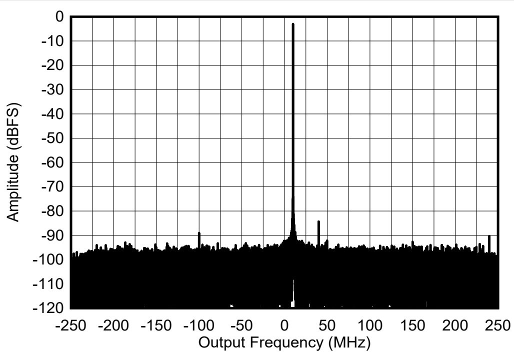
50MHz Tone Spacing

図 7-433. RX 2-tone SFDR vs Digital Amplitude at 8.11 GHz



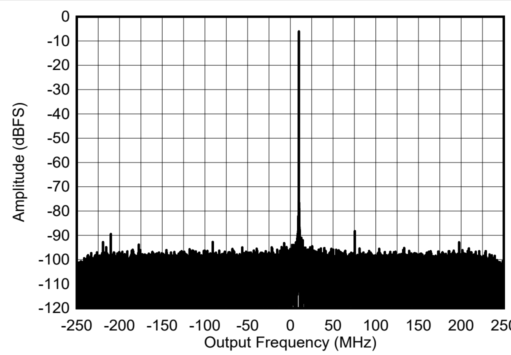
External clock mode

図 7-434. RX Single Tone Output FFT at 8.11 GHz, -1 dBFS



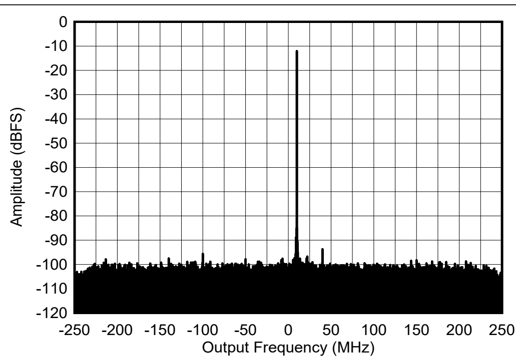
External clock mode

図 7-435. RX Single Tone Output FFT at 8.11 GHz, -3 dBFS



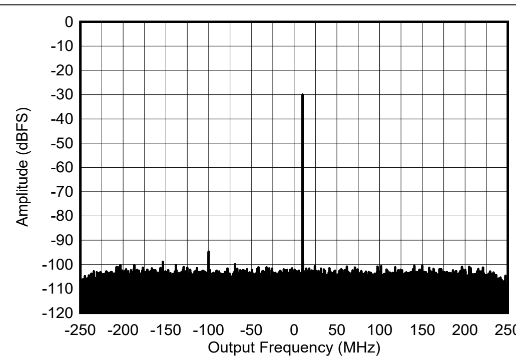
External clock mode

図 7-436. RX Single Tone Output FFT at 8.11 GHz, -6 dBFS



External clock mode

図 7-437. RX Single Tone Output FFT at 8.11 GHz, -12 dBFS

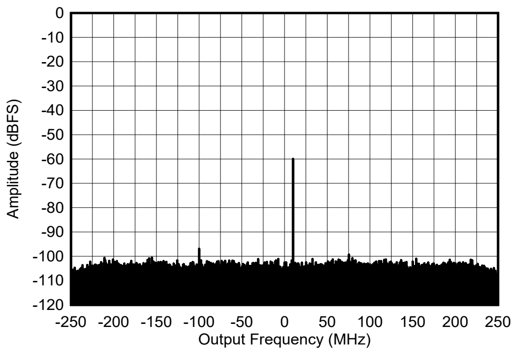


External clock mode

図 7-438. RX Single Tone Output FFT at 8.11 GHz, -30 dBFS

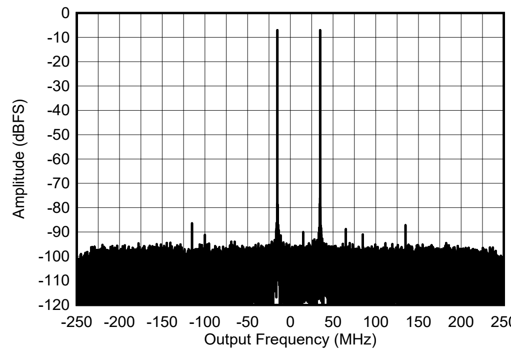
7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 8.1 GHz matching.



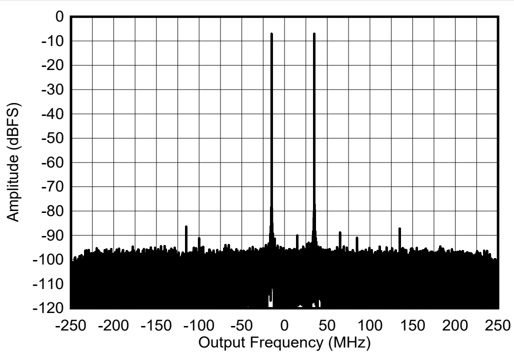
External clock mode

図 7-439. RX Single Tone Output FFT at 8.11 GHz, -60 dBFS



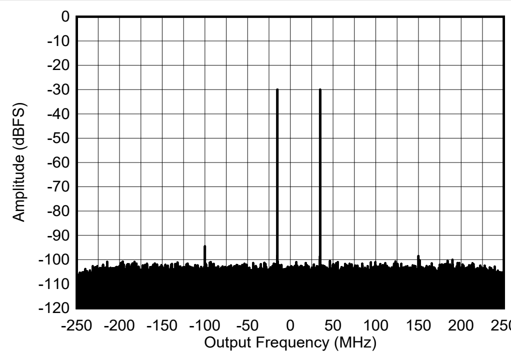
External clock mode, -7 dBFS each tone

図 7-440. RX Dual Tone Output FFT at 8.11 GHz



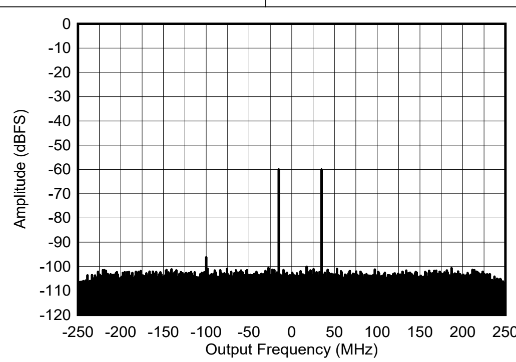
External clock mode, -12 dBFS each tone

図 7-441. RX Dual Tone Output FFT at 8.11 GHz



External clock mode, -30 dBFS each tone

図 7-442. RX Dual Tone Output FFT at 8.11 GHz

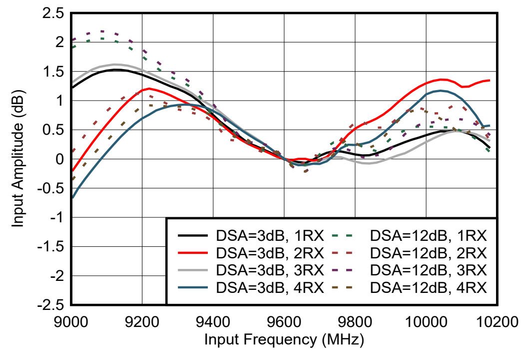


External clock mode, -60 dBFS each tone

図 7-443. RX Dual Tone Output FFT at 8.11 GHz

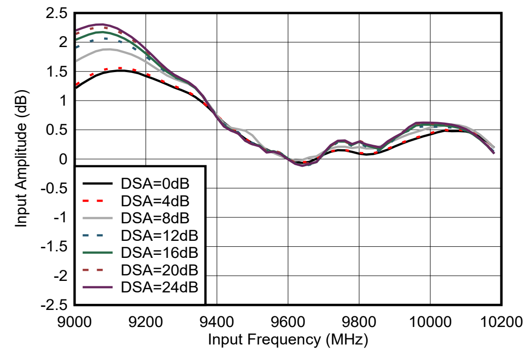
7.12.14 RX Typical Characteristics at 9.6 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 9.6 GHz matching.



Normalized to 9.6 GHzRX Input Amplitude vs Frequency at 9.6

図 7-444. RX Input Amplitude vs Frequency



Normalized to 9.6 GHz

図 7-445. GHz

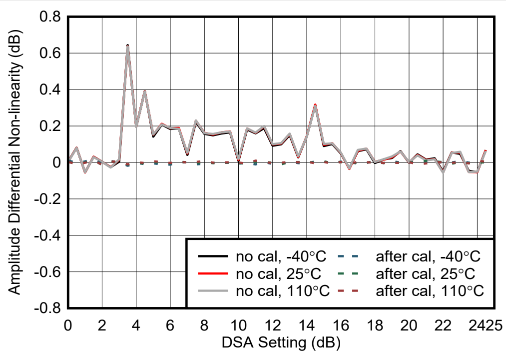


図 7-446. RX Amplitude Differential Non-linearity at 9.6 GHz

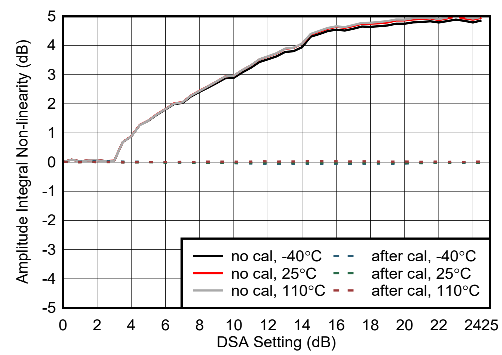


図 7-447. RX Amplitude Integrated Non-linearity at 9.6 GHz

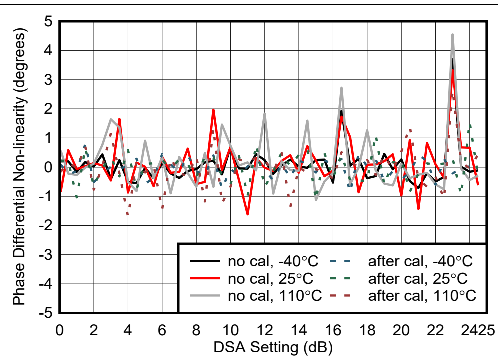


図 7-448. RX Phase Differential Non-linearity at 9.6 GHz

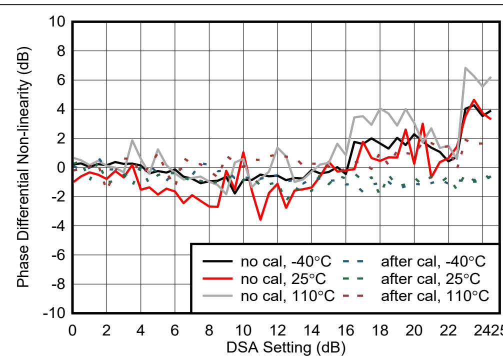


図 7-449. RX Phase Integrated Non-linearity at 9.6 GHz

7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 9.6 GHz matching.

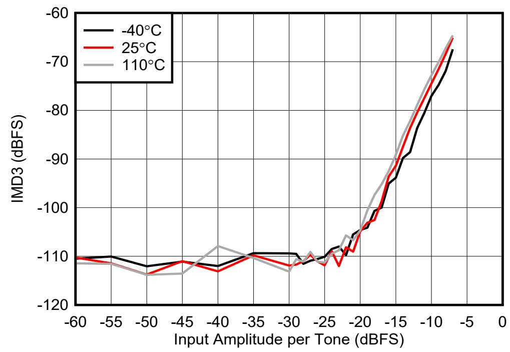
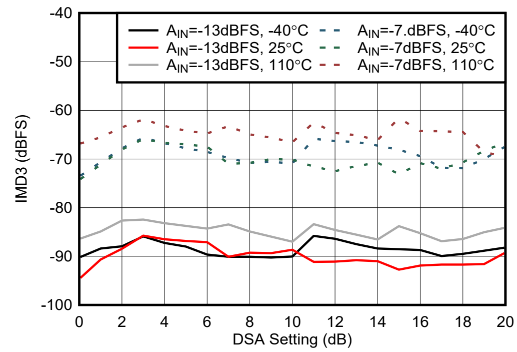
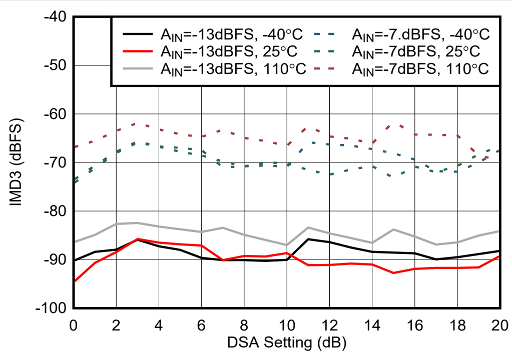


図 7-450. RX IMD3 vs Digital Amplitude at 9.6 GHz



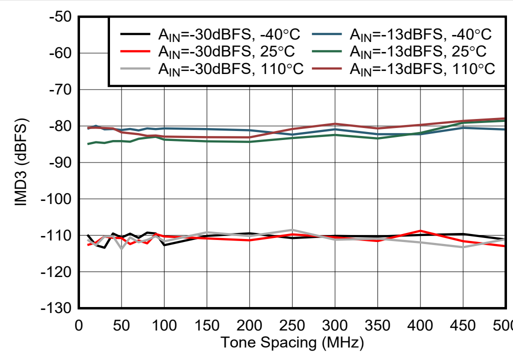
50 MHz tone spacing

図 7-451. RX IMD3 vs DSA Setting at 9.6 GHz



50 MHz tone spacing

図 7-452. RX IMD3 vs DSA Setting at 9.6 GHz



50 MHz tone spacing

図 7-453. RX IMD3 vs Tone Spacing at 9.6 GHz

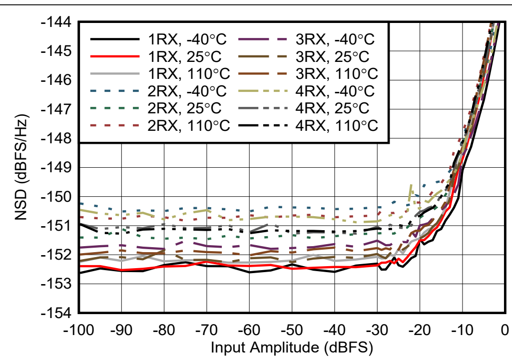


図 7-454. RX NSD vs Digital Amplitude at 9.6 GHz

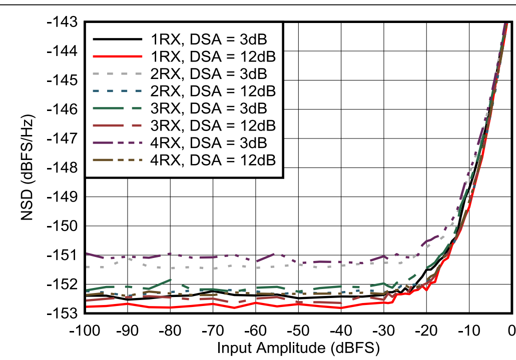


図 7-455. RX NSD vs Digital Amplitude at 9.6 GHz

7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 9.6 GHz matching.

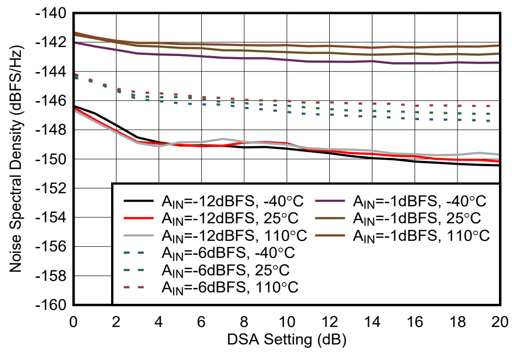


図 7-456. RX NSD vs DSA Setting at 9.6 GHz

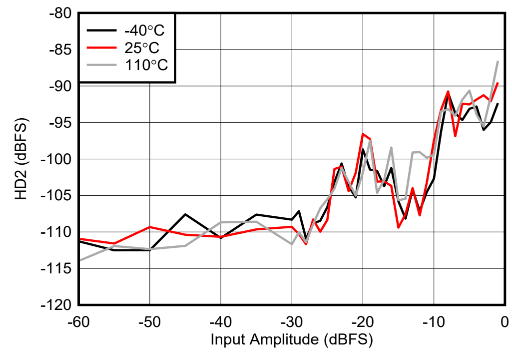


図 7-457. RX HD2 vs Digital Level at 9.6 GHz

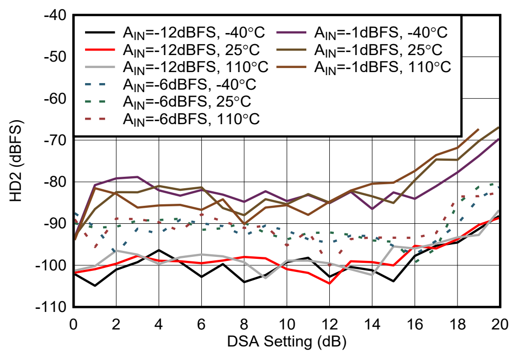


図 7-458. RX HD2 vs DSA Setting at 9.6 GHz

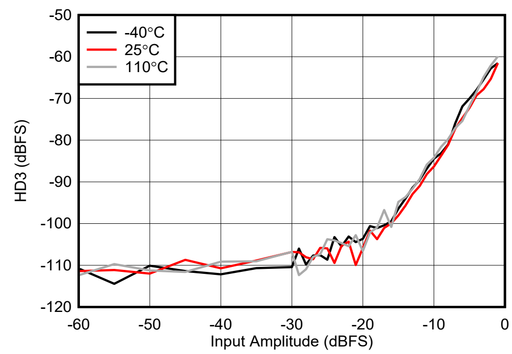


図 7-459. RX HD3 vs Digital Level at 9.6 GHz

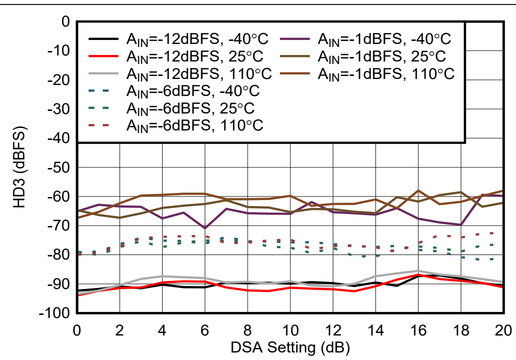
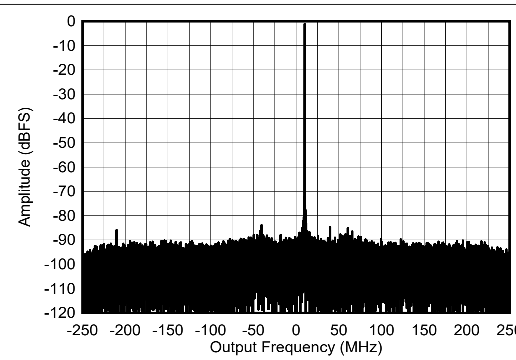


図 7-460. RX HD3 vs DSA Setting at 9.6 GHz

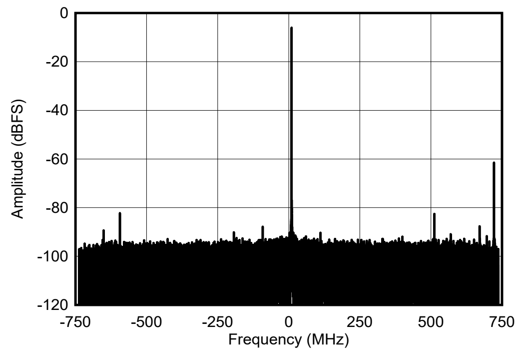


-1 dBFS

図 7-461. RX Single Tone Output FFT at 9.61 GHz

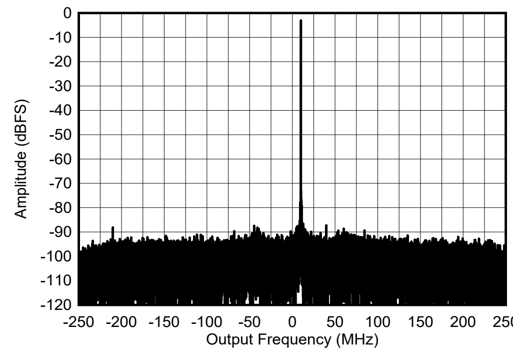
7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 9.6 GHz matching.



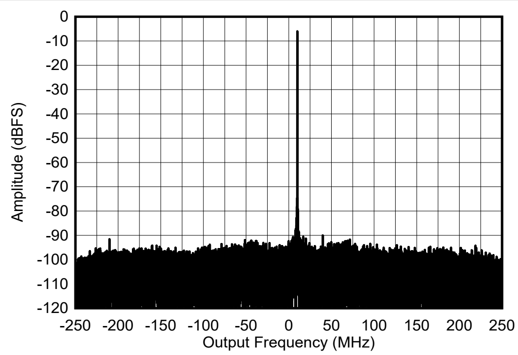
-6 dBFS

図 7-462. RX Single Tone Output FFT at 9.61 GHz



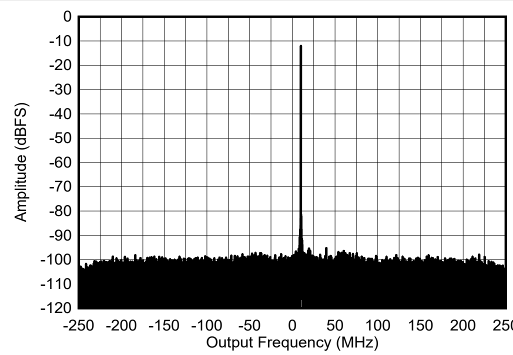
-3 dBFS

図 7-463. RX Single Tone Output FFT at 9.61 GHz



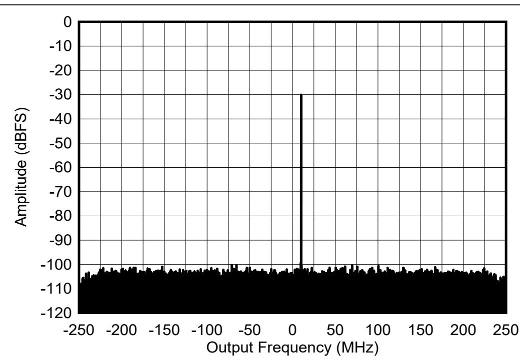
-6 dBFS

図 7-464. RX Single Tone Output FFT at 9.61 GHz



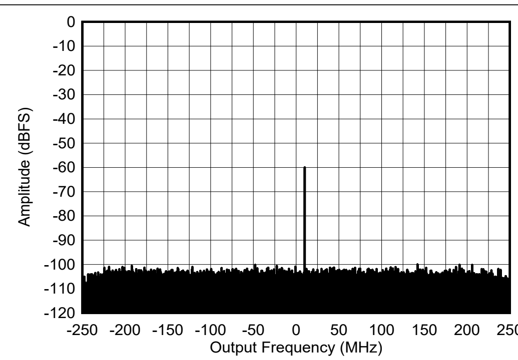
-12 dBFS

図 7-465. RX Single Tone Output FFT at 9.61 GHz



-30 dBFS

図 7-466. RX Single Tone Output FFT at 9.61 GHz

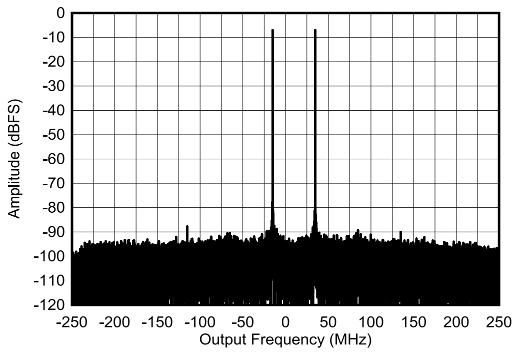


-60 dBFS

図 7-467. RX Single Tone Output FFT at 9.61 GHz

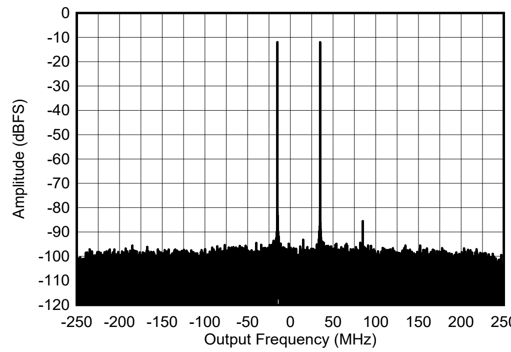
7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2) , External clock mode with f_{CLK} = 11796.48 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB, 9.6 GHz matching.



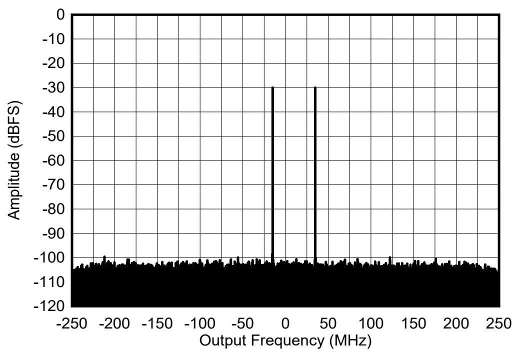
9.585 and 9.635 GHz, -7 dBFS each tone

図 7-468. RX Two Tone Output FFT at 9.61 GHz



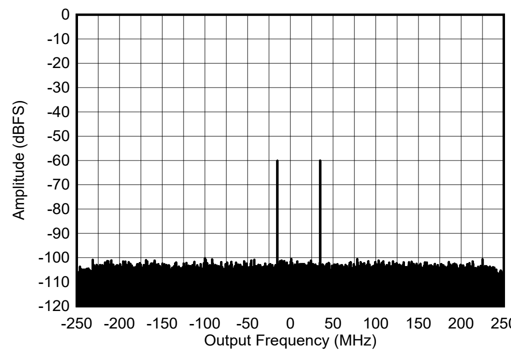
9.585 and 9.635 GHz, -12 dBFS each tone

図 7-469. RX Two Tone Output FFT at 9.61 GHz



9.585 and 9.635 GHz, -30 dBFS each tone

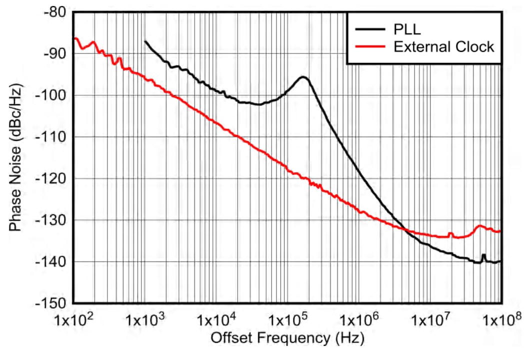
図 7-470. RX Two Tone Output FFT at 9.61 GHz



9.585 and 9.635 GHz, -60 dBFS each tone

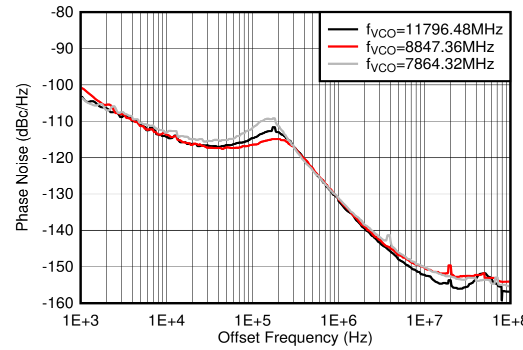
図 7-471. RX Two Tone Output FFT at 9.61 GHz

7.12.15 PLL and Clock Typical Characteristics



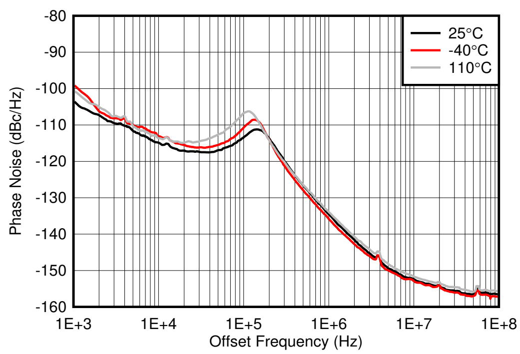
measured at TX output, normalized to 12 GHz by 20 x log10(12GHz/F_{OUT})

図 7-472. Phase Noise vs Offset Frequency for PLL and External Clock at 12 GHz



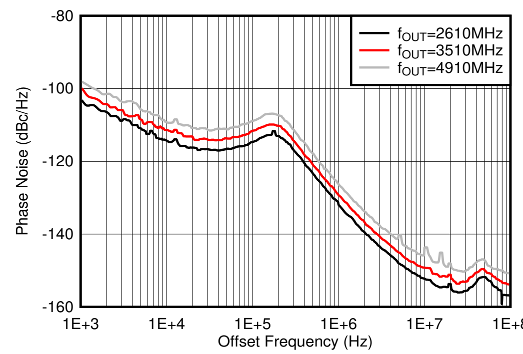
PLL enabled, f_{REF} = 491.52 MSPS, measured at TX output

図 7-473. Phase Noise vs Offset Frequency and f_{VCO} at f_{OUT} = 2610 MHz



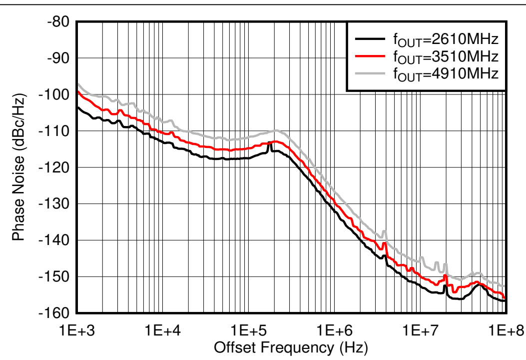
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-474. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



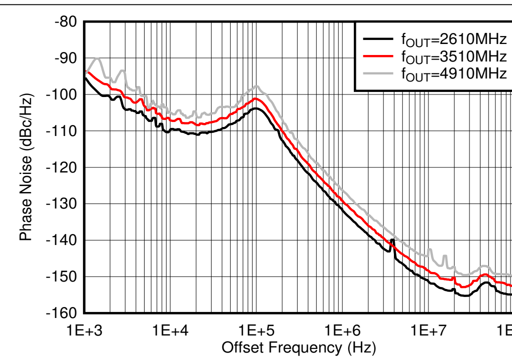
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-475. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



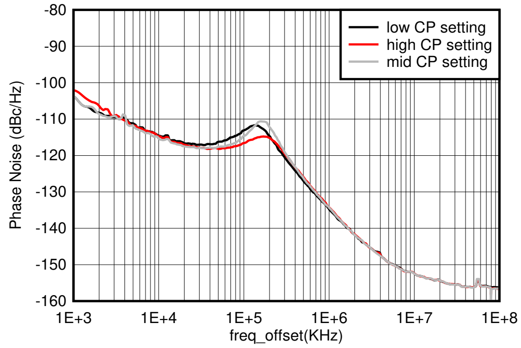
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-476. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



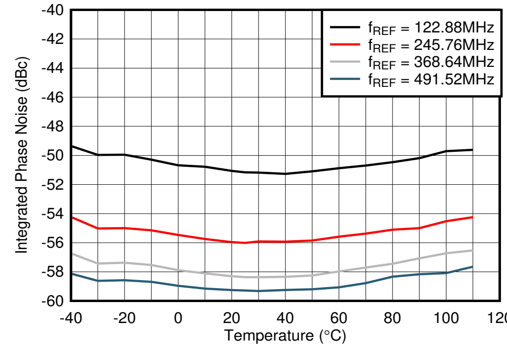
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-477. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



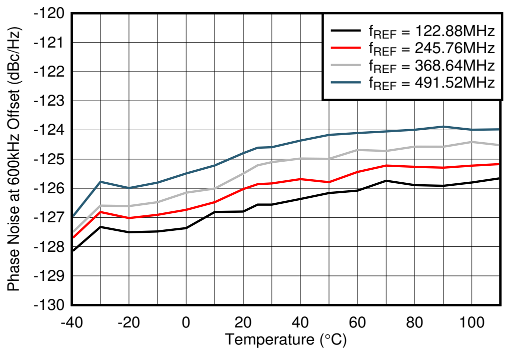
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-478. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at f_{OUT} = 2.6 GHz



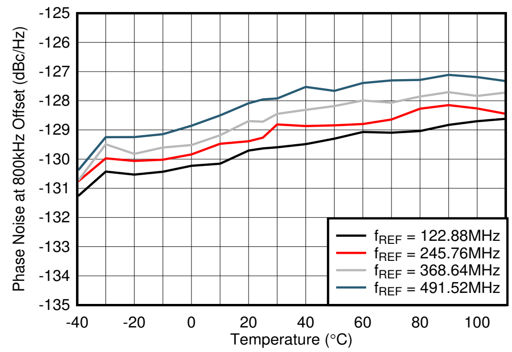
PLL enabled, f_{VCO} = 11796.48 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

図 7-479. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



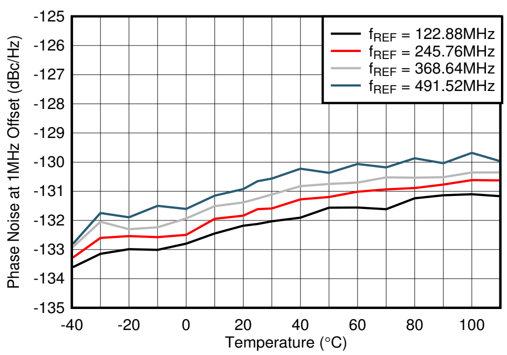
PLL enabled, f_{VCO} = 11796.48 MHz, measured at TX output

図 7-480. Phase Noise for 12-GHz VCO at 600 kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



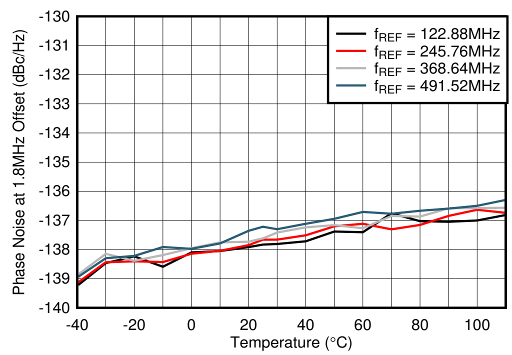
A. PLL enabled, f_{VCO} = 11796.48 MHz, measured at TX output

図 7-481. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



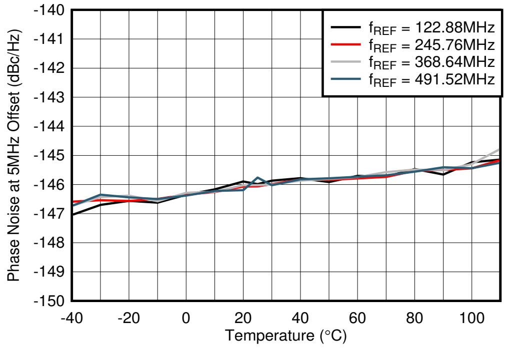
PLL enabled, f_{VCO} = 11796.48 MHz, measured at TX output

図 7-482. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



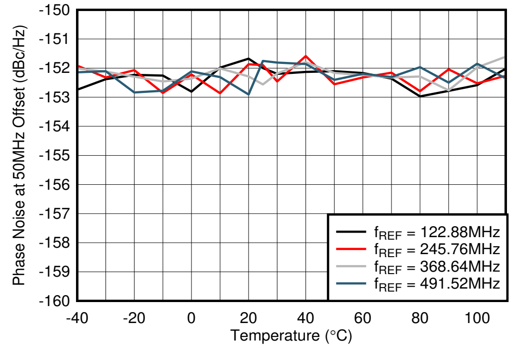
PLL enabled, f_{VCO} = 11796.48 MHz, measured at TX output

図 7-483. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



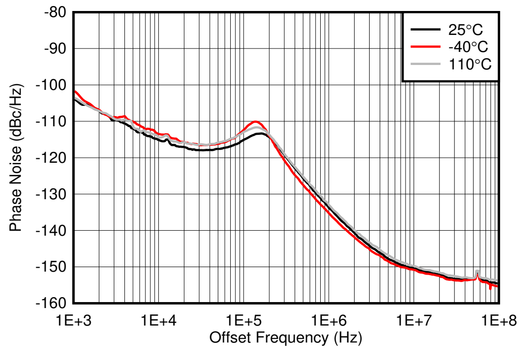
PLL enabled, f_{VCO} = 11796.48 MHz, measured at TX output

図 7-484. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



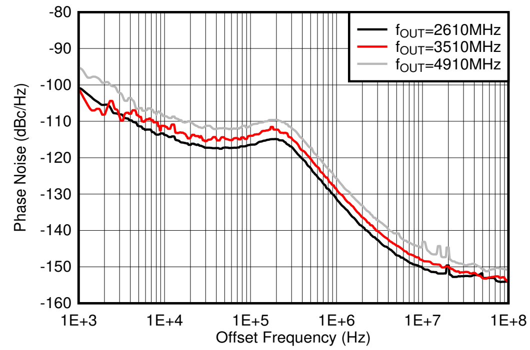
PLL enabled, f_{VCO} = 11796.48 MHz, measured at TX output

図 7-485. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



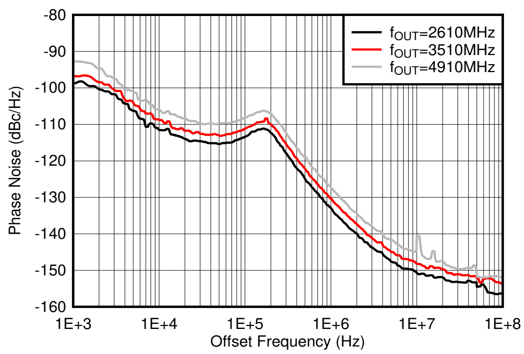
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-486. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



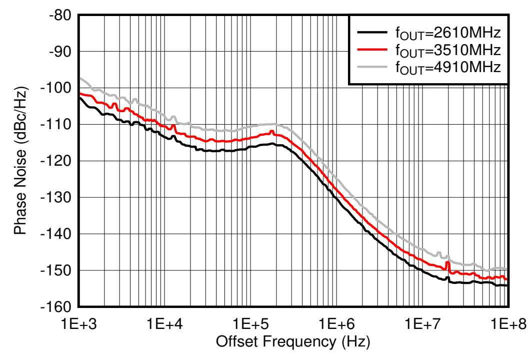
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-487. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



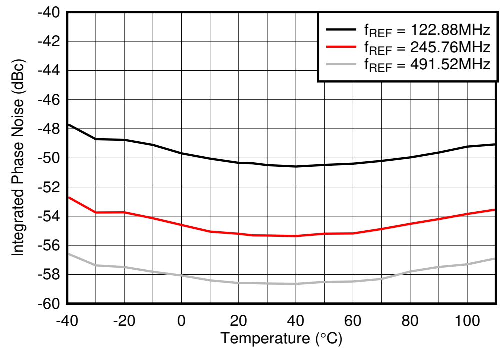
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-488. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



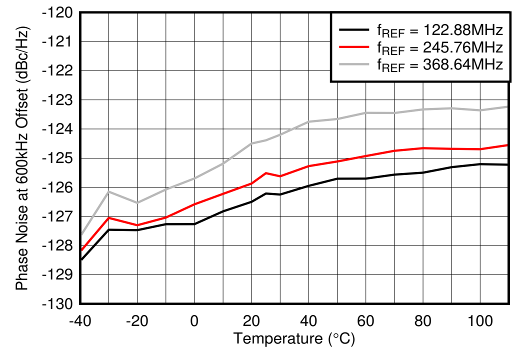
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-489. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



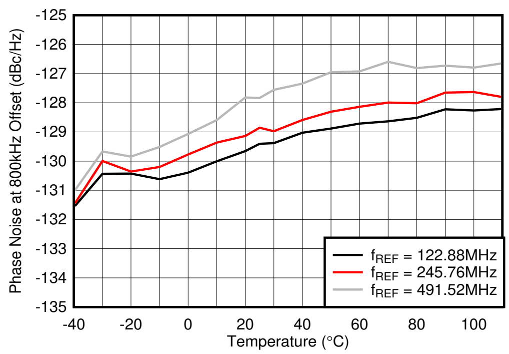
PLL enabled, f_{VCO} = 9830.4 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

図 7-490. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



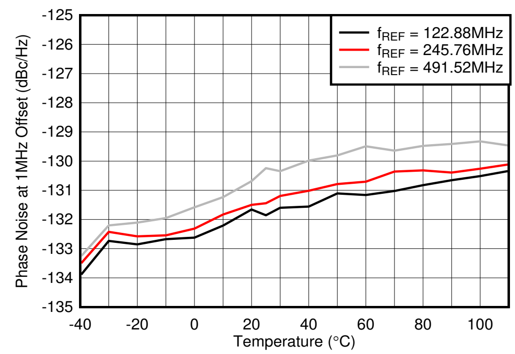
PLL enabled, f_{VCO} = 9830.4 MHz, measured at TX output

図 7-491. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



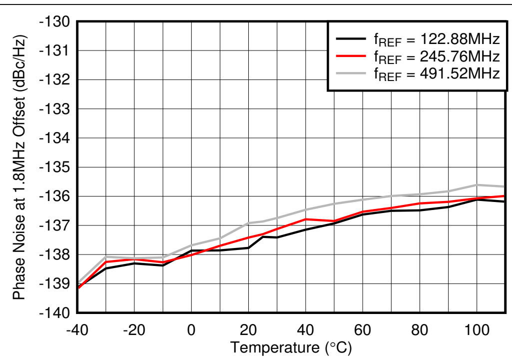
PLL enabled, f_{VCO} = 9830.4 MHz, measured at TX output

図 7-492. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



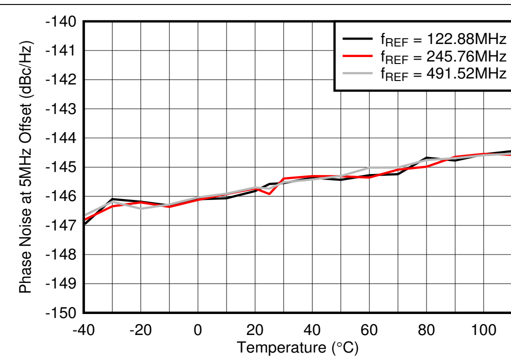
PLL enabled, f_{VCO} = 9830.4 MHz, measured at TX output

図 7-493. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



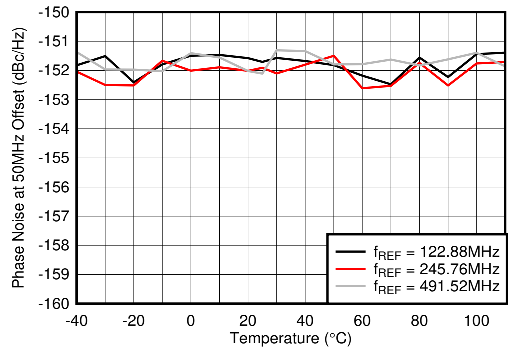
PLL enabled, f_{VCO} = 9830.4 MHz, measured at TX output

図 7-494. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



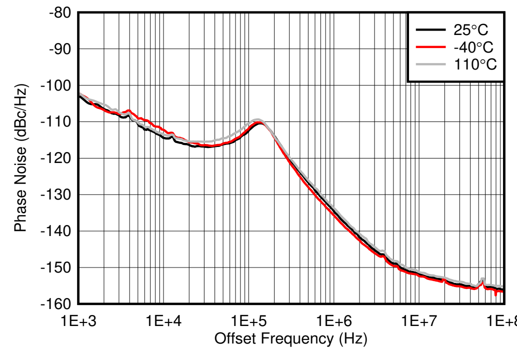
PLL enabled, f_{VCO} = 9830.4 MHz, measured at TX output

図 7-495. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



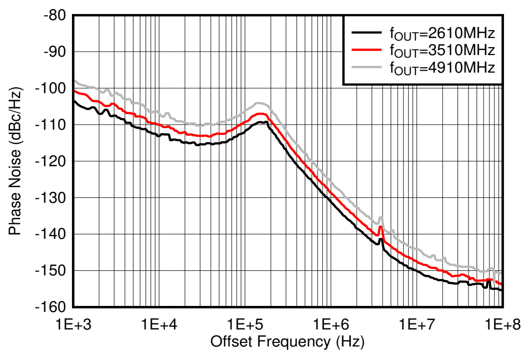
PLL enabled, f_{VCO} = 9830.4 MHz, measured at TX output

図 7-496. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



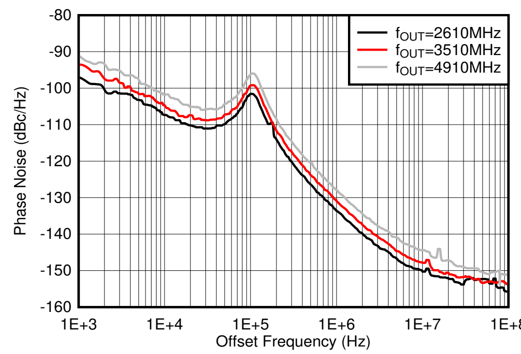
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-497. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



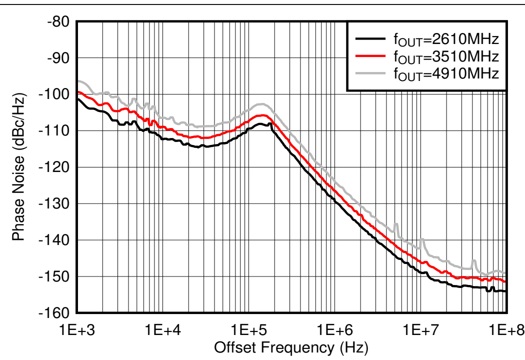
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-498. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



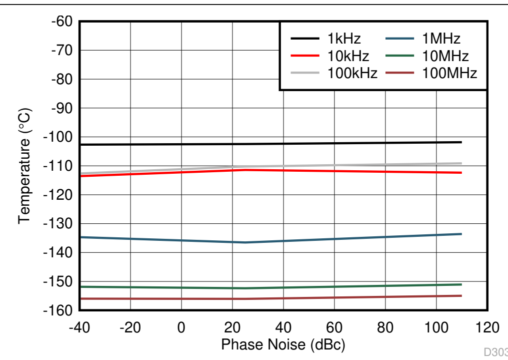
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-499. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



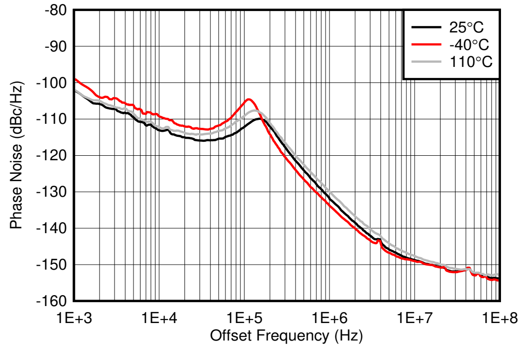
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-500. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, minimum LPF BW, measured at TX output

図 7-501. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 7864.32 MHz, f_{REF} = 491.52 MSPS, measured at TX output

図 7-502. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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8.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7951IABJ	Active	Production	FCBGA (ABJ) | 400	90 | JEDEC TRAY (5+1)	Yes	SNAGCU | SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7951I
AFE7951IABJ.B	Active	Production	FCBGA (ABJ) | 400	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7951I
AFE7951IALK	Active	Production	FCBGA (ALK) | 400	90 | JEDEC TRAY (5+1)	No	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7951 SNPB
AFE7951IALK.B	Active	Production	FCBGA (ALK) | 400	90 | JEDEC TRAY (5+1)	No	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7951 SNPB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

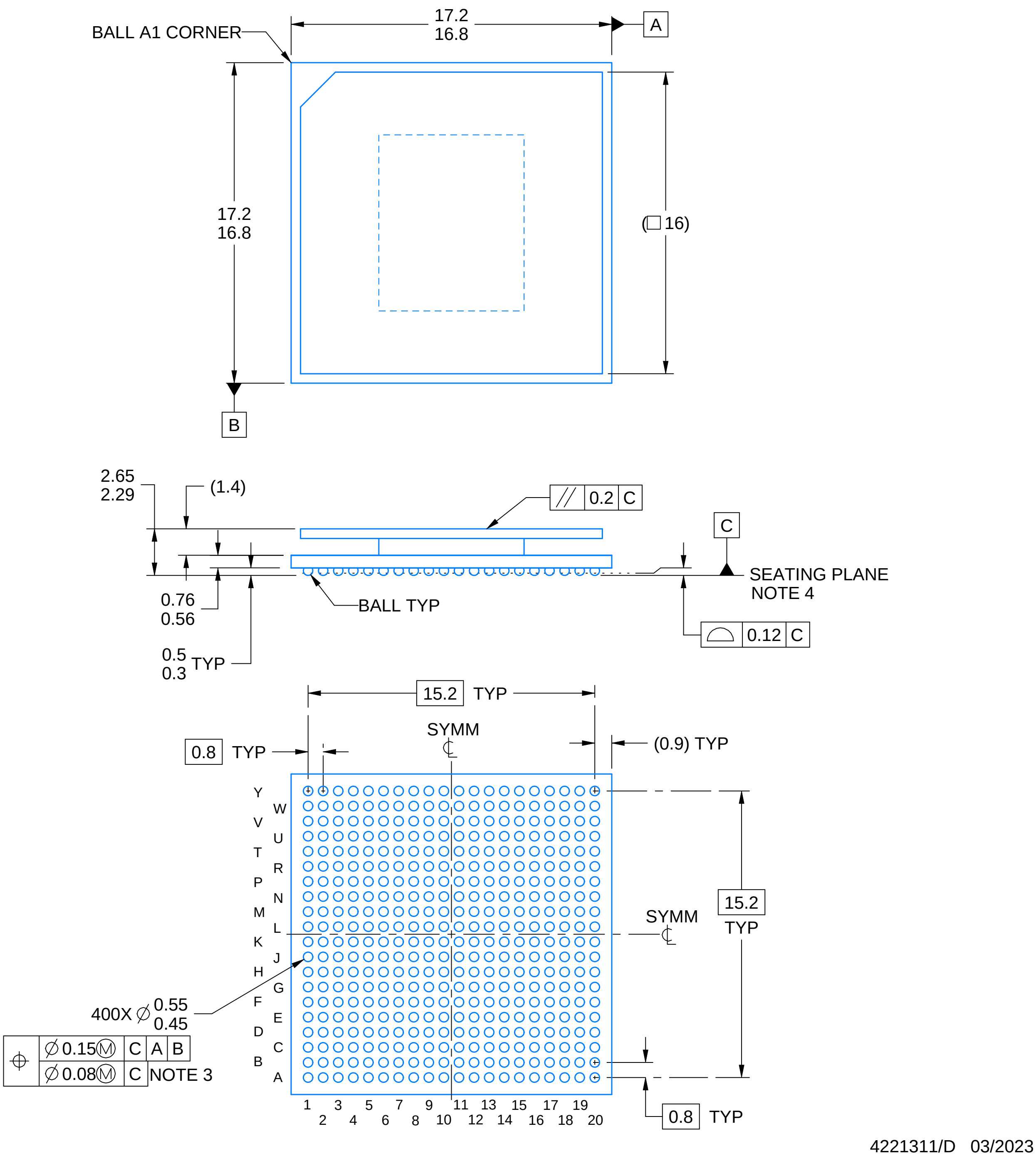
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

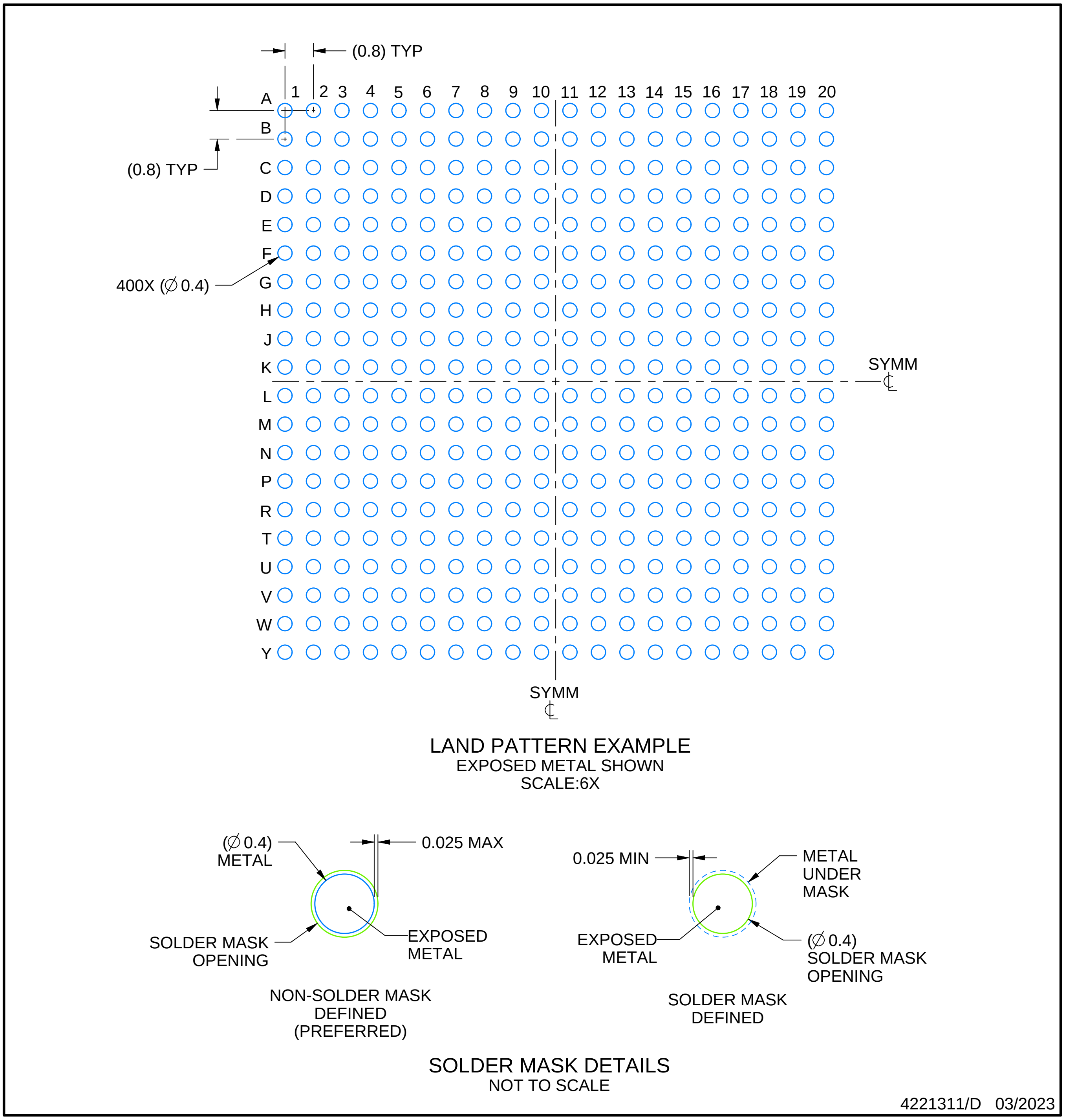
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



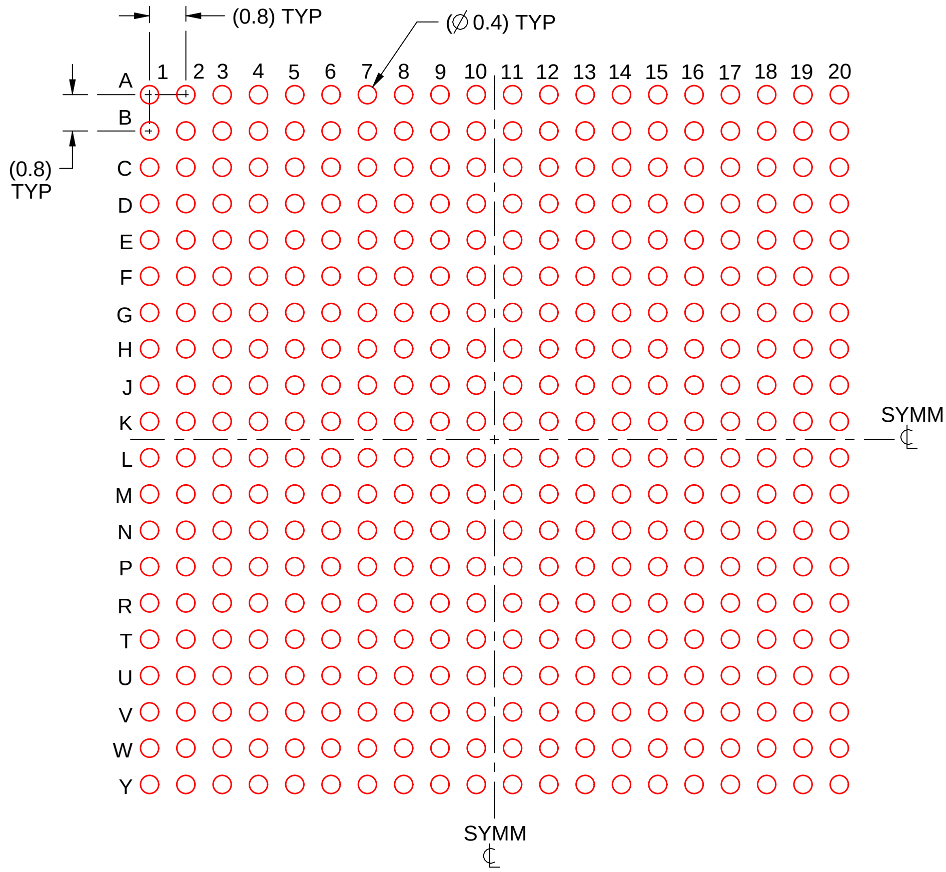
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

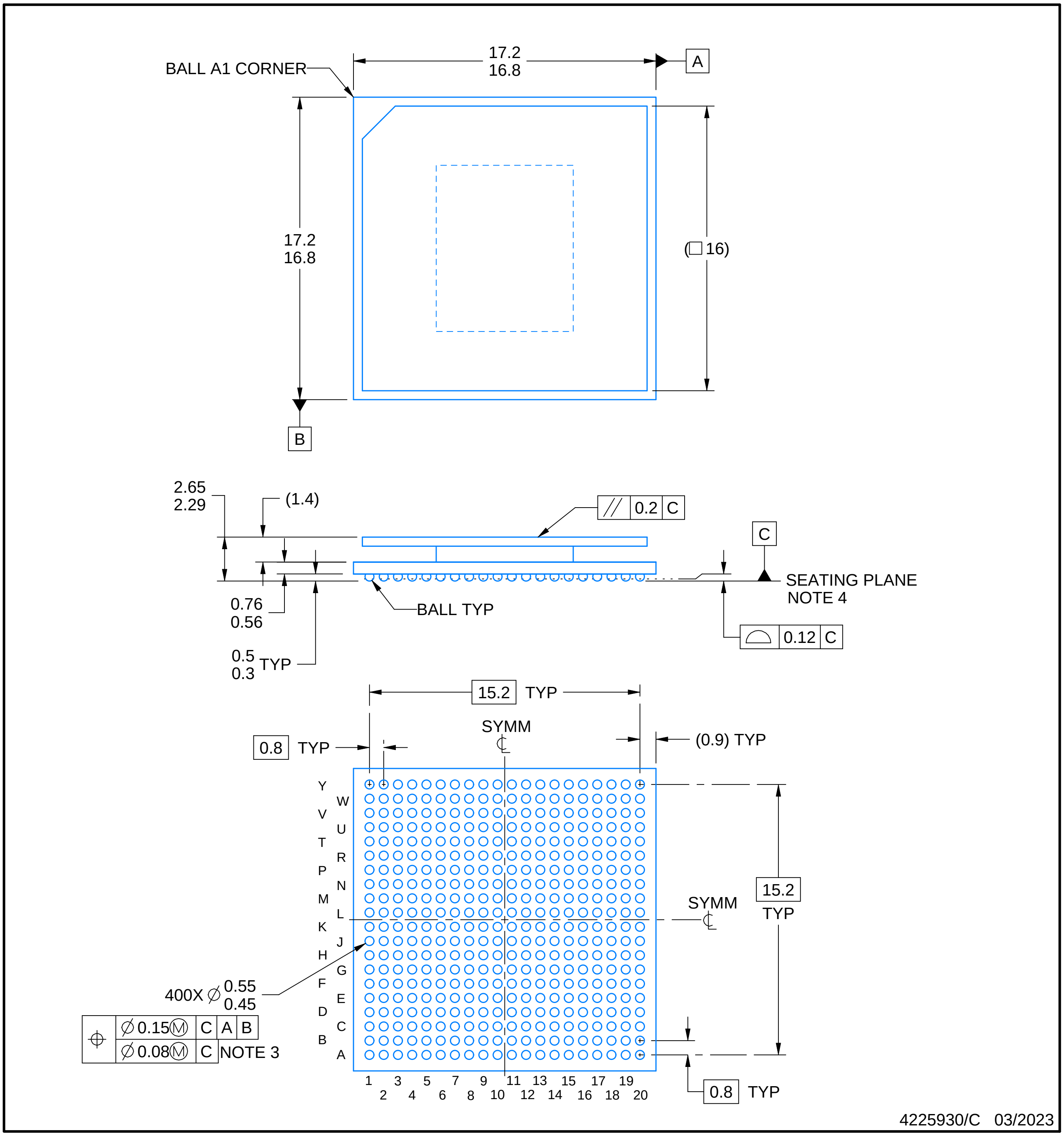


SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4221311/D 03/2023

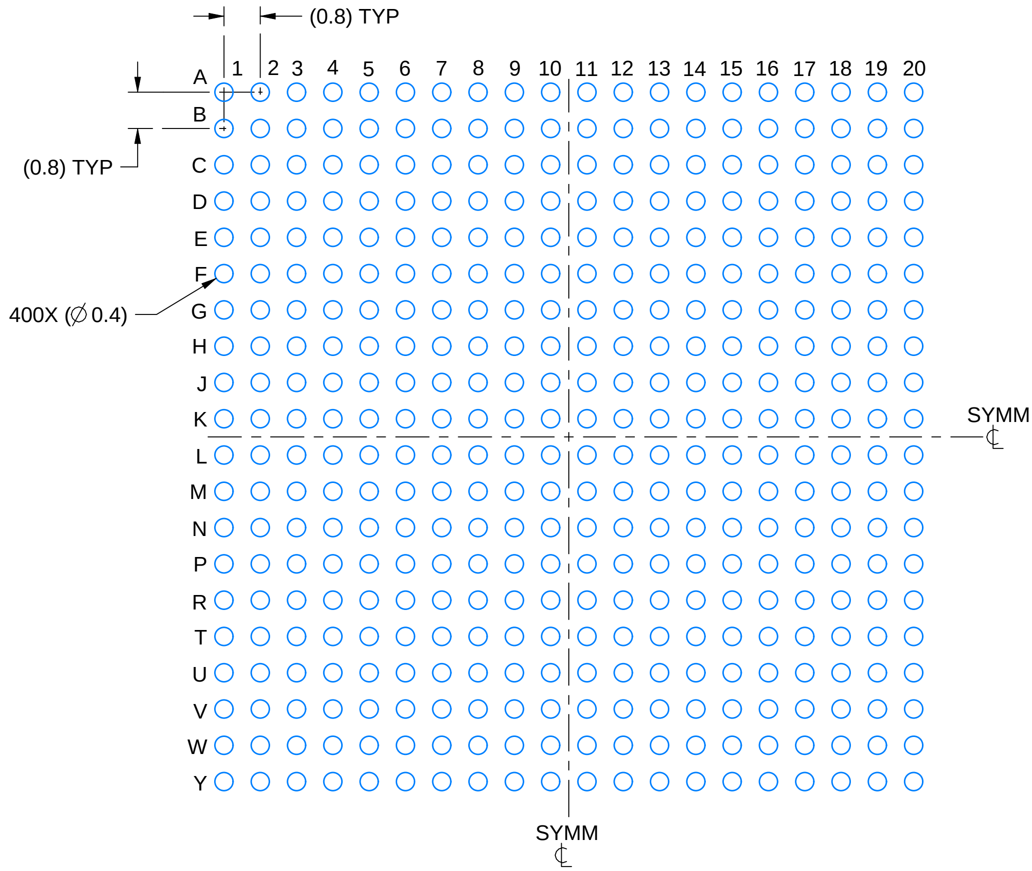
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

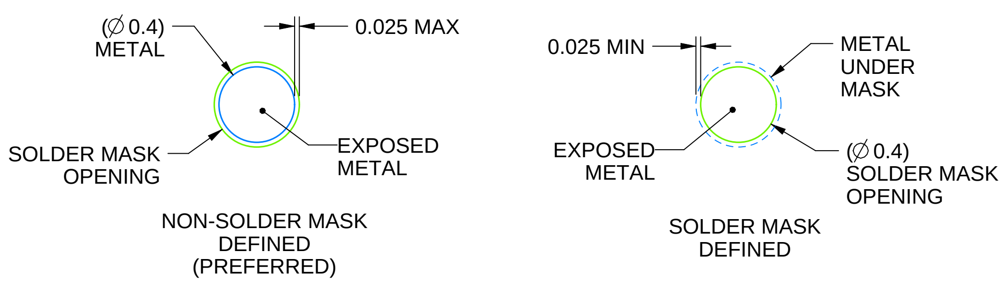


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

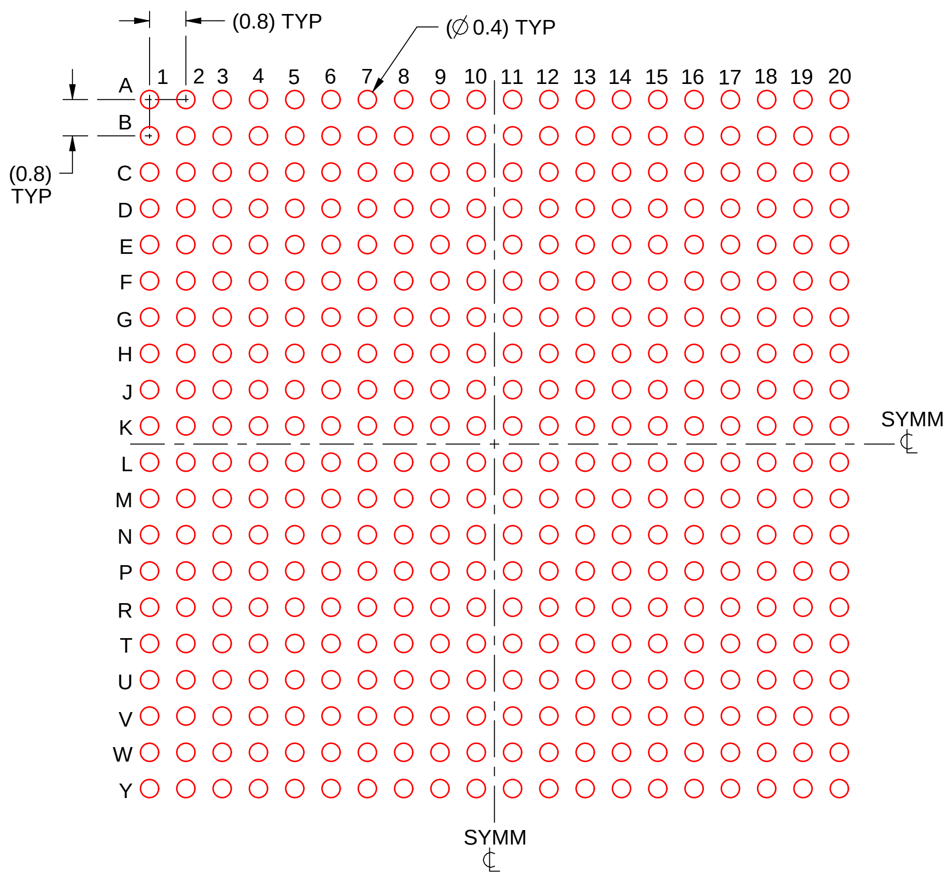


SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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