

# AFEx82H1 16 ビットおよび 14 ビット、低消費電力 D/A コンバータ (DAC)、HART® モデム、電圧リファレンス、プロセス制御用診断 ADC 内蔵

## 1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 低い静止電流：180μA (代表値)
- HART® 準拠の物理レイヤ モデム
  - TX 信号の振幅をプログラム可能
  - RX 復調器とバンドパス フィルタ
- 16 ビットまたは 14 ビット、モノリシック高性能 DAC
  - DAC 出力範囲：0V ~ 2.5V
  - デジタル DAC スループート制御
  - 16 ビットでの INL、4LSB
  - 40°C ~ +125°C の範囲で TUE が 0.07% FSR (最大値)
- 高度な診断向け、12 ビット、3.84kSPS の ADC (A/D コンバータ)
- 1.25V 基準電圧 (最大 10ppm/°C) を内蔵
- クロック出力付き内蔵 1.2288MHz 発振器
- デジタル インターフェイス
  - シリアル ペリフェラル インターフェイス (SPI)：DAC および HART 用の共有バス
  - UART (Universal Asynchronous Receiver-Transmitter)：DAC および HART 用の共有バス
  - 両方：DAC 用の SPI と HART 用の UART
- フォルト検出：CRC ビット エラー チェック、ウィンドウ付きウォッチドッグ タイマ、診断 ADC
- 広い動作温度範囲 -55°C ~ +125°C

## 2 アプリケーション

- プロセス制御および産業用オートメーション
- PLC または DCS I/O モジュール
- 3 線式および 4 線式のトランスミッタ
- 4mA ~ 20mA のループ電源アプリケーション

## 3 概要

16 ビットの AFE882H1 および 14 ビットの AFE782H1 (AFEx82H1) は、HART 対応のプロセス制御および産業用オートメーション アプリケーション向けに設計された高集積、高精度、超低消費電力の電圧出力 DAC です。

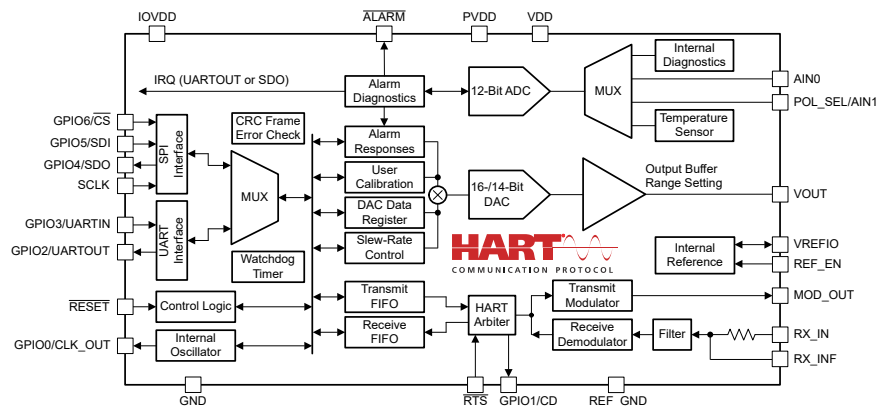
AFEx82H1 デバイスには、4mA から 20mA の 3 線式または 4 線式センサ トランスミッタまたはアナログ出力モジュールを設計するために必要な構成要素のほとんどが含まれています。これらのデバイスには、高精度な DAC に加えて、HART® 準拠 FSK モデム、10ppm/°C の電圧リファレンス、および診断用 A/D コンバータ (ADC) が内蔵されています。内在的および機能安全上の問題に対応するには、外部の電圧電流変換と、電源のレギュレーションが必要です。

内蔵の診断 ADC は複数の内部ノードに多重化されており、自動的な自己ヘルス チェックを可能にしています。このチェックにより、内蔵のバイアス源や電源レギュレータ、電圧リファレンス、DAC 出力、ダイ温度に関するエラーや故障を検出でき、さらにオプションとして外部電圧源の問題も検出できます。診断用 ADC、CRC フレーム エラー チェック、あるいはウィンドウ付きのウォッチドッグ タイマから、いずれかの障害が検出された場合、本デバイスは (オプションとして) 割り込みの発行、あるいはユーザー指定のフェイルセーフ状態への遷移、またはその両方を開始できます。

### 製品情報

部品番号	分解能	パッケージ <sup>(1)</sup>
AFE782H1	14 ビット	RRU (UQFN, 24) 4.00 mm × 4.00mm
AFE882H1	16 ビット	

(1) 詳細については、[セクション 11](#) を参照してください。



機能ブロック図



このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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## 4 Pin Configuration and Functions

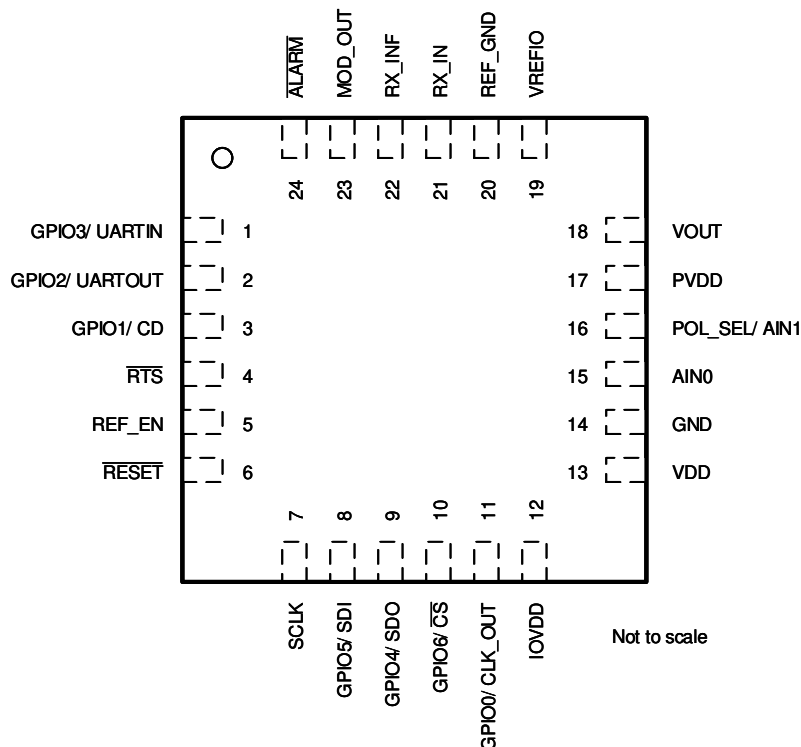


図 4-1. RRU Package, 24-pin UQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
AIN0	15	AI	ADC input voltage. The input range is 0 V to 2 × VREF.
ALARM	24	DO	Alarm notification pin, open drain, active low. When alarm condition is asserted, this pin is held to logic low; otherwise, this pin is in a high-impedance state (Hi-Z).
GND	14	P	Digital and analog ground. Ground reference point for all circuitry on the device.
GPIO0/ CLK_OUT	11	DO/DI	General-purpose input/output (GPIO) pin. Can be configured as a clock output for the 1.2288-MHz internal clock or as a timer. In Hi-Z if not driven. An external pullup or pulldown resistor is required.
GPIO1/ CD	3	DO/DI	General-purpose input/output (GPIO) pin. Configured as a carrier detect output at power up. A logic high on this pin indicates a valid carrier is present. In Hi-Z if not driven. An external pullup or pulldown resistor is required.
GPIO2/ UARTOUT	2	DO/DI	General-purpose input/output (GPIO) pin. Configured as UART data output at power up. This pin can be configured to function as IRQ pin in SPI only mode. In Hi-Z if not driven. An external pullup or pulldown resistor is required.
GPIO3/ UARTIN	1	DI/DO	General-purpose input/output (GPIO) pin. Configured as UART data input at power up. Connect to IOVDD or logic high if not used. An external pullup or pulldown resistor is required.
GPIO4/ SDO	9	DO/DI	General-purpose input/output (GPIO) pin. Can be configured as an SPI data output in SPI mode. Data are output on the rising edge of SCLK when $\overline{CS}$ is low. Interrupt request (IRQ) pin in the UART break mode (UBM). The output is in Hi-Z at power up and must be enabled in the CONFIG register. An external pullup or pulldown resistor is required.
GPIO5/ SDI	8	DI/DO	General-purpose input/output (GPIO) pin. Configured as an SPI data input at power up. Data are clocked into the 24-bit input shift register on the falling edge of the serial clock input. SDI is a Schmitt-trigger logic input. An external pullup or pulldown resistor is required.
GPIO6/ CS	10	DI/DO	General-purpose input/output (GPIO) pin. Configured as an SPI chip-select input at power up. Data bits are clocked into the serial shift register when $\overline{CS}$ is low. When $\overline{CS}$ is high, SDO is in Hi-Z and data on SDI are ignored. An external pullup or pulldown resistor is required.

表 4-1. Pin Functions (続き)

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IOVDD	12	P	Interface supply. Supply voltage for digital input and output circuitry. This voltage sets the logical thresholds for the digital interfaces.
MOD_OUT	23	AO	FSK output sinusoid. Maximum supported parallel load capacitance is 2 nF.
POL_SEL/ AIN1	16	DI/AI	ADC input voltage if SPECIAL_CFG.AIN1_ENB bit is set to 1. The input range is 0 V to 2 × VREF. Otherwise, this pin acts as ALMV_POL, which sets the polarity of the VOUT alarm voltage.
PVDD	17	P	Power supply for the internal low-dropout regulator (LDO), ADC input and VOUT DAC output.
REF_EN	5	DI	Internal VREF enable input. A logic high on this pin enables the internal VREF and the VREFIO pin outputs 1.25 V. A logic low on this pin disables the internal VREF and the external 1.25-V reference is required at the VREFIO pin.
REF_GND	20	P	GND reference for VREFIO pin.
RESET	6	DI	Reset pin, active low. Logic low on this pin turns off the internal oscillator and resets the device. Logic high returns the device to normal operation. Do not leave any digital pins floating.
RTS	4	DI	Request to send pin. A logic high on this pin enables the demodulator and disables the modulator. A logic low on this pin enables the modulator and disables the demodulator. Do not leave any digital pins floating.
RX_IN	21	AI	HART FSK input if no external filter is used; otherwise, no connect.
RX_INF	22	AI	HART FSK input if using the external band-pass filter. If using the internal band-pass filter by connecting the HART FSK to RX_IN, then connect 680-pF capacitor to this pin.
SCLK	7	DI	SPI clock. Data are transferred at rates up to 12.5 MHz. SCLK is a Schmitt-trigger logic input. Connect to GND or logic low if not used. Do not leave any digital pins floating.
VDD	13	P/AO	Internal low voltage LDO output. When 2.7 V to 5.5 V on PVDD pin is provided, the internal LDO is enabled. Connect a 1-μF to 10-μF capacitor on this pin.
VOUT	18	AO	DAC output voltage.
VREFIO	19	AI/AO	When the internal VREF is enabled by REF_EN pin, this pin outputs the internal VREF voltage. In this case, a load capacitance of 70 nF to 130 nF is required for stability. When disabled, this pin is the external 1.25-V reference input.

(1) AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
	Voltage	PVDD, IOVDD to GND	−0.3	5.5	V
		VDD to GND	−0.3	1.98	V
		AIN0, POL_SEL/AIN1, VOUT to GND	−0.3	PVDD + 0.3	V
		Digital Input/Output to GND	−0.3	IOVDD + 0.3	V
		VREFIO to GND	−0.3	VDD + 0.3	V
		REF_GND to GND	−0.3	0.3	V
	HART voltage	RX_IN, RX_INF, MOD_OUT to GND	−0.3	VDD + 0.3	V
	Input current into any pin		−10	10	mA
T <sub>J</sub>	Junction temperature		−55	150	°C
T <sub>stg</sub>	Storage temperature		−65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
		PVDD to GND	2.7		5.5	V
		VDD to GND	1.71		1.89	V
		IOVDD to GND	1.71		5.5	V
		VREFIO to GND, external VREF	1.2	1.25	1.3	V
T <sub>A</sub>	Ambient temperature	Specified	−40		125	°C
		Operating	−55		125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>1</sup>		AFE82H1	UNIT
		RRU (UQFN)	
		24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	103.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	84.4	°C/W
R <sub>θJC(bottom)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	69.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	68.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 5.5 Electrical Characteristics

all minimum and maximum values at  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and all typical values at  $T_A = 25^{\circ}\text{C}$ ,  $\text{PVDD} = \text{IOVDD} = 3.3\text{ V}$ , external or internal  $\text{VREFIO} = 1.25\text{ V}$ ,  $\text{R}_{\text{LOAD}} = 50\text{ k}\Omega$  to GND,  $\text{C}_{\text{LOAD}} = 100\text{ pF}$  to GND, and digital inputs at IOVDD or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOUT DAC STATIC PERFORMANCE						
	Resolution	AFE882H1	16			Bits
		AFE782H1	14			
INL	Integral nonlinearity <sup>(1)</sup>	AFE882H1, T <sub>A</sub> = −40°C to +125°C	−12		12	LSB
		AFE882H1, T <sub>A</sub> = −40°C to +85°C	−4		4	
		AFE782H1	−3		3	
DNL	Differential nonlinearity <sup>(1)</sup>		−1		1	LSB
TUE	Total unadjusted error <sup>(1)</sup>	T <sub>A</sub> = −40°C to +125°C	−0.1		0.1	%FSR
		T <sub>A</sub> = −40°C to +85°C	−0.08		0.08	
		T <sub>A</sub> = 25°C	−0.05		0.05	
	Zero code error, no load	T <sub>A</sub> = −40°C to +125°C			1	mV
		T <sub>A</sub> = −40°C to +85°C			1	
		T <sub>A</sub> = 25°C			0.5	
	Zero code error temperature coefficient		±3			ppm/°C
	Offset error <sup>(1)</sup>	T <sub>A</sub> = −40°C to +125°C	−0.07		0.07	%FSR
		T <sub>A</sub> = −40°C to +85°C	−0.05		0.05	
		T <sub>A</sub> = 25°C	−0.03		0.03	
	Offset error temperature coefficient <sup>(1)</sup>		±3			ppm/°C
	Gain error <sup>(1)</sup>	T <sub>A</sub> = −40°C to +125°C	−0.1		0.1	%FSR
		T <sub>A</sub> = −40°C to +85°C	−0.08		0.08	
		T <sub>A</sub> = 25°C	−0.05		0.05	
	Gain error temperature coefficient <sup>(1)</sup>		±3			ppm FSR/°C
	Full-scale error	T <sub>A</sub> = −40°C to +125°C	−0.1		0.1	%FSR
		T <sub>A</sub> = −40°C to +85°C	−0.08		0.08	
		T <sub>A</sub> = 25°C	−0.05		0.05	
	Full-scale error temperature coefficient		±3			ppm FSR/°C
VOUT DAC DYNAMIC PERFORMANCE						
t <sub>s</sub>	Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling to ±2 LSB	65			µs
		10-mV step settling to ±2 LSB	30			
	Slew rate	Full-scale transition measured from 10% to 90%	30			mV/µs
V <sub>n</sub>	Output noise	0.1 Hz to 10 Hz, DAC at midscale	0.25			LSBpp
		100-kHz bandwidth, DAC at midscale	32			µVrms
V <sub>n</sub>	Output noise density	Measured at 1 kHz, DAC at midscale, PVDD = 3 V	180			nV/√Hz
		Measured at 1 kHz, DAC at midscale, PVDD = 5 V	260			
	Power supply rejection ratio (ac)	200-mV 50-Hz to 60-Hz sine wave superimposed on power supply voltage, DAC at midscale.	85			dB
	Code change glitch impulse	Midcode ±1 LSB (including feedthrough)	4.5			nV-s
	Code change glitch magnitude	Midcode ±1 LSB (including feedthrough), PVDD = 5 V	1.5			mV
	Digital feedthrough	At SCLK = 1 MHz, DAC output at midscale	1			nV-s

## 5.5 Electrical Characteristics (続き)

all minimum and maximum values at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and all typical values at  $T_A = 25^\circ\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VOUT DAC OUTPUT CHARACTERISTICS</b>						
	Output voltage		0		2.5	V
	VOUT alarm output high		2.35	2.5	2.65	V
	VOUT alarm output low		0.285	0.3	0.315	V
$R_{LOAD}$	Resistive load <sup>(2)</sup>		10			k $\Omega$
$C_{LOAD}$	Capacitive load <sup>(2)</sup>				100	pF
	Load regulation	DAC at midscale, $-1\text{ mA} \leq I_{OUT} \leq +1\text{ mA}$		10		$\mu\text{V}/\text{mA}$
	Short-circuit current	Full scale output shorted to GND		5		mA
		Zero output shorted to VDD		5		
	Output voltage headroom to PVDD	DAC at full code, $I_{OUT} = 1\text{ mA}$ (sourcing)	200			mV
$Z_O$	Large signal dc output impedance	To GND, DAC at code 0		60		$\Omega$
		DAC at midscale		10		m $\Omega$
		DAC at code 65535		10		
		Output Hi-Z		500		k $\Omega$
	Power supply rejection ratio (dc)	DAC at midscale		0.1		mV/V
	Output voltage drift vs time, ideal VREF	$T_A = 35^\circ\text{C}$ , VOUT = midscale, 1000 hours		$\pm 5$		ppmFSR
<b>DIAGNOSTIC ADC</b>						
	Input voltage		0		2.5	V
	Resolution			12		Bits
DNL	Differential nonlinearity	Specified 12-bit monotonic	-1	$\pm 0.2$	1	LSB
INL	Integral nonlinearity		-4	$\pm 1$	4	LSB
	Offset error	After calibration	-10	$\pm 1.6$	10	LSB
	Gain error		-0.8	$\pm 0.13$	0.8	%FSR
	Noise			$\pm 4$		LSB
	Input capacitance			6		pF
	Input bias current	ADC not converting	-50		50	nA
	Acquisition time			52		$\mu\text{s}$
	Conversion time			210		$\mu\text{s}$
	Conversion rate				3.84	kSPS
	Temperature sensor accuracy			5		$^\circ\text{C}$
<b>INTERNAL OSCILLATOR</b>						
	Frequency	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	1.2165	1.2288	1.2411	MHz

## 5.5 Electrical Characteristics (続き)

all minimum and maximum values at  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and all typical values at  $T_A = 25^{\circ}\text{C}$ ,  $\text{PVDD} = \text{IOVDD} = 3.3\text{ V}$ , external or internal  $\text{VREFIO} = 1.25\text{ V}$ ,  $R_{\text{LOAD}} = 50\text{ k}\Omega$  to GND,  $C_{\text{LOAD}} = 100\text{ pF}$  to GND, and digital inputs at IOVDD or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>HART MODEM</b>						
<b>RX_IN INPUT (HART MODE)</b>						
	Input voltage range	External or internal reference source, design architecture. Signal applied at the input to the dc blocking capacitor.	0		1.5	$V_{\text{PP}}$
	Receiver sensitivity	Threshold for successful carrier detection and demodulation, assuming ideal sinusoidal input FSK signals with valid preamble using internal filter.	80	100	120	$\text{mV}_{\text{PP}}$
	Carrier detect time	1200 Hz of carrier frequency present at the input before CD asserted	3			baud
<b>MOD_OUT OUTPUT (HART MODE)</b>						
	Output voltage	Measured at MOD_OUT pin with 160- $\Omega$ load, ac-coupled (2.2 $\mu\text{F}$ )	400	500	800	$\text{mV}_{\text{PP}}$
	Mark frequency			1200		Hz
	Space frequency			2200		Hz
	Frequency error	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	-1		1	%
	Phase continuity error	Design architecture			0	Degrees
	Minimum resistive load	AC-coupled with 2.2 $\mu\text{F}$	160			$\Omega$
	Transmit impedance	$\overline{\text{RTS}}$ low, measured at the MOD_OUT pin, 1-mA measurement current		25		$\text{m}\Omega$
	Transmit impedance	$\text{RTS}$ high, measured at the MOD_OUT pin, $\pm 200\text{-nA}$ measurement current		50		$\text{k}\Omega$



## 5.5 Electrical Characteristics (続き)

all minimum and maximum values at  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and all typical values at  $T_A = 25^{\circ}\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , external or internal  $V_{REFIO} = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE INPUT						
Z <sub>VREFIO</sub>	Reference input impedance (VREFIO)			125		kΩ
C <sub>VREFIO</sub>	Reference input capacitance (VREFIO)			100		pF
VOLTAGE REFERENCE OUTPUT						
	Output (initial accuracy) <sup>(3)</sup>	T <sub>A</sub> = 25°C	1.248	1.25	1.252	V
	Output drift <sup>(3)</sup>	T <sub>A</sub> = −40°C to +125°C			10	ppm/°C
	Output impedance <sup>(3)</sup>			0.1		Ω
	Output noise <sup>(3)</sup>	0.1 Hz to 10 Hz		7.5		μV <sub>PP</sub>
	Output noise density <sup>(3)</sup>	Measured at 10 kHz, reference load = 100 nF		200		nV/√Hz
	Load current <sup>(3)</sup>	Sourcing, 0.1% VREF change from nominal		2.5		mA
		Sinking, 0.1% VREF change from nominal			0.3	
	Load regulation <sup>(3)</sup>	Sourcing, 0 mA to 2.5 mA		4		μV/mA
C <sub>OUT</sub>	Stable output capacitance	T <sub>A</sub> = −40°C to +125°C, ESR from 10 mΩ to 400 mΩ	70	100	130	nF
	Line regulation <sup>(3)</sup>			100		μV/V
	Output voltage drift vs time <sup>(3)</sup>	T <sub>A</sub> = 35°C, 1000 hours		±100		ppm
	Thermal hysteresis <sup>(3)</sup>	1st cycle		500		μV
		Additional cycles		25		μV
VDD VOLTAGE REGULATOR OUTPUT						
	Output voltage		1.71	1.8	1.89	V
	Output impedance <sup>(3)</sup>	Sourcing, 0.5 mA to 2.5 mA		3		Ω
	Load current <sup>(3)</sup>	Sourcing, 1% VDD change from nominal		4		mA
THERMAL ALARM						
	Alarm trip point			130		°C
	Warning trip point			85		°C
	Hysteresis			12		°C
	Trip point absolute accuracy			5		°C
	Trip point relative accuracy			2		°C
DIGITAL INPUT CHARACTERISTICS						
V <sub>IH</sub>	High-level input voltage		0.7			V/IOVDD
V <sub>IL</sub>	Low-level input voltage				0.3	V/IOVDD
	Hysteresis voltage		0.05			V/IOVDD
	Input current		−1.56		1.56	μA
	Pin capacitance	Per pin		10		pF
DIGITAL OUTPUT CHARACTERISTICS						
V <sub>OH</sub>	High-level output voltage	I <sub>SOURCE</sub> = 1 mA	0.8			V/IOVDD
V <sub>OL</sub>	Low-level output voltage	I <sub>SINK</sub> = 1 mA			0.2	V/IOVDD
V <sub>OL</sub>	Open-drain low-level output voltage	I <sub>SINK</sub> = 2 mA			0.3	V
	Output pin capacitance			10		pF

## 5.5 Electrical Characteristics (続き)

all minimum and maximum values at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and all typical values at  $T_A = 25^\circ\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER REQUIREMENTS</b>						
$I_{PVDD}$	Current flowing into PVDD	DAC at zero-scale, SPI static		180	220	$\mu\text{A}$
$I_{REFIO}$	Internal reference current consumption			52	70	$\mu\text{A}$
$I_{HART}$	HART Tx modem current consumption			10		$\mu\text{A}$
$I_{ADC}$	ADC current consumption	ADC converting at 3.84 kSPS		10		$\mu\text{A}$
$C_{VDD}$	Recommended VDD decoupling capacitance		1		10	$\mu\text{F}$
$I_{IOVDD}$	Current flowing into IOVDD	SPI static		10	25	$\mu\text{A}$
$I_{VREFIO}$	Current flowing into VREFIO	DAC at midscale code		10		$\mu\text{A}$

- (1) End point fit between code 512 to code 65,535 for 16-bit, code 128 to code 16,383 for 14-bit, DAC output unloaded, performance under resistive and capacitive load conditions are specified by design and characterization.
- (2) Not production tested. Design target.
- (3) Not production tested. Derived from the characterization data.

## 5.6 Timing Requirements

all input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $2.7 \text{ V} \leq PVDD \leq 5.5 \text{ V}$ ,  $V_{IH} = 1.62 \text{ V}$ ,  $V_{IL} = 0.15 \text{ V}$ ,  $V_{REFIO} = 1.25 \text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
<b>SERIAL INTERFACE - WRITE AND READ OPERATION</b>					
$f_{SCLK}$	Serial clock frequency			12.5	MHz
$t_{SCLKHIGH}$	SCLK high time	36			ns
$t_{SCLKLOW}$	SCLK low time	36			ns
$t_{CSHIGH}$	$\overline{CS}$ high time	80			ns
$t_{CSS}$	$\overline{CS}$ to SCLK falling edge setup time	30			ns
$t_{CSH}$	SCLK falling edge to $\overline{CS}$ rising edge	30			ns
$t_{CSRI}$	$\overline{CS}$ rising edge to SCLK falling edge ignore	30			ns
$t_{CSFI}$	SCLK falling edge ignore to $\overline{CS}$ falling edge	5			ns
$t_{SDIS}$	SDI setup time	5			ns
$t_{SDIH}$	SDI hold time	5			ns
$t_{SDOZD}$	$\overline{CS}$ falling edge to SDO tri-state condition to driven			40	ns
$t_{SDODZ}$	$\overline{CS}$ rising edge to SDO driven to tri-state condition			40	ns
$t_{SDODLY}$	SCLK to SDO output delay			40	ns
<b>UART</b>					
$t_{BAUDUART}$	Baud rate = 9600 $\pm 1\%$		104		$\mu\text{s}$
$t_{BAUDUART}$	Baud rate = 1200 $\pm 1\%$		833		$\mu\text{s}$
<b>HART</b>					
$t_{BAUDHART}$	Baud rate = 1200 $\pm 1\%$		833		$\mu\text{s}$
<b>DIGITAL LOGIC</b>					
$t_{DACWAIT}$	Sequential DAC update wait time	2.1			$\mu\text{s}$
$t_{POR}$	POR reset delay			100	$\mu\text{s}$
$t_{RESET}$	RESET pulse duration	100			ns
$t_{RESETWAIT}$	Wait time after RESET pulse	10			$\mu\text{s}$
$t_{PULSE\_GPIO}$	GPIO input pulse duration	10			ns

## 5.7 Timing Diagrams

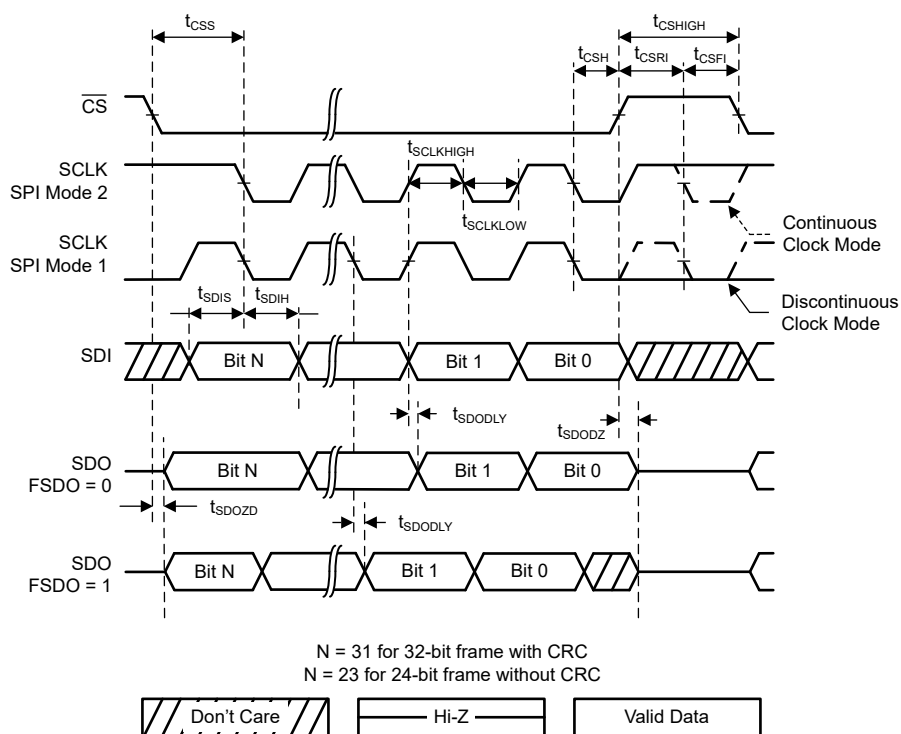


図 5-1. SPI Timing

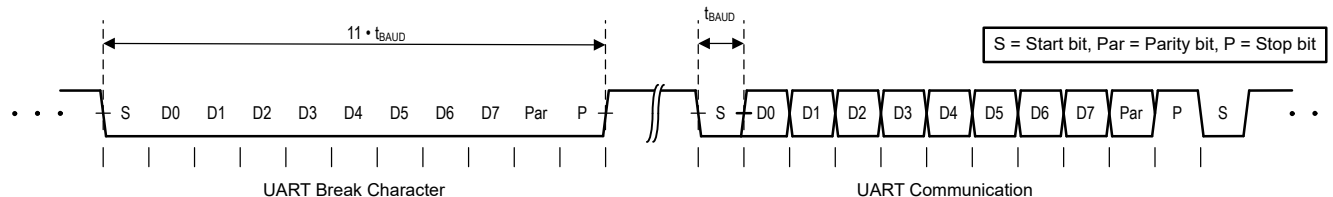


図 5-2. UBM Timing

## 5.8 Typical Characteristics: VOUT DAC

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = 2.7\text{ V}$ ,  $IOVDD = 1.8\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

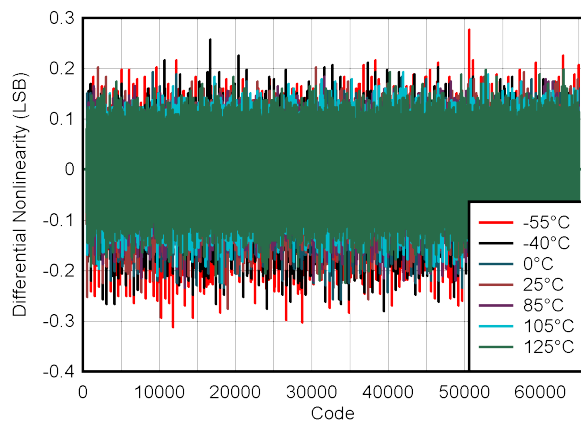


図 5-3. DAC DNL vs Digital Input Code

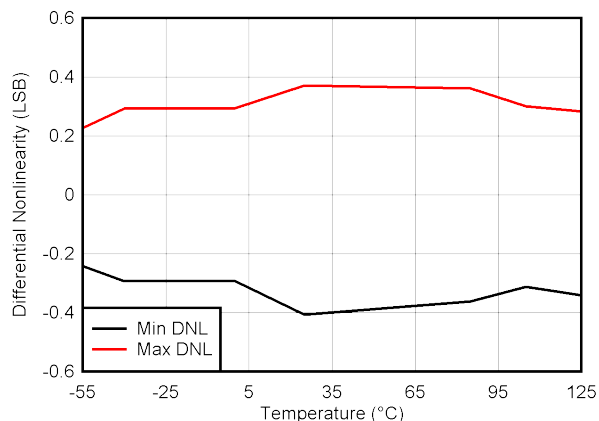


図 5-4. MIN and MAX DAC DNL Range vs Temperature

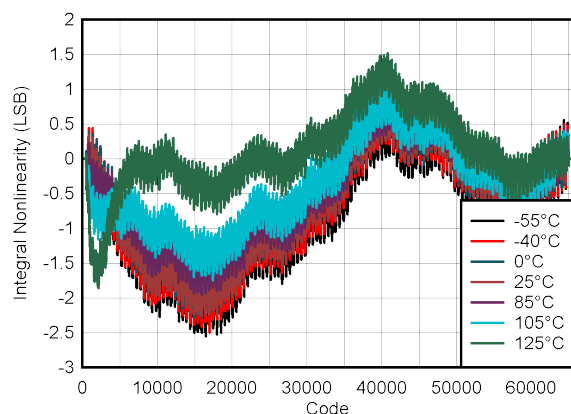


図 5-5. DAC INL vs Digital Input Code

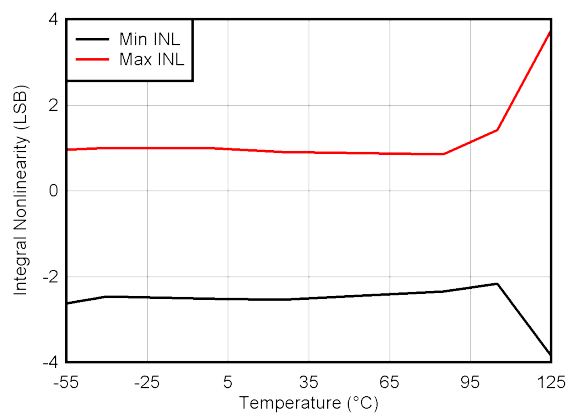


図 5-6. MIN and MAX DAC INL Range vs Temperature

## 5.8 Typical Characteristics: VOUT DAC (continued)

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = 2.7\text{ V}$ ,  $IOVDD = 1.8\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

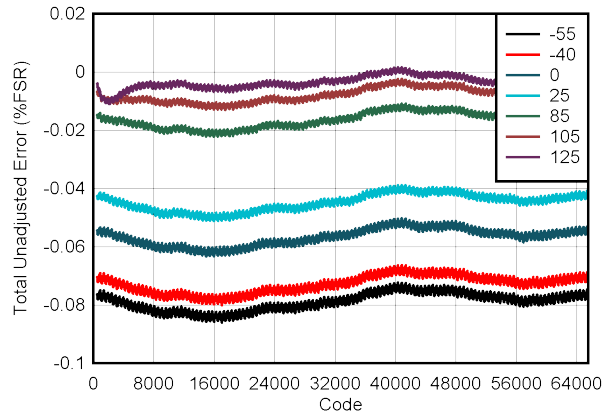


図 5-7. DAC TUE vs Digital Input Code

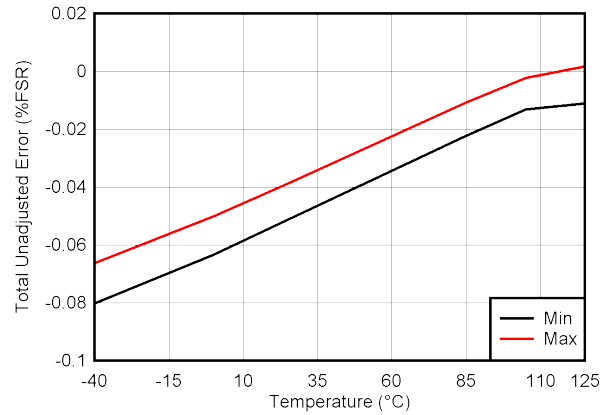


図 5-8. MIN and MAX DAC TUE vs Temperature

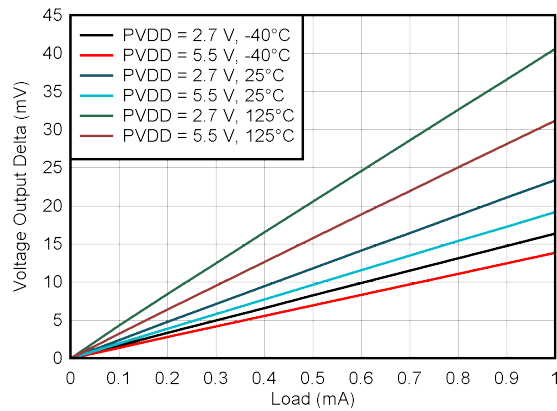


図 5-9. Zero-code Impedance

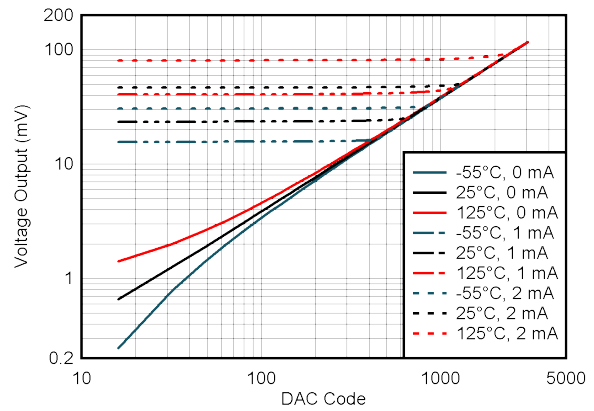
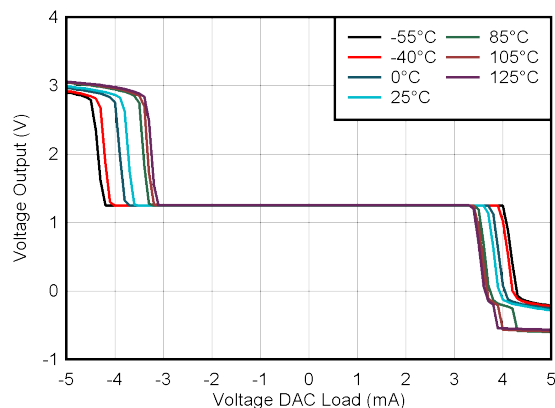


図 5-10. DAC Footroom Over Temperature and Load

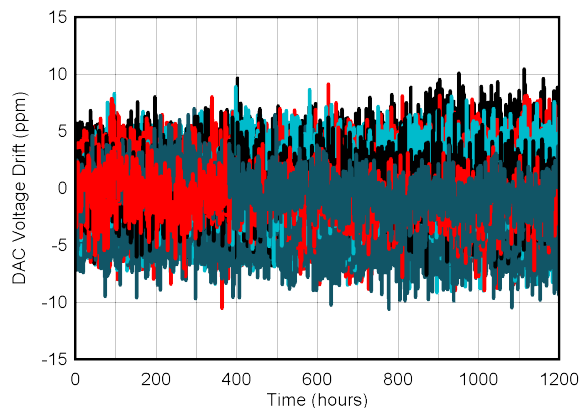
## 5.8 Typical Characteristics: VOUT DAC (continued)

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = 2.7\text{ V}$ ,  $IOVDD = 1.8\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)



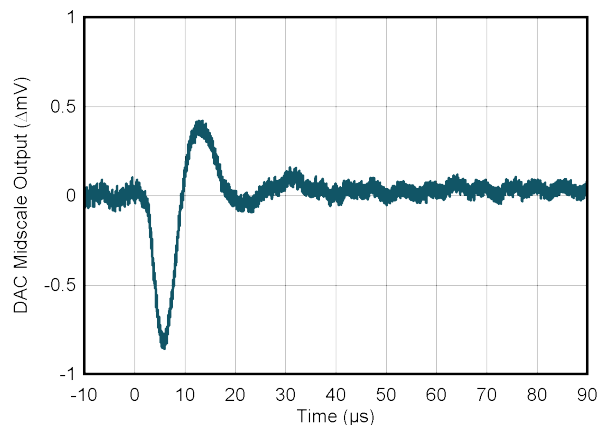
DAC at midcode

図 5-11. DAC Source and Sink Current Capability



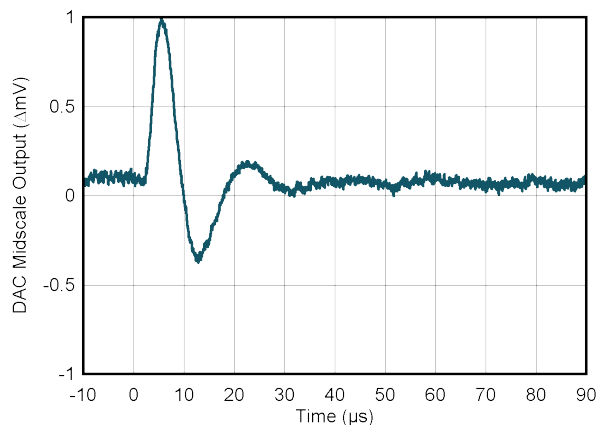
Ideal reference

図 5-12. DAC Output Voltage Long-Term Stability



$PVDD = 5.5\text{ V}$

図 5-13. DAC Glitch Impulse Rising Edge



$PVDD = 5.5\text{ V}$

図 5-14. DAC Glitch Impulse Falling Edge

## 5.8 Typical Characteristics: VOUT DAC (continued)

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = 2.7\text{ V}$ ,  $IOVDD = 1.8\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

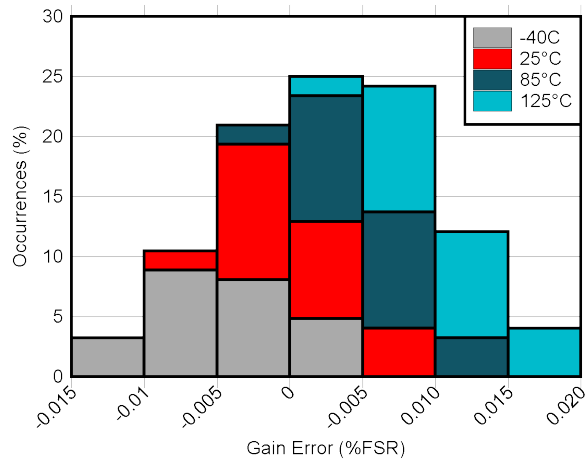


図 5-15. DAC Gain Error vs Temperature

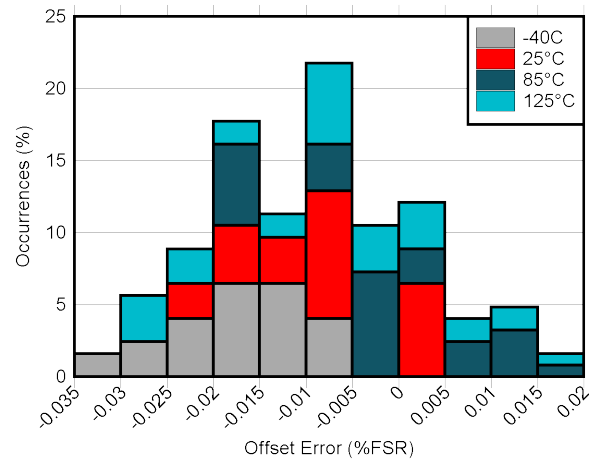


図 5-16. DAC Offset Error vs Temperature

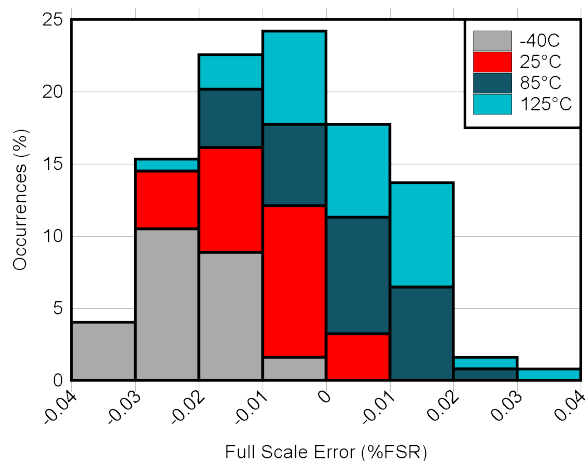


図 5-17. DAC Full Scale Error vs Temperature

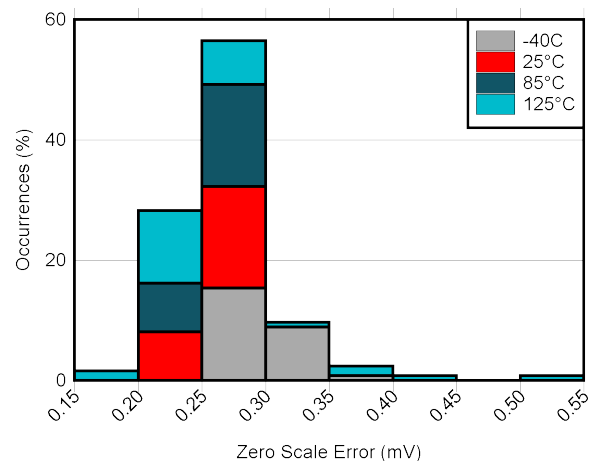
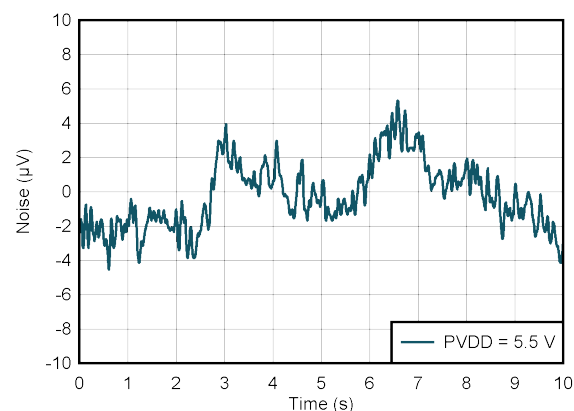
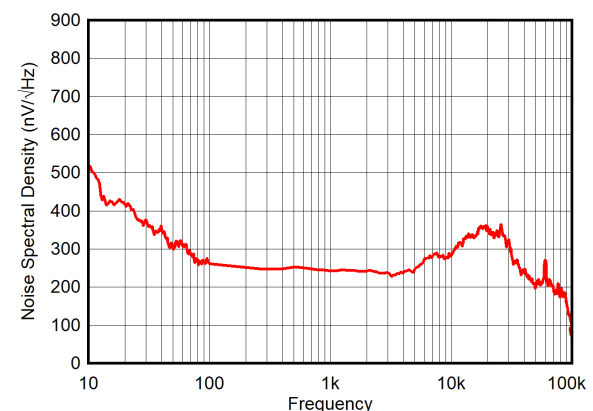


図 5-18. DAC Zero Scale Error vs Temperature



DAC at midcode PVDD = 5.5 V

図 5-19. DAC Output Noise, 0.1 Hz to 10 Hz



DAC at midcode PVDD = 5.5 V

図 5-20. DAC Output Noise Density vs Frequency



## 5.8 Typical Characteristics: VOUT DAC (continued)

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = 2.7\text{ V}$ ,  $IOVDD = 1.8\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

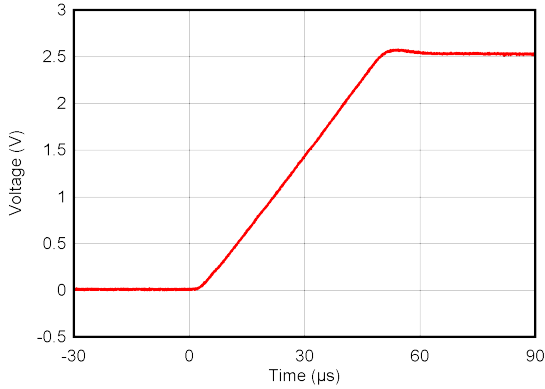


図 5-21. DAC Rising Settling Time

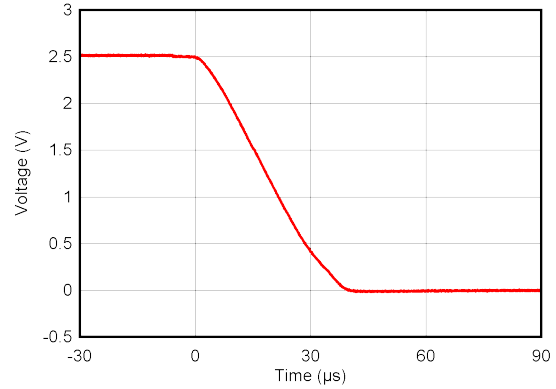


図 5-22. DAC Falling Settling Time

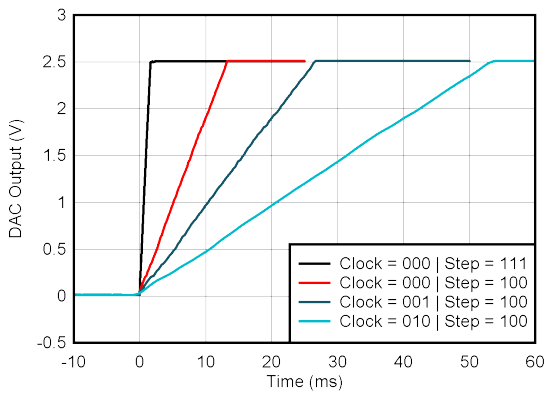


図 5-23. DAC Settling Time With Linear Slew Rate Control

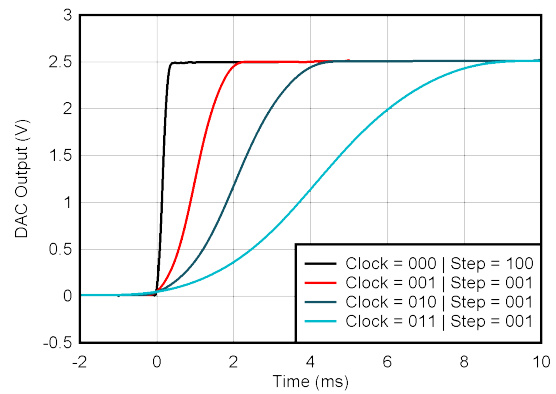


図 5-24. DAC Settling Time With Sinusoidal Slew Rate Control

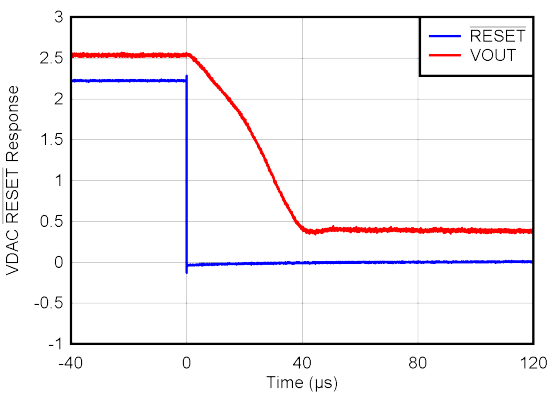


図 5-25. DAC RESET Response

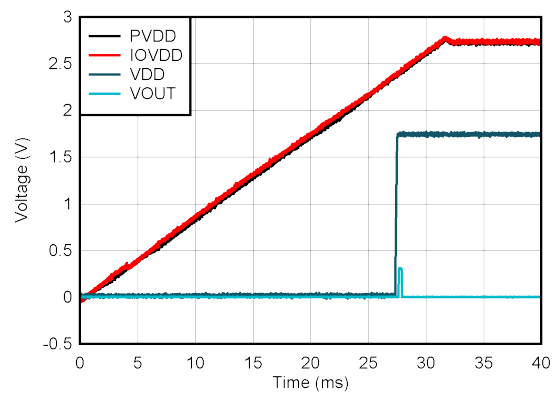
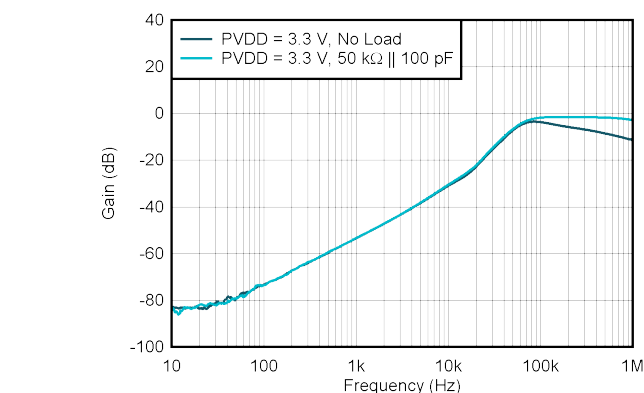


図 5-26. DAC Supply Power On,  $PVDD = 2.7\text{ V}$

## 5.8 Typical Characteristics: VOUT DAC (continued)

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = 2.7\text{ V}$ ,  $IOVDD = 1.8\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)



Internal reference

図 5-27. DAC AC PSRR vs Frequency

## 5.9 Typical Characteristics: ADC

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = 3.3\text{ V}$ ,  $IOVDD = 1.8\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

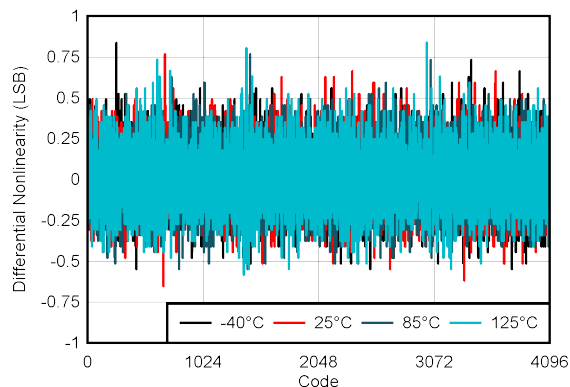


図 5-28. ADC DNL vs Digital Input Code

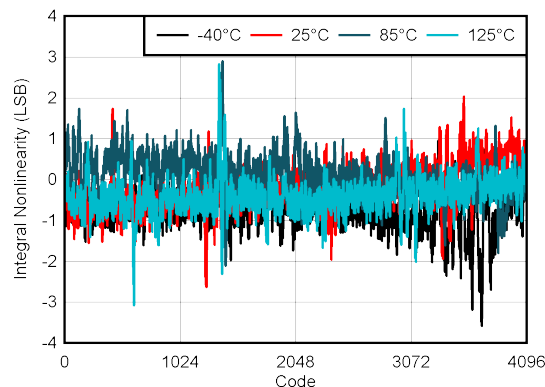


図 5-29. ADC INL vs Digital Input Code

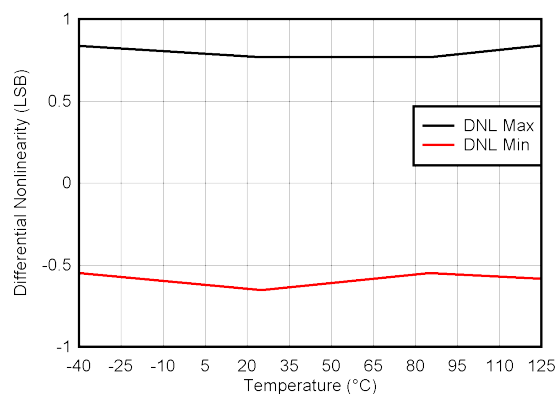


図 5-30. ADC DNL Range vs Temperature

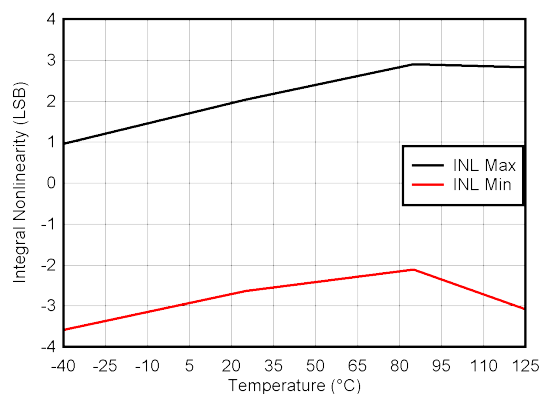


図 5-31. ADC INL Range vs Temperature

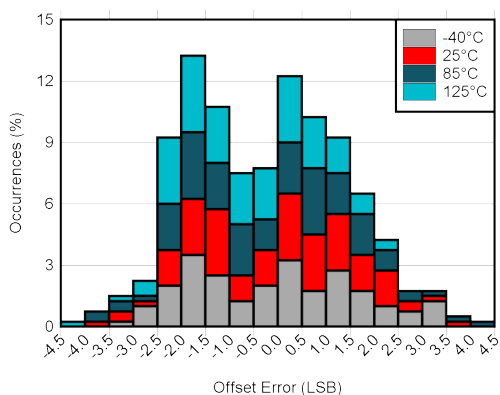


図 5-32. ADC Offset Error vs Temperature

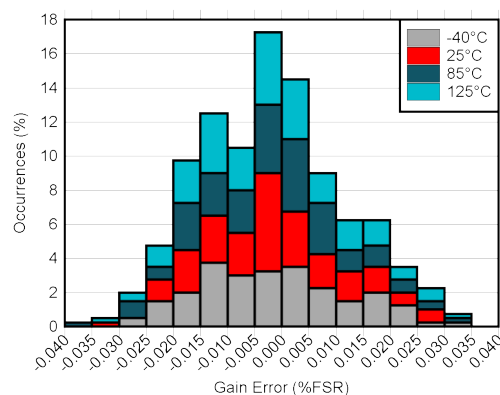


図 5-33. ADC Gain Error vs Temperature

## 5.10 Typical Characteristics: Reference

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at IOVDD or GND (unless otherwise noted)

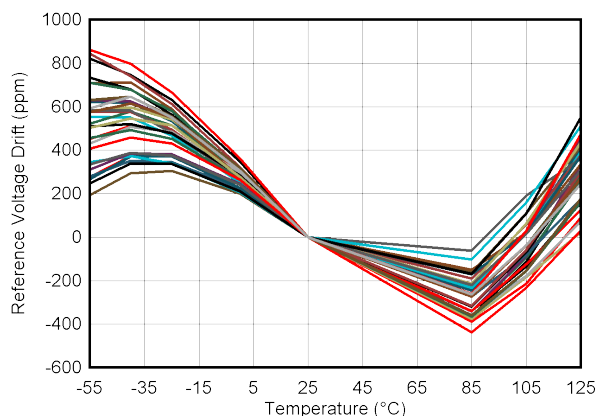


Figure 5-34. Reference Voltage Temperature Drift

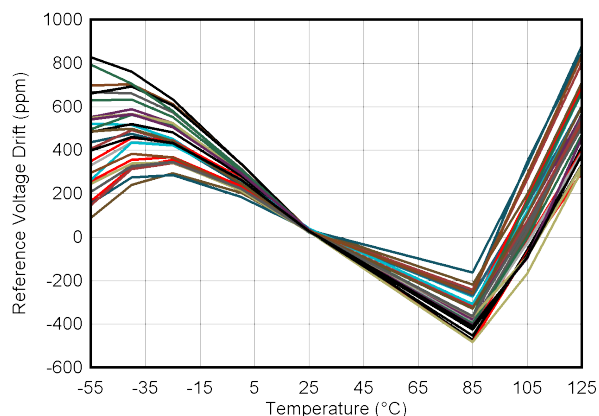


Figure 5-35. Reference Voltage Temperature Drift

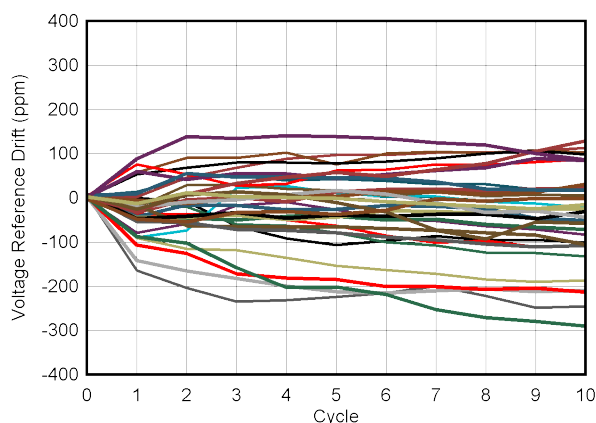


Figure 5-36. Multiple Temperature Cycle Hysteresis

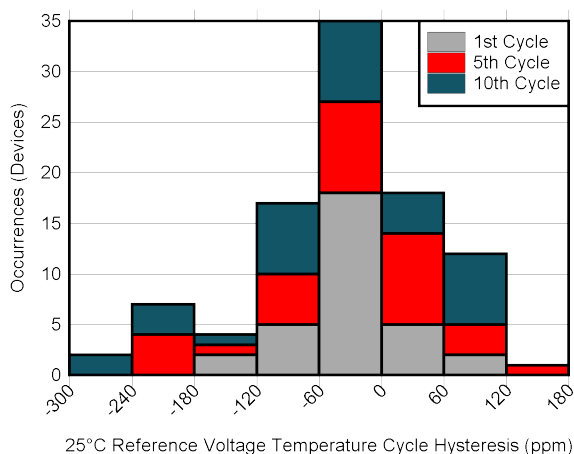
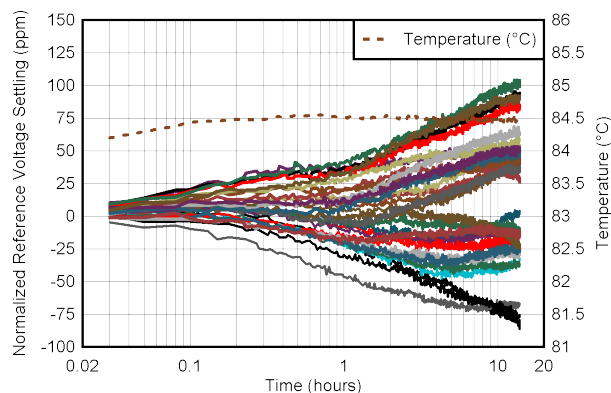


Figure 5-37. Multiple Temperature Cycle Hysteresis

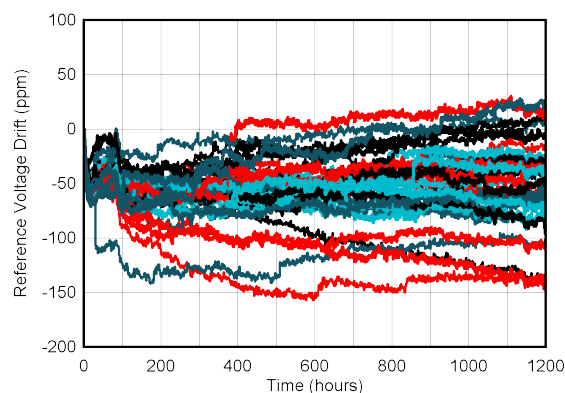
## 5.10 Typical Characteristics: Reference (continued)

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at IOVDD or GND (unless otherwise noted)



Two minutes after  $25^\circ\text{C}$  to  $85^\circ\text{C}$  temperature step, 30 units

図 5-38. Ambient Temperature Change Settling



30 units

図 5-39. Reference Voltage Long-Term Stability

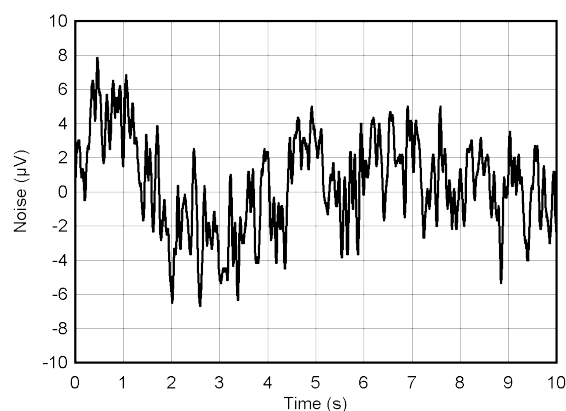


図 5-40. Reference Output Noise, 0.1 Hz to 10 Hz

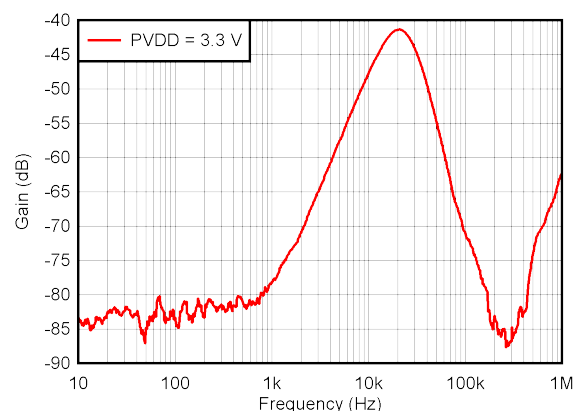


図 5-41. Reference AC PSRR vs frequency

## 5.10 Typical Characteristics: Reference (continued)

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at IOVDD or GND (unless otherwise noted)

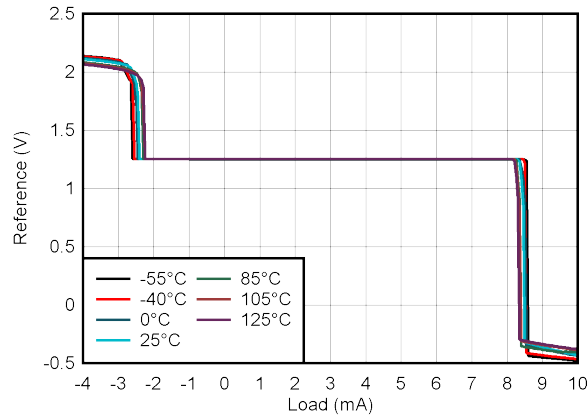


図 5-42. Reference Source and Sink Current Capability

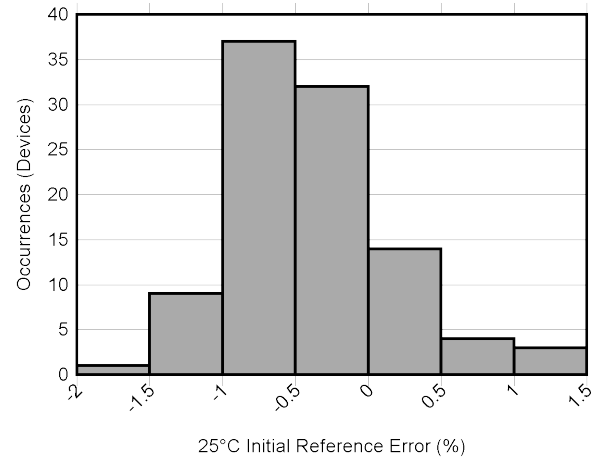
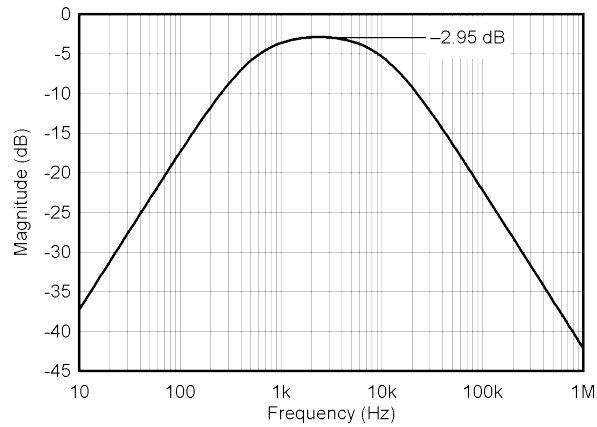


図 5-43. Initial Accuracy Distribution

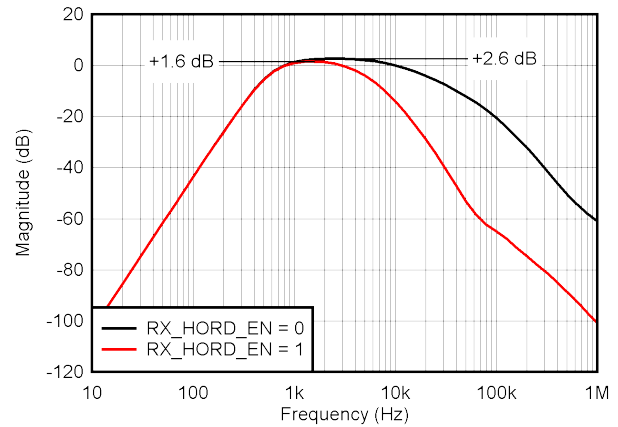
## 5.11 Typical Characteristics: HART Modem

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , external or internal  $VREFIO = 1.25\text{ V}$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at IOVDD or GND (unless otherwise noted)



2.2 nF HART\_RX Input Capacitor      680 pF RX\_INF Capacitor to Ground

**図 5-44. HART Internal Mode First Stage Band-Pass Filter Response (From HART\_RX Signal to RX\_INF Pin)**



2.2 nF HART\_RX Input Capacitor      680 pF RX\_INF Capacitor to Ground

**図 5-45. HART Internal Mode Complete Band-Pass Filter Response (From HART\_RX Signal to Internal Demodulator)**

## 5.12 Typical Characteristics: Power Supply

at  $T_A = 25^\circ\text{C}$ ,  $PVDD = IOVDD = 3.3\text{ V}$ , internal  $VREFIO$ ,  $R_{LOAD} = 50\text{ k}\Omega$  to GND,  $C_{LOAD} = 100\text{ pF}$  to GND, and digital inputs at  $IOVDD$  or GND (unless otherwise noted)

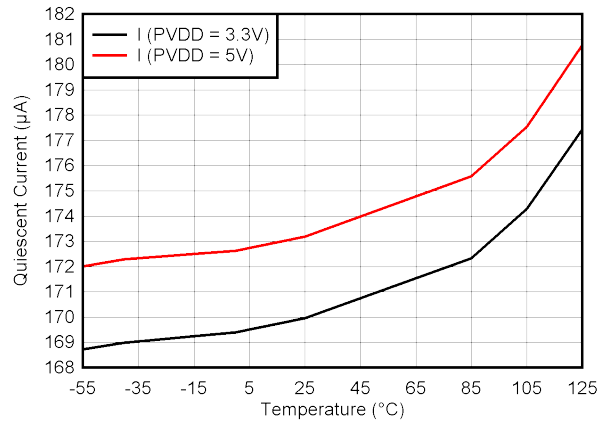


図 5-46. PVDD Supply Current vs Temperature

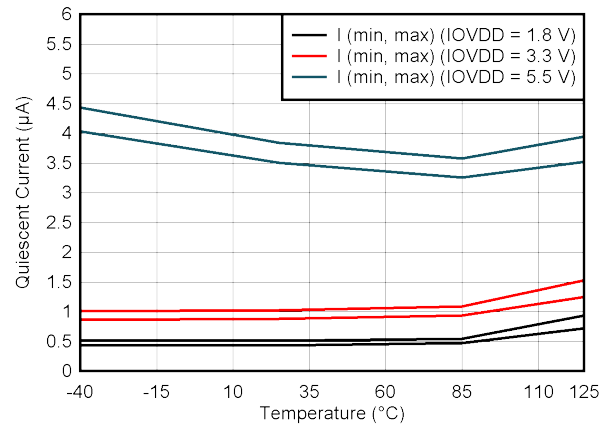


図 5-47. IOVDD Supply Current vs Temperature

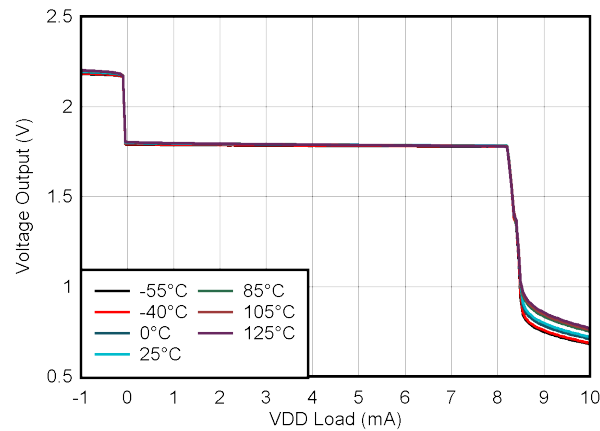


図 5-48. VDD Voltage vs Load Current



## 6 Detailed Description

### 6.1 Overview

The AFEx82H1 feature a 16-bit (AFE882H1) or 14-bit (AFE782H1) string DAC with voltage output buffer. Both devices have a buffered voltage output and are designed for use in three-wire or four-wire sensor transmitters or analog output modules. The DAC has calibration registers for setting gain and offset values for adjusting the DAC outputs. The DAC also has different output slewing modes that allow for a programmable linear slew and a sinusoidal shaped output slew.

The AFEx82H1 also feature a 12-bit SAR ADC that can be multiplexed to measure different inputs, including external nodes and internal nodes for diagnostic measurements on the device. The ADC is capable of making direct-mode measurements with on-demand conversions or auto-mode measurements through continuous conversions using a channel sequencer with a multiplexer. The devices have optional alarm configurations with fault detection and alarm actions.

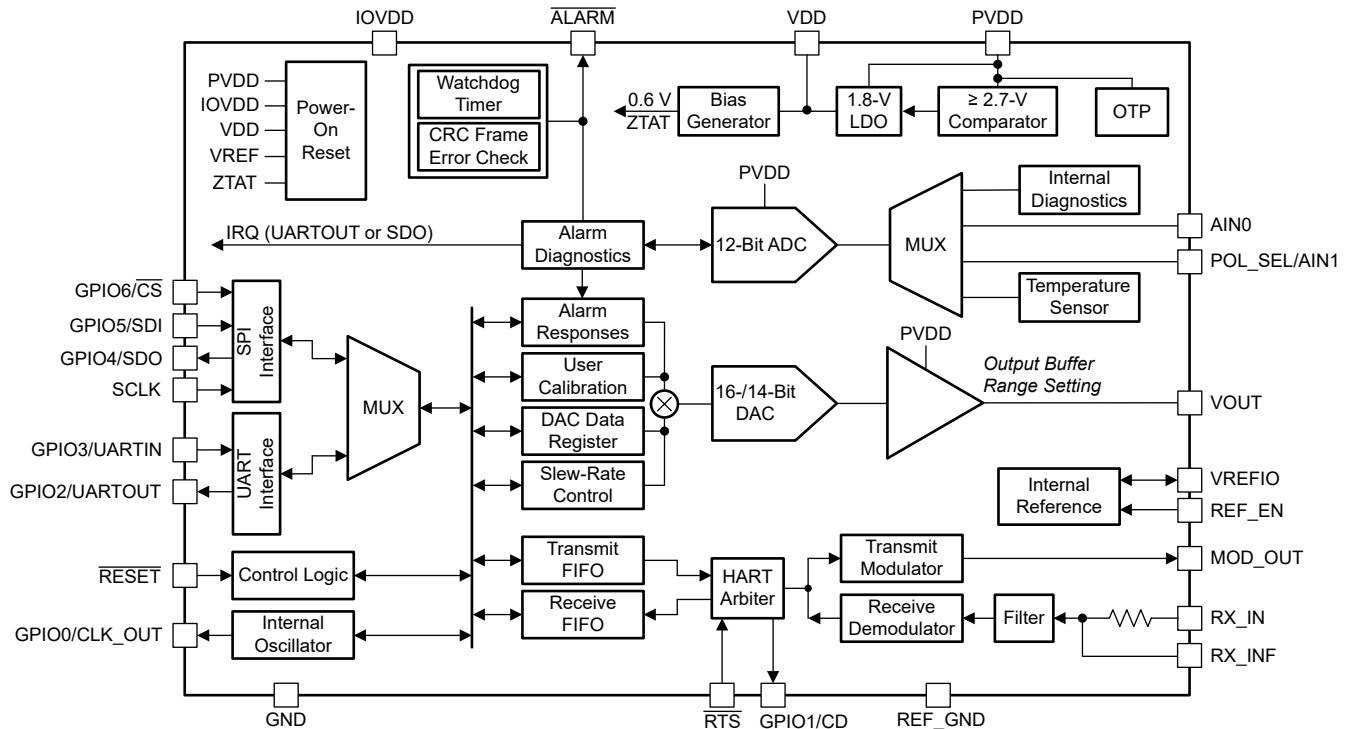
Device communication and programming are done through an SPI, SPI plus a UART interface, or through the UART break mode (UBM). With the SPI, a cyclic redundancy check (CRC) is implemented by default, which can be disabled. Additionally, communications can be monitored with a watchdog timer (WDT) that alerts the user if the device becomes unresponsive to periodic communication.

For the field transmitter, a HART interface is created through modulation and demodulation using the SPI or UART. The demodulation of the input signal is done using the combination of the external and internal band-pass filtering.

The AFEx82H1 feature a 1.25-V, onboard precision voltage reference, and an integrated precision oscillator.

Throughout this data sheet, register and bit names are combined with a period to use the following format: <register\_name>.<bit\_name>. For example, the CLR bit in the DAC\_CFG register is labeled DAC\_CFG.CLR.

### 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Digital-to-Analog Converter (DAC) Overview

The AFEx82H1 feature a 16-bit (AFE882H1) or 14-bit (AFE782H1) string DAC followed by an output voltage buffer. Using an external circuit, the device output voltage can be translated to different output voltages and output currents for use in 3-wire or 4-wire sensor transmitters or analog output modules. The DAC is configured to support a 0-V to 2.5-V range of operation. The alarm function is triggered when PVDD exceeds the valid configuration range of 2.7 V to 5.5 V; see also 表 6-5.

#### 6.3.1.1 DAC Resistor String

図 6-1 shows that the resistor string structure consists of a series of resistors, each of value  $R$ . The code loaded to the DAC determines the node on the string at which the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. The resistor string architecture has inherent monotonicity, voltage output, and low glitch.

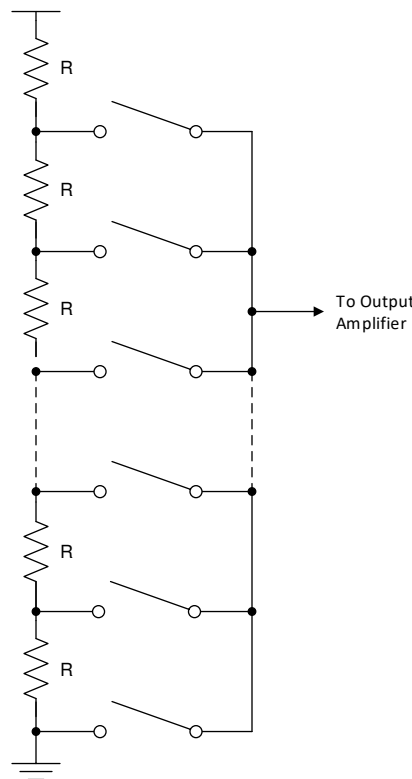


図 6-1. DAC Resistor String

#### 6.3.1.2 DAC Buffer Amplifier

The VOUT output pin is driven by the DAC output buffer amplifier. The output amplifier default settings are designed to drive capacitive loads as high as 100 pF without oscillation. The output buffer is able to source and sink 1 mA. The device implements short-circuit protection for momentary output shorts to ground and VDD supply. The source and sink short-circuit current thresholds are set to 5 mA.

### 6.3.1.3 DAC Transfer Function

The following equation describes the DAC transfer function, which is the relationship between internal signal DAC\_CODE and output voltage VOUT:

$$V_{OUT} = \frac{DAC\_CODE}{2^N} \times FSR \quad (1)$$

where

- DAC\_CODE is an internal signal and the decimal equivalent of the gain and offset calibrated binary code loaded into the DAC\_DATA register. DAC\_CODE range = 0 to  $2^N - 1$ .
- N = DAC\_CODE resolution in bits (16 for the AFE882H1 and 14 for the AFE782H1).
- FSR = VOUT full-scale range = 2.5 V.

### 6.3.1.4 DAC Gain and Offset Calibration

The AFEx82H1 provide DAC gain and offset calibration capability to correct for end-point errors present in the system. Implement the gain and offset calibration using two registers, DAC\_GAIN.GAIN and DAC\_OFFSET.OFFSET. Update DAC\_DATA register after gain or offset codes are changed for the new values to take effect. The DAC\_GAIN can be programmed from 0.5 to 1.499985 using 式 2.

$$DAC\_GAIN = \frac{1}{2} + \frac{GAIN}{2^N} \quad (2)$$

where

- N = DAC\_GAIN resolution in bits: 16 for the AFE882H1 and 14 for the AFE782H1.
- GAIN is the decimal value of the DAC\_GAIN register setting.
- GAIN data are left justified; the last two LSBs in the DAC\_GAIN register are ignored for the AFE782H1.

The example DAC\_GAIN settings for the AFE882H1 are shown in 表 6-1.

**表 6-1. DAC\_GAIN Setting vs GAIN Code**

DAC_GAIN	GAIN (HEX)
0.5	0x0000
1.0	0x8000
1.499985	0xFFFF

The DAC\_OFFSET is stored in the DAC\_OFFSET register using 2's-complement encoding. The DAC\_OFFSET value can be programmed from  $-2^{(N-1)}$  to  $2^{(N-1)} - 1$  using 式 3.

$$DAC\_OFFSET = -OFFSET_{MSB} \times 2^{(N-1)} + \sum_{i=0}^{(N-2)} OFFSET_i \times 2^i \quad (3)$$

where

- N = DAC\_OFFSET resolution in bits: 16 for the AFE882H1 and 14 for the AFE782H1.
- $OFFSET_{MSB}$  = MSB bit of the DAC\_OFFSET register.
- $OFFSET_i$  = The rest of the bits of the DAC\_OFFSET register.
- i = Position of the bit in the DAC\_OFFSET register.
- OFFSET data are left justified; the last two LSBs in the DAC\_OFFSET register are ignored for the device.

The most significant bit determines the sign of the number and is called the sign bit. The sign bit has the weight of  $-2^{(N-1)}$  as shown in 式 3.

The example DAC\_OFFSET settings for the AFE882H1 are shown in 表 6-2.

**表 6-2. DAC\_OFFSET Setting vs OFFSET Code**

DAC_OFFSET	OFFSET (HEX)
32767	0x7FFF
1	0x0001
0	0x0000
-1	0xFFFF
-2	0xFFFE
-32768	0x8000

The following transfer function is applied to the DAC\_DATA.DATA based on the DAC\_GAIN and DAC\_OFFSET values:

$$\text{DAC\_CODE} = (\text{DATA} \times \text{DAC\_GAIN}) + \text{DAC\_OFFSET} \quad (4)$$

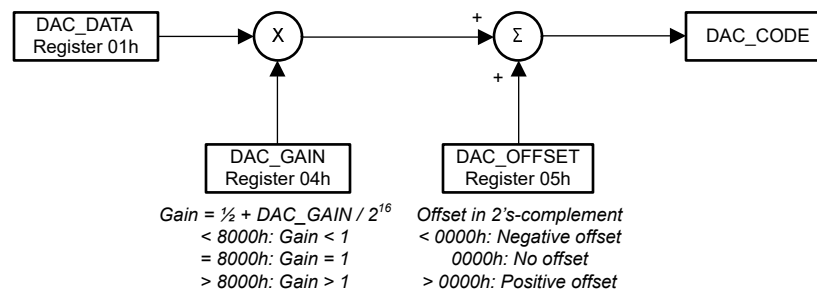
where

- DAC\_CODE is the internal signal applied to the DAC.
- DATA is the decimal value of the DAC\_DATA register.
- DAC\_GAIN and DAC\_OFFSET are the user calibration settings.
- DATA data are left justified; the last two LSBs in the DAC\_DATA register are ignored for the AFE782H1.

Substituting DAC\_GAIN and DAC\_OFFSET in 式 4 with 式 2 and 式 3 results in:

$$\text{DAC\_CODE} = \left( \text{DATA} \times \left[ \frac{1}{2} + \frac{\text{GAIN}}{2^N} \right] \right) - \text{OFFSET}_{\text{MSB}} \times 2^{(N-1)} + \sum_{i=0}^{(N-2)} \text{OFFSET}_i \times 2^i \quad (5)$$

The multiplier is implemented using truncation instead of rounding. This truncation can cause a difference of one LSB if rounding is expected. 図 6-2 shows the DAC calibration path.



**図 6-2. DAC Calibration Path**

### 6.3.1.5 Programmable Slew Rate

The slew rate feature controls the rate at which the output voltage or current changes. This feature is disabled by default and is enabled by writing a logic 1 to the DAC\_CFG.SR\_EN bit. With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by DAC\_CFG.SR\_STEP[2:0] and DAC\_CFG.SR\_CLK[2:0]. SR\_CLK defines the rate at which the digital slew updates. SR\_STEP defines the amount by which the output value changes at each update. The register descriptions show different settings for SR\_STEP and SR\_CLK.

The time required for the output to slew is expressed as 式 6:

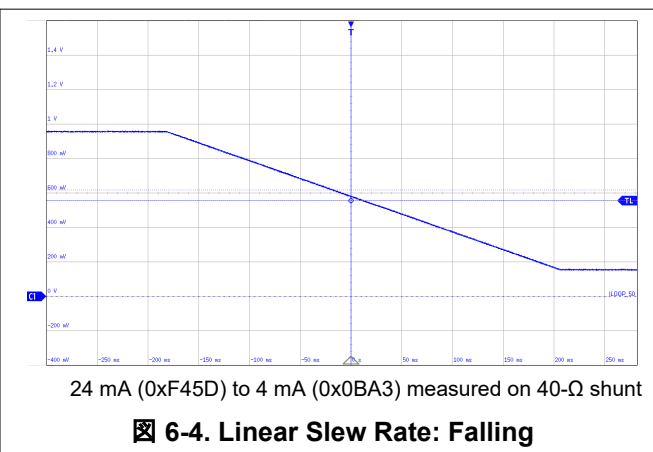
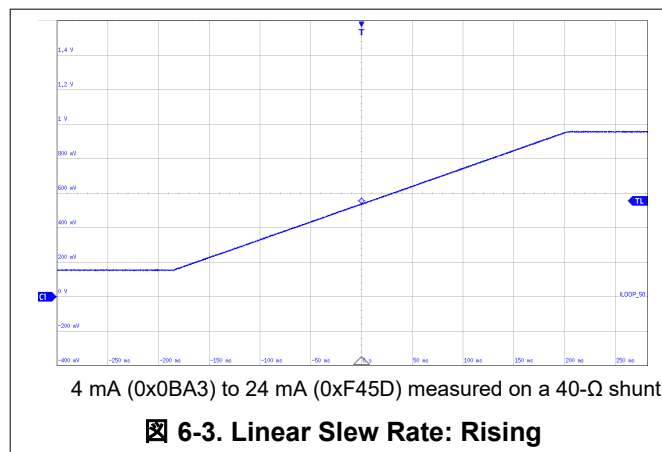
$$\text{Slew Time} = \frac{\text{Delta Code Change}}{\text{Slew Step} \times \text{Slew Clock Rate}} \quad (6)$$

where

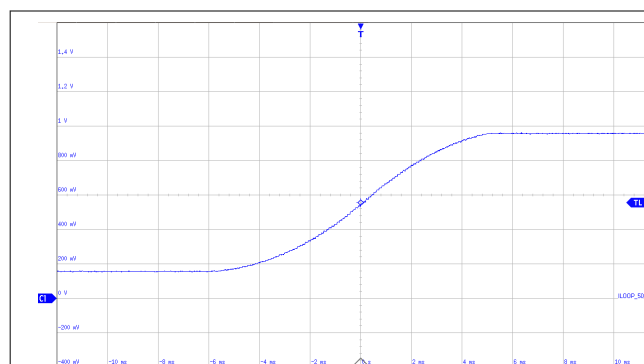
- *Slew Time* is expressed in seconds
- *Slew Step* is controlled by DAC\_CFG.SR\_STEP
- *Slew Clock Rate* is controlled by DAC\_CFG.SR\_CLK

When the slew-rate control feature is enabled, the output changes at the programmed slew rate. This configuration results in a staircase formation at the output. If the clear code is asserted (see セクション 6.3.1.6), the output slews to the DAC\_CLR\_CODE value at the programmed slew rate. When new DAC data are written, the output starts slewing to the new value at the slew rate determined by the current DAC code and the new DAC data.

Two slew-rate control modes are available: linear (default) and sinusoidal. 図 6-3 and 図 6-4 show the typical rising and falling DAC output waveforms, respectively.

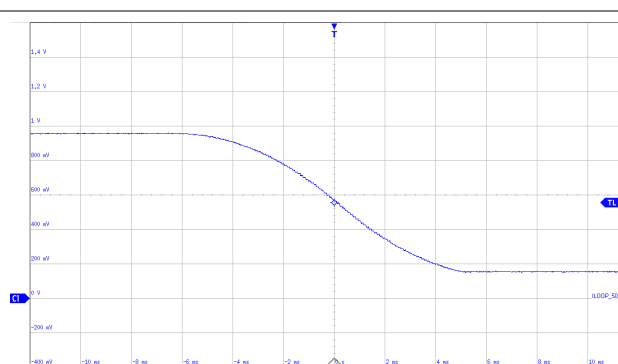


Sinusoidal mode enables fast DAC settling while improving analog rate of change characteristics. Sinusoidal mode is selected by the DAC\_CFG.SR\_MODE bit. 図 6-5 and 図 6-6 show the typical rising and falling DAC output waveforms with sinusoidal slew-rate control, respectively.



4 mA (0x0BA3) to 24 mA (0xF45D) measured on a 40-Ω shunt

**図 6-5. Sinusoidal Slew Rate: Rising**



24 mA (0xF45D) to 4 mA (0x0BA3) measured on a 40-Ω shunt

**図 6-6. Sinusoidal Slew Rate: Falling**

If the slew-rate feature is disabled while the DAC is executing the slew-rate command, the slew-rate operation is aborted, and the DAC output goes to the target code.

### 6.3.1.6 DAC Register Structure and CLEAR State

The AFE882H1 DAC has a 16-bit voltage output, and the AFE782H1 DAC has a 14-bit voltage output. The output range is 0 V to 2.5 V.

The AFE82H1 provide the option to quickly set the DAC output to the value set in the DAC\_CLR\_CODE register without writing to the DAC\_DATA register, referred to as the CLEAR state. For register details, see 表 7-6.

Transitioning from the DAC\_DATA to the DAC\_CLR\_CODE is synchronous to the clock. If slew mode is enabled, the output slews during the transition. 図 6-7 shows the full AFEx82H1 DAC\_DATA signal path. The devices synchronize the DAC\_DATA code to the internal clock, causing up to 2.5 internal clock cycles of latency (2  $\mu$ s) with respect to the rising edge of  $\overline{CS}$  or the end of a UBM command. Update DAC\_GAIN and DAC\_OFFSET values when DAC\_CFG.SR\_EN = 0 to avoid an IRQ pulse generated by SR\_BUSY.

Set the DAC to CLEAR state either by:

1. Setting DAC\_CFG.CLR.
2. Configuring the DAC to transition to the CLEAR state in response to an alarm condition.
3. Using the SDI pin in UBM as the CLEAR state input pin.

Method 1 is a direct command to the AFEx82H1 to set the DAC to CLEAR state. Set the DAC\_CFG.CLR bit to 1h to set the DAC to CLEAR state.

Method 2 is controlled by settings of ALARM\_ACT register. For details of conditions and other masks required to use this method, see 表 7-17 and セクション 6.3.3.2.

Method 3 supports setting the DAC to CLEAR state without writing to the AFEx82H1. This pin-based DAC CLEAR state function is available only in UBM on the SDI pin. For details of connection options based on communication modes and pins used in each mode, see セクション 6.5.1. Set the appropriate pin high to drive the DAC to CLEAR state.

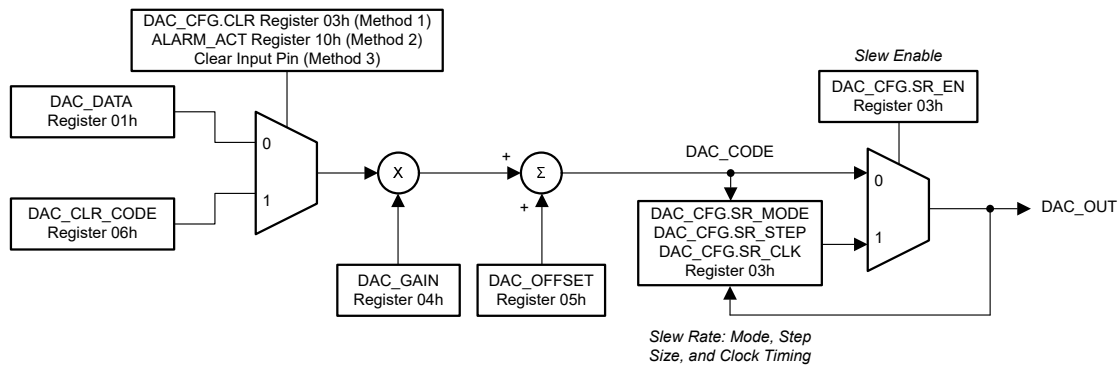


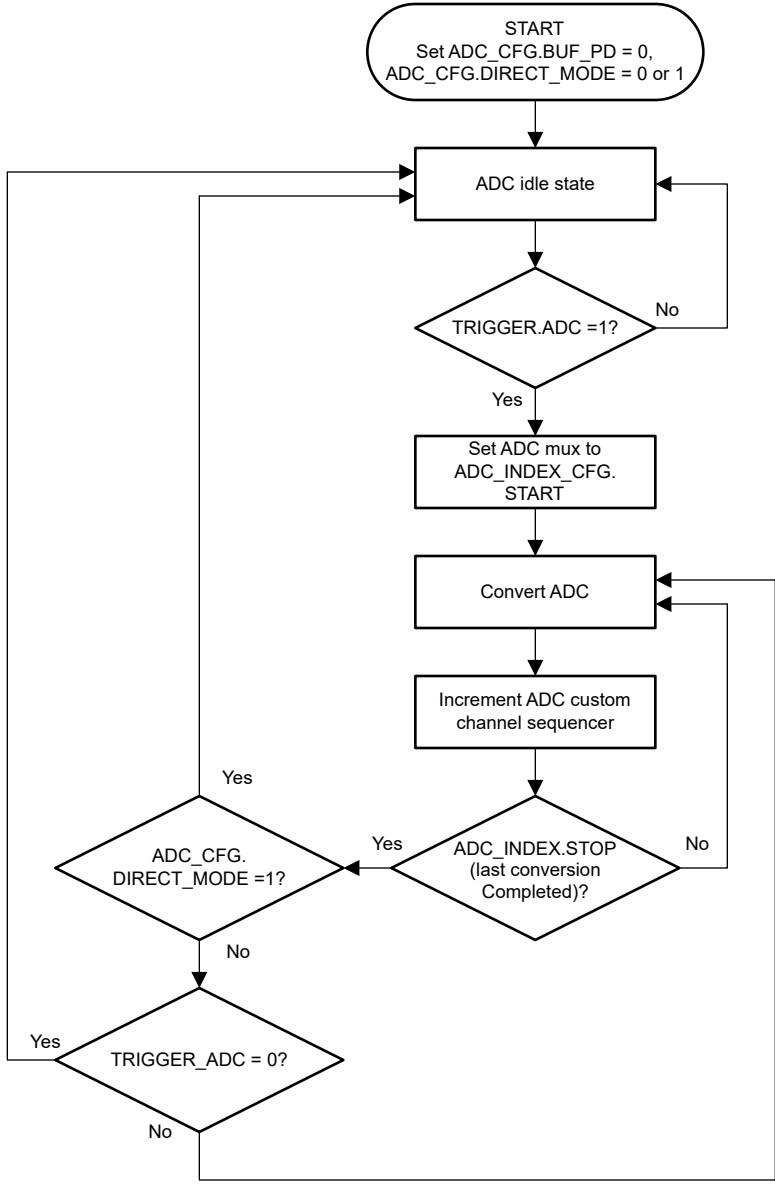
図 6-7. DAC Data Path

### 6.3.2 Analog-to-Digital Converter (ADC) Overview

The AFE82H1 feature a monitoring system centered on a 12-bit successive approximation register (SAR) ADC and a highly flexible analog multiplexer. The monitoring system is capable of sensing up to two external inputs, as well as several internal device signals.

The ADC uses the VREFIO pin voltage as a reference. The ADC timing signals are derived from an on-chip oscillator. The conversion results are accessed through the device serial interface.

#### 6.3.2.1 ADC Operation

The device ADC supports direct-mode and auto-mode conversions. Both conversion modes use a custom channel sequencer to determine which of the input channels are converted by the ADC. The sequence order is fixed. The user selects the start channel and stop channel of the conversion sequence. The conversion method and channel sequence are specified in the ADC Configuration registers. The default conversion method is auto-mode.  shows the ADC conversion sequence.

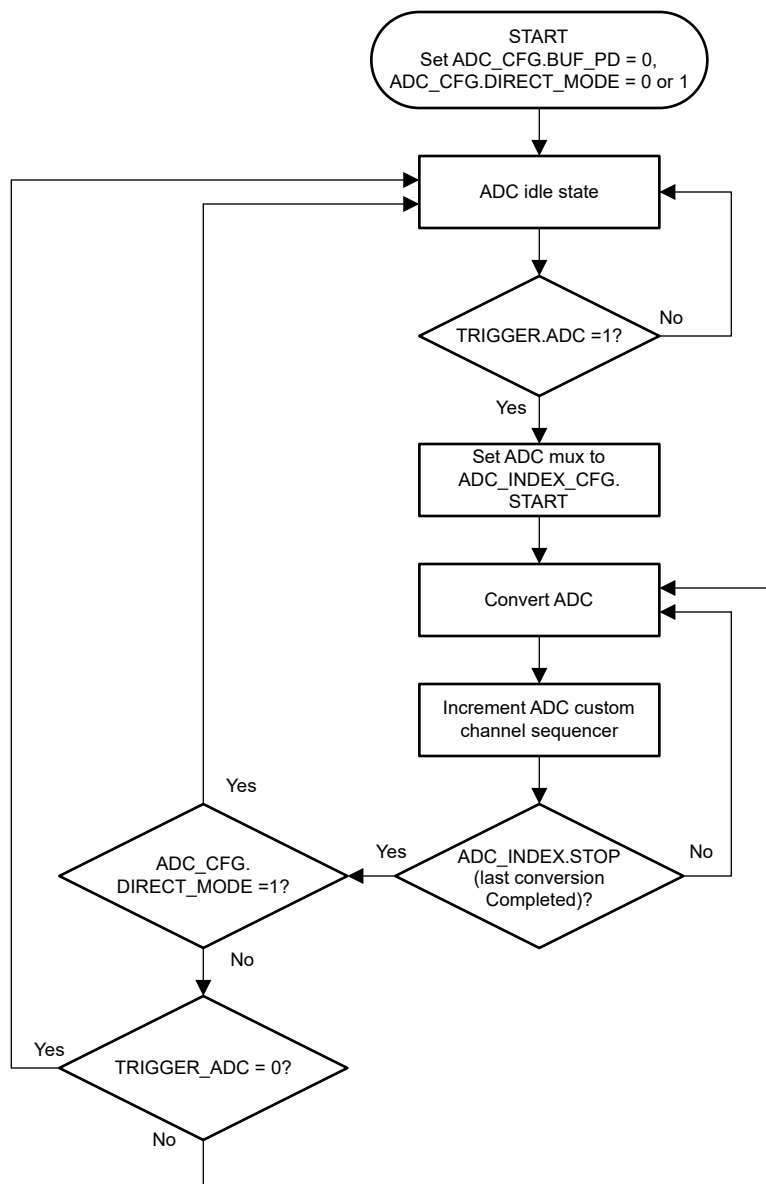


図 6-8. ADC Conversion Sequence



To use the ADC, first enable the ADC buffer by setting `ADC_CFG.BUF_PD = 0`. Then wait at least 210  $\mu$ s before setting the trigger using the `TRIGGER.ADC` bit. An internal delay is forced if the trigger signal is sent before the timer has expired. Make sure the ADC is not converting before setting the `ADC_CFG.BUF_PD = 1`. If `ADC_CFG.BUF_PD` is set to 1 while the ADC is still converting, the internal timer delays this command. When the timer expires, the enable signal for the ADC is cleared, and the current conversion finishes before powering down the ADC and the ADC Buffer.

A trigger signal must occur for the ADC to exit the idle state. The ADC trigger is generated through the `TRIGGER.ADC` bit. The ADC data registers have the latest available data. Accessing the data registers does not interfere with the conversion process, and thus provides continuous ADC operation.

In direct-mode conversion, the selected ADC input channels are converted on demand by issuing an ADC trigger signal. After the last enabled channel is converted, the ADC enters the idle state and waits for a new trigger. Read the results of the ADC conversion through the register map. Direct-mode conversion is typically used to gather the ADC data of any of the data channels. In direct-mode, use the `ADC_BUSY` bit to determine when a direct-mode conversion is complete and the ADC has returned to the idle state. Direct mode is set by writing `ADC_CFG.DIRECT_MODE = 1`.

In auto-mode conversion, the selected ADC input channels are converted continuously. The conversion cycle is initiated by issuing an ADC trigger. Upon completion of the first conversion sequence, another sequence is automatically started. Conversion of the selected channels occurs repeatedly until the auto-mode conversion is stopped by clearing the ADC trigger signal. Auto-mode conversion is not typically used to gather the ADC data. Instead, auto-mode conversions are used in combination with upper and lower ADC data thresholds to detect when the data has exceeded the programmable out-of-range alarm thresholds. Auto mode is set by writing `ADC_CFG.DIRECT_MODE = 0`.

Regardless of the selected conversion method, update the ADC configuration register only while the ADC is in the idle state. Do not change the ADC configuration bits while the ADC is converting channels. Before changing configuration bits, disable the ADC and verify that `GEN_STATUS.ADC_BUSY = 0`.

### 6.3.2.2 ADC Custom Channel Sequencer

The device uses a custom channel sequencer to control the multiplexer of the ADC. The ADC sequencer allows the user to specify which channels are converted. The sequencer consists of 16 indexed slots with programmable start and stop index fields to configure the start and stop conversion points.

In direct-mode conversion, the ADC converts from the start index to the stop index once and then stops. In auto-mode conversion, the ADC converts from the start to stop index repeatedly until the ADC is stopped. 図 6-9 shows the indexed custom channel sequence slots available in the device.

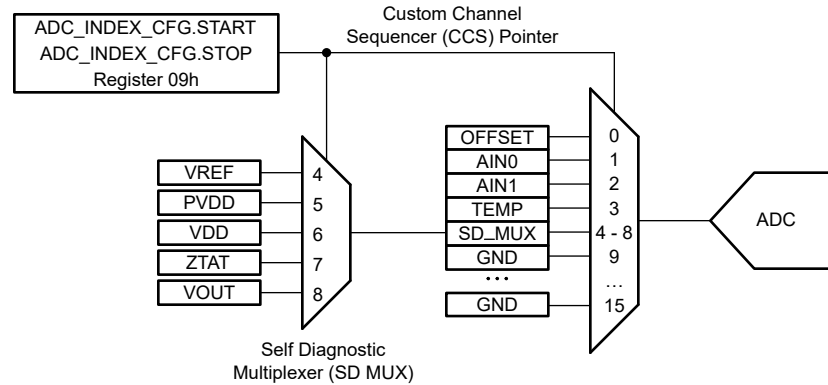


図 6-9. ADC MUX Control

表 6-3 lists the ADC input channel assignments for the sequencer.

表 6-3. Indexed Custom Channel Sequence

CCS POINTER	CHANNEL	CONV_RATE	RANGE
0	OFFSET	2560 Hz	VREF
1	AIN0	Programmable	Programmable
2	AIN1	Programmable	Programmable
3	TEMP	2560 Hz	VREF
4	SD0 (VREF)	2560 Hz	VREF
5	SD1 (PVDD)	2560 Hz	VREF
6	SD2 (VDD)	2560 Hz	VREF
7	SD3 (ZTAT)	2560 Hz	VREF
8	SD4 (VOUT)	2560 Hz	2 × VREF
9-15	GND	2560 Hz	VREF

Use the ADC\_INDEX\_CFG register to select the channels. The order of the channels is fixed and shown in 表 6-3. Then, use ADC\_INDEX\_CFG.START and ADC\_INDEX\_CFG.STOP to select the range of indices to convert. If these two values are the same, then the ADC only converts a single channel. If the START and STOP values are different, then the ADC cycles through the corresponding indices. By default, all channels are configured to be converted; START = 0 and STOP = 8. If the AIN1 channel is not configured as an ADC input, then the result for this channel is 0x000. The minimum time for a conversion is still allotted to AIN1 if the channel is within the START and STOP range. If START is configured to be greater than STOP, then the device interprets the conversion sequence as if START = STOP.

In direct mode, each selected channel in the ADC\_INDEX\_CFG register is converted once per TRIGGER.ADC command. In auto mode, each channel selected in the ADC\_INDEX\_CFG register is converted once; after the last channel, the loop is repeated as long as the ADC is enabled. In auto mode, writing to TRIGGER.ADC = 1 starts the conversions. Writing TRIGGER.ADC = 0 disables the ADC after the current channel being converted

finishes. In direct mode, writing `TRIGGER.ADC = 1` starts the sequence. When the sequence ends, then `TRIGGER.ADC` is self-cleared.

A minimum of 20 clock cycles is required to perform one conversion. The ADC clock is derived from the internal oscillator and divided by 16, which gives an ADC clock frequency of  $1.2288 \text{ MHz} / 16 = 76.8 \text{ kHz}$ , for a clock period = 13.02  $\mu\text{s}$ .

Each of the internal nodes has a fixed conversion rate. Pins `AIN0` and `AIN1` have programmable conversion rates (see also the `ADC_CFG` register). Pins `AIN0` and `AIN1` also have a configurable range. The input range can be either 0 V to 1.25 V or 0 V to 2.5 V, depending on the `ADC_CFG.RANGE` bit.

If any ADC configuration bits are changed, the following sequence is recommended:

1. Disable the ADC
2. Wait for `ADC_BUSY` to go low
3. Change the configuration
4. Restart the conversions

`ADC_BUSY` can be monitored in the `GEN_STATUS` register.

If the ADC is configured for direct mode (`ADC_CFG.DIRECT_MODE = 1`), then after setting the desired channels to convert, write a 1 to `TRIGGER.ADC`. This bit is self-cleared when the sequence is finished converting. This command converts all the selected channels once. To initiate another conversion of the channels, send another `TRIGGER.ADC` command.

#### **6.3.2.3 ADC Synchronization**

The trigger signal must be generated for the ADC to exit the idle state and start conversions. The ADC trigger is generated through the `TRIGGER.ADC` bit. The ADC data registers have the latest available data. Accessing the data registers does not interfere with the conversion process, and thus provides continuous ADC operation.

In direct-mode, use the `GEN_STATUS.ADC_BUSY` bit to determine when a direct-mode conversion is complete, and the ADC has returned to the idle state. Similarly, monitor the `TRIGGER.ADC` bit to see if the ADC has returned to the idle state.

#### **6.3.2.4 ADC Offset Calibration**

Channel 0 of the CCS pointer is named `OFFSET`. The `OFFSET` channel is used to calibrate and improve the ADC offset performance. Convert the `OFFSET` channel, and use the result as a calibration for the ADC offset in subsequent measurements.

This ADC channel samples  $V_{REF} / 2$  and compares this result against 7FFh as a measure of the ADC offset. The data rate for the ADC measuring this channel is 2560 Hz. The ADC conversion for the `OFFSET` channel is subtracted from 7FFh and the resulting value is stored in `ADC_OFFSET` (28h). The offset can be positive or negative; therefore, the value is stored in 2's complement notation.

With the subtraction from 7FFh, `ADC_OFFSET` is the negative of the offset. This value is subtracted from conversions of the ADC by default. For direct measurements of the ADC, set `ADC_BYP.OFST_BYP_EN` to 1 to enable the offset bypass; see [セクション 6.3.2.8](#).

### 6.3.2.5 External Monitoring Inputs

The AFE882H1 have two analog inputs for external voltage sensing. Channels 1 and 2 for the CCS pointer are for external monitoring inputs that can be measured by pins AIN0 and AIN1, respectively. The input range for the analog inputs is configurable to either 0 V to 1.25 V or 0 V to 2.5 V. The analog inputs conversion values are stored in straight binary format in the ADC registers. The ADC resolution can be computed by 式 7:

$$1 \text{ LSB} = \frac{V_{\text{RANGE}}}{2^{12}} \quad (7)$$

where

- $V_{\text{RANGE}} = 2.5 \text{ V}$  for the 0-V to 2.5-V input range or 1.25 V for the 0-V to 1.25-V input range.

図 6-10 and 表 6-4 detail the transfer characteristics.

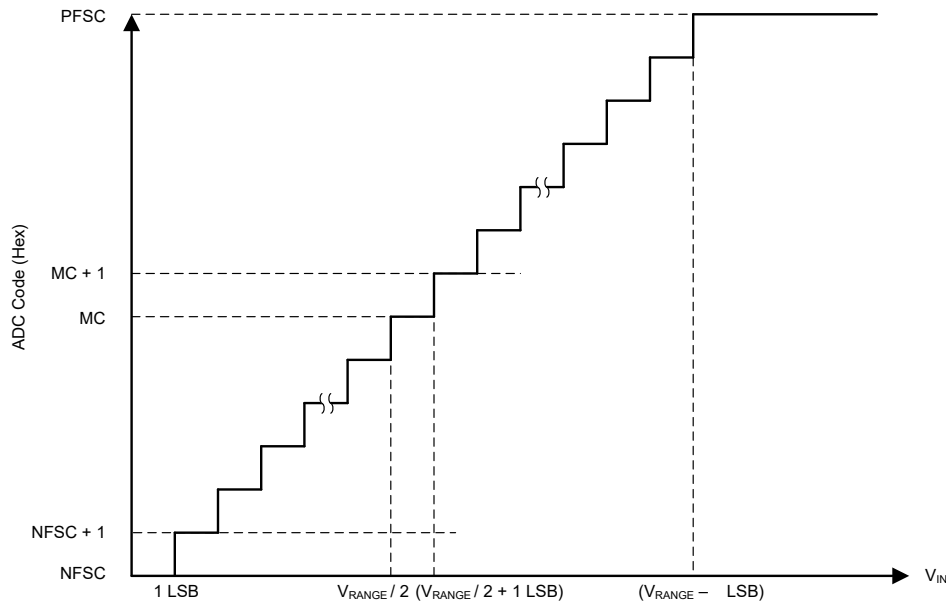


図 6-10. ADC Transfer Characteristics

表 6-4. Transfer Characteristics

INPUT VOLTAGE	CODE	DESCRIPTION	IDEAL OUTPUT CODE
$\leq 1 \text{ LSB}$	NFSC	Negative full-scale code	000
1 LSB to 2 LSB	NFSC + 1	Negative full-scale code plus 1	001
$(V_{\text{RANGE}} / 2) \text{ to } (V_{\text{RANGE}} / 2) + 1 \text{ LSB}$	MC	Midcode	800
$(V_{\text{RANGE}} / 2) + 1 \text{ LSB to } (V_{\text{RANGE}} / 2) + 2 \text{ LSB}$	MC + 1	Midcode plus 1	801
$\geq V_{\text{RANGE}} - 1 \text{ LSB}$	PFSC	Positive full-scale code	FFF

For these external monitoring inputs, the ADC is configurable for both data rate and voltage range. The data rate is set to either 640 Hz, 1280 Hz, 2560 Hz, or 3840 Hz with the ADC\_CFG.CONV\_RATE bits. The range of the ADC measurement is set with the ADC\_CFG.AIN\_RANGE bit. The ADC range is  $2 \times V_{\text{REF}}$  when the bit = 0; the ADC range is  $V_{\text{REF}}$  when the bit = 1.

When the ADC conversion is completed for AIN0 and AIN1, the resulting ADC data are stored in the ADC\_AIN0.DATA and ADC\_AIN1.DATA bits at 24h and 25h of the register map.

If the external monitoring inputs are not used, connect the AIN0 and AIN1 pins to GND through a 1-kΩ resistor.

### 6.3.2.6 Temperature Sensor

Channel 3 of the CCS is used to measure the die temperature of the device. The ADC measures an internal temperature sensor that measures a voltage complementary to the absolute temperature (CTAT). This CTAT voltage has a negative temperature coefficient. The ADC converts this voltage at a data rate of 2560 Hz. When the ADC conversion is completed, the data are found in the ADC\_TEMP.DATA bits (address 26h).

The relationship between the ambient temperature and the ADC code is shown in 式 8:

$$\text{ADC Code} = 2681 - 11 \times T_A(^{\circ}\text{C}) \quad (8)$$

### 6.3.2.7 Self-Diagnostic Multiplexer

In addition to the ADC offset, the two external monitoring inputs, and the temperature sensor, the ADC of the AFEx82H1 has five other internal inputs to monitor the reference voltage, the power supplies, a static voltage, and the DAC output. These five voltages measurements are part of the self-diagnostic multiplexer (SD0 to SD4) measurements of the ADC, and are reported in the ADC\_SD\_MUX register at 27h; see also セクション 7.

Channel 4 (SD0) measures the reference voltage of the device. The ADC measures the reference voltage through a resistor divider (divide by two). Be aware that all ADC measurements are a function of the reference; using SD0 to measure the reference is not revealing as a diagnostic measurement. The data rate for this conversion is 2560 Hz and the range of the ADC is set to VREF.

Channel 5 (SD1) measures the PVDD power supply of the device. The ADC measures the PVDD voltage through a resistor divider (divide by six). The data rate for this conversion is 2560 Hz and the range of the ADC is set to VREF.

Channel 6 (SD2) measures the VDD power supply of the device. When channel 6 is selected, the ADC measures the VDD voltage through a resistor divider (divide by 2). The data rate for this conversion is 2560 Hz and the range of the ADC is set to VREF.

Channel 7 (SD3) is a ZTAT (zero temperature coefficient) voltage. This internal voltage is nominally 0.6 V with a low temperature drift and does not depend on the reference voltage. An ADC measurement of ZTAT voltage can be useful to determine the state of the reference voltage. The data rate for this conversion is 2560 Hz and the range of the ADC is set to VREF.

Channel 8 (SD4) measures the VOUT of the DAC. The ADC measures the VOUT voltage through a resistor divider (divide by two). The data rate for this conversion is 2560 Hz and the range of the ADC is set to  $2 \times \text{VREF}$ .

### 6.3.2.8 ADC Bypass

To test the offset, modify the ADC data path by programming the bypass data register, ADC\_BYP.DATA (2Eh). This read/write register is used in two different ways.

First, by setting the ADC\_BYP.OFST\_BYP\_EN to 1, this bypass data register is used as a substitute for the ADC\_OFFSET. However, if the ADC\_BYP.DATA data must be stored in the ADC\_OFFSET register, use the second method.

Second, the ADC\_BYP.DATA is used to set a known value into the ADC readback register of the channel being converted. Write the desired data into ADC\_BYP.DATA, set the ADC\_BYP.DATA\_BYP\_EN bit, and convert the selected channel. When ADC\_BYP.DATA\_BYP\_EN bit is set to 1, the ADC conversion is bypassed, and the value of ADC\_BYP.DATA is written into the selected ADC channel readback register. This setting is used to test the alarm settings of the ADC.

When the ADC bypass is unused, set the ADC\_BYP.DATA to 000h.

図 6-11 shows the ADC bypass data flow.

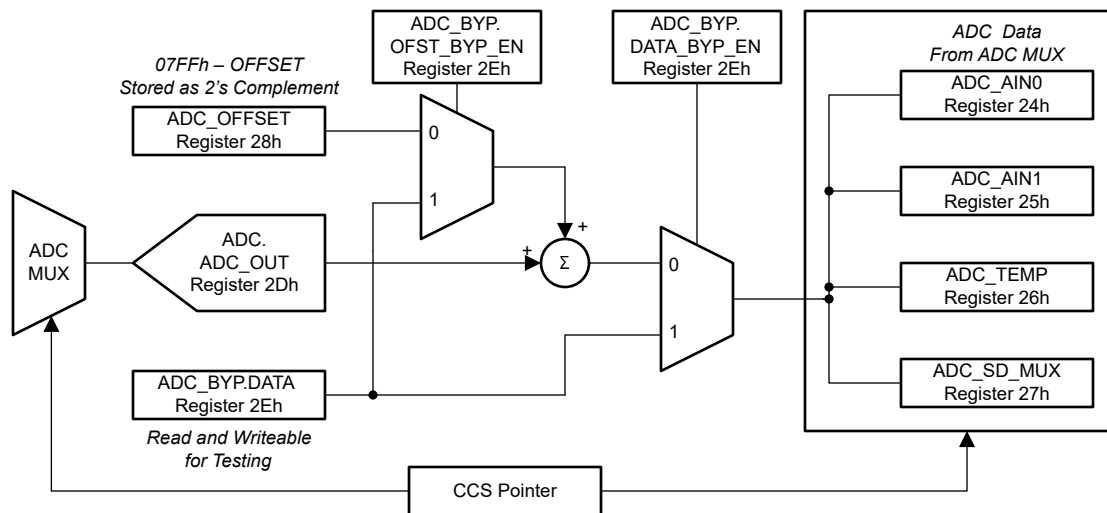


図 6-11. ADC Bypass Data Flow

### 6.3.3 Programmable Out-of-Range Alarms

The AFE882H1 are capable of continuously analyzing the supplies, external ADC inputs, DAC output voltage, reference, internal temperature, and other internal signals for normal operation.

Normal operation for the conversion results is established through the lower- and upper-threshold registers. When any of the monitored inputs are out of the specified range, the corresponding alarm bit in the alarm status registers is set.

The alarm bits in the alarm status registers are latched. The alarm bits are referred to as being latched because the alarm bits remain set until read by software. This design makes sure that out-of-limit events cannot be missed if the software is polling the device periodically. All bits are cleared when reading the alarm status registers, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle. When the alarm event is cleared, the DAC is reloaded with the contents of the DAC active registers, which allows the DAC outputs to return to the previous operating point without any additional commands

All alarms can be used to generate a hardware interrupt signal on the  $\overline{\text{ALARM}}$  pin; see also [セクション 6.3.3.1](#). In addition, [セクション 6.3.3.2](#) describes how the alarm action can be individually configured for each alarm.

### 6.3.3.1 Alarm-Based Interrupts

One or more of the available alarms can be set to activate the  $\overline{\text{ALARM}}$  pin. Connect the  $\overline{\text{ALARM}}$  pin as an optional hardware interrupt to the host. The host can query the alarm status registers to determine the alarm source upon assertion of the interrupt. Any alarm event activates the pin, as long as the alarm is not masked in the `ALARM_STATUS_MASK` register. When an alarm event is masked, the occurrence of the event sets the corresponding status bit in the alarm status registers, but does not activate the  $\overline{\text{ALARM}}$  pin.

#### 注

The  $\overline{\text{ALARM}}$  pin output depends on `ALARM_STATUS` and `ALARM_STATUS_MASK` register settings, independent of `ALARM_ACT` register settings.

### 6.3.3.2 Alarm Action Configuration Register

The AFE82H1 provides an alarm action configuration register: `ALARM_ACT`, 表 7-17. Writing to this register selects the device action that automatically occurs for a specific alarm condition. The `ALARM_ACT` register determines how the main DAC responds to an alarm event from either an ADC conversion on the self-diagnostics channels (`AIN0`, `AIN1`, and `TEMP`), or from a CRC, WDT, VREF, `TEMP_HI`, or `TEMP_LO` fault. Only these faults cause a response by the DAC. Any other alarm status events trigger the  $\overline{\text{ALARM}}$  pin. There are four options for alarm action. In case different settings are selected for different alarm conditions, the following low-to-high priority is considered when taking action:

- 0. → No action
- 1. → DAC CLEAR state
- 2. → VOUT alarm voltage
- 3. → VOUT Hi-Z

If option 1 is selected when the alarm event occurs, then the DAC is forced to the clear code. This operation is done by controlling the input code to the DAC.

If option 2 is selected when the alarm event occurs, then VOUT is forced to the alarm voltage. The alarm voltage is controlled by either pin or register bit. If `SPECIAL_CFG.AIN1_ENB` = 0, then the `AIN1` pin controls alarm polarity. Also, register bit `SPECIAL_CFG.ALMV_POL` can be used. If either of these signals = 1, then the alarm voltage is high; otherwise, the alarm voltage is low. The `SPECIAL_CFG` register is only reset with POR, so the user setting remains intact through hardware or software resets.

If option 3 is selected when the alarm event occurs, then the VOUT buffer is put into Hi-Z. If multiple events occur, then the highest setting takes precedence. Option 3 has the highest priority.

To disable action response to an alarm, set the corresponding bits in `ALARM_ACT` to 0h. Alarm action response is cleared either when the triggered condition bit resets (behavior depends on whether the fault bit in `ALARM_STATUS` is sticky or not), or by changing the action configuration to 0h.

#### 注

An alarm action, as configured, executes when an alarm occurs depending on `ALARM_STATUS` and `ALARM_ACT` registers. Action response is independent of `ALARM_STATUS_MASK` settings.



### 6.3.3.3 Alarm Voltage Generator

Figure 6-12 shows that the alarm voltage is generated independently from the DAC output voltage. The alarm polarity control logic selects the output level of the alarm voltage generator. The alarm action control logic selects between the DAC output and alarm voltage generator output voltages. The alarm action control logic also controls the output buffer Hi-Z switch.

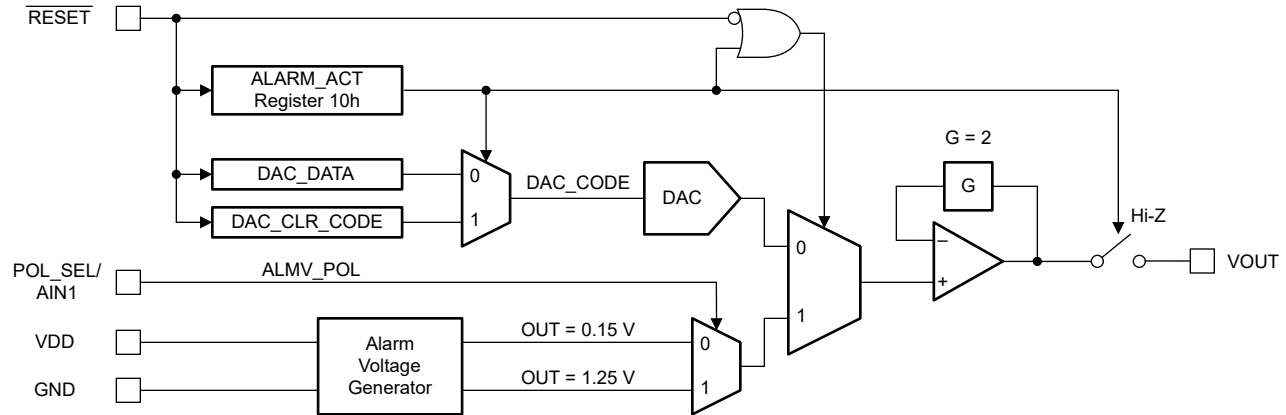


Figure 6-12. Alarm Voltage Generator Architecture

During normal operation, the expected VOUT voltage depends on the DAC\_CODE. The ADC thresholds for the SD4 (VOUT) diagnostic channel are set around the programmed DAC\_CODE. During the alarm condition, if the alarm action changes the VOUT voltage to the alarm voltage, or switches the VOUT buffer into Hi-Z mode, the VOUT voltage no longer depends on the DAC\_CODE. In this case, the SD4 (VOUT) diagnostic channel also reports the alarm. To clear this alarm, as long as all other alarm conditions are cleared, set the alarm action to either no action or to the DAC clear code. Applying either alarm action sets the VOUT voltage within the expected ADC thresholds and clears the alarm after the next ADC measurement of the SD4 (VOUT) channel.

Give special consideration to the alarm logic during the transient events. When the new DAC\_CODE goes beyond the SD4 (VOUT) alarm thresholds with the ADC monitoring the SD4 (VOUT) input in auto mode, the ADC conversion can occur while VOUT settles to a new value. This conversion can trigger a false alarm. There are two ways to prevent this false alarm:

1. Use direct mode and allow VOUT to settle before triggering the next ADC conversion.
2. Set ADC\_CFG.FLT\_CNT > 0. With this configuration, a single error in SD4 or any other measurement does not cause an alarm condition to be asserted.

### 6.3.3.4 Temperature Sensor Alarm Function

The AFE882H1 continuously monitor the internal die temperature. In addition to the ADC measurement, the temperature sensor triggers a comparator to show a thermal warning and a thermal error. A thermal warning alarm is set when the temperature exceeds 85°C. Additionally, a thermal error alarm is set when the die temperature exceeds 130°C.

The thermal warning and thermal error alarms can be configured to set the  $\overline{\text{ALARM}}$  pin and are indicated in the ALARM\_STATUS register. These alarms can be masked with the ALARM\_MASK register and also be configured to control the DAC output with the ALARM\_ACT register.

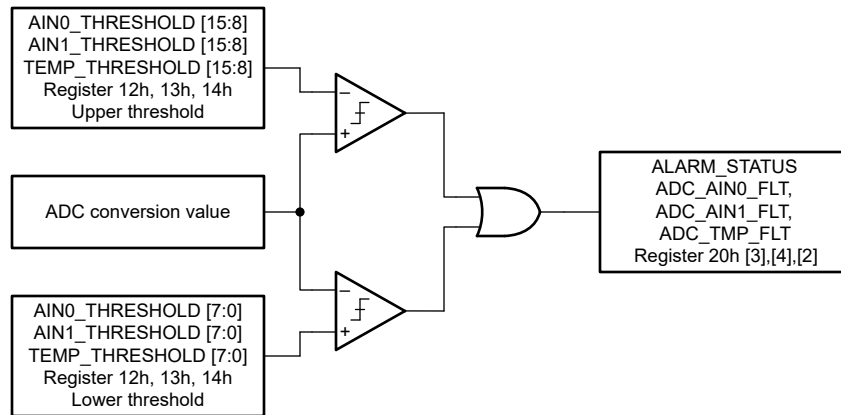
### 6.3.3.5 Internal Reference Alarm Function

The devices provide out-of-range detection for the reference voltage. When the reference voltage exceeds  $\pm 5\%$  of the nominal value, the reference alarm flag (VREF\_FLT bit) is set. Make sure that a reference alarm condition has not been issued by the device before powering up the DAC output.



### 6.3.3.6 ADC Alarm Function

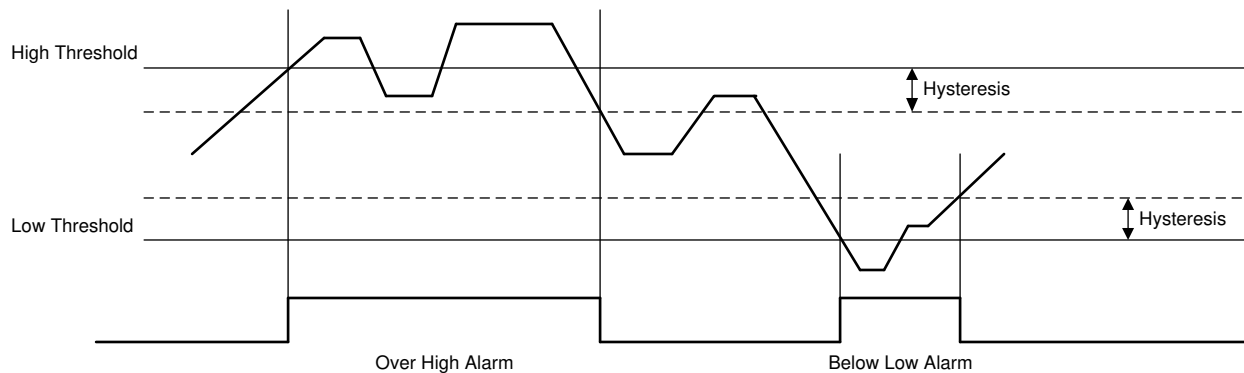
The AFEx82H1 provide independent out-of-range detection for each of the ADC inputs. [Figure 6-13](#) shows the out-of-range detection block. When the measurement is out of range, the corresponding alarm bit is set to flag the out-of-range condition.



**Figure 6-13. ADC Out-of-Range Alarm**

An alarm event is only registered when the monitored signal is out of range for  $N$  number of consecutive conversions, where  $N$  is configured in the ADC\_CFG.FLT\_CNT false alarm register settings. If the monitored signal returns to the normal range before  $N$  consecutive conversions, an alarm event is not issued.

If an ADC input signal is out of range and the alarm is enabled, then the corresponding alarm bit is set to 1. However, the alarm condition is cleared only when the conversion result returns to a value less than the high-limit register setting and greater than the low-limit register setting by the number of codes specified by the hysteresis setting (see [Figure 6-14](#)). The hysteresis is a programmable value between 0 LSB to 127 LSB in the ADC\_CFG.HYST register.



**Figure 6-14. ADC Alarm Hysteresis**

### 6.3.3.7 Fault Detection

There are two fields within the ADC\_CFG register: FLT\_CNT and HYST. These fields are applied to the assertion and deassertion of alarm conditions for all the ADC channels.

ADC\_CFG.FLT\_CNT determines the maximum number of accepted consecutive failures before an alarm condition is reported. For example, if ADC\_CFG.FLT\_CNT is set for two counts, then three consecutive conversions must be outside of the thresholds to trigger an alarm. Each failure counts towards the FLT\_CNT limit even if the failures alternate between high threshold and low threshold.

ADC\_CFG.HYST sets the hysteresis used by the alarm-detection circuit. After an alarm is triggered, the hysteresis is applied before the alarm condition is released. In the case of the high threshold, the hysteresis is subtracted from the threshold value. In the case of the low threshold limit, the hysteresis is added to the threshold value.

Channels AIN0, AIN1, and TEMP have high and low thresholds associated with them. If a conversion value falls outside of these limits (that is, if  $TEMP < \text{low threshold}$  or  $TEMP > \text{high threshold}$ ), an alarm condition for that channel is set. The alarms are disabled by setting 0x000 for the low threshold and 0xFFF for the high threshold, respectively. These alarms are disabled by default. Because the configuration fields for the thresholds are only eight bits wide, the four LSBs are hardcoded for each threshold. The high thresholds four LSBs are hardcoded to 0xF, and the low thresholds four LSBs are hardcoded to 0x0.

All the self diagnostic (SD) channels have fixed thresholds, except SD4, which measures the VOUT of the main DAC. The threshold for SD4 tracks the VOUT with respect to the DAC code. 表 6-5 shows the calculations used to determine the high and low ADC thresholds for each SD channel. The limits in the two right-most columns are determined by the threshold columns to the left and given some margin. The four LSBs are assigned as described previously.

**表 6-5. Self Diagnostic (SD) Alarm ADC Thresholds**

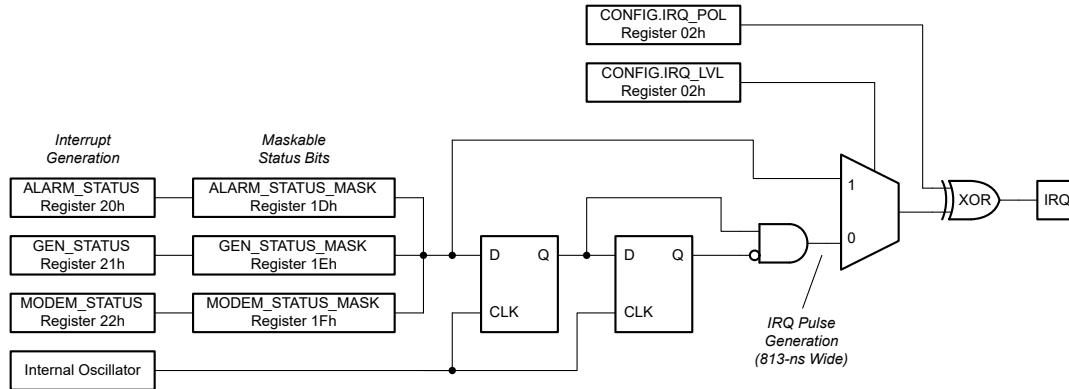
SD	ADC INPUT	ACCEPTED LOW VALUE	ACCEPTED HIGH VALUE	LOW THRESHOLD	HIGH THRESHOLD	ADC LOW (HEX)	ADC HIGH (HEX)
SD0	VREF/2	$VREF/2 - 9\% - 25 \text{ mV}$	$VREF/2 + 9\% + 25 \text{ mV}$	0.54375 V	0.70625 V	0x6D0	0x92F
SD1	PVDD/6	$1.65/6 - 25 \text{ mV}$	$6/6 + 25 \text{ mV}$	0.25 V	1.025 V	0x310	0xD3F
SD2	VDD/2	$1.6/2 - 25 \text{ mV}$	$2/2 + 25 \text{ mV}$	0.775 V	1.025 V	0x9C0	0xD3F
SD3	0.6 V	$0.6 \text{ V} - 9\% - 25 \text{ mV}$	$0.6 \text{ V} + 9\% + 25 \text{ mV}$	0.521 V	0.679 V	0x690	0x8CF
SD4	VOUT/2	$VOUT/2 - 6 \text{ mV}$	$VOUT/2 + 6 \text{ mV}$	$VOUT - 12 \text{ mV}$	$VOUT + 12 \text{ mV}$	Expected - 0x040	Expected + 0x040

The alarm threshold for the SD4 input depends on the expected ADC measurement based on the DAC code. 式 9 shows the expected ADC code for SD4.

$$\text{ADC Expected Code} = \text{DAC\_CODE}[\text{MSB}:\text{MSB}-11] \quad (9)$$

### 6.3.4 IRQ

The devices include an interrupt request (IRQ) to communicate the occurrence of a variety of events to the host controller. The IRQ block initiates interrupts that are reported internally in a status register, externally on the IRQ pin if the function is enabled, or on the  $\overline{\text{ALARM}}$  pin if the condition is from the ALARM\_STATUS register. [Figure 6-15](#) shows the IRQ block diagram.



**Figure 6-15. IRQ Block Diagram**

There are three registers that can generate interrupts: GEN\_STATUS, MODEM\_STATUS, and ALARM\_STATUS. Each of these registers has a corresponding STATUS\_MASK register. The mask register controls which of the events trigger an interrupt. Writing a 1 in the mask register masks, or disables, the event from triggering an interrupt. Writing a 0 in the mask register allows the event to trigger an IRQ. All bits are masked by default. Some status bits are sticky. Reading the corresponding register clears a sticky bit, unless the condition still exists.

The IRQ is configured through CONFIG.IRQ\_LVL to be edge- or level-sensitive. Set this bit to logic 1 to enable level-sensitive functionality (default). In edge-sensitive mode, the IRQ signal is a synchronous pulse, one internal clock period wide (813 ns). In level-sensitive mode, the IRQ is set and remains set as long as the condition exists. After the IRQ condition is removed, the condition is cleared by reading the corresponding status register. Trying to clear the bit while the condition still exists does not allow the bit to be cleared if the bit is sticky.

CONFIG.IRQ\_POL determines the active level of the IRQ. A logic 1 configures IRQ to be active high.

When using edge-sensitive IRQ signals, there is a clock cycle delay for synchronization and edge detection. With a 307.2-kHz clock, this delay is up to 3.26  $\mu$ s. For level-sensitive mode, the delay is approximately 10 ns to 20 ns.

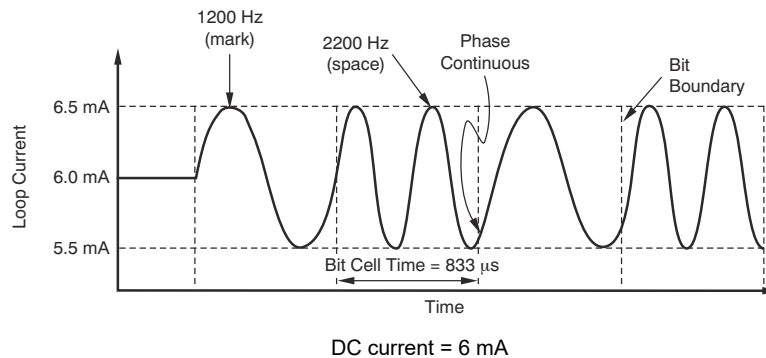
Most status bits have two versions within the design. The first version is an edge event that is created when the status is asserted. This signal is used to generate edge-sensitive IRQs. This edge detection prevents multiple status events from blocking one another. The second version is the sticky version of the status bit. This signal is set upon assertion of the status bit and cleared when the corresponding status register is read, as long as the status condition does not still persist. Signals GEN\_IRQ, MODEM\_IRQ, and ALARM\_IRQ are driven by the logical OR of the of the status bits within the corresponding register.

If a status bit is unmasked and the sticky version of that bit has been asserted, and the IRQ is level-sensitive, then an interrupt is triggered as soon as the bit is unmasked. If the IRQ is edge-sensitive then a status event must occur after the bit has been unmasked to assert an interrupt.

FIFO flags are not sticky; therefore, an IRQ can be triggered, but the status flag can be deasserted by the time the status information is transmitted at the output. For example, If FIFO\_U2H\_LEVEL\_FLAG is unmasked and the FIFO\_U2H level drops below the set threshold, the IRQ triggers. If the device is configured to output UBM IRQ messages and a HART data byte is received on UARTIN after the IRQ, but before the UBM captures the IRQ status, then the IRQ status and data information reads back all zeros. If UBM IRQ mode is used, wait until the IRQ message is fully transmitted on UARTOUT before putting data on UARTIN.

### 6.3.5 HART Interface

On the AFE82H1, a HART frequency-shift keyed (FSK) signal can be modulated onto the MOD\_OUT pin. [Figure 6-16](#) illustrates the output current versus time operation for a typical HART interface.



**Figure 6-16. Output Current vs Time**

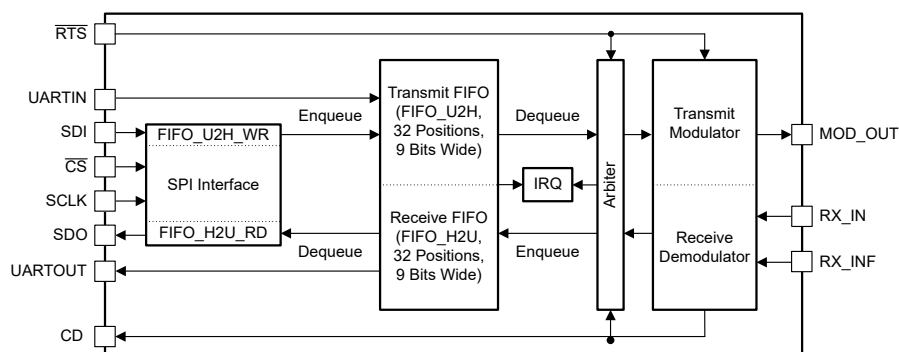
To enable the HART interface, set the HART\_EN bit in the MODEM\_CFG register. An external capacitor, placed in series between the RX\_IN pin and HART FSK source, is required to ac-couple the HART FSK signal to the RX\_IN pin. The recommended capacitance for this external capacitor is 2.2 nF.

If additional filtering is required, the AFE82H1 also support an external band-pass filter. For this configuration, use the RX\_INF pin instead of RX\_IN pin.

#### 6.3.5.1 FIFO Buffers

First-in, first-out (FIFO) buffers are used to transmit and receive HART data using both the SPI and UART. Both the transmit FIFO (FIFO\_U2H) and receive FIFO (FIFO\_H2U) buffers are 32 rows and 9-bits wide. The 9-bit width allows the storage of the parity bit with the data byte. Bit[8] is the parity bit as received by either the UART or HART demodulator, depending on the direction of the data flow. The device does not calculate the parity bit in this case, and transmits the data with the wrong parity bit if the wrong parity bit was received. Bits[7:0] are the data.

The AFE82H1 HART implementation is shown in [Figure 6-17](#).



**Figure 6-17. HART Architecture**

HART data bytes are enqueued into a transmit FIFO\_U2H buffer using the SPI or UART. The input data bits are translated into the *mark* (1200 Hz) and *space* (2200 Hz) FSK analog signals (see [Figure 6-16](#)) used in HART communication by the internal HART transmit modulator. The receive demodulator enqueues HART data into the receive FIFO\_H2U buffer. An arbiter is implemented with signals to CD and from the  $\overline{\text{RTS}}$  pins to manage the HART physical connections on MOD\_OUT, and either the RX\_IN or RX\_INF pin. To enable efficient and

error-free communication, the arbiter in conjunction with the two FIFO buffers can be used to produce an IRQ for the system controller.

An incorrect stop bit in the HART receive character causes a HART frame error. The device reports the frame error in the status register and discards the character. When the character is discarded, the HART data are not enqueued into FIFO\_H2U. If the frame error check is not masked, an IRQ event is also triggered.

Similarly, an incorrect stop bit in the UARTIN character causes a UART frame error. The device reports the frame error in the status register and discards the character. When the character is discarded, the UART data are not enqueued into FIFO\_U2H. If the frame error check is not masked, an IRQ event is also triggered.

#### 6.3.5.1.1 FIFO Buffer Access

In SPI only mode, both FIFO buffers are accessed using register addresses. HART bus communication activity is reported to the host controller through the IRQ pin and MODEM\_STATUS register. See [セクション 6.3.5.8](#) for recommended IRQ based communication techniques when using the AFE82H1 to convert between the SPI and HART.

Write to the FIFO\_U2H\_WR register to enqueue the HART transmit data into FIFO\_U2H. Calculate the correct parity bit and include the parity bit with the data. Do not attempt to read data from the FIFO\_U2H because a read request from the FIFO\_U2H\_WR register is not supported. The read from the FIFO\_U2H\_WR register returns the data from the dequeue pointer location of FIFO\_U2H, but does not dequeue the data.

Read the FIFO\_H2U\_RD register to dequeue the HART receive data from FIFO\_H2U. If CRC is enabled and a CRC error occurs during a read request, no data are dequeued from the FIFO\_H2U buffer, and the data in the readback frame are invalid. A write to the FIFO\_H2U\_RD register is ignored.

When communicating with the HART modem through the UART interface in SPI plus UART mode, any character received on the UARTIN pin is directly enqueued into FIFO\_U2H. The character is then automatically dequeued from FIFO\_U2H and transmitted on the MOD\_OUT pin when the clear-to-send (CTS) response is asserted. Similarly, any character received on the RX\_IN or RX\_INF pin is directly enqueued into FIFO\_H2U. The character is then automatically dequeued from FIFO\_H2U and transmitted on UARTOUT as a normal UART character.

The FIFO buffers are accessed directly by the UART; therefore, do not use the FIFO\_U2H\_WR and FIFO\_H2U\_RD registers with the SPI. As a result of using FIFO\_U2H in the data path, there is a latency from the UARTIN pin to the MOD\_OUT pin; see also [セクション 6.3.5.6](#). Similarly, as a result of using FIFO\_H2U, there is a latency from the RX\_IN or RX\_INF pin to the UARTOUT pin; see also [セクション 6.3.5.7](#).

HART bus communication activity is interfaced to the host controller through the CD and RTS pins. If the CD and RTS pins are not used, poll the MODEM\_STATUS register regularly to monitor the status of the modem.

In UBM mode, any character received on the UARTIN pin that is not a part of a break command is directly enqueued into FIFO\_U2H. The character is then automatically dequeued from FIFO\_U2H and transmitted on the MOD\_OUT pin when the CTS response is asserted. Although the UBM packets can access all registers, do not use the break command to write the HART transmit data into FIFO\_U2H\_WR register. Use the standard 8O1 UART character format to enqueue data into the FIFO\_U2H buffer, and thus to the HART modulator.

Similarly, do not use the break command to read the HART receive data from the FIFO\_H2U\_RD register. HART receive data are automatically dequeued from FIFO\_H2U and transmitted on UARTOUT as normal UART characters in UBM mode.

#### 6.3.5.1.2 FIFO Buffer Flags

Status bits exist for both transmit and receive FIFO buffers in the MODEM\_STATUS, FIFO\_STATUS and FIFO\_H2U\_RD registers. These include full, empty, and level flags. Buffer level flags are used to trigger IRQs for HART communication; see also [セクション 6.3.5.8](#). The status fields in the FIFO\_H2U\_RD register represent the state of FIFO\_H2U before the read is performed and the data byte is dequeued. This implementation means that if the EMPTY\_FLAG is set, the data byte received in that frame is invalid. Similarly, the LEVEL field represents the 4 MSBs for the FIFO\_H2U level before dequeuing. The LSB is not reported, and there are only

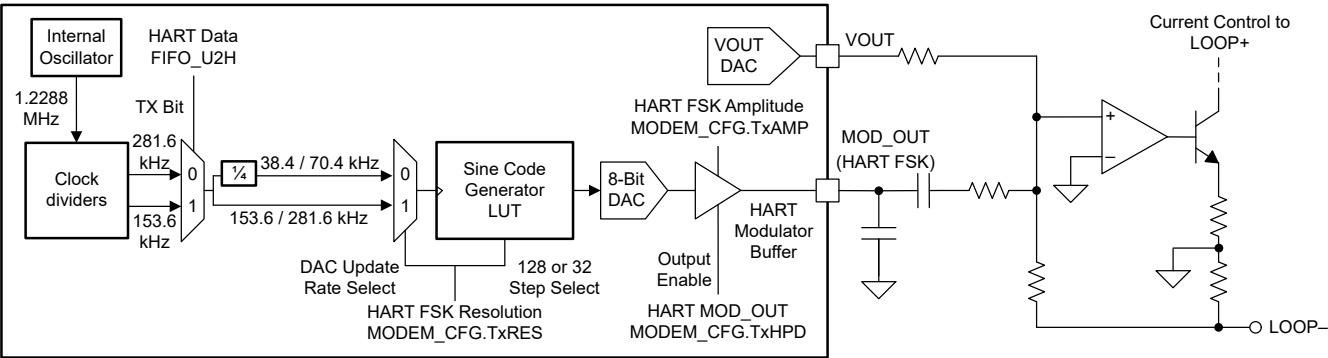
five internal bits to represent 32 levels; therefore, the LEVEL = 0 is reported when the actual level is 0, 1, or 32. Use FULL\_FLAG and EMPTY\_FLAG when LEVEL = 0 to differentiate between these three cases.

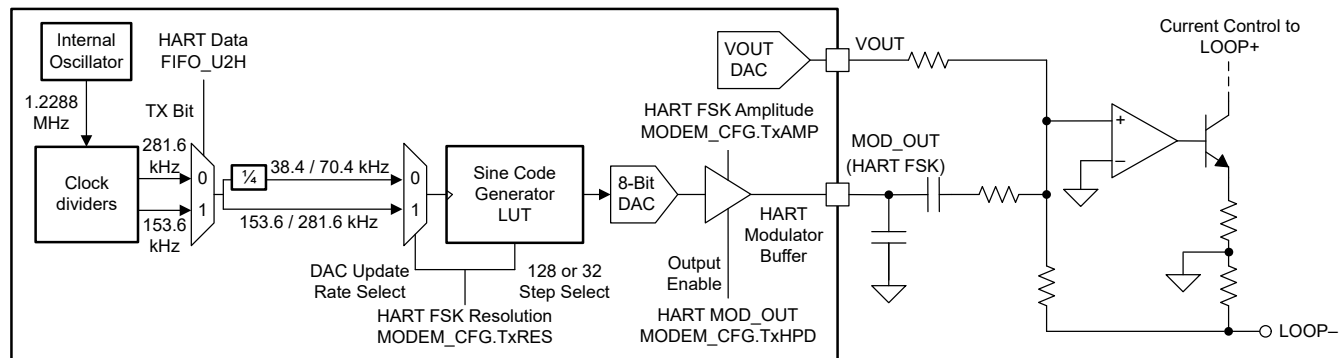
The FIFO\_H2U and FIFO\_U2H buffers have 32 levels; however, the level setting for generating IRQ events only uses four bits. For the receive FIFO\_H2U buffer, the LSB in the FIFO level threshold comparison is always 1 (FIFO\_CFG.H2U\_LEVEL\_SET[3:0], 1). This configuration is designed to alert the user when FIFO\_H2U is getting nearly full so as to enable a timely data dequeue, and prevent the loss of incoming HART data due to FIFO overload. For this reason, the FIFO\_H2U\_LEVEL\_FLAG is also a greater-than (>) comparison to the FIFO\_CFG.H2U\_LEVEL\_SET. For example, if FIFO\_CFG.H2U\_LEVEL\_SET = 4'b1000, then when the level of the FIFO\_H2U > 5'b10001, the FIFO\_H2U\_LEVEL\_FLAG is set. Setting FIFO\_CFG.H2U\_LEVEL\_SET = 4'b1111 (default) effectively disables this flag. Use FIFO\_H2U\_FULL\_FLAG to detect the FIFO\_H2U full event. When the FIFO\_H2U is full, the new incoming data are blocked from enqueueing into the FIFO and ignored to preserve the existing data.

Similarly, for the transmit FIFO\_U2H buffer, the LSB in the FIFO level threshold comparison is always 0 (FIFO\_CFG.U2H\_LEVEL\_SET[3:0], 0). This configuration is designed to alert the user when FIFO\_U2H is getting nearly empty so as to enable a timely data enqueue, and prevent FIFO\_U2H from becoming empty prematurely and causing a gap error on the HART bus. For this reason, the FIFO\_U2H\_LEVEL\_FLAG is also a less-than (<) comparison with the FIFO\_CFG.U2H\_LEVEL\_SET. For example, if FIFO\_CFG.U2H\_LEVEL\_SET = 4'b1000, then when the level of the FIFO\_U2H < 5'b10000, the FIFO\_U2H\_LEVEL\_FLAG is set. Setting FIFO\_CFG.U2H\_LEVEL\_SET = 4'b0000 (default) effectively disables this flag. Use FIFO\_U2H\_EMPTY\_FLAG to detect the FIFO\_U2H empty event.

To avoid buffer overflow, monitor the level of FIFO\_U2H by watching for a buffer-full or buffer-threshold event. If the FIFO\_U2H\_LEVEL\_FLAG bit in the MODEM\_STATUS\_MASK register is set to 0, the IRQ pin toggles when the threshold is exceeded. Similarly, an alarm can be triggered based on the FIFO\_U2H\_FULL\_FLAG bit in the MODEM\_STATUS register. When the FIFO\_U2H is full the new incoming data are blocked from enqueueing into the FIFO and ignored to preserve the existing data.

### 6.3.5.2 HART Modulator

The HART modulator implements a look-up table (LUT) containing 128, 8-bit, signed values that represent a single-phase, continuous sinusoidal cycle. A counter is implemented that incrementally loads the table values to a DAC at a clock frequency determined by the binary value of the input data. The DAC clock frequency is determined by the logical value of the data bit being transmitted. A logic 1 transmits at the internal clock frequency of 32 (default) steps times 1200 Hz. A logic 0 transmits at the internal clock frequency of 32 (default) steps times 2200 Hz. All frequencies are derived from 1.2288 MHz. This process creates the *mark* and *space* analog output signals used to represent HART data. The default mode uses 32 sinusoidal codes per period from the LUT for power savings. To generate a 128-step-per-period sinusoidal signal set MODEM\_CFG.TxRES = 1.  shows the HART modulator architecture.



**图 6-18. HART Modulator Architecture**

### 6.3.5.3 HART Demodulator

The HART demodulator converts the HART FSK input signals applied at the HART input pins (RX\_IN and RX\_INF) to binary data that are enqueued into the receive FIFO (FIFO\_H2U). Data from the FIFO\_H2U can then be dequeued by the host controller using the SPI or output on UARTOUT. 図 6-19 shows the HART demodulator architecture. The AFE882H1 supports two different input bandpass filter modes: internal and external.

In internal filter mode, the HART input signal is connected to the RX\_IN pin through the high-pass filter capacitor. In this mode, the low-pass filter capacitor is connected to the RX\_INF pin.

In external filter mode, the band-pass filter is implemented with external components for better flexibility, and the resulting band-pass-filtered signal is connected to the RX\_INF pin. In this mode, float the RX\_IN pin.

Use the MODEM\_CFG.RX\_EXFILT\_EN bit to select between these two modes, depending on the external band-pass filter implementation and HART input signal connection.

The input band-pass filter (either fully external or partially internal with external capacitors and internal resistors) is followed by the internal second-order high-pass filter and the internal second-order low-pass filter. To enable the second-order low-pass filter, use the MODEM\_CFG.RX\_HORD\_EN bit.

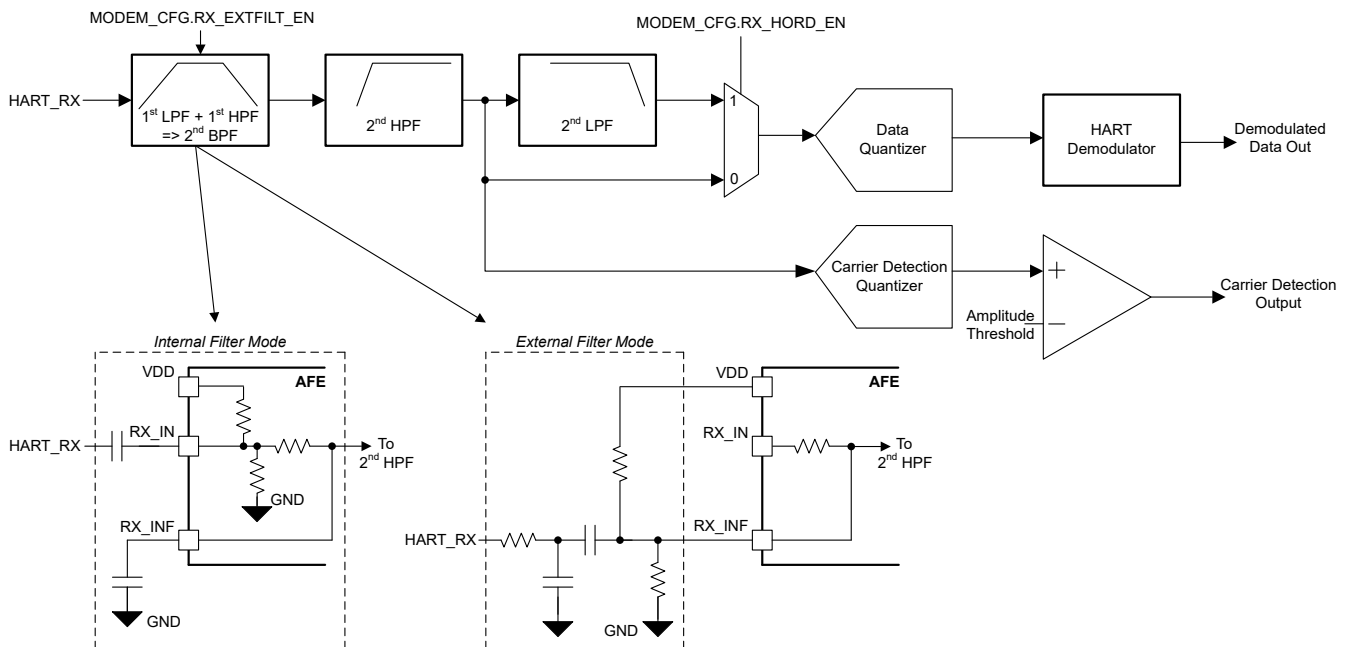


図 6-19. HART Demodulator Architecture

The HART demodulator asserts a carrier detect (CD) signal, when a carrier-above-threshold level is detected. Hysteresis is implemented with the carrier-detect feature to prevent erroneous carrier-detection signals. The glitch-free CD signal is available internally to the arbiter and externally to the system controller on the CD pin.



#### 6.3.5.4 HART Modem Modes

The HART modulator-demodulator operates in either half-duplex or full-duplex mode.

##### 6.3.5.4.1 Half-Duplex Mode

Half-duplex mode is the main functional mode of operation for the AFEx82H1, in conjunction with the half-duplex HART protocol. In half-duplex mode, either the modulator or demodulator is active at any given instant, but never simultaneously enabled. By default, the demodulator is active and the modulator is inactive. When using half-duplex mode, the modem arbitrates when modulator and demodulator are active. For more details, see [セクション 6.3.5.5](#).

##### 6.3.5.4.2 Full-Duplex Mode

In full-duplex mode, the modulator and demodulator are simultaneously enabled. This configuration allows a self-test feature to verify functionality of the transmit and receive signal chains to improve system diagnostics. There are internal and external full-duplex modes.

In internal full-duplex mode, the MOD\_OUT pin is internally shorted to the RX\_INF pin. Set MODEM\_CFG.DUPLEX = 1 to enable an internal connection between the HART transmitter and receiver to verify communication.

In external full-duplex mode, the HART modulator and demodulator are enabled, but the MOD\_OUT pin is not internally shorted to the RX\_IN or RX\_INF pins. To enable the external full-duplex mode, short MOD\_OUT to RX\_IN or RX\_INF pins externally, and set MODEM\_CFG.DUPLEX\_EXT = 1.

#### 6.3.5.5 HART Modulation and Demodulation Arbitration

In half-duplex HART-protocol mode, the device arbitrates when the modulator and demodulator are active, based on activity on the HART bus. The system controller has various means of monitoring and interacting with the AFEx82H1. For the methods used in SPI mode, see [セクション 6.3.5.9](#). For the reporting method used in UART mode, see [セクション 6.3.5.10](#).

In the default idle state, the  $\overline{\text{RTS}}$  pin is high (inactive), and the CD pin is low. The demodulator is active and the modulator is inactive.

##### 6.3.5.5.1 HART Receive Mode

When a carrier is detected, the CD pin toggles high, and data bytes received by the modem are automatically enqueued into FIFO\_H2U. This mode is the highest priority, and the device continues to remain in this mode as long as a valid carrier is present. The system controller must timely dequeue the data from the FIFO\_H2U as long as CD remains high and the demodulator enqueues new data into FIFO\_H2U. CD is deasserted when the level of the incoming carrier is reduced to less than the HART specification. For receive operation timing details, see [セクション 6.3.5.7](#).

##### 6.3.5.5.2 HART Transmit Mode

To transmit the HART data, issue a request to send (RTS) either by toggling the  $\overline{\text{RTS}}$  pin low or asserting MODEM\_CFG.RTS, depending on the selected communication setup. When the HART bus is available for transmission and no carrier is detected, the device deasserts the CD pin, disables the demodulator, asserts the CTS response by setting MODEM\_STATUS.CTS\_ASSERT = 1, and begins modulating the carrier. If the CD pin is used, wait for the CD pin to be deasserted. Otherwise, unmask CTS\_ASSERT and set up the appropriate IRQs for the FIFO\_U2H levels and CTS flags to enable the system controller to receive an IRQ when CTS is asserted. See also [セクション 6.3.5.8](#). When the CD pin and IRQ are not used, poll the MODEM\_STATUS register regularly to detect when the CTS response is asserted.

As long as the CD pin is asserted, the demodulator remains active and the RTS request is held pending by the arbiter. Any HART transmit data bytes received by the AFEx82H1 are enqueued into FIFO\_U2H, but not transmitted immediately. The system controller must monitor the FIFO\_U2H level to avoid buffer overflow in this condition.



When the CTS response is asserted, the data enqueued into FIFO\_U2H are dequeued and transmitted onto the MOD\_OUT pin. If no data are enqueued into FIFO\_U2H, the modulator starts transmitting the *mark* signal. The beginning of the bit stream must meet the minimum bit times requirement to make sure there is enough time for successful detection of the *mark-to-space* transition on the receiving side; see also [セクション 6.3.5.6](#).

The system controller is then required to maintain adequate an FIFO\_U2H buffer level to avoid gap errors and deassert the RTS at the end of bit stream with the correct timing delays; see also [セクション 6.3.5.6](#).

#### 6.3.5.6 HART Modulator Timing and Preamble Requirements

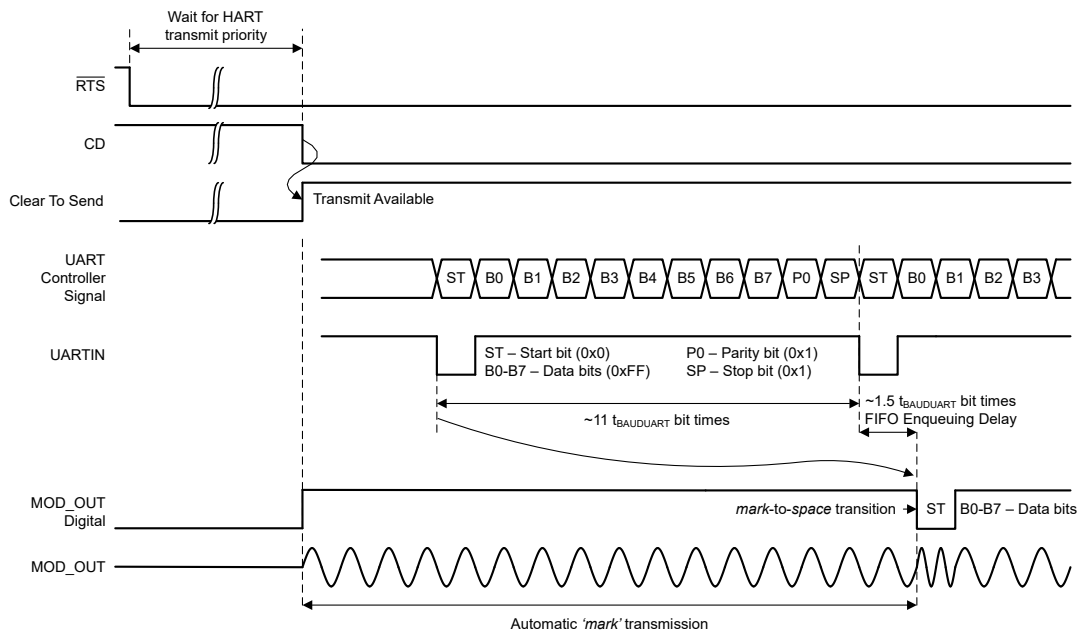
The HART modulator starts modulating the carrier as soon as the CTS response is asserted. If data are enqueued into FIFO\_U2H before the CTS is asserted, make sure to enqueue the required preamble bytes at the beginning of the data packet in accordance with [表 6-6](#). The first byte is used by the HART recipient receiver to recognize the carrier and properly detect the *mark-to-space* transition of the start bit in the second character. Alternatively, wait for CTS\_ASSERT, and give an appropriate delay while the modulator is transmitting the *mark* signal. Then enqueue the preamble bytes followed by the data bytes into FIFO\_U2H. Monitor the level of FIFO\_U2H and timely enqueue the new data to avoid transmission gap errors.

**表 6-6. Carrier Detect and Preamble**

HART REQUIREMENT	FIFO_U2H STATE	AFEx82H1 BEHAVIOR	RECOMMENDED USE CASE
Transmit at least 6 bit times of HART signal of specified amplitude for the carrier to be detected by the receiver.	FIFO_U2H is empty.	HART modulator starts sending <i>mark</i> FSK signal as soon as CTS is asserted.	Wait at least 6 bit times from CTS assert before transmitting first preamble byte. Calculate the time to enqueue the data into FIFO_U2H based on the interface mode used.
	FIFO_U2H is preloaded with data.	HART modulator starts sending FIFO_U2H data as soon as CTS is asserted.	Preload FIFO_U2H with one additional preamble byte.

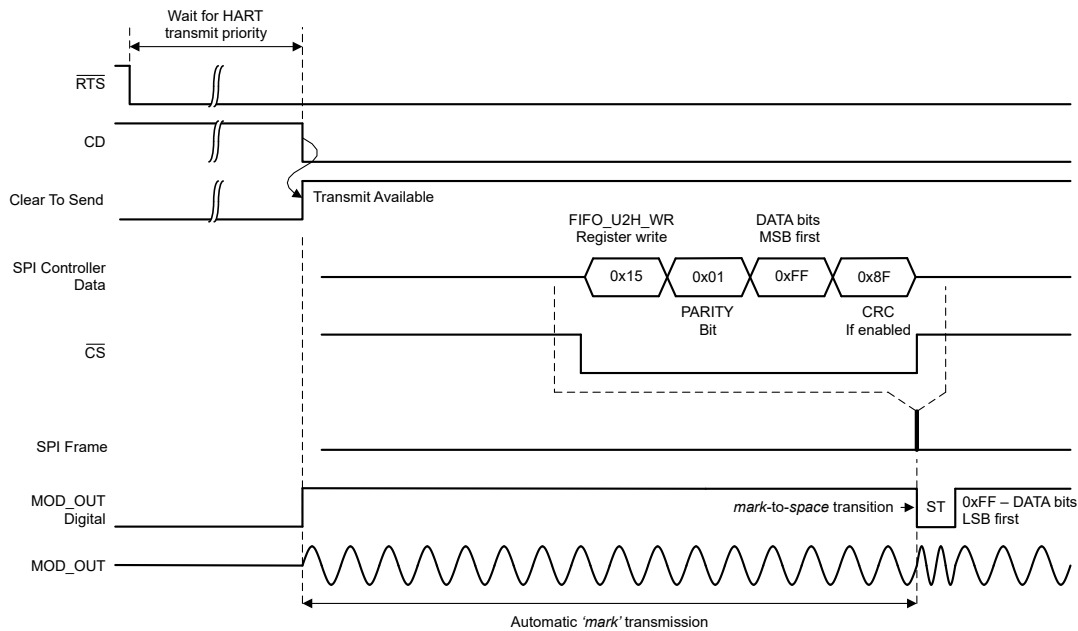
Depending on the interface mode, there is a latency from the UARTIN or  $\overline{CS}$  pin to the MOD\_OUT pin as a result of using FIFO\_U2H in the data path.

In the SPI plus UART and UBM modes, a delay of approximately 1.5 bit times ( $1.5 \times t_{\text{BAUDUART}}$ ) occurs from the stop bit on the UARTIN pin until the data are enqueued into FIFO\_U2H as a result of data decoding and synchronization. [図 6-20](#) shows this timing.



**図 6-20. HART Transmit Start Timing Diagram (UART Mode)**

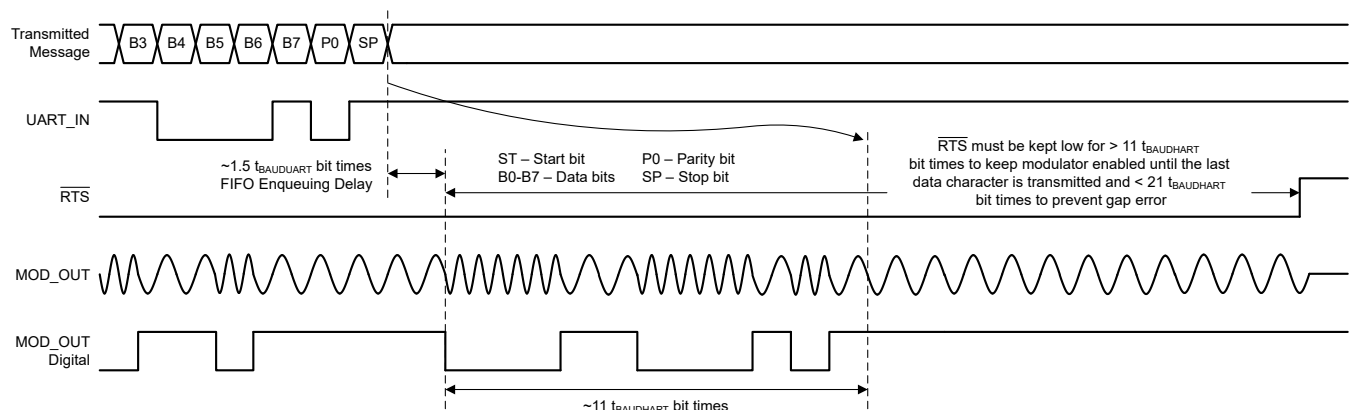
In SPI only mode, the HART transmit data are enqueued into FIFO\_U2H using FIFO\_U2H\_WR register. Therefore, in this mode, take the standard SPI timing into consideration while calculating the latency of the HART transmit data from the  $\overline{CS}$  pin to the MOD\_OUT pin. 6-21 shows the HART transmit start timing for SPI mode.



6-21. HART Transmit Start Timing Diagram (SPI Mode)

The HART character contains 11 bits; therefore, a delay of approximately 11 bit times ( $11 \times t_{\text{BAUDHART}}$ ) occurs from the moment the data are dequeued from FIFO\_U2H until the data are fully transmitted on the MOD\_OUT pin (see 6-22).

Additional delay is accumulated when there is a frequency mismatch between the incoming UART\_IN data and the HART data transmitted on MOD\_OUT. If the UART\_IN data frequency is 2% greater compared to the MOD\_OUT data frequency, a delay of approximately 1 bit time is accumulated every five HART characters. Add a gap of at least 1 bit time between every five HART characters to account for this latency. Keep the request to send (RTS) asserted until the data are fully transmitted on MOD\_OUT.



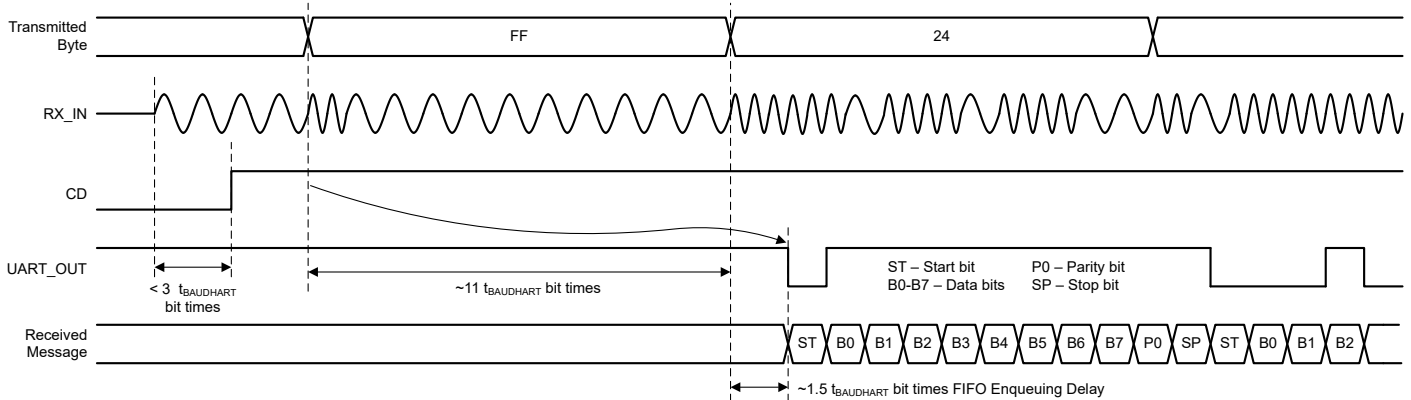
6-22. HART Transmit End Timing Diagram (UBM, UART Plus SPI Modes)

### 6.3.5.7 HART Demodulator Timing and Preamble Requirements

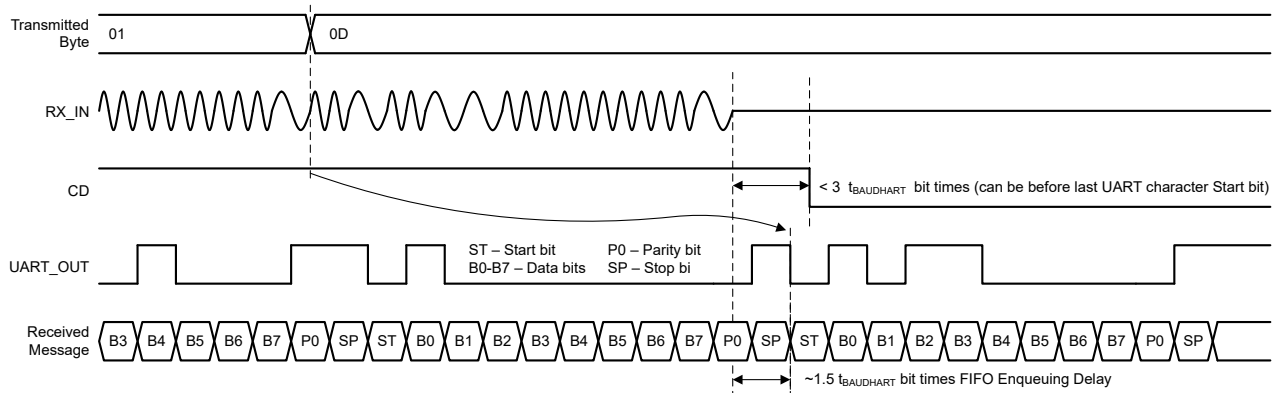
The RX\_IN and RX\_INF pins are continuously monitored by the HART demodulator when not transmitting. AFE882H1 requires at least 3 *mark* bits ( $3 \times t_{\text{BAUDHART}}$ ) of 1200 Hz for carrier detection.

For UART-based communication setup, the HART data are automatically dequeued from FIFO\_H2U and transmitted on the UARTOUT pin as UART characters. A delay of approximately 1.5 bit times ( $1.5 \times t_{\text{BAUDHART}}$ ) occurs as a result of data decoding and synchronization from the end of the character on RX\_IN or RX\_INF pin until the data are enqueued into FIFO\_H2U. Thus, when CD deasserts, there is typically still one UART character pending transfer to the system controller on UARTOUT (see Figure 6-24).

FIFO latency is as low as a few microseconds when using the SPI to dequeue the data from FIFO\_H2U by reading FIFO\_H2U\_RD register. Figure 6-23 and Figure 6-24 show the timing diagrams for the start and end of the HART receive character, respectively.



**Figure 6-23. HART Receive Start Timing Diagram (SPI and UART Modes)**



**Figure 6-24. HART Receive End Timing Diagram (UART Mode)**

### 6.3.5.8 IRQ Configuration for HART Communication

To enable robust and error-free communication on the HART bus, the events listed in 表 6-7 must be detected from the AFE82H1 by the system controller in a timely manner. If the IRQ signal is not directly connected to the system controller, poll the corresponding status flags. In UART mode, the automatic dequeue of FIFO\_H2U simplifies event management significantly, and not all events must be translated to IRQs.

When using the HART modem with the IRQ, the IRQ features help control communication in both directions. Enable IRQ functionality by following these steps:

1. Configure the IRQ to be either edge or level sensitive using CONFIG.IRQ\_LVL. See also セクション 6.3.4.
2. Configure the IRQ polarity with CONFIG.IRQ\_POL, as needed per the respective system. See also セクション 6.3.4.
3. For SPI only mode, set CONFIG.IRQ\_PIN\_EN = 1 to enable IRQ functionality on the UARTOUT pin. Also, set CONFIG.UART\_DIS = 1 to disable all UART functionality.
4. For UBM, use one of the two following methods:
  - a. Set CONFIG.IRQ\_PIN\_EN = 1 to enable IRQ functionality on the SDO pin, or
  - b. Set CONFIG.UBM\_IRQ\_EN = 1 to enable interrupts being sent UARTOUT using UBM.
5. After IRQ functionality is enabled, unmask all the required interrupt signals in the MODEM\_STATUS\_MASK register (set each bit = 0).

表 6-7. IRQ Sources and Uses

AFE82H1 HART STATE	EVENT	MODEM_STATUS FLAG	ASSERTION METHOD <sup>(1)</sup>	ACTION
Receive	RTS deasserted	CTS_DEASSERT	Toggle RTS pin high or set MODEM_CFG.RTS = 0.	Demodulator enabled and ready to receive HART data.
	Carrier detect asserted	CD_ASSERT	Demodulator detects the HART carrier signal of valid amplitude.	Expect to receive HART data. Set desired FIFO_H2U level trigger threshold.
	FIFO_H2U level threshold trigger	FIFO_H2U_LEVEL_FLAG	Automatic enqueue of FIFO_H2U by HART demodulator.	Dequeue data from FIFO_H2U when level exceeds the set threshold. Prevent FIFO_H2U from being full to avoid the loss of incoming data.
	FIFO_H2U full	FIFO_H2U_FULL_FLAG	Automatic enqueue of FIFO_H2U by HART demodulator. System controller has not dequeued FIFO_H2U.	Critical flag. Dequeue FIFO_H2U immediately to avoid the loss of incoming data.
	Carrier detect deasserted	CD_DEASSERT	Demodulator stops detecting the HART carrier signal of valid amplitude.	Dequeue remaining data from FIFO_H2U. Monitor the empty flag to make sure that all data have been received.
	FIFO_H2U empty	FIFO_H2U_EMPTY_FLAG	Dequeue of FIFO_H2U by system controller.	If using UART, wait to make sure the last character is received on UARTOUT.
Transmit	RTS asserted	NA	Toggle RTS pin low or write set MODEM_CFG.RTS = 1.	Wait for clear-to-send confirmation flag.
	Clear to send (CTS)	CTS_ASSERT	RTS asserted and CD deasserted.	Modulator enabled. Device starts modulating the carrier on MOD_OUT. Set desired FIFO_U2H level trigger threshold. Enqueue data into FIFO_U2H. Modulator automatically dequeues FIFO_U2H and transmits the HART data.
	FIFO_U2H level threshold trigger	FIFO_U2H_LEVEL_FLAG	Automatic dequeue of FIFO_U2H by HART modulator.	Enqueue new data into FIFO_U2H when the level drops below the set threshold. Prevent FIFO_U2H from being empty to avoid a gap in transmission.
	FIFO_U2H full	FIFO_U2H_FULL_FLAG	System controller enqueue of the new data into FIFO_U2H.	Critical flag. Stop enqueue of data into FIFO_U2H immediately to avoid loss of HART data.
	FIFO_U2H empty	FIFO_U2H_EMPTY_FLAG	Automatic dequeue of FIFO_U2H by HART modulator. System controller has not enqueued new data into FIFO_U2H.	Critical flag in the middle of the data packet. Enqueue new data into FIFO_U2H immediately to avoid a gap in transmission. When the last character is dequeued from FIFO_U2H, wait until the character is fully transmitted on MOD_OUT before deasserting RTS.

(1) For CD, RTS, ALARM, and IRQ connection choices, see セクション 6.5.1.

### 6.3.5.9 HART Communication Using the SPI

HART bus communication activity is reported to the host controller through the IRQ signal routed to the UARTOUT pin and MODEM\_STATUS register. Read the MODEM\_STATUS register to determine the source of the IRQ when an IRQ is received. If the UARTOUT pin is not connected, poll the status registers regularly through the SPI.

To transmit data, set up the desired FIFO\_U2H level thresholds using FIFO\_CFG.U2H\_LEVEL\_SET. Assert the RTS. After CTS\_ASSERT is set, begin to fill FIFO\_U2H. Enqueue enough data into FIFO\_U2H to fill the FIFO above the set threshold level. The HART modulator automatically dequeues the data from FIFO\_U2H and transmits the data on MOD\_OUT. When FIFO\_U2H level drops below the set threshold, an IRQ triggers, indicating that new data bytes can be enqueued without losing any data. After the last set of data have been enqueued into FIFO\_U2H, an IRQ event triggered by the level flag can be ignored. Wait for the IRQ event triggered by FIFO\_U2H\_EMPTY\_FLAG. Deassert the RTS after required delay; see also [セクション 6.3.5.6](#). When the RTS is deasserted, the CTS\_DEASSERT bit is set. CTS\_DEASSERT is an informational bit.

To receive data, set up an IRQ event based on CD\_ASSERT to know when the carrier is detected and the new data bytes are expected. Also, set up the additional IRQ events to trigger each time FIFO\_H2U\_LEVEL\_FLAG is set. Select the desired level of FIFO\_H2U. Dequeue the data from FIFO\_H2U every time the level exceeds the set threshold. Also, set up IRQ event trigger based on CD\_DEASSERT to know when all the data have been received. At this point, monitor FIFO\_H2U.EMPTY\_FLAG when dequeuing each character to know when FIFO\_H2U is empty and all the data bytes have been dequeued and transmitted to the microcontroller.

Alternatively, the CD pin can be directly connected to the microcontroller to monitor the status of the HART bus. In this configuration, mask CD\_ASSERT flag by setting MODEM\_STATUS\_MASK.CD\_ASSERT bit = 1 to prevent CD\_ASSERT from generating an IRQ event.

### 6.3.5.10 HART Communication Using UART

In SPI plus UART mode, the UART data are transmitted and received at 1200 baud, which is matched to the HART FSK input and output signals. Both SDO and UARTOUT pins are used; therefore, the IRQ functionality is not available in SPI plus UART mode. FIFO\_H2U level monitoring is not required because any HART data received by the demodulator and enqueued into FIFO\_H2U are automatically dequeued and transmitted on UARTOUT. FIFO\_U2H level monitoring is also not required if HART bus communication activity is interfaced to the host controller through the CD and  $\overline{\text{RTS}}$  pins. The host controller can properly time the  $\overline{\text{RTS}}$  pin to transmit the HART data when no carrier is detected on the bus. If the CD and  $\overline{\text{RTS}}$  pins are not used in SPI plus UART mode, the host controller can periodically poll the MODEM\_STATUS register through the SPI to detect when the carrier is not present on the HART bus, and assert the request to send by setting MODEM\_CFG.RTS bit = 1.

In UBM, the UART data are transmitted and received at 9600 baud. The HART data characters are interleaved with break commands for register map access or interrupt reporting; see also [セクション 6.5.4.1.1](#). Similar to SPI plus UART mode, monitoring of FIFO\_H2U and FIFO\_U2H levels is not required. The CD and  $\overline{\text{RTS}}$  pins are available to interface the HART bus activity with the microcontroller. IRQ functionality is also available on the SDO pin. If the SDO pin is connected to the microcontroller, the IRQ event based on CD\_ASSERT can be set to report when the carrier is detected. In this case, CD pin connection to the microcontroller is not required. Similarly,  $\overline{\text{RTS}}$  pin connection is not required if MODEM\_CFG.RTS is used to issue a request to send. The SDO pin connection to the microcontroller is also not required if the microcontroller can periodically poll the MODEM\_STATUS register using break commands, and monitor all the required flags.

#### 6.3.5.11 Memory Built-In Self-Test (MBIST)

Memory built-in self-test (MBIST) verifies the validity of the static random-access memory (SRAM) used for the FIFO buffers. When initiated, the MBIST takes control of the SRAM module until completion.

Disable HART communication while the MBIST is running. Communication with the FIFO buffers during the MBIST produces unreliable results. Two status bits, GEN\_STATUS.MBIST\_DONE and GEN\_STATUS.MBIST\_FAIL, can be monitored for completion or failure, or used to create IRQ events.

Do not try to read back the GEN\_STATUS register while the MBIST is running. The MBIST control logic generates narrow pulses for the MBIST\_DONE and MBIST\_FAIL status flags. The status flags can be missed if these pulses occur during the readback of the GEN\_STATUS register. To avoid missing the MBIST\_DONE flag, mask all the status bits except GEN\_STATUS\_MASK.MBIST\_DONE and then either:

1. monitor for an IRQ event, or
2. periodically send a NOP and check the GEN\_IRQ status bit.

Wait until MBIST\_DONE is reported, verify the status of the MBIST\_FAIL flag, and then resume normal operation.

#### 6.3.6 Internal Reference

The AFE82H1 family of devices includes a 1.25-V precision band-gap reference. The internal reference is externally available at the VREFIO pin and sources up to 2.5 mA. For noise filtering, use a 100-nF capacitor between the reference output and GND.

The internal reference circuit is enabled or disabled by using the REF\_EN pin. A logic high on this pin enables the internal reference, and the VREFIO pin outputs 1.25 V. A logic low on this pin disables the internal reference, and the device expects to have 1.25 V from external VREF at the VREFIO pin.

An invalid reference voltage asserts an alarm condition. The DAC response depends on the VREF\_FLT setting in the ALARM\_ACT register (10h).

#### 6.3.7 Integrated Precision Oscillator

The internal time base of the device is provided by an internal oscillator that is trimmed to less than 0.5% tolerance at room temperature. The precision oscillator is the timing source for ADC conversions. At power up, the internal oscillator and ADC take roughly 300  $\mu$ s to reach < 1% error stability. After the clock stabilizes, the ADC data output is accurate to the electrical specifications provided in [セクション 5](#).

#### 6.3.8 Precision Oscillator Diagnostics

The AFE82H1 features two methods to continuously detect the functional status of the internal precision oscillator.

The first method requires a connection from the AFE82H1 to the system controller. To use the first method, program the AFE82H1 to output a subdivided internal oscillator clock signal on the CLK\_OUT pin. Write to the CONFIG.CLKO register field (see [表 7-5](#)) to enable the output with the chosen divider or to disable the output. The output digital signal is compliant to the [セクション 5.5](#). The CLK\_OUT pin is also a shared GPIO pin. For details on connecting CLK\_OUT and CLK\_OUT interoperability as a GPIO pin, see [セクション 6.5.1](#).

The second method does not require a connection from the AFE82H1 and is a polled-communication-based method to determine the functionality of the internal oscillator using SPI communication. See [セクション 6.5.3.1](#) and [セクション 6.5.5](#) for SPI communication details and SDO status bits details, respectively. The OSC\_DIV\_2 bit reports the logical value of a subdivided internal oscillator signal (divided by 2) sampled at the  $\overline{CS}$  falling edge. Use an appropriate SCLK frequency and interval between SPI frames to capture bit changes from frame to frame as a method of verifying the continued proper operation of the clock. Similar status reports of the logical value of a subdivided internal oscillator signal (divided by 1024) are available in UBM as the OSC\_DIV\_1024 bit. For details on UBM frames and timing, see [セクション 6.5.4.1](#).



### 6.3.9 One-Time Programmable (OTP) Memory

One-time programmable (OTP) memory in the device is used to store the device trim settings and is not accessible to users. The OTP memory data are loaded to the memory (OTP shadow load) at power up. The OTP memory CRC is performed to verify the correct data are loaded. The TRIGGER.SHADOWLOAD bit is available to initiate a reload of the OTP memory data if a CRC error is detected. The SPECIAL\_CFG.OTP\_LOAD\_SW\_RST bit controls whether the OTP memory data are reloaded with a software reset.

### 6.3.10 GPIO

AFE82H1 feature multiple GPIO pins, each independently configurable in either input only or output only or input-output mode through GPIO\_CFG and GPIO registers. Select either push-pull or pseudo open drain sub modes supported when the GPIO is in output mode. No dedicated GPIO pins are present since the same pins are also configurable for communication interfaces. Based on the selection of the interface protocol and how many pins are used for communication purposes, the AFE82H1 have up to four available GPIOs. Refer to [セクション 6.5.1](#) for detailed diagrams of available GPIOs in each communication mode. If a GPIO pin is unused or undriven, the pin must be tied resistively to either IOVDD or GND according to the connection diagrams in [セクション 6.5.1](#). Unconnected floating input pins lead to unknown states for the communication interfaces and varying supply currents for the AFE82H1. When functioning as an output, each GPIO pin is capable of sourcing and sinking current and when functioning as an input the register address 0x1C reflects the digital state of the GPIO pins (for details of source and sink capabilities and input thresholds, see [セクション 5.5](#)). The minimum pulse width for transition detection is  $t_{PULSE\_GPIO}$ . When a state transition occurs on a GPIO input, the new state must be held for a minimum of  $t_{PULSE\_GPIO}$  for detection by the AFE82H1.

### 6.3.11 Timer

The AFE82H1 have an integrated timer for generating accurate time delays, pulse width modulation or oscillation. The devices have the ability to have timing parameters from the microseconds range to hours. The timer is brought out on the CLK\_OUT pin by setting CONFIG.CLKO = Fh. The timer is controlled with three registers; TIMER\_CFG\_0, TIMER\_CFG\_1, and TIMER\_CFG\_2.

In the first of the three registers, TIMER\_CFG\_0.ENABLE turns the timer function on and off. If the timer is off, then the output defaults to 0. TIMER\_CFG\_0.INVERT inverts the output of the timer. If the INVERT bit is set, the output defaults to 1. TIMER\_CFG\_0.CLK\_SEL selects the clock frequency according to [表 6-8](#). If 2'b00 is selected, and no clock is applied, then the timer pauses if the timer has previously been enabled and counting.

**表 6-8. Timer Select Range**

CLK_SEL	Clock Frequency	Resolution	Range
00	No clock	-	-
01	1.2288 MHz	814 ns	53.3 ms
10	1.200 kHz	833 $\mu$ s	54.6 s
11	1.171 Hz	853 ms	55,923 s

The second timer register, TIMER\_CFG\_1.PERIOD sets the period of the timer. The period of the timer is PERIOD + 1 cycles of the clock period.

The last timer register, TIMER\_CFG\_2.SET\_TIME determines when the timer output goes to 1 (INVERT = 0). This effectively defines the duty cycle of the timer. The duty cycle can be calculated as (PERIOD – SET\_TIME)  $\times$  clock period.

### 6.3.12 Unique Chip Identifier (ID)

AFE82H1 include two read only registers: CHIP\_ID\_MSB (1Ah) and CHIP\_ID\_LSB (19h) where unique chip ID is stored. The 16-bit CHIP\_ID\_MSB register stores the encoded lot identification number while the CHIP\_ID\_LSB register stores the unique part number within each lot.

### 6.3.13 Scratch Pad Register

AFE82H1 feature a 16-bit Scratch Pad register to enable interface debug and verification without affecting the part functionality. This register is located at the address 18h. The readback value of the Scratch Pad register is the inverted code of the value stored in the register (for example, writing 0xAAAA results in 0x5555 while reading back ).

## 6.4 Device Functional Modes

### 6.4.1 DAC Power-Down Mode

Power-down mode facilitates rapid turn-off of the voltage at the DAC output. The DAC can be set to enter and exit power-down mode through hardware, software, or automatically in response to an alarm event. The DAC output is specified for glitch-free performance when going into and out of power-down mode.

Power-down mode is also be enabled by setting DAC\_CFG.PD to 1. In power-down mode, the DAC output amplifier powers down and the DAC output pin is put into the Hi-Z configuration. The DAC output remains in power-down mode until the DAC output is re-enabled.

Alarm control of the power-down mode is enabled by setting the alarm events as DAC power-down sources. The alarm events that trigger the DAC output power-down state must be specified in the ALARM\_ACT register. After the alarm bit is cleared, the DAC returns to normal operation, as long as no other power-down controlling alarm event has been triggered.

The DAC register does not change when the DAC enters power-down mode, which enables the device to return to the original operating point after return from the power-down mode. Additionally, the DAC register can be updated while the DAC is in power-down mode, thus allowing the DAC to output a new value upon return to normal operation.

### 6.4.2 Register Built-In Self-Test (RBIST)

The AFE82H1 feature a register built-in self-test (RBIST) that runs on all the registers listed in 表 6-9 through a CRC calculation in the order the registers are listed in 表 6-9. If a register is reserved, the reset value is used in the calculation of the RBIST. If the final CRC value is zero, then no error is present in the configuration of the registers. If a non-zero value is present at the end of the calculation, then there is a configuration error. The polynomial used has a Hamming distance (HD) of 4 for data packets up to 2048 bits. With HD = 4, the CRC detects any combination of 4-bit errors within the stored data. Independently calculate the expected CRC polynomial and store the output in the RBIST\_CRC register at 3Fh.

The final value of the CRC is read in the CRC\_RD register at address 3Eh. This value is updated while either an RBIST or shadow load is running. Both the RBIST and OTP memory use the same CRC calculation engine and polynomial. The value in the CRC\_RD register remains constant until another RBIST or SHADOWLOAD in TRIGGER register (0Ah) is triggered.

Set TRIGGER.RBIST to 1 to initiate an RBIST. The TRIGGER.RBIST bit stays high as long as the RBIST is running and clears when the self-test is complete. While the RBIST is running, the registers cannot be written to or read. Send NOP commands and monitor the RBIST SDO status bit to determine if the RBIST has completed.

In UBM, the RBIST does not interfere with register communication. UBM communication is slow enough that the RBIST completes before any following read or write command.

The GEN\_STATUS.BIST\_DONE and GEN\_STATUS.BIST\_FAIL bits have the same functionality for both MBIST and RBIST. GEN\_STATUS.BIST\_MODE is used to select between two tests (1 = RBIST and 0 = MBIST). This bit is sticky until the GEN\_STATUS register is read.

The FIFO\_CFG.FIFO\_H2U\_FLUSH and FIFO\_CFG.FIFO\_U2H\_FLUSH bits are write-self-clear (WSC) and considered 0 by the CRC module.

The 16-bit CRC used to generate the RBIST is compliant to the openSAFETY (0x755B) standard with the following polynomial:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^8 + x^6 + x^4 + x^3 + x^1 + 1.$$



The list of registers covered by the RBIST is listed in 表 6-9. Not all registers feature the RBIST.

**表 6-9. List of Registers Covered by RBIST**

ADDR (HEX)	REGISTER	RESET (HEX)
01h	DAC_DATA	0000h
02h	CONFIG	0036h
03h	DAC_CFG	0B00h
04h	DAC_GAIN	8000h
05h	DAC_OFFSET	0000h
06h	DAC_CLR_CODE	0000h
08h	ADC_CFG	8810h
09h	ADC_INDEX_CFG	0080h
0Bh	SPECIAL_CFG	0000h
0Dh	RESERVED	0100h
0Eh	MODEM_CFG	0040h
0Fh	FIFO_CFG	00F0h
10h	ALARM_ACT	8020h
11h	WDT	0018h
12h	AIN0_THRESHOLD	FF00h
13h	AIN1_THRESHOLD	FF00h
14h	TEMP_THRESHOLD	FF00h
1Bh	GPIO_CFG	00FFh
1Dh	ALARM_STATUS_MASK	EFDh
1Eh	GEN_STATUS_MASK	FFFFh
1Fh	MODEM_STATUS_MASK	FFFFh
3Fh	RBIST_CRC	0000h

### 6.4.3 Reset

There are three reset mechanisms in the device: a power-on reset (POR), a  $\overline{\text{RESET}}$  pin, and the SW\_RST command that can be sent through the either the SPI or by UBM.

When power is first applied to the device, a POR circuit holds the device in reset until all supplies reach the specified operating voltages. The power-on reset returns the device to a known operating state in case a brownout event occurs (when the supplies have dipped below the minimum operating voltages). The POR starts all digital circuits in reset as the supply settles, and releases them to make sure that the device starts in the default condition and loads the OTP memory. After the OTP memory has been loaded, the ALARM pin is released. At this time, communication with the device is safe. This  $t_{\text{POR}}$  time is less than 100  $\mu\text{s}$ .

The devices also have a  $\overline{\text{RESET}}$  pin that is used as a hardware reset to the device. Send the  $\overline{\text{RESET}}$  pin low for a minimum of 100 ns ( $t_{\text{RESET}}$ ) to reset the device. A delay time of 10  $\mu\text{s}$  ( $t_{\text{RESETWAIT}}$ ) is required before sending the first serial interface command as the device latches and releases the reset. The release of the internal reset state is synchronized to the internal clock. The  $\overline{\text{RESET}}$  pin resets the SPI and the UART interfaces, the HART FIFO buffer, the watchdog timer, the internal oscillator, and the device registers.  $\overline{\text{RESET}}$  does not reload the OTP memory.

The command to RESET.SW\_RST = 0xAD resets the device as a software reset. The command is decoded at the rising edge of  $\overline{\text{CS}}$  with an SPI command or during the stop bit of the last character of a UBM frame. Set UBM.REG\_MODE again to put the device back into UBM when resetting the device in UBM. After sending the RESET command, no delay time is required before sending the first serial interface command as the device latches and releases the reset. The reset is synchronized to the falling edge of the internal clock and is released

well before the next rising edge. The  $\overline{\text{ALARM}}$  pin pulses low for the width of the internal reset. This pulse duration is less than 20 ns. This command resets the SPI and the UART interface, the HART FIFO, and the watchdog timer, but does not reset the internal oscillator. The software reset also reloads internal factory trim registers if properly configured in the SPECIAL\_CFG register. The SPECIAL\_CFG register is only reset with a POR.

The POR and hardware reset place the internal oscillator into a reset condition, which holds the clock low. When these two signals are released, there is a delay of a few microseconds before the first rising edge of the clock. The hardware reset,  $\overline{\text{RESET}}$ , pulse width must be at least 100 ns to allow the oscillator to properly reset. The SW\_RST command is a short pulse. This pulse is not long enough to adequately reset the oscillator. The SW\_RST is asserted with a falling edge of the clock. As a result of the long oscillator period, the design architecture provides that all devices are out of reset by the next rising edge.

Figure 6-25 shows the reset tree.

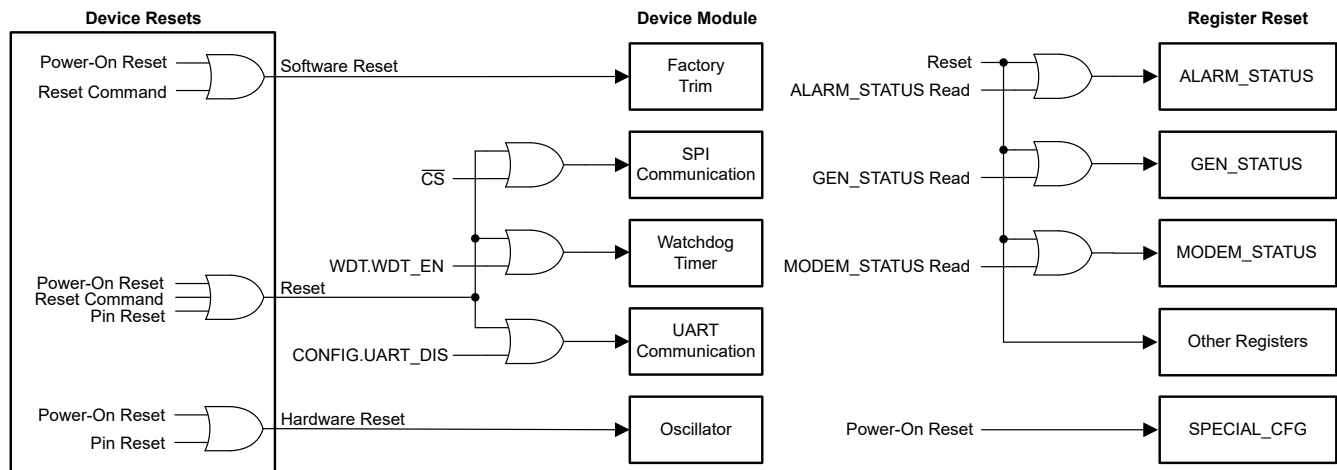


Figure 6-25. Reset Conditions

## 6.5 Programming

The AFE82H1 communicate with the system controller through a serial interface that supports either a UART-compatible two-wire bus or an SPI-compatible bus. Based on the hardware configuration, either interface can be enabled. 図 6-26 and 図 6-27 show the configurations to enable SPI mode and UART break mode (UBM), respectively. The SPI supports an 8-bit frame-by-frame CRC that is enabled by default, but can be disabled by the user. UBM does not support CRC, but does support the UART protocol parity bit.

The AFE82H1 are designed to leverage the existing firmware for communication with DACs or HART modems. A special SPI- and UART-capable dual mode of communication that is available to enable firmware reuse from discrete HART architecture is shown in 図 6-28. See セクション 6.5.1.3 for more details.

### 6.5.1 Communication Setup

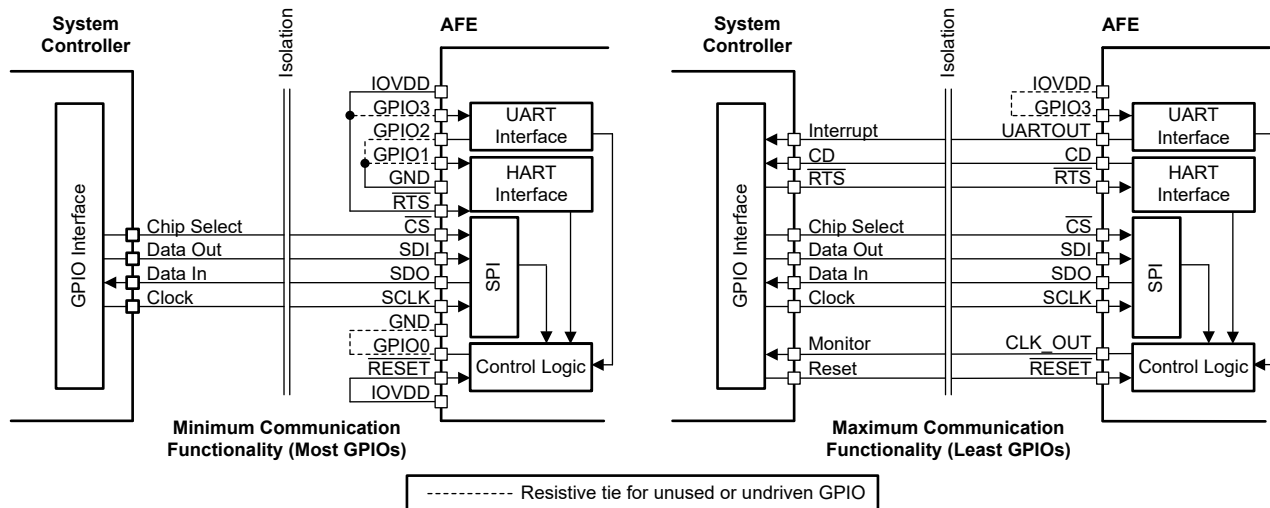
After any reset or power up, the AFE82H1 wake up able to use the SPI or UART break mode (UBM). The devices include a robust mechanism that configures the interface between either an SPI-compatible or UART-compatible protocol based system, thus preventing protocol change during normal operation. The selection is based on initial conditions from the respective hardware configurations (see 図 6-26 and 図 6-27) and any subsequent user configuration.

In SPI plus UART mode, all communication pins on the system microcontroller are connected to the AFE82H1, as shown in 図 6-28.

#### 6.5.1.1 SPI Mode

By default, the AFE82H1 can be fully accessed with the SPI (except UBM.REG\_MODE). To set up the device in SPI mode:

1. Set CONFIG.UART\_DIS = 1 (disables the UART communication).
2. Optionally, set CONFIG.DSDO, CONFIG.FSDO, and CONFIG.IRQ\_PIN\_EN. For details, see 表 7-5.



**図 6-26. SPI Mode Connections**

図 6-26 shows the SPI mode logical connections (through the isolation barrier, if used) for both minimum communication functionality (all optional communication pins disconnected, most GPIO pins available shown) and maximum communication functionality (all communication pins connected, least GPIO pins available shown). If CONFIG.IRQ\_PIN\_EN = 1 is set, then the UARTOUT pin functions as the IRQ output. In SPI mode, set CONFIG.SDO\_DSDO = 0 to enable the readback function. This function is disabled by default to save power. If the readback function not enabled, SDO remains in Hi-Z mode even during the subsequent frame after a read request. Enable each GPIO pin for use through proper register configuration. If a pin remains unused, tied the pin to either IOVDD using a pullup resistor or to GND using a pulldown resistor as indicated to avoid floating IOs.

### 6.5.1.2 UART Mode

At power up, the UART interface is set to 9600 baud with UBM enabled. Any reset clears the UBM register, and the register must be set again to use UBM. To set up the device in UBM:

1. Using UBM, set UBM.REG\_MODE = 1 at 9600 baud. This setting blocks the SPI from accessing the device and enables the UART interface access to the entire register map.
2. Optionally, set CONFIG.CLR\_PIN\_EN and CONFIG.IRQ\_PIN\_EN (See 表 7-5 for details).

図 6-27 shows the UBM logical connections (through the isolation barrier, if used) for both minimum communication functionality (all optional communication pins disconnected, most GPIO pins available shown) and maximum communication functionality (all communication pins connected, least GPIO pins available shown). If CONFIG.IRQ\_PIN\_EN = 1 is set, then the SDO pin functions as the IRQ output. If CONFIG.CLR\_PIN\_EN = 1 is set, then the SDI pin controls the clear pin function. Enable each GPIO pin for use through proper register configuration. If a GPIO pin remains unused, tie the pin to either IOVDD using a pullup resistor or to GND using a pulldown resistor to avoid floating I/Os.

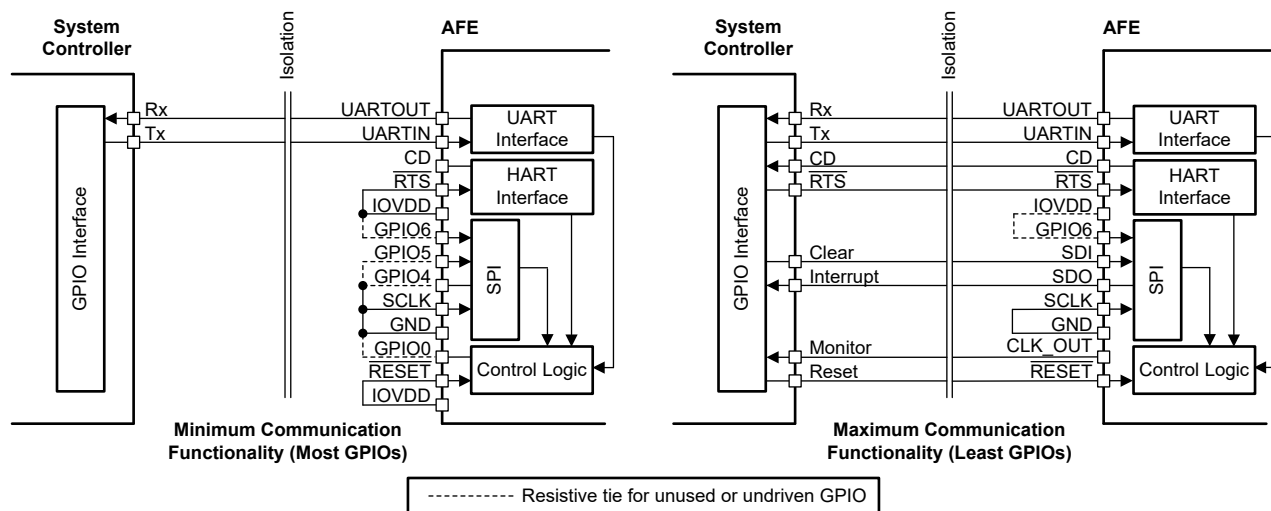


図 6-27. UBM (UART Interface) Connections

### 6.5.1.3 SPI Plus UART Mode

In this mode, communicate with the integrated HART modem using the UART while communicating with the DAC using the SPI. Many discrete DACs use SPI communication, whereas HART modems use UART communication, but this special communication interface enables easy transition from discrete to integrated HART architecture. 図 6-28 shows the UBM logical connections (through the isolation barrier, if used) for both minimum communication functionality (all optional communication pins disconnected, most GPIO pins available shown) and maximum communication functionality (all communication pins connected, least GPIO pins available shown). Enable each GPIO pin for use through proper register configuration. If a pin remains unused, tie the pin to either IOVDD using a pullup or to GND using a pulldown as indicated to avoid floating I/Os.

To setup the device in SPI plus UART mode using the SPI, set CONFIG.UART\_BAUD = 0 to set the baud rate to 1200 for the UART, and to track the HART baud rate of 1200. The UART also works at a 9600 baud, but the 1200 baud rate of HART must be considered, and the FIFO STATUS must be monitored through the SPI.

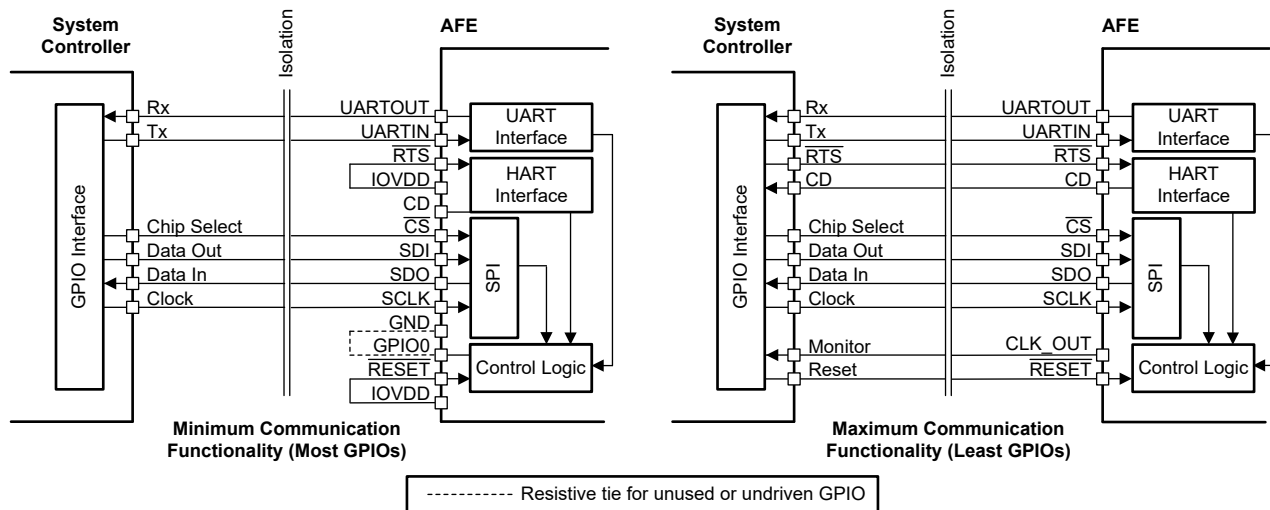


図 6-28. SPI Plus UART Mode Connections

#### 6.5.1.4 HART Functionality Setup Options

表 6-10 shows the various options to set up HART functionality based on communication options by connected pin.

**表 6-10. HART Function Setup Options by Communication Pins Used**

FUNCTION	INTERFACE MODE <sup>1</sup>	PIN NAME	HARDWARE METHOD (PIN CONNECTED)	ALTERNATE METHOD (PIN NOT CONNECTED)
Request to send (RTS)	Any	$\overline{\text{RTS}}$ (input)	L: RTS asserted. H: RTS deasserted.	Write to MODEM_CFG.RTS bit 1: RTS asserted. 0: RTS deasserted.
Carrier detect (CD)	Any	CD (output)	L: CD deasserted. H: CD asserted.	Connect and setup interrupt request or Poll CD_ASSERT / CD_DEASSERT
Clear to send (CTS)	Any	None	Not available	Connect and setup interrupt request or Poll CTS_ASSERT
Alarm	Any	$\overline{\text{ALARM}}$ (output)	Multiple alarm based interrupt sources for system controller; see also <a href="#">セクション 6.3.3</a> .	Connect and setup interrupt request or Poll ALARM_STATUS register
Interrupt request (IRQ) <sup>2</sup>	UART	SDO (output)	Level- and polarity-configurable interrupt pin (see <a href="#">セクション 6.3.4</a> ). Multiple interrupt sources for system controller; see also <a href="#">セクション 6.3.5.8</a> .	Set CONFIG.UBM_IRQ_EN = 1 to generate soft IRQ as break command followed by data on UARTOUT. See <a href="#">セクション 6.5.4.1</a> for details.
	SPI only	UARTOUT (Output)		Poll status registers
	SPI plus UART	None	Not available	Poll status registers

1. For option details, see [セクション 6.5.1](#).
2. For IRQ configuration details, see [表 6-7](#).

## 6.5.2 GPIO Programming

Seven physical pins are interoperable as GPIOs in the AFE82H1 when not used for communication. The state of these pins is set after the communication interface mode is determined (see [セクション 6.5.1](#) for power-up conditions and connection-diagram options for each communication mode supported by the AFE82H1). Configure any unused communication pins as GPIO, and resistively tie the pins to IOVDD or GND, respectively, as described in [セクション 6.5.1](#).

[表 6-11](#) shows the pins and pin functions in UBM, SPI Mode, or SPI plus UART mode and lists the register configuration conditions to enable GPIO functionality for each pin. In addition to these register configurations, to use an available pin as GPIO, set the corresponding GPIO\_CFG.EN bit.

For a GPIO pin to be configured as an input, the following conditions must be met:

1. GPIO\_CFG.ODE for the pin must = 1
2. GPIO.DATA for the pin must = 1

After initialization, the pin state is Hi-Z. Reading the GPIO.DATA register reads the pin value.

If the previous conditions are not met, the pin is an output. In this case, the output drive type is determined by the GPIO\_CFG.ODE bits to be push-pull or pseudo open drain. The GPIO output is driven by the GPIO.DATA bits. All reads of GPIO.DATA reports the values of the pins, regardless if the pins are configured as GPIO or not. Data written to the GPIO.DATA bits cannot be read directly. If a pin is available for use as GPIO, then the corresponding GPIO\_CFG.EN bit must be set to enable GPIO functionality.

**表 6-11. Pin Configuration in Each Interface Mode**

PIN	UBM		SPI		SPI PLUS UART		REGISTER CONFIGURATION TO ENABLE GPIO <sup>(1)</sup>
	FUNCTION	DIRECTION	FUNCTION	DIRECTION	FUNCTION	DIRECTION	
GPIO6/ $\overline{\text{CS}}$	GPIO	Input/Output	$\overline{\text{CS}}$	Input	$\overline{\text{CS}}$	Input	(UBM.REG_MODE = 1)
GPIO5/SDI	CLR/GPIO	Input/Output	SDI	Input	SDI	Input	(UBM.REG_MODE = 1) AND (CONFIG.CLR_PIN_EN = 0)
GPIO4/SDO	IRQ/GPIO	Input/Output	SDO	Output	SDO	Output	(UBM.REG_MODE = 1) AND (CONFIG.IRQ_PIN_EN = 0)
GPIO3/ UARTIN	UARTIN	Input	GPIO	Input/Output	UARTIN	Input	(CONFIG.UART_DIS = 1)
GPIO2/ UARTOUT	UARTOUT	Output	IRQ/GPIO	Input/Output	UARTOUT	Output	(CONFIG.UART_DIS = 1) AND (CONFIG.IRQ_PIN_EN = 0)
GPIO1/CD	CD	Output	CD/GPIO	Input/Output	CD	Output	(CONFIG.UART_DIS = 1)
GPIO0/ CLK_OUT	CLKO/GPIO	Input/Output	CLKO/GPIO	Input/Output	CLKO/GPIO	Input/Output	(CONFIG.CLKO = 0) AND ((UBM.REGMODE = 1) OR (CONFIG.UART_DIS = 1))

(1) Required by pin in addition to the corresponding GPIO\_CFG.EN bit.

### 6.5.3 Serial Peripheral Interface (SPI)

The AFEx82H1 are controlled over a versatile four-wire serial interface (SDIN, SDO, SCLK, and  $\overline{\text{CS}}$ ). The interface operates at clock rates of up to 12.5 MHz and is compatible with SPI, QSPI, Microwire, and digital signal processing (DSP) standards. The SPI communication command consists of a read or write address, a data word, and an optional CRC byte.

The SPI can access all register addresses except for the UBM register. Read-only and read-write capability is defined by register (see 表 7-1). The SPI supports both SPI Mode 1 (CPOL = 0, CPHA = 1) and SPI Mode 2 (CPOL = 1, CPHA = 0). The default SCLK value is low for SPI Mode 1 and high for SPI Mode 2. See セクション 5.7 for timing diagrams in each mode. The serial clock, SCLK, can be continuous or gated.

#### 6.5.3.1 SPI Frame Definition

Subject to the timing requirements listed in the [Timing Requirements](#), the first SCLK falling edge immediately following the falling edge of  $\overline{\text{CS}}$  captures the first frame bit. Subject to the same requirements, the last SCLK falling edge before the rising edge of  $\overline{\text{CS}}$  captures the last bit of the frame. 図 6-29 shows that the SPI shift register frame is 32-bits wide, and consists of an R/W bit, followed by a 7-bit address, and a 16-bit data word. The 8-bit CRC is optional (enabled by default) and is disabled by setting CONFIG.CRC\_EN = 0 (see also セクション 6.5.3.3). 図 6-30 shows that when the CRC is disabled, the frame is 24-bits wide.

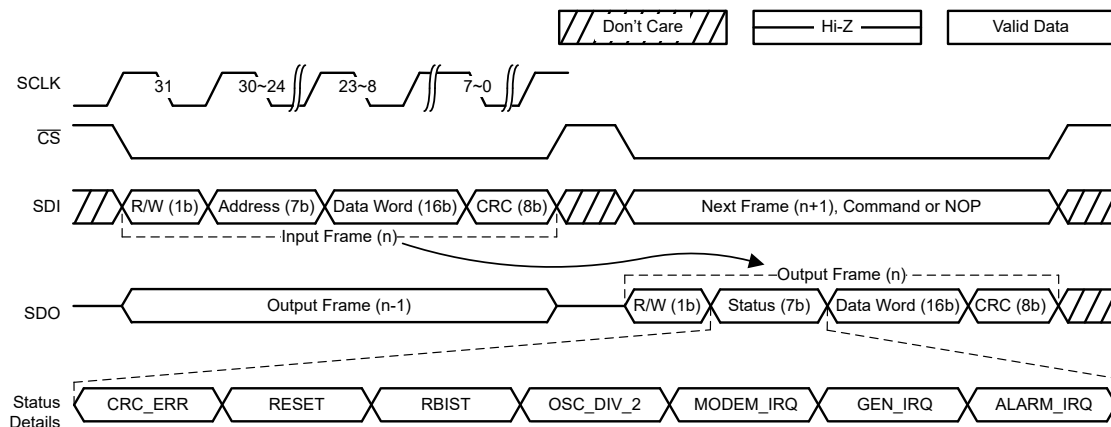


図 6-29. SPI Frame Details (Default, CRC Enabled)

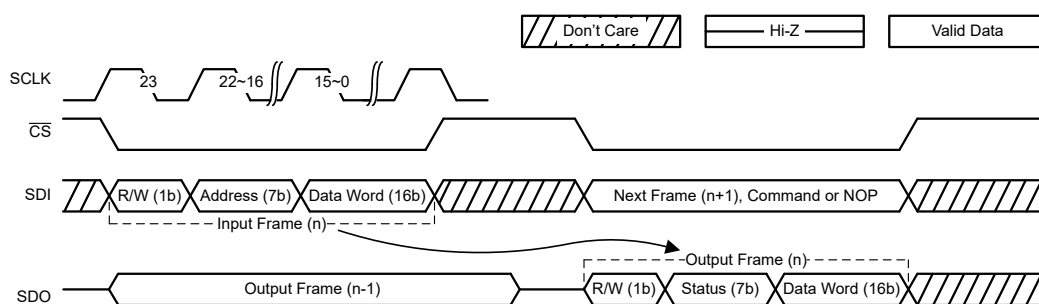


図 6-30. SPI Frame Details (CRC Disabled)

For a valid frame, a full frame length of data (24 bits if CRC is disabled or 32 bits if CRC is enabled) must be transmitted before  $\overline{\text{CS}}$  is brought high. If  $\overline{\text{CS}}$  is brought high before the last falling SCLK edge of a full frame, then the data word is not transferred into the internal registers. If more than a full frame length of falling SCLK edges are applied before  $\overline{\text{CS}}$  is brought high, then the last full frame length number of bits are used. In other words, if the number of falling SCLK edges while  $\overline{\text{CS}} = 0$  is 34, then the last 32 SCLK cycles (or 24 if CRC is disabled) are treated as the valid frame. The device internal registers are updated from the SPI shift register on the rising edge of  $\overline{\text{CS}}$ . To start another serial transfer, bring  $\overline{\text{CS}}$  low again. When  $\overline{\text{CS}}$  is high, the SCLK and SDI signals are blocked and the SDO pin is high impedance.



### 6.5.3.2 SPI Read and Write

The SDI input bit is latched on the SCLK falling edge. The SDI pin receives right-justified data. At the rising edge of  $\overline{CS}$ , the right-most (last) bits are evaluated as a frame. Extra clock cycles (exceeding frame length) during the frame begin to output on SDO the SDI data delayed by one frame length.

A read operation is started when R/W bit is 1. The data word input for SDI is ignored in the read command frame. Send the subsequent read or write command frame into SDI to clock out the data of the addressed register on SDO. If no other read or write commands are needed, then issue a NOP command to retrieve the requested data. The read register value is output most significant bit first on SDO on successive edges (rising or falling based on CONFIG.FSDO setting) of SCLK.

A write operation starts when R/W bit is 0. The SDO output to a write command, delivered in the next frame, contains status bits, data described in [表 6-12](#), and if the CRC is enabled, an 8-bit CRC for the output frame.

**表 6-12. Command Functions**

COMMAND BIT	SDI INPUT DATA WORD	SDO RESPONSE DATA WORD <sup>(1)</sup>
Write (R/W = 0)	Data to be written (16b)	0x0000
Read (R/W = 1)	Ignored <sup>(2)</sup>	Register output data (16b)

(1) Response data portion in next frame output.

(2) The input bits are included in the calculation for CRC, if enabled (see [セクション 6.5.3.3](#)).

Valid SDO output is driven only when  $\overline{CS} = 0$  and CONFIG.DSDO = 0; otherwise, the SDO pin remains Hi-Z to save power. The SDO data bits are left-justified within the frame, meaning the most significant bit is produced on the line (subject to timing details) when  $\overline{CS}$  is asserted low (bit is driven by falling edge of  $\overline{CS}$ ). The subsequent bits in the frame are driven by the rising SCLK edge when CONFIG.FSDO = 0 (default). To drive the SDO data on the falling edge of SCLK, set CONFIG.FSDO = 1. This setting effectively gives the SDO data an additional ½ clock period for setup time, but at the expense of hold time.

The frame output on SDO contains the command bit of the input that generated the frame (previous input frame), followed by seven status bits (see [図 6-29](#)). When an input frame CRC error is detected, the status bit CRC\_ERR = 1. If there is no input frame CRC error, then CRC\_ERR = 0. See [表 6-13](#) for details.

### 6.5.3.3 Frame Error Checking

If the AFE82H1 are used in a noisy environment, use the CRC to check the integrity of the SPI data communication between the device and the system controller. This feature is enabled by default and is controlled by the CONFIG.CRC\_EN bit. If the CRC is not required in the system, disable frame error checking through the CRC\_EN bit, and switch from the default 32-bit frame to the 24-bit frame.

Frame error checking is based on the CRC-8-ATM (HEC) polynomial:  $x^8 + x^2 + x + 1$  (9'b100000111).

For the output register readback, the AFE82H1 supply the calculated 8-bit CRC for the 24 bits of data provided, as part of the 32-bit frame.

The AFE82H1 decodes 24-bits of the input frame data and the 8-bit CRC to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is nonzero (that is, the input frame has single-bit or multiple-bit errors) the ALARM\_STATUS.CRC\_ERR\_CNT bits are incremented. A bad CRC value prevents execution of commands to the device, which prevents FIFO data from being lost as a result of an invalid read command.

When the CRC error counter reaches the limit programmed in CONFIG.CRC\_ERR\_CNT, the CRC\_FLT status bit is set in the ALARM\_STATUS register. The fault is reported (as long as the corresponding mask is not set) as an ALARM\_IRQ on SDO during the next frame. The  $\overline{ALARM}$  pin asserts low if enabled by the alarm action configuration (see [セクション 6.3.3.2](#)).

The CRC\_ERR status bit (see [図 6-29](#)) in the SDO frame is not sticky and is only reported for the previous frame. The ALARM\_STATUS.CRC\_FLT bit is sticky and is only cleared after a successful read of the

ALARM\_STATUS register. Read the GEN\_STATUS, MODEM\_STATUS or ALARM\_STATUS registers to clear any sticky bits that are set.

The sticky status bits are cleared at the start of the readback frame and are latched again at the end of the readback frame. Therefore, if the fault condition previously reported in the status register is no longer present at the end of the readback frame, and the data are received by the microcontroller with the CRC error, the fault information is lost. If a robust monitoring of the status bits is required in a noisy environment, use the IRQ pin in combination with the status mask bits to find out the status of each fault before clearing the status bits. Set the CONFIG.IRQ\_LVL bit to monitor the signal level on the IRQ pin, and unmask each status bit one at a time to retrieve the information from the status registers.

#### 6.5.3.4 Synchronization

The AFEx82H1 register map runs on the internal clock domain. Both the SPI and UBM packets are synchronized to this domain. This synchronization adds a latency of 0.4  $\mu$ s to 1.22  $\mu$ s (1.5 internal clocks), with respect to the rising edge of  $\overline{CS}$  or the STOP bit of the last byte of the UBM packet.

The effect of clock synchronization on UBM communication is not evident because of the lower speed and asynchronous nature of UBM communication.

In SPI mode, if changing register bits CONFIG.DSDO, CONFIG.FSDO, or CONFIG.CRC\_EN, keep  $\overline{CS}$  high for at least two clock cycles before issuing the next frame. Frame data corruption can occur if the two extra cycles are not used. The following are examples of frame corruption:

- Setting CONFIG.DSDO = 0: SDO begins to drive in the middle of the next frame.
- Changing CONFIG.FSDO: The launching edge of SDO changes in the middle of the next frame.
- Setting CONFIG.CRC\_EN = 1: The next frame has a CRC error because the CRC is enabled in the middle of the frame.

Send a NOP command (SDI = 0x00\_0000) after setting the DSDO, FSDO, and CRC\_EN bits to prevent the corrupted frames from impacting communication. Sending a NOP after CONFIG.CRC\_EN is set still generates a CRC error, and is reported in the STATUS portion of SDO. To avoid false errors, wait approximately 2  $\mu$ s after setting CONFIG.CRC\_EN before sending the next frame.

## 6.5.4 UART Interface

In UART mode, the device expects 1 start bit, 8 data bits, 1 odd parity bit, and 1 stop bit, or an 8O1 UART character format.

When using SPI to communicate with the registers, and only using UART for HART communication, use 1200 baud. The baud must have  $\pm 1\%$  accuracy.

### 6.5.4.1 UART Break Mode (UBM)

In UART break mode (UBM), the microcontroller issues a UART break to start communication. The device interprets the UART break as the start to receive commands from the UART. A communication UART character consists of one start bit, eight data bits, one odd parity bit, and at least one stop bit. A UART break character is all 11 bits (including start, data, parity and stop bit) held low by the microcontroller on the UARTIN pin and by the AFE82H1 on the UARTOUT pin. When a valid break character is detected on UARTIN by the AFE82H1, no parity (even though parity is odd) or stop bit errors are flagged for this character. The parity and stop bit differences between valid UBM break and communication characters must be managed by the system microcontroller when receiving these characters from the UARTOUT pin of the AFE82H1. See [図 5-2](#) for UBM break character, communication timing details, and bit order.

Two baud rates are supported for UART communication: 9600 and 1200. The 9600 baud rate is default for UBM. The 1200 baud rate is supported to maintain backward compatibility and requires the use of SPI to communicate with the register map; whereas, the UART pins are used only for HART communication. The baud rates are selected by register bit CONFIG.UART\_BAUD. When CONFIG.UART\_BAUD = 1 (default), the UART operates at 9600 baud. When CONFIG.UART\_BAUD = 0, the UART operates at 1200 baud. The break function of the UART protocol is enabled only for 9600 baud. This configuration allows interleaving of HART data with register communication and enables the access to all registers of the device, when configured correctly.

Set UBM.REG\_MODE = 1 to enable register map access through the UART. By default, this bit is set to 0. The entire register map can only be accessed with SPI, except for the UBM register. The UBM register can only be accessed with UBM. After UBM.REG\_MODE is set to 1, the SPI does not have access to the register map, and the full register map is accessible by UBM.

A UBM data output packet is initiated by AFE82H1 on UARTOUT in two cases. See [図 6-33](#) for packet structure details. If the R/IRQn status bit is 0 an IRQ event initiated the break command. If the R/IRQn status bit is 1, the break command is a response to the prior read request. For details on HART data see [セクション 6.5.4.1.1](#).

To enable IRQ events, set CONFIG.UBM\_IRQ\_EN = 1. When IRQ is enabled, the AFE82H1 triggers a break command followed by data on UARTOUT (see [図 6-33](#)).

The contents of the data are listed in order of priority below.

1. If ALARM\_IRQ bit is set, then the contents of the ALARM\_STATUS register are output.
2. If GEN\_IRQ is set, then the contents of the GEN\_STATUS register are output.
3. If MODEM\_IRQ bit is set, then the contents of the MODEM\_STATUS register are output.
4. If none of the previous bits are set, then an IRQ is not generated.

A break byte is followed by three bytes. These three bytes have information identical to the SPI frame without the CRC (see [図 6-30](#)). The CRC cannot be enabled for UBM. All communication characters on the UART bus are transmitted least significant data bit (D0) first.

[図 6-31](#) shows the data structure of the UBM write command, and [図 6-32](#) shows the data structure of the UBM read command.

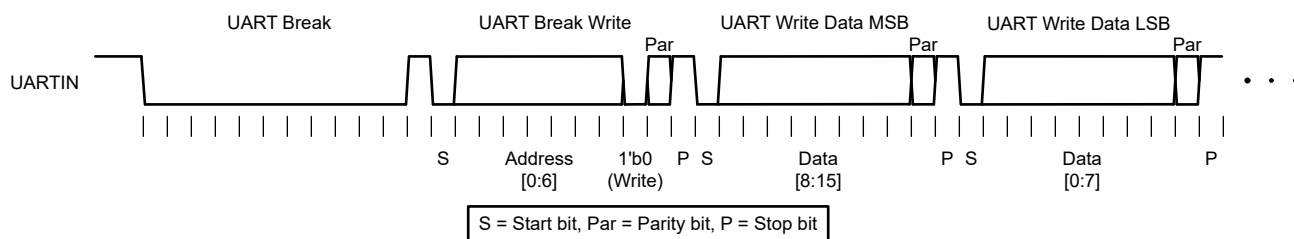


図 6-31. UARTIN Break Write Data Format

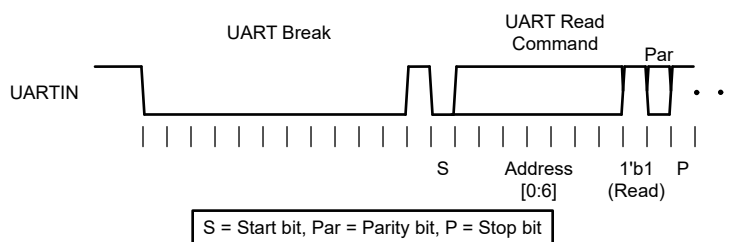


図 6-32. UARTIN Break Read Data Format

図 6-33 shows the UARTOUT data frame with details of the status bits produced by the AFEx82H1. See 表 6-13 for details.

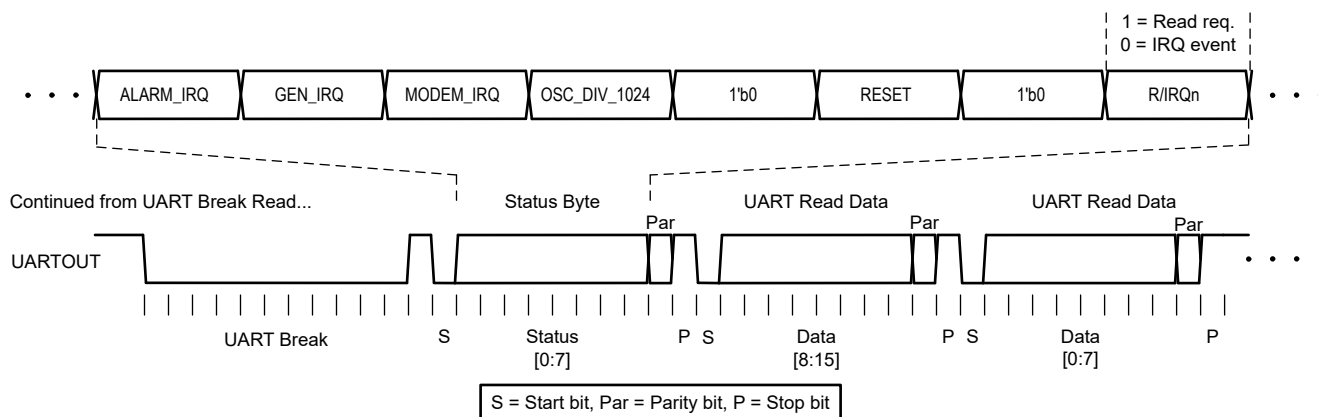


図 6-33. UARTOUT Break Data Format

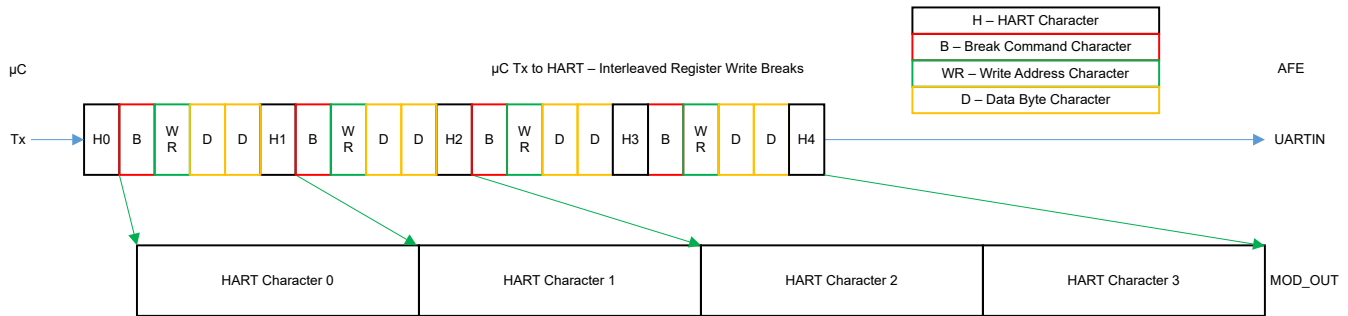
#### 6.5.4.1.1 Interface With FIFO Buffers and Register Map

In UBM, the HART data characters are interleaved with break commands for register map access or interrupt reporting.

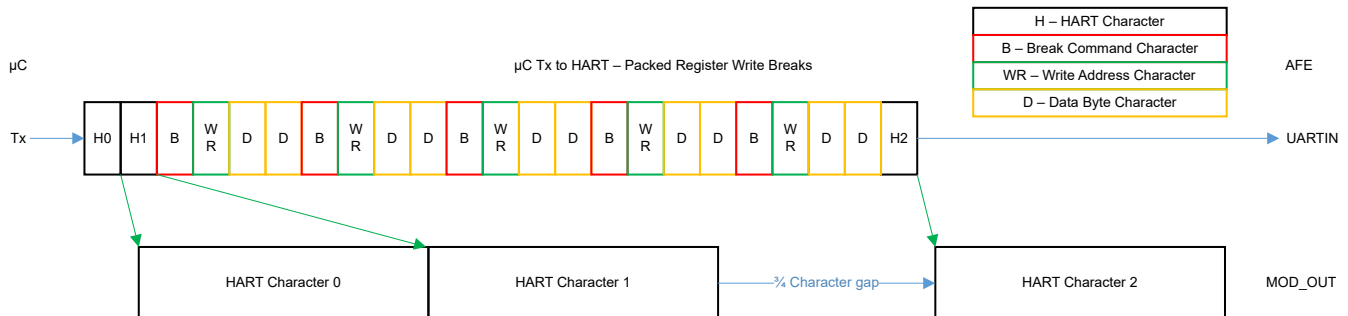
The device reports parity and frame errors received on UARTIN. These status bits can be found in the GEN\_STATUS register and are maskable to create IRQ events.

Avoid the large gaps between the HART bytes. The HART standard has a gap specification of 11 bit times ( $11 \times t_{\text{BAUDHART}}$  ms); therefore, gaps longer than 10.5 HART bit times ( $10.5 \times t_{\text{BAUDHART}}$  ms) can cause a gap error in the HART modem.

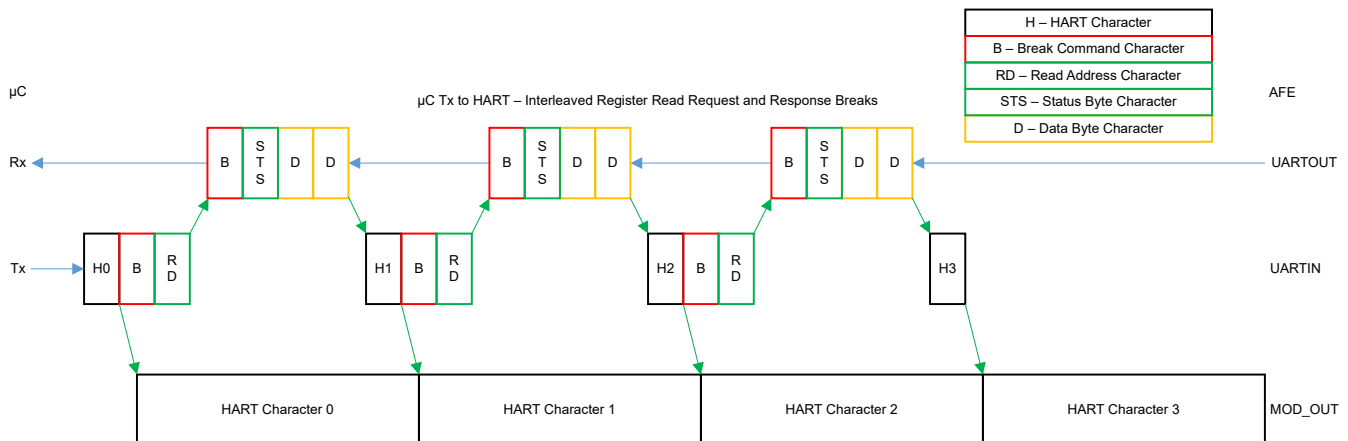
The following timing diagrams illustrate examples of microcontroller communication with the device registers, as well as HART transmit and receive data transfers.



**Figure 6-34. Interleaved HART Transmit With UBM Register Writes**



**Figure 6-35. Packed HART Transmit With UBM Register Writes**



**Figure 6-36. Interleaved HART Transmit With UBM Register Read Requests and Responses**

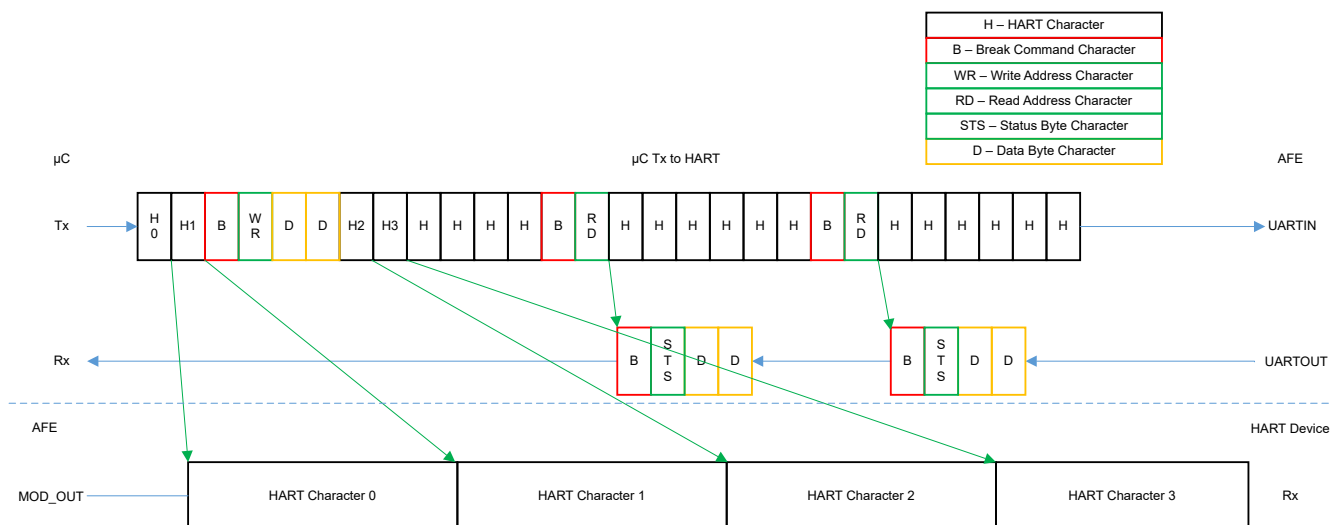


图 6-37. Packed HART Transmit With UBM Register Write and Read Requests and Responses

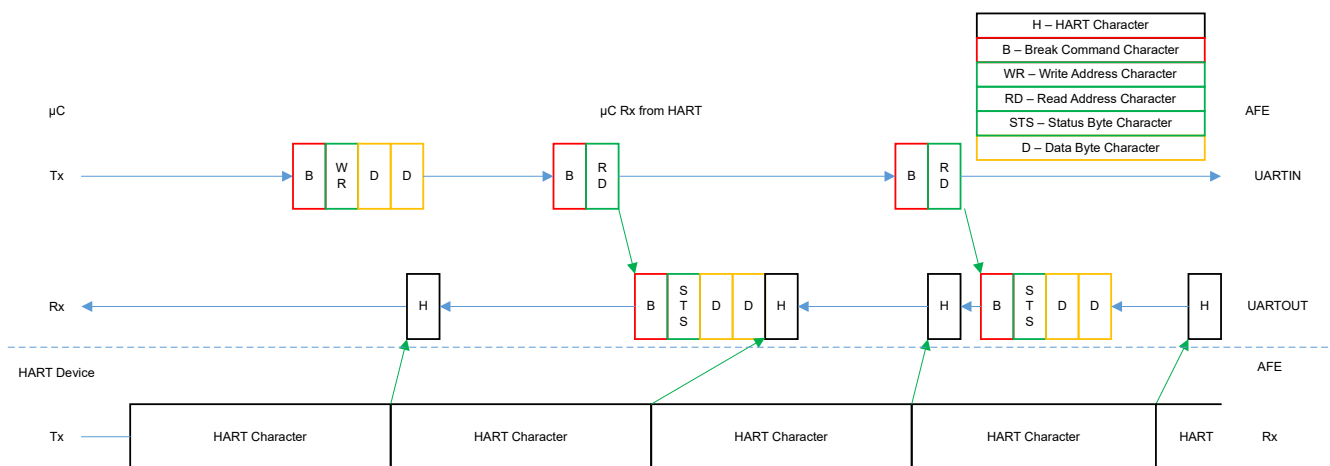


图 6-38. Interleaved HART Receive With UBM Register Write and Read Requests and Responses

### 6.5.5 Status Bits

In SPI mode and UBM, every response from the AFEx82H1 includes a set of status bits. For SPI mode bit order, see [セクション 6.5.3.1](#). For UBM bit order, [セクション 6.5.4.1](#).

**表 6-13. Status Bits**

STATUS BIT	DESCRIPTION	NOTES / REFERENCE
ALARM_IRQ	1h = ALARM_IRQ asserted 0h = Normal operation	From the GEN_STATUS <sup>(1)</sup> register (表 7-33). See also <a href="#">セクション 6.3.4</a> .
CRC_ERR (CRC enabled SPI only)	1h = CRC error detect in input frame 0h = No CRC error detected	Generated by the SPI on a frame by frame basis. See <a href="#">セクション 6.5.3.3</a> .
GEN_IRQ	1h = GEN_IRQ asserted 0h = Normal Operation	From the ALARM_STATUS <sup>(1)</sup> register (表 7-32). See also <a href="#">セクション 6.3.4</a> .
MODEM_IRQ	1h = MODEM_IRQ asserted 0h = Normal operation	From the GEN_STATUS <sup>(1)</sup> register (表 7-33). See also <a href="#">セクション 6.3.4</a> .
OSC_DIV_1024 (UBM mode)	1h = Sampled signal is high 0h = Sampled signal is low	Subdivided internal oscillator clock signal (frequency divided by 1024) sampled at the falling edge of the status byte start bit. See also <a href="#">セクション 6.3.8</a> .
OSC_DIV_2 (SPI mode)	1h = Sampled signal is high 0h = Sampled signal is low	Subdivided internal oscillator clock signal (frequency divided by 2) sampled at CS falling edge. See also <a href="#">セクション 6.3.8</a> .
R/IRQn (UBM only)	1h = Read request 0h = IRQ event	Generated by the UART interface on a frame by frame basis. See <a href="#">セクション 6.5.4.1</a> for details.
RBIST	1h = RBIST busy (registers not readable) 0h = RBIST done (registers readable)	RBIST running status. See <a href="#">セクション 6.4.2</a> for details.
RESET	1h = First readback after RESET 0h = All other readbacks	From the GEN_STATUS register (表 7-33). See also <a href="#">セクション 6.4.3</a> .

- (1) ALARM\_STATUS, MODEM\_STATUS, and GEN\_STATUS registers contain cross-readable IRQ flags for the other registers. The ALARM\_STATUS register has the GEN\_IRQ and MODEM\_IRQ bits. MODEM\_STATUS has the GEN\_IRQ and ALARM\_IRQ bits. GEN\_STATUS has the ALARM\_IRQ and MODEM\_IRQ bits. This functionality enables the system microcontroller to always get full status information by reading only one register, and thus save power.

### 6.5.6 Watchdog Timer

The AFEx82H1 include a watchdog timer (WDT) that is used to make sure that communication between the system controller and the device is not lost. The WDT checks that the device received a communication from the system controller within a programmable period of time. To enable this feature, set WDT.WDT\_EN to 1. The WDT monitors both SPI and UBM communications.

The WDT has two limit fields: WDT.WDT\_UP and WDT.WDT\_LO. The WDT\_UP field sets the upper time limit for the WDT. The WDT\_LO field sets the lower time limit. If the WDT\_LO is set to a value other than 2'b00, then the WDT acts as a window comparator. If the write occurs too quickly (less than the WDT\_LO time), or too slowly (greater than the WDT\_UP time), then a WDT error is asserted. When acting as a window comparator, in the event of a WDT error, the WDT resets only when a write to the WDT register occurs. If the WDT\_LO is set to 2'b00, then a write to any register resets the WDT time counter. In this mode, the WDT error is asserted when the timer expires.

If enabled, the chip must have any SPI or UBM write to the device within the programmed timeout window. Otherwise, the ALARM pin asserts low, and the ALARM\_STATUS.WD\_FLT bit is set to 1. The WD\_FLT bit is sticky. After a WD\_FLT has been asserted, WDT.WDT\_EN must be set to 0 to clear the WDT condition. Then the WDT can be re-enabled. The WDT condition is also cleared by issuing a software or hardware reset. After the WDT condition is clear, WD\_FLT is cleared by reading the ALARM\_STATUS register.

When using multiple AFEx82H1 devices in a daisy-chain configuration, connect the open-drain  $\overline{\text{ALARM}}$  pins of all devices together to form a wired-OR network. The watchdog timer can be enabled in any number of the devices in the chain; although, enabling the watchdog timer in one device in the chain is usually sufficient. The wired-OR  $\overline{\text{ALARM}}$  pin can be pulled low in response to the simultaneous presence of different trigger conditions in the devices in the daisy-chain. The host processor must read the ALARM\_STATUS register of each device to know all the fault conditions present in the chain.

The watchdog timeout period is based on a 1200-Hz clock (1.2288 MHz / 1024).

## 7 Register Maps

表 7-1 lists the memory-mapped registers for the AFEx82H1 registers. Consider all register offset addresses not listed in 表 7-1 as reserved locations; do not modify these register contents.

表 7-1. Register Map

ADDR (HEX)	REGISTER	BIT DESCRIPTION																
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00h	NOP	NOP [15:0]																
01h	DAC_DATA	DATA [15:0]																
02h	CONFIG	CRC_ERR_CNT [1:0]		CLKO [3:0]				UBM_IRQ_EN	IRQ_PIN_EN	CLR_PIN_EN	UART_DIS	UART_BAUD	CRC_EN	IRQ_POL	IRQ_LVL	DSDO	FSDO	
03h	DAC_CFG	RESERVED			PD	SR_CLK [2:0]			SR_STEP [2:0]			SR_EN	SR_MODE	RESERVED	CLR	RESERVED		
04h	DAC_GAIN	GAIN [15:0]																
05h	DAC_OFFSET	OFFSET [15:0]																
06h	DAC_CLR_CODE	CODE [15:0]																
07h	RESET	RESERVED								SW_RST [7:0]								
08h	ADC_CFG	BUF_PD	HYST [6:0]						FLT_CNT [2:0]			AIN_RANGE	EOC_PER_CH	CONV_RATE [1:0]		DIRECT_MODE		
09h	ADC_INDEX_CFG	RESERVED								STOP [3:0]				START [3:0]				
0Ah	TRIGGER	RESERVED												RBIST	MBIST	SHADOW_LOAD	ADC	
0Bh	SPECIAL_CFG <sup>(1)</sup>	RESERVED														OTP_LOAD_SW_RST	ALMV_POL	AIN1_ENB
0Eh	MODEM_CFG	Tx2200Hz	RESERVED		DUPLEX_EXT	RX_HORD_EN	RX_EXT_FILT_EN	TxRES	TxAMP [4:0]				HART_EN	DUPLEX	TxHPD	RTS		
0Fh	FIFO_CFG	RESERVED						FIFO_H2U_FLUSH	FIFO_U2H_FLUSH	H2U_LEVEL_SET [3:0]				U2H_LEVEL_SET [3:0]				
10h	ALARM_ACT	SD_FLT [1:0]		TEMP_FLT [1:0]		AIN1_FLT [1:0]		AIN0_FLT [1:0]		CRC_WDT_FLT [1:0]		VREF_FLT [1:0]		THERM_ERR_FLT [1:0]		THERM_WARN_FLT [1:0]		
11h	WDT	RESERVED										WDT_UP [2:0]			WDT_LO [1:0]		WDT_EN	
12h	AIN0_THRESHOLD	Hi [7:0]								Lo [7:0]								
13h	AIN1_THRESHOLD	Hi [7:0]								Lo [7:0]								
14h	TEMP_THRESHOLD	Hi [7:0]								Lo [7:0]								
15h	FIFO_U2H_WR	RESERVED						PARITY		DATA [7:0]								
16h	UBM <sup>(2)</sup>	RESERVED															REG_MODE	
18h	SCRATCH	DATA [15:0]																
19h	CHIP_ID_LSB	ID [15:0]																
1Ah	CHIP_ID_MSB	ID [15:0]																
1Bh	GPIO_CFG	RESERVED	EN [6:0]						RESERVED		ODE [6:0]							



**表 7-1. Register Map (続き)**

ADDR (HEX)	REGISTER	BIT DESCRIPTION															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1Ch	GPIO	RESERVED										DATA [6:0]					
1Dh	ALARM_STATUS_MASK	RESERVED		SD_FLT	OSC_FAIL	RESERVED			OTP_CRC_ERR	CRC_FLT	WD_FLT	VREF_FLT	ADC_AIN1_FLT	ADC_AIN0_FLT	ADC_TEMP_FLT	THERM_ERR_FLT	THERM_WARN_FLT
1Eh	GEN_STATUS_MASK	RESERVED					BIST_DONE	BIST_FAIL	RESERVED	SR_BUSYn	ADC_EOC	RESERVED		BREAK_FRAME_ERR	BREAK_PARITY_ERR	UART_FRAME_ERR	UART_PARITY_ERR
1Fh	MODEM_STATUS_MASK	RESERVED			GAP_ERR	FRAME_ERR	PARITY_ERR	FIFO_H2U_LEVEL_FLAG	FIFO_H2U_FULL_FLAG	FIFO_H2U_EMPTY_FLAG	FIFO_U2H_LEVEL_FLAG	FIFO_U2H_FULL_FLAG	FIFO_U2H_EMPTY_FLAG	CD_DE_ASSERT	CD_ASSERT	CTS_DE_ASSERT	CTS_ASSERT
20h	ALARM_STATUS	GEN_IRQ	MODEM_IRQ	SD_FLT	OSC_FAIL	CRC_CNT [1:0]		OTP_LOADEDn	OTP_CRC_ERR	CRC_FLT	WD_FLT	VREF_FLT	ADC_AIN1_FLT	ADC_AIN0_FLT	ADC_TEMP_FLT	THERM_ERR_FLT	THERM_WARN_FLT
21h	GEN_STATUS	ALARM_IRQ	MODEM_IRQ	RESERVED	OTP_BUSY	BIST_MODE	BIST_DONE	BIST_FAIL	RESET	SR_BUSYn	ADC_EOC	ADC_BUSY	PVDD_HI	BREAK_FRAME_ERR	BREAK_PARITY_ERR	UART_FRAME_ERR	UART_PARITY_ERR
22h	MODEM_STATUS	ALARM_IRQ	GEN_IRQ	RESERVED	GAP_ERR	FRAME_ERR	PARITY_ERR	FIFO_H2U_LEVEL_FLAG	FIFO_H2U_FULL_FLAG	FIFO_H2U_EMPTY_FLAG	FIFO_U2H_LEVEL_FLAG	FIFO_U2H_FULL_FLAG	FIFO_U2H_EMPTY_FLAG	CD_DE_ASSERT	CD_ASSERT	CTS_DE_ASSERT	CTS_ASSERT
23h	ADC_FLAGS	RESERVED							SD4_FAIL	SD3_FAIL	SD2_FAIL	SD1_FAIL	SD0_FAIL	TEMP_FAIL	AIN1_FAIL	AIN0_FAIL	RESERVED
24h	ADC_AIN0	RESERVED				DATA [11:0]											
25h	ADC_AIN1	RESERVED				DATA [11:0]											
26h	ADC_TEMP	RESERVED				DATA [11:0]											
27h	ADC_SD_MUX	RESERVED				DATA [11:0]											
28h	ADC_OFFSET	RESERVED				DATA [11:0]											
2Ah	FIFO_H2U_RD	LEVEL [3:0]				LEVEL_FLAG	FULL_FLAG	EMPTY_FLAG	PARITY	DATA [7:0]							
2Bh	FIFO_STATUS	H2U_LEVEL [3:0]				H2U_LEVEL_FLAG	H2U_FULL_FLAG	H2U_EMPTY_FLAG	RESERVED	U2H_LEVEL [3:0]				U2H_LEVEL_FLAG	U2H_FULL_FLAG	U2H_EMPTY_FLAG	RESERVED
2Ch	DAC_OUT	DATA [15:0]															
2Dh	ADC_OUT	RESERVED				DATA [11:0]											
2Eh	ADC_BYP	DATA_BYP_EN	OFST_BYP_EN	DIS_GND_SAMP	RESERVED	DATA [11:0]											
2Fh	FORCE_FAIL	CRC_FLT	VREF_FLT	THERM_ERR_FLT	THERM_WARN_FLT	RESERVED		SD4_HI_FLT	SD4_LO_FLT	SD3_HI_FLT	SD3_LO_FLT	SD2_HI_FLT	SD2_LO_FLT	SD1_HI_FLT	SD1_LO_FLT	SD0_HI_FLT	SD0_LO_FLT
3Bh	TIMER_CFG_0	RESERVED												CLK_SEL [1:0]		INVERT	ENABLE
3Ch	TIMER_CFG_1	PERIOD [15:0]															
3Dh	TIMER_CFG_2	SET_TIME [15:0]															
3Eh	CRC_RD	CRC [15:0]															
3Fh	RBIST_CRC	CRC [15:0]															

- (1) The SPECIAL\_CFG register can only be reset with POR, and does not respond to the RESET pin or SW\_RST command.  
 (2) The UBM register can only be accessed with a UBM command.

## 7.1 AFEx82H1 Registers

Complex bit access types are encoded to fit into small table cells. The following table shows the codes that are used for access types in this section.

**表 7-2. AFEx82H1 Access-Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
W	WO	Write only
W	WSC	Write self clear
<b>Reset or Default Value</b>		
-n		Value after reset or the default value
<b>Register Array Variables</b>		
i,j,k,l,m,n		When used in a register name, an offset, or an address, these variables refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When used in a register name, an offset, or an address, this variable refers to the value of a register array.

### 7.1.1 NOP Register (Offset = 0h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-3. NOP Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	NOP	WO	0h	No operation. Data written to this field have no effect. Always reads zeros.

### 7.1.2 DAC\_DATA Register (Offset = 1h) [Reset = 0000h]

Return to the [Register Map](#).

DAC code for VOUT.

**表 7-4. DAC\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	DATA	R/W	0h	Data. DAC code for VOUT.

### 7.1.3 CONFIG Register (Offset = 2h) [Reset = 0036h]

Return to the [Register Map](#).

**表 7-5. CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	CRC_ERR_CNT	R/W	0h	CRC Errors Count Limit Sets the numbers of consecutive SPI CRC frames that must have errors before the status bits is set. 0h = 1 (default); 1h = 2; 2h = 4; 3h = 8
13-10	CLKO	R/W	0h	CLKO Enable Enable the CLK_OUT pin and set the divider value. 0h = CLKO disabled (default); 1h = 1.2288 MHz; 2h = 1.2288 / 2 MHz; 3h = 1.2288 / 4 MHz; 4h = 1.2288 / 8 MHz; 5h = 1.2288 / 16 MHz; 6h = 1.2288 / 32 MHz; 7h = 1.2288 / 64 MHz; 8h = 1.2288 / 128 MHz; 9h = 1.2288 / 256 MHz; Ah = 1.2288 / 512 MHz; Bh = 1.2288 / 1024 MHz; Ch = 1'b0; Dh = 1'b0; Eh = 1'b0; Fh = Timer
9	UBM_IRQ_EN	R/W	0h	UBM IRQ Enable Enable IRQ to be sent on UARTOUT through UBM. 0h = Disabled (default); 1h = Enabled
8	IRQ_PIN_EN	R/W	0h	IRQ Pin Enable Enable IRQ pin functionality. 0h = Disabled (default); 1h = Enabled
7	CLR_PIN_EN	R/W	0h	Clear Input Pin Enable Enable pin-based transition to the CLEAR state in UBM. 0h = Disabled (default); 1h = SDI pin configured as clear input pin
6	UART_DIS	R/W	0h	UART Disable Disable UART functionality. 0h = UART Enabled (default); 1h = UART Disabled
5	UART_BAUD	R/W	1h	UART Baud Configure BAUD rate for UART. 0h = 1200 baud (no break); 1h = 9600 baud (Break mode) (default)
4	CRC_EN	R/W	1h	CRC Enable Enable CRC for SPI. 0h = Disabled; 1h = Enabled (default)
3	IRQ_POL	R/W	0h	IRQ Polarity 0h = Active low (default); 1h = Active high
2	IRQ_LVL	R/W	1h	IRQ Level 0h = Edge sensitive; 1h = Level sensitive (default)
1	DSDO	R/W	1h	SDO Hi-Z 0h = Drive SDO during $\overline{CS}$ = 0; 1h = SDO always Hi-Z (default)
0	FSDO	R/W	0h	Fast SDO SDO is driven on negative edge of SCLK. 0h = drive SDO on rising edge of SCLK (launching edge) (default) 1h = drive SDO on falling edge of SCLK (capture edge 1/2 clock early)

### 7.1.4 DAC\_CFG Register (Offset = 3h) [Reset = 0B00h]

Return to the [Register Map](#).

**表 7-6. DAC\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	
12	PD	R/W	0h	DAC Output Buffer Power-down DAC output set to Hi-Z in power-down. 0h = DAC output buffer enabled (default) 1h = DAC output buffer disabled
11-9	SR_CLK	R/W	5h	Slew Clock Rate 0h = 307.2 kHz 1h = 153.6 kHz 2h = 76.8 kHz 3h = 38.4 kHz 4h = 19.2 kHz 5h = 9600 Hz (default) 6h = 4800 Hz 7h = 2400 Hz
8-6	SR_STEP	R/W	4h	Slew Step Size 0h = 1 code 1h = 2 codes 2h = 4 codes 3h = 8 codes 4h = 16 codes (default) 5h = 32 codes 6h = 64 codes 7h = 128 codes
5	SR_EN	R/W	0h	Slew Enable Enables slew on the output voltage. 0h = Disabled (default) 1h = Enabled
4	SR_MODE	R/W	0h	Slew Mode Output slew rate mode select. 0h = Linear Slew (default) 1h = Sinusoidal Slew
3	RESERVED	R	0h	
2	CLR	R/W	0h	CLEAR State 0h = Normal operation (default) 1h = Force the DAC to the CLEAR state
1-0	RESERVED	R	0h	

### 7.1.5 DAC\_GAIN Register (Offset = 4h) [Reset = 8000h]

Return to the [Register Map](#).

**表 7-7. DAC\_GAIN Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	GAIN	R/W	8000h	Gain Set the gain of the DAC output from 0.5 – 1.499985. For example: 0000h = 0.5 8000h = 1.0 (default) FFFFh = 1.499985

### 7.1.6 DAC\_OFFSET Register (Offset = 5h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-8. DAC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	OFFSET	R/W	0h	Offset Adjust the offset of the DAC output, 2's complement number. For example: 0000h = 0 (default) FFFFh = -1

### 7.1.7 DAC\_CLR\_CODE Register (Offset = 6h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-9. DAC\_CLR\_CODE Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	CODE	R/W	0h	CLEAR State DAC Code DAC code applied in the CLEAR state. See <a href="#">セクション 6.3.1.6</a> .

### 7.1.8 RESET Register (Offset = 7h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-10. RESET Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	SW_RST	WSC	0h	Software Reset Write ADh to initiate software reset.

## 7.1.9 ADC\_CFG Register (Offset = 8h) [Reset = 8810h]

Return to the [Register Map](#).

**表 7-11. ADC\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	BUF_PD	R/W	1h	ADC Buffer Power-Down 0h = ADC buffer enabled; 1h = ADC buffer powered down (default)
14-8	HYST	R/W	8h	Hysteresis The number of codes of hysteresis used when a threshold is exceeded for an ADC measurement of AIN0/AIN1/TEMP.
7-5	FLT_CNT	R/W	0h	Fault Count Number of successive faults to trip an alarm. Number of successive faults is programmed value + 1 (1-8 faults).
4	AIN_RANGE	R/W	1h	ADC Analog Input Range Can only be set if PVDD ≥ 2.7 V to use 2.5-V range for AIN0 and AIN1 inputs. 0h = 2 × VREF; 1h = 1 × VREF (default)
3	EOC_PER_CH	R/W	0h	ADC End-of-Conversion for Every Channel Sends an EOC pulse at the end of each channel instead of at the end of all the channels. 0h = EOC after last channel (default); 1h = EOC for every channel
2-1	CONV_RATE	R/W	0h	ADC Conversion Rate This setting only affects the conversion rate for channels AIN0 and AIN1. Rates are based on a 76.8-kHz ADC clock. All other channels use 2560 Hz. 0h = 3840 Hz (default) 1h = 2560 Hz 2h = 1280 Hz 3h = 640 Hz
0	DIRECT_MODE	R/W	0h	Direct Mode Enable 0h = Auto mode (default); 1h = Direct mode

## 7.1.10 ADC\_INDEX\_CFG Register (Offset = 9h) [Reset = 0080h]

Return to the [Register Map](#).

The ADC custom channel sequencing configuration is shown in [表 7-12](#).

**表 7-12. ADC\_INDEX\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-4	STOP	R/W	8h	Custom Channel Sequencer Stop Index CCS index to stop ADC sequence. Must be ≥ START. If not, STOP is forced to = START. 0h = OFFSET 1h = AIN0 2h = AIN1 3h = TEMP 4h = SD0 (VREF) 5h = SD1 (PVDD) 6h = SD2 (VDD) 7h = SD3 (ZTAT) 8h = SD4 (VOUT) (default) 9h through Fh = GND
3-0	START	R/W	0h	Custom Channel Sequencer Start Index CCS index to start ADC sequence. 0h through Fh = Same as STOP field (0h is default)

### 7.1.11 TRIGGER Register (Offset = Ah) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-13. TRIGGER Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	
3	RBIST	WSC	0h	RBIST Trigger This trigger initiates a Register BIST. This BIST runs a CRC calculation through the configuration registers (表 6-9) and compares the result to a stored CRC value in the RBIST_CRC register.
2	MBIST	WSC	0h	Memory Built-In Self-Test Trigger This trigger initiates an MBIST on the SRAM that is used for the FIFO. During this time communication to/from HART does not work as MBIST takes over the control of the SRAM.
1	SHADOWLOAD	WSC	0h	Shadow Load Trigger This trigger initiates the loading of the OTP array into the parallel latches. If an OTP CRC error is detected, assert this trigger to try and reload the OTP into the memory locations.
0	ADC	WSC	0h	ADC Trigger In auto mode, this bit enables or disables the conversions. Manually set to 1 (enable) or 0 (disable). In direct mode, set this bit to start a conversion sequence. The bit is cleared at the end of the sequence. To stop a sequence prematurely, manually clear this bit.

### 7.1.12 SPECIAL\_CFG Register (Offset = Bh) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-14. SPECIAL\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	
2	OTP_LOAD_SW_RST	R/W	0h	OTP (One Time Programmable Factory Trimmed Registers) LOAD with SW RESET OTP reloads with the assertion of a software reset (SW_RST). 0h = No reload with SW_RST 1h = Reload with SW_RST
1	ALMV_POL	R/W	0h	Alarm Voltage Polarity This register bit is ORed with the POL_SEL/AIN1 pin (if AIN1_ENB bit is low) to control the VOUT during a hardware reset condition or if alarm is active and alarm action is set appropriately. The following Boolean function is implemented for the internal signal ALMV_POL_o that sets the VOUT voltage: ALMV_POL_o = ALMV_POL OR (POL_SEL/AIN1 AND NOT AIN1_ENB) 0h = Low (0 V) 1h = High (2.5 V)
0	AIN1_ENB	R/W	0h	AIN1 Pin Enable This bit determines whether the POL_SEL/AIN1 pin acts as alarm voltage polarity control bit or an input channel to the ADC. 0h = AIN1 pin acts as alarm voltage polarity bit and ADC converts GND 1h = AIN1 pin is an active channel to the ADC

### 7.1.13 MODEM\_CFG Register (Offset = Eh) [Reset = 0040h]

Return to the [Register Map](#).

**表 7-15. MODEM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	Tx2200Hz	R/W	0h	Transmit 2200 Hz Only By not sending data to the FIFO buffer and asserting RTS, the user can transmit multiples of 1200 Hz as long as RTS is asserted. By setting this bit the user can transmit multiples of 2200 Hz. Setting this bit prevents data in the FIFO buffer from being correctly transmitted. If using this bit there is no need to use the FIFO buffer. 0h = Transmit 1200 Hz and 2200 Hz (default) 1h = Transmit only 2200 Hz
14-13	RESERVED	R	0h	
12	DUPLEX_EXT	R/W	0h	Duplex External Mode Allows full duplex mode but expects the connection of MOD_OUT to RX_IN to be made externally. 0h = Internal duplex connection (default) 1h = External duplex connection
11	RX_HORD_EN	R/W	0h	High Order Filter Enable Enables a higher order filter on HART_RX. 0h = Disable (default); 1h = Enable
10	RX_EXTFILT_EN	R/W	0h	External Filter Enable Enables the use of an external filter for HART_RX. If enabled, then connect the HART signal to RX_INF. 0h = Use internal filter (default); 1h = Use external filter
9	TxRES	R/W	0h	HART Transmit Resolution 0h = 32 steps per period (default) at 38.4 kHz update rate for 1200 baud 1h = 128 steps per period at 153.6 kHz update rate for 1200 baud 128-step per period waveform consumes more power.
8-4	TxAMP	R/W	4h	Transmit Amplitude HART Tx amplitude. 00h = 400 mV <sub>PP</sub> ; 01h = 425 mV <sub>PP</sub> 02h = 450 mV <sub>PP</sub> ; 03h = 475 mV <sub>PP</sub> 04h = 500 mV <sub>PP</sub> (default); 05h = 525 mV <sub>PP</sub> 06h = 550 mV <sub>PP</sub> ; 07h = 575 mV <sub>PP</sub> 08h = 600 mV <sub>PP</sub> ; 09h = 625 mV <sub>PP</sub> 0Ah = 650 mV <sub>PP</sub> ; 0Bh = 675 mV <sub>PP</sub> 0Ch = 700 mV <sub>PP</sub> ; 0Dh = 725 mV <sub>PP</sub> 0Eh = 750 mV <sub>PP</sub> ; 0Fh = 775 mV <sub>PP</sub> 10h through 1Fh = 800 mV <sub>PP</sub>
3	HART_EN	R/W	0h	HART Enable Enable the HART Tx and Rx. 0h = Disable (default); 1h = Enable
2	DUPLEX	R/W	0h	Duplex Mode Enable internal connection of Tx to Rx for debug and testing. 0h = Normal operation (default); 1h = Duplex enabled
1	TxHPD	R/W	0h	HART Tx DAC Output Buffer Hi-Z in Rx Mode or When Disabled 0h = HART Tx DAC output is set to midcode with 50 kΩ output impedance (default) 1h = HART Tx DAC is Hi-Z in Rx mode or when disabled. Users can set the default voltage level with an external circuit.
0	RTS	R/W	0h	Request To Send Starts transmitting a carrier on MOD_OUT pin. 0h = No action (default) 1h = Request to send. Device starts modulating the MOD_OUT pin if CD = 0.



### 7.1.14 FIFO\_CFG Register (Offset = Fh) [Reset = 00F0h]

Return to the [Register Map](#).

**表 7-16. FIFO\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	
9	FIFO_H2U_FLUSH	WSC	0h	Flush HART-to-μC FIFO (FIFO_H2U) Clear the pointers for the FIFO_H2U.
8	FIFO_U2H_FLUSH	WSC	0h	Flush μC-to-HART FIFO (FIFO_U2H) Clear the pointers for the FIFO_U2H.
7-4	H2U_LEVEL_SET	R/W	Fh	FIFO_H2U FIFO Level Flag Trip Set Sets the level for FIFO_H2U at which the Level Flag trips. This is a (>) comparison. Because the FIFO size is 5 bits wide, the LSB is not used with this 4-bit setting. Only change this field while MODEM_CFG.HART_EN = 0.
3-0	U2H_LEVEL_SET	R/W	0h	FIFO_U2H FIFO Level Flag Trip Set Sets the level for FIFO_U2H at which the Level Flag trips. This is a (<) comparison. Because the FIFO size is 5 bits wide, the LSB is not used with this 4-bit setting. Only change this field while MODEM_CFG.HART_EN = 0.

### 7.1.15 ALARM\_ACT Register (Offset = 10h) [Reset = 8020h]

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**表 7-17. ALARM\_ACT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	SD_FLT	R/W	2h	Self-Diagnostic Fault Action These bits set the device action after a self-diagnostic fault. 0h = No Action 1h = Set DAC to CLEAR state 2h = Switch to alarm voltage determined by ALMV_POL (default) 3h = Place DAC into Hi-Z (power-down)
13-12	TEMP_FLT	R/W	0h	TEMP Fault Action These bits set the device action if the ADC temperature is outside the TEMP_THRESHOLD Hi or Lo thresholds. 0h through 3h = Same as SD_FLT field (default 0h)
11-10	AIN1_FLT	R/W	0h	AIN1 Fault Action These bits set the device action if the ADC AIN1 channel is outside the AIN1_THRESHOLD Hi or Lo thresholds. 0h through 3h = Same as SD_FLT field (default 0h)
9-8	AIN0_FLT	R/W	0h	AIN0 Fault Action These bits set the device action if the ADC AIN0 channel is outside the AIN0_THRESHOLD Hi or Lo thresholds. 0h through 3h = Same as SD_FLT field (default 0h)
7-6	CRC_WDT_FLT	R/W	0h	CRC and WDT Fault Action These bits set the device action when a SPI CRC or SPI Watchdog Timeout error occurs. 0h through 3h = Same as SD_FLT field (default 0h)
5-4	VREF_FLT	R/W	2h	VREF Fault Action These bits set the device action when a fault is detected on VREF. 0h through 3h = Same as SD_FLT field a
3-2	THERM_ERR_FLT	R/W	0h	Thermal Error Fault Action These bits set the device action when a high temperature error occurs (> 130°C). 0h through 3h = Same as SD_FLT field (default 0h)

表 7-17. ALARM\_ACT Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1-0	THERM_WARN_FLT	R/W	0h	Thermal Warning Fault Action These bits set the device action when a high temperature warning occurs (> 85°C). 0h through 3h = Same as SD_FLT field (default 0h)

### 7.1.16 WDT Register (Offset = 11h) [Reset = 0018h]

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**表 7-18. WDT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	
5-3	WDT_UP	R/W	3h	Watchdog Timer (WDT) Upper Limit If the WDT is enabled and the timer exceeds the programmed value, a WDT error is asserted. All times are based on 1200-Hz clock (1.2288 MHz / 1024). 0h = 53 ms (64 clocks) 1h = 106 ms (128 clocks) 2h = 427 ms (512 clocks) 3h = 853 ms (1024 clocks, default) 4h = 1.7 s (2048 clocks) 5h = 2.56 s (3072 clocks) 6h = 3.41 s (4096 clocks) 7h = 5.12 s (6144 clocks)
2-1	WDT_LO	R/W	0h	WDT Lower Limit If the WDT is enabled and the WDT Lower Limit is enabled, then only a write to this register resets the WDT timer. If the write occurs before the WDT Lower Limit time, or after the WDT Upper Limit time, then a WDT error is asserted. If WDT Lower Limit is disabled, then a write to any register resets the timer. This is true for both SPI and UART Break modes. All times are based on 1200-Hz clock (1.2288 MHz / 1024). 0h = Disabled (default) 1h = 53 ms (64 clocks) 2h = 106 ms (128 clocks) 3h = 427 ms (512 clocks)
0	WDT_EN	R/W	0h	WDT Enable 0h = Disabled (default); 1h = Enabled

### 7.1.17 AIN0\_THRESHOLD Register (Offset = 12h) [Reset = FF00h]

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**表 7-19. AIN0\_THRESHOLD Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	Hi	R/W	FFh	High Threshold for Channel AIN0 {[11:4],4b1111} This value is compared (>) against AIN0 data bits[11:0].
7-0	Lo	R/W	0h	Low Threshold for Channel AIN0 {[11:4],4b0000} This value is compared (<) against AIN0 data bits[11:0].

### 7.1.18 AIN1\_THRESHOLD Register (Offset = 13h) [Reset = FF00h]

Return to the [Register Map](#).

**表 7-20. AIN1\_THRESHOLD Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	Hi	R/W	FFh	High Threshold for Channel AIN1 {[11:4],4b1111} This value is compared (>) against AIN1 data bits[11:0].
7-0	Lo	R/W	0h	Low Threshold for Channel AIN1 {[11:4],4b0000} This value is compared (<) against AIN1 data bits[11:0].

### 7.1.19 TEMP\_THRESHOLD Register (Offset = 14h) [Reset = FF00h]

Return to the [Register Map](#).

**表 7-21. TEMP\_THRESHOLD Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	Hi	R/W	FFh	High Threshold for Channel TEMP {[11:4],4b1111} This value is compared (>) against TEMP data bits[11:0].
7-0	Lo	R/W	0h	Low Threshold for Channel TEMP {[11:4],4b0000} This value is compared (<) against TEMP data bits[11:0].

### 7.1.20 FIFO\_U2H\_WR Register (Offset = 15h) [Reset = 0000h]

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This register controls the HART to microcontroller FIFO buffer.

**表 7-22. FIFO\_U2H\_WR Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	
8	PARITY	WO	0h	Parity Odd parity bit to be transmitted with data. This field can only be written by SPI and affects the FIFO when CONFIG.UART_DIS = 1. Otherwise writes to this register are ignored.
7-0	DATA	WO	0h	Data Byte This field can only be written by SPI and affects the FIFO when CONFIG.UART_DIS = 1. Otherwise writes to this register are ignored.

### 7.1.21 UBM Register (Offset = 16h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-23. UBM Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	
0	REG_MODE	R/W	0h	Register Mode Configure the rest of the Register Map to be accessed by UART break mode (UBM) or SPI. This register can only be written by the UART Break communication. 0h = SPI Mode (default) 1h = UART Break Mode

### 7.1.22 SCRATCH Register (Offset = 18h) [Reset = FFFFh]

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**表 7-24. SCRATCH Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	DATA	R/W	FFFFh	Scratch Data Data written is read back as the inverted value. For example, writing 0xAAAA is read back as 0x5555.

### 7.1.23 CHIP\_ID\_LSB Register (Offset = 19h)

Return to the [Register Map](#).

**表 7-25. CHIP ID LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	ID	R		Unique part number within each lot

### 7.1.24 CHIP\_ID\_MSB Register (Offset = 1Ah)

Return to the [Register Map](#).

**表 7-26. CHIP ID MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	ID	R		Encoded lot identification number

### 7.1.25 GPIO\_CFG Register (Offset = 1Bh) [Reset = 00FFh]

Return to the [Register Map](#).

**表 7-27. GPIO CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14-8	EN	R/W	00h	GPIO per Pin Enable. (See <a href="#">表 6-11</a> for additional configuration required specific to each pin and communication mode) [14] = GPIO6 [13] = GPIO5 [12] = GPIO4 [11] = GPIO3 [10] = GPIO2 [9] = GPIO1 [8] = GPIO0 0h = GPIO function disable 1h = GPIO function enabled For any pin used either for the communication function or not used as an active GPIO, set this bit to 0h.
7	RESERVED	R	0h	
6-0	ODE	R/W	FFh	Pseudo Open Drain Enable GPIO output enable and pseudo open drain functionality on the GPIO pins. (See <a href="#">表 6-11</a> for additional configuration required specific to each pin and communication mode.) [6] = GPIO6 [5] = GPIO5 [4] = GPIO4 [3] = GPIO3 [2] = GPIO2 [1] = GPIO1 [0] = GPIO0 0h = Push-pull output enabled 1h = Pseudo open-drain output enabled

### 7.1.26 GPIO Register (Offset = 1Ch) [Reset = 007Fh]

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**表 7-28. GPIO Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	
6-0	DATA	R/W	7Fh	<p>GPIO pin data.</p> <p>For GPIO input this bit must be written as 1 and GPIO_CFG.ODE = 1 and GPIO_CFG.EN = 1. Reading this register reads the pin value when the pin is correctly enabled. (See <a href="#">表 6-11</a> for additional configuration required specific to each pin and communication mode)</p> <p>For GPIO output this bit sets the pin value.</p> <p>[6] = GPIO6  [5] = GPIO5  [4] = GPIO4  [3] = GPIO3  [2] = GPIO2  [1] = GPIO1  [0] = GPIO0</p>

### 7.1.27 ALARM\_STATUS\_MASK Register (Offset = 1Dh) [Reset = EFDFh]

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**表 7-29. ALARM\_STATUS\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	3h	
13	SD_FLT	R/W	1h	SD Fault Mask 0h = Fault asserts IRQ 1h = The mask prevents IRQ or Alarm being triggered (default). The status is always set if the condition exists.
12	OSC_FAIL	R/W	0h	OSC_FAIL Fault Mask Same as SD Fault Mask (default 0h).
11-9	RESERVED	R	7h	
8	OTP_CRC_ERR	R/W	1h	OTP CRC Error Mask Same as SD Fault Mask (default 1h).
7	CRC_FLT	R/W	1h	SPI CRC Fault Mask Same as SD Fault Mask (default 1h).
6	WD_FLT	R/W	1h	Watchdog Fault Mask Same as SD Fault Mask (default 1h).
5	VREF_FLT	R/W	0h	VREF Fault Mask Same as SD Fault Mask (default 0h).
4	ADC_AIN1_FLT	R/W	1h	ADC AIN1 Fault Mask Same as SD Fault Mask (default 1h).
3	ADC_AIN0_FLT	R/W	1h	ADC AIN0 Fault Mask Same as SD Fault Mask (default 1h).
2	ADC_TEMP_FLT	R/W	1h	ADC TEMP Fault Mask Same as SD Fault Mask (default 1h).
1	THERM_ERR_FLT	R/W	1h	Temperature > 130°C Error Mask Same as SD Fault Mask (default 1h).
0	THERM_WARN_FLT	R/W	1h	Temperature > 85°C Warning Mask Same as SD Fault Mask (default 1h).

## 7.1.28 GEN\_STATUS\_MASK Register (Offset = 1Eh) [Reset = FFFFh]

Return to the [Register Map](#).

**表 7-30. GEN\_STATUS\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	
10	BIST_DONE	R/W	1h	BIST Done Mask 0h = Fault asserts IRQ 1h = The mask prevents IRQ or Alarm being triggered (default). The status is always set if the condition exists.
9	BIST_FAIL	R/W	1h	BIST Failed Fault Mask Same as BIST Done Mask (default 1h).
8	RESERVED	R	1h	
7	SR_BUSYn	R/W	1h	Slew Rate Not Busy Mask Same as BIST Done Mask (default 1h).
6	ADC_EOC	R/W	1h	ADC End Of Conversion Mask Same as BIST Done Mask (default 1h).
5-4	RESERVED	R	3h	
3	BREAK_FRAME_ERR	R/W	1h	Break Frame Error Fault Mask Same as BIST Done Mask (default 1h).
2	BREAK_PARITY_ERR	R/W	1h	Break Parity Error Fault Mask Same as BIST Done Mask (default 1h).
1	UART_FRAME_ERR	R/W	1h	UART Frame Error Fault Mask Same as BIST Done Mask (default 1h).
0	UART_PARITY_ERR	R/W	1h	UART Parity Error Fault Mask Same as BIST Done Mask (default 1h).



## 7.1.29 MODEM\_STATUS\_MASK Register (Offset = 1Fh) [Reset = FFFFh]

Return to the [Register Map](#).

**表 7-31. MODEM\_STATUS\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	
12	GAP_ERR	R/W	1h	HART Gap Error Fault Mask 0h = Fault asserts IRQ 1h = The mask prevents IRQ or Alarm being triggered (default). The status is always set if the condition exists.
11	FRAME_ERR	R/W	1h	HART Frame Error Fault Mask Same as HART Gap Error Fault Mask (default 1h).
10	PARITY_ERR	R/W	1h	HART Parity (ODD) Error Fault Mask Same as HART Gap Error Fault Mask (default 1h).
9	FIFO_H2U_LEVEL_FLAG	R/W	1h	FIFO_H2U Level Flag Mask Same as HART Gap Error Fault Mask (default 1h).
8	FIFO_H2U_FULL_FLAG	R/W	1h	FIFO_H2U Full Flag Mask Same as HART Gap Error Fault Mask (default 1h).
7	FIFO_H2U_EMPTY_FLAG	R/W	1h	FIFO_H2U Empty Flag Mask Same as HART Gap Error Fault Mask (default 1h).
6	FIFO_U2H_LEVEL_FLAG	R/W	1h	FIFO_U2H Level Flag Mask Same as HART Gap Error Fault Mask (default 1h).
5	FIFO_U2H_FULL_FLAG	R/W	1h	FIFO_U2H Full Flag Mask Same as HART Gap Error Fault Mask (default 1h).
4	FIFO_U2H_EMPTY_FLAG	R/W	1h	FIFO_U2H Empty Flag Mask Same as HART Gap Error Fault Mask (default 1h).
3	CD_DEASSERT	R/W	1h	CD Deasserted Flag Mask Same as HART Gap Error Fault Mask (default 1h).
2	CD_ASSERT	R/W	1h	CD Asserted Flag Mask Same as HART Gap Error Fault Mask (default 1h).
1	CTS_DEASSERT	R/W	1h	CTS Deasserted Flag Mask Same as HART Gap Error Fault Mask (default 1h).
0	CTS_ASSERT	R/W	1h	CTS Asserted Flag Mask Same as HART Gap Error Fault Mask (default 1h).

### 7.1.30 ALARM\_STATUS Register (Offset = 20h) [Reset = 0200h]

Return to the [Register Map](#).

**表 7-32. ALARM\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	GEN_IRQ	R	0h	General IRQ OR of all the unmasked bits in the GEN_STATUS register. 0h = All of the unmasked bits of the GEN_STATUS register are low 1h = At least one of the unmasked bits in the GEN_STATUS register is high
14	MODEM_IRQ	R	0h	Modem IRQ OR of all the unmasked bits in the MODEM_STATUS register. 0h = All of the unmasked bits of the MODEM_STATUS register are low 1h = At least one of the unmasked bits in the MODEM_STATUS register is high
13	SD_FLT	R	0h	Self Diagnostic (SD) Fault 0h = All self diagnostic channels are within threshold limits 1h = At least one of the self diagnostic channels has failed
12	OSC_FAIL	R	0h	Oscillator Fault Oscillator failed to start. This bit holds $\overline{\text{ALARM}}$ low and does not feed IRQ. 0h = Oscillator started; 1h = Oscillator has failed to start
11-10	CRC_CNT	R	0h	CRC Fault Counter If counter limit $\leq 4$ then bits[1:0] of the counter are shown here. If the counter limit = 8 then bits[2:1] of the counter are shown.
9	OTP_LOADEDn	R	1h	OTP NOT Loaded Clears when OTP has loaded at least once. Keeps $\overline{\text{ALARM}}$ asserted until OTP finishes loading. Does not feed IRQ. 0h = OTP has loaded at least once; 1h = OTP has not finished loading
8	OTP_CRC_ERR	R	0h	OTP CRC Error Maskable fault. An error occurred with the OTP CRC calculation. Sticky, cleared by reading register, unless condition still persist. 0h = No OTP CRC fault; 1h = OTP CRC fault
7	CRC_FLT	R	0h	CRC Fault Maskable fault. Invalid CRC value transmitted during SPI frame. Sticky, cleared by reading register, unless condition still persist. 0h = No CRC fault; 1h = CRC fault
6	WD_FLT	R	0h	Watchdog Timer Fault Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = No watchdog fault; 1h = Watchdog fault
5	VREF_FLT	R	0h	Invalid Reference Voltage Maskable fault. OR with FORCE_FAIL.VREF_FLT bit. Active signal, set as long as condition is true. Direct input from analog circuit. 0h = Valid VREF voltage; 1h = Invalid VREF voltage
4	ADC_AIN1_FLT	R	0h	ADC AIN1 Fault. Maskable fault. 0h = AIN1 ADC measurement within threshold limits 1h = AIN1 ADC measurement outside threshold limits
3	ADC_AIN0_FLT	R	0h	ADC AIN0 Fault. Maskable fault. 0h = AIN0 ADC measurement within threshold limits 1h = AIN0 ADC measurement outside threshold limits
2	ADC_TEMP_FLT	R	0h	ADC Temp Fault. Maskable fault. 0h = TEMP ADC measurement within threshold limits 1h = TEMP ADC measurement outside threshold limits
1	THERM_ERR_FLT	R	0h	Temperature > 130°C error. Maskable fault. OR with FORCE_FAIL.THERM_ERR_FLT bit. Active signal, set as long as condition is true. Direct input from analog circuit. 0h = Temperature $\leq 130^\circ\text{C}$ ; 1h = Temperature > 130°C
0	THERM_WARN_FLT	R	0h	Temperature > 85°C warning. Maskable fault. OR with FORCE_FAIL.THERM_WARN_FLT bit. Active signal, set as long as condition is true. Direct input from analog circuit. 0h = Temperature $\leq 85^\circ\text{C}$ ; 1h = Temperature > 85°C

### 7.1.31 GEN\_STATUS Register (Offset = 21h) [Reset = 1180h]

Return to the [Register Map](#).

**表 7-33. GEN\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ALARM_IRQ	R	0h	Alarm IRQ OR of all the unmasked bits in the ALARM_STATUS register. 0h = All of the unmasked bits of the ALARM_STATUS register are low 1h = At least one of the unmasked bits in the ALARM_STATUS register is high
14	MODEM_IRQ	R	0h	Modem IRQ OR of all the unmasked bits in the MODEM_STATUS register. 0h = All of the unmasked bits of the MODEM_STATUS register are low 1h = At least one of the unmasked bits in the MODEM_STATUS register is high
13	RESERVED	R	0h	
12	OTP_BUSY	R	1h	OTP Busy Status = 1h at power up while the OTP is being loaded into the trim latches. 0h = OTP has completed loading into the device 1h = OTP is being loaded into the device
11	BIST_MODE	R	0h	Denotes which BIST is being run. 0h = MBIST; 1h = RBIST
10	BIST_DONE	R	0h	BIST Completed. Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = BIST has not completed; 1h = BIST has completed
9	BIST_FAIL	R	0h	BIST Failed. Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = BIST has passed; 1h = BIST has failed
8	RESET	R	1h	Device Reset Occurred. Status only. Does not feed IRQ. Sticky, cleared by reading register, unless condition still persist. 0h = Device has not reset since last read of register 1h = Device has reset since last read of register
7	SR_BUSYn	R	1h	Slew Rate Not Busy. Maskable fault. 0h = DAC is slewing to the target code 1h = DAC_OUT has reached the DAC_DATA. If slew rate is disabled, then this signal produces a rising edge within 3 internal clock cycles. If slew rate is enabled, this signal creates an IRQ event when the DAC_OUT has reached the DAC_DATA. At this time, slew rate can be safely disabled. If slew rate is disabled prior to DAC_OUT = DAC_DATA then a jump of DAC_OUT occurs. This can cause an unwanted fast transition on VOUT.
6	ADC_EOC	R	0h	ADC End of Conversion (EOC). Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = No EOC since last read of register; 1h = ADC end of conversion
5	ADC_BUSY	R	0h	ADC Busy. Status only. Does not feed IRQ. Active signal, set as long as condition is true. 0h = No ADC activity; 1h = ADC is actively converting
4	PVDD_HI	R	0h	PVDD High. Status only. Does not feed IRQ. Set as long as condition is true. 0h = PVDD < 2.7 V; 1h = PVDD ≥ 2.7 V
3	BREAK_FRAME_ERR	R	0h	Incorrect Stop Bit During Break Character. Maskable fault. Applies to UARTIN. Sticky, cleared by reading register, unless condition still persist. 0h = No break frame error; 1h = Break frame error
2	BREAK_PARITY_ERR	R	0h	Incorrect parity (ODD) bit during break character. Maskable fault. Applies to UARTIN. Sticky, cleared by reading register, unless condition still persist. 0h = No break parity error; 1h = Break parity error
1	UART_FRAME_ERR	R	0h	Incorrect Stop Bit During UART Character. Maskable fault. Applies to UARTIN. Sticky, cleared by reading register, unless condition still persist. 0h = No UART frame error; 1h = UART frame error
0	UART_PARITY_ERR	R	0h	Incorrect Parity (ODD) Bit During UART Character. Maskable fault. Applies to UARTIN. Sticky, cleared by reading register, unless condition still persist. 0h = No UART parity error; 1h = UART parity error

## 7.1.32 MODEM\_STATUS Register (Offset = 22h) [Reset = 009Ah]

Return to the [Register Map](#).

**表 7-34. MODEM\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ALARM_IRQ	R	0h	Alarm IRQ OR of all the unmasked bits in the ALARM_STATUS register. 0h = All of the unmasked bits of the ALARM_STATUS register are low 1h = At least one of the unmasked bits in the ALARM_STATUS register is high
14	GEN_IRQ	R	0h	General IRQ OR of all the unmasked bits in the GEN_STATUS register. 0h = All of the unmasked bits of the GEN_STATUS register are low 1h = At least one of the unmasked bits in the GEN_STATUS register is high
13	RESERVED	R	0h	
12	GAP_ERR	R	0h	HART Gap Error. Maskable fault. Applies to RX_IN/RX_INF. Too much time (11 bit times) between HART characters. Sticky, cleared by reading register, unless condition still persist. Fatal Fault. 0h = No HART gap error; 1h = HART gap error
11	FRAME_ERR	R	0h	Incorrect Stop Bit in HART Character. Maskable fault. Applies to RX_IN/RX_INF. Sticky, cleared by reading register, unless condition still persist. Fatal Fault. 0h = No HART frame error; 1h = HART frame error
10	PARITY_ERR	R	0h	Incorrect Parity (ODD) Bit in HART Character. Maskable fault. Applies to RX_IN/RX_INF. Sticky, cleared by reading register, unless condition still persist. 0h = No HART parity error; 1h = HART parity error
9	FIFO_H2U_LEVEL_FLAG	R	0h	FIFO HART-to-μC Level Flag. Maskable fault. If the level of the FIFO_H2U is full, then the level flag is not asserted, but the full flag is, so no information is lost. 0h = FIFO_H2U level ≤ {FIFO_CFG.H2U_LEVEL_SET[3:0], 1b1} 1h = FIFO_H2U level > {FIFO_CFG.H2U_LEVEL_SET[3:0], 1b1}
8	FIFO_H2U_FULL_FLAG	R	0h	FIFO HART-to-μC Full Flag. Maskable fault. 0h = FIFO_H2U is not full; 1h = FIFO_H2U is full
7	FIFO_H2U_EMPTY_FLAG	R	1h	FIFO HART-to-μC Empty Flag. Maskable fault. 0h = FIFO_H2U is not empty; 1h = FIFO_H2U is empty
6	FIFO_U2H_LEVEL_FLAG	R	0h	FIFO μC-to-HART Level Flag. Maskable fault. FIFO_U2H < {FIFO_CFG.U2H_LEVEL_SET[3:0], 1b0}. When the FIFO_U2H is empty, this flag is set unless FIFO_CFG.U2H_LEVEL_SET = 0. This flag and the empty flag can be set at the same time. 0h = FIFO_U2H level ≥ {FIFO_CFG.U2H_LEVEL_SET[3:0], 1b0} 1h = FIFO_U2H level < {FIFO_CFG.U2H_LEVEL_SET[3:0], 1b0}
5	FIFO_U2H_FULL_FLAG	R	0h	FIFO μC-to-HART Full Flag. Maskable fault. 0h = FIFO_U2H is not full; 1h = FIFO_U2H is full
4	FIFO_U2H_EMPTY_FLAG	R	1h	FIFO μC-to-HART Empty Flag. Maskable fault. 0h = FIFO_U2H is not empty; 1h = FIFO_U2H is empty
3	CD_DEASSERT	R	1h	Carrier Detect Deasserted. Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = Carrier detect is asserted; 1h = Carrier detect is deasserted
2	CD_ASSERT	R	0h	Carrier Detect Asserted. Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = Carrier detect is deasserted; 1h = Carrier detect is asserted
1	CTS_DEASSERT	R	1h	Clear To Send Deasserted. Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = Clear to send is asserted; 1h = Clear to send is deasserted
0	CTS_ASSERT	R	0h	Clear To Send Asserted. Maskable fault. Sticky, cleared by reading register, unless condition still persist. 0h = Clear to send is deasserted; 1h = Clear to send is asserted

### 7.1.33 ADC\_FLAGS Register (Offset = 23h) [Reset = 0000h]

Return to the [Register Map](#).

The limits for Self Diagnostic (SD) Alarm ADC Thresholds are shown in [表 6-5](#).

**表 7-35. ADC\_FLAGS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	
8	SD4_FAIL	R	0h	SD4 (VOUT) Limit Fail
7	SD3_FAIL	R	0h	SD3 (ZTAT) Limit Fail
6	SD2_FAIL	R	0h	SD2 (VDD) Limit Fail
5	SD1_FAIL	R	0h	SD1 (PVDD) Limit Fail
4	SD0_FAIL	R	0h	SD0 (VREF) Limit Fail
3	TEMP_FAIL	R	0h	TEMP Limit Fail
2	AIN1_FAIL	R	0h	AIN1 Limit Fail
1	AIN0_FAIL	R	0h	AIN0 Limit Fail
0	RESERVED	R	0h	

### 7.1.34 ADC\_AIN0 Register (Offset = 24h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-36. ADC\_AIN0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	
11-0	DATA	R	0h	Converted Value of Voltage on Pin AIN0

### 7.1.35 ADC\_AIN1 Register (Offset = 25h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-37. ADC\_AIN1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	
11-0	DATA	R	0h	Converted Value of Voltage on Pin AIN1

### 7.1.36 ADC\_TEMP Register (Offset = 26h) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-38. ADC\_TEMP Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	
11-0	DATA	R	0h	Converted Value of Temperature

### 7.1.37 ADC\_SD\_MUX Register (Offset = 27h) [Reset = 0000h]

Return to the [Register Map](#).

表 7-39. ADC\_SD\_MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	
11-0	DATA	R	0h	Converted Value of Voltage on Self-Diagnostic (SD) MUX Input

### 7.1.38 ADC\_OFFSET Register (Offset = 28h) [Reset = 0000h]

Return to the [Register Map](#).

表 7-40. ADC\_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	
11-0	DATA	R	0h	ADC Comparator Offset This value reports the offset measured in the device, and can be used to adjust each conversion value. If ADC_BYP.OFST_BYP_EN is set, then the value in ADC_BYP.DATA is used as the offset. This value is not affected by ADC_BYP.

### 7.1.39 FIFO\_H2U\_RD Register (Offset = 2Ah) [Reset = 0200h]

Return to the [Register Map](#).

表 7-41. FIFO\_H2U\_RD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	LEVEL	R	0h	Level Current Level of FIFO_H2U, bits [4:1] represented as Level[3:0]. Pre-dequeue.
11	LEVEL_FLAG	R	0h	HART-to-μC FIFO Level Flag Set when FIFO_H2U Level > {Level, 1b1}. Pre-dequeue. 0h = FIFO_H2U level ≤ {Level, 1b1} 1h = FIFO_H2U level > {Level, 1b1}
10	FULL_FLAG	R	0h	HART-to-μC FIFO Full Flag. Pre-dequeue. 0h = FIFO_H2U is not full, pre-dequeue 1h = FIFO_H2U is full, pre-dequeue
9	EMPTY_FLAG	R	1h	HART-to-μC FIFO Empty Flag. Pre-dequeue. 0h = FIFO_H2U is not empty 1h = FIFO_H2U is empty
8	PARITY	R	0h	Parity Bit (ODD) Parity bit received with data on HART. This field can only be read by SPI when CONFIG.UART_DIS = 1. Otherwise reads from this register are ignored and do not dequeue FIFO. The default value is unknown until data are written to the FIFO.
7-0	DATA	R	0h	Data 8-bit data received on HART. This field can only be read by SPI when CONFIG.UART_DIS = 1. Otherwise reads from this register are ignored and do not dequeue FIFO. The default value is unknown until data are written to the FIFO.

### 7.1.40 FIFO\_STATUS Register (Offset = 2Bh) [Reset = 0202h]

Return to the [Register Map](#).

The FIFO\_STATUS register is provided to allow the user to view the state of both FIFOs without enqueueing or dequeuing data in the FIFO. This also allows the flags to be viewed without disturbing other status bits in the MODEM\_STATUS register. This register is provided to enable users to check the FIFO status register without disturbing other functions within the device.

**表 7-42. FIFO\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	H2U_LEVEL	R	0h	HART-to-μC FIFO Level Current level of FIFO_H2U, right shifted 1 bit (>>1) so only even counts are represented.
11	H2U_LEVEL_FLAG	R	0h	HART-to-μC FIFO Level Flag Set when FIFO Level > {Level, 1b1}. 0h = FIFO_H2U level ≤ {Level, 1b1} 1h = FIFO_H2U level > {Level, 1b1}
10	H2U_FULL_FLAG	R	0h	HART-to-μC FIFO Full Flag Set when FIFO is full. 0h = FIFO_H2U is not full 1h = FIFO_H2U is full
9	H2U_EMPTY_FLAG	R	1h	HART-to-μC Empty Flag Set when FIFO is empty. 0h = FIFO_H2U is not empty 1h = FIFO_H2U is empty
8	RESERVED	R	0h	
7-4	U2H_LEVEL	R	0h	μC-to-HART FIFO Level Current level of FIFO_U2H, right shifted 1 bit (>>1) so only even counts are represented
3	U2H_LEVEL_FLAG	R	0h	μC-to-HART FIFO Level Flag Set when FIFO_U2H Level < {Level, 1b0}. 0h = FIFO_U2H level ≥ {Level, 1b0} 1h = FIFO_U2H level < {Level, 1b0}
2	U2H_FULL_FLAG	R	0h	μC-to-HART Full Flag Set when FIFO_U2H is full. 0h = FIFO_U2H is not full 1h = FIFO_U2H is full
1	U2H_EMPTY_FLAG	R	1h	μC-to-HART Empty Flag Set when FIFO_U2H is empty. 0h = FIFO_U2H is not empty 1h = FIFO_U2H is empty
0	RESERVED	R	0h	

### 7.1.41 DAC\_OUT Register (Offset = 2Ch) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-43. DAC\_OUT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	DATA	R	0h	DAC Code Applied to the Analog Circuit

## 7.1.42 ADC\_OUT Register (Offset = 2Dh) [Reset = 0000h]

Return to the [Register Map](#).

**表 7-44. ADC\_OUT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	
11-0	DATA	R	0h	ADC Data for Each Conversion Does not include ADC_OFFSET.DATA adjustment. Is not affected by ADC_BYP.DATA.

## 7.1.43 ADC\_BYP Register (Offset = 2Eh) [Reset = 0000h]

Return to the [Register Map](#).

ADC\_BYP is shown in [ADC\\_BYP Register Field Descriptions](#).

**表 7-45. ADC\_BYP Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	DATA_BYP_EN	R/W	0h	Data Bypass Enable Applies ADC_BYP.DATA to the ADC channel being converted. ADC_OFFSET is ignored. Do not set OFST_BYP_EN and DATA_BYP_EN at the same time. If OFST_BYP_EN is also set, DATA_BYP_EN takes priority over OFST_BYP_EN. After a channel is converted, the ADC_BYP.DATA value appears in the readback register for the converted channel and is used to calculate faults. 0h = Data bypass disabled (default) 1h = Data bypass enabled
14	OFST_BYP_EN	R/W	0h	Offset Bypass Enable Overrides the offset register with the ADC_BYP.DATA value. When using this bit, the ADC_BYP.DATA field is processed as 2's complement. Do not set OFST_BYP_EN and DATA_BYP_EN at the same time. 0h = Offset bypass disabled (default) 1h = Offset bypass enabled
13	DIS_GND_SAMP	R/W	0h	Disable GND Sampling This bit disables the sampling of GND during SAR activity. The sampling of GND is used to fully discharge the sampling CAP to reduce channel crosstalk. 0h = GND sampling enabled (default) 1h = GND sampling disabled
12	RESERVED	R	0h	
11-0	DATA	R/W	0h	Bypass Data



## 7.1.44 FORCE\_FAIL Register (Offset = 2Fh) [Reset = 0000h]

Return to the [Register Map](#).

Force failures for fault detection.

**表 7-46. FORCE\_FAIL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	CRC_FLT	R/W	0h	Force CRC Failure on SDO by Inverting the CRC Byte 0h = No force failure of CRC (default) 1h = Force failure of CRC
14	VREF_FLT	R/W	0h	Force Reference Voltage Failure. Analog signal. 0h = No force failure of VREF (default) 1h = Force failure of VREF
13	THERM_ERR_FLT	R/W	0h	Force Temperature > 130°C Thermal Error. Analog signal. 0h = No force temperature > 130°C error (default) 1h = Force temperature > 130°C error
12	THERM_WARN_FLT	R/W	0h	Force Temperature > 85°C thermal Warning. Analog signal. 0h = No force temperature > 85°C warning (default) 1h = Force temperature > 85°C warning
11-10	RESERVED	R/W	0h	
9	SD4_HI_FLT	R/W	0h	SD4 (VOUT) High Limit Failure. ADC measurement. 0h = No force failure of SD4 (VOUT) (default) 1h = Force failure of SD4 (VOUT)
8	SD4_LO_FLT	R/W	0h	SD4 (VOUT) Low limit failure. ADC measurement. 0h = No force failure of SD4 (VOUT) (default) 1h = Force failure of SD4 (VOUT)
7	SD3_HI_FLT	R/W	0h	SD3 (ZTAT) High Limit Failure. ADC measurement. 0h = No force failure of SD3 (ZTAT) (default) 1h = Force failure of SD3 (ZTAT)
6	SD3_LO_FLT	R/W	0h	SD3 (ZTAT) Low Limit Failure. ADC measurement. 0h = No force failure of SD3 (ZTAT) (default) 1h = Force failure of SD3 (ZTAT)
5	SD2_HI_FLT	R/W	0h	SD2 (VDD) High Limit Failure. ADC measurement. 0h = No force failure of SD2 (VDD) (default) 1h = Force failure of SD2 (VDD)
4	SD2_LO_FLT	R/W	0h	SD2 (VDD) Low Limit Failure. ADC measurement. 0h = No force failure of SD2 (VDD) (default) 1h = Force failure of SD2 (VDD)
3	SD1_HI_FLT	R/W	0h	SD1 (PVDD) High Limit Failure. ADC measurement. 0h = No force failure of SD1 (PVDD) (default) 1h = Force failure of SD1 (PVDD)
2	SD1_LO_FLT	R/W	0h	SD1 (PVDD) Low Limit Failure. ADC measurement. 0h = No force failure of SD1 (PVDD) (default) 1h = Force failure of SD1 (PVDD)
1	SD0_HI_FLT	R/W	0h	SD0 (VREF) High Limit Failure. ADC measurement. 0h = No force failure of SD0 (VREF) (default) 1h = Force failure of SD0 (VREF)
0	SD0_LO_FLT	R/W	0h	SD0 (VREF) Low Limit Failure. ADC measurement. 0h = No force failure of SD0 (VREF) (default) 1h = Force failure of SD0 (VREF)

#### 7.1.45 TIMER\_CFG\_0 Register (Offset = 3Bh) [Reset = 0000h]

Return to the [Register Map](#).

TIMER Configuration 0.

**表 7-47. TIMER CONFIG 0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	RESERVED	TO	0h	
3-2	CLK_SEL	R/W	0h	Clock Select Selects the timer clock frequency. 0h = None (default) 1h = 1.2288 MHz 2h = 1.200 kHz 3h = 1.171 Hz
1	INVERT	R/W	0h	Invert Output Invert the Timer output. By default, the output is set to 1 when the counter is $\geq$ SET_TIME (3Dh).
0	ENABLE	R/W	0h	Timer Enable The CLK_OUT pin must also be configured to output the Timer.

#### 7.1.46 TIMER\_CFG\_1 Register (Offset = 3Ch) [Reset = 0000h]

Return to the [Register Map](#).

TIMER Configuration 1.

**表 7-48. TIMER CONFIG 1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	PERIOD	R/W	0h	This field defines the period of the timer. The period is the product of (PERIOD + 1) and the clock period of CLK_SEL. For example, CLK_SEL = 2h (1200 Hz), The period is (PERIOD + 1) $\times$ 853 ms.

#### 7.1.47 TIMER\_CFG\_2 Register (Offset = 3Dh) [Reset = 0000h]

Return to the [Register Map](#).

TIMER Configuration 2.

**表 7-49. TIMER CONFIG 2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	SET_TIME	R/W	0h	The SET_TIME determine when the output of the timer goes high. The bits define the duty cycle of the timer (PERIOD – SET_TIME). The timer starts out as 0 and transitions to 1 when the SET_TIME is met. The polarity of the timer can be inverted using the TIMER_CFG_0.INVERT bit.

#### 7.1.48 CRC\_RD Register (Offset = 3Eh) [Reset = 0000h]

Return to the [Register Map](#).

CRC read.

**表 7-50. CRC Read Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	CRC	R/O	0h	Calculated CRC for RBIST or SHADOWLOAD. Final value is calculated internally. This value changes while RBIST or shadow load are running.

#### 7.1.49 RBIST\_CRC Register (Offset = 3Fh) [Reset = 0000h]

Return to the [Register Map](#).

RBIST CRC.

**表 7-51. RBIST CRC Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	RBIST CRC	R/W	0h	Calculated CRC for Register RBIST

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The AFEx82H1 are extremely low-power 16-bit and 14-bit voltage output DACs. The DACs support an output range of 0 V to 2.5 V. These devices have an onboard oscillator and an optional precision internal reference. This DAC is designed for analog voltage or current output modules. These devices also feature a SAR ADC that is used to measure internal and external nodes for making diagnostic measurements with fault detection and alarm actions. Use these diagnostic measurements together with the CRC and watchdog timer monitoring for device and system monitoring for functional safety.

The AFEx82H1 devices support modem functionality with the Highway Addressable Remote Transducer (HART) Protocol through SPI or UART communications. A HART interface is created through modulation and demodulation using the SPI or UART. Demodulate the input through band-pass filtering internal or external to the device.

The PVDD power supply has an operating range of 2.7 V to 5.5 V. The VDD is powered from an onboard LDO. Run the digital interface supply, IOVDD, from 1.71 V to 5.5 V.

#### 8.1.1 Multichannel Configuration

The integration of receive and transmit FIFOs for HART communication enables easy scalability in multichannel configurations using the SPI only interface. Because  $\overline{CS}$  low is required for communication and SDO can be set to a tri-state condition, only individual  $\overline{CS}$  signals are required from the microcontroller for all the AFEx82H1 devices in the system. The SDI, SDO, and SCLK signals can be combined. All the individual  $\overline{ALARM}$  pins can be wired-OR together. This minimizes the number of microcontroller GPIO signals required for communication, as well as the number of isolation channels for isolated systems. The multichannel configuration block diagram is shown in [図 8-1](#).

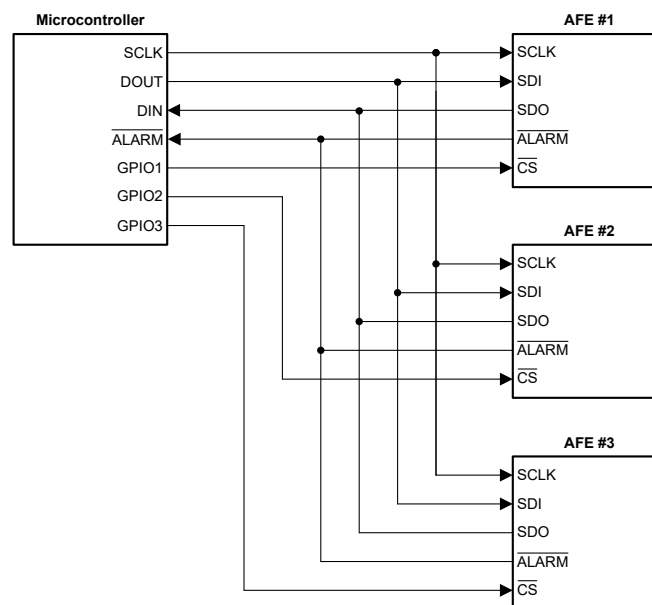


図 8-1. Multichannel Configuration

## 8.2 Typical Application

This design example shows a loop-powered, 4-mA to 20-mA field transmitter featuring the AFE882H1. The AFE782H1 can also be used in this design for lower-resolution applications.

This design example creates a simple HART-enabled loop controller that can be used for most field sensors in two-wire, current-loop applications. The design accepts bus voltages from 15 V to 36 V, while regulating the loop-current representation of a sensor to a post-calibration accuracy of less than 0.1% full-scale range (FSR) of total error at room temperature. The high integration in the system allows for a compact circuit, making this device an excellent choice for field transmitters where space is a concern. In field-transmitter applications, the current-loop transmitter, microcontroller, sensors, and analog front end are all required to consume less than the minimum bus current of 3 mA. Use an efficient low-power DC/DC converter instead of an LDO in the system to extend the current budget and allow more current for sensors and the AFE.

 **8-2** shows the schematic diagram for the loop-powered, 4-mA to 20-mA field transmitter.

[illegible]

### 8-2. AFEx82H1 in a 4-mA to 20-mA Current Transmitter

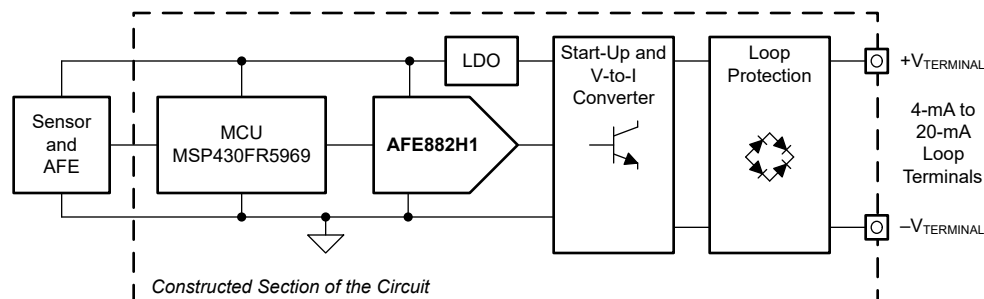
### 8.2.1.1 Design Requirements

The design requirements are:

- Transmitter with a current output range of 4 mA to 20 mA to represent a process variable signal
- Out-of-range current output capability below 3.6 mA and above 21 mA for NAMUR NE43 sensor fault signal levels
- Total on-board current less than or equal to 3 mA to operate the board, but allow for low out-of-range outputs
- Operation with standard industrial automation supply voltages from 15 V to 36 V
- Current and voltage outputs with TUE less than 0.5% at 25°C after calibration

### 8.2.1.2 Detailed Design Procedure

Figure 8-3 shows a block diagram of a loop-powered, 4-mA to 20-mA current transmitter.



**Figure 8-3. Block Diagram of a Loop-Powered, 4-mA to 20-mA Current Transmitter**

The terminals connected to the loop are shown on the right side of the block diagram. This connection to the loop powers the entire transmitter. A bridge rectifier at the input protects against reverse connection to the loop. The rectified loop voltage powers a start-up circuit that provides power to an LDO, that in turn powers the AFE882H1 and an MCU.

The AFE882H1 controls the loop current through the voltage-to-current (V-to-I) converter block. The DAC voltage sets the output from 0 V to 2.5 V. The output is sent through a V-to-I converter block using an OPA333 and an NPN bipolar junction transistor (BJT).

The HART signal is not received at the positive terminal of the 4-mA to 20-mA connections, but instead is received after the loop-protection rectifier. This HART signal input is capacitively coupled to this LOOP+ internal node of the circuit as shown in Figure 8-2. The HART signal output is modulated onto the loop current from the AFE882H1 through the V-to-I converter circuit.

### 8.2.1.2.1 Current Loop Control

The DAC of the AFE882H1 sets an output voltage from 0 V to 2.5 V. 図 8-4 shows the V-to-I circuit that sets the loop current from the DAC output voltage.

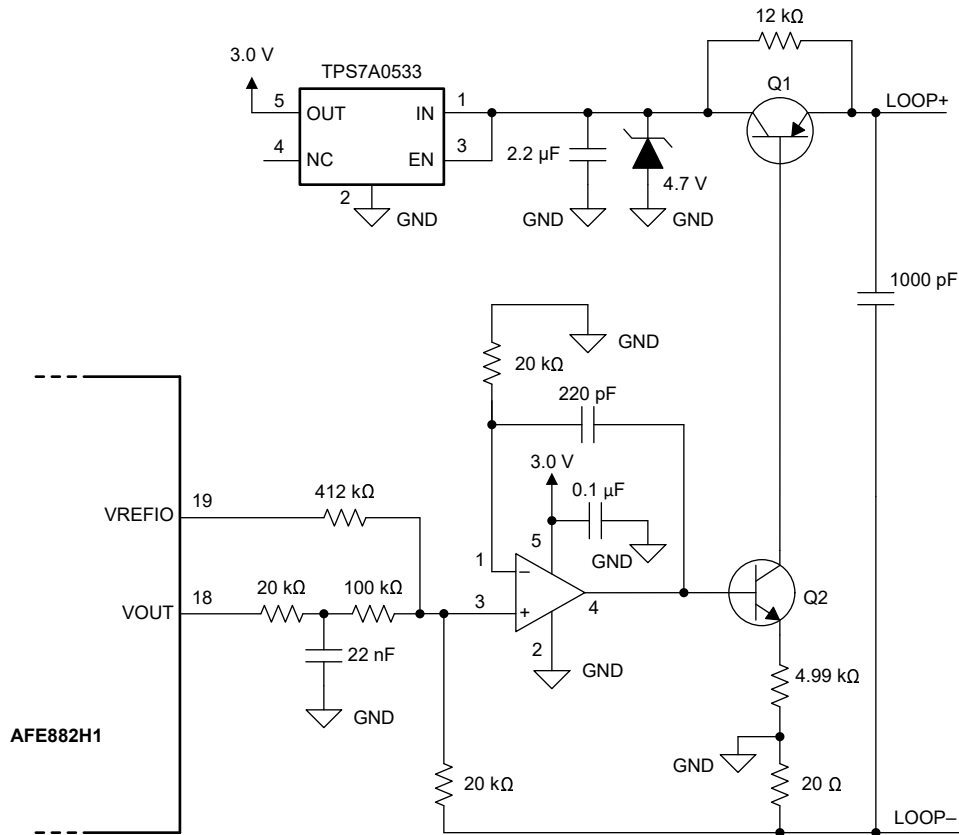


図 8-4. Current Loop Control for the AFE882H1 Transmitter

In this circuit, the loop current is set by the addition of the currents of V-to-I conversion from the output of VREFIO and the DAC VOUT. The current generated from these AFE882H1 outputs are analyzed separately.

First, the voltage from VREFIO is placed across a 412-kΩ resistor. This 1.25-V reference voltage creates a current that is directed into the summing node of an OPA333 amplifier that is set to ground. The voltage at LOOP- contributed from this current is calculated in 式 10.

$$V_{\text{LOOP-}} = \frac{-V_{\text{VREFIO}}}{412 \text{ k}\Omega} \times 20 \text{ k}\Omega = -1.25 \text{ V} \times 0.04854 = -0.06068 \text{ V} \quad (10)$$

From the feedback of the OPA333, the loop voltage from 式 10 is placed across the 20-Ω resistor and sets the current through the loop as 式 11 shows.

$$I_{\text{LOOP\_VREFIO}} = \left( \frac{-V_{\text{LOOP-}}}{20 \Omega} \right) + \left( \frac{-V_{\text{LOOP-}}}{20 \text{ k}\Omega} \right) = 0.06068 \text{ V} \times \left( \frac{1}{20 \Omega} + \frac{1}{20 \text{ k}\Omega} \right) = 3.037 \text{ mA} \quad (11)$$

This 3-mA current acts as a starting current for the loop. When the AFE882H1 DAC output is 0 V, this is the current on the loop.

In addition to this initial current, the AFE882H1 DAC output also controls the loop current. The VOUT voltage is set across 120 kΩ of resistance (from the 20 kΩ plus 100 kΩ of series resistance). The opposite end of the 120 kΩ of resistance is set to ground by the feedback of the OPA333. Similar to the calculations in 式 10 and 式 11, the voltage at VOUT sets a loop current, as 式 12 and 式 13 show.



$$V_{\text{LOOP-}} = \frac{-V_{\text{OUT}}}{120 \text{ k}\Omega} \times 20 \text{ k}\Omega = -V_{\text{OUT}} \times 0.1667 \quad (12)$$

$$I_{\text{LOOP\_VOUT}} = \left( \frac{-V_{\text{LOOP-}}}{20 \text{ }\Omega} \right) + \left( \frac{-V_{\text{LOOP-}}}{20 \text{ k}\Omega} \right) = V_{\text{OUT}} \times 0.1667 \times \left( \frac{1}{20 \text{ }\Omega} + \frac{1}{20 \text{ k}\Omega} \right) \quad (13)$$

When the DAC output voltage is set to 0 V, the contribution to the loop current is basically 0 mA. When the DAC output voltage is set to 2.5 V, the contribution to the loop current is 20.85 mA.

As mentioned previously, the total loop current is the sum of the contribution of the current created from the VREFIO voltage and the VOUT voltage. Using these voltages, the loop current has a range from 3.037 mA to 23.89 mA.

The AFE882H1 DAC output voltage is set through a 16-bit output code. Therefore, this final conversion from the DAC code to the loop current is set based on 式 14.

$$I_{\text{LOOP}} = I_{\text{LOOP\_VREFIO}} + I_{\text{LOOP\_VOUT}} = 3.037 \text{ mA} + \left( \text{DAC Code} \times \frac{20.85 \text{ mA}}{2^{16}} \right) \quad (14)$$

In 4-mA to 20-mA systems, the nominal output operates from 4 mA as the low output and 20 mA as the high output. However, systems sometimes use current outputs that are outside this range to indicate different error conditions. Loop currents of 3.375 mA and 21.75 mA are often used to indicate different loop errors. 表 8-1 shows different loop output currents, along with the DAC code and voltages used.

**表 8-1. DAC Voltage Output and Loop Current Based on DAC Output Codes**

OUTPUT CONDITION	DAC CODE	DAC OUTPUT (V)	LOOP CURRENT (mA)
DAC minimum	0x0000	0	3.037
Error low	0x0426	0.04051	3.375
In-range minimum	0x0BD2	0.1154	4
In-range midscale	0x6E07	1.0745	12
In-range maximum	0xD03C	2.0335	20
Error high	0xE5B7	2.2433	21.75
DAC maximum	0xFFFF	2.5	23.891

Among the passive devices included in the design, choose current-setting resistors with tight tolerances to achieve high accuracy and low drift. These resistors discussed in the previous equations are primarily responsible for setting the gain of the current loop, and therefore, the current magnitude of the loop.

### 8.2.1.2.2 HART Connections

Connections of the HART signal to the loop are done through the AFE882H1 MOD\_OUT and RX\_IN pins. Similar to converting the VOUT pin voltage to the loop current magnitude, the HART output from the MOD\_OUT pin is converted from a voltage to a current. A dc-blocking capacitor of 1000 pF is used to couple in the HART signal, without the dc output offset from the MOD\_OUT pin. From MOD\_OUT, the HART sinusoid nominal output is 500 mV<sub>PP</sub>. 式 15 shows that this V<sub>MOD</sub> HART sinusoid voltage is set across a 499-kΩ resistor to create signal voltage V<sub>LOOPAC</sub> superimposed onto V<sub>LOOP-</sub>.

$$V_{\text{LOOP\_AC}} = \frac{V_{\text{MOD}}}{499 \text{ k}\Omega} \times 20 \text{ k}\Omega = \frac{500 \text{ mV}_{\text{PP}}}{499 \text{ k}\Omega} \times 20 \text{ k}\Omega = 20.04 \text{ mV}_{\text{PP}} \quad (15)$$

The V<sub>LOOP\\_AC</sub> voltage sets the HART-modulated loop current that flows from ground to LOOP- through the 20-Ω resistor. This current is sourced from ground but controlled by the current sunk from Q4 coming from the start-up circuit. 式 16 calculates the total loop current based on the 20 mV<sub>PP</sub> of V<sub>LOOP\\_AC</sub>.

$$I_{\text{LOOP\_AC}} = V_{\text{LOOP\_AC}} \times \left( \frac{1}{20 \text{ }\Omega} + \frac{1}{20 \text{ k}\Omega} \right) = 1 \text{ mA}_{\text{PP}} \quad (16)$$

Using the 1000-pF capacitor as a dc-blocking capacitor and the 499-k $\Omega$  resistor, the 500-mV<sub>PP</sub> MOD\_OUT signal is converted to a 1-mA<sub>PP</sub> HART signal on the current loop.

HART signals are received by the AFE882H1 through the RX\_IN pin. A dc-blocking capacitor for the HART input at RX\_IN is shown with a series resistance of 1 k $\Omega$  in 図 8-2. A diode clamps the pin to the device supply and the resistance limits the input current. This configuration protects the RX\_IN from damage from an overvoltage event at the start up of the circuit.

#### 8.2.1.2.3 Input Protection and Rectification

図 8-5 shows the simple protection scheme implemented in the design to mitigate issues that arise from voltage and current transients on the bus. These transients have two main components: high-frequency and high-energy. These two components can be leveraged with a strategy of attenuation and diversion by the protection circuitry to deliver robust immunity.

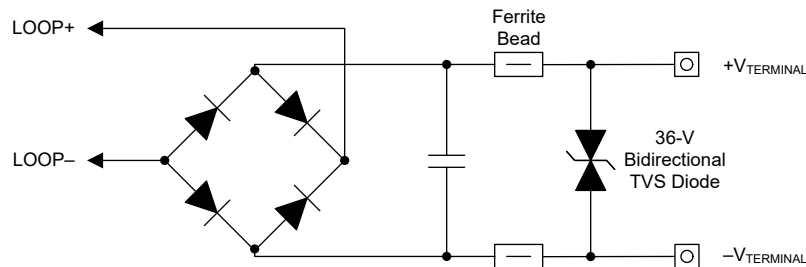


図 8-5. Loop Input Protection

Attenuation uses passive components, primarily resistors and capacitors, to attenuate high-frequency transients and to limit series current. Use ferrite beads to maintain dc accuracy while still delivering the ability to limit current from high-frequency transients. This circuit uses a capacitor placed across the input terminals, as well as ferrite beads in series with the terminals.

Diversion capitalizes on the high-voltage properties of the transient signals by using a diode to clamp the transient within supply voltages, or to divert the energy away from the system. Transient voltage suppressor (TVS) diodes help protect against transients because TVS diodes break down very quickly and often feature high power ratings that are critical to survive multiple transient strikes.

A rectifier is also implemented for reverse polarity protection so that the design can be connected to the bus regardless of the pin orientation or polarity without damage to the design.

#### 8.2.1.2.4 System Current Budget

Power consumption is an important consideration when designing two-wire transmitters. Power supplied from the loop must power all the circuitry related to the transmitter and sensor. The minimum loop current in two-wire applications is typically 4 mA. However, for error indications, this current is as low as 3.375 mA. Therefore, the power budget of all transducer circuitry is designed to be less than the maximum allowable system power budget of 3 mA. 表 8-2 lists the specified maximum quiescent current of all included active components (provided from the respective data sheets).

表 8-2. Typical Component Currents

DEVICE	DESCRIPTION	TYPICAL CURRENT ( $\mu$ A)
TPS7A0533	LDO	4
AFE882H1	16-bit DAC	180
OPA333 (2)	Operational amplifier	17 (each)
MSP430	Microcontroller	Dependent on firmware

### 8.2.1.3 Application Curves



図 8-6. DAC Code to Loop Current

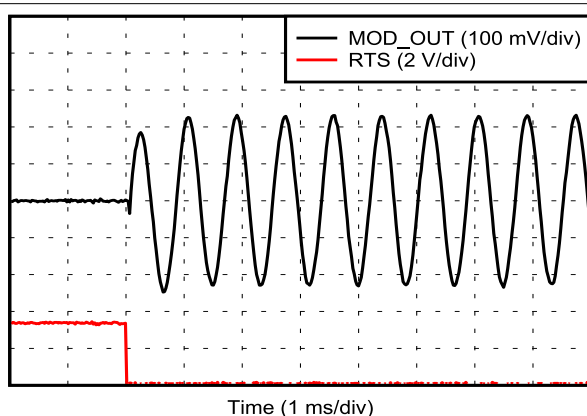


図 8-7.  $\overline{\text{RTS}}$  Start Timing

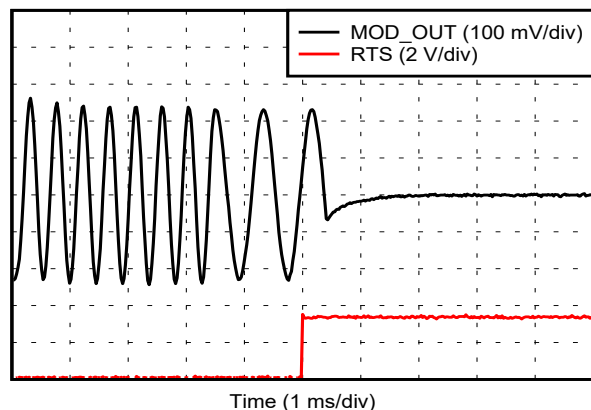


図 8-8.  $\overline{\text{RTS}}$  Stop Timing

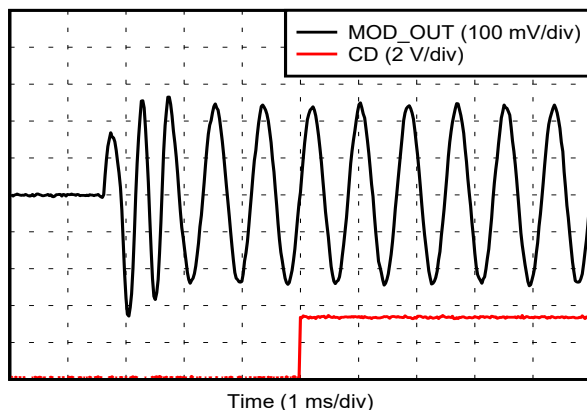


図 8-9. CD Start Timing

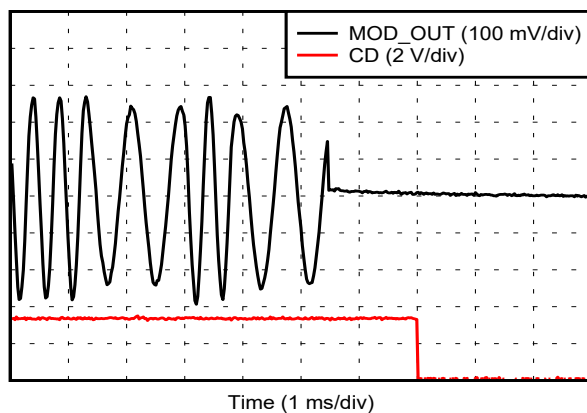


図 8-10. CD Stop Timing

## 8.3 Initialization Setup

This section describes several recommendations to set up the AFEx82H1.

The AFEx82H1 power up with the CRC enabled. If the device is intended to be run without the CRC, the CRC must be disabled by setting the CRC\_EN bit to 0h in the CONFIG register. Be aware that the command to write to this register is first done with the CRC enabled. The CRC byte must be appended to the command for the device to interpret the command correctly. To disable the CRC after start up, write 0x02 0x00 0x26 0x24 to the device. The first three bytes write the command, while the last byte is the CRC byte. For more information on the CRC, see the communication description in [セクション 6.5.3.3](#).

The AFEx82H1 also power up with the SDO pin disabled. The SDO pin is required for reading from any of the device registers, as well as reading any data from the ADC in SPI mode. The SDO pin is enabled by writing 0h into the DSDO bit in the CONFIG register. See also [セクション 6.5.3.1](#) and [セクション 6.5.3.2](#).

To enable the ADC, first enable the ADC buffer by writing 0h into the BUF\_PD bit in the ADC\_CFG register. For information about using the ADC in different modes of operation, see [セクション 6.3.2](#).

## 8.4 Power Supply Recommendations

The AFEx82H1 can operate within a single-supply range of 2.7 V to 5.5 V applied to the PVDD pin. When 2.7 V to 5.5 V is provided to PVDD, an internal LDO is enabled that drives VDD internally. VDD pin must have 1  $\mu$ F to 10  $\mu$ F of capacitance for operation.

The digital interface supply, IOVDD, can operate with a supply range of 1.71 V to 5.5 V.

Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage or current through various paths between the power connections and analog output. To further reduce noise, include bulk and local decoupling capacitors. The current consumption on the PVDD and IOVDD pins, the short-circuit current limit for the voltage output, and the current ranges for the current output are listed in the [Electrical Characteristics](#). The power supply must meet the requirements listed in the [Recommended Operating Conditions](#).

## 8.5 Layout

### 8.5.1 Layout Guidelines

To maximize the performance of the AFEx82H1 in any application, follow good layout practices and proper circuit design. The following recommendations are specific to the device:

- For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on restrictions imposed by specific end equipment, a dedicated ground plane is not always practical. If ground-plane separation is necessary, make a direct connection of the planes at the DAC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.
- IOVDD and PVDD must have 100-nF decoupling capacitors local to the respective pins. VDD must have at least a 1-μF decoupling capacitor used for the internal LDO. Use a high-quality ceramic-type NP0 or X7R capacitor for best performance across temperature and a very low dissipation factor.
- Place a 100-nF reference capacitor close to the VREFIO pin.
- Avoid routing switching signals near the reference input.
- Maintain proper placement for the digital and analog sections with respect to the digital and analog components. Separate the analog and digital circuitry for less coupling into neighboring blocks and to minimize the interaction between analog and digital return currents.
- For designs that include protection circuits:
  - Place diversion elements, such as TVS diodes or capacitors, close to off-board connectors to make sure that return current from high-energy transients does not cause damage to sensitive devices
  - Use large, wide traces to provide a low-impedance path to divert high-energy transients away from the I/O pins.

### 8.5.2 Layout Example

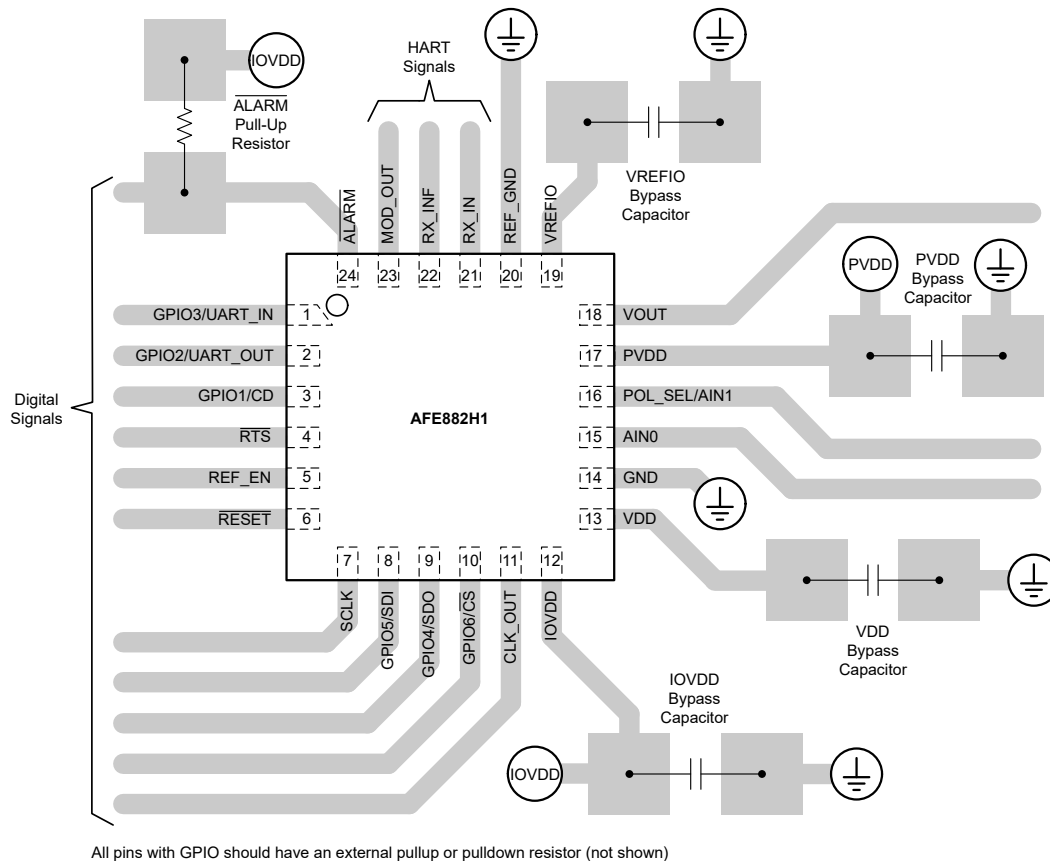


図 8-11. Layout Example

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [AFE882H1 Evaluation Module User's Guide](#)
- Texas Instruments, [REF35 Ultra Low-Power, High-Precision Voltage Reference data sheet](#)
- Texas Instruments, [XTR305 Industrial Analog Current or Voltage Output Driver data sheet](#)
- Texas Instruments, [ADS1220 4-Channel, 2-kSPS, Low-Power, 24-Bit ADC with Integrated PGA and Reference data sheet](#)
- Texas Instruments, [TPS7A16 60-V, 5- \$\mu\$ A IQ, 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good data sheet](#)
- Texas Instruments, [TPS7A02 Nanopower IQ, 25-nA, 200-mA, Low-Dropout Voltage Regulator With Fast Transient Response data sheet](#)
- Texas Instruments, [ISO7021 Ultra-Low Power Two-Channel Digital Isolator data sheet](#)
- Texas Instruments, [Isolated, Ultra-Low Power Design for 4- to 20-mA Loop Powered Transmitters design guide](#)
- Texas Instruments, [Isolated Loop Powered Thermocouple Transmitter design guide](#)
- Texas Instruments, [Small Form Factor, 2-Wire, 4- to 20-mA Current-Loop, RTD Temperature Transmitter design guide](#)
- Texas Instruments, [Isolated Power and Data Interface for Low-power Applications reference design](#)
- Texas Instruments, [Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications design guide](#)

#### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。  
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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#### 9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial release.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">AFE782H1RRUR</a>	Active	Production	UQFN (RRU)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	AFE 782H1
AFE782H1RRUR.A	Active	Production	UQFN (RRU)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	AFE 782H1
AFE782H1RRUT.A	Active	Production	UQFN (RRU)   24	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	AFE 782H1
<a href="#">AFE882H1RRUR</a>	Active	Production	UQFN (RRU)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	AFE 882H1
AFE882H1RRUR.A	Active	Production	UQFN (RRU)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	AFE 882H1
AFE882H1RRUT.A	Active	Production	UQFN (RRU)   24	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	AFE 882H1

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

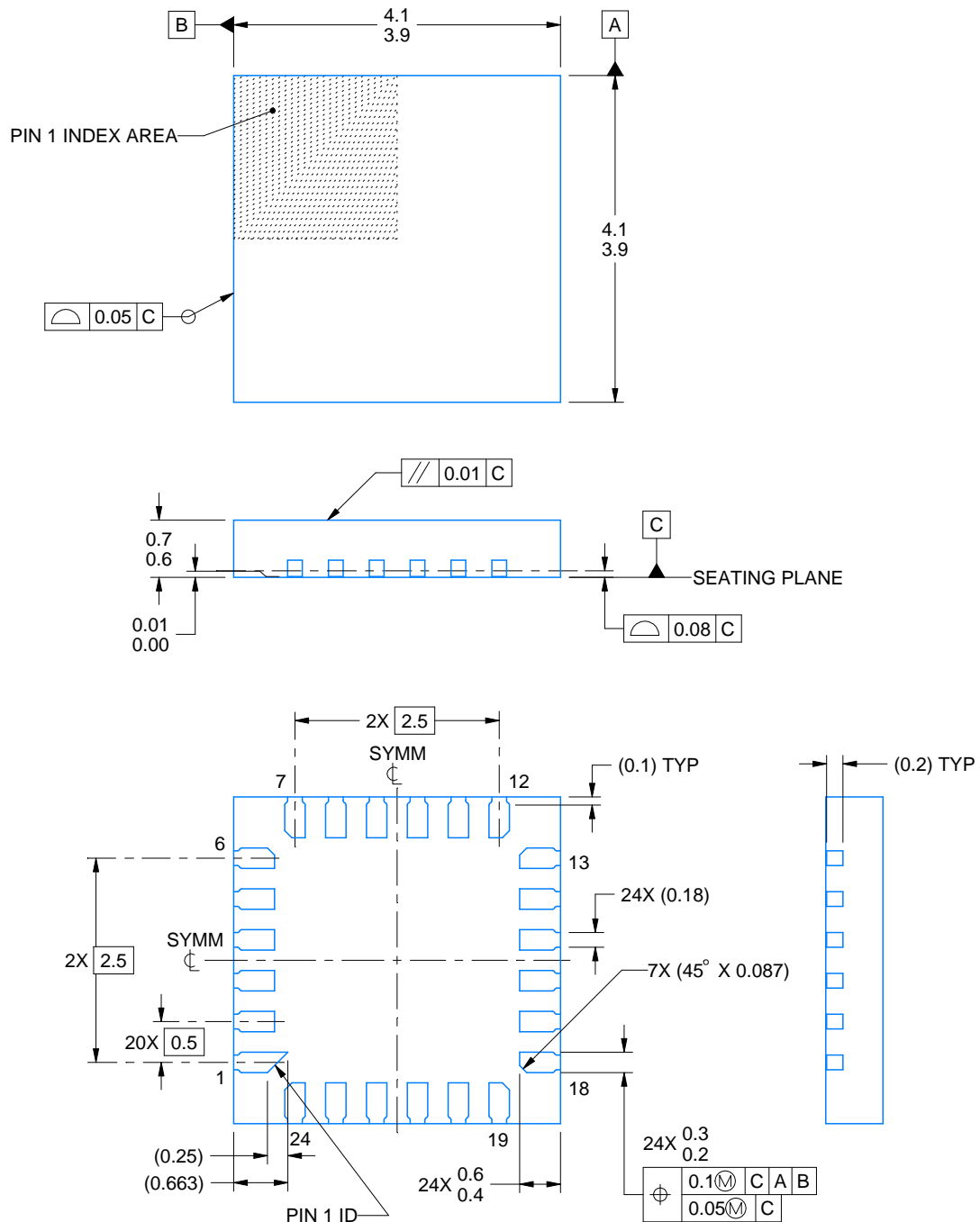
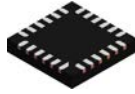
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



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## NOTES:

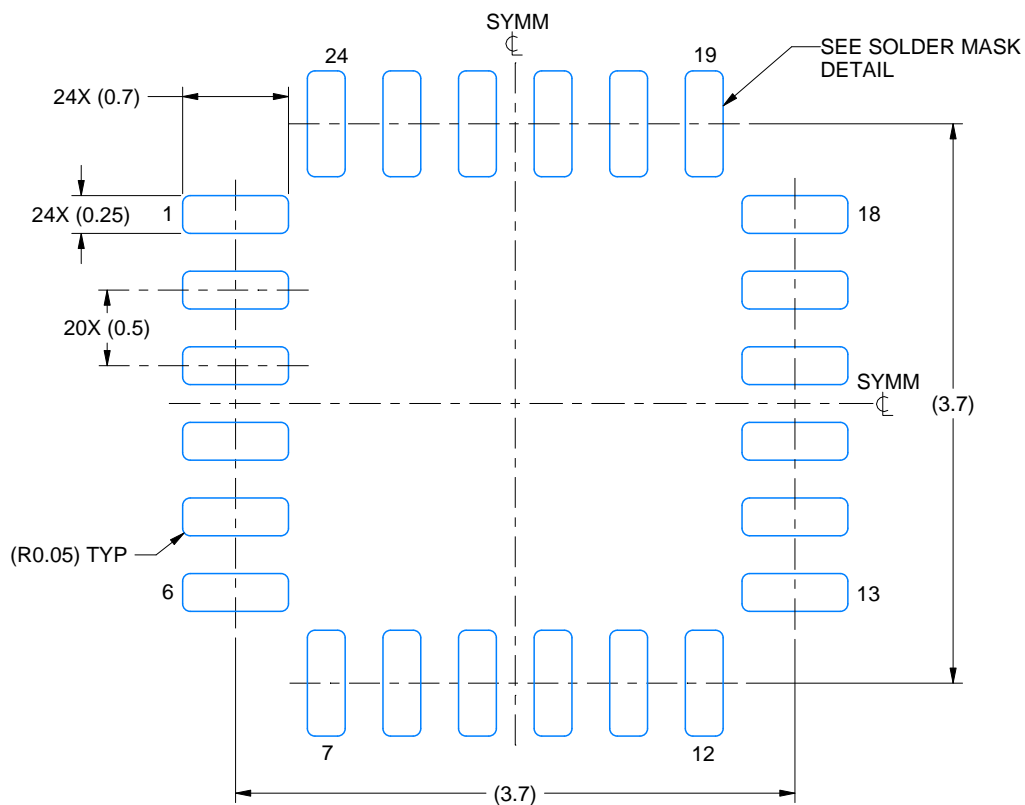
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

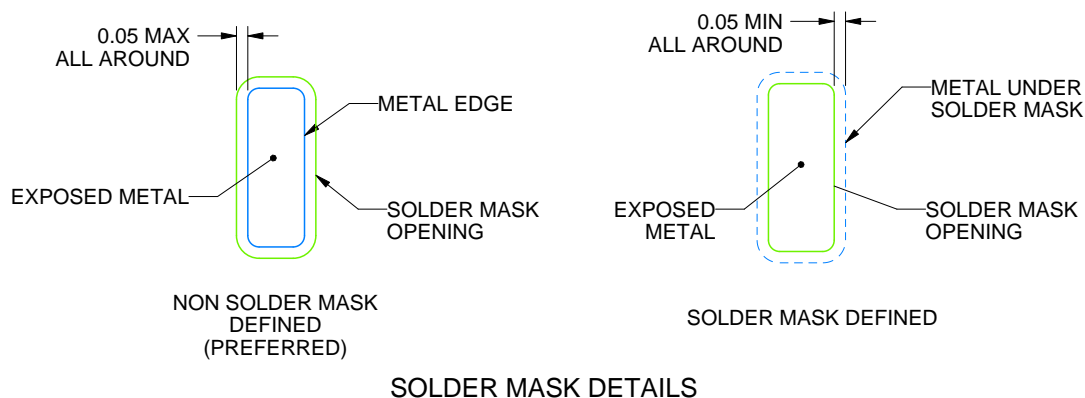
RRU0024A

UQFN - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



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NOTES: (continued)

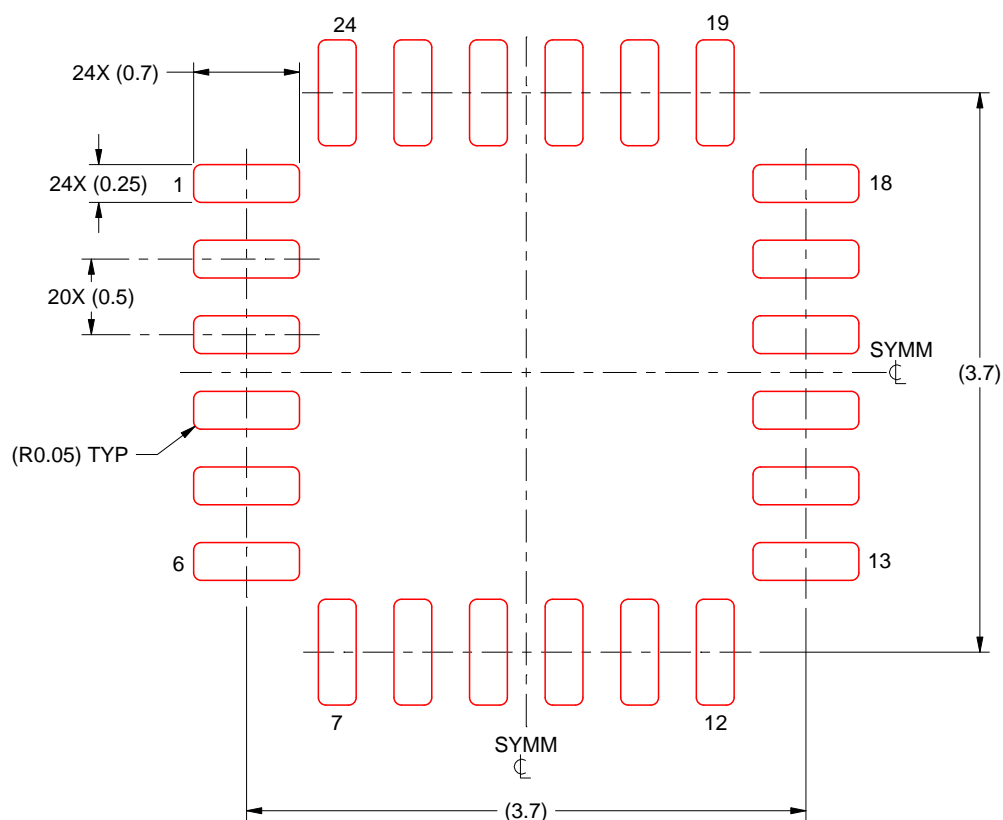
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RRU0024A

UQFN - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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