ADS8661W バイポーラ入力範囲をプログラム可能な 12 ビット、高速、単一電源 SAR (逐次比較型) ADC データ アクイジション システム

1 特長

- アナログ フロントエンド内蔵の 12 ビット ADC
- 高速度:1.25MSPS
- 入力範囲をソフトウェアでプログラム可能
  - バイポーラ差動範囲:±12.288V、±10.24V、±6.144V、±5.12V、±2.56V
  - ユニポーラ差動範囲:0V～12.288V、0V～10.24V、0V～6.144V、および 0V～5.12V
- アナログ電源 (5V):1.65V～5V の I/O 電源
- 1MΩ 以上の一定の抵抗性入力インピーダンス
- 入力帯域幅:450 kHz
- 入力過電圧保護:最大 ±20V
- オンチップの低ドリフト 4.096V 基準電圧
- 優れた性能
  - DNL:±0.1LSB、INL:±0.15LSB
  - 信号対雑音比:74dBFS、THD:-102dB
- 高 / 低スレッショルドのアラーム機能
- デイジー チェーン対応の multiSPI™ インターフェイス
- 拡張産業用温度範囲に対応:
  - -40℃ ～ +125℃

2 アプリケーション

- アナログ入力モジュール
- 半導体テスト
- サーボ ドライブ制御モジュール

3 概要

ADS8661W、、逐次比較型 (SAR) A/D コンバータ (ADC) トポロジを使った統合型データ アクイジション システム の製品です。これらのには、高速、高精度の SAR ADC と、統合型の差動アナログ フロントエンド (AFE) 入力ドライバ回路が搭載されています。ADS8661W には、最大 ±20V の過電圧保護回路と、温度ドリフトが非常に小さい 4.096V のオンチップ基準電圧が内蔵されています。

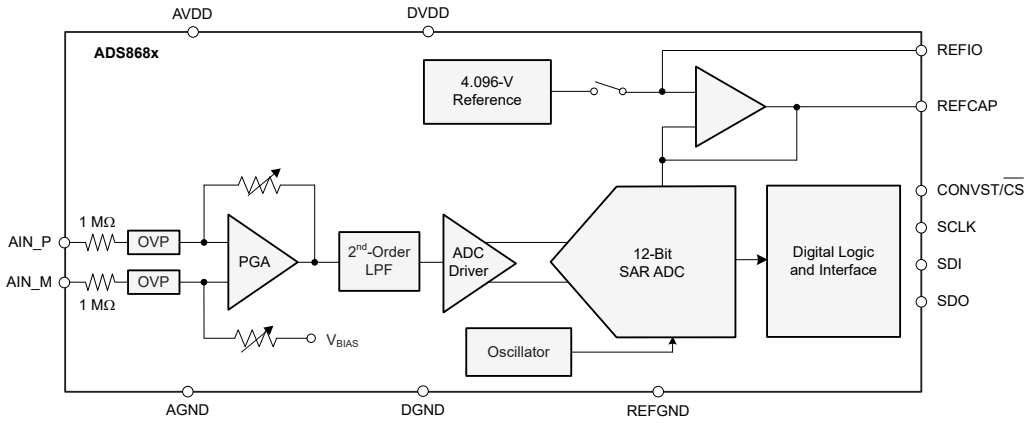
これらのは 5V の単一アナログ電源で動作しますが、真のバイポーラ入力範囲とユニポーラ入力範囲をサポートします。バイポーラ入力範囲は ±12.288V、±6.144V、±10.24V、±5.12V、±2.56V です。また、ユニポーラ入力範囲は 0V～12.288V、10.24V、6.144V、5.12V です。これらのデバイスは、選択した入力範囲にかかわらず、高い抵抗性入力インピーダンス (1MΩ 以上) を実現しています。

内蔵の multiSPI デジタル インターフェイスは、従来の SPI プロトコルと下位互換性があります。さらに、設定可能な機能により、広範なホスト コントローラとの接続が簡素化されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ADS8661W	RUM (WQFN、16)	4mm × 4mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



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4 Pin Configuration and Functions

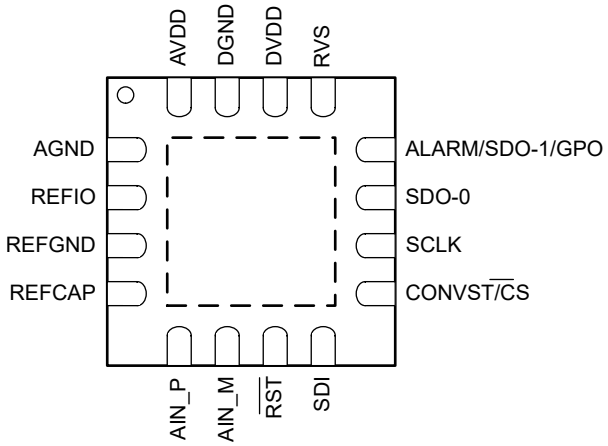


図 4-1. RUM Package, 16-Pin WQFN (Top View)

表 4-1. Pin Functions

NAME	NO.	TYPE(1)	DESCRIPTION
AGND	1	P	Analog ground pin. Decouple with the AVDD pin.
AIN_M	6	AI	Analog input: negative. Decouple with the AIN_P pin.
AIN_P	5	AI	Analog input: positive. Decouple with the AIN_M pin.
ALARM/SDO-1/GPO	12	DO	Multifunction output pin. Active high alarm. Data output 1 for serial communication. General-purpose output pin.
AVDD	16	P	Analog supply pin. Decouple with the AGND pin.
CONVST/$\overline{CS}$	9	DI	Dual-functionality pin. Active high logic: Conversion start input pin. A CONVST rising edge brings the device from acquisition phase to conversion phase. Active low logic: Chip-select input pin. The device takes control of the data bus when $\overline{CS}$ is low. The SDO-x pins go to tri-state when $\overline{CS}$ is high.
DGND	15	P	Digital ground pin. Decouple with the DVDD pin.
DVDD	14	P	Digital supply pin. Decouple with the DGND pin.
REFCAP	4	AO	ADC reference buffer decoupling capacitor pin. Decouple with the REFGND pin.
REFGND	3	P	Reference ground pin. Short this pin to the analog ground plane. Decouple with the REFIO and REFCAP pins.
REFIO	2	AIO	Internal reference output and external reference input pin. Decouple with REFGND.
$\overline{RST}$	7	DI	Active-low logic input to reset the device.
RVS	13	DO	Multifunction output pin for serial interface, see the *RESET State* section. With $\overline{CS}$ held high, RVS reflects the status of the internal ADCST signal. With $\overline{CS}$ low, the status of RVS depends on the output protocol selection.
SCLK	10	DI	Serial communication: Clock input pin for the serial interface. All system-synchronous data transfer protocols are timed with respect to the SCLK signal.
SDI	8	DI	Dual function: Data input pin for serial communication. Chain data input during serial communication in daisy-chain mode.
SDO-0	11	DO	Serial communication: Data output 0.

(1) AI = analog input, AIO = analog input/output, DI = digital input, DO = digital output, and P = power supply.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AIN_P, AIN_M to GND	AVDD = 5V	–20	20	V
	AVDD = Unpowered	–15	15	
AVDD to GND or DVDD to GND		–0.3	7	V
REFCAP to REFGND or REFIO to REFGND		–0.3	5.7	V
GND to REFGND		–0.3	0.3	V
Digital input pins to GND		–0.3	DVDD + 0.3	V
Digital output pins to GND		–0.3	DVDD + 0.3	V
Input current to any pin except supply pins		–10	10	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, analog input pins (AIN_P, AIN_M)(1)	±4000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±2000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog power supply	AVDD to GND	4.75	5	5.25	V
DVDD	Digital interface power supply	DVDD to GND	1.65	3.3	AVDD	V
REFERENCE VOLTAGE						
V_{REFIO_EXT}	External reference voltage on REFIO	REFIO pin configured as an input	4.046	4.096	4.146	V
ANALOG INPUTS						
AIN_x	Full-scale input span (AIN_P to AIN_M)	Input range = ±3 x V_{REF}	–12.288		12.288	V
		Input range = ±2.5 x V_{REF}	–10.24		10.24	
		Input range = ±1.5 x V_{REF}	–6.144		6.144	
		Input range = ±1.25 x V_{REF}	–5.12		5.12	
		Input range = ±0.625 x V_{REF}	–2.56		2.56	
		Input range = 3 x V_{REF}	0		12.288	
		Input range = 2.5 x V_{REF}	0		10.24	
		Input range = 1.5 x V_{REF}	0		6.144	
		Input range = 1.25 x V_{REF}	0		5.12	
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		ADS8661W RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5V, DVDD = 3.3V, VREF = 4.096V (internal), and maximum throughput (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{IN}	Full-scale input span (AIN_P to AIN_M)	Input range = ±3 x V_{REF}	–12.288		12.288	V
		Input range = ±2.5 x V_{REF}	–10.24		10.24	V
		Input range = ±1.5 x V_{REF}	–6.144		6.144	V
		Input range = ±1.25 x V_{REF}	–5.12		5.12	V
		Input range = ±0.625 x V_{REF}	–2.56		2.56	V
		Input range = 3 x V_{REF}	0		12.288	V
		Input range = 2.5 x V_{REF}	0		10.24	V
		Input range = 1.5 x V_{REF}	0		6.144	V
		Input range = 1.25 x V_{REF}	0		5.12	V
AIN_x	Full-scale input span (AIN_P to AIN_M)	Input range = ±3 x V_{REF}	–12.288		12.288	V
		Input range = ±2.5 x V_{REF}	–10.24		10.24	V
		Input range = ±1.5 x V_{REF}	–6.144		6.144	V
		Input range = ±1.25 x V_{REF}	–5.12		5.12	V
		Input range = ±0.625 x V_{REF}	–2.56		2.56	V
		Input range = 3 x V_{REF}	0		12.288	V
		Input range = 2.5 x V_{REF}	0		10.24	V
		Input range = 1.5 x V_{REF}	0		6.144	V
		Input range = 1.25 x V_{REF}	0		5.12	V
R_{IN}	Input impedance	Input range = ±3 x V_{REF} at T_A = 25℃	1.02	1.2	1.38	V
		Input range = ±2.5 x V_{REF} at T_A = 25℃	0.85	1	1.15	V
		Input range = ±1.5 x V_{REF} at T_A = 25℃	1.02	1.2	1.38	V
		Input range = ±1.25 x V_{REF} at T_A = 25℃	0.85	1	1.15	V
		Input range = ±0.625 x V_{REF} at T_A = 25℃	0.85	1	1.15	V
		Input range = 3 x V_{REF} at T_A = 25℃	1.02	1.2	1.38	V
		Input range = 2.5 x V_{REF} at T_A = 25℃	0.85	1	1.15	V
		Input range = 1.5 x V_{REF} at T_A = 25℃	1.02	1.2	1.38	V
		Input range = 1.25 x V_{REF} at T_A = 25℃	0.85	1	1.15	V
I_{IN}	Input current	All input ranges		(V_{IN} – 2.5) / R_{IN}		µA
INPUT OVERVOLTAGE PROTECTION CIRCUIT						
V_{OVP}	All input ranges	AVDD = 5V, all input ranges	–20		20	V
		AVDD = floating, all input ranges	–15		15	V
INPUT BANDWIDTH						
$f_{-3\ dB}$	Small-signal Input bandwidth	–3dB all input ranges		500		kHz
$f_{-0.1\ dB}$	Small-signal Input bandwidth	–0.1dB all input ranges		75		kHz

5.5 Electrical Characteristics (続き)

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5V, DVDD = 3.3V, VREF = 4.096V (internal), and maximum throughput (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
	Resolution		12			Bits
NMC	No missing codes		12			Bits
DNL	Differential nonlinearity	All input ranges	–0.5	±0.1	0.5	LSB
INL	Integral nonlinearity	All input ranges	–0.5	±0.15	0.5	LSB
E_O	Offset error	All bipolar ranges at T_A = 25°C	–1	±0.2	1	mV
		All unipolar ranges at T_A = 25°C	–2	±0.2	2	
	Offset error drift with temperature	All input ranges	–3	±0.75	3	ppm/°C
E_G	Gain error	All input ranges at T_A = 25°C	–0.038	±0.01	0.038	%FSR
	Gain error drift with temperature	All input ranges	–5	±1	5	ppm/°C
AC PERFORMANCE						
SNR	Signal-to-noise ratio	All input ranges	71.5	72.4		dBFS
THD	Total harmonic distortion	All input ranges		–102		dB
SINAD	Signal-to-noise + distortion	All input ranges	71.4	72.3		dB
SFDR	Spurious-free dynamic range	All input ranges		103		dB
INTERNAL REFERENCE OUTPUT						
V_{REFIO}	On the REFIO pin (configured as an output)	WQFN (RUM) at T_A = 25°C	4.094	4.096	4.098	V
dV_{REFIO}/dT_A	Internal reference temperature drift	WQFN (RUM) at T_A = 25°C		5		ppm/°C
COUT_REFIO	Decoupling capacitor on REFIO pin		4.7			µF
VREFCAP	Reference voltage to the ADC (on the REFCAP pin)		4.0945	4.096	4.0975	V
	REFCAP temperature drift			0.5	2	ppm/°C
COUT_REFCAP	Decoupling capacitor on REFCAP pin		10			µF
	Turn-on time	C_{OUT_REFCAP} = 10µF, C_{OUT_REFIO} = 10µF		20		ms
EXTERNAL REFERENCE INPUT						
V_{REFIO_EXT}	External reference voltage on REFIO	REFIO pin configured as an input	4.046	4.096	4.146	
AVDD COMPARATOR						
V_{TH_HIGH}	High threshold voltage			5.3		V
V_{TH_LOW}	Low threshold voltage			4.7		V
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog power-supply voltage	Operating range	4.75	5	5.25	V
DVDD	Digital power-supply voltage	Operating range	1.65	3.3	AVDD	V
		Supply range for specified performance	2.7	3.3	AVDD	V
I_{AVDD_DYN}	Analog supply current, device converting at maximum throughput	Internal reference		7	9	mA
		External reference		5.8	7.25	
I_{AVDD_STC}	Analog supply current, device not converting	Internal reference		4.7	6.25	mA
		External reference		2.9	4	
I_{AVDD_STDBY}	Analog supply current, device in STANDBY mode	Internal reference		2.8		mA
		External reference		1.6		

5.5 Electrical Characteristics (続き)

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5V, DVDD = 3.3V, VREF = 4.096V (internal), and maximum throughput (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{AVDD_PD}	Analog supply current, device in PD mode	Internal reference		10		µA
		Enternal reference		10		
I_{DVDD_DYN}	Digital supply current, maximum throughput			0.2	0.25	mA
I_{DVDD_STDBY}	Digital supply current, device in STANDBY mode			1		µA
I_{DVDD_PD}	Digital supply current, device in PD mode			1		µA
DIGITAL INPUTS (CMOS)						
V_{IH}	Digital high input voltage logic level	DVDD > 2.35V	0.7 × DVDD		DVDD + 0.3	V
		DVDD ≤ 2.35V	0.8 × DVDD		DVDD + 0.3	V
V_{IL}		DVDD > 2.35V	–0.3		0.3 x DVDD	V
		DVDD ≤ 2.35V	–0.3		0.2 x DVDD	V
	Input leakage current			100		nA
	Input pin capacitance			5		pF
DIGITAL OUTPUTS (CMOS)						
V_{OH}	Digital high output voltage logic level	I_O = 500µA source	0.8 × DVDD		DVDD	V
V_{OL}	Digital low output voltage logic level	I_O = 500µA sink	0		0.2 × DVDD	V
	Floating state leakage current	Only for digital output pins		1		µA
	Internal pin capacitance			5		pF

5.6 Timing Requirements

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5V, DVDD = 3.3V, VREF = 4.096V (internal), and maximum throughput (unless otherwise noted)

		MIN	TYP	MAX	UNIT
CONVERSION CYCLE					
f_{cycle}	Sampling frequency			1250	kSPS
t_{cycle}	ADC cycle time period	1 / f_{cycle}			s
t_{acq}	Acquisition time	250			ns
ASYNCHRONOUS RESET					
t_{wl_RST}	Pulse duration: $\overline{RST}$ low	100			ns
SPI-COMPATIBLE SERIAL INTERFACE					
f_{CLK}	Serial clock frequency			66.67	MHz
t_{CLK}	Serial clock time period	1/f_{CLK}			
t_{PH_CK}	SCLK high time	0.45		0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{CLK}
t_{SU_CSCK}	Setup time: CONVST/$\overline{CS}$ falling to first SCLK capture edge	7.5			ns
t_{SU_CKDI}	Setup time: SDI data valid to SCLK capture edge	7.5			ns
t_{HT_CKDI}	Hold time: SCLK capture edge to (previous) data valid on SDI	7.5			ns
SOURCE-SYNCHRONOUS SERIAL INTERFACE (EXTERNAL CLOCK)					
f_{CLK}	Serial clock frequency			66.67	MHz
t_{CLK}	Serial clock time period	1/f_{CLK}			
t_{PH_CK}	SCLK high time	0.45		0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{CLK}

5.7 Switching Characteristics

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5V, DVDD = 3.3V, VREF = 4.096V (internal), and maximum throughput (unless otherwise noted)

		MIN	TYP	MAX	UNIT
ASYNCHRONOUS RESET					
t_{conv}	Conversion time			550	ns
$t_{D\_RST\_POR}$	Delay time for POR reset: RST rising to RVS rising		20		ms
$t_{D\_RST\_APP}$	Delay time for application reset: $\overline{RST}$ rising to CONVST/$\overline{CS}$ rising			1	µs
t_{NAP_WKUP}	Wake-up time: NAP mode			20	µs
t_{PWRUP}	Power-up time: PD mode		20		ms
SPI-COMPATIBLE SERIAL INTERFACE					
t_{HT_CKCS}	Delay time: last SCLK capture edge to CONVST/$\overline{CS}$ rising	7.5			ns
t_{DEN_CSDO}	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to 3-state			10	ns
t_{D_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO-x			12	ns
t_{D_CSRVS}	Delay time: CONVST/CS rising edge to RVS falling			14	ns
SOURCE-SYNCHRONOUS SERIAL INTERFACE (EXTERNAL CLOCK)					
	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to tri-state			10	ns
	Delay time: SCLK rising edge to RVS rising			14	ns
	Delay time: SCLK falling edge to RVS falling			14	ns
	Delay time: RVS rising to (next) data valid on SDO-x			2.5	ns
	Delay time: CONVST/$\overline{CS}$ rising edge to RVS displaying internal device state			15	ns
SOURCE-SYNCHRONOUS SERIAL INTERFACE (INTERNAL CLOCK)					
t_{DEN_CSDO}	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to tri-state			10	ns
t_{DEN_CSRVS}	Delay time: CONVST/$\overline{CS}$ falling edge to first rising edge on RVS			50	ns
t_{D_RVSDO}	Delay time: RVS rising to (next) data valid on SDO-x			2.5	ns
t_{INTCLK}	Time period: internal clock	15			ns
t_{CYC_RVS}	Time period: RVS signal	15			ns
t_{WH_RVS}	RVS high time	0.4		0.6	t_{INTCLK}
t_{WL_RVS}	RVS low time	0.4		0.6	t_{INTCLK}
t_{D_CSRVS}	Delay time: CONVST/$\overline{CS}$ rising edge to RVS displaying internal device state			15	ns

5.8 Timing Diagrams

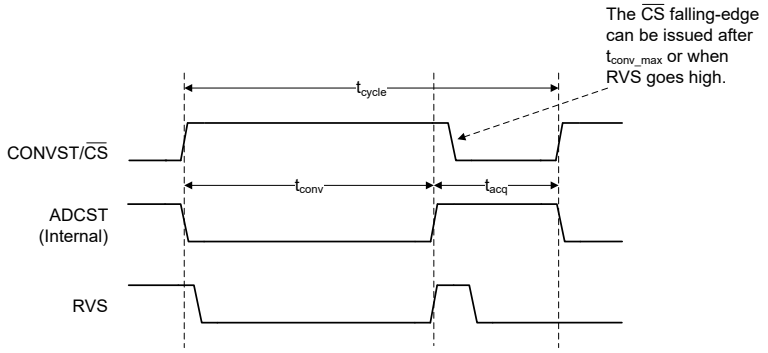


図 5-1. Conversion Cycle Timing Diagram

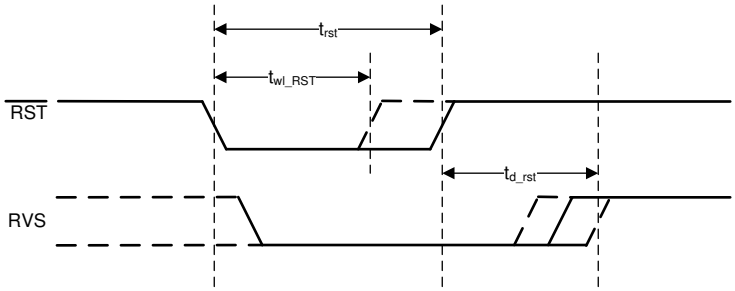


図 5-2. Asynchronous Reset Timing Diagram

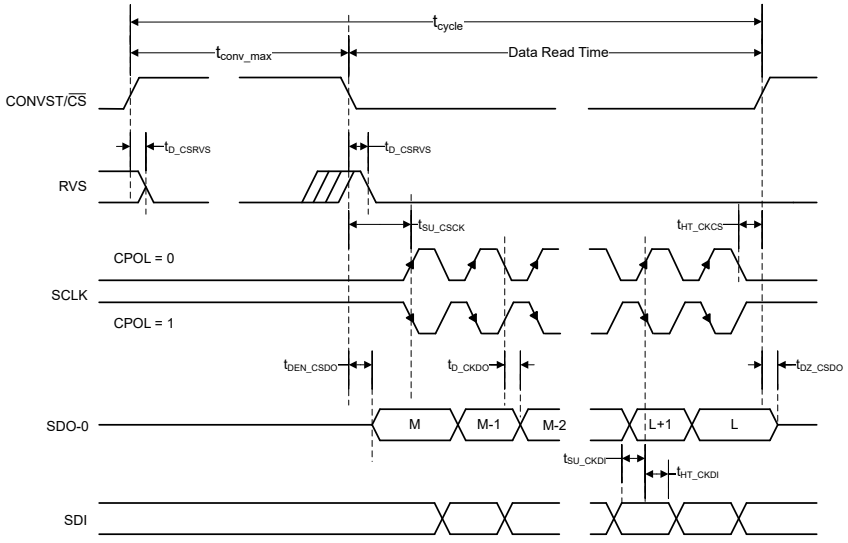


図 5-3. Standard SPI Interface Timing Diagram for CPHA = 0

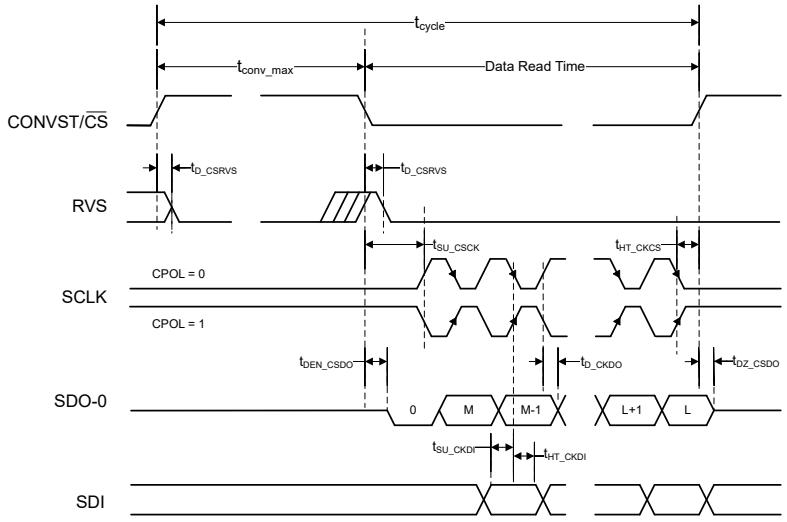


図 5-4. Standard SPI Interface Timing Diagram for CPHA = 1

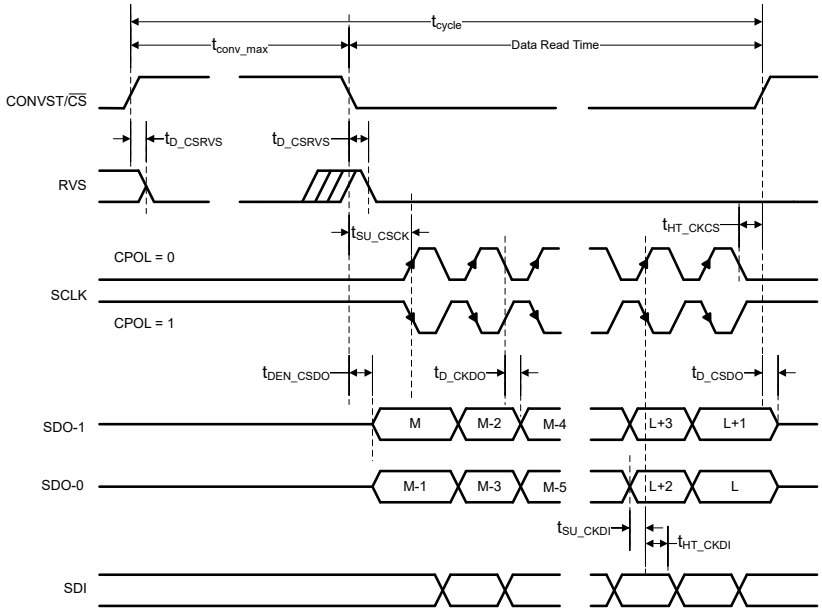


図 5-5. multiSPI Interface Timing Diagram for Dual SDO-x and CPHA = 0

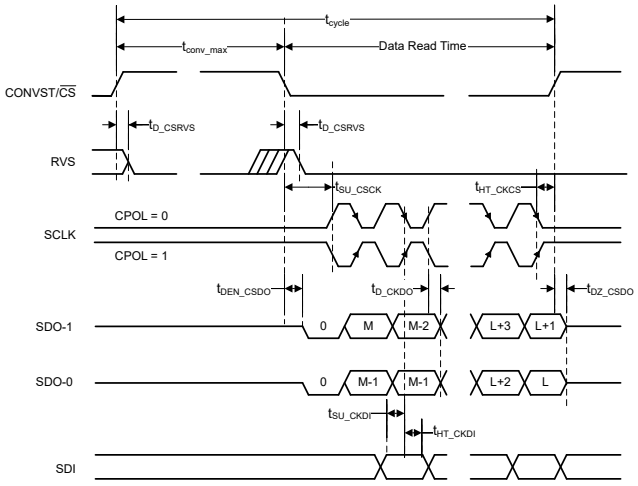


図 5-6. multiSPI Interface Timing Diagram for Dual SDO-x and CPHA = 1

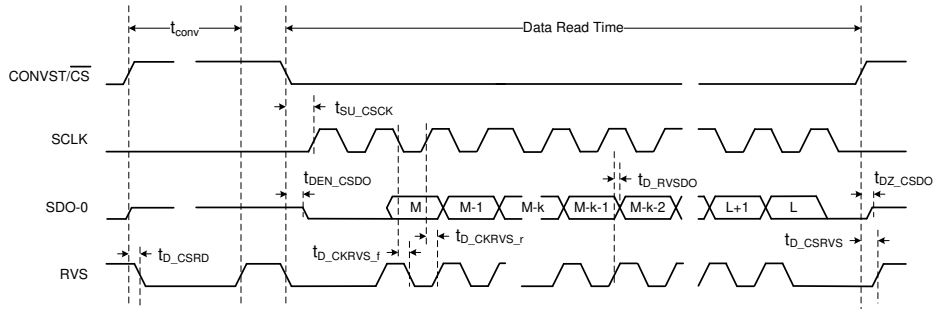


図 5-7. multiSPI Source-Synchronous External Clock Serial Interface Timing Diagram

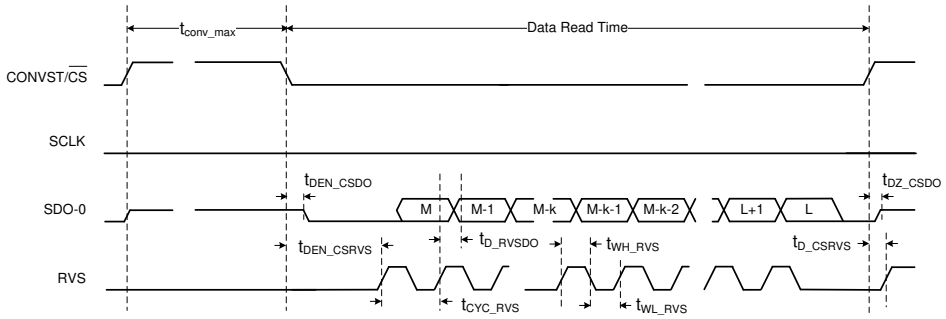


図 5-8. multiSPI Source-Synchronous Internal Clock Serial Interface Timing Diagram

5.9 Typical Characteristics

at T_A = 25°C, AVDD = 5V, DVDD = 3V, V_{REF} = 4.096V (internal), and maximum throughput (unless otherwise noted)

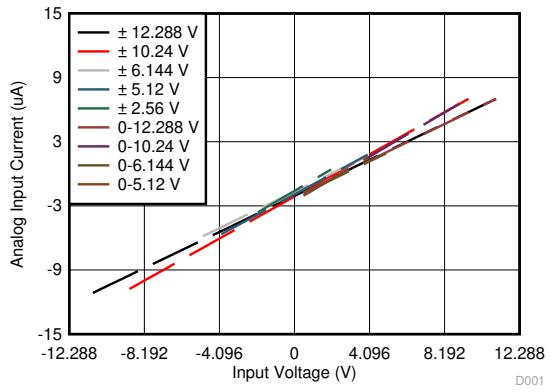
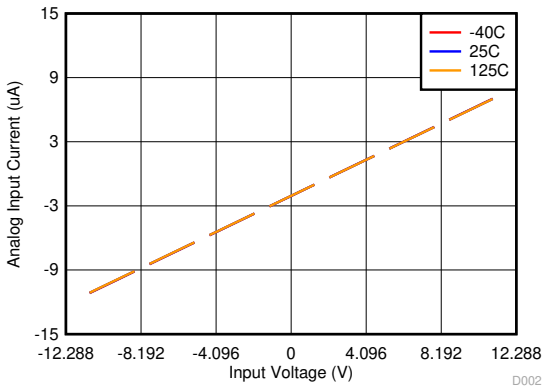


図 5-9. Input I-V Characteristic Across Input Ranges



Range = ±12.288V

図 5-10. Input I-V Characteristic Across Temperature

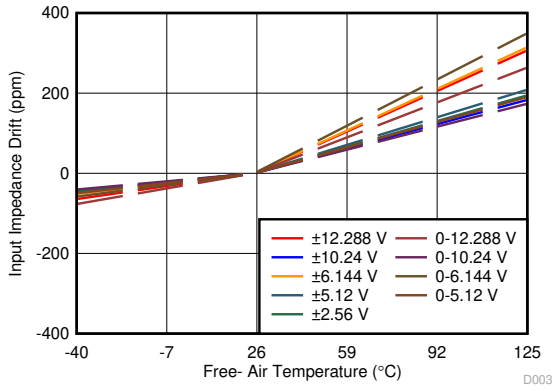
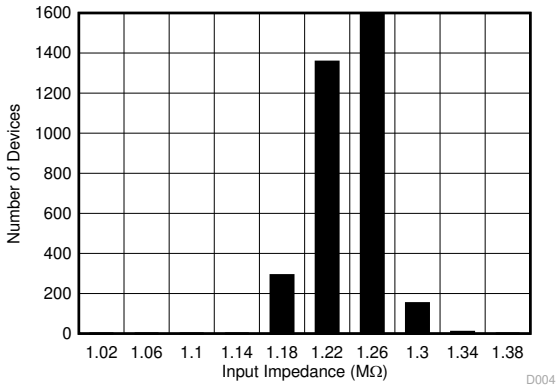
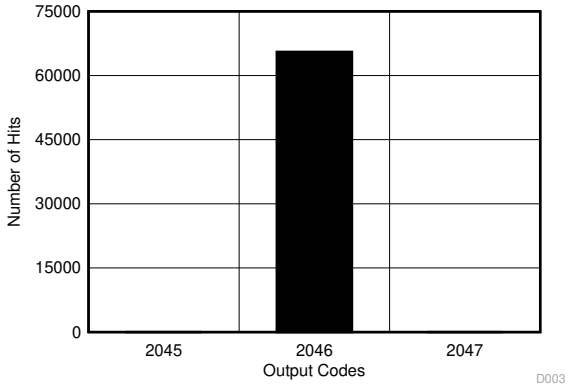


図 5-11. Input Impedance Drift vs Temperature



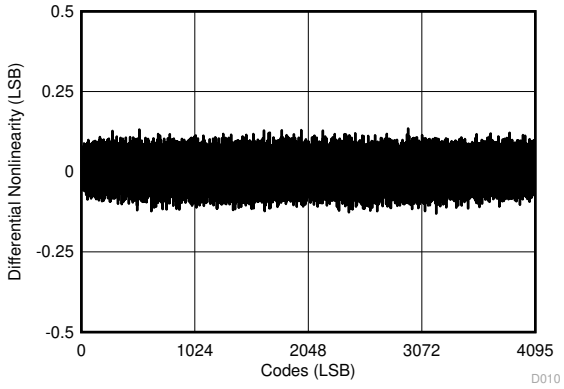
Number of samples = 3398

図 5-12. Typical Distribution of Input Impedance



Mean = 2046, sigma = 0, input = midscale

図 5-13. DC Histogram for Midscale Inputs For All Input Ranges

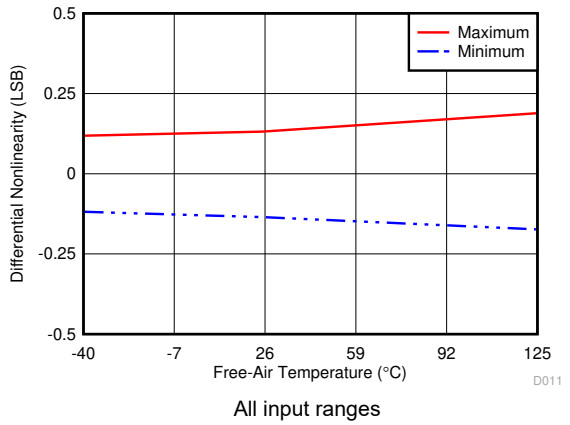


All input ranges

図 5-14. Typical DNL for All Codes

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, DVDD = 3V, V_{REF} = 4.096V (internal), and maximum throughput (unless otherwise noted)



All input ranges

図 5-15. DNL vs Temperature

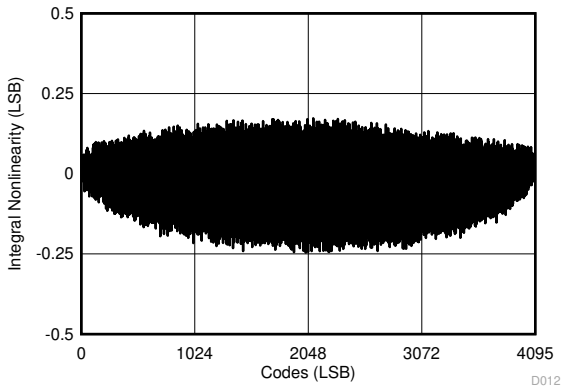


図 5-16. Typical INL for All Codes (All Bipolar Ranges)

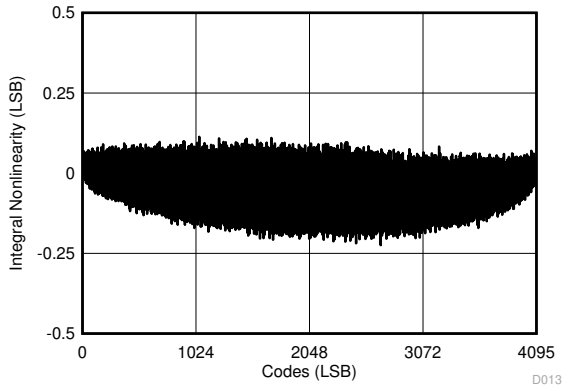


図 5-17. Typical INL for All Codes (All Unipolar Ranges)

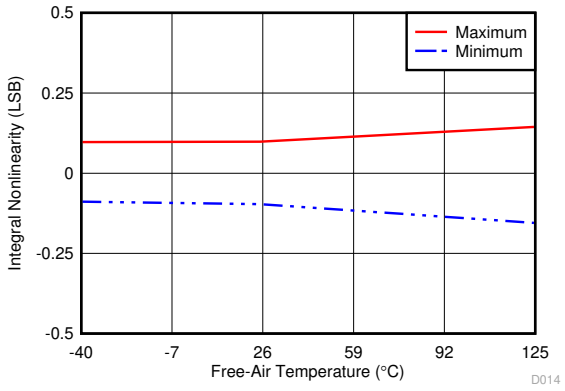


図 5-18. INL vs Temperature (All Bipolar Ranges)

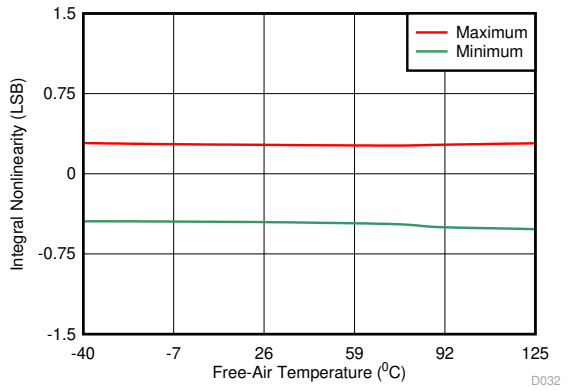


図 5-19. INL vs Temperature (All Unipolar Ranges)

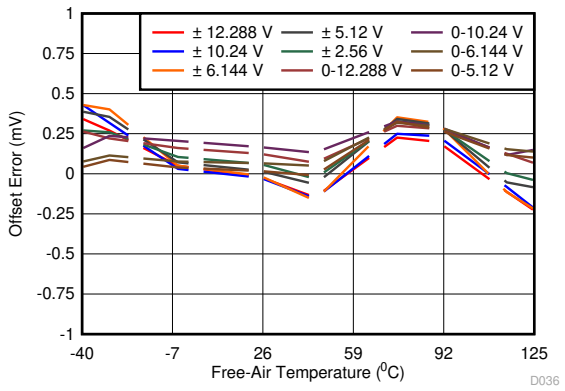


図 5-20. Offset Error vs Temperature Across Input Ranges

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, DVDD = 3V, V_{REF} = 4.096V (internal), and maximum throughput (unless otherwise noted)

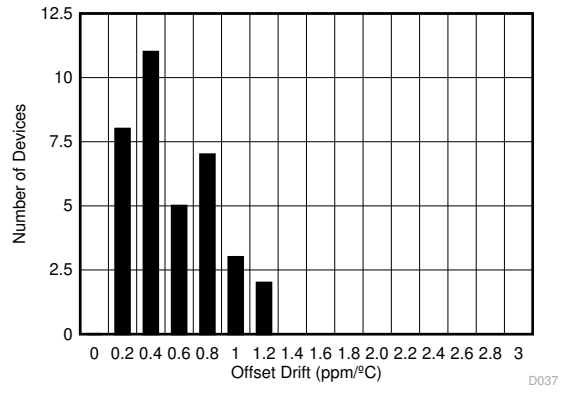


図 5-21. Typical Histogram for Offset Drift

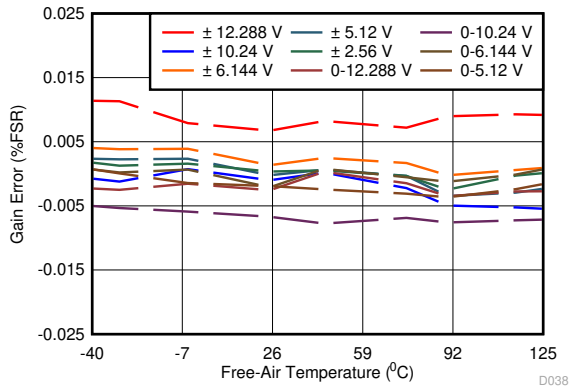


図 5-22. Gain Error vs Temperature Across Input Ranges

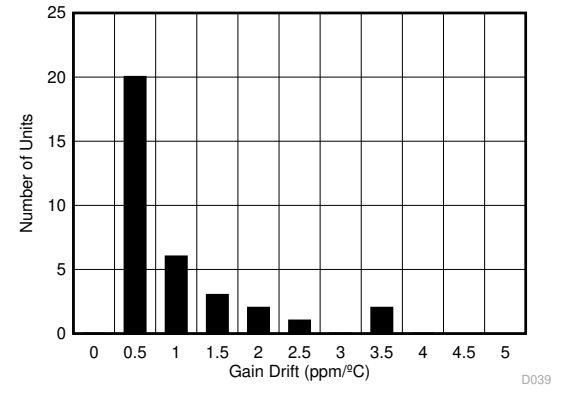


図 5-23. Typical Histogram for Gain Error Drift

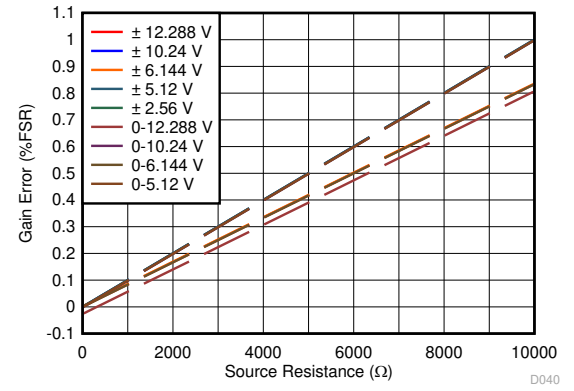
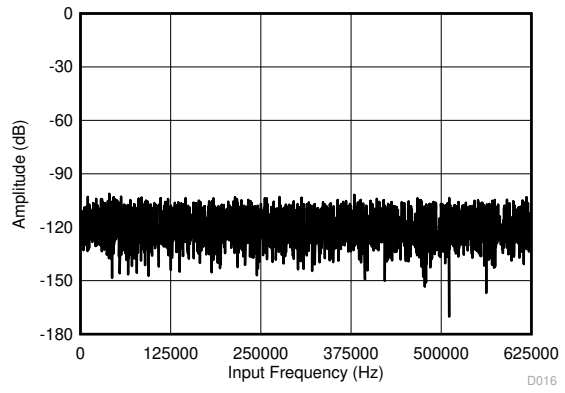


図 5-24. Gain Error vs External Resistance (R_{EXT})



Number of points = 64k, f_{IN} = 1kHz

図 5-25. Typical FFT Plot (All Ranges) for the ADS8661W

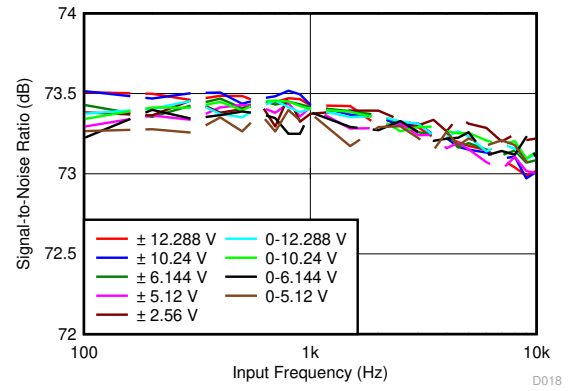
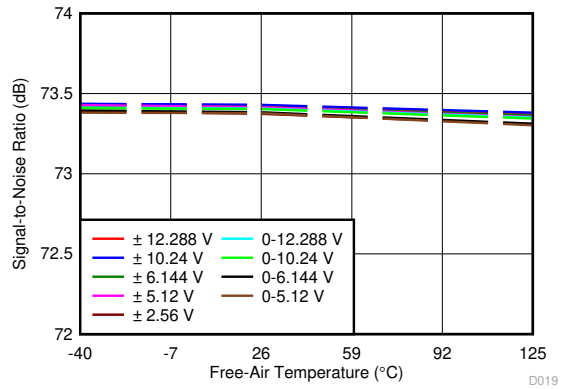


図 5-26. SNR vs Input Frequency

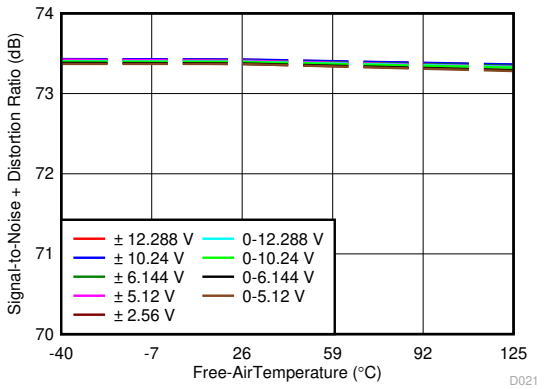
5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, DVDD = 3V, V_{REF} = 4.096V (internal), and maximum throughput (unless otherwise noted)



f_{IN} = 1kHz

図 5-27. SNR vs Temperature



f_{IN} = 1kHz

図 5-28. SINAD vs Temperature

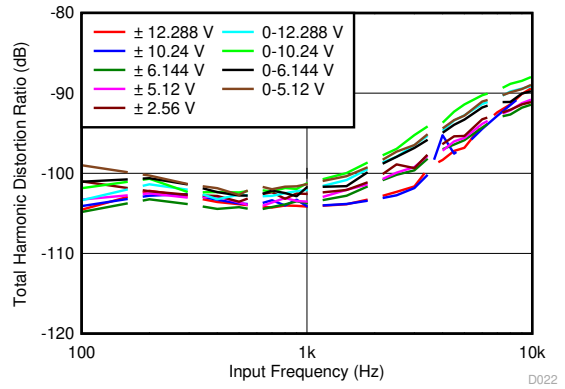
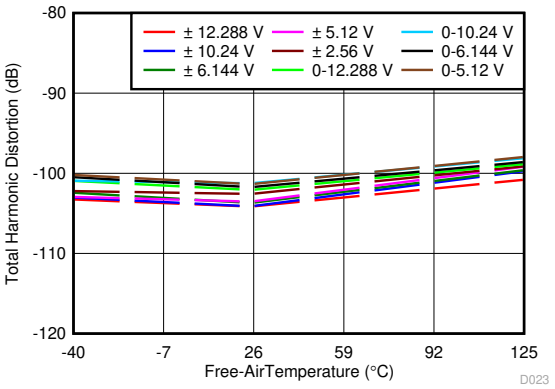


図 5-29. THD vs Input Frequency



f_{IN} = 1kHz

図 5-30. THD vs Temperature

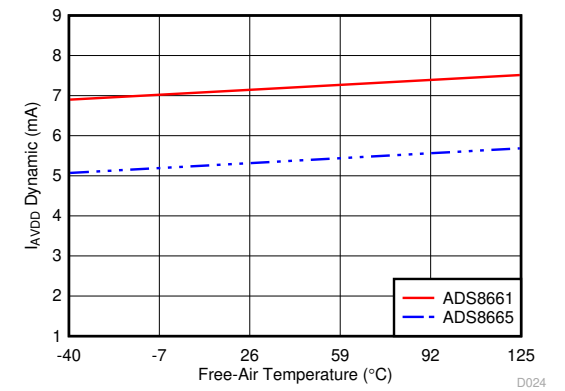


図 5-31. AVDD Current vs Temperature

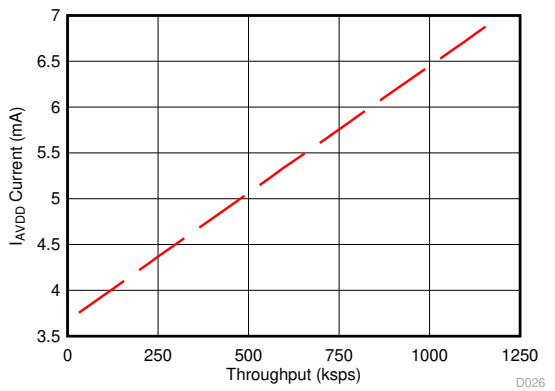


図 5-32. AVDD Current vs Throughput

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, DVDD = 3V, V_{REF} = 4.096V (internal), and maximum throughput (unless otherwise noted)

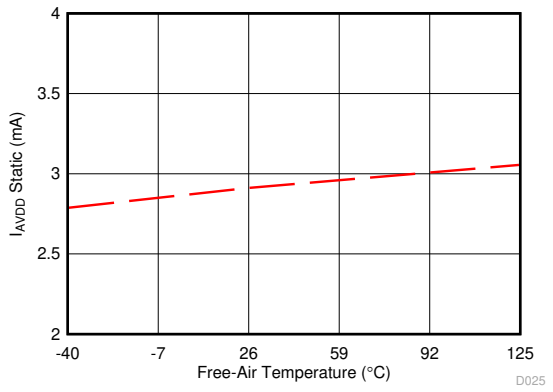


図 5-33. AVDD Current vs Temperature (During Sampling)

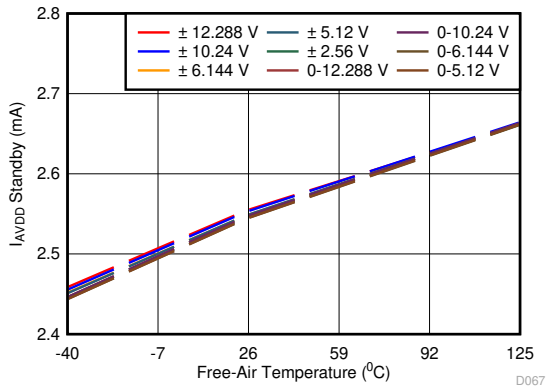


図 5-34. AVDD Current vs Temperature (Standby Mode)

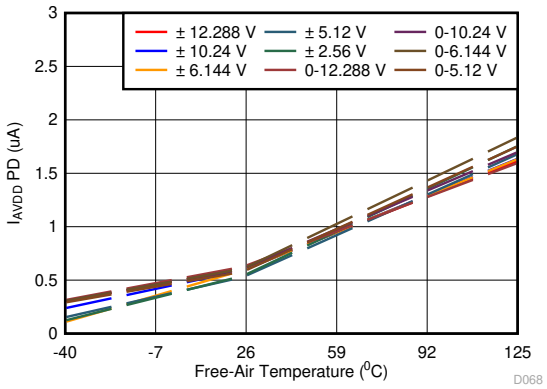


図 5-35. AVDD Current vs Temperature (Power-Down Mode)

6 Detailed Description

6.1 Overview

The ADS8661W is a high-speed, high-performance, easy-to-use integrated data acquisition system device. Theis single-channel device supports true bipolar differential and single-ended input voltage swings up to ±12.288V and operates on a single 5V analog supply. The ADS8661W features an enhanced SPI interface (multiSPI) that allows the sampling rate to be maximized even with lower speed host controllers.

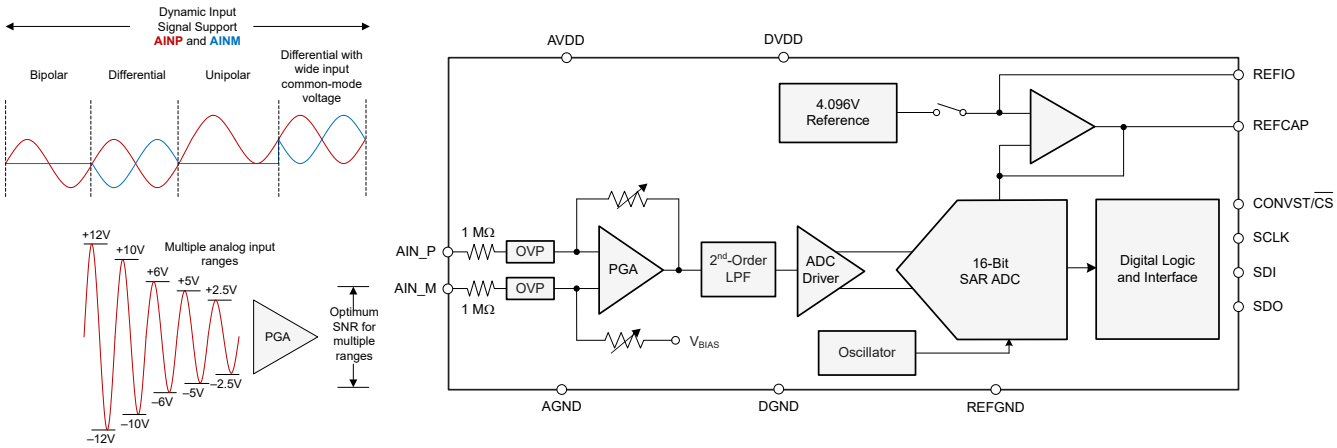
The ADS8661W consists of a high-precision successive approximation register (SAR) analog-to-digital converter (ADC) and a power-optimized analog front-end (AFE) circuit for signal conditioning. The ADS8661W includes:

- A high-resistive input impedance (≥ 1MΩ) that is independent of the sampling rate
- A programmable gain amplifier (PGA) with a differential and single-ended input configuration supporting nine software-programmable unipolar and bipolar input ranges
- A second-order, low-pass antialiasing filter
- An ADC driver amplifier that provides quick settling of the SAR ADC input for high accuracy
- An input overvoltage protection circuit up to ±20V

The device features a low temperature drift, 4.096V internal reference with a fast-settling buffer and a multiSPI serial interface with daisy-chain (DAISY) and ALARM features.

The integrated precision AFE circuit includes high input impedance and a precision ADC operating from a single 5V supply. This AFE circuit offers a simplified end solution without requiring external high-voltage bipolar supplies and complicated driver circuits.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Input Structure

The device features a differential input structure. 図 6-1 shows the simplified circuit schematic for the AFE circuit, including the input overvoltage protection circuit, PGA, low-pass filter (LPF), and high-speed ADC driver.

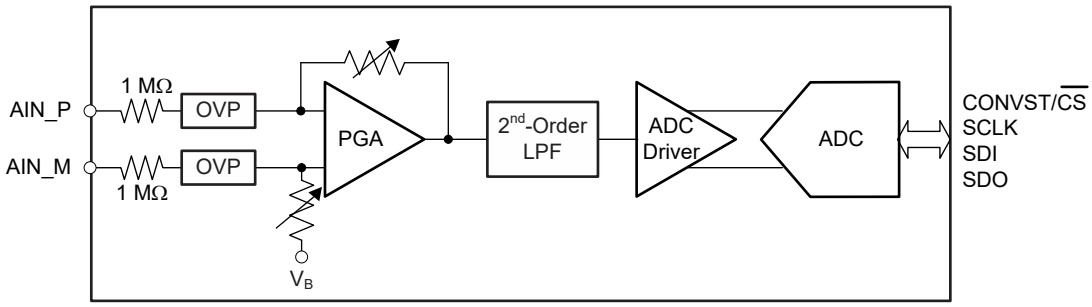


図 6-1. Simplified Analog Front-End Circuit Schematic

The ADS8661W supports multiple unipolar or bipolar, single-ended and differential input voltage ranges based on the program register configurations. As explained in the RANGE_SEL_REG register, configure the input voltage range to be bipolar or unipolar. The bipolar ranges are ±3V × V_{REF}, ±2.5V × V_{REF}, ±1.5V × V_{REF}, ±1.25V × V_{REF}, and ±0.625V × V_{REF}. The unipolar ranges are 0V to 3V × V_{REF}, 0V to 2.5V × V_{REF}, 0V to 1.5 × V_{REF}, and 0V to 1.25 × V_{REF}. With the internal or external reference voltage set to 4.096V, configure the device input ranges to bipolar or unipolar ranges. The configured bipolar ranges are ±12.288V, ±10.24V, ±6.144V, ±5.12V, and ±2.56V. The configured unipolar ranges are 0V to 12.288V, 0V to 10.24V, 0V to 6.144V, and 0V to 5.12V.

The device samples the voltage difference between the AIN_P and the AIN_M pins. For optimum performance, make sure the input currents and impedances along each input path are matched. Route the two single-ended signals to AIN_P and AIN_M as symmetrically as possible from the signal source to the ADC input pins.

If the analog input pins (AIN_P) or (AIN_M) to the device are left floating, the output of the ADC corresponds to an internal biasing voltage. The output from the ADC is considered invalid if the device operates with floating input pins. This condition does not cause any damage to the device, which becomes fully functional when a valid input voltage is applied to the pins.

6.3.2 Analog Input Impedance

The device presents a resistive input impedance ≥ 1MΩ on each of the analog inputs. The input impedance is independent of the ADC sampling frequency or the input signal frequency. The primary advantage of such high-impedance inputs is the ease of driving the ADC inputs without requiring driving amplifiers with low output impedance. Bipolar, high-voltage power supplies are not required in the system because this ADC does not require any high-voltage, front-end drivers. In most applications, the signal sources or sensor outputs are directly connected to the ADC input, thus significantly simplifying the design of the signal chain.

To maintain the dc accuracy of the system, match the external source impedance on the AIN_P input pin with an equivalent resistance on the AIN_M pin. This matching helps cancel any additional offset error contributed by the external resistance.

6.3.3 Input Protection Circuit

The device features an internal overvoltage protection (OVP) circuit on each of the analog inputs. Use the external protection devices in the end application to protect against surges, electrostatic discharge (ESD), and electrical fast transient (EFT) conditions. 図 6-2 illustrates a conceptual block diagram of the internal OVP circuit.

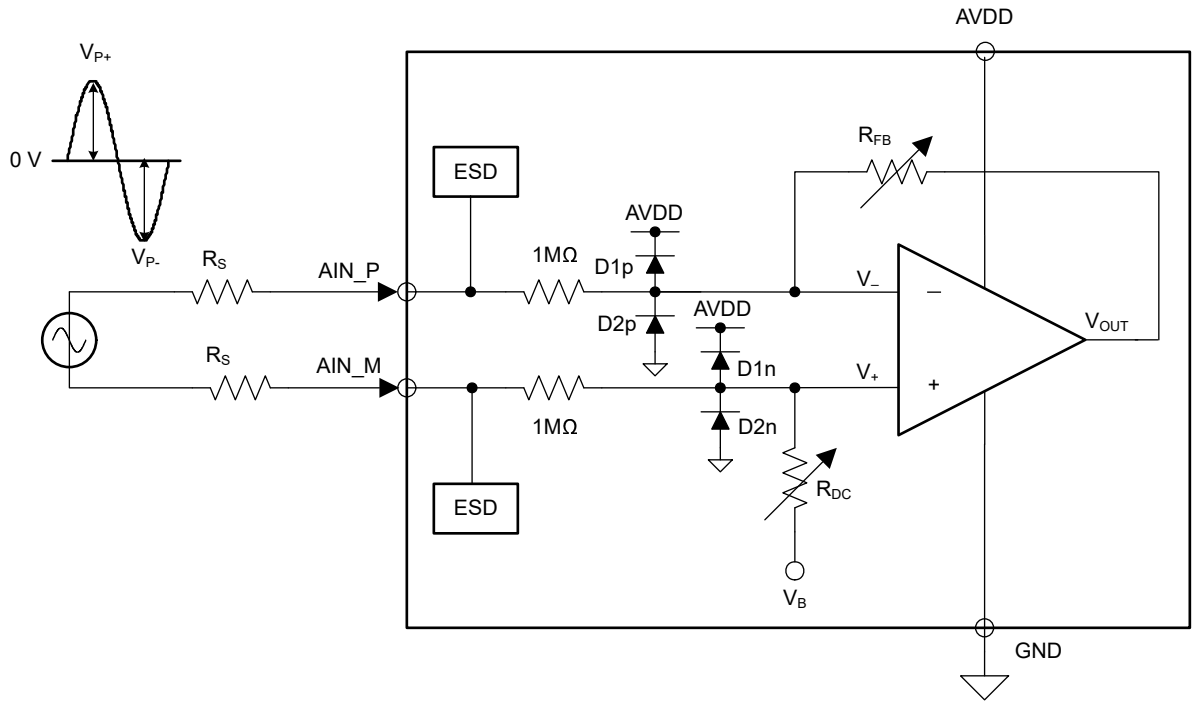


図 6-2. Input Overvoltage Protection Circuit Schematic

As shown in 図 6-2, the combination of input resistors and PGA gain-setting resistors R_{FB} and R_{DC} limit the current flowing into the input pin. Use 1MΩ (or 1.2MΩ for appropriate input ranges) input resistors. A combination of antiparallel diodes, D1 and D2, are added to protect the internal circuitry and set the overvoltage protection limits.

表 6-1 explains the various operating conditions for the device when powered on. Make sure the device is properly powered up (AVDD = 5V) or offers a low impedance of < 30kΩ. When properly set, the internal overvoltage protection circuit withstands up to ±20V on the analog input pins.

表 6-1. Input Overvoltage Protection Limits When AVDD = 5V

INPUT CONDITION(1) (V_{OVP} = ±20V)		TEST CONDITION	ADC OUTPUT	COMMENTS
CONDITION	RANGE			
$\|V_{IN}\| < \|V_{RANGE}\|$	Within operating range	All input ranges	Valid	The device functions as per data sheet specifications.
$\|V_{RANGE}\| < \|V_{IN}\| < \|V_{OVP}\|$	Beyond operating range but within overvoltage range	All input ranges	Saturated	The ADC output is saturated, but the device is internally protected (not recommended for extended time).
$\|V_{IN}\| > \|V_{OVP}\|$	Beyond overvoltage range	All input ranges	Saturated	This usage condition potentially causes irreversible damage to the device.

(1) GND = 0V, AIN_M = 0V, $|V_{RANGE}|$ is the maximum input voltage for any selected input range, and $|V_{OVP}|$ is the breakdown voltage for the internal OVP circuit. Assume that R_S is approximately 0Ω.

The results indicated in 表 6-1 assume that the analog input pin is driven by a very low impedance source (R_S is approximately 0Ω). However, if the source driving the input has higher impedance, the current flowing through the protection diodes reduces further, thereby increasing the OVP voltage range. Higher source impedances result in gain errors and contribute to overall system noise performance.

図 6-3 illustrates the voltage versus current response of the internal overvoltage protection circuit when the device is powered on. According to this current-to-voltage (I-V) response, the current flowing into the device input pin is limited by the input impedance. The input impedance is 1MΩ (or 1.2MΩ for appropriate input ranges). However, for voltages beyond ±20V, the internal node voltages surpass the breakdown voltage for internal transistors. Thus, the limit for overvoltage protection is set on the input pin.

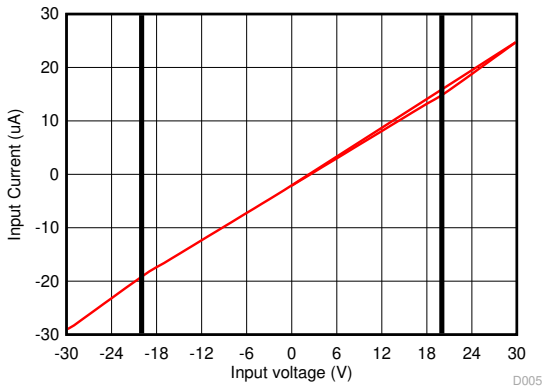


図 6-3. I-V Curve for the Input OVP Circuit (AVDD = 5V)

The same overvoltage protection circuit also provides protection to the device when the device is not powered on and AVDD is floating. This condition arises when the input signals are applied before the ADC is fully powered on. 表 6-2 shows the overvoltage protection limits for this condition.

表 6-2. Input Overvoltage Protection Limits When AVDD = Floating

INPUT CONDITION(1) (V_{OVP} = ±15V)		TEST CONDITION	ADC OUTPUT	COMMENTS
CONDITION	RANGE			
$\|V_{IN}\| < \|V_{OVP}\|$	Within overvoltage range	All input ranges	Invalid	The device is not functional but is protected internally by the OVP circuit.
$\|V_{IN}\| > \|V_{OVP}\|$	Beyond overvoltage range	All input ranges	Invalid	This usage condition potentially causes irreversible damage to the device.

(1) AVDD = floating, GND = 0V, AIN_M = 0V, $|V_{RANGE}|$ is the maximum input voltage for any selected input range, and $|V_{OVP}|$ is the breakdown voltage for the internal OVP circuit. Assume that R_S is approximately 0Ω.

図 6-4 shows the I-V response of the internal overvoltage protection circuit when the device is not powered on. According to this I-V response, the current flowing into the device input pin is limited by the 1MΩ input impedance. However, for voltages beyond ±15V, the internal node voltage surpasses the breakdown voltage for internal transistors. Thus, the limit for overvoltage protection is set on the input pin.

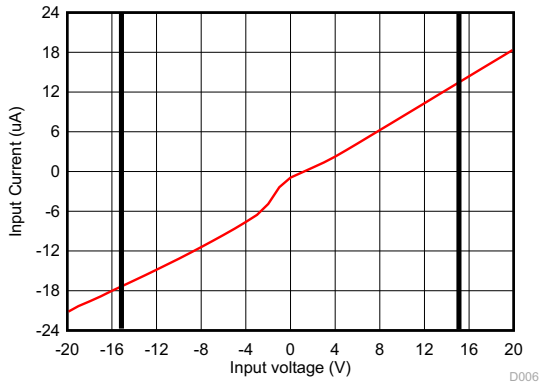


図 6-4. I-V Curve for the Input OVP Circuit (AVDD = Floating)

6.3.4 Programmable Gain Amplifier (PGA)

The device features a programmable gain amplifier (PGA) as part of the analog signal-conditioning circuit. This circuit converts the original single-ended or differential input signal into a signal that drives the internal SAR ADC. The PGA also adjusts the common-mode level of the input signal before the signal is fed into the SAR ADC. This process provides maximum usage of the ADC input dynamic range. Depending on the range of the input signal, adjust the PGA gain by setting the RANGE_SEL[3:0] bits in the configuration register. See the RANGE_SEL_REG register. The default or power-on state for the RANGE_SEL[3:0] bits is 0000, corresponding to an input signal range of ±3V × V_{REF}. 表 6-3 lists the various configurations of the RANGE_SEL[3:0] bits for the different analog input voltage ranges.

The PGA uses a precisely-matched network of resistors for multiple gain configurations. Matching between these resistors is accurately trimmed to keep the overall gain error low across all input ranges.

表 6-3. Input Range Selection Bits Configuration

ANALOG INPUT RANGE (AIN_P – AIN_M)	RANGE_SEL[3:0]			
	BIT 3	BIT 2	BIT 1	BIT 0
±3V × V_{REF}	0	0	0	0
±2.5V × V_{REF}	0	0	0	1
±1.5V × V_{REF}	0	0	1	0
±1.25V × V_{REF}	0	0	1	1
±0.625V × V_{REF}	0	1	0	0
0V–3V × V_{REF}	1	0	0	0
0V–2.5V × V_{REF}	1	0	0	1
0V–1.5V × V_{REF}	1	0	1	0
0V–1.25V × V_{REF}	1	0	1	1

6.3.5 Second-Order, Low-Pass Filter (LPF)

To mitigate the noise of the front-end amplifier and PGA gain resistors, the device AFE circuit features a second-order, antialiasing LPF at the PGA output. 図 6-5 and 図 6-6 show the magnitude and phase response of the analog antialiasing filter, respectively. For maximum performance, the –3dB cutoff frequency for the antialiasing filter is typically set to 500kHz. The performance of the filter is consistent across all input ranges supported by the ADC.

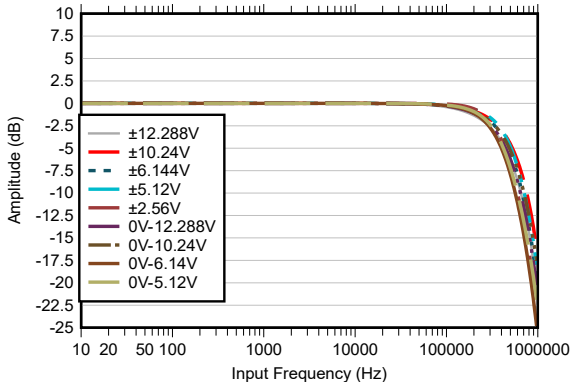


図 6-5. Second-Order LPF Magnitude Response

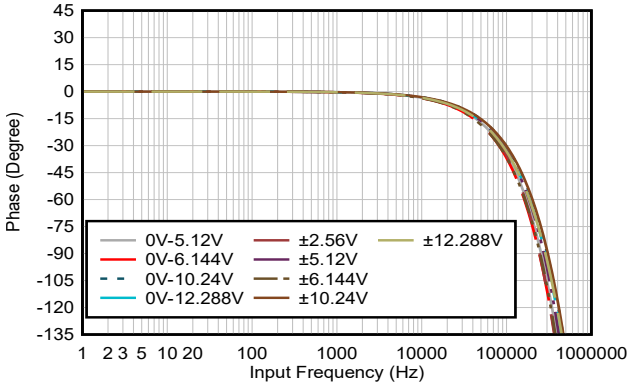


図 6-6. Second-Order LPF Phase Response

6.3.6 ADC Driver

To meet device performance at the maximum sampling rate, make sure the sample-and-hold capacitors at the ADC input successfully charge and discharge during the acquisition time window. This drive requirement at the input of the ADC necessitates the use of a high-bandwidth, low-noise, and stable amplifier buffer. Such an input driver is integrated in the front-end signal path of the device analog input channel.

6.3.7 Reference

The device operates with either an internal or external voltage reference using the internal buffer. The internal or external reference selection is determined by programming the INTREF_DIS bit of the RANGE_SEL_REG register. The internal reference source is enabled (INTREF_DIS = 0) by default after reset or when the device powers up. Program the INTREF_DIS bit to logic 1 to disable the internal reference source whenever an external reference source is used.

6.3.7.1 Internal Reference

The device features an internal reference source with a nominal output value of 4.096V. To select the internal reference, program the INTREF_DIS bit of the RANGE_SEL_REG register to logic 0. When the internal reference is used, the REFIO pin becomes an output with the internal reference value. As shown in 図 6-7, place a 4.7µF (minimum) decoupling capacitor between the REFIO and REFGND pins. The output impedance of the internal band-gap circuit creates a low-pass filter with this capacitor to band-limit the noise of the reference. Using a smaller capacitor value allows higher reference noise in the system that potentially degrades SNR and SINAD performance. Do not use the REFIO pin to drive external ac or dc loads because of limited current output capability. Use the REFIO pin as a source if followed by an acceptable op amp buffer (such as the OPA320).

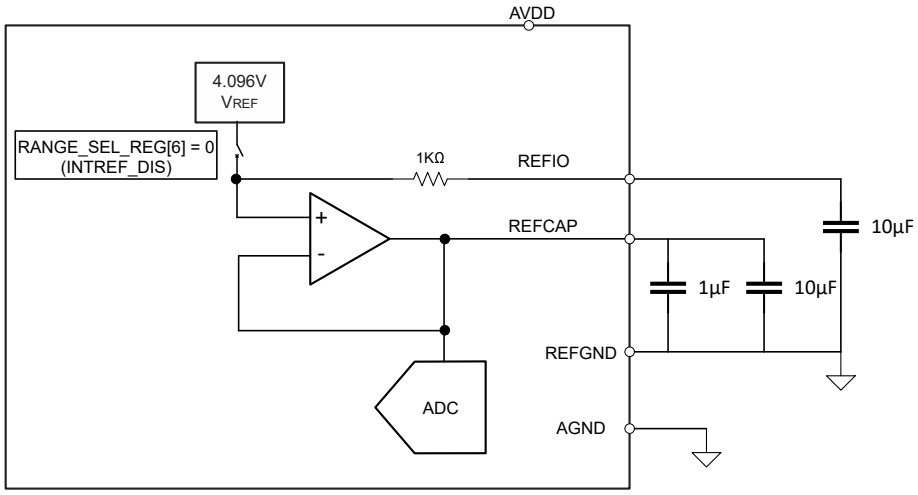


図 6-7. Device Connections for Using an Internal 4.096V Reference

The device internal reference is factory-trimmed to provide the initial accuracy specification. The histogram in 図 6-8 shows the distribution of the internal voltage reference output taken from more than 3420 production devices.

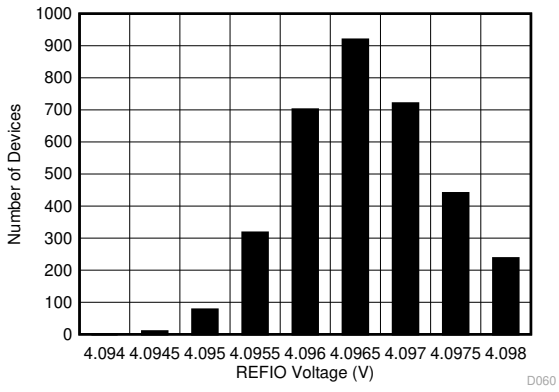


図 6-8. Internal Reference Accuracy Histogram at Room Temperature

The initial accuracy specification for the internal reference is degraded if the die is exposed to any mechanical or thermal stress. Heating the device while soldering to a printed circuit board (PCB) and any subsequent solder reflow is a primary cause for shifts in the V_{REF} value. The main cause of thermal hysteresis is a change in die stress and is a function of the package, die-attach material, molding compound, and device layout.

To illustrate this effect, 30 devices were soldered using lead-free solder paste with the manufacturer suggested reflow profile. This process is explained in the *AN-2029 Handling and Process Recommendations* application note. As shown in 図 6-9, the internal voltage reference output is measured before and after the reflow process and the typical shift in value. Although all tested units exhibit a positive shift in the output voltages, negative shifts are also possible. The histogram in 図 6-9 shows the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, which is common on PCBs with surface-mount components on both sides, causes additional shifts in the output voltage. If the PCB is to be exposed to multiple reflows, solder the ADS8661W in the second pass to minimize device exposure to thermal stress.

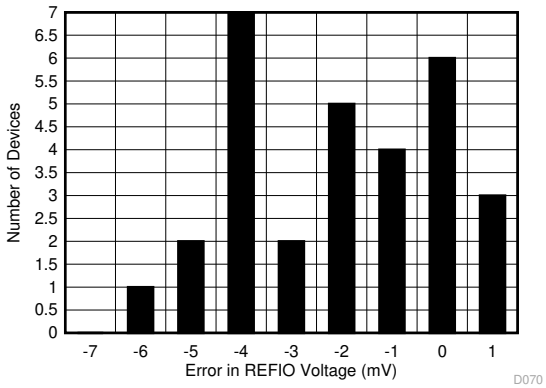


図 6-9. Solder Heat Shift Distribution Histogram

The internal reference is also temperature compensated to provide excellent temperature drift over an extended industrial temperature range of –40°C to +125°C. 図 6-10 shows the variation of the internal reference voltage across temperature for different values of the AVDD supply voltage. 図 6-11 shows histogram distribution of the reference voltage drift for the WQFN (RUM) package.

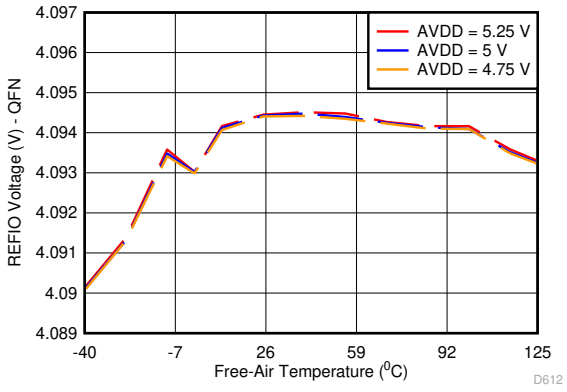
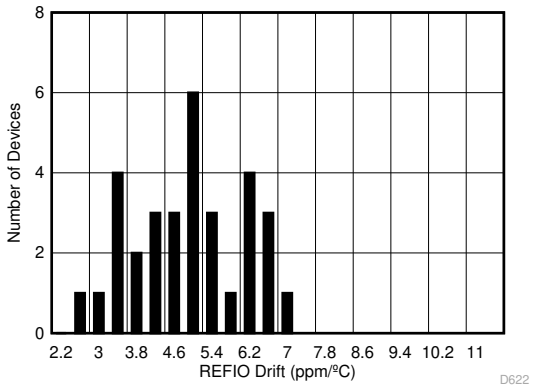


図 6-10. REFIO Voltage Variation Across AVDD and Temperature



AVDD = 5V, number of devices = 30, ΔT = –40°C to +125°C

図 6-11. Internal Reference Temperature Drift Histogram

6.3.7.2 External Reference

The device provides a provision for applications that require a better reference voltage or a common reference voltage for multiple devices. This provision allows an external reference source to be used with an internal buffer to drive the ADC reference pin. To select the external reference mode, program the INTREF_DIS bit of the RANGE_SEL_REG register to logic 1. In this mode, apply an external 4.096V reference at the REFIO pin, which functions as an input. The internal buffer is optimally designed to handle the dynamic loading on the REFCAP pin that is internally connected to the ADC reference input. Thus, any low-power, low-drift, or small-size external reference is applicable in this mode. Appropriately filter the output of the external reference to minimize the resulting effect of the reference noise on system performance. 図 6-12 shows a typical connection diagram for this mode.

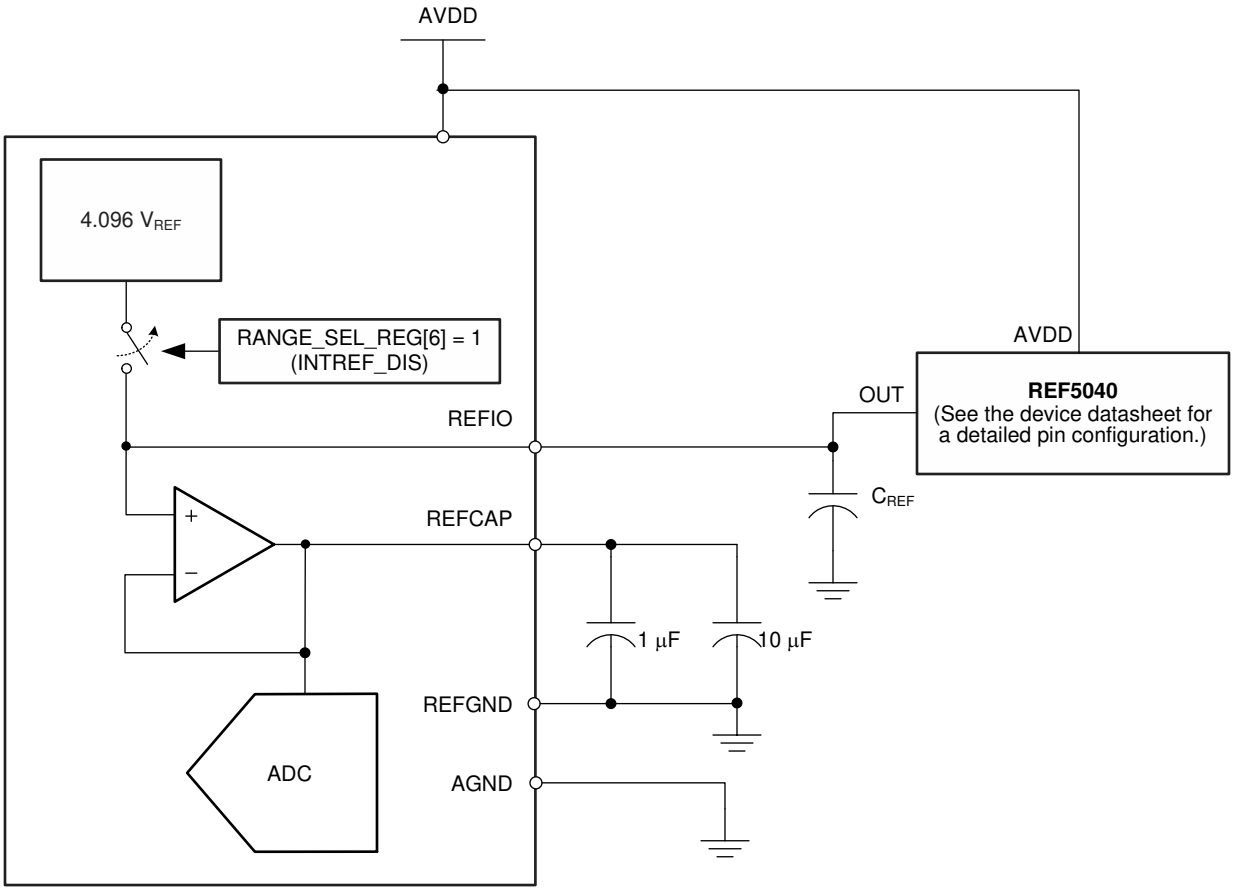


図 6-12. Device Connections for Using an External 4.096V Reference

The output of the internal reference buffer appears at the REFCAP pin. Place a 10µF minimum capacitance between the REFCAP and REFGND pins. Place another 1µF capacitor as close to the REFCAP pin as possible for decoupling high-frequency signals. Do not use the internal buffer to drive external ac or dc loads because of the limited current output capability of this buffer.

The performance of the internal buffer output is very stable across the entire operating temperature range of –40°C to +125°C. 図 6-13 shows the variation in the REFCAP output across temperature for different values of the AVDD supply voltage. As shown in 図 6-14, the typical specified value of the reference buffer drift over temperature is 0.5ppm/°C. The maximum specified temperature drift is equal to 2ppm/°C.

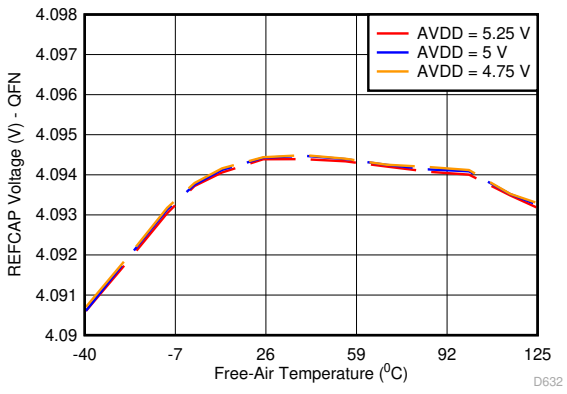
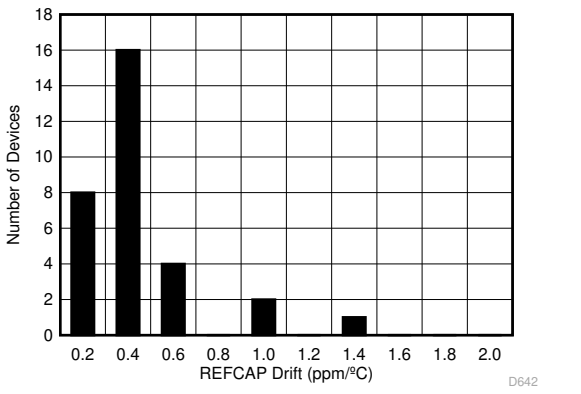


図 6-13. Reference Buffer Output (REFCAP) Variation vs Supply and Temperature



AVDD = 5V, number of devices = 30, ΔT = –40°C to +125°C

図 6-14. Reference Buffer Temperature Drift Histogram

6.3.8 ADC Transfer Function

The device supports single-ended and differential inputs supporting both bipolar and unipolar input ranges. The output of the device is in straight-binary format for both bipolar and unipolar input ranges.

図 6-15 shows the ideal transfer characteristic for all input ranges. The full-scale range (FSR) for each input signal is equal to the difference between the positive full-scale (PFS) and the negative full-scale (NFS) input voltage. The LSB size is equal to FSR / 2^{12}. For a reference voltage of V_{REF} = 4.096V, 表 6-4 lists the LSB values corresponding to the different input ranges.

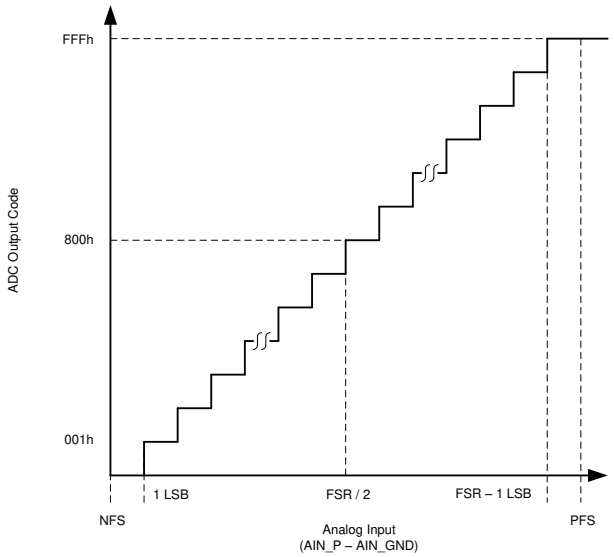


図 6-15. Device Transfer Function (Straight-Binary Format)

表 6-4. ADC LSB Values for Different Input Ranges (V_{REF} = 4.096V)

INPUT RANGE	POSITIVE FULL-SCALE (V)	NEGATIVE FULL-SCALE (V)	FULL-SCALE RANGE (V)	LSB
±3V × V_{REF}	12.288	–12.288	24.576	6mV
±2.5V × V_{REF}	10.24	–10.24	20.48	5mV
±1.5V × V_{REF}	6.144	–6.144	12.288	3mV
±1.25V × V_{REF}	5.12	–5.12	10.24	2.5mV
±0.625V × V_{REF}	2.56	–2.56	5.12	1.25mV
0V to 3V × V_{REF}	12.288	0	12.288	3mV
0V to 2.5V × V_{REF}	10.24	0	10.24	2.5mV
0V to 1.5V × V_{REF}	6.144	0	6.144	1.5mV
0V to 1.25V × V_{REF}	5.12	0	5.12	1.25mV

6.3.9 Alarm Features

The device features an active-high alarm output on the ALARM/SDO-1/GPO pin, provided that the pin is configured for alarm functionality. To enable the ALARM output on the multifunction pin, set the SDO1_CONFIG[1:0] bits of the SDO_CTL_REG register to 01b.

The device features two types of alarm functions: an input alarm and an AVDD alarm.

- For the input alarm, the voltage at the ADC input is monitored and compared against user-programmable high and low threshold values. The device sets an active high alarm output when the corresponding digital value of the input signal goes beyond the high or low threshold set by the user. See the *Input Alarm* section for a detailed explanation of the input alarm feature functionality.
- For the AVDD alarm, the ADC analog supply voltage (AVDD) is monitored and compared against the specified typical threshold values of the AVDD supply. The low threshold value is 4.7V and the high threshold value is 5.3V. The device sets an active high alarm output if the AVDD value crosses the specified low (4.7V) or high threshold (5.3V) values in either direction.

When the alarm functionality is turned on, both the input and AVDD alarm functions are enabled by default. These alarm functions are selectively disabled by programming the IN_AL_DIS and VDD_AL_DIS bits (respectively) of the RST_PWRCTL_REG register.

Each alarm (input or AVDD) has two associated types of alarm flags: the *active* alarm flag and the *tripped* alarm flag. All alarm flags are read in the ALARM_REG register. Both flags are set when the associated alarm is triggered. The active alarm is cleared at the end of the current ADC conversion (and set again if the alarm condition persists). However, the tripped flag is cleared only after ALARM_REG is read.

The ALARM output flags are updated internally at the end of every conversion. These output flags are read during any data frame that the user initiates by bringing the CONVST/$\overline{CS}$ signal to a low level.

Read the ALARM output flags in three different ways. Read these flags with the ALARM output pin, by reading the internal ALARM registers, or by appending the ALARM flags to the data output.

- A high level on the ALARM pin indicates an over- or undervoltage condition on AVDD or on the analog input channel of the device. This pin is able to be wired to interrupt the host input.
- The internal ALARM flag bits in the ALARM_REG register are updated at the end of conversion. After receiving an ALARM interrupt on the output pin, read the internal alarm flag registers for more details on the conditions that generated the alarm.
- The alarm output flags are selectively appended to the data output bit stream (see the DATAOUT_CTL_REG register for configuration details).

図 6-16 depicts a functional block diagram for the device alarm functionality.

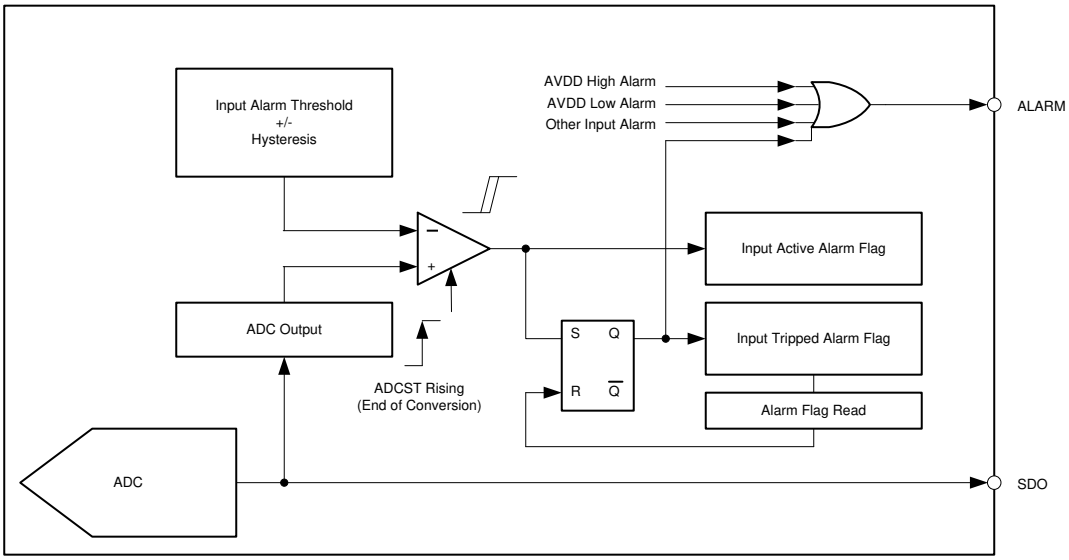


図 6-16. Alarm Functionality Schematic

6.3.9.1 Input Alarm

The device features a high and a low alarm on the analog input. The alarms corresponding to the input signal have independently programmable thresholds and a common hysteresis setting controlled through the ALARM_H_TH_REG and ALARM_L_TH_REG registers.

The device sets the input high alarm when the digital output exceeds the high alarm upper limit [high alarm threshold (T)]. The alarm resets when the digital output is less than or equal to the high alarm lower limit [high alarm (T) – H – 1]. 図 6-17 shows this function.

Similarly, the input low alarm is triggered when the digital output falls below the low alarm lower limit [low alarm threshold (T)]. The alarm resets when the digital output is greater than or equal to the low alarm higher limit [low alarm (T) + H + 1]. 図 6-18 shows this function.

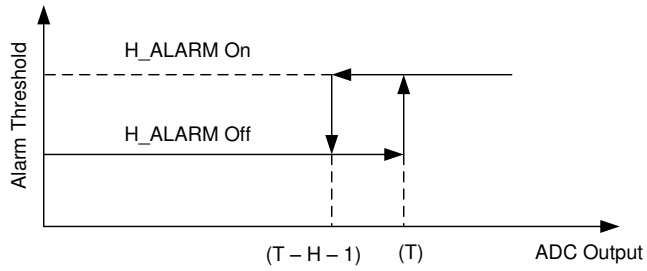


図 6-17. High ALARM Hysteresis

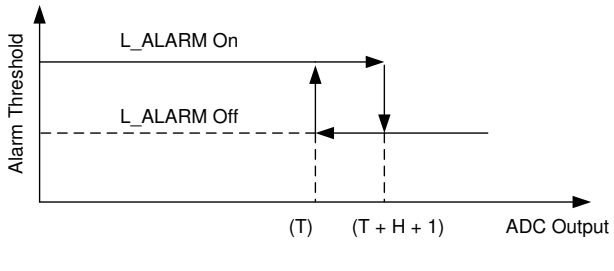


図 6-18. Low ALARM Hysteresis

6.3.9.2 AVDD Alarm

The device features a high and a low alarm on the analog voltage supply, AVDD. Unlike the input signal alarm, the AVDD alarm has fixed trip points that are set by design. The device features an internal analog comparator that constantly monitors the analog supply against the high and low threshold voltages. The high alarm is set if AVDD exceeds a typical value of 5.3V and the low alarm is asserted if AVDD drops below 4.7V. This feature is specially useful for debugging unusual device behavior caused by a glitch or brownout condition on the analog AVDD supply.

6.4 Device Functional Modes

The device features the multiSPI digital interface for communication and data transfer between the device and host controller. The multiSPI interface supports many data transfer protocols that the host uses to exchange data and commands with the device. The host transfers data into the device using one of the standard SPI modes. However, the device has various configurations available to output data to meet the specific application demands of throughput and latency. The data output in these modes is controlled either by the host or the device, and the timing is either system synchronous or source synchronous. For detailed explanation of the supported data transfer protocols, see the *Data Transfer Protocols* section.

This section describes the main components of the digital interface module and the supported configurations and protocols. As shown in 図 6-19, the interface module is comprised of shift registers (both input and output), configuration registers, and a protocol unit. During any particular data frame, data are transferred both into and out of the device. As a result, the host always perceives the device as a 32-bit, input-output shift register.

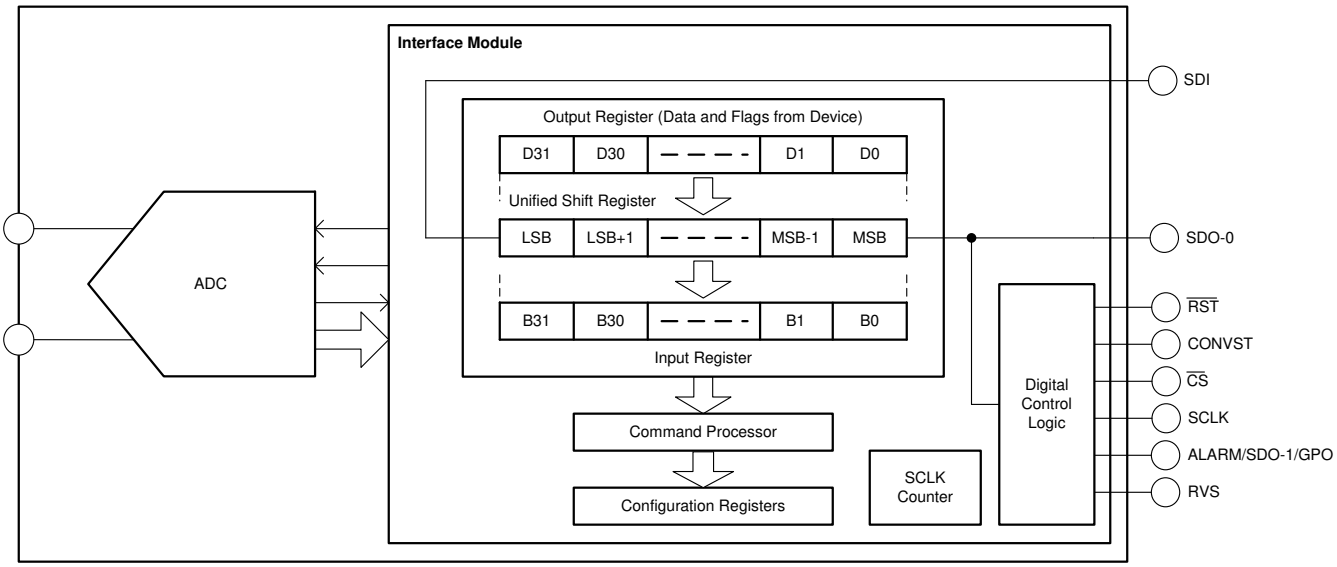


図 6-19. Device Interface Module

The *Pin Configuration and Functions* section provides descriptions of the interface pins. The *Data Transfer Frame* section details the functions of shift registers, the SCLK counter, and the command processor. The *Data Transfer Frame* section details supported protocols, and the *Register Maps* section explains the configuration registers and bit settings.

6.4.1 Host-to-Device Connection Topologies

The multiSPI interface and device configuration registers offer great flexibility in the ways a host controller exchanges data or commands with the device. This section describes how to select the hardware connection topology to meet different system requirements.

6.4.1.1 Single Device: All multiSPI Options

図 6-20 shows the pin connection between a host controller and a stand-alone device to exercise all options provided by the multiSPI interface.

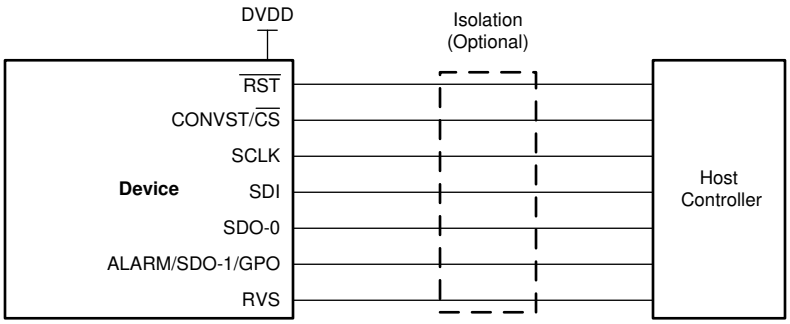


図 6-20. All multiSPI Protocols Pin Configuration

6.4.1.2 Single Device: Standard SPI Interface

図 6-21 shows the minimum pin interface for applications using a standard SPI protocol.

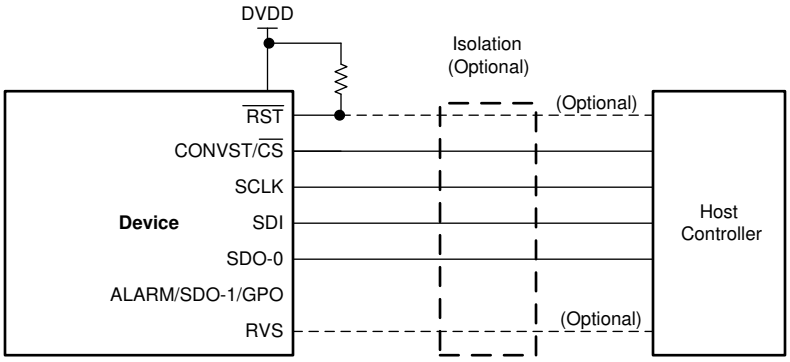


図 6-21. Standard SPI Protocol Pin Configuration

The CONVST/CS, SCLK, SDI, and SDO-0 pins constitute a standard SPI port of the host controller. Tie the RST pin to DVDD. Monitor the RVS pin for timing benefits. Do not place any external connection on the ALARM/SDO-1/GPO pin.

6.4.1.3 Multiple Devices: Daisy-Chain Topology

図 6-22 shows a typical connection diagram with multiple devices in a daisy-chain topology.

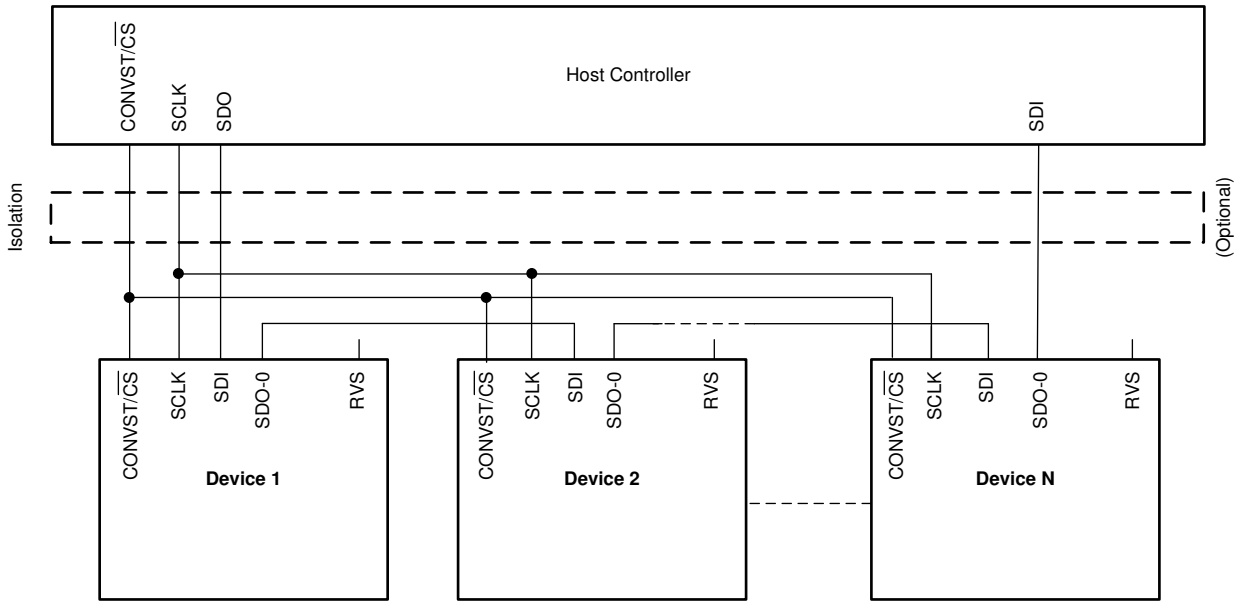


図 6-22. Daisy-Chain Connection Schematic

The CONVST/$\overline{CS}$ and SCLK inputs of all devices are connected together and controlled by a single CONVST/$\overline{CS}$ and SCLK pin of the host controller, respectively. The SDI input pin of the first device in the chain (device 1) is connected to the SDO-x pin of the host controller. The SDO-0 output pin of device 1 is connected to the SDI input pin of device 2, and so forth. The SDO-0 output pin of the last device in the chain (device N) is connected to the SDI pin of the host controller.

To operate multiple devices in a daisy-chain topology, the host controller programs the configuration registers in each device with identical values. The devices operate with a single SDO-0 output, using the external clock with any legacy, SPI-compatible protocols for data read and data write operations. In the SDO_CTL_REG register, program bits 7-0 to 00h.

All devices in the daisy-chain topology sample the analog input signals on the rising edge of the CONVST/$\overline{CS}$ signal. The data transfer frame starts with a falling edge of the same signal. At the launch edge of the SCLK signal, every device in the chain shifts out the MSB to the SDO-0 pin. On every SCLK capture edge, each daisy-chained device -shifts in data received on the SDI pin as the LSB bit of the unified shift register. 図 6-19 provides a diagram of this process. Therefore, in a daisy-chain configuration, the host controller receives the data of device N, followed by the data of device N-1, and so forth. This process continues in MSB-first fashion. On the rising edge of the CONVST/$\overline{CS}$ signal, each device decodes the contents in the unified shift register and takes appropriate action.

For N devices connected in a daisy-chain topology, an optimal data transfer frame contains 32 × N SCLK capture edges (see 図 6-23). Avoid shorter data transfer frames, which result in an erroneous device configuration. For data transfer frames with > 32 × N SCLK capture edges, the host controller appropriately aligns the configuration data for each device. The host then brings CONVST/$\overline{CS}$ high.

The overall throughput of the system is proportionally reduced with the number of devices connected in a daisy-chain topology.

図 6-23 shows a typical timing diagram for three devices connected in a daisy-chain topology and using the SPI-00-S protocol.

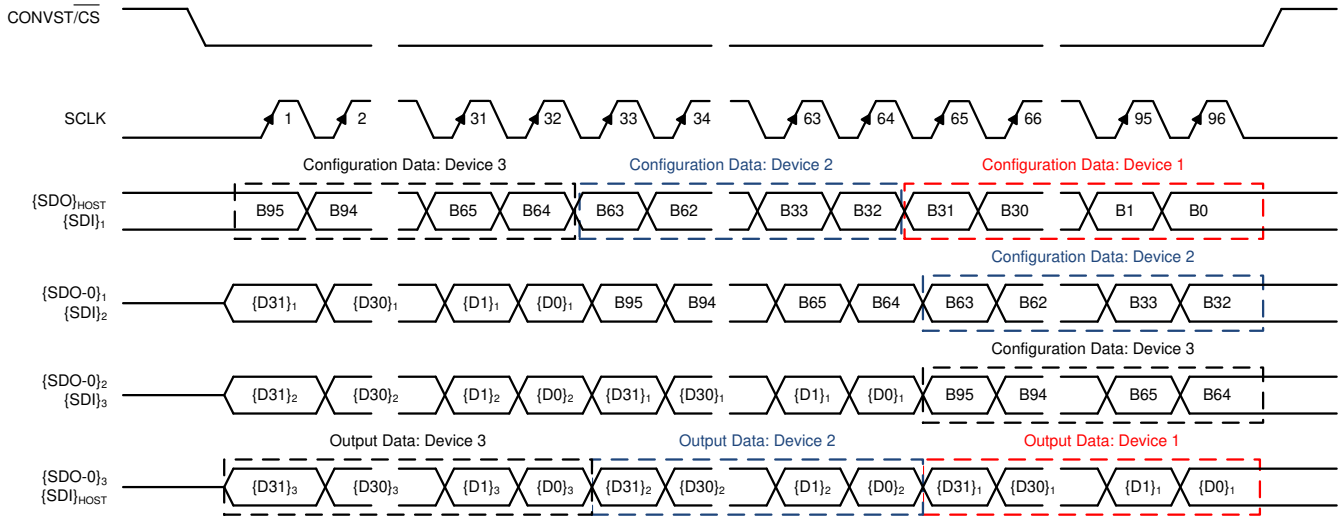


図 6-23. Three Devices in Daisy-Chain Mode Timing Diagram

6.4.2 Device Operational Modes

As shown in 図 6-24, the device supports three functional states: RESET, ACQ, and CONV. The device state is determined by the status of the CONVST/$\overline{CS}$ and $\overline{RST}$ control signals provided by the host controller.

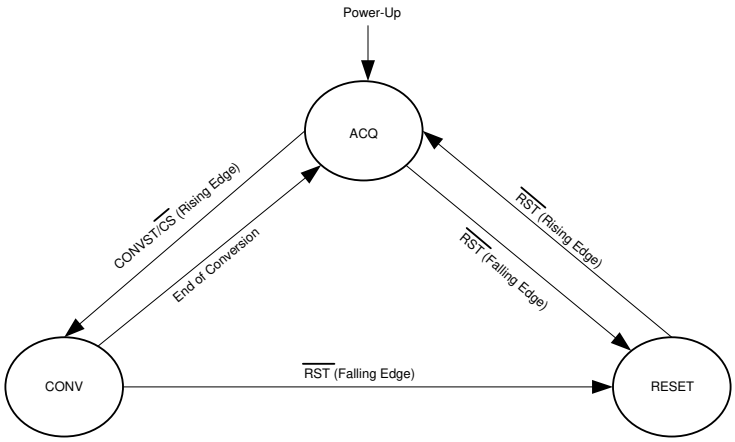


図 6-24. Device Functional States

6.4.2.1 RESET State

The device features an active-low $\overline{RST}$ pin that is an asynchronous digital input. To enter a RESET state, pull and keep the $\overline{RST}$ pin low for the t_{wl_RST} duration (as specified in the *Switching Characteristics* table).

The device features two different types of reset functions: an application reset or a power-on reset (POR). The functionality of the $\overline{RST}$ pin is determined by the state of the RSTn_APP bit in the RST_PWRCTL_REG register.

- To configure the $\overline{RST}$ pin to issue an application reset, configure the RSTn_APP bit in the RST_PWRCTL_REG register to 1b. In this RESET state, all configuration registers (see the *Register Maps*) are reset to default values, RVS pins remain low, and SDO-x pins are tri-stated.
- The default configuration for the $\overline{RST}$ pin issues a power-on reset when pulled to a low level. The RSTn_APP bit is set to 0b in this state. When a POR is issued, all internal device circuitry (including the PGA, ADC driver, and voltage reference) are reset. When the device comes out of the POR state, allow for the $t_{D\_RST\_POR}$ time duration so the internal circuitry accurately settles. See the *Switching Characteristics* table for the $t_{D\_RST\_POR}$ time duration.

To exit any of the RESET states, pull the $\overline{RST}$ pin high with CONVST/$\overline{CS}$ and SCLK held low. After a delay of $t_{D\_RST\_POR}$ or $t_{D\_RST\_APP}$ (see the *Switching Characteristics* table), the device enters ACQ state and the RVS pin goes high.

To operate the device in any of the other two states (ACQ or CONV), hold the $\overline{RST}$ pin high. With the $\overline{RST}$ pin held high, transitions on the CONVST/$\overline{CS}$ pin determine the functional state of the device. A typical conversion cycle is illustrated in 図 5-1.

6.4.2.2 ACQ State

In ACQ state, the device acquires the analog input signal. The device enters ACQ state on power-up, after any asynchronous reset, or after the end of every conversion.

The $\overline{RST}$ falling edge takes the device from an ACQ state to a RESET state. A rising edge of the CONVST/$\overline{CS}$ signal takes the device from ACQ state to a CONV state.

The device offers a low-power NAP mode to reduce power consumption in the ACQ state. See the *NAP Mode* section for more details on NAP mode.

6.4.2.3 CONV State

The device moves from ACQ state to CONV state on the rising edge of the CONVST/$\overline{CS}$ signal. The conversion process uses an internal clock and the device ignores any further transitions on the CONVST/$\overline{CS}$ signal until the ongoing conversion is complete. That is, the device ignores any further transitions during the time interval of t_{conv}.

At the end of conversion, the device enters ACQ state. The cycle time for the device is given by 式 1:

$$t_{cycle\text{-}min} = t_{conv} + t_{acq\text{-}min} \quad (1)$$

注

The conversion time, t_{conv}, varies within the specified limits of t_{conv_min} and t_{conv_max} (as specified in the *Switching Characteristics* table). After initiating a conversion, the host controller monitors for a low-to-high transition on the RVS pin or waits for the t_{conv_max} duration to elapse. The host then initiates a new operation (data transfer or conversion). If RVS is not monitored, substitute t_{conv} in 式 1 with t_{conv_max}.

6.5 Programming

The device features nine configuration registers (as described in the *Register Maps* section) and supports two types of data transfer operations. These operations are data write (the host configures the device), and data read (the host reads data from the device).

6.5.1 Data Transfer Frame

A data transfer frame between the device and the host controller begins at the falling edge of the CONVST/$\overline{CS}$ pin. This frame ends when the device starts conversions at the subsequent rising edge. The host controller initiates a data transfer frame by bringing the CONVST/$\overline{CS}$ signal low (図 6-25) after the end of the CONV phase. This process is described in the *CONV State* section.

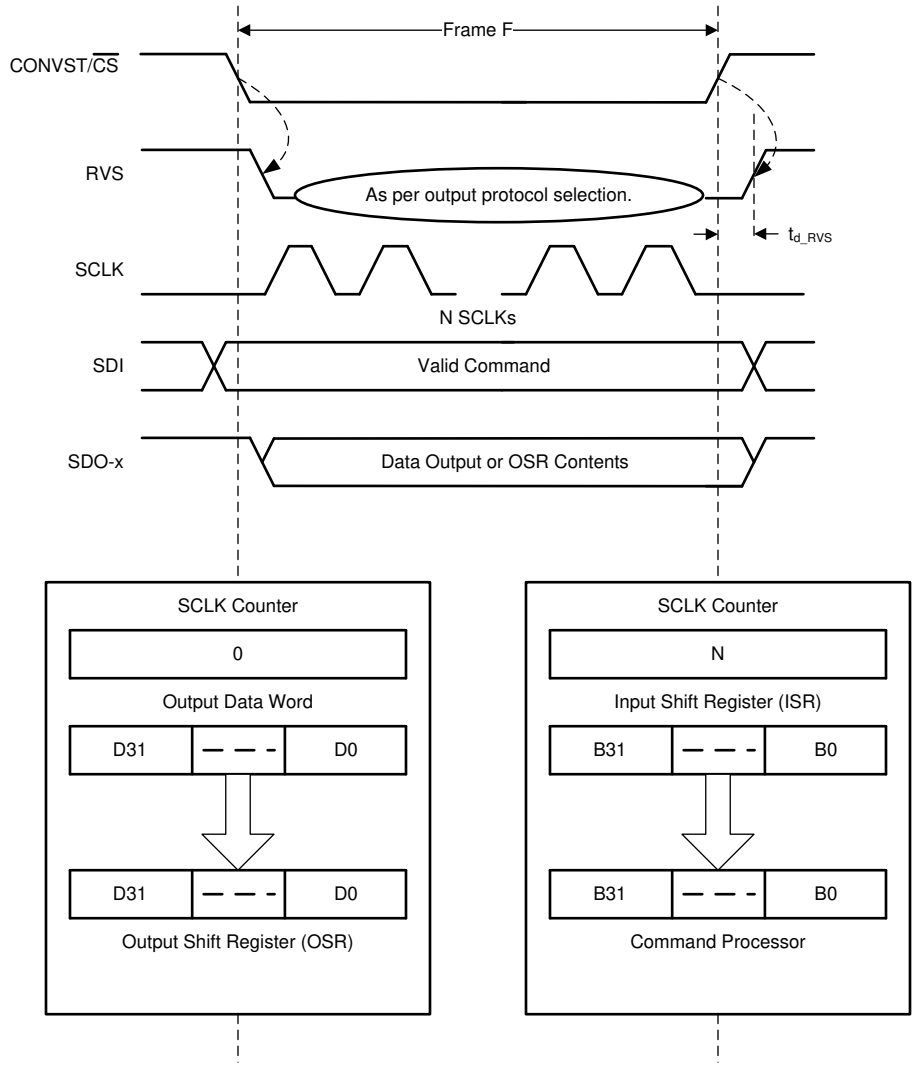


図 6-25. Data Transfer Frame

For a typical data transfer frame F:

1. The host controller pulls CONVST/$\overline{CS}$ low to initiate a data transfer frame. On the falling edge of the CONVST/$\overline{CS}$ signal:
   - RVS goes low, indicating the beginning of the data transfer frame.
   - The internal SCLK counter is reset to 0.
   - The device takes control of the data bus. As illustrated in 図 6-25, the contents of the output data word are loaded into the 32-bit output shift register (OSR).
   - The internal configuration register is reset to 0000h, corresponding to a NOP command.
2. During the frame, the host controller provides clocks on the SCLK pin:
   - On each SCLK capture edge, the SCLK counter is incremented. The data bit received on the SDI pin is then shifted into the LSB of the input shift register.
   - On each launch edge of the output clock, the MSB of the output shift register data is shifted out on the selected SDO-x pins. In this case the SCLK is the output clock.
   - The status of the RVS pin depends on the output protocol selection (see the *Protocols for Reading From the Device* section).
3. The host controller pulls the CONVST/$\overline{CS}$ pin high to end the data transfer frame. On the rising edge of CONVST/$\overline{CS}$:
   - The SDO-x pins go to tri-state.
   - As illustrated in 図 6-25, the contents of the input shift register are transferred to the command processor for decoding and further action.
   - RVS output goes low, indicating the beginning of conversion.

After pulling CONVST/$\overline{CS}$ high, the host controller monitors for a low-to-high transition on the RVS pin. Alternatively, the host controller waits for the t_{conv_max} time (see the *Switching Characteristics* table) to elapse before initiating a new data transfer frame.

At the end of the data transfer frame F:

- If the SCLK counter is 32, then the device treats the frame F as an *optimal* data transfer frame for any read or write operation. At the end of an optimal data transfer frame, the command processor treats the 32-bit input shift register contents as a valid command word.
- If the SCLK counter is less than 32, then the device treats the frame F as a *short* data transfer frame.
  - The data write operation to the device in invalid and the device treats this frame as an NOP command.
  - The output data bits transferred during a short frame on the SDO-x pins are still valid data. The host controller uses the short data transfer frame to read only the required number of MSB bits from the 32-bit output shift register.
- If the SCLK counter is greater than 32, then the device treats the frame F as a *long* data transfer frame. At the end of a long data transfer frame, the command processor treats the 32-bit input shift register contents as a valid command word. There is no restriction on the maximum number of clocks provided within any data transfer frame F. When the host provides a long data transfer frame, the last 32 bits shifted into the device before the CONVST/$\overline{CS}$ rising edge constitute the desired command.

6.5.2 Input Command Word and Register Write Operation

Any data write operation to the device is always synchronous to the external clock provided on the SCLK pin.

The device allows either one byte or two bytes (equivalent to half a word) to be read or written during any device programming operation. 表 6-5 lists the input commands supported by the device. The input commands associated with reading or writing two bytes in a single operation are suffixed as *HWORD*.

For any HWORD command, the LSB of the 9-bit address is always ignored and considered as 0b. For example, regardless whether address 04h or 05h is entered for any particular HWORD command, the device always exercises the command on address 04h.

表 6-5. List of Input Commands

OPCODE B[31:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
00000000_000000000_ 00000000_00000000	NOP	No operation
11000_xx_<9-bit address>_ <16-bit data>(1)	CLEAR_HWORD	• Command used to clear any (or a group of) bits of a register. • Any bit marked 1 in the data field results in that particular bit of the specified register being reset to 0. The other bits remain unchanged. • Half-word command (that is, the command functions on 16 bits at a time). • LSB of the 9-bit address is always ignored and considered as 0b.(2)
11001_xx_<9-bit address>_ 00000000_00000000	READ_HWORD	• Command used to perform a 16-bit read operation. • Half-word command (that is, the device outputs 16 bits of register data at a time). • LSB of the 9-bit address is always ignored and considered as 0b. • Upon receiving this command, the device sends out 16 bits of the register in the next frame.
01001_xx_<9-bit address>_ 00000000_00000000	READ	• Same as the READ_HWORD except that only eight bits of the register (byte read) are returned in the next frame.
11010_00_<9-bit address>_ <16-bit data>	WRITE	• Half-word write command (two bytes of input data are written into the specified address). • LSB of the 9-bit address is always ignored and considered as 0b.
11010_01_<9-bit address>_ <16-bit data>		• Half-word write command. • LSB of the 9-bit address is always ignored and considered as 0b. • With this command, only the MS byte of the 16-bit data word is written at the specified register address. The LSB is ignored.
11010_10_<9-bit address>_ <16-bit data>		• Half-word write command. • LSB of the 9-bit address is always ignored and considered as 0b. • With this command, only the LSB of the 16-bit data word is written at the specified register address. The MSB is ignored.
11011_xx_<9-bit address>_ <16-bit data>	SET_HWORD	• Command used to set any (or a group of) bits of a register. • Any bit marked 1 in the data field results in that particular bit of the specified register being set to 1. The other bits remain unchanged. • Half-word command (that is, the command functions on 16 bits at a time). • LSB of the 9-bit address is always ignored and considered as 0b.
All other input command combinations	NOP	No operation

(1) <9-bit address> is realized by adding a 0 at the MSB location followed by an 8-bit register address as defined in 表 7-1. The <9-bit address> for register 0x04h is 0x0-0000-0100b.

(2) An HWORD command operates on a set of 16 bits in the register map that is usually identified as two registers of eight bits each. For example, the command 11000_xx_<0_0000_0101><16-bit data> is treated the same as the command 11000_xx_<0_0000_0100><16-bit data> for bits 15:0 of the RST_PWRCTL_REG register.

Verify all input commands (including the CLEAR_HWORD, WRITE, and SET_HWORD commands listed in 表 6-5) used to configure the internal registers are 32 bits long. If any of these commands are provided in a particular data frame F, that command gets executed at the rising edge of the CONVST/$\overline{CS}$ signal.

6.5.3 Output Data Word

Data read from the device is synchronized to the external clock on the SCLK pin or to an internal device clock by programming the configuration registers. See the *Data Transfer Protocols* section for details.

In any data transfer frame, the contents of the internal output shift register are shifted out on the SDO-x pins. The output data for any frame (F+1) is determined by the command issued in frame F and the status of the DATA_VAL[2:0] bits:

- If the DATA_VAL[2:0] bits in the DATAOUT_CTL_REG register are set to 1xxb, the output data word for frame (F+1) contains fixed data pattern.
- If a valid READ command is issued in frame F, the output data word for frame (F+1) contains 8-bit register data, followed by 0's.
- If a valid READ_HWORD command is issued in frame F, the output data word for frame (F+1) contains 16-bit register data, followed by 0's.
- For all other combinations, the output data word for frame (F+1) contains the latest 16-bit conversion result. Program the DATAOUT_CTL_REG register to append various data flags to the conversion result. The data flags are appended as per the following sequence:
  1. DEVICE_ADDR[3:0] bits are appended if the DEVICE_ADDR_INCL bit is set to 1.
  2. ADC INPUT RANGE FLAGS are appended if the RANGE_INCL bit is set to 1.
  3. AVDD ALARM FLAGS are appended if the VDD_ACTIVE_ALARM_INCL bit is set to 1.
  4. INPUT ALARM FLAGS are appended if the IN_ACTIVE_ALARM_INCL bit is set to 1.
  5. PARITY bits are appended if the PAR_EN bit is set to 1.
  6. All the remaining bits in the 32-bit output data word are set to 0.

表 6-6 shows the output data word with all data flags enabled.

表 6-6. Output Data Word With All Data Flags Enabled

DEVICE_ADDR_INCL = 1b, VDD_ACTIVE_ALARM_INCL = 1b, IN_ACTIVE_ALARM_INCL = 1b, RANGE_INCL = 1b, and PAR_EN = 1b						
D[31:16]	D[15:12]	D[11:8]	D[7:6]	D[5:4]	D[3:2]	D[1:0]
Conversion result	Device address	ADC input range	AVDD alarm flags	Input alarm flags	Parity bits	00b

表 6-7 shows output data word with only some of the data flags enabled.

表 6-7. Output Data Word With Only Some Data Flags Enabled

DEVICE_ADDR_INCL = 0b, VDD_ACTIVE_ALARM_INCL = 1b, IN_ACTIVE_ALARM_INCL = 0b, RANGE_INCL = 1b, and PAR_EN = 1b				
D[31:16]	D[15:12]	D[11:10]	D[9:8]	D[7:0]
Conversion result	ADC input range	AVDD alarm flags	Parity bits	00000000b

6.5.4 Data Transfer Protocols

The device features a multiSPI interface. This interface allows the host controller to operate at slower SCLK speeds and still achieve the required cycle time with a faster response time.

- For any data write operation, the host controller uses any of the four legacy, SPI-compatible protocols to configure the device. These protocols are described in the *Protocols for Configuring the Device* section.
- For any data read operation from the device, the multiSPI interface module offers the following options:
  - Legacy, SPI-compatible protocol with a single SDO-x (see the *Legacy, SPI-Compatible (SYS-xy-S) Protocols With a Single SDO-x* section)
  - Legacy, SPI-compatible protocol with dual SDO-x (see the *Legacy, SPI-Compatible (SYS-xy-S) Protocols With Dual SDO-x* section)
  - ADC controller clock or source-synchronous (SRC) protocol for data transfer (see the *Source-Synchronous (SRC) Protocols* section)

6.5.4.1 Protocols for Configuring the Device

As described in 表 6-8, the host controller uses any of the four legacy, SPI-compatible protocols to write data into the device. These protocols are SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S.

表 6-8. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	SDI_CTL_REG	SDO_CTL_REG	DIAGRAM
SPI-00-S	Low	Rising	00h	00h	図 6-26
SPI-01-S	Low	Falling	01h	00h	図 6-26
SPI-10-S	High	Falling	02h	00h	図 6-27
SPI-11-S	High	Rising	03h	00h	図 6-27

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations. To select a different SPI-compatible protocol, program the SDI_MODE[1:0] bits in the SDI_CNTL_REG register. This first write operation adheres to the SPI-00-S protocol. Any subsequent data transfer frames adhere to the newly-selected protocol. The SPI protocol selected by the configuration of the SDI_MODE[1:0] is applicable to both read and write operations.

図 6-26 and 図 6-27 detail the four protocols using an optimal data frame; see the *Switching Characteristics* table for associated timing parameters.

注

A valid write operation to the device requires a minimum of 32 SCLKs to be provided within a data transfer frame. See the *Data Transfer Frame* section for details.

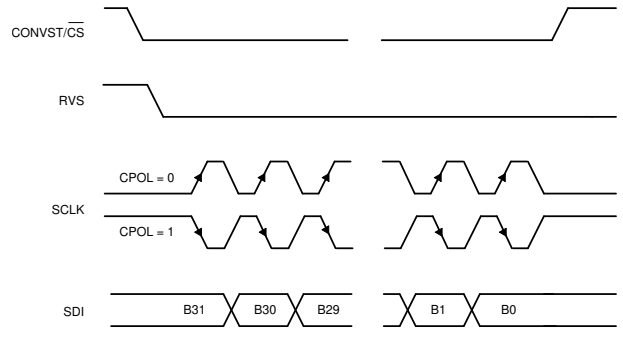


図 6-26. Standard SPI Timing Protocol (CPHA = 0, 32 SCLK Cycles)

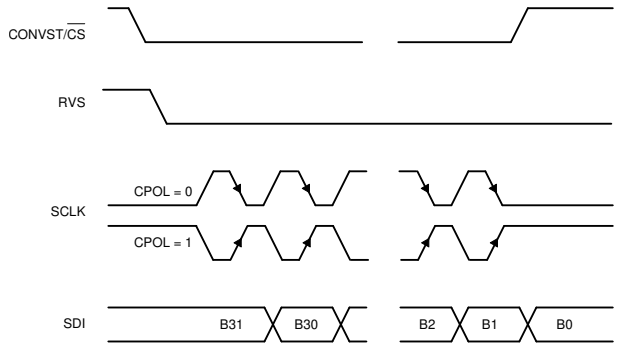


図 6-27. Standard SPI Timing Protocol (CPHA = 1, 32 SCLK Cycles)

6.5.4.2 Protocols for Reading From the Device

The protocols for the data read operation are broadly classified into three categories:

1. Legacy, SPI-compatible protocols with a single SDO-x
2. Legacy, SPI-compatible protocols with dual SDO-x
3. ADC controller clock or source-synchronous (SRC) protocol for data transfer

6.5.4.2.1 Legacy, SPI-Compatible (SYS-xy-S) Protocols With a Single SDO-x

As shown in 表 6-9, the host controller uses any of the four legacy, SPI-compatible protocols to read data from the device. These protocols are SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S.

表 6-9. SPI Protocols for Reading From the Device

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CTL_REG	SDO_CTL_REG	DIAGRAM
SPI-00-S	Low	Rising	$\overline{CS}$ falling	00h	00h	図 6-28
SPI-01-S	Low	Falling	1st SCLK rising	01h	00h	図 6-28
SPI-10-S	High	Falling	$\overline{CS}$ falling	02h	00h	図 6-29
SPI-11-S	High	Rising	1st SCLK falling	03h	00h	図 6-29

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations. To select a different SPI-compatible protocol for both the data transfer operations:

1. Program the SDI_MODE[1:0] bits in the SDI_CTL_REG register. This first write operation adheres to the SPI-00-S protocol. Any subsequent data transfer frames adhere to the newly-selected protocol.
2. Set the SDO_MODE[1:0] bits = 00b in the SDO_CTL_REG register.

注

The SPI transfer protocol selected by configuring the SDI_MODE[1:0] bits in the SDI_CTL_REG register determines the data transfer protocol for both write and read operations. Either data are read from the device or one of the SRC protocols is selected for data read, as explained in the *Source-Synchronous (SRC) Protocols* section. When data are read from the device, use the selected SPI protocol by configuring the SDO_MODE[1:0] bits = 00b in the SDO_CTL_REG register.

When using any of the SPI-compatible protocols, the RVS output remains low throughout the data transfer frame. See the *Switching Characteristics* table for associated timing parameters.

図 6-28 and 図 6-29 explain the details of the four protocols. The host controller uses a short data transfer frame to read only the required number of MSB bits from the 32-bit output data word. See the *Data Transfer Frame* section for details

If the host controller uses a long data transfer frame with SDO_CNTL_REG[7:0] = 00h, then the device exhibits daisy-chain operation. See the *Multiple Devices: Daisy-Chain Topology* section.

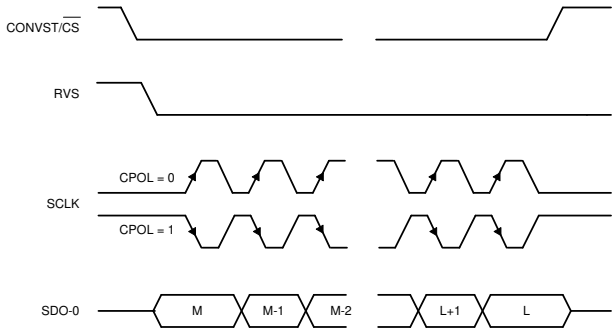


図 6-28. Standard SPI Timing Protocol (CPHA = 0, Single SDO-x)

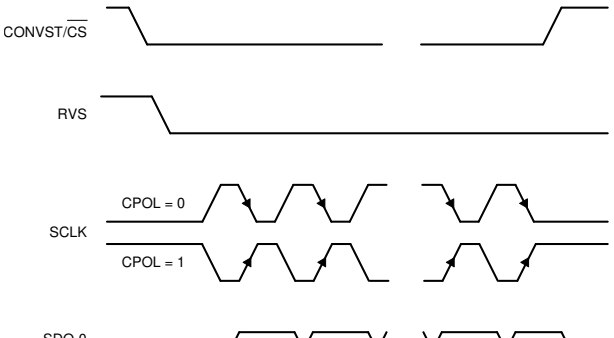


図 6-29. Standard SPI Timing Protocol (CPHA = 1, Single SDO-x)

6.5.4.2.2 Legacy, SPI-Compatible (SYS-xy-S) Protocols With Dual SDO-x

Optionally, the device increases the SDO-x bus width from one bit to two bits (dual SDO-x) when operating with any data transfer protocol. The default bus width is one bit (single SDO-x). To operate the device in dual SDO mode, set the SDO1_CONFIG[1:0] bits in the SDO_CTL_REG register to 11b. In this mode, the ALARM/ SDO-1/GPO pin functions as SDO-1.

In dual SDO mode, two bits of data are launched on the two SDO-x pins (SDO-0 and SDO-1) on every SCLK launch edge. 図 6-30 and 図 6-31 show timing diagrams for dual SDO mode.

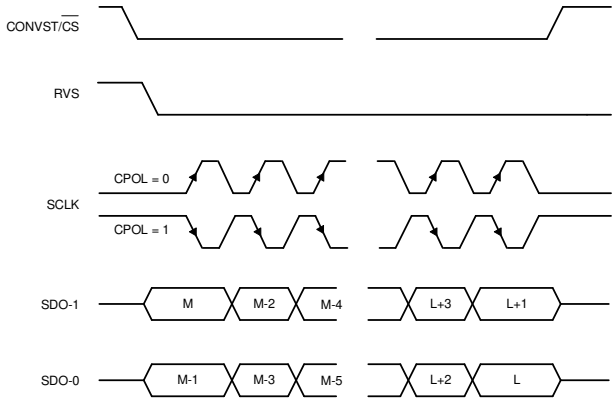


図 6-30. Standard SPI Timing Protocol (CPHA = 0, Dual SDO-x)

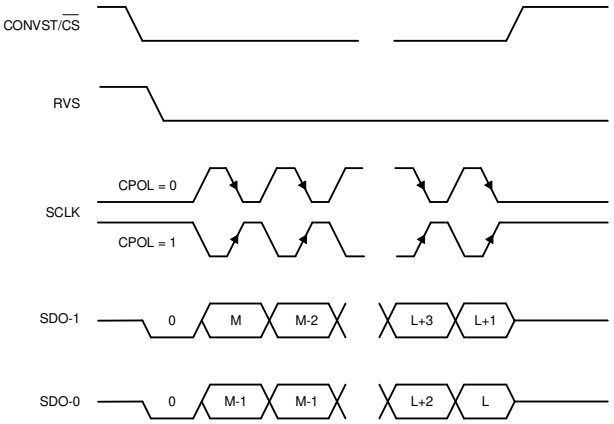


図 6-31. Standard SPI Timing Protocol (CPHA = 1, Dual SDO-x)

注

For any particular SPI protocol, the device follows the same timing specifications for single and dual SDO modes. The only difference is that the device requires half as many SCLK cycles to output the same number of bits when in single SDO mode. Thus, the minimum required SCLK frequency is reduced for a certain sampling rate of the ADC.

6.5.4.2.3 Source-Synchronous (SRC) Protocols

The multiSPI interface supports an ADC controller clock or source-synchronous mode of data transfer between the device and host controller. In this mode, the device provides an output clock that is synchronous with the output data. Furthermore, the host controller also selects the output clock source and data bus width options in this mode of operation. In all SRC modes of operation, the RVS pin provides the output clock, synchronous to the device data output.

The SRC protocol allows the clock source (internal or external) and the output bus width to be configured, similar to the SPI protocols.

6.5.4.2.3.1 Output Clock Source Options

The device allows the output clock on the RVS pin to be synchronous to either the external clock or the device internal clock. In this case, the external clock is provided on the SCLK pin. This selection is done by configuring the SSYNC_CLK bit, as explained in the SDO_CTL_REG register. The timing diagram and specifications for operating the device with an SRC protocol in external CLK mode are provided in 図 5-7 and the *Switching Characteristics* table. The timing diagram and specifications for operating the device with an SRC protocol in internal CLK mode are provided in 図 5-8 and the *Switching Characteristics* table.

6.5.4.2.3.2 Output Bus Width Options

Optionally, the device increases the SDO-x bus width from one bit to two bits (dual SDO-x) when operating with any of the SRC protocols. The default bus width is one bit (single SDO-x). To operate the device in dual SDO mode, set the SDO1_CONFIG[1:0] bits in the SDO_CTL_REG register to 11b. In this mode, the ALARM/SDO-1/GPO pin functions as SDO-1.

注

For any particular SRC protocol, the device follows the same timing specifications for single and dual SDO modes. The only difference is that the device requires half as many clock cycles to output the same number of bits when in single SDO mode. Thus, the minimum required clock frequency is reduced for a certain sampling rate of the ADC.

7 Register Maps

7.1 Device Configuration and Register Maps

The device features nine configuration registers, mapped as described in 表 7-1. Each configuration registers is comprised of four registers, each containing a data byte.

表 7-1. Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER FUNCTION
00h	DEVICE_ID_REG	Device ID register
04h	RST_PWRCTL_REG	Reset and power control register
08h	SDI_CTL_REG	SDI data input control register
0Ch	SDO_CTL_REG	SDO-x data input control register
10h	DATAOUT_CTL_REG	Output data control register
14h	RANGE_SEL_REG	Input range selection control register
20h	ALARM_REG	ALARM output register
24h	ALARM_H_TH_REG	ALARM high threshold and hysteresis register
28h	ALARM_L_TH_REG	ALARM low threshold register

表 7-2 lists the access codes for the configuration registers.

表 7-2. Register Section Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
-n		Value after reset or the default value

7.1.1 DEVICE_ID_REG Register (address = 00h)

This register contains the unique identification numbers associated to a device that is used in a daisy-chain configuration involving multiple devices.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 00h, 01h, 02h, and 03h, respectively.

図 7-1. DEVICE_ID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Reserved				DEVICE_ADDR[3:0]			
R-00h								R-0000b				R/W-0000b			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															
R-0000h															

表 7-3. DEVICE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	00h	Reserved. Reads return 00h.
23-20	Reserved	R	0000b	Reserved. Reads return 0000b.
19-16	DEVICE_ADDR[3:0](1)	R/W	0000b	These bits identify up to 16 different devices in a system.
15-0	Reserved	R	0000h	Reserved. Reads return 0000h.

(1) These bits are useful in daisy-chain mode.

7.1.2 RST_PWRCTL_REG Register (address = 04h)

This register controls the reset and power-down features offered by the converter.

Write operations to the RST_PWRCTL_REG register are preceded by a write operation with the register address set to 05h and the register data set to 69h.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 04h, 05h, 06h, and 07h, respectively.

図 7-2. RST_PWRCTL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKEY[7:0]								Reserved		VDD_AL_DIS	IN_AL_DIS	Reserved	RSTn_APP	NAP_EN	PWRDN
R/W-00h								R-00b		R/W-0b	R/W-0b	R-0b	R/W-<0>b	R/W-<0>b	R/W-0b

表 7-4. RST_PWRCTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	WKEY[7:0]	R/W	00h	This value functions as a protection key to enable writes to bits 5-0. Bits are written only if WKEY is set to 69h first.
7-6	Reserved	R	00b	Reserved. Reads return 00b
5	VDD_AL_DIS	R/W	0b	0b = VDD alarm is enabled 1b = VDD alarm is disabled
4	IN_AL_DIS	R/W	0b	0b = Input alarm is enabled 1b = Input alarm is disabled
3	Reserved	R	0b	Reserved. Reads return 0h.
2	RSTn_APP(1)	R/W	0b	0b = $\overline{\text{RST}}$ pin functions as a POR class reset (causes full device initialization) 1b = $\overline{\text{RST}}$ pin functions as an application reset (only user-programmed modes are cleared)
1	NAP_EN(2)	R/W	0b	0b = Disables the NAP mode of the converter 1b = Enables the converter to enter NAP mode if CONVST/$\overline{\text{CS}}$ is held high after the current conversion completes
0	PWRDN(2)	R/W	0b	0b = Puts the converter into active mode 1b = Puts the converter into power-down mode

(1) Setting this bit forces the $\overline{\text{RST}}$ pin to function as an application reset until the next power cycle.
(2) See the table for details on the latency encountered when entering and exiting the associated low-power mode.

7.1.3 SDI_CTL_REG Register (address = 08h)

This register configures the protocol used for writing data to the device.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 08h, 09h, 0Ah, and 0Bh, respectively.

図 7-3. SDI_CTL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Reserved						SDI_MODE [1:0]	
R-00h								R-000000b						R/W-<00>b	

表 7-5. SDI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	Reserved	R	00h	Reserved. Reads return 00h.
7-2	Reserved	R	000000b	Reserved. Reads return 000000b.
1-0	SDI_MODE[1:0]	R/W	00b	These bits select the protocol for reading from or writing to the device. 00b = Standard SPI with CPOL = 0 and CPHASE = 0 01b = Standard SPI with CPOL = 0 and CPHASE = 1 10b = Standard SPI with CPOL = 1 and CPHASE = 0 11b = Standard SPI with CPOL = 1 and CPHASE = 1

7.1.4 SDO_CTL_REG Register (address = 0Ch)

This register controls the data protocol used to transmit data out from the SDO-x pins of the device.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 0Ch, 0Dh, 0Eh, and 0Fh, respectively.

図 7-4. SDO_CTL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			GPO_VAL	Reserved		SDO1_CONFIG[1:0]		Reserved	SSYNC_CLK	Reserved				SDO_MODE[1:0]	
R-000b			R/W-0b	R-00b		R/W-00b		R-0b	R/W-<0>b	R-0h				R/W-<0>b	

表 7-6. SDO_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0h.
15-13	Reserved	R	000b	Reserved. Reads return 000b.
12	GPO_VAL	R/W	0b	1-bit value for the output on the GPO pin.
11-10	Reserved	R	00b	Reserved. Reads return 00b.
9-8	SDO1_CONFIG[1:0]	R/W	00b	Two bits configure ALARM/SDO-1/GPO: 00b = SDO-1 is always tri-stated; 1-bit SDO mode 01b = SDO-1 functions as ALARM; 1-bit SDO mode 10b = SDO-1 functions as GPO; 1-bit SDO mode 11b = SDO-1 combined with SDO-0 offers a 2-bit SDO mode
7	Reserved	R	0b	Reserved. Reads return 0b.
6	SSYNC_CLK(1)	R/W	0b	This bit controls the source of the clock selected for source-synchronous transmission. 0b = External SCLK (no division) 1b = Internal clock (no division)
5-2	Reserved	R	0000b	Reserved. Reads return 0000b.
1-0	SDO_MODE[1:0]	R/W	00b	These bits control the data output modes of the device. 0xb = SDO mode follows the same SPI protocol as that used for SDI; see the SDI_CTL_REG register 10b = Invalid configuration 11b = SDO mode follows the ADC controller clock or source-synchronous protocol

(1) This bit takes effect **only** in the ADC controller clock or source-synchronous mode of operation.

7.1.5 DATAOUT_CTL_REG Register (address = 10h)

This register controls the data output by the device.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 10h, 11h, 12h, and 13h, respectively.

図 7-5. DATAOUT_CTL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DEVICE_ADDR_INCL	VDD_ACTIVE_ALARM_INCL[1:0]		IN_ACTIVE_ALARM_INCL[1:0]		Reserved	RANGE_INCL	Reserved				PAR_EN	DATA_VAL[2:0]		
R-0b	R/W-0b	R/W-0b		R/W-0b		R-0b	R/W-0b	R-0000b				R/W-<0>b	R/W-000b		

表 7-7. DATAOUT_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15	Reserved	R	0b	Reserved. Reads return 0b.
14	DEVICE_ADDR_INCL	R/W	0b	Control to include the 4-bit DEVICE_ADDR register value in the SDO-x output bit stream. 0b = Do not include the register value 1b = Include the register value
13-12	VDD_ACTIVE_ALARM_INCL[1:0]	R/W	00b	Control to include the active VDD ALARM flags in the SDO-x output bit stream. 00b = Do not include 01b = Include ACTIVE_VDD_H_FLAG 10b = Include ACTIVE_VDD_L_FLAG 11b = Include both flags
11-10	IN_ACTIVE_ALARM_INCL[1:0]	R/W	00b	Control to include the active input ALARM flags in the SDO-x output bit stream. 00b = Do not include 01b = Include ACTIVE_IN_H_FLAG 10b = Include ACTIVE_IN_L_FLAG 11b = Include both flags
9	Reserved	R	0b	Reserved. Reads return 0h.
8	RANGE_INCL	R/W	0b	Control to include the 4-bit input range setting in the SDO-x output bit stream. 0b = Do not include the range configuration register value 1b = Include the range configuration register value
7-4	Reserved	R	0000b	Reserved. Reads return 0000b.
3	PAR_EN(1)	R/W	0b	0b = Output data does not contain parity information 1b = Two parity bits (ADC output and output data frame) are appended to the LSBs of the output data The ADC output parity bit reflects an even parity for the ADC output bits only. The output data frame parity bit reflects an even parity signature for the entire output data frame. This signature includes the ADC output bits and any internal flags or register settings. The ADC output parity bit is not included in the frame parity bit computation.
2-0	DATA_VAL[2:0]	R/W	000b	These bits control the data value output by the converter. 0xxb = Value output is the conversion data 100b = Value output is all 0's 101b = Value output is all 1's 110b = Value output is alternating 0's and 1's 111b = Value output is alternating 00's and 11's

(1) Setting this bit increases the length of the output data by two bits.

7.1.6 RANGE_SEL_REG Register (address = 14h)

This register controls the configuration of the internal reference and input voltage ranges for the converter.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 14h, 15h, 16h, and 17h, respectively.

図 7-6. RANGE_SEL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Reserved	INTREF_ DIS	Reserved		RANGE_SEL[3:0]			
R-00h								R-0b	R/W-0b	R-00b		R/W-<0000>b			

表 7-8. RANGE_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	Reserved	R	00h	Reserved. Reads return 00h.
7	Reserved	R	0b	Reserved. Reads return 0b.
6	INTREF_DIS	R/W	0b	Control to disable the ADC internal reference. 0b = Internal reference is enabled 1b = Internal reference is disabled
5-4	Reserved	R	00b	Reserved. Reads return 00b.
3-0	RANGE_SEL[3:0]	R/W	0000b	These bits comprise the 4-bit register that selects the nine input ranges of the ADC. 0000b = ±3V × V_{REF} 0001b = ±2.5V × V_{REF} 0010b = ±1.5V × V_{REF} 0011b = ±1.25V × V_{REF} 0100b = ±0.625V × V_{REF} 1000b = 3V × V_{REF} 1001b = 2.5V × V_{REF} 1010b = 1.5V × V_{REF} 1011b = 1.25V × V_{REF}

7.1.7 ALARM_REG Register (address = 20h)

This register contains the output alarm flags (active and tripped) for the input and AVDD alarm.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 20h, 21h, 22h, and 23h, respectively.

図 7-7. ALARM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVE_VDD_L_FLAG	ACTIVE_VDD_H_FLAG	Reserved		ACTIVE_IN_L_FLAG	ACTIVE_IN_H_FLAG	Reserved		TRP_VDD_L_FLAG	TRP_VDD_H_FLAG	TRP_IN_L_FLAG	TRP_IN_H_FLAG	Reserved			OVW_ALARM
R-0b	R-0b	R-00b		R-0b	R-0b	R-00b		R-0b	R-0b	R-0b	R-0b	R-000b			R-0b

表 7-9. ALARM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15	ACTIVE_VDD_L_FLAG	R	0b	Active ALARM output flag for low AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
14	ACTIVE_VDD_H_FLAG	R	0b	Active ALARM output flag for high AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
13-12	Reserved	R	00b	Reserved. Reads return 00b.
11	ACTIVE_IN_L_FLAG	R	0b	Active ALARM output flag for low input voltage. 0b = No ALARM condition 1b = ALARM condition exists
10	ACTIVE_IN_H_FLAG	R	0b	Active ALARM output flag for high input voltage. 0b = No ALARM condition 1b = ALARM condition exists
9-8	Reserved	R	00b	Reserved. Reads return 00b.
7	TRP_VDD_L_FLAG	R	0b	Tripped ALARM output flag for low AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
6	TRP_VDD_H_FLAG	R	0b	Tripped ALARM output flag for high AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
5	TRP_IN_L_FLAG	R	0b	Tripped ALARM output flag for low input voltage. 0b = No ALARM condition 1b = ALARM condition exists
4	TRP_IN_H_FLAG	R	0b	Tripped ALARM output flag for high input voltage. 0b = No ALARM condition 1b = ALARM condition exists
3-1	Reserved	R	000b	Reserved. Reads return 000b.
0	OVW_ALARM	R	0b	Logical OR outputs all tripped ALARM flags. 0b = No ALARM condition 1b = ALARM condition exists

7.1.8 ALARM_H_TH_REG Register (address = 24h)

This register controls the hysteresis and high threshold for the input alarm.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 24h, 25h, 26h, and 27h, respectively.

図 7-8. ALARM_H_TH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INP_ALRM_HYST[1:0]		Reserved													
R/W-0h		R-000h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INP_ALRM_HIGH_TH[11:0]												Reserved			
R/W-FFFh												R-0h			

表 7-10. ALARM_H_TH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	INP_ALRM_HYST[1:0]	R/W	0h	2-bit hysteresis value for the input ALARM.
29-16	Reserved	R	000h	Reserved. Do not modify from reset value.
15-4	INP_ALRM_HIGH_TH[11:0]	R/W	FFFh	12-bit threshold for comparison.
3-0	Reserved	R	0h	Reserved. Do not modify from reset value.

7.1.9 ALARM_L_TH_REG Register (address = 28h)

This register controls the low threshold for the input alarm.

The address for bits 7-0, 15-8, 23-16, and 31-24 is 28h, 29h, 2Ah, and 2Bh, respectively.

図 7-9. ALARM_L_TH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INP_ALRM_LOW_TH[11:0]												Reserved			
R/W-000h												R-0h			

表 7-11. ALARM_L_TH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
32:16	Reserved	R	0000h	Reserved. Do not modify from reset value.
15-4	INP_ALRM_LOW_TH[11:0]	R/W	000h	These bits are the threshold for comparison.
3:0	Reserved	R	0000h	Reserved. Do not modify from reset value.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADS8661W is a fully integrated, fully differential input, data acquisition (DAQ) device based on a 16-bit successive approximation (SAR) analog-to-digital converter (ADC). The device includes an integrated analog front-end (AFE) circuit to drive the inputs of the ADC and an integrated precision reference with a buffer. As such, these devices do not require any additional external circuits for driving the reference or analog input pins of the ADC.

8.2 Typical Application

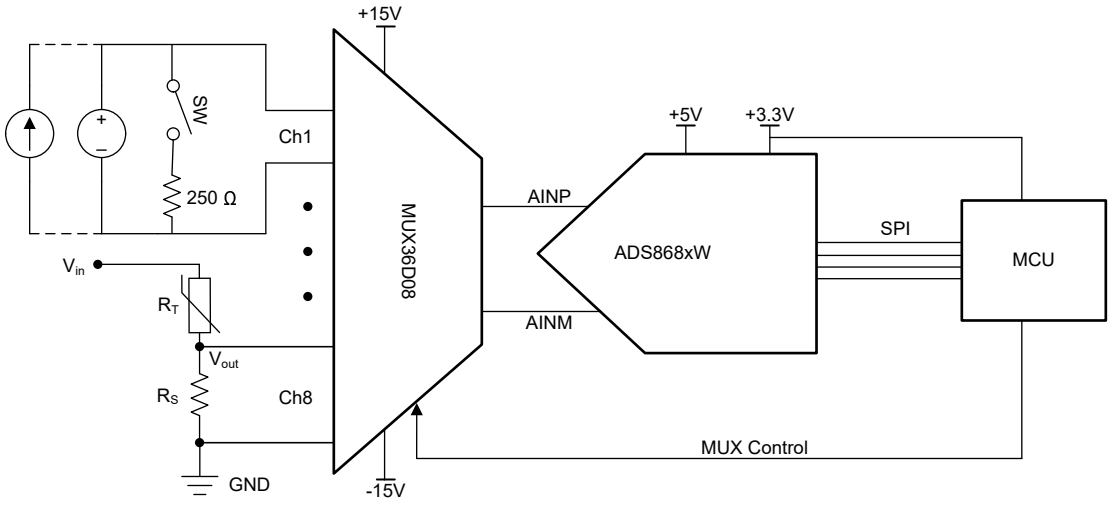


図 8-1. 16-Bit, 8-Channel, Analog Input Module for Programmable Logic Controllers (PLCs)

8.2.1 Design Requirements

This section describes using the ADS8661W in an industrial analog input module. This design is an example of a process control end equipment that digitizes standard bipolar or unipolar industrial inputs with input ranges up to ±10V. Programmable logic controllers (PLCs), distributed control systems (DCS), or data acquisition systems (DAS) modules are end equipment examples. The analog voltage and current ranges typically include ±2.5V, ±5V, ±10V, 0V to 5V, 0V to 10V, 4mA to 20mA, and 0mA to 20mA. These ranges are for an industrial environment. This reference design measures all standard industrial voltage and current inputs. Eight channels are provided on the module, and each channel is configured as a current or voltage input with software configuration.

表 8-1 lists the parameters for this design.

表 8-1. Design Parameters

PARAMETER	VALUE
Fast settling time for quick channel switching	5µs at 1% accuracy
Fully differential amplifier channels with user programmable inputs	Up to eight channels
Voltage inputs (typical Z_{IN} = 1MΩ)	±12V

表 8-1. Design Parameters (続き)

PARAMETER	VALUE
16-bit SAR ADC	3.3V digital output lines

8.2.2 Detailed Design Procedure

This design combines the single-channel, 16-bit ADS8661W SAR ADC with the eight-channel MUX36D08 differential multiplexer. The ADS8661W provides the fast-settling, high-bandwidth performance necessary to support an external discrete multiplexer for responsive channel-to-channel operation.

The ADS8661W is settles to 1% accuracy at under 5µs (図 8-2) because of the device high-bandwidth input of up to 400kHz at −3dB. The ADS8661W also includes an internal programmable gain amplifier, ADC driver, and reference. Thus, making the device incredibly simple to connect a signal with an amplitude of up to ±12.288V on a single analog supply. This device also includes a variety of safety features, such as overvoltage protection, an input alarm, and AVDD alarm.

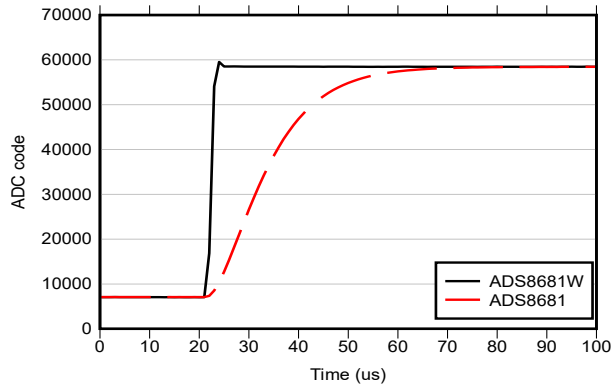


図 8-2. Step Settling Response Time

The MUX36D08 is a differential multiplexer. This multiplexer enables using up to eight differential inputs to perform fast and accurate voltage, current, or temperature sensing across a wide input voltage range. This device accepts three digital control lines to select the analog inputs.

The ADS8661W interfaces with a controller through an enhanced SPI communication protocol, simplifying the controller speed requirements. Overall, this system simplifies connecting a wide range of single-ended or differential signals, and includes features to safely monitor these signals in an industrial environment.

8.2.3 Application Curve

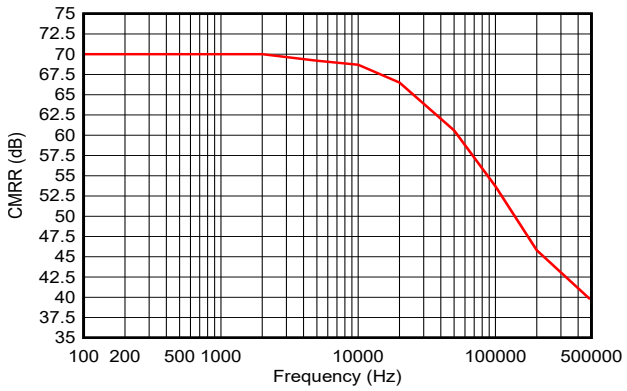


図 8-3. Common-Mode Rejection Ratio vs Frequency

8.3 Power Supply Recommendations

The device uses two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD and DVDD is used for the digital interface. Independently set AVDD and DVDD to any value within the permissible range.

8.3.1 Power Supply Decoupling

Decouple the AVDD supply pins with AGND by using a minimum 10µF and 1µF capacitor on each supply. Place the 1µF capacitor as close to the supply pins as possible. Place a minimum 10µF decoupling capacitor very close to the DVDD supply to provide the high-frequency digital switching current. The effect of using the decoupling capacitor is illustrated in the difference between the power-supply rejection ratio (PSRR) performance of the device. 図 8-4 shows the PSRR of the device without using a decoupling capacitor. As shown in 図 8-5, the PSRR improves when the decoupling capacitors are used.

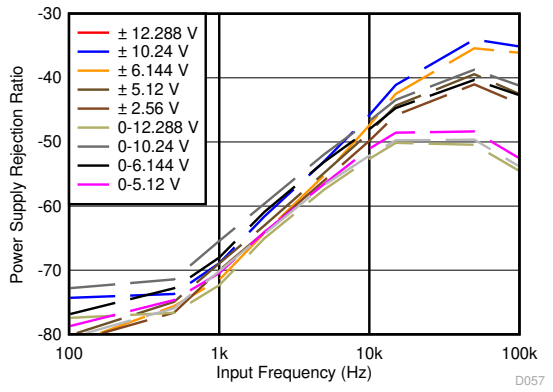


図 8-4. PSRR Without a Decoupling Capacitor

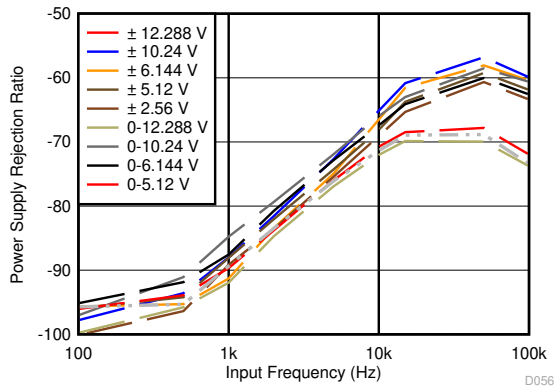


図 8-5. PSRR With a Decoupling Capacitor

8.3.2 Power Saving

In normal mode of operation, the device does not power down between conversions, and therefore achieves high throughput. However, the device offers two programmable low-power modes: NAP and power-down (PD) to reduce power consumption when the device operates at lower throughput rates.

8.3.2.1 NAP Mode

In NAP mode, the device internal blocks are placed into a low-power mode to reduce the overall device power consumption in ACQ state.

To enable NAP mode:

- Write 69h to register address 05h to unlock the RST_PWRCTL_REG register.
- Set the NAP_EN bit in the RST_PWRCTL_REG register to 1b. Keep the CONVST/$\overline{CS}$ pin high at the end of the conversion process. The device then enters NAP mode at the end of conversion and remains in NAP mode as long as the CONVST/$\overline{CS}$ pin is held high.

A falling edge on the CONVST/$\overline{CS}$ brings the device out of NAP mode. However, the host controller initiates a new conversion (CONVST/$\overline{CS}$ rising edge) only after the t_{NAP_WKUP} time has elapsed (see the *Switching Characteristics* table).

8.3.2.2 Power-Down (PD) Mode

The device also features a deep power-down mode (PD) to reduce the power consumption at very low throughput rates.

Complete the following steps to enter PD mode:

1. Write 69h to register address 05h to unlock the RST_PWRCTL_REG register.
2. Set the PWRDN bit in the RST_PWRCTL_REG register to 1b. The device enters PD mode on the rising edge of the CONVST/$\overline{CS}$ signal.

In PD mode, all analog blocks within the device are powered down. However, the interface remains active and the register contents are also retained. The RVS pin is high, indicating that the device is ready to receive the next command.

To exit PD mode:

1. Clear the PWRDN bit in the RST_PWRCTL_REG register to 0b.
2. The RVS pin goes high, indicating that the device has started coming out of PD mode. However, the host controller waits for the t_{PWRUP} time (see the *Switching Characteristics* table) to elapse before initiating a new conversion.

8.4 Layout

8.4.1 Layout Guidelines

図 8-6 illustrates a PCB layout example for the ADS8661W with a single-ended input configuration and AINM connected to GND.

- Partition the PCB into analog and digital sections. Make sure the analog signals are kept away from the digital lines. This layout helps keep the analog input and reference input signals away from the digital noise. In this layout example, the analog input and reference signals are routed on the lower side of the board. Additionally, the digital connections are routed on the top side of the board.
- Use a single dedicated ground plane.
- Make sure power sources to the ADS8661W are clean and well-bypassed. Use a 1µF, X7R-grade, 0603-size ceramic capacitor with at least a 10V rating in close proximity to the analog (AVDD) supply pins. For decoupling the digital supply pin (DVDD), use a 1µF, X7R-grade, 0603-size ceramic capacitor with at least a 10V rating. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane with short, low-impedance paths.
- There are two decoupling capacitors used for the REFCAP pin. The first is a small, 1µF, 0603-size ceramic capacitor placed close to the device pins for decoupling the high-frequency signals. The second is a 10µF, 0805-size ceramic capacitor to provide the charge required by the reference circuit of the device. Use a capacitor with an ESR less than 0.2Ω for the 10µF capacitor. Directly connect both capacitors to the device pins without any vias between the pins and capacitors.
- Decouple the REFIO pin with a minimum of 4.7µF ceramic capacitor if the internal reference of the device is used. Place the capacitor close to the device pins.

8.4.2 Layout Example

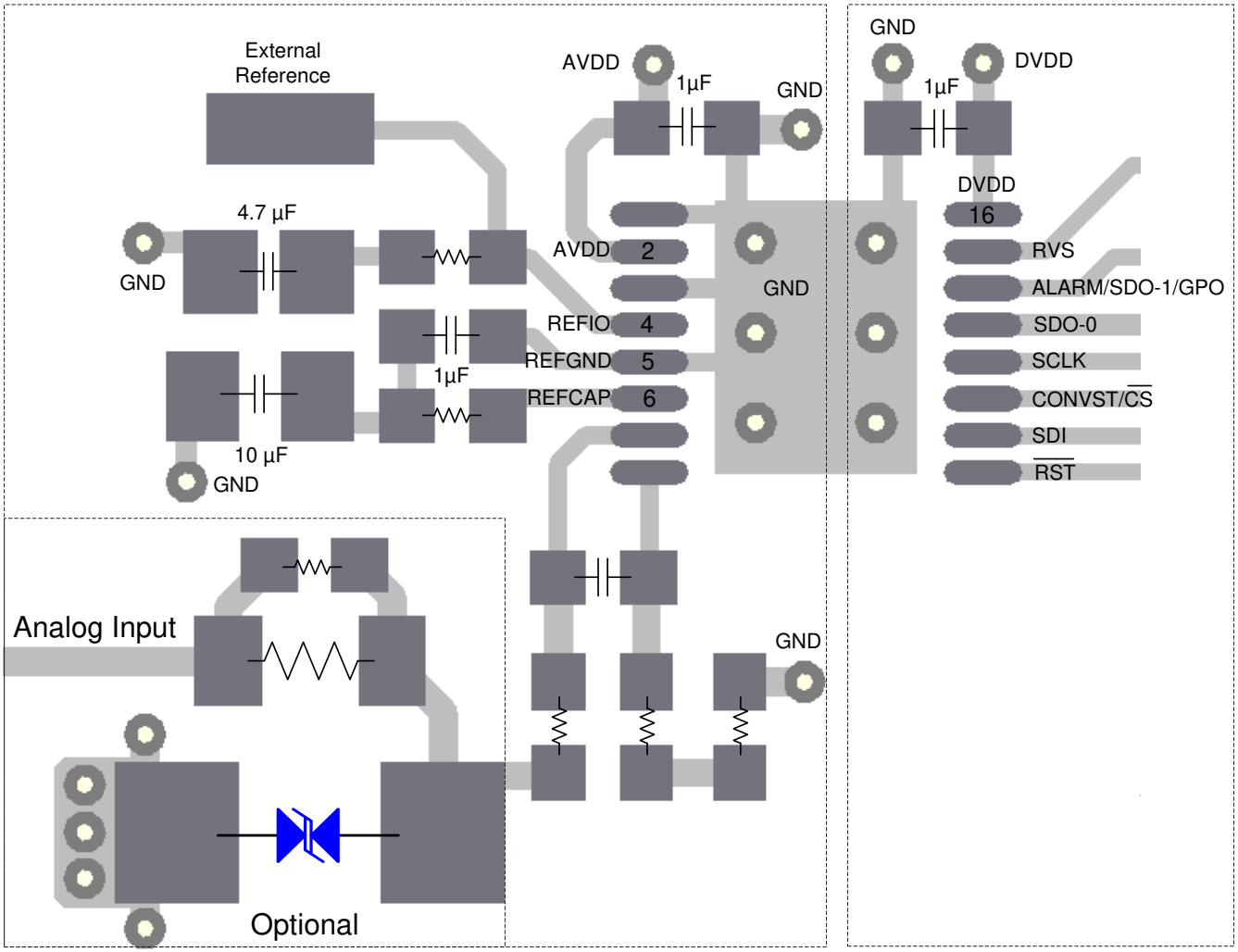


図 8-6. Board Layout for the ADS8661W

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA320 Precision, 20MHz, 0.9pA, Low-Noise, RRIO, CMOS Operational Amplifier with Shutdown* data sheet
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *TPS7A49 36-V, 150-mA, Ultralow-Noise, Positive Linear Regulator* data sheet
- Texas Instruments, *ISO764xFM Low-Power Quad-Channel Digital Isolators* data sheet
- Texas Instruments, *AN-2029 Handling and Process Recommendations* application note

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8661WRUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD8661W
ADS8661WRUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD8661W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

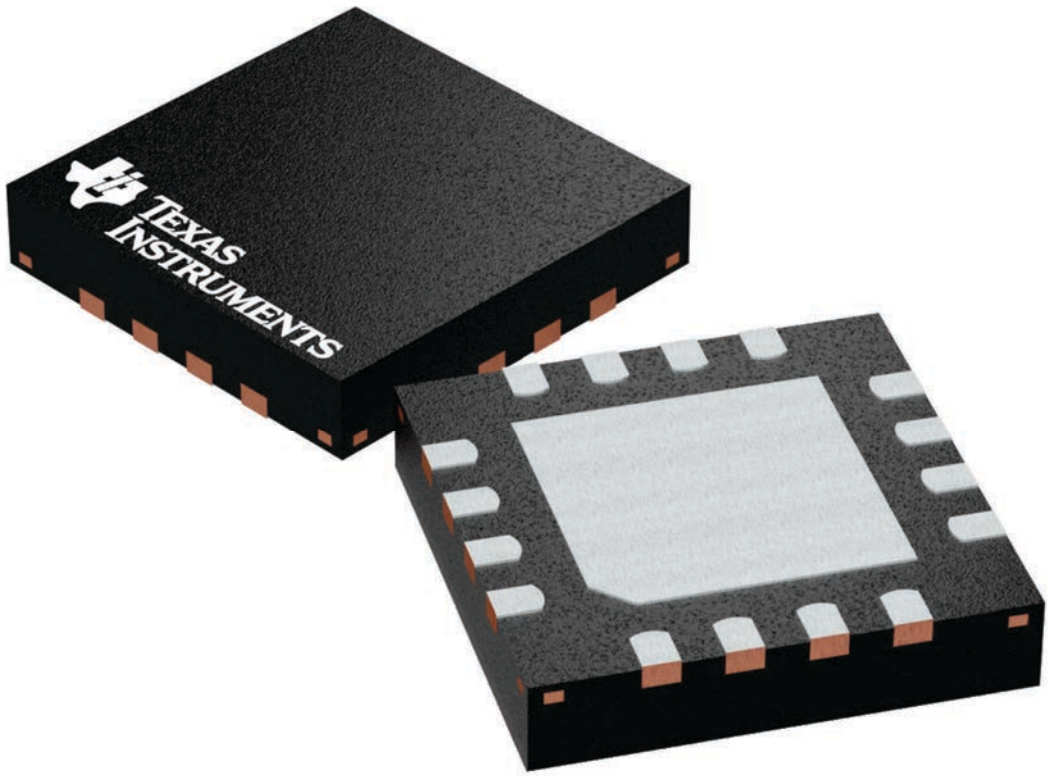
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

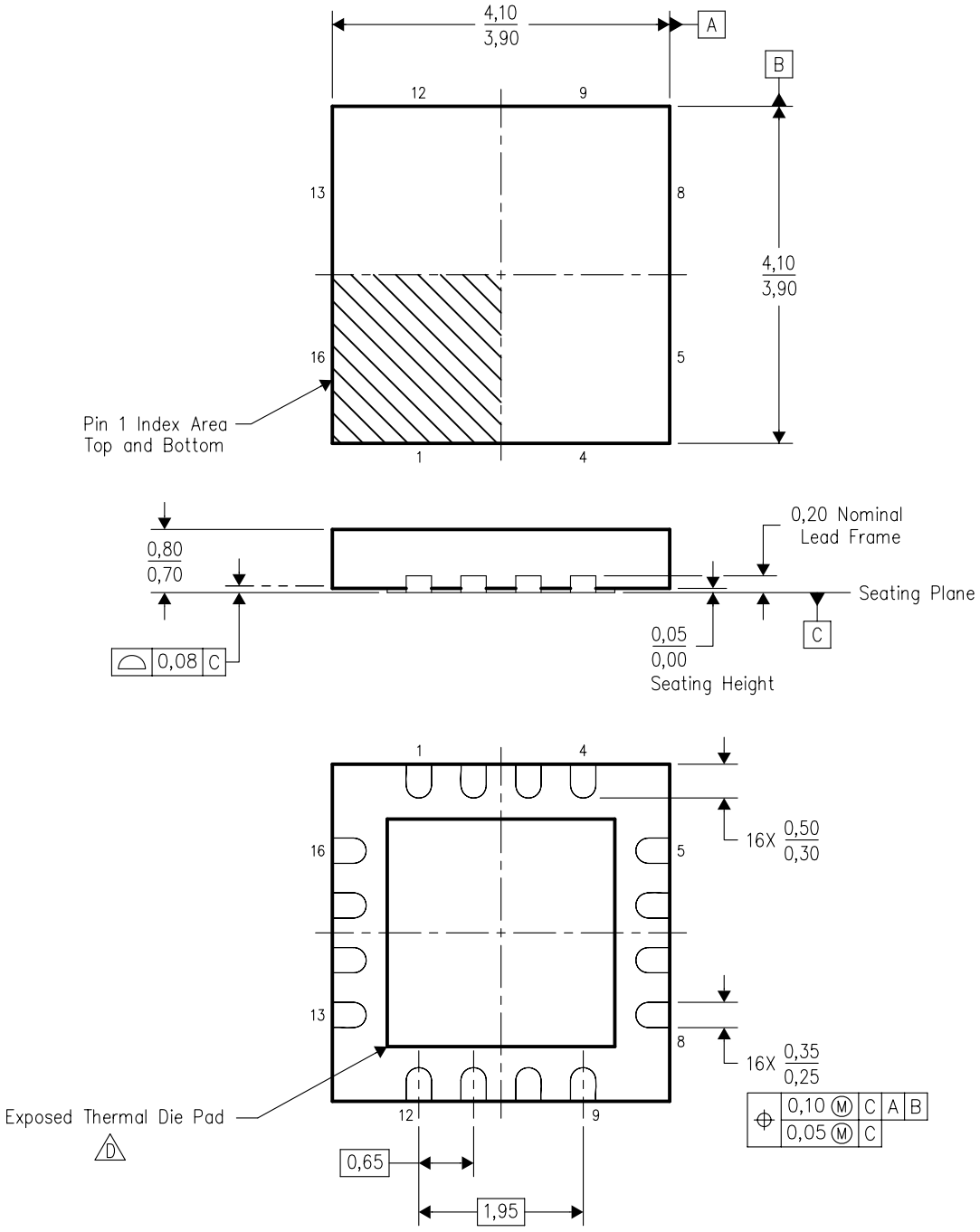
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224843/A

RUM (S–PQFP–N16) PLASTIC QUAD FLATPACK



4209092/A 10/2007

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation WGGC–3.

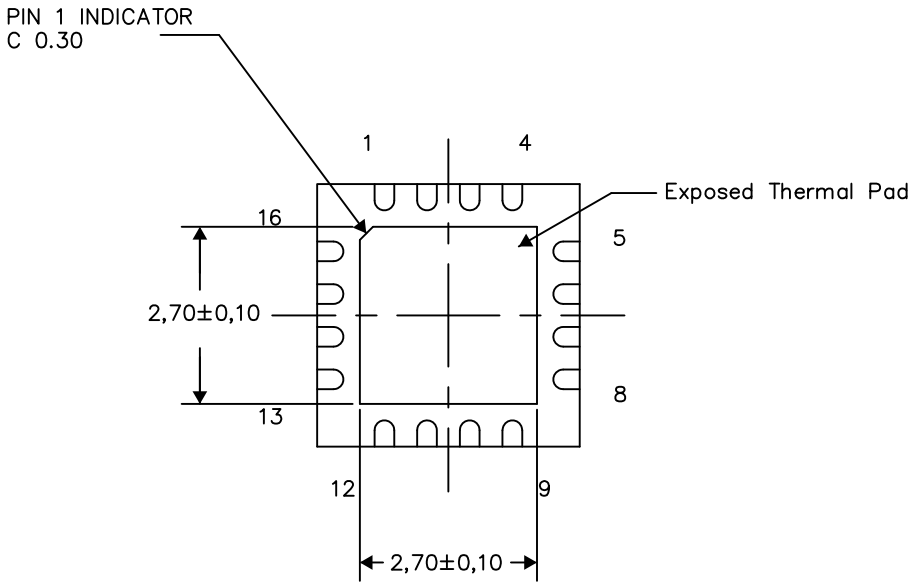
RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209093–2/F 09/15

NOTES: All linear dimensions are in millimeters

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