ADS54J20
2チャネル、12ビット、1.0GSPS、A/Dコンバータ

1 特長

- 12ビットの分解能、2チャネル、1GSPS ADC
- ノイズ・フロア: –157dBFS/Hz
- スペクトラム性能(f_{IN} = 170MHz、–1dBFS時)
  - SNR: 67.8dBFS
  - NSD: –155dBFS/Hz
  - SFDR: 86dBc (インターリーブ・トーンを含む)
  - SFDR: 89dBc (HD2、HD3、およびインターリーブ・トーンを除く)
- スペクトラム性能(f_{IN} = 350MHz、–1dBFS時)
  - SNR: 65.6dBFS
  - NSD: –152.6dBFS/Hz
  - SFDR: 75dBc
  - SFDR: 85dBc (HD2、HD3、およびインターリーブ・トーンを除く)
- チャネル分離: f_{IN} = 170MHzのとき100dBc
- 入力フル・スケール: $1.9V_{PP}$
- 入力帯域幅(3dB): 1.2GHz
- オンチップ・ディザリング
- 広帯域DDCブロックを搭載
- サブクラス1をサポートするJESD204Bインターフェイス
  - 10.0Gbpsで、ADCごとに2レーン
  - 5.0Gbpsで、ADCごとに4レーン
  - マルチチップの同期をサポート
- 消費電力: 1GSPSのとき1.35W/Ch
- パッケージ: 72ピンVQFNP (10mm×10mm)

2 アプリケーション

- レーダーおよびアンテナ・アレイ
- 広帯域ワイヤレス
- ケーブルCMTS、DOCSIS 3.1レシーバ
- 通信テスト機器
- マイクロ波受信機
- ソフトウェア定義ラジオ(SDR)
- デジタイザ
- 医療用画像処理および診断

3 説明

ADS54J20は低電力で広帯域幅の12ビット、1.0GSPS、2チャネルのA/Dコンバータ(ADC)です。このデバイスは信号対雑音比(SNR)が高くなるよう設計され、ノイズ・フロアで–157dBFS/Hzを実現しており、広い瞬間的帯域幅にわたって最高のダイナミック・レンジを求めるアプリケーションに適しています。デバイスはJESD204Bシリアル・インターフェイスをサポートし、10Gbpsまでのデータ転送速度で、ADCごとに2レーンまたは4レーンをサポートします。アナログ・バッファ入力により、広い周波数帯域にわたって入力インピーダンスが均一で、サンプルとホールドのグリッチ・エネルギーが最小化されます。オプションとして、各ADCチャネルを広帯域のデジタル・ダウン・コンバータ(DDC)ブロックへ接続できます。ADS54J20は、広い入力周波数範囲にわたって、非常に優れたスプリアス・フリー・ダイナミック・レンジ(SFDR)を提供し、消費電力も非常にわずかです。

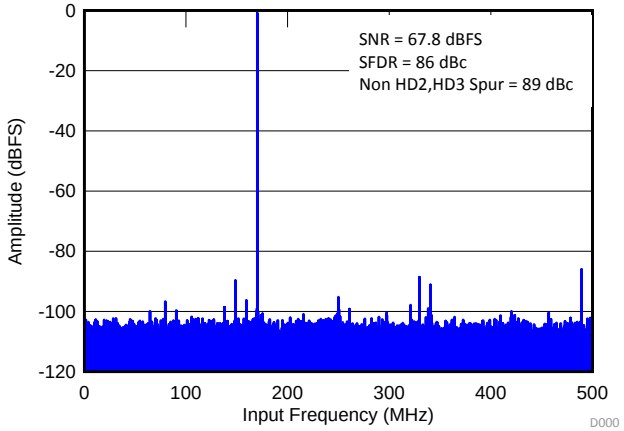
JESD204Bインターフェイスにより、インターフェイス・ラインの数を削減でき、システムの集積密度を高めることができます。内蔵のフェーズ・ロック・ループ(PLL)は、ADCサンプリング・クロックを逓倍して、各チャネルからの12ビット・データをシリアル化するためのビット・クロックを生成します。

製品情報

型番	パッケージ	本体サイズ(公称)
ADS54J20	VQFNP (72)	10.00mm×10.00mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

170MHzの入力信号に対するFFT



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

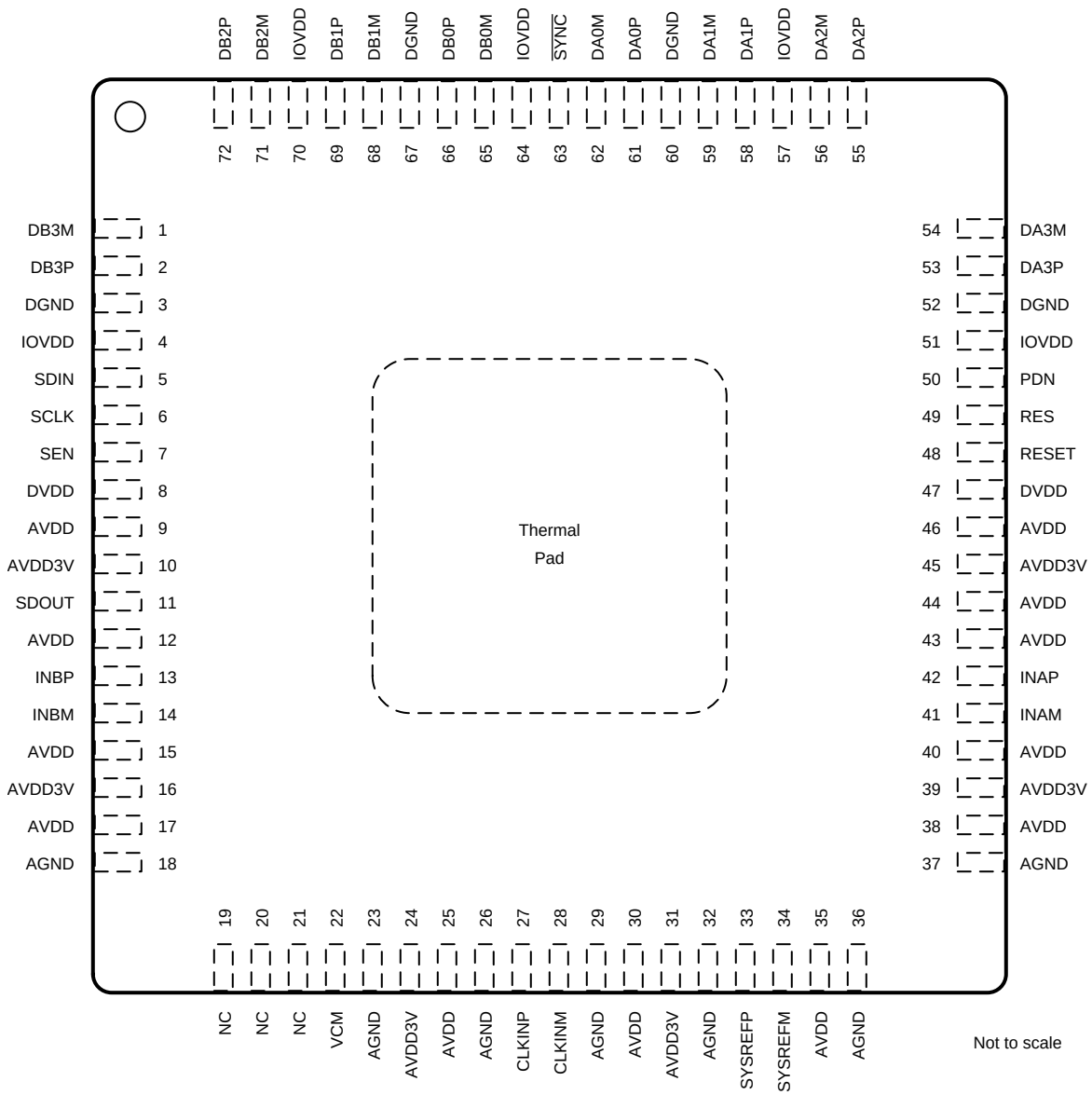
2016年5月発行のものから更新	**Page**
• 量産向けにリリース	1

5 Device Comparison Table

DEVICE	SPEED GRADE (MSPS)	RESOLUTION (Bits)	CHANNEL
ADS54J60	1000	16	Dual
ADS54J40	1000	14	Dual
ADS54J42	625	14	Dual
ADS54J20	1000	12	Dual
ADS54J69	500	16	Dual

6 Pin Configuration and Functions

RMP Package
72-Pin VQFNP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK, SYSREF			
CLKINM	28	I	Negative differential clock input for the ADC
CLKINP	27	I	Positive differential clock input for the ADC
SYSREFM	34	I	Negative external SYSREF input
SYSREFP	33	I	Positive external SYSREF input
CONTROL, SERIAL			
PDN	50	I/O	Power-down. Can be configured via an SPI register setting. Can be configured as a fast overrange output for channel A via the SPI.
RESET	48	I	Hardware reset; active high. This pin has an internal 20-kΩ pulldown resistor.
SCLK	6	I	Serial interface clock input
SDIN	5	I	Serial interface data input
SDOUT	11	O	Serial interface data output. Can be configured as a fast overrange output for channel B via the SPI.
SEN	7	I	Serial interface enable
DATA INTERFACE			
DA0M	62	O	JESD204B serial data negative output for channel A
DA1M	59	O	
DA2M	56	O	
DA3M	54	O	
DA0P	61	O	JESD204B serial data positive output for channel A
DA1P	58	O	
DA2P	55	O	
DA3P	53	O	
DB0M	65	O	JESD204B serial data negative output for channel B
DB1M	68	O	
DB2M	71	O	
DB3M	1	O	
DB0P	66	O	JESD204B serial data positive output for channel B
DB1P	69	O	
DB2P	72	O	
DB3P	2	O	
$\overline{\text{SYNC}}$	63	I	Synchronization input for the JESD204B port
INPUT, COMMON MODE			
INAM	41	I	Differential analog negative input for channel A
INAP	42	I	Differential analog positive input for channel A
INBM	14	I	Differential analog negative input for channel B
INBP	13	I	Differential analog positive input for channel B
VCM	22	O	Common-mode voltage, 2.1 V. Note that analog inputs are internally biased to this pin through 600 Ω (effective), no external connection from the VCM pin to the INxP or INxM pin is required.
POWER SUPPLY			
AGND	18, 23, 26, 29, 32, 36, 37	I	Analog ground
AVDD	9, 12, 15, 17, 25, 30, 35, 38, 40, 43, 44, 46	I	Analog 1.9-V power supply
AVDD3V	10, 16, 24, 31, 39, 45	I	Analog 3.0-V power supply for the analog buffer
DGND	3, 52, 60, 67	I	Digital ground
DVDD	8, 47	I	Digital 1.9-V power supply
IOVDD	4, 51, 57, 64, 70	I	Digital 1.15-V power supply for the JESD204B transmitter
NC, RES			
NC	19, 20, 21	—	Unused pin, do not connect
RES	49	I	Reserved pin. Connect to DGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	
	DVDD	–0.3	2.1	
	IOVDD	–0.2	1.4	
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3	3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3	
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3	
	SCLK, SEN, SDIN, RESET, $\overline{\text{SYNC}}$, PDN	–0.2	2.1	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	NOM	MAX	UNIT
Supply voltage range	AVDD3V		2.85	3.0	3.6	V
	AVDD		1.8	1.9	2.0	
	DVDD		1.7	1.9	2.0	
	IOVDD		1.1	1.15	1.2	
Analog inputs	Differential input voltage range			1.9		V_{PP}
	Input common-mode voltage			2.0		V
	Maximum analog input frequency for a 1.9-V_{PP} input amplitude(3)(4)			400		MHz
Clock inputs	Input clock frequency, device clock frequency		250(5)		1000	MHz
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.75	1.5		V_{PP}
		LVPECL, ac-coupled	0.8	1.6		
		LVDS, ac-coupled		0.7		
	Input device clock duty cycle		45%	50%	55%	
Temperature	Operating free-air, T_A		–40		85	°C
	Operating junction, T_J			105(6)	125	

(1) SYSREF must be applied for the device to initialize; see the *SYSREF Signal* section for details.
(2) After power-up, always use a hardware reset to reset the device for the first time; see Table 66 for details.
(3) Operating 0.5 dB below the maximum-supported amplitude is recommended to accommodate gain mismatch in interleaving ADCs.
(4) At high frequencies, the maximum supported input amplitude reduces; see Figure 36 for details.
(5) See Table 9 and Table 11.
(6) Prolonged use above the nominal junction temperature can increase the device failure-in-time (FIT) rate.

7.4 Thermal Information

THERMAL METRIC(1)		ADS54J20 RMP (VQFNP) 72 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
	ADC sampling rate				1000	MSPS
	Resolution		12			Bits
POWER SUPPLIES						
AVDD3V	3.0-V analog supply		2.85	3.0	3.6	V
AVDD	1.9-V analog supply		1.8	1.9	2.0	V
DVDD	1.9-V digital supply		1.7	1.9	2.0	V
IOVDD	1.15-V SerDes supply		1.1	1.15	1.2	V
I_{AVDD3V}	3.0-V analog supply current	V_{IN} = full-scale on both channels		334	360	mA
I_{AVDD}	1.9-V analog supply current	V_{IN} = full-scale on both channels		359	510	mA
I_{DVDD}	1.9-V digital supply current	8 lanes active (LMFS = 8224)		197	260	mA
		4 lanes active (LMFS = 4222), 2X decimation		197		mA
		2 lanes active (LMFS = 2221), 4X decimation		176		mA
I_{IOVDD}	1.15-V SerDes supply current	8 lanes active (LMFS = 8224)		566	920	mA
		4 lanes active (LMFS = 4222), 2X decimation		593		mA
		2 lanes active (LMFS = 2221), 4X decimation		562		mA
P_D	Total power dissipation(1)	8 lanes active (LMFS = 8224)		2.71	3.1	W
		4 lanes active (LMFS = 4222), 2X decimation		2.74		W
		2 lanes active (LMFS = 2221), 4X decimation		2.66		W
	Global power-down power dissipation			139	315	mW
ANALOG INPUTS (INAP, INAM, INBP, INBM)						
	Differential input full-scale voltage			1.9		V_{PP}
V_{IC}	Common-mode input voltage			2.0		V
R_{IN}	Differential input resistance	At 170-MHz input frequency		0.6		kΩ
C_{IN}	Differential input capacitance	At 170-MHz input frequency		4.7		pF
	Analog input bandwidth (3 dB)	50-Ω source driving ADC inputs terminated with 50 Ω		1.2		GHz
CLOCK INPUT (CLKINP, CLKINM)						
	Internal clock biasing	CLKINP and CLKINM are connected to internal biasing voltage through 400 Ω		1.15		V

(1) See the *Power-Down Mode* section for details.

7.6 AC Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input amplitude, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			68.4		dBFS
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			68.3		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		64	67.8		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			67.4		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			67.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			66.7		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			65.8		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			66.3		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		65.5		
			A_{IN} = –6 dBFS, gain = 5 dB		61.5		
NSD	Noise spectral density	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			155.4		dBFS/Hz
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			155.3		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		151	154.8		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			154.4		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			154.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			153.7		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			152.8		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			153.3		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		152.5		
			A_{IN} = –6 dBFS, gain = 5 dB		148.5		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			68.3		dBFS
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			68.1		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		63.2	67.7		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			67.2		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			66.7		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			66.3		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			65.0		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			65.7		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		64.7		
			A_{IN} = –6 dBFS, gain = 5 dB		60.8		
SFDR	Spurious-free dynamic range (excluding IL spurs)	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			85.0		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			83.0		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		74	86.0		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			85.0		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			81.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			78.0		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			73.0		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			72.0		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		68.0		
			A_{IN} = –6 dBFS, gain = 5 dB		69.0		

AC Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input amplitude, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			85.0		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			90.0		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		74	92.0		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			85.0		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			81.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			81.0		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			76.0		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			72.0		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		68.0		
			A_{IN} = –6 dBFS, gain = 5 dB		69.0		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			85.0		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			83.0		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		74	86.0		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			87.0		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			81.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			78.0		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			73.0		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			70.0		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		77.0		
			A_{IN} = –6 dBFS, gain = 5 dB		79.0		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3, and IL spur)	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			94.0		dBFS
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			97.0		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		77	93.0		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			95.0		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			95.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			91.0		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			85.0		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			88.0		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		80.0		
			A_{IN} = –6 dBFS, gain = 5 dB		83.0		
ENOB	Effective number of bits	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			11.1		Bits
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			11.0		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		10.2	11.0		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			10.9		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			10.8		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			10.7		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			10.5		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			10.6		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		10.5		
			A_{IN} = –6 dBFS, gain = 5 dB		9.8		

AC Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input amplitude, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			82.0		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			80.0		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		72	83.0		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			82.0		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			78.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			75.0		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			70.0		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			71.0		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		67.0		
			A_{IN} = –6 dBFS, gain = 5 dB		69.0		
SFDR_IL	Interleaving spur	f_{IN} = 10 MHz, A_{IN} = –1 dBFS			84.0		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS			85.0		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		69	84.0		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS			83.0		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS			82.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS			81.0		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS			81.0		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS			78.0		
		f_{IN} = 720 MHz	A_{IN} = –6 dBFS		79.0		
			A_{IN} = –6 dBFS, gain = 5 dB		82.0		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, A_{IN} = –7 dBFS			85		dBFS
		f_{IN1} = 365 MHz, f_{IN2} = 370 MHz, A_{IN} = –7 dBFS			79		
		f_{IN1} = 465 MHz, f_{IN2} = 470 MHz, A_{IN} = –7 dBFS			75		
	Crosstalk isolation between channel A and B	Full-scale, 170-MHz signal on aggressor, idle channel is victim			100		dB

7.7 Digital Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, $\overline{\text{SYNC}}$, PDN)(1)						
V_{IH}	High-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels	0.8			V
V_{IL}	Low-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		µA
		RESET, SCLK, SDIN, PDN, $\overline{\text{SYNC}}$		50		
I_{IL}	Low-level input current	SEN		50		µA
		RESET, SCLK, SDIN, PDN, $\overline{\text{SYNC}}$		0		
DIGITAL INPUTS (SYSREFP, SYSREFM)						
V_D	Differential input voltage		0.35	0.45	1.4	V
$V_{(CM\_DIG)}$	Common-mode voltage for SYSREF(2)			1.3		V
DIGITAL OUTPUTS (SDOUT, PDN(2))						
V_{OH}	High-level output voltage		DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)(3)						
V_{OD}	Output differential voltage	With default swing setting		700		mV_{PP}
V_{OC}	Output common-mode voltage			450		mV
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) The RESET, SCLK, SDIN, and PDN pins have a 20-kΩ (typical) internal pulldown resistor to ground, and the SEN pin has a 20-kΩ (typical) pullup resistor to IOVDD.
(2) When functioning as an OVR pin for channel B.
(3) 100-Ω differential termination.

7.8 Timing Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

		MIN	TYP	MAX	UNITS
SAMPLE TIMING					
	Aperture delay	0.75		1.6	ns
	Aperture delay matching between two channels on the same device		±70		ps
	Aperture delay matching between two devices at the same temperature and supply voltage		±270		ps
	Aperture jitter		120		f_S rms
WAKE-UP TIMING					
	Wake-up time to valid data after coming out of global power-down		150		µs
LATENCY					
	Data latency(1): ADC sample to digital output		134		Input clock cycles
	OVR latency: ADC sample to OVR bit		62		Input clock cycles
t_{PD}	Propagation delay: logic gates and output buffers delay (does not change with f_S)		4		ns
SYSREF TIMING					
t_{SU_SYSREF}	Setup time for SYSREF, referenced to the input clock falling edge	300		900	ps
t_{H_SYSREF}	Hold time for SYSREF, referenced to the input clock falling edge	100			ps
JESD OUTPUT INTERFACE TIMING CHARACTERISTICS					
	Unit interval	100		400	ps
	Serial output data rate	2.5		6.25	Gbps
	Total jitter for BER of 1E-15 and lane rate = 6.25 Gbps		26		ps
	Random jitter for BER of 1E-15 and lane rate = 6.25 Gbps		0.75		ps rms
	Deterministic jitter for BER of 1E-15 and lane rate = 6.25 Gbps		12		ps, pk-pk
t_R, t_F	Data rise time, data fall time: rise and fall times are measured from 20% to 80%, differential output waveform, 2.5 Gbps ≤ bit rate ≤ 6.25 Gbps		35		ps

(1) Overall ADC latency = data latency + t_{PDI}.

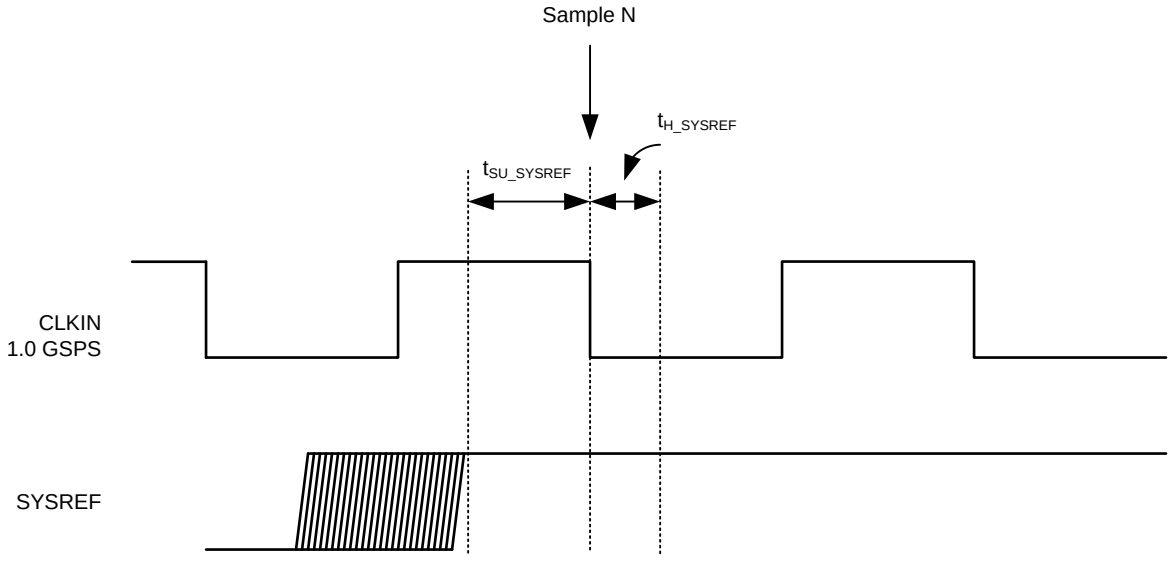


Figure 1. SYSREF Timing

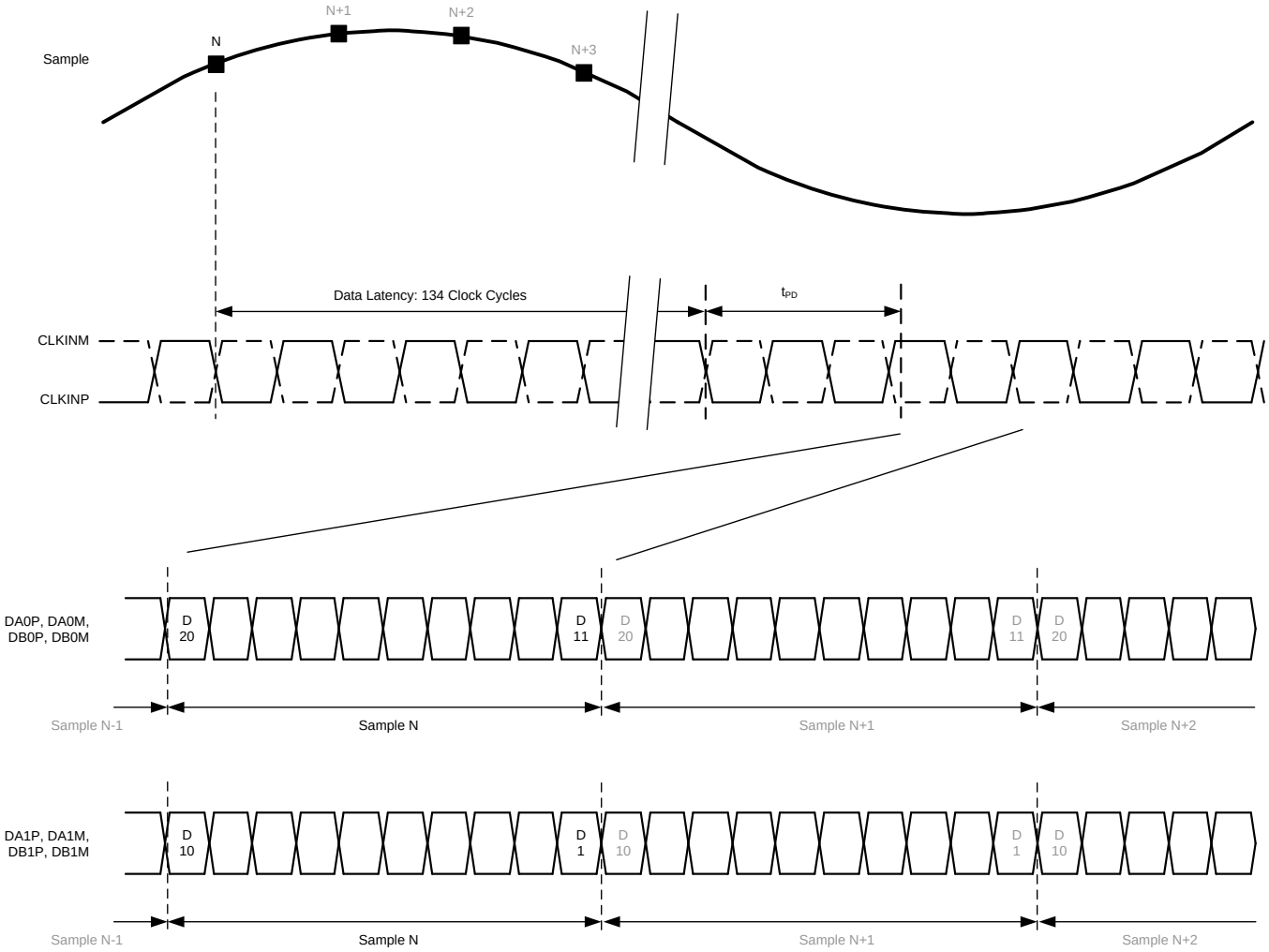
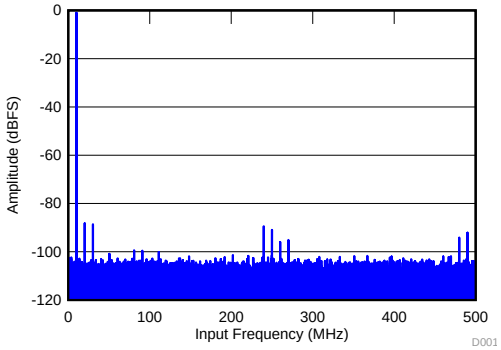


Figure 2. Sample Timing Requirements

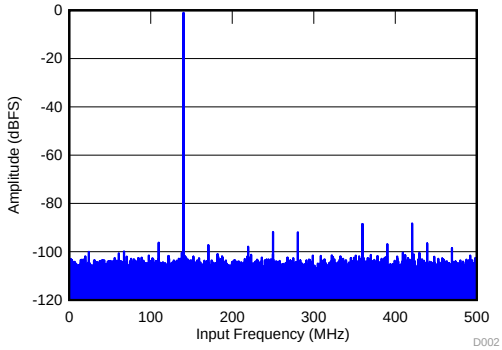
7.9 Typical Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



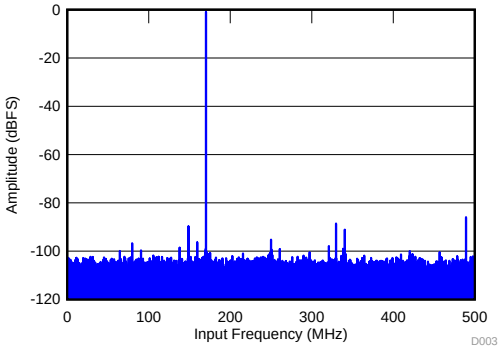
SNR = 68.4 dBFS, SINAD = 68.3 dBFS,
THD = 84 dBc, IL spur = 89 dBc, SFDR = 87 dBc,
non HD2, HD3 spur = 93 dBc

Figure 3. FFT for 10-MHz Input Signal



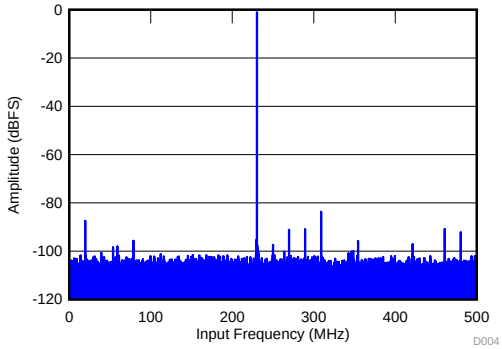
SNR = 67.9 dBFS, SINAD = 67.8 dBFS,
SFDR = 87 dBc, THD = 85 dBc, IL spur = 88 dBc,
non HD2, HD3 spur = 96 dBc

Figure 4. FFT for 140-MHz Input Signal



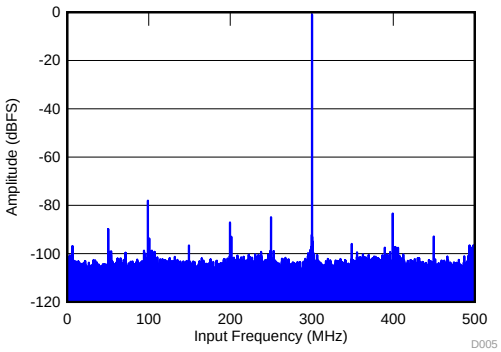
SNR = 67.8 dBFS, SINAD = 67.7 dBFS,
SFDR = 86 dBc, THD = 81 dBc, IL spur = 88 dBc,
non HD2, HD3 spur = 89 dBc

Figure 5. FFT for 170-MHz Input Signal



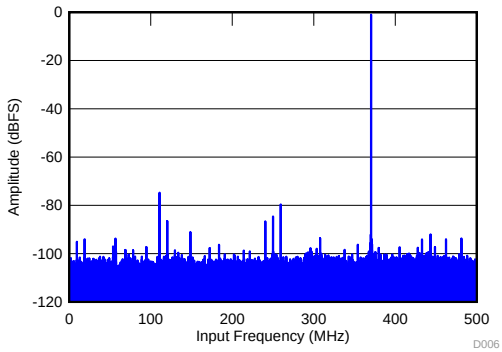
SNR = 67.4 dBFS, SINAD = 67.2 dBFS,
IL spur = 87 dBc, SFDR = 84 dBc, THD = 82 dBc,
non HD2, HD3 spur = 90 dBc

Figure 6. FFT for 230-MHz Input Signal



SNR = 66.7 dBFS, SINAD = 66.3 dBFS,
IL spur = 85 dBc, SFDR = 77 dBc, THD = 76 dBc,
non HD2, HD3 spur = 92 dBc

Figure 7. FFT for 300-MHz Input Signal

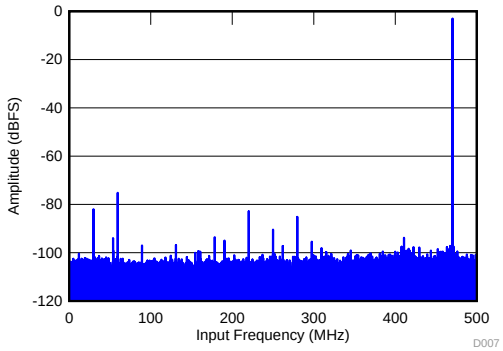


SNR = 65.8 dBFS, SINAD = 65 dBFS,
SFDR = 74 dBc, THD = 72 dBc,
IL spur = 85 dBc, non HD2, HD3 spur = 86 dBc

Figure 8. FFT for 370-MHz Input Signal

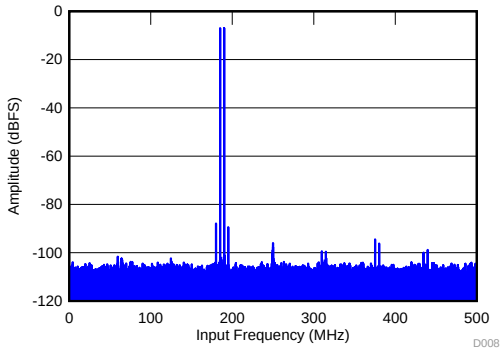
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



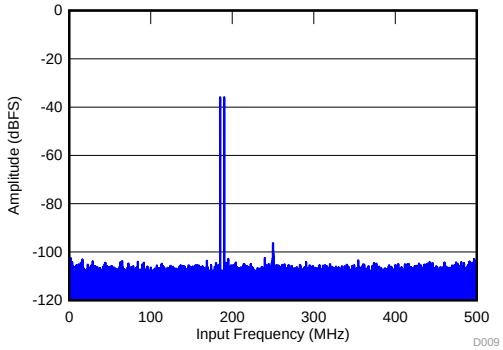
SNR = 66.3 dBFS, SINAD = 65.7 dBFS,
SFDR = 72 dBc, THD = 71 dBc,
IL spur = 81 dBc, non HD2, HD3 spur = 90 dBc

Figure 9. FFT for 470-MHz Input Signal



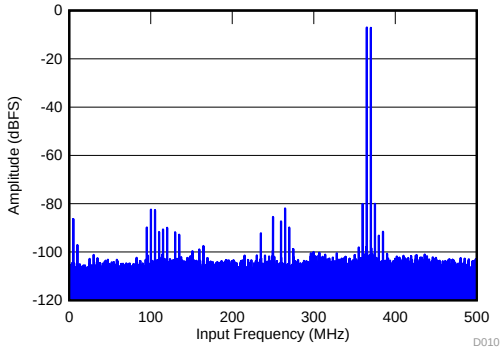
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, each tone at –7 dBFS,
IMD = 85 dBFS

Figure 10. FFT for Two-Tone Input Signal (–7 dBFS)



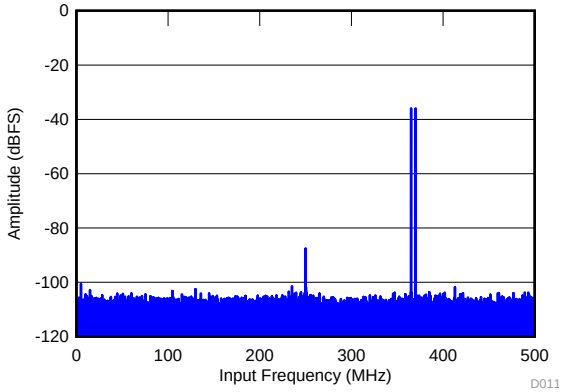
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, each tone at –36 dBFS,
IMD = 103 dBFS

Figure 11. FFT for Two-Tone Input Signal (–36 dBFS)



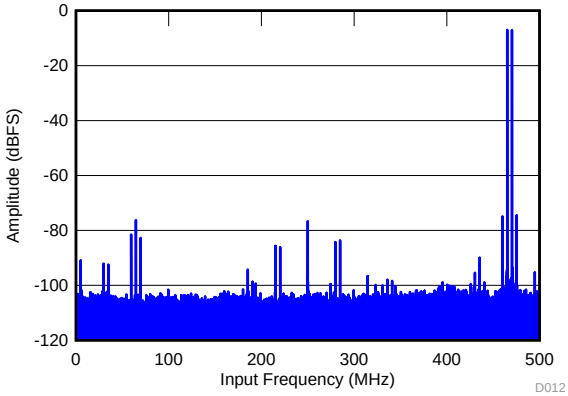
f_{IN1} = 370 MHz, f_{IN2} = 365 MHz, each tone at –7 dBFS,
IMD = 80 dBFS

Figure 12. FFT for Two-Tone Input Signal (–7 dBFS)



f_{IN1} = 370 MHz, f_{IN2} = 365 MHz, each tone at –36 dBFS,
IMD = 109 dBFS

Figure 13. FFT for Two-Tone Input Signal (–36 dBFS)

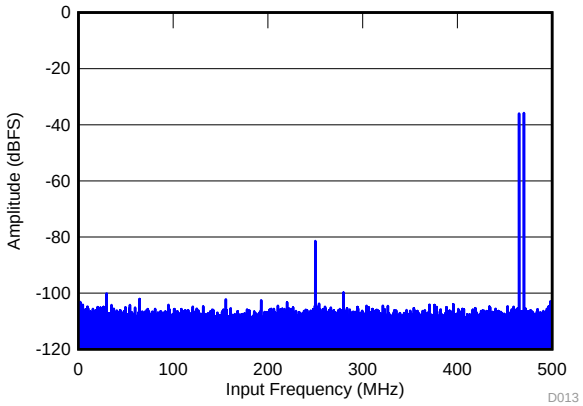


f_{IN1} = 470 MHz, f_{IN2} = 465 MHz, each tone at –7 dBFS,
IMD = 74.9 dBFS

Figure 14. FFT for Two-Tone Input Signal (–7 dBFS)

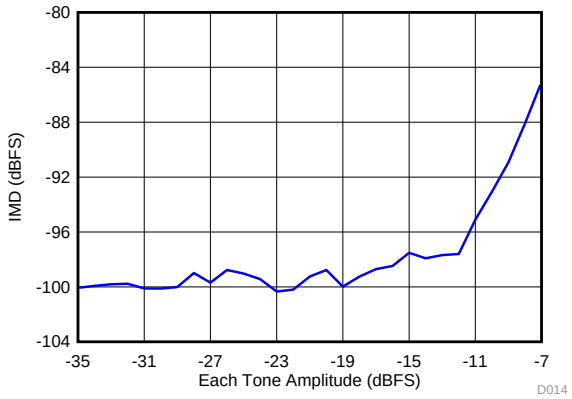
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



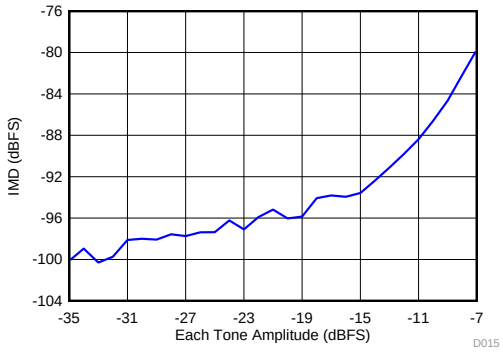
f_{IN1} = 470 MHz, f_{IN2} = 465 MHz, each tone at –36 dBFS, IMD = 109.2 dBFS

Figure 15. FFT for Two-Tone Input Signal (–36 dBFS)



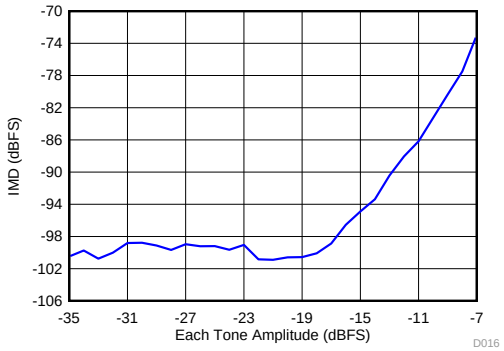
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)



f_{IN1} = 365 MHz, f_{IN2} = 370 MHz

Figure 17. Intermodulation Distortion vs Input Amplitude (365 MHz and 370 MHz)



f_{IN1} = 465 MHz, f_{IN2} = 470 MHz

Figure 18. Intermodulation Distortion vs Input Amplitude (465 MHz and 470 MHz)

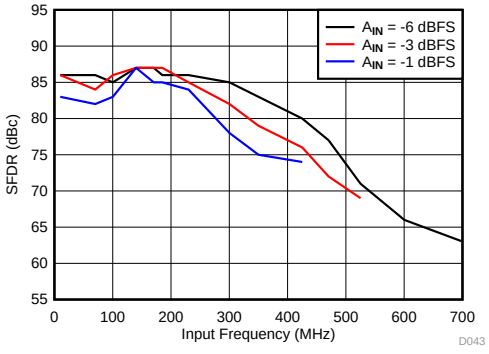


Figure 19. Spurious-Free Dynamic Range vs Input Frequency

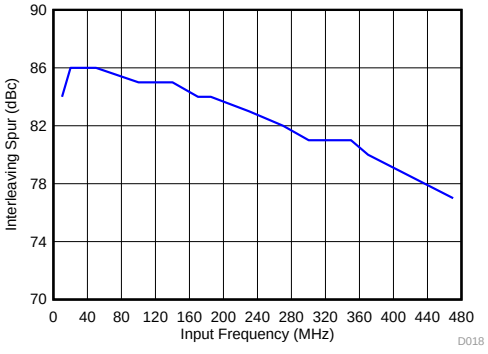


Figure 20. Interleaving Spur vs Input Frequency

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

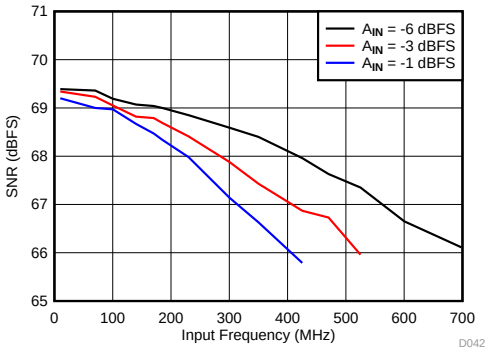
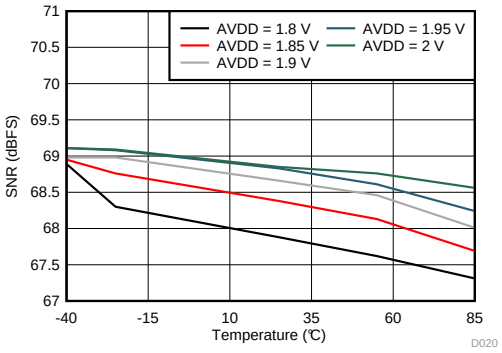
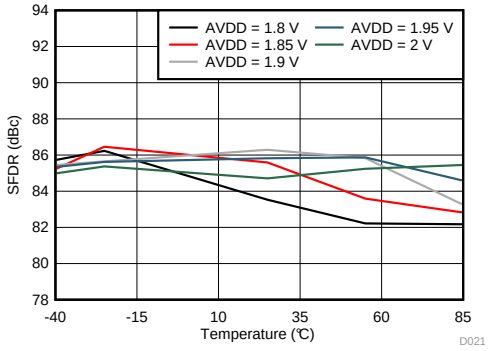


Figure 21. Signal-to-Noise Ratio vs Input Frequency



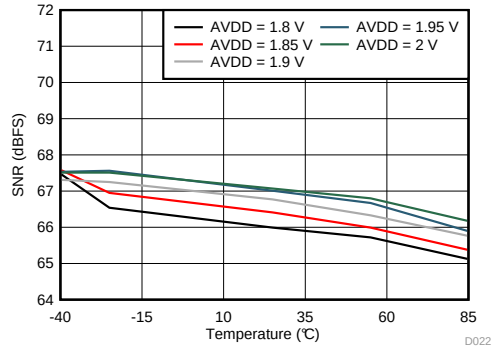
f_{IN} = 170 MHz

Figure 22. Signal-to-Noise Ratio vs AVDD Supply and Temperature



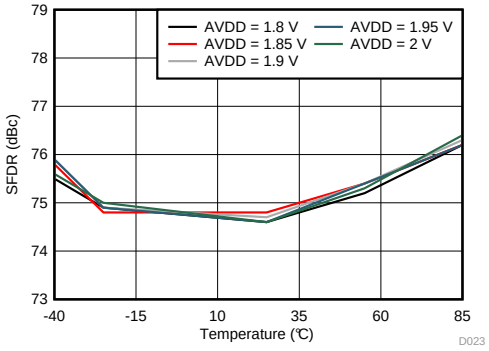
f_{IN} = 170 MHz

Figure 23. Spurious-Free Dynamic Range vs AVDD Supply and Temperature



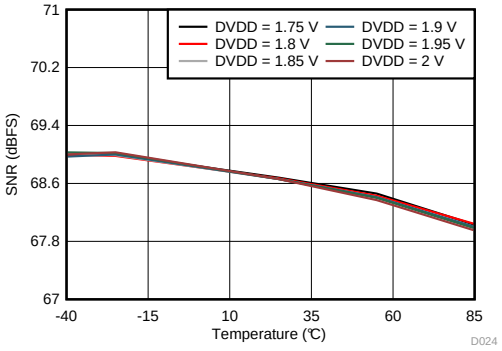
f_{IN} = 350 MHz

Figure 24. Signal-to-Noise Ratio vs AVDD Supply and Temperature



f_{IN} = 350 MHz

Figure 25. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

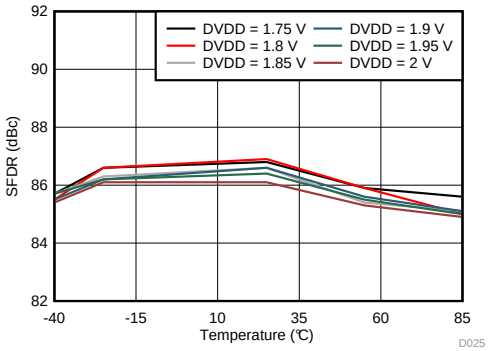


f_{IN} = 170 MHz

Figure 26. Signal-to-Noise Ratio vs DVDD Supply and Temperature

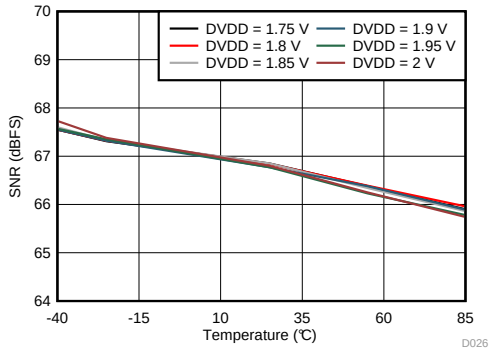
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



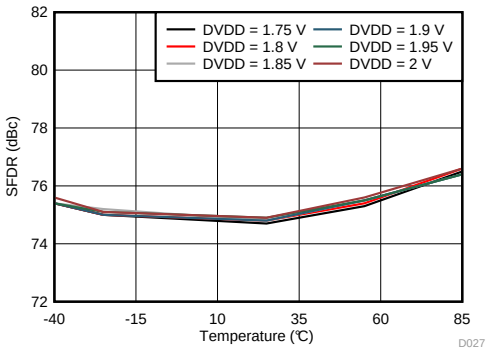
f_{IN} = 170 MHz

Figure 27. Spurious-Free Dynamic Range vs DVDD Supply and Temperature



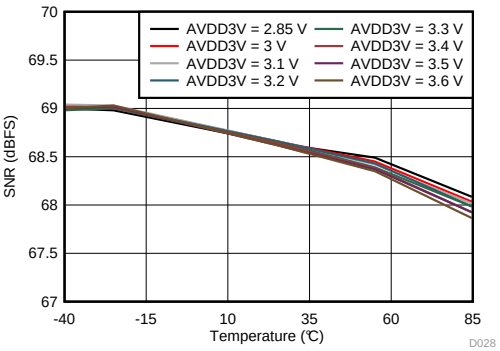
f_{IN} = 350 MHz

Figure 28. Signal-to-Noise Ratio vs DVDD Supply and Temperature



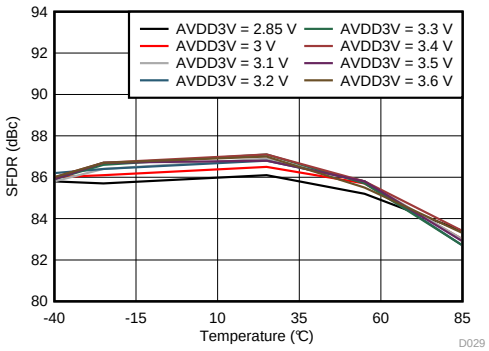
f_{IN} = 350 MHz

Figure 29. Spurious-Free Dynamic Range vs DVDD Supply and Temperature



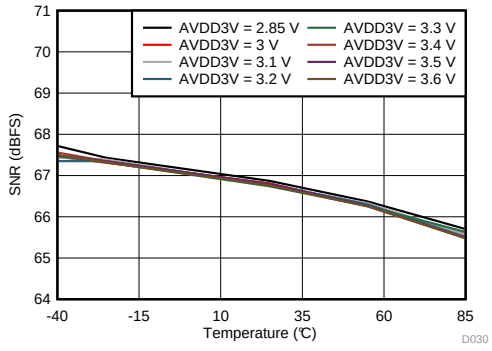
f_{IN} = 170 MHz

Figure 30. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature



f_{IN} = 170 MHz

Figure 31. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

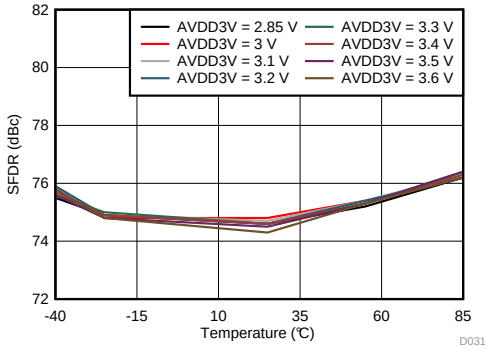


f_{IN} = 350 MHz

Figure 32. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



f_{IN} = 350 MHz

Figure 33. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

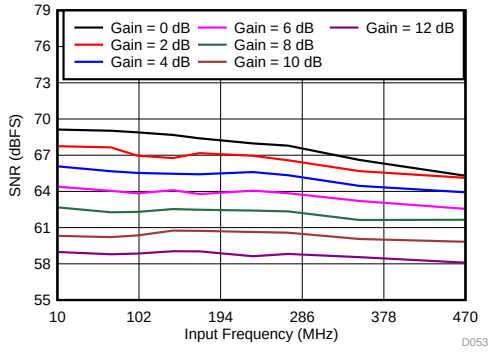


Figure 34. Signal-to-Noise Ratio vs Gain and Input Frequency

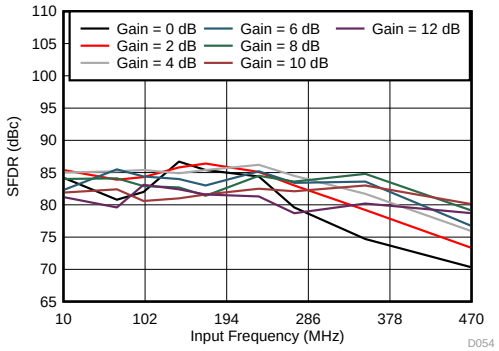


Figure 35. Spurious-Free Dynamic Range vs Gain and Input Frequency

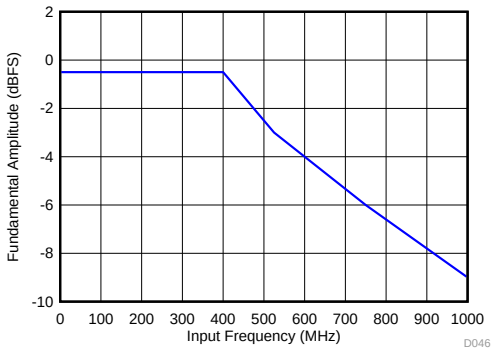
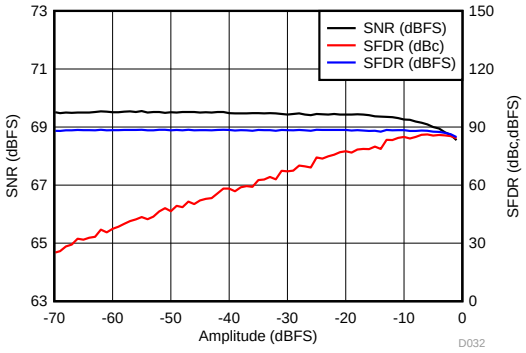
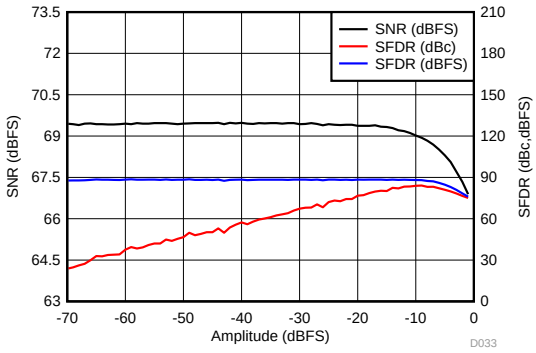


Figure 36. Maximum Supported Amplitude vs Frequency



f_{IN} = 170 MHz

Figure 37. Performance vs Input Amplitude

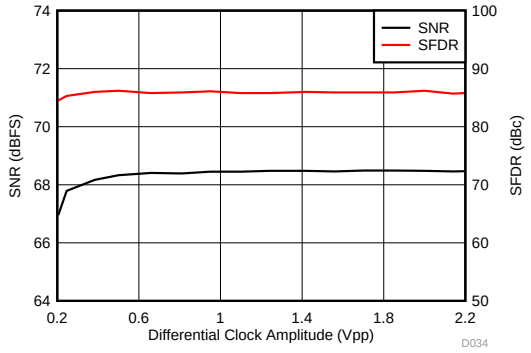


f_{IN} = 350 MHz

Figure 38. Performance vs Input Amplitude

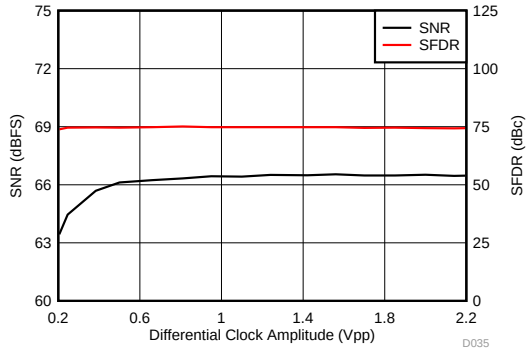
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



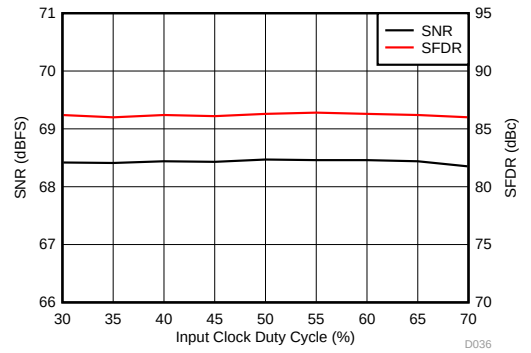
f_{IN} = 170 MHz

Figure 39. Performance vs Sampling Clock Amplitude



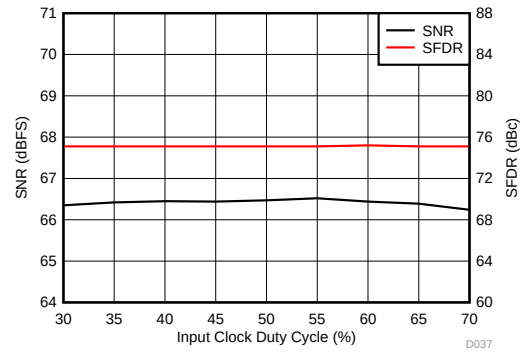
f_{IN} = 350 MHz

Figure 40. Performance vs Sampling Clock Amplitude (Differential)



f_{IN} = 170 MHz

Figure 41. Performance vs Clock Duty Cycle



f_{IN} = 350 MHz

Figure 42. Performance vs Clock Duty Cycle

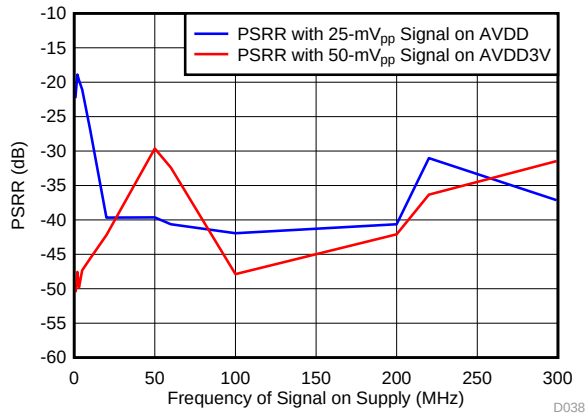
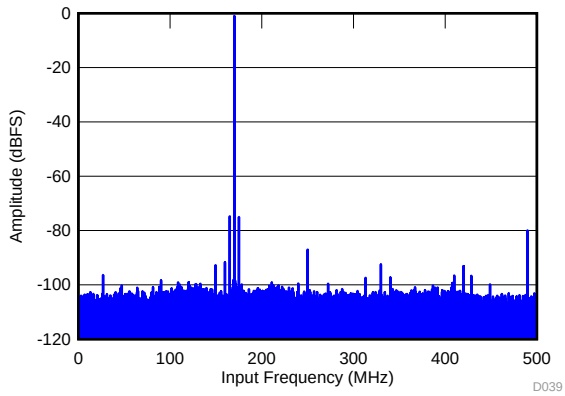


Figure 43. Power-Supply Rejection Ratio vs Supply Signal



SNR = 66.7 dBFS, SINAD = 65.7 dBFS,
SFDR = 79 dBc, f_{IN} = 170.1 MHz,
f_{PSRR} = 5 MHz, non HD2, HD3 spur = 84 dBc

Figure 44. Power-Supply Rejection Ratio FFT for Test Signals on the AVDD Supply

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

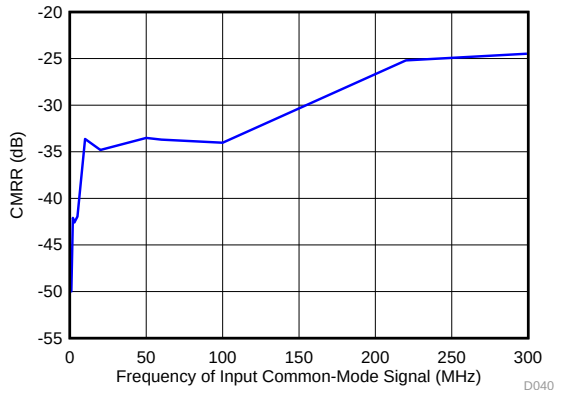


Figure 45. Common-Mode Rejection Ratio vs Signal Frequency

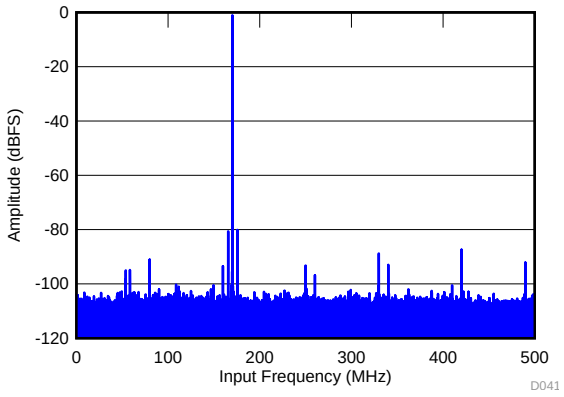


Figure 46. Common-Mode Rejection Ratio FFT

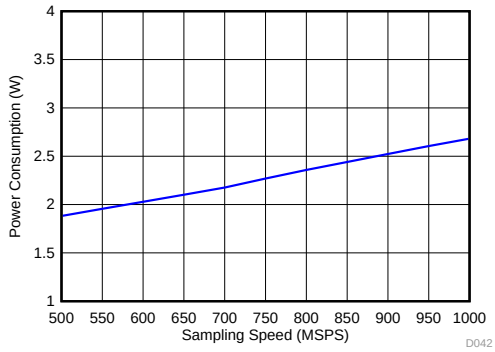


Figure 47. Power Consumption vs Sampling Speed

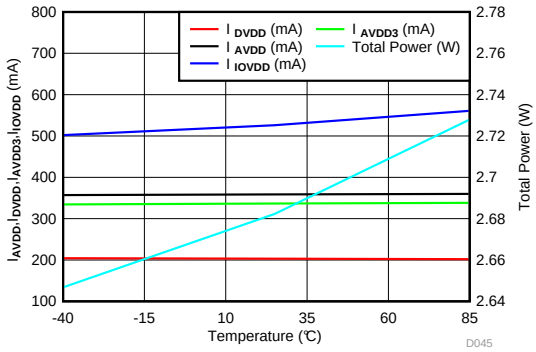
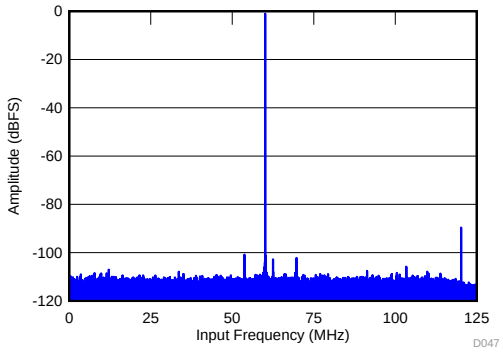
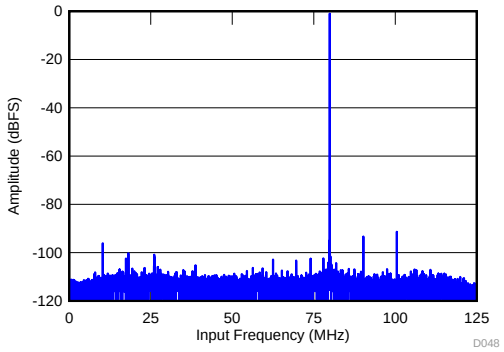


Figure 48. Power vs Temperature



SNR = 70.5 dBFS, SINAD = 69.9 dBFS,
f_S = 250 MHz, f_{IN} = 60 MHz, SFDR = 88.6 dBc,
THD = 83 dBc, non HD2, HD3 spur = 99.96 dBc

Figure 49. FFT for 60-MHz Input Signal in Decimate-by-4 Mode

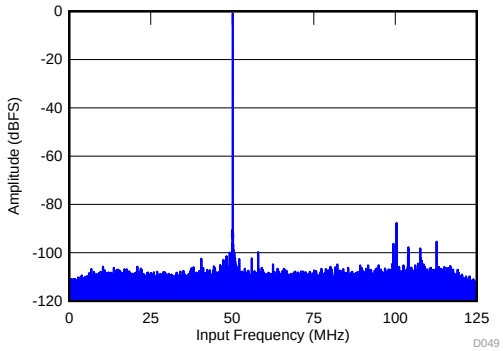


SNR = 70.2 dBFS, SINAD = 69.6 dBFS,
f_S = 250 MHz, f_{IN} = 170 MHz, SFDR = 87 dBc,
non HD2, HD3 spur = 90.42 dBc

Figure 50. FFT for 170-MHz Input Signal in Decimate-by-4 Mode

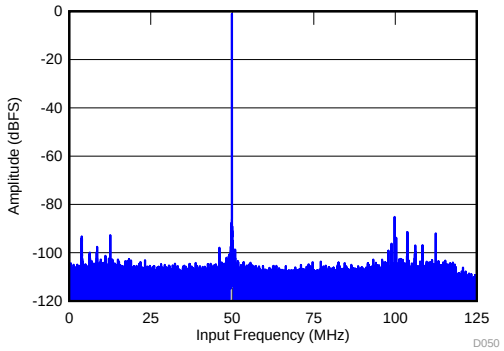
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



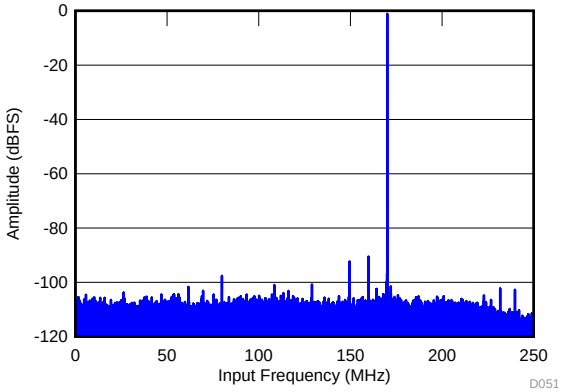
SNR = 69.3 dBFS, SINAD = 68.6 dBFS,
f_S = 250 MHz, f_{IN} = 300 MHz, SFDR = 86 dBc,
non HD2, HD3 spur = 94.42 dBc

Figure 51. FFT for 300-MHz Input Signal in Decimate-by-4 Mode



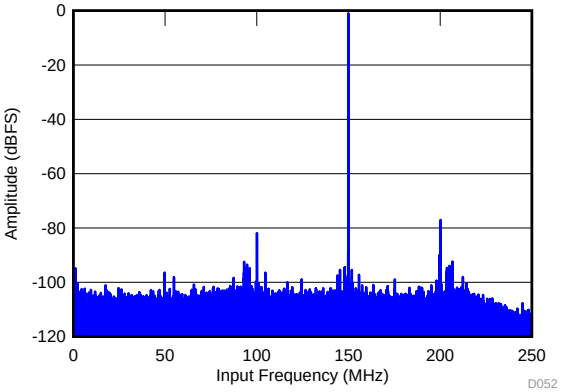
SNR = 67.6 dBFS, SINAD = 66.8 dBFS,
f_S = 250 MHz, f_{IN} = 450 MHz, SFDR = 83 dBc,
non HD2, HD3 spur = 90.44 dBc

Figure 52. FFT for 450-MHz Input Signal in Decimate-by-4 Mode



SNR = 68.9 dBFS, SINAD = 68.2 dBFS,
f_S = 500 MHz, f_{IN} = 170 MHz, SFDR = 86 dBc,
non HD2, HD3 spur = 81.94 dBc

Figure 53. FFT for 170-MHz Input Signal in Decimate-by-2 Mode



SNR = 66.7 dBFS, SINAD = 65.9 dBFS,
f_S = 500 MHz, f_{IN} = 350 MHz, SFDR = 80 dBc,
non HD2, HD3 spur = 80.83 dBc

Figure 54. FFT for 350-MHz Input Signal in Decimate-by-2 Mode

7.10 Typical Characteristics: Contour

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

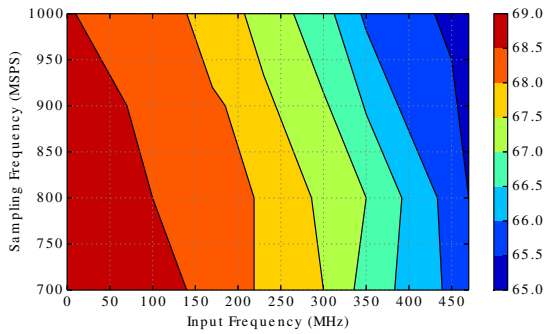


Figure 55. Signal-to-Noise-Ratio with 0-dB Digital Gain

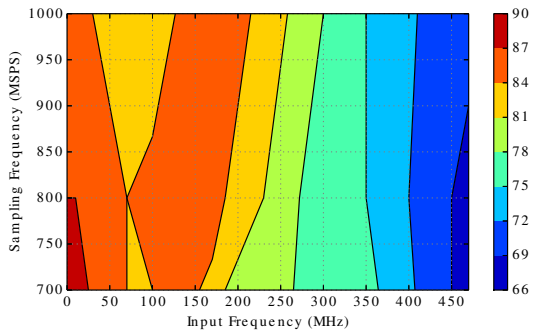


Figure 56. Spurious-Free Dynamic Range with 0-dB Digital Gain

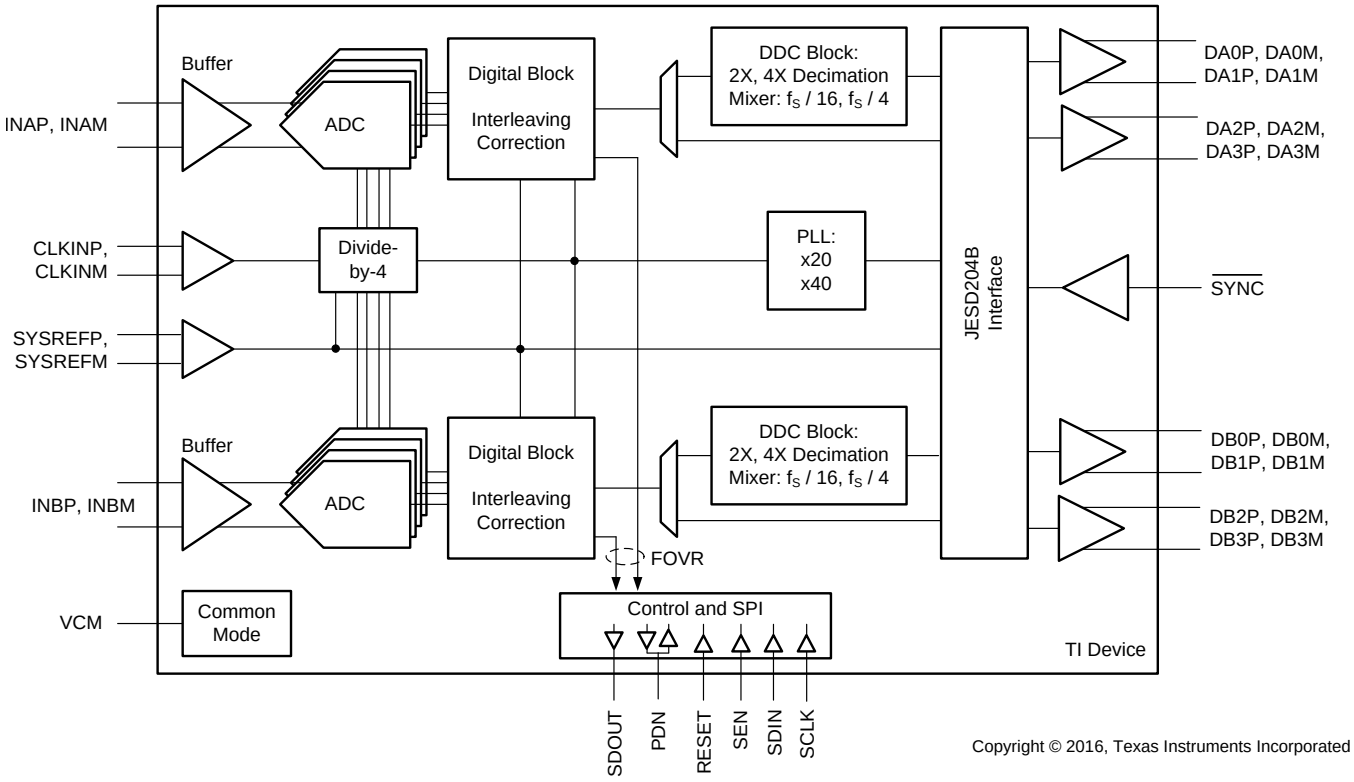
8 Detailed Description

8.1 Overview

The ADS54J20 is a low-power, wide-bandwidth, 12-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). The ADS54J20 employs four interleaving ADCs for each channel to achieve a noise floor of –157 dBFS/Hz. The ADS54J20 uses TI's proprietary interleaving and dither algorithms to achieve a clean spectrum with a high spurious-free dynamic range (SFDR). The device also offers various programmable decimation filtering options for systems requiring higher signal-to-noise ratio (SNR) and SFDR over a wide range of frequencies.

Analog input buffers isolate the ADC driver from glitch energy generated from sampling process, thereby simplifying the driving network on-board. The JESD204B interface reduces the number of interface lines with two-lane and four-lane options, allowing for a high system integration density. The JESD204B interface operates in subclass 1, enabling multi-chip synchronization with the SYSREF input.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs

The ADS54J20 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. Resulting from the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source that enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, resulting in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to VCM using 600-Ω resistors, allowing for ac-coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.475 V) and (VCM – 0.475 V), resulting in a 1.9-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 1.2 GHz. An equivalent analog input network diagram is shown in Figure 57.

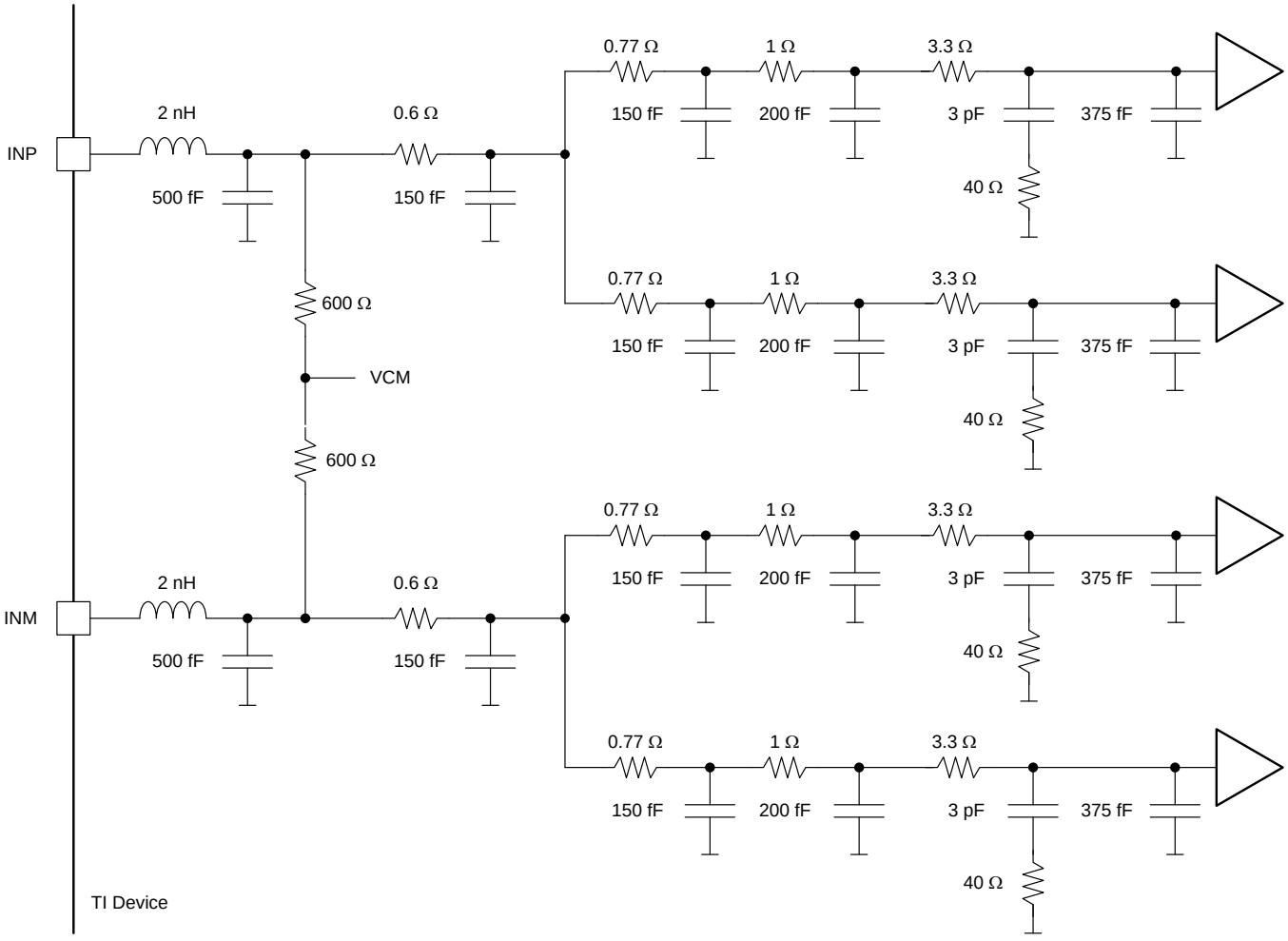


Figure 57. Analog Input Network

Feature Description (continued)

The input bandwidth shown in Figure 58 is measured with respect to a 50-Ω differential input termination at the ADC input pins.

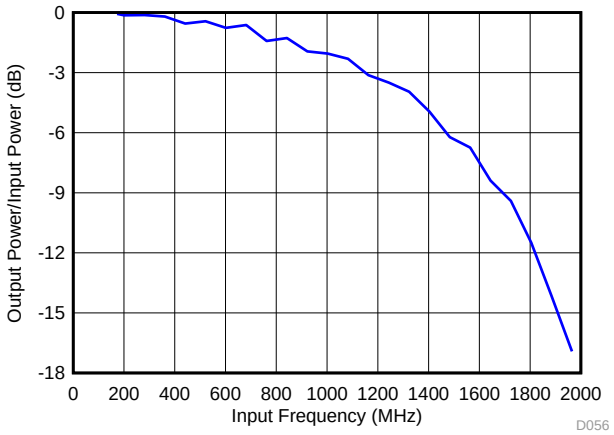
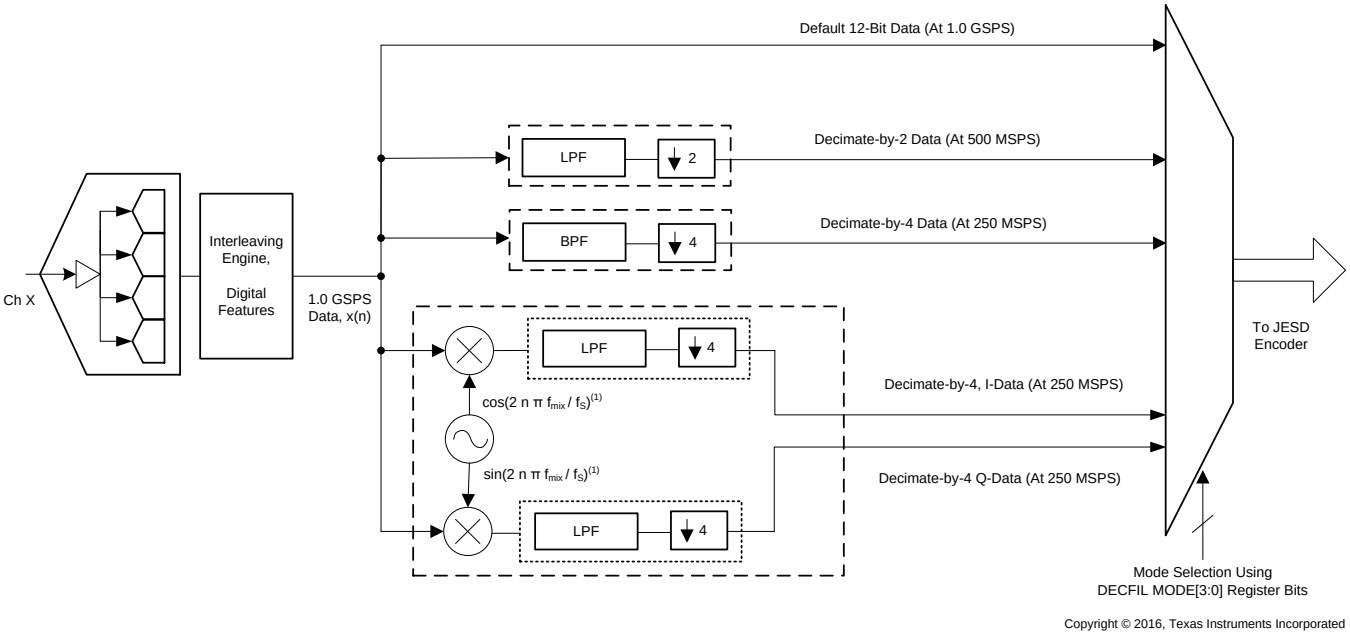


Figure 58. Transfer Function versus Frequency

8.3.2 DDC Block

The ADS54J20 has an optional digital down-converter (DDC) block that can be enabled via an SPI register write. Each ADC channel is followed by a DDC block consisting of three different decimate-by-2 and decimate-by-4 finite impulse response (FIR) half-band filter options. The different decimation filter options can be selected via SPI programming.

Figure 59 shows the signal processing done inside the DDC block of the ADS54J20.



(1) In IQ decimate-by-4 mode, the mixer frequency is fixed at $f_{mix} = f_S / 4$. For f_S = 1.0 GSPS and f_{mix} = 250 MHz.

Figure 59. DDC Block

Feature Description (continued)

8.3.2.1 Decimate-by-2 Filter

This decimation filter has 41 taps. The stop-band attenuation is approximately 90 dB and the pass-band flatness is ±0.05 dB. Table 1 shows corner frequencies for the low-pass and high-pass filter options.

Table 1. Corner Frequencies for the Decimate-by-2 Filter

CORNERS (dB)	LOW PASS	HIGH PASS
–0.1	0.202 × f_S	0.298 × f_S
–0.5	0.210 × f_S	0.290 × f_S
–1	0.215 × f_S	0.285 × f_S
–3	0.227 × f_S	0.273 × f_S

Figure 60 and Figure 61 show the frequency response of the decimate-by-2 filter from dc to f_S / 2.

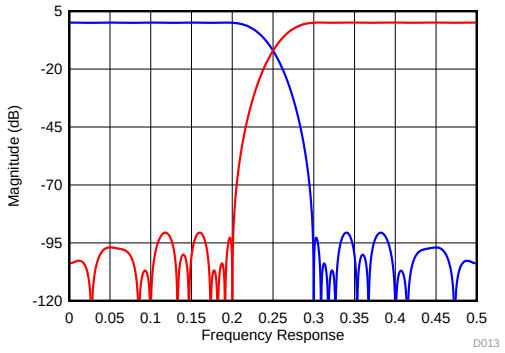


Figure 60. Decimate-by-2 Filter Response

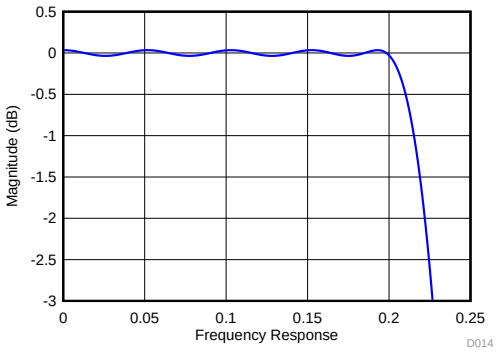


Figure 61. Decimate-by-2 Filter Response (Zoomed)

8.3.2.2 Decimate-by-4 Filter Using a Digital Mixer

This band-pass decimation filter consists of a digital mixer and three concatenated FIR filters with a combined latency of approximately 28 output clock cycles. The alias-band attenuation is approximately 55 dB and the pass-band flatness is ±0.1 dB. By default after reset, the band-pass filter is centered at f_S / 16. Using the SPI, the center frequency can be programmed at N × f_S / 16 (where N = 1, 3, 5, or 7). Table 2 shows corner frequencies for two extreme options.

Table 2. Corner frequencies for the Decimate-by-4 Filter

CORNERS (dB)	CORNER FREQUENCY AT LOWER SIDE (Center Frequency f_S / 16)	CORNER FREQUENCY AT HIGHER SIDE (Center Frequency f_S / 16)
–0.1	0.011 × f_S	0.114 × f_S
–0.5	0.010 × f_S	0.116 × f_S
–1	0.008 × f_S	0.117 × f_S
–3	0.006 × f_S	0.120 × f_S

Figure 62 and Figure 63 show the frequency response of the decimate-by-4 filter for center frequencies f_S / 16 and 3 × f_S / 16 (N = 1 and N = 3, respectively).

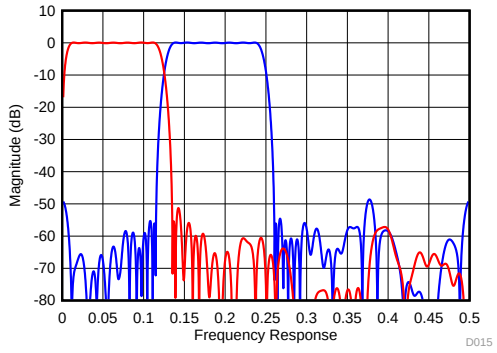


Figure 62. Decimate-by-4 Filter Response

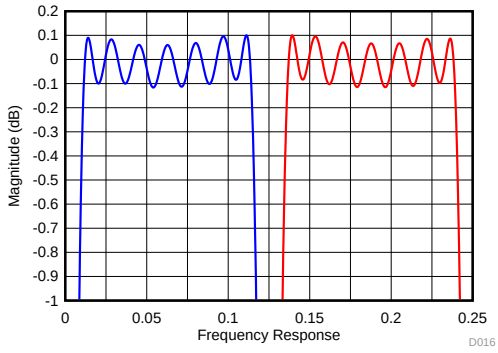


Figure 63. Decimate-by-4 Filter Response (Zoomed)

8.3.2.3 Decimate-by-4 Filter with IQ Outputs

In this configuration, the DDC block includes a fixed digital f_S / 4 mixer. Thus, the IQ pass band is approximately ±0.11 f_S, centered at f_S / 4. This decimation filter has 41 taps with a latency of approximately ten output clock cycles. The stop-band attenuation is approximately 90 dB and the pass-band flatness is ±0.05 dB. Table 3 shows the corner frequencies for a low-pass, decimate-by-4 IQ filter.

Table 3. Corner Frequencies for a Decimate-by-4 IQ Output Filter

CORNERS (dB)	LOW PASS
–0.1	0.107 × f_S
–0.5	0.112 × f_S
–1	0.115 × f_S
–3	0.120 × f_S

Figure 64 and Figure 65 show the frequency response of a decimate-by-4 IQ output filter from dc to f_S / 2.

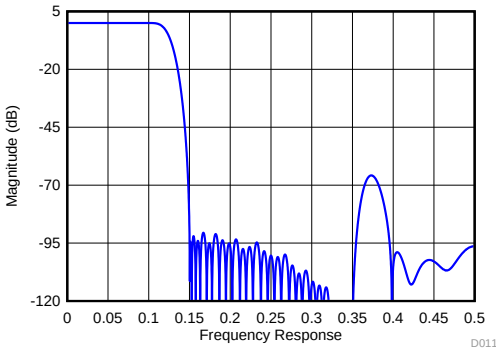


Figure 64. Decimate-by-4 IQ Output Filter Response

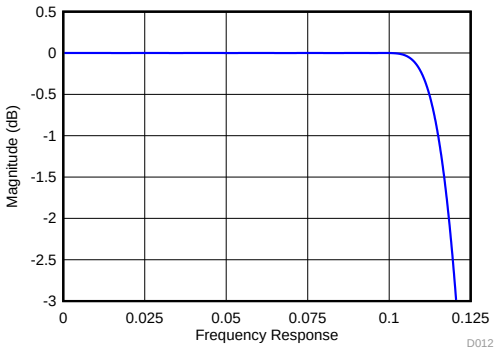


Figure 65. Decimate-by-4 IQ Output Filter Response (Zoomed)

8.3.3 SYSREF Signal

The SYSREF signal is a periodic signal that is sampled by the ADS54J20 device clock and used to align the boundary of the local multiframe clock inside the data converter. SYSREF is required to be a sub-harmonic of the local multiframe clock (LMFC) internal timing. To meet this requirement, the timing of SYSREF is dependent on the device clock frequency and the LMFC frequency, as determined by the selected DDC decimation and frames per multiframe settings. The SYSREF signal is recommended to be a low-frequency signal in the range of 1 MHz to 5 MHz to reduce coupling to the signal path both on the printed circuit board (PCB) as well as internal to the device.

The external SYSREF signal must be a sub-harmonic of the internal LMFC clock, as shown in Equation 1 and Table 4.

$$SYSREF = LMFC / 2^N \quad (1)$$

where

- N = 0, 1, 2, and so forth

Table 4. LMFSC Clock Frequency

LMFS CONFIGURATION	DECIMATION	LMFC CLOCK(1)(2)
4211	—	f_S / K
4244	—	(f_S / 4) / K
8224	—	(f_S / 4) / K
4222	2X	(f_S / 4) / K
2242	2X	(f_S / 4) / K
2221	4X	(f_S / 4) / K
2441	4X (IQ)	(f_S / 4) / K
4421	4X (IQ)	(f_S / 4) / K
1241	4X	(f_S / 4) / K

(1) K = Number of frames per multiframe (JESD digital page 6900h, address 06h, bits 4-0).
(2) f_S = sampling (device) clock frequency.

For example, if LMFS = 8224, the default value of K is 8 + 1 = 9 (the actual value for K = the value set in the SPI register + 1). If the device clock frequency is f_S = 1.0 GSPS, then the local multiframe clock frequency becomes (1000 / 4) / 9 = 27.778 MHz. The SYSREF signal frequency can be chosen as LMFC frequency / 8 = 3.47222 MHz.

8.3.4 Overrange Indication

The ADS54J20 provides a fast overrange indication that can be presented in the digital output data stream via SPI configuration. Alternatively, if not used, the SDOUT (pin 11) and PDN (pin 50) pins can be configured via the SPI to output the fast OVR indicator.

The JESD 8b, 10b encoder receives 16-bit data that are formed by 12-bit ADC data padded with four 0s as LSBs. When the FOVR indication is embedded in the output data stream, the LSB of the 16-bit data stream going to the 8b, 10b encoder is replaced, as shown in Figure 66.

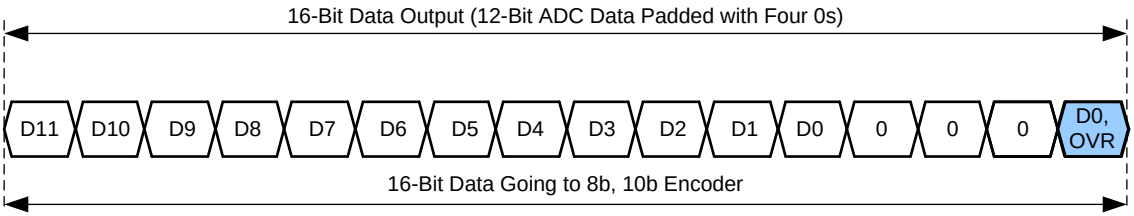


Figure 66. Overrange Indication in a Data Stream

8.3.4.1 Fast OVR

The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after only seven clock cycles, thus enabling a quicker reaction to an overrange event.

The input voltage level that the overload is detected at is referred to as the *threshold*. The threshold is programmable using the FOVR THRESHOLD bits, as shown in Figure 67. The FOVR is triggered seven output clock cycles after the overload condition occurs.

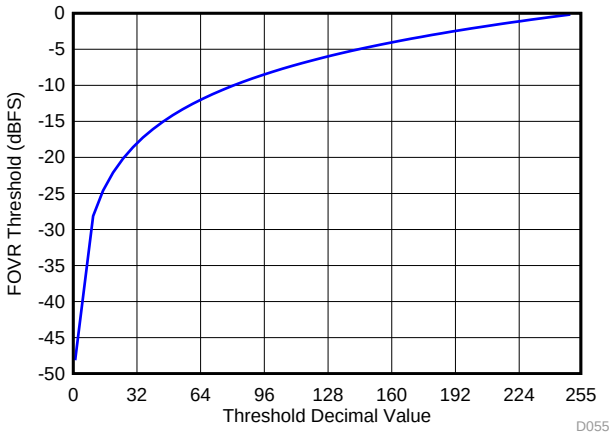


Figure 67. Programming Fast OVR Thresholds

The input voltage level that the fast OVR is triggered at is defined by Equation 2:

Full-Scale × [Decimal Value of the FOVR Threshold Bits] / 255) (2)

The default threshold is E3h (227d), corresponding to a threshold of –1 dBFS.

In terms of full-scale input, the fast OVR threshold can be calculated as Equation 3:

20log (FOVR Threshold / 255) (3)

8.3.5 Power-Down Mode

The ADS54J20 provides a highly-configurable power-down mode. Power-down can be enabled using the PDN pin or SPI register writes.

A power-down mask can be configured that allows a trade-off between wake-up time and power consumption in power-down mode. Two independent power-down masks can be configured: MASK 1 and MASK 2, as shown in Table 5. See the master page registers in Table 14 for further details.

Table 5. Register Addresses for Power-Down Modes

REGISTER ADDRESS A[7:0] (Hex)	COMMENT	REGISTER DATA							
		7	6	5	4	3	2	1	0
MASTER PAGE (80h)									
20	MASK 1	PDN ADC CHA				PDN ADC CHB			
21		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	MASK 2	PDN ADC CHA				PDN ADC CHB			
24		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	CONFIG	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
53		0	MASK SYSREF	0	0	0	0	0	0
55		0	0	0	PDN MASK	0	0	0	0

To save power, the device can be put in complete power-down by using the GLOBAL PDN register bit. However, when JESD is required to remain active when putting the device in power-down, the ADC and analog buffer can be powered down by using the PDN ADC CHx and PDN BUFFER CHx register bits after enabling the PDN MASK register bit. The PDN MASK SEL register bit can be used to select between MASK 1 or MASK 2. Table 6 shows the power consumption for different combinations of the GLOBAL PDN, PDN ADC CHx, and PDN BUFF CHx register bits.

Table 6. Power Consumption in Different Power-Down Settings

REGISTER BIT	COMMENT	I_{AVDD3V} (mA)	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{IOVDD} (mA)	TOTAL POWER (W)
Default	After reset, with a full-scale input signal to both channels	247	260	137	382	1.94
GBL PDN = 1	The device is in a complete power-down state	3	6	23	192	0.28
GBL PDN = 0, PDN ADC CHx = 1 (x = A or B)	The ADC of one channel is powered down	206	166	97	367	1.54
GBL PDN = 0, PDN BUFF CHx = 1 (x = A or B)	The input buffer of one channel is powered down	195	258	137	381	1.78
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A or B)	The ADC and input buffer of one channel are powered down	152	166	97	363	1.37
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A and B)	The ADC and input buffer of both channels are powered down	55	70	56	356	0.81

8.4 Device Functional Modes

8.4.1 Device Configuration

The ADS54J20 can be configured by using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down mode.

The ADS54J20 supports a 24-bit (16-bit address, 8-bit data) SPI operation and uses paging (see the *Register Maps* section) to access all register bits.

8.4.1.1 Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDIN (serial interface data) pins, as shown in Figure 68. SPI bits in Figure 68 are explained in Table 7. Serially shifting bits into the device is enabled when SEN is low. Serial data on SDIN are latched at every SCLK rising edge when SEN is active (low). The interface can function with SCLK frequencies from 2 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

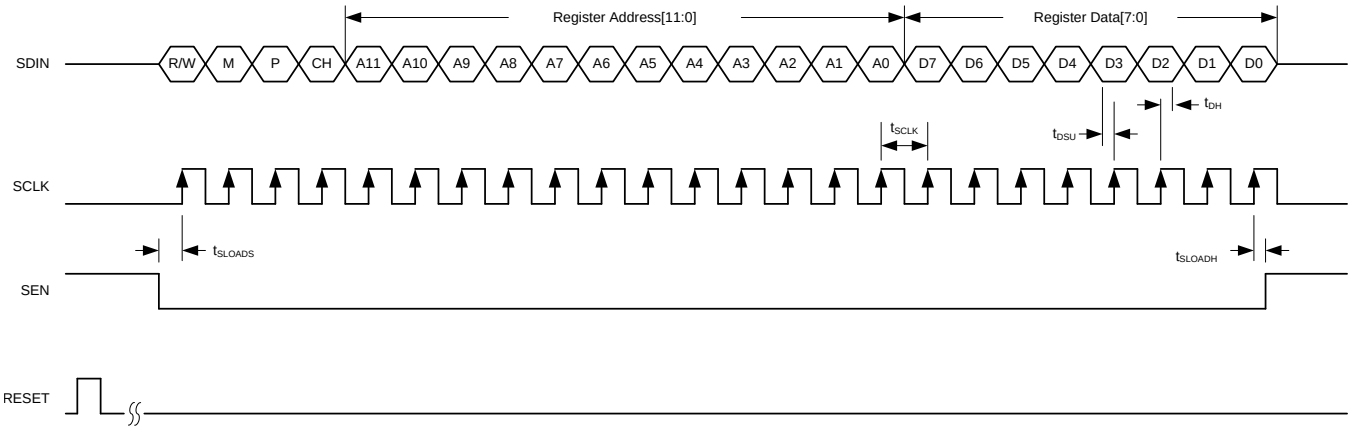


Figure 68. SPI Timing Diagram

Table 7. SPI Timing Diagram Legend

SPI BITS	DESCRIPTION	BIT SETTINGS
R/W	Read/write bit	0 = SPI write 1 = SPI read back
M	SPI bank access	0 = Analog SPI bank (master and ADC pages) 1 = JESD SPI bank (main digital, JESD analog, and JESD digital pages)
P	JESD page selection bit	0 = Page access 1 = Register access
CH	SPI access for a specific channel of the JESD SPI bank	0 = Channel A 1 = Channel B By default, both channels are being addressed.
A[11:0]	SPI address bits	—
D[7:0]	SPI data bits	—

Table 8 shows the timing requirements for the serial interface signals in Figure 68.

Table 8. SPI Timing Requirements

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		2	MHz
t_{SLOADS}	SEN to SCLK setup time	100			ns
t_{SLOADH}	SCLK to SEN hold time	100			ns
t_{DSU}	SDIN setup time	100			ns
t_{DH}	SDIN hold time	100			ns

8.4.1.2 Serial Register Write: Analog Bank

The analog SPI bank contains two pages (the master and ADC pages). The internal register of the ADS54J20 analog SPI bank can be programmed by:

1. Driving the SEN pin low.
2. Initiating a serial interface cycle specifying the page address of the register whose content must be written.
   - Master page: write address 0011h with 80h.
   - ADC page: write address 0011h with 0Fh.
3. Writing the register content as shown in Figure 69. When a page is selected, multiple writes into the same page can be done.

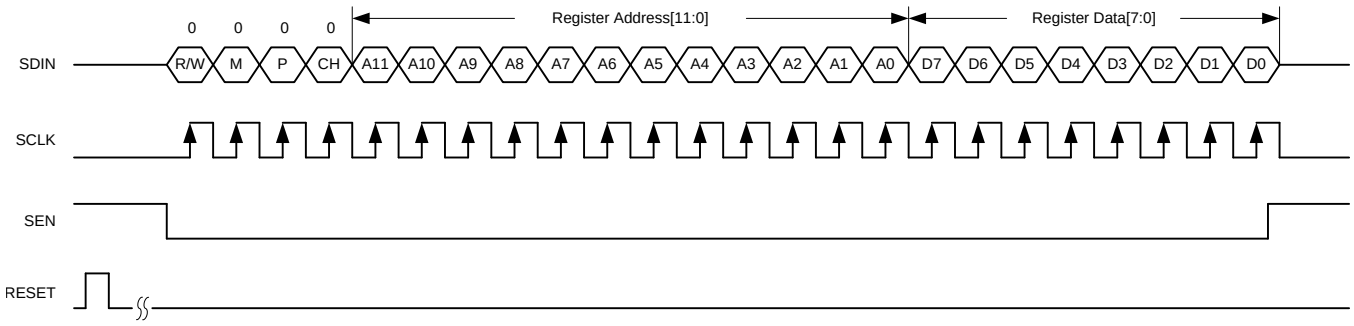


Figure 69. Serial Register Write Timing Diagram

8.4.1.3 Serial Register Readout: Analog Bank

The content from one of the two analog banks can be read out by:

1. Driving the SEN pin low.
2. Selecting the page address of the register whose content must be read.
   - Master page: write address 0011h with 80h.
   - ADC page: write address 0011h with 0Fh.
3. Setting the R/W bit to 1 and writing the address to be read back.
4. Reading back the register content on the SDOUT pin, as shown in Figure 70. When a page is selected, multiple read backs from the same page can be done.

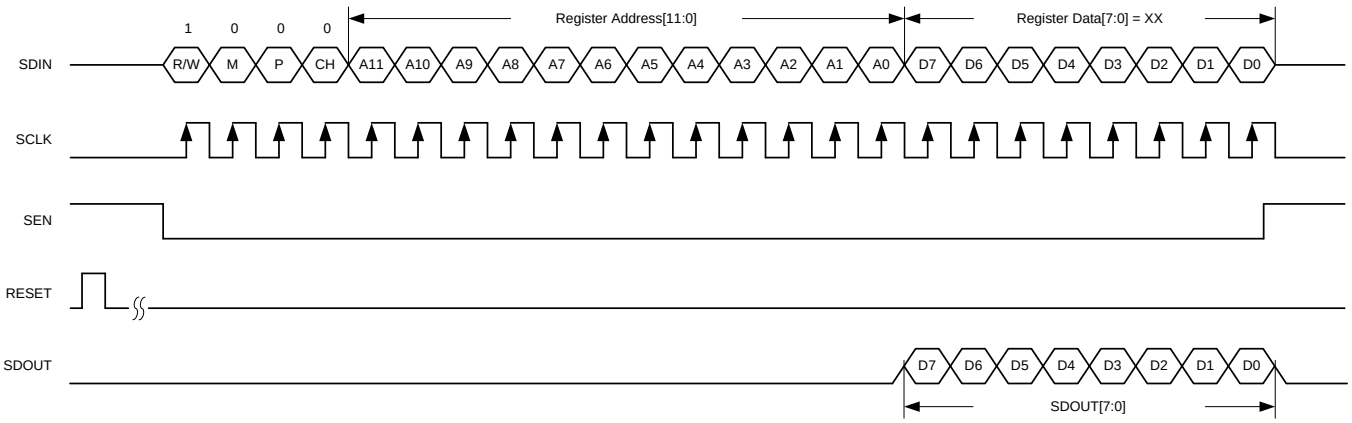


Figure 70. Serial Register Read Timing Diagram

8.4.1.4 JESD Bank SPI Page Selection

The JESD SPI bank contains three pages (main digital, JESD digital, and JESD analog pages). The individual pages can be selected by:

1. Driving the SEN pin low.
2. Setting the M bit to 1 and specifying the page with two register writes. Note that the P bit must be set to 0, as shown in Figure 71.
   - Write address 4003h with 00h (LSB byte of the page address).
   - Write address 4004h with the MSB byte of the page address.
     - For the main digital page: write address 4004h with 68h.
     - For the JESD digital page: write address 4004h with 69h.
     - For the JESD analog page: write address 4004h with 6Ah.

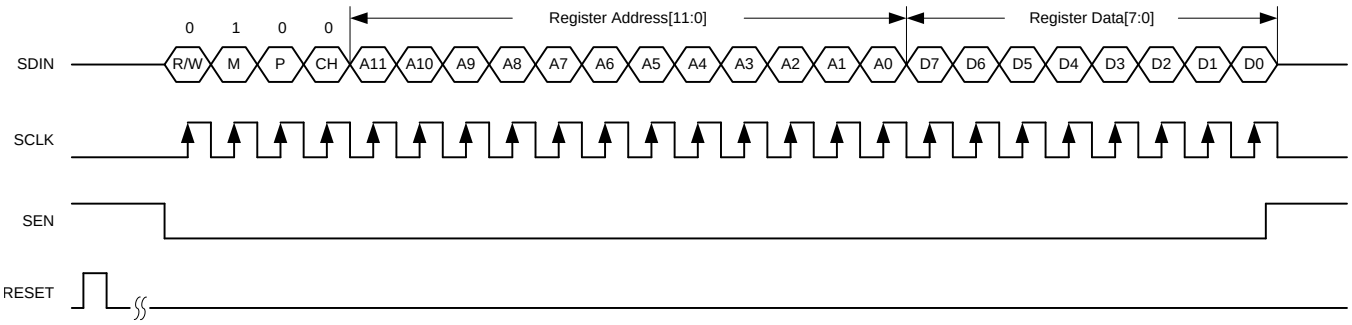


Figure 71. SPI Page Selection

8.4.1.5 Serial Register Write: JESD Bank

The ADS54J20 is a dual-channel device and the JESD204B portion is configured individually for each channel by using the CH bit. Note that the P bit must be set to 1 for register writes.

1. Drive the SEN pin low.
2. Select the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   - Write address 4003h with 00h.
   - Write address 4005h with 01h to enable separate control for both channels.
     - For the main digital page: write address 4004h with 68h.
     - For the JESD digital page: write address 4004h with 69h.
     - For the JESD analog page: write address 4004h with 6Ah.
3. Set the M and P bits to 1, select channel A (CH = 0) or channel B (CH = 1), and write the register content as shown in Figure 72. When a page is selected, multiple writes into the same page can be done.

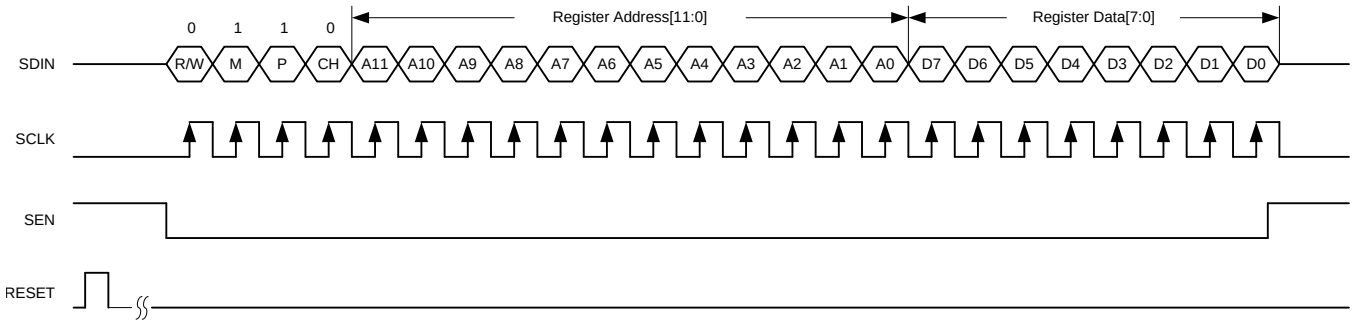


Figure 72. JESD Serial Register Write Timing Diagram

8.4.1.5.1 Individual Channel Programming

By default, register writes are applied to both channels. To enable individual channel writes, write address 4005h with 01h (default is 00h).

8.4.1.6 Serial Register Readout: JESD Bank

The content from one of the pages of the JESD bank can be read out by:

1. Driving the SEN pin low.
2. Selecting the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   - Write address 4003h with 00h.
   - Write address 4005h with 01h to enable separate control for both channels.
     - For the main digital page: write address 4004h with 68h.
     - For the JESD digital page: write address 4004h with 69h.
     - For the JESD analog page: write address 4004h with 6Ah.
3. Setting the R/W, M, and P bits to 1, selecting channel A or channel B, and writing the address to be read back.
4. Reading back the register content on the SDOUT pin; see Figure 73. When a page is selected, multiple read backs from the same page can be done.

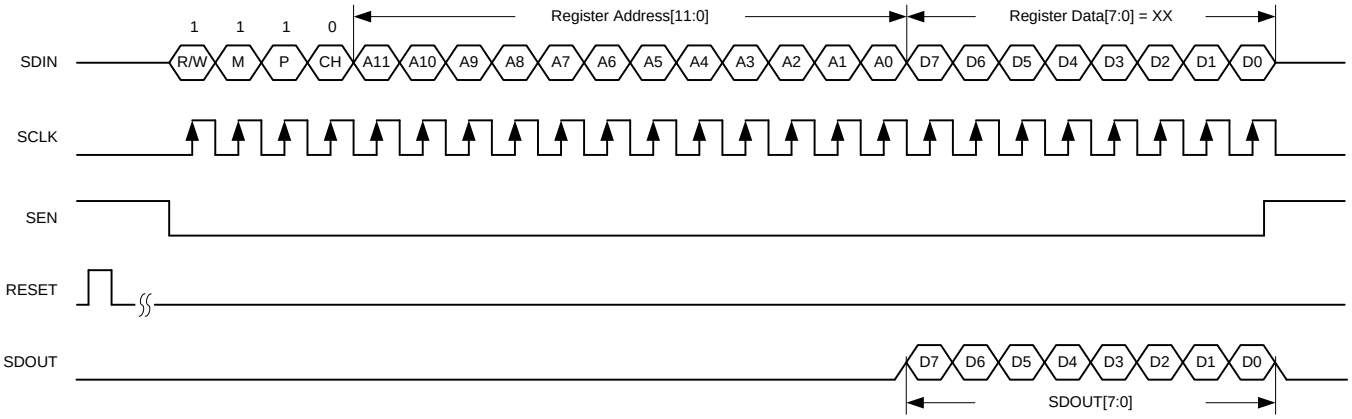


Figure 73. JESD Serial Register Read Timing Diagram

8.4.2 JESD204B Interface

The ADS54J20 supports device subclass 1 with a maximum output data rate of 6.25 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge, allowing synchronization of multiple devices in a system and minimizing timing and alignment uncertainty. The $\overline{\text{SYNC}}$ input is used to control the JESD204B SerDes blocks.

Depending on the ADC output data rate, the JESD204B output interface can be operated with either two or four lanes per single ADC, as shown in Figure 74. The JESD204B setup and configuration of the frame assembly parameters is controlled via the SPI interface.

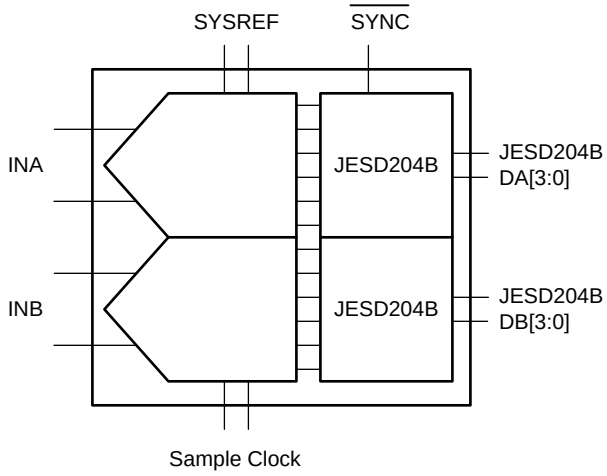


Figure 74. ADS54J20 Block Diagram

The JESD204B transmitter block shown in Figure 75 consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format. The link layer performs the 8b, 10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

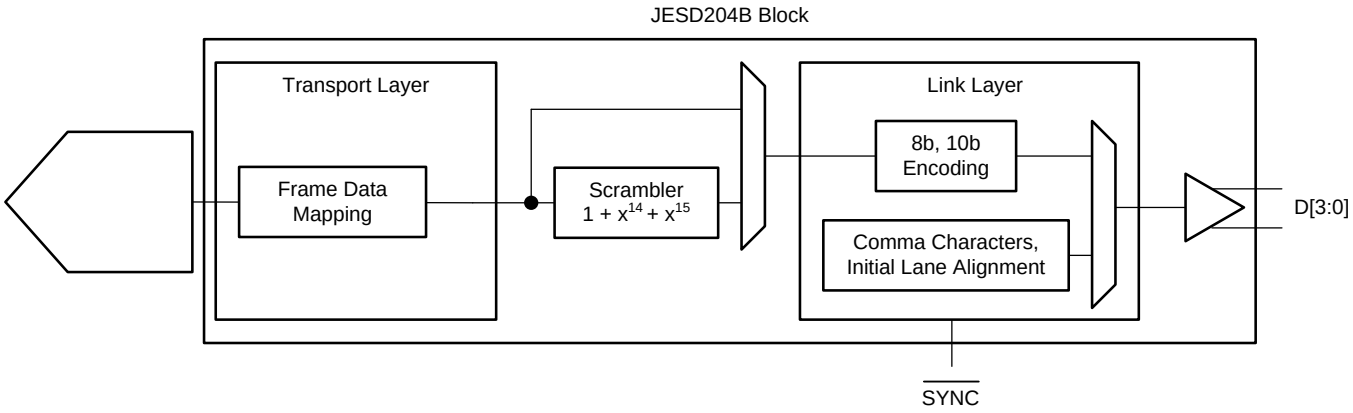


Figure 75. JESD204B Transmitter Block

8.4.2.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started when the receiving device deasserts the SYNC signal, as shown in Figure 76. When a logic low is detected on the SYNC input pin, the ADS54J20 starts transmitting comma (K28.5) characters to establish a code group synchronization.

When synchronization is complete, the receiving device asserts the SYNC signal and the ADS54J20 starts the initial lane alignment sequence with the next local multiframe clock boundary. The ADS54J20 transmits four multiframes, each containing K frames (K is SPI programmable). Each of the multiframes contains the frame start and end symbols and the second multiframe also contains the JESD204 link configuration data.

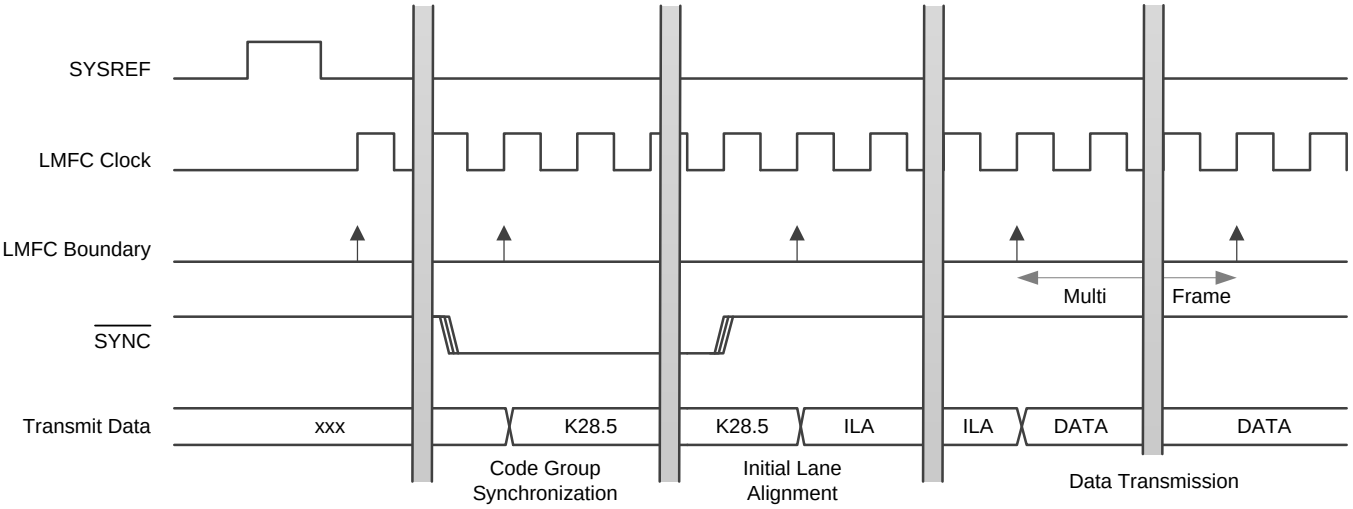


Figure 76. Lane Alignment Sequence

8.4.2.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADS54J20 supports a clock output, encoded, and a PRBS ($2^{15} – 1$) pattern. These test patterns can be enabled via an SPI register write and are located in the JESD digital page of the JESD bank.

8.4.2.3 JESD204B Frame

The JESD204B standard defines the following parameters:

- L is the number of lanes per link.
- M is the number of converters per device.
- F is the number of octets per frame clock period, per lane.
- S is the number of samples per frame per converter.

8.4.2.4 JESD204B Frame

Table 9 lists the available JESD204B formats and valid ranges for the ADS54J20 when the decimation filter is not used. The ranges are limited by the SerDes lane rate and the maximum ADC sample frequency.

NOTE

The 16-bit data going to the JESD 8b, 10b encoder are formed by padding four 0s as LSBs into the 12-bit ADC data.

Table 9. Default Interface Rates

L	M	F	S	DECIMATION	MINIMUM RATES		MAXIMUM RATES	
					SAMPLING RATE (MSPS)	SERDES BIT RATE (Gbps)	SAMPLING RATE (MSPS)	SERDES BIT RATE (Gbps)
4	2	1	1	Not used	250	2.5	1000	10.0
4	2	4	4	Not used	250	2.5	1000	10.0
8	2	2	4	Not used	500	2.5	1000	5.0

NOTE

In the LMFS = 8224 row of Table 10, the sample order on the lanes is DA2, DA3, DA1, and DA0 for channel A. Similarly for channel B, the sample order on the lanes is DB2, DB3, DB1, and DB0.

The detailed frame assembly is shown in Table 10.

Table 10. Default Frame Assembly(1)

OUTPUT LANE	LMFS = 4211	LMFS = 4244				LMFS = 8224	
DA0						A_3[11:4]	A_3[3:0], 0000
DA1	A_0[3:0], 0000	A_2[11:4]	A_2[3:0], 0000	A_3[11:4]	A_3[3:0], 0000	A_2[11:4]	A_2[3:0], 0000
DA2	A_0[11:4]	A_0[11:4]	A_0[3:0], 0000	A_1[11:4]	A_1[3:0], 0000	A_0[11:4]	A_0[3:0], 0000
DA3						A_1[11:4]	A_1[3:0], 0000
DB0						B_3[11:4]	B_3[3:0], 0000
DB1	B_0[3:0], 0000	B_2[11:4]	B_2[3:0], 0000	B_3[11:4]	B_3[3:0], 0000	B_2[11:4]	B_2[3:0], 0000
DB2	B_0[11:4]	B_0[11:4]	B_0[3:0], 0000	B_1[11:4]	B_1[3:0], 0000	B_0[11:4]	B_0[3:0], 0000
DB3						B_1[11:4]	B_1[3:0], 0000

(1) Blue shading indicates channel A and yellow shading indicates channel B.

8.4.2.5 JESD204B Frame Assembly with Decimation

Table 11 lists the available JESD204B formats and valid ranges for the ADS54J20 when enabling the decimation filter. The ranges are limited by the SerDes lane rate (2.5 Gbps to 10.0 Gbps) and the ADC sample frequency (300 MSPS to 1000 MSPS).

Table 11. Interface Rates with Decimation Filter

L	M	F	S	DECIMATION	MINIMUM RATES			MAXIMUM RATES		
					DEVICE CLOCK FREQUENCY (MSPS)	OUTPUT SAMPLE RATE (MSPS)	SERDES BIT RATE (Gbps)	DEVICE CLOCK FREQUENCY (MSPS)	OUTPUT SAMPLE RATE (MSPS)	SERDES BIT RATE (Gbps)
4	4	2	1	4X (IQ)	500	125	2.5	1000	250	5
4	2	2	2	2X	500	250	2.5	1000	500	5
2	2	4	2	2X	300	150	3	1000	500	10
2	2	2	1	4X	500	125	2.5	1000	250	5
2	4	4	1	4X (IQ)	300	75	3	1000	250	10
1	2	4	1	4X	300	75	3	1000	250	10

Table 12 lists the detailed frame assembly with different decimation options.

Table 12. Frame Assembly with Decimation Filter(1)

OUTPUT LANE	LMFS = 4222, 2X DECIMATION		LMFS = 2242, 2X DECIMATION				LMFS = 2221, 4X DECIMATION		LMFS = 2441, 4X DECIMATION (IQ)				LMFS = 4421, 4X DECIMATION (IQ)		LMFS = 1241, 4X DECIMATION			
DA0	A_1 [11:4]	A_1 [3:0], 0000											AQ_0 [11:4]	AQ_0 [3:0], 0000				
DA1	A_0 [11:4]	A_0 [3:0], 0000	A_0 [11:4]	A_0 [3:0], 0000	A_1 [11:4]	A_1 [3:0], 0000	A_0 [11:4]	A_0 [3:0], 0000	AI_0 [11:4]	AI_0 [3:0], 0000	AQ_0 [11:4]	AQ_0 [3:0], 0000	AI_0 [11:4]	AI_0 [3:0], 0000	A_0 [11:4]	A_0 [3:0], 0000	B_0 [11:4]	B_0 [3:0], 0000
DA2																		
DA3																		
DB0	B_1 [11:4]	B_1 [3:0], 0000											BQ_0 [11:4]	BQ_0 [3:0], 0000				
DB1	B_0 [11:4]	B_0 [3:0], 0000	B_0 [11:4]	B_0 [3:0], 0000	B_1 [11:4]	B_1 [3:0], 0000	B_0 [11:4]	B_0 [3:0], 0000	BI_0 [11:4]	BI_0 [3:0], 0000	BQ_0 [11:4]	BQ_0 [3:0], 0000	BI_0 [11:4]	BI_0 [3:0], 0000				
DB2																		
DB3																		

(1) Blue shading indicates channel A and yellow shading indicates channel B.

Appropriate register bits must be programmed to enable different options when the decimation filter is enabled. Table 13 summarizes all the decimation filter options available in the DDC block, the corresponding JESD link parameters (L, M, F, and S), and the register bits required to be programmed for each option.

Table 13. Program Summary of DDC Modes and JESD Link Configuration(1)(2)

LMFS OPTIONS				DDC MODES PROGRAMMING				JESD LINK (LMFS) PROGRAMMING						
L	M	F	S	DECIMATION OPTIONS	DEC MODE EN, DECFIL EN(3)	DECFIL MODE[3:0](4)	JESD FILTER(5)	JESD MODE(6)	JESD PLL MODE(7)	LANE SHARE(8)	DA_BUS_REORDER(9)	DB_BUS_REORDER(10)	BUS_REORDER EN1(11)	BUS_REORDER EN2(12)
4	2	1	1	No decimation	00	00	000	100	10	0	00h	00h	0	0
4	2	4	4	No decimation	00	00	000	010	10	0	00h	00h	0	0
8	2	2	4	No decimation (Default after reset)	00	00	000	001	00	0	00h	00h	0	0
4	4	2	1	4X (IQ)	11	0011 (LPF with f_S / 4 mixer)	111	001	00	0	0Ah	0Ah	1	1
4	2	2	2	2X	11	0010 (LPF) or 0110 (HPF)	110	001	00	0	0Ah	0Ah	1	1
2	2	4	2	2X	11	0010 (LPF) or 0110 (HPF)	110	010	10	0	0Ah	0Ah	1	1
2	2	2	1	4X	11	0000, 0100, 1000, or 1100 (all BPFs with different center frequencies).	100	001	00	0	0Ah	0Ah	1	1
2	4	4	1	4X (IQ)	11	0011 (LPF with an f_S / 4 mixer)	111	010	10	0	0Ah	0Ah	1	1
1	2	4	1	4X	11	0000, 0100, 1000, or 1100 (all BPFs with different center frequencies)	100	010	10	1	0Ah	0Ah	1	1

(1) Keeping the same LMFS settings for both channels is recommended.
(2) The PULSE RESET register bit must be pulsed after the registers in the main digital page are programmed.
(3) The DEC MODE EN and DECFIL EN register bits are located in the main digital page, register 04Dh (bit 3) and register 041h (bit 4).
(4) The DECFIL MODE[3:0] register bits are located in the main digital page, register 041h (bits 5 and 2-0).
(5) The JESD FILTER register bits are located in the JESD digital page, register 001h (bits 5-3).
(6) The JESD MODE register bits are located in the JESD digital page, register 001h (bits 2-0).
(7) The JESD PLL MODE register bits are located in the JESD analog page, register 016h (bits 1-0).
(8) The LANE SHARE register bit is located in the JESD digital page, register 016h (bit 4).
(9) The DA_BUS_REORDER register bits are located in the JESD digital page, register 031h (bits 7-0).
(10) The DB_BUS_REORDER register bits are located in the JESD digital page, register 032h (bits 7-0).
(11) The BUS_REORDER EN1 register bit is located in the main digital page, register 052h (bit 7).
(12) The BUS_REORDER EN2 register bit is located in the main digital page, register 072h (bit 3).

8.4.2.5.1 JESD Transmitter Interface

Each of the 6.25-Gbps SerDes JESD transmitter outputs require ac-coupling between the transmitter and receiver. The differential pair must be terminated with 100-Ω resistors as close to the receiving device as possible to avoid unwanted reflections and signal degradation, as shown in Figure 77.

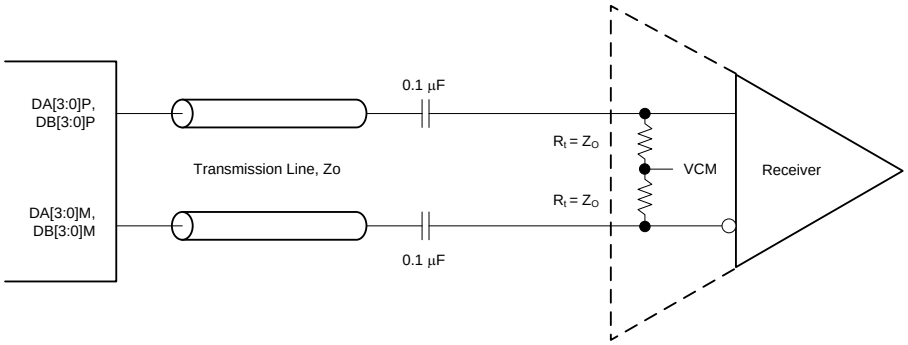


Figure 77. Output Connection to Receiver

8.4.2.5.2 Eye Diagrams

Figure 78 to Figure 81 show the serial output eye diagrams of the ADS54J20 at 5.0 Gbps and 10 Gbps with default and increased output voltage swing against the JESD204B mask.

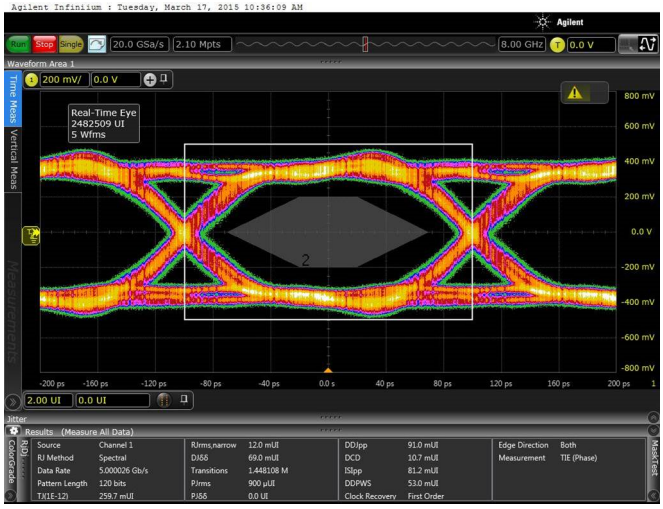


Figure 78. Eye Diagram at 5-Gbps Bit Rate with Default Output Swing

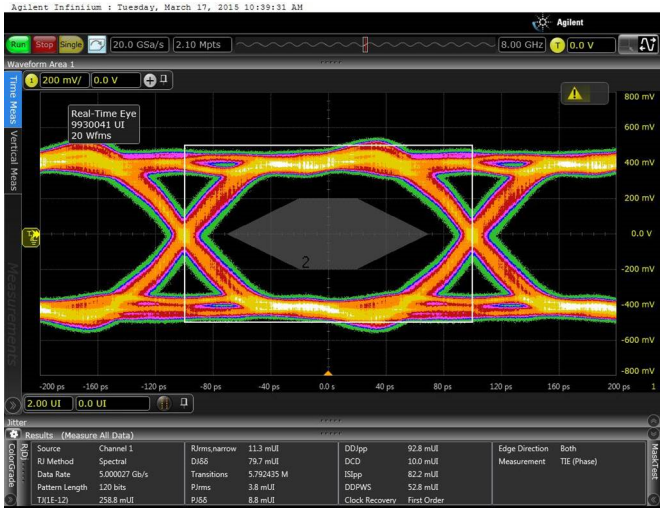


Figure 79. Eye Diagram at 5-Gbps Bit Rate with Increased Output Swing

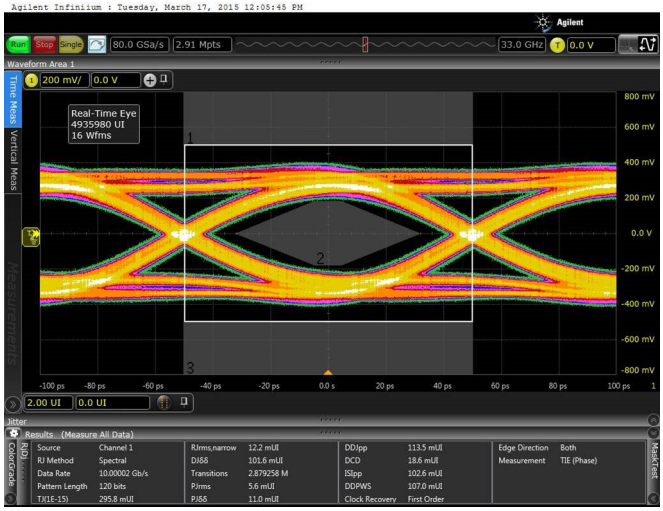


Figure 80. Eye Diagram at 10-Gbps Bit Rate with Default Output Swing

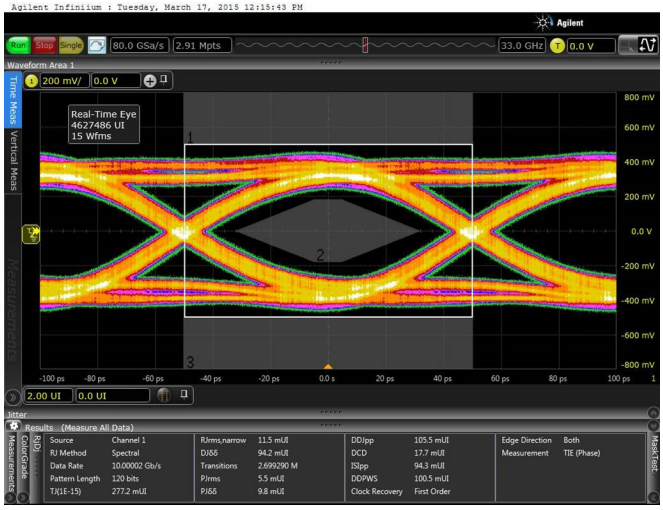


Figure 81. Eye Diagram at 10-Gbps Bit Rate with Increased Output Swing

8.5 Register Maps

Figure 82 shows a conceptual diagram of the serial registers.

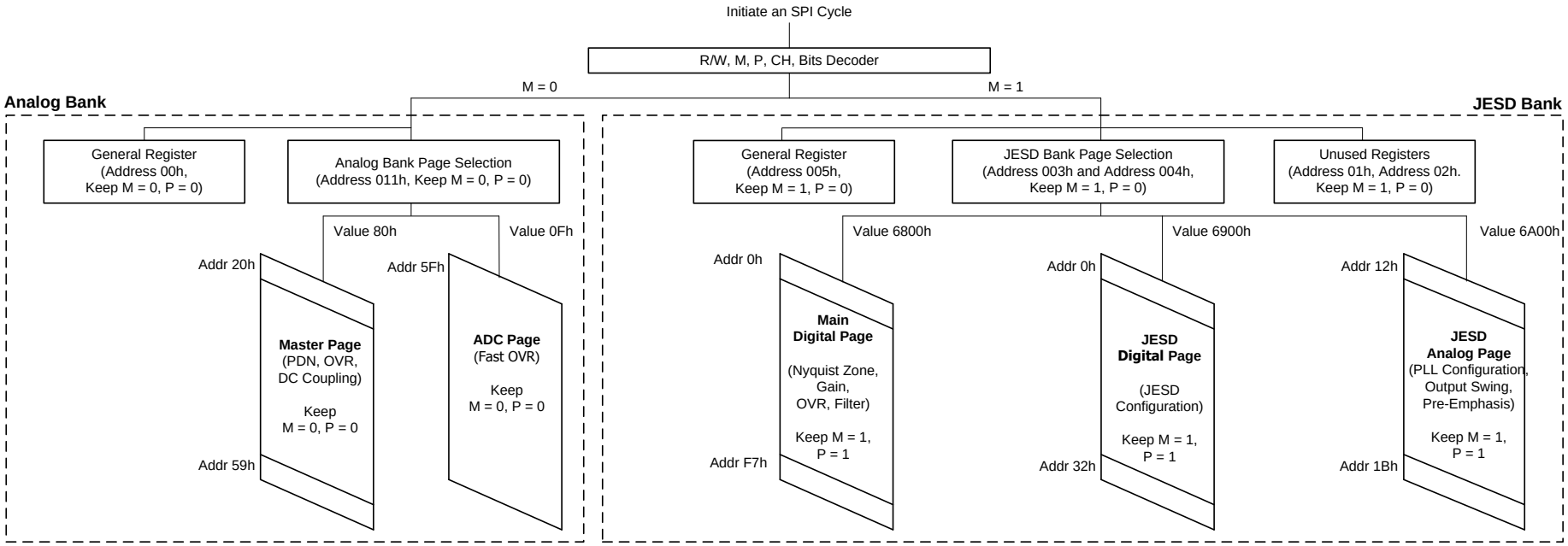


Figure 82. Serial Interface Registers

8.5.1 Detailed Register Information

The ADS54J20 contains two main SPI banks. The analog SPI bank provides access to the ADC analog blocks and the digital SPI bank controls the interleaving engine and anything related to the JESD204B serial interface. The analog SPI bank is divided into two pages (master and ADC) and the digital SPI bank is divided into three pages (main digital, JESD digital, and JESD analog). Table 14 lists a register map for the ADS54J20.

Table 14. Register Map

REGISTER ADDRESS	REGISTER DATA							
A[11:0] (Hex)	7	6	5	4	3	2	1	0
GENERAL REGISTERS								
0	RESET	0	0	0	0	0	0	RESET
3	JESD BANK PAGE SEL[7:0]							
4	JESD BANK PAGE SEL[15:8]							
5	0	0	0	0	0	0	0	DISABLE BROADCAST
11	ANALOG BANK PAGE SEL							
MASTER PAGE (80h)								
20	PDN ADC CHA				PDN ADC CHB			
21	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	PDN ADC CHA				PDN ADC CHB			
24	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
39	HIGH FREQ 1	HIGH FREQ 0	0	0	0	0	0	0
3A	0	HIGH FREQ 2	0	0	0	0	0	0
4F	0	0	0	0	0	0	0	EN INPUT DC COUPLING
53	0	MASK SYSREF	0	0	0	0	EN SYSREF DC COUPLING	0
55	0	0	0	PDN MASK	0	0	0	0
56	0	0	0	0	0	HIGH FREQ 3	0	0
59	FOVR CHB	0	ALWAYS WRITE 1	0	0	0	0	0
ADC PAGE (0Fh)								
5F	FOVR THRESHOLD PROG							
MAIN DIGITAL PAGE (6800h)								
0	0	0	0	0	0	0	0	PULSE RESET
41	0	0	DECFIL MODE[3]	DECFIL EN	0	DECFIL MODE[2:0]		
42	0	0	0	0	0	NYQUIST ZONE		
43	0	0	0	0	0	0	0	FORMAT SEL
44	0	DIGITAL GAIN						
4B	0	0	FORMAT EN	0	0	0	0	0
4D	0	0	0	0	DEC MODE EN	0	0	0
4E	CTRL NYQUIST	0	0	0	0	0	0	0
52	BUS_ REORDER EN1	0	0	0	0	0	0	DIG GAIN EN
72	0	0	0	0	BUS_ REORDER EN2	0	0	0
AB	0	0	0	0	0	0	0	LSB SEL EN
AD	0	0	0	0	0	0	LSB SELECT	
F7	0	0	0	0	0	0	0	DIG RESET

Table 14. Register Map (continued)

REGISTER ADDRESS	REGISTER DATA							
A[11:0] (Hex)	7	6	5	4	3	2	1	0
JESD DIGITAL PAGE (6900h)								
0	CTRL K	0	0	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK DIS
1	SYNC REG	SYNC REG EN	JESD FILTER			JESD MODE		
2	LINK LAYER TESTMODE			LINK LAYER RPAT	LMFC MASK RESET	0	0	0
3	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
5	SCRAMBLE EN	0	0	0	0	0	0	0
6	0	0	0	FRAMES PER MULTI FRAME (K)				
7	0	0	0	0	SUBCLASS	0	0	0
16	1	0	0	LANE SHARE	0	0	0	0
31	DA_BUS_REORDER[7:0]							
32	DB_BUS_REORDER[7:0]							
JESD ANALOG PAGE (6A00h)								
12	SEL EMP LANE 1						0	0
13	SEL EMP LANE 0						0	0
14	SEL EMP LANE 2						0	0
15	SEL EMP LANE 3						0	0
16	0	0	0	0	0	0	JESD PLL MODE	
17	0	PLL RESET	0	0	0	0	0	0
1A	0	0	0	0	0	0	FOVR CHA	0
1B	JESD SWING			0	FOVR CHA EN	0	0	0

8.5.2 Example Register Writes

This section provides three different example register writes. Table 15 describes a global power-down register write, Table 16 describes the register writes when the default lane setting (eight active lanes per device) is changed to four active lanes (LMFS = 4211), and Table 17 describes the register writes for 2X decimation with four active lanes (LMFS = 4222).

Table 15. Global Power Down

ADDRESS (Hex)	DATA (Hex)	COMMENT
0-011h	80h	Set the master page
0-026h	C0h	Set the global power-down

Table 16. Two Lanes per Channel Mode (LMFS = 4211)

ADDRESS (Hex)	DATA (Hex)	COMMENT
4-004h	69h	Select the JESD digital page
4-003h	00h	Select the JESD digital page
6-001h	02h	Select the digital to 40X mode
4-004h	6Ah	Select the JESD analog page
6-016h	02h	Set the SerDes PLL to 40X mode

Table 17. 2X Decimation (LPF for Both Channels) with Four Active Lanes (LMFS = 4222)

ADDRESS (Hex)	DATA (Hex)	COMMENT
4-004h	68h	Select the main digital page (6800h)
4-003h	00h	Select the main digital page (6800h)
6-041h	12h	Set decimate-by-2 (low-pass filter)
6-04Dh	08h	Enable decimation filter control
6-072h	08h	BUS_REORDER EN2
6-052h	80h	BUS_REORDER EN1
6-000h	01h	Pulse the PULSE RESET bit (so that register writes to the main digital page go into effect).
6-000h	00h	
4-004h	69h	Select the JESD digital page (6900h)
4-003h	00h	Select the JESD digital page (6900h)
6-031h	0Ah	Output bus reorder for channel A
6-032h	0Ah	Output bus reorder for channel B
6-001h	31h	Program the JESD MODE and JESD FILTER register bits for LMFS = 4222.

8.5.3 Register Descriptions

8.5.3.1 General Registers

8.5.3.1.1 Register 0h (address = 0h)

Figure 83. Register 0h

7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Table 18. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0
6-1	0	W	0h	Must write 0
0	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0

8.5.3.1.2 Register 3h (address = 3h)

Figure 84. Register 3h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 19. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL[7:0]	R/W	0h	Program these bits to access the desired page in the JESD bank. 6800h = Main digital page selected 6900h = JESD digital page selected 6A00h = JESD analog page selected

8.5.3.1.3 Register 4h (address = 4h)

Figure 85. Register 4h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. Register 4h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL[15:8]	R/W	0h	Program these bits to access the desired page in the JESD bank. 6800h = Main digital page selected 6900h = JESD digital page selected 6A00h = JESD analog page selected

8.5.3.1.4 Register 5h (address = 5h)

Figure 86. Register 5h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DISABLE BROADCAST
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DISABLE BROADCAST	R/W	0h	0 = Normal operation; channel A and B are programmed as a pair 1 = Channel A and B can be individually programmed based on the CH bit

8.5.3.1.5 Register 11h (address = 11h)

Figure 87. Register 11h

7	6	5	4	3	2	1	0
ANALOG PAGE SELECTION							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 22. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANALOG BANK PAGE SEL	R/W	0h	Program these bits to access the desired page in the analog bank. Master page = 80h ADC page = 0Fh

8.5.3.2 Master Page (080h) Registers

8.5.3.2.1 Register 20h (address = 20h), Master Page (080h)

Figure 88. Register 20h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 23. Registers 20h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register bit 5 in address 26h. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
3-0	PDN ADC CHB	R/W	0h	

8.5.3.2.2 Register 21h (address = 21h), Master Page (080h)

Figure 89. Register 21h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 24. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
5-4	PDN BUFFER CHA	R/W	0h	
3-0	0	W	0h	Must write 0.

8.5.3.2.3 Register 23h (address = 23h), Master Page (080h)

Figure 90. Register 23h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 25. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
3-0	PDN ADC CHB	R/W	0h	

8.5.3.2.4 Register 24h (address = 24h), Master Page (080h)

Figure 91. Register 24h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 26. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
5-4	PDN BUFFER CHA	R/W	0h	
3-0	0	W	0h	Must write 0.

8.5.3.2.5 Register 26h (address = 26h), Master Page (080h)

Figure 92. Register 26h

7	6	5	4	3	2	1	0
GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 27. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL PDN	R/W	0h	Bit 6 (OVERRIDE PDN PIN) must be set before this bit can be programmed. 0 = Normal operation 1 = Global power-down via the SPI
6	OVERRIDE PDN PIN	R/W	0h	This bit ignores the power-down pin control. 0 = Normal operation 1 = Ignores inputs on the power-down pin
5	PDN MASK SEL	R/W	0h	This bit selects power-down mask 1 or mask 2. 0 = Power-down mask 1 1 = Power-down mask 2
4-0	0	W	0h	Must write 0

8.5.3.2.6 Register 39h (address = 39h), Master Page (080h)

Figure 93. Register 39h

7	6	5	4	3	2	1	0
HIGH FREQ 1	HIGH FREQ 0	0	0	0	0	0	0
R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
7	HIGH FREQ 1	R/W	0h	Set these bits (and the HIGH FREQ[3:2] bits) high when the input frequency > 400 MHz.
6	HIGH FREQ 0	R/W	0h	
5-0	0	W	0h	Must write 0

8.5.3.2.7 Register 3Ah (address = 3Ah), Master Page (080h)

Figure 94. Register 3Ah

7	6	5	4	3	2	1	0
0	HIGH FREQ 2	0	0	0	0	0	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register 3Ah Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	HIGH FREQ 2	R/W	0h	Set this bit (and the HIGH FREQ 3 and HIGH FREQ[1:0] bits) high when the input frequency > 400 MHz.
5-0	0	W	0h	Must write 0

8.5.3.2.8 Register 4Fh (address = 4Fh), Master Page (080h)

Figure 95. Register 4Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN INPUT DC COUPLING
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 30. Register 4Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	EN INPUT DC COUPLING	R/W	0h	This bit enables dc-coupling between the analog inputs and the driver by changing the internal biasing resistor between the analog inputs and VCM from 600 Ω to 5 kΩ. 0 = The dc-coupling support is disabled 1 = The dc-coupling support is enabled

8.5.3.2.9 Register 53h (address = 53h), Master Page (080h)

Figure 96. Register 53h

7	6	5	4	3	2	1	0
0	MASK SYSREF	0	0	0	0	EN SYSREF DC COUPLING	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register 53h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	MASK SYSREF	R/W	0h	0 = Normal operation 1 = Ignores the SYSREF input
5-2	0	W	0h	Must write 0
1	EN SYSREF DC COUPLING	R/W	0h	This bit enables a higher common-mode voltage input on the SYSREF signal (up to 1.6 V). 0 = Normal operation 1 = Enables a higher SYSREF common-mode voltage support
0	0	W	0h	Must write 0

8.5.3.2.10 Register 55h (address = 55h), Master Page (080h)

Figure 97. Register 55h

7	6	5	4	3	2	1	0
0	0	0	PDN MASK	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 55h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	PDN MASK	R/W	0h	This bit enables power-down via a register bit. 0 = Normal operation 1 = Power-down is enabled by powering down the internal blocks as specified in the selected power-down mask
3-0	0	W	0h	Must write 0

8.5.3.2.11 Register 56h (address = 56h), Master Page (080h)

Figure 98. Register 56h

7	6	5	4	3	2	1	0
0	0	0	0	0	HIGH FREQ 3	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 56h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2	HIGH FREQ 3	R/W	0h	Set this bit (and the HIGH FREQ[2:0] bits) high when the input frequency > 400 MHz.
1-0	0	W	0h	Must write 0

8.5.3.2.12 Register 59h (address = 59h), Master Page (080h)

Figure 99. Register 59h

7	6	5	4	3	2	1	0
FOVR CHB	0	ALWAYS WRITE 1	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 59h Field Descriptions

Bit	Field	Type	Reset	Description
7	FOVR CHB	W	0h	This bit outputs the FOVR signal for channel B on the SDOUT pin. 0 = Normal operation 1 = The FOVR signal is available on the SDOUT pin
6	0	W	0h	Must write 0
5	ALWAYS WRITE 1	R/W	0h	Must write 1
4-0	0	W	0h	Must write 0

8.5.3.3 ADC Page (0Fh) Register

8.5.3.3.1 Register 5F (addresses = 5F), ADC Page (0Fh)

Figure 100. Register 5F

7	6	5	4	3	2	1	0
FOVR THRESHOLD PROG							
R/W-E3h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 35. Register 5F Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOVR THRESHOLD PROG	R/W	E3h	Program the fast OVR thresholds together for channel A and B, as described in the *Overrange Indication* section.

8.5.3.4 Main Digital Page (6800h) Registers

8.5.3.4.1 Register 0h (address = 0h), Main Digital Page (6800h)

Figure 101. Register 0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PULSE RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 36. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	PULSE RESET	R/W	0h	This bit must be pulsed after power-up or after configuring registers in the main digital page of the JESD bank. Any register bits in the main digital page (6800h) take effect only after this bit is pulsed; see the *Start-Up Sequence* section for the correct sequence. 0 = Normal operation 0 → 1 → 0 = This bit is pulsed

8.5.3.4.2 Register 41h (address = 41h), Main Digital Page (6800h)

Figure 102. Register 41h

7	6	5	4	3	2	1	0
0	0	DECFIL MODE[3]	DECFIL EN	0	DECFIL MODE[2:0]		
W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 41h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	DECFIL MODE[3]	R/W	0h	This bit selects the decimation filter mode. Table 38 lists the bit settings. The decimation filter control (DEC MODE EN, register 4Dh, bit 3) and decimation filter enable (DECFIL EN, register 41h, bit 4) must be enabled.
4	DECFIL EN	R/W	0h	This bit enables the digital decimation filter. 0 = Normal operation, full rate output 1 = Digital decimation enabled
3	0	W	0h	Must write 0
2-0	DECFIL MODE[2:0]	R/W	0h	These bits select the decimation filter mode. Table 38 lists the bit settings. The decimation filter control (DEC MODE EN, register 4Dh, bit 3) and decimation filter enable (DECFIL EN, register 41h, bit 4) must be enabled.

Table 38. DECFIL MODE Bit Settings

BITS (5, 2-0)	FILTER MODE	DECIMATION
0000	Band-pass filter centered on $3 \times f_S / 16$	4X
0100	Band-pass filter centered on $5 \times f_S / 16$	4X
1000	Band-pass filter centered on $1 \times f_S / 16$	4X
1100	Band-pass filter centered on $7 \times f_S / 16$	4X
0010	Low-pass filter	2X
0110	High-pass filter	2X
0011	Low-pass filter with $f_S / 4$ mixer	4X (IQ)

8.5.3.4.3 Register 42h (address = 42h), Main Digital Page (6800h)

Figure 103. Register 42h

7	6	5	4	3	2	1	0
0	0	0	0	0	NYQUIST ZONE		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 39. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2-0	NYQUIST ZONE	R/W	0h	The Nyquist zone must be selected for proper interleaving correction. Nyquist refers to the device clock / 2. For a 1.0-GSPS device clock, the Nyquist frequency is 500 MHz. The CTRL NYQUIST register bit (register 4Eh, bit 7) must also be set. 000 = First Nyquist zone (0 MHz to 500 MHz) 001 = Second Nyquist zone (500 MHz to 1000 MHz) 010 = Third Nyquist zone (1000 MHz to 1500 MHz) All others = Not used

8.5.3.4.4 Register 43h (address = 43h), Main Digital Page (6800h)

Figure 104. Register 43h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FORMAT SEL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 40. Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	FORMAT SEL	R/W	0h	This bit changes the output format. Set the FORMAT EN bit to enable control using this bit. 0 = Twos complement 1 = Offset binary

8.5.3.4.5 Register 44h (address = 44h), Main Digital Page (6800h)

Figure 105. Register 44h

7	6	5	4	3	2	1	0
0	DIGITAL GAIN						
R/W-0h	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 41. Register 44h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must write 0
6-0	DIGITAL GAIN	R/W	0h	These bits set the digital gain setting. The DIG GAIN EN register bit (register 52h, bit 0) must be enabled to use these bits. Gain in dB = 20log (digital gain / 32). 7Fh = 127 equals a digital gain of 9.5 dB.

8.5.3.4.6 Register 4Bh (address = 4Bh), Main Digital Page (6800h)

Figure 106. Register 4Bh

7	6	5	4	3	2	1	0
0	0	FORMAT EN	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 42. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	FORMAT EN	R/W	0h	This bit enables control for data format selection using the FORMAT SEL register bit. 0 = Default, output is in twos complement format 1 = Output is in offset binary format after the FORMAT SEL bit is set
4-0	0	W	0h	Must write 0

8.5.3.4.7 Register 4Dh (address = 4Dh), Main Digital Page (6800h)

Figure 107. Register 4Dh

7	6	5	4	3	2	1	0
0	0	0	0	DEC MOD EN	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 43. Register 4Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	DEC MOD EN	R/W	0h	This bit enables control of the decimation filter mode via the DECFIL MODE[3:0] register bits. 0 = Default 1 = Decimation mode control is enabled
2-0	0	W	0h	Must write 0

8.5.3.4.8 Register 4Eh (address = 4Eh), Main Digital Page (6800h)

Figure 108. Register 4Eh

7	6	5	4	3	2	1	0
CTRL NYQUIST	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 44. Register 4Eh Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL NYQUIST	R/W	0h	This bit enables selecting the Nyquist zone using register 42h, bits 2-0. 0 = Selection disabled 1 = Selection enabled
6-0	0	W	0h	Must write 0

8.5.3.4.9 Register 52h (address = 52h), Main Digital Page (6800h)

Figure 109. Register 52h

7	6	5	4	3	2	1	0
BUS_REORDER EN1	0	0	0	0	0	0	DIG GAIN EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 45. Register 52h Field Descriptions

Bit	Field	Type	Reset	Description
7	BUS_REORDER EN1	R/W	0h	Must write 1 in DDC mode only.
6-1	0	W	0h	Must write 0
0	DIG GAIN EN	R/W	0h	This bit enables selecting the digital gain for register 44h. 0 = Digital gain disabled 1 = Digital gain enabled

8.5.3.4.10 Register 72h (address = 72h), Main Digital Page (6800h)

Figure 110. Register 72h

7	6	5	4	3	2	1	0
0	0	0	0	BUS_REORDER EN2	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 46. Register 72h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	BUS_REORDER EN2	R/W	0h	Must write 1 in DDC mode only.
2-0	0	W	0h	Must write 0

8.5.3.4.11 Register ABh (address = ABh), Main Digital Page (6800h)

Figure 111. Register ABh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LSB SEL EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register ABh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	LSB SEL EN	R/W	0h	This bit enables control for the LSB SELECT register bit. 0 = Default 1 = LSB of the 16-bit data (12-bit ADC data padded with four 0s as the LSBs) can be programmed as fast OVR using the LSB SELECT register bit.

8.5.3.4.12 Register ADh (address = ADh), Main Digital Page (6800h)

Figure 112. Register ADh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LSB SELECT	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 48. Register ADh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	LSB SELECT	R/W	0h	These bits enable the output of the FOVR flag instead of the output data LSB. Ensure that the LSB SEL EN register bit is set to 1. 00 = Output is 16-bit data (12-bit ADC data padded with four 0s as the LSBs) 11 = The LSB of the 16-bit output data is replaced by the FOVR information for each channel

8.5.3.4.13 Register F7h (address = F7h), Main Digital Page (6800h)

Figure 113. Register F7h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Table 49. Register F7h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DIG RESET	W	0h	This bit is the self-clearing reset for the digital block and does not include interleaving correction. 0 = Normal operation 1 = Digital reset

8.5.3.5 JESD Digital Page (6900h) Registers

8.5.3.5.1 Register 0h (address = 0h), JESD Digital Page (6900h)

Figure 114. Register 0h

7	6	5	4	3	2	1	0
CTRL K	0	0	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK DIS
R/W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 50. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL K	R/W	0h	This bit is the enable bit for a number of frames per multiframe. 0 = Default is five frames per multiframe 1 = Frames per multiframe can be set in register 06h
6-5	0	W	0h	Must write 0
4	TESTMODE EN	R/W	0h	This bit generates the long transport layer test pattern mode, as per section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
3	FLIP ADC DATA	R/W	0h	0 = Normal operation 1 = Output data order is reversed: MSB to LSB.
2	LANE ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.3) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
1	FRAME ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.7) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
0	TX LINK DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when $\overline{\text{SYNC}}$ is deasserted. 0 = Normal operation 1 = ILA disabled

8.5.3.5.2 Register 1h (address = 1h), JESD Digital Page (6900h)

Figure 115. Register 1h

7	6	5	4	3	2	1	0
SYNC REG	SYNC REG EN	JESD FILTER			JESD MODE		
R/W-0h	R/W-0h	R/W-0h			R/W-01h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 51. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC REG	R/W	0h	This bit is the register control for the sync request. 0 = Normal operation 1 = ADC output data are replaced with K28.5 characters; the SYNC REG EN register bit must also be set to 1
6	SYNC REG EN	R/W	0h	This bit enables register control for the sync request. 0 = Use the $\overline{\text{SYNC}}$ pin for sync requests 1 = Use the SYNC REG register bit for sync requests
5-3	JESD FILTER	R/W	0h	These bits and the JESD MODE bits set the correct LMFS configuration for the JESD interface. The JESD FILTER setting must match the configuration in the decimation filter page. 000 = Filter bypass mode See Table 52 for valid combinations for register bits JESD FILTER along with JESD MODE.
2-0	JESD MODE	R/W	01h	These bits select the number of serial JESD output lanes per ADC. The JESD PLL MODE register bit located in the JESD analog page must also be set accordingly. 001 = Default after reset(Eight active lanes) See Table 52 for valid combinations for register bits JESD FILTER along with JESD MODE.

Table 52. Valid Combinations for JESD FILTER and JESD MODE Bits

REGISTER BIT JESD FILTER	REGISTER BIT JESD MODE	DECIMATION FACTOR	NUMBER OF ACTIVE LANES PER DEVICE
000	100	No decimation	Four lanes are active
000	010	No decimation	Four lanes are active
000	001	No decimation (default after reset)	Eight lanes are active
111	001	4X (IQ)	Four lanes are active
110	001	2X	Four lanes are active
110	010	2X	Two lanes are active
100	001	4X	Two lanes are active
111	010	4X (IQ)	Two lanes are active
100	010	4X	One lane is active

8.5.3.5.3 Register 2h (address = 2h), JESD Digital Page (6900h)

Figure 116. Register 2h

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAYER RPAT	LMFC MASK RESET	0	0	0
R/W-0h			R/W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 53. Register 2h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK LAYER TESTMODE	R/W	0h	These bits generate a pattern as per section 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 100 = 12-octet RPAT jitter pattern All others = Not used
4	LINK LAYER RPAT	R/W	0h	This bit changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100). 0 = Normal operation 1 = Changes disparity
3	LMFC MASK RESET	R/W	0h	This bit masks the LMFC reset coming to the digital block. 0 = LMFC reset is not masked 1 = Ignore the LMFC reset request
2-0	0	W	0h	Must write 0

8.5.3.5.4 Register 3h (address = 3h), JESD Digital Page (6900h)

Figure 117. Register 3h

7	6	5	4	3	2	1	0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
R/W-0h	R/W-0h					R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 54. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE LMFC COUNT	R/W	0h	This bit forces the LMFC count. 0 = Normal operation 1 = Enables using a different starting value for the LMFC counter
6-2	MASK SYSREF	R/W	0h	When SYSREF transmits to the digital block, the LMFC count resets to 0 and K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the receiver can be synchronized early because the LANE ALIGNMENT SEQUENCE is received early. The FORCE LMFC COUNT register bit must be enabled.
1-0	RELEASE ILANE SEQ	R/W	0h	These bits delay the generation of the lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3

8.5.3.5.5 Register 5h (address = 5h), JESD Digital Page (6900h)

Figure 118. Register 5h

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-Undefined	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 55. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
7	SCRAMBLE EN	R/W	Undefined	This bit is the scramble enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
6-0	0	W	0h	Must write 0

8.5.3.5.6 Register 6h (address = 6h), JESD Digital Page (6900h)

Figure 119. Register 6h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTI FRAME (K)				
W-0h	W-0h	W-0h	R/W-8h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 56. Register 6h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4-0	FRAMES PER MULTI FRAME (K)	R/W	8h	These bits set the number of multiframes. Actual K is the value in hex + 1 (that is, 0Fh is K = 16).

8.5.3.5.7 Register 7h (address = 7h), JESD Digital Page (6900h)

Figure 120. Register 7h

7	6	5	4	3	2	1	0
0	0	0	0	SUBCLASS	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-1h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 57. Register 7h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	SUBCLASS	R/W	1h	This bit sets the JESD204B subclass. 000 = Subclass 0 is backward compatible with JESD204A 001 = Subclass 1 deterministic latency using the SYSREF signal
2-0	0	W	0h	Must write 0

8.5.3.5.8 Register 16h (address = 16h), JESD Digital Page (6900h)

Figure 121. Register 16h

7	6	5	4	3	2	1	0
1	0	0	LANE SHARE	0	0	0	0
W-1h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 58. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7	1	W	1h	Must write 1
6-5	0	W	0h	Must write 0
4	LANE SHARE	R/W	0h	When using decimate-by-4, the data of both channels are output over one lane (LMFS = 1241). 0 = Normal operation (each channel uses one lane) 1 = Lane sharing is enabled, both channels share one lane (LMFS = 1241)
3-0	0	W	0h	Must write 0

8.5.3.5.9 Register 31h (address = 31h), JESD Digital Page (6900h)

Figure 122. Register 31h

7	6	5	4	3	2	1	0
DA_BUS_REORDER[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 59. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DA_BUS_REORDER[7:0]	R/W	0h	Use these bits to program output connections between data streams and output lanes in decimate-by-2 and decimate-by-4 mode. Table 13 lists the supported combinations of these bits.

8.5.3.5.10 Register 32h (address = 32h), JESD Digital Page (6900h)

Figure 123. Register 32h

7	6	5	4	3	2	1	0
DB_BUS_REORDER[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 60. Register 32h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DB_BUS_REORDER[7:0]	R/W	0h	Use these bits to program output connections between data streams and output lanes in decimate-by-2 and decimate-by-4 mode. Table 13 lists the supported combinations of these bits.

8.5.3.6 JESD Analog Page (6A00h) Registers

8.5.3.6.1 Registers 12h-5h (addresses = 12h-5h), JESD Analog Page (6A00h)

Figure 124. Register 12h

7	6	5	4	3	2	1	0
SEL EMP LANE 1						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 125. Register 13h

7	6	5	4	3	2	1	0
SEL EMP LANE 0						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 126. Register 14h

7	6	5	4	3	2	1	0
SEL EMP LANE 2						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 127. Register 15h

7	6	5	4	3	2	1	0
SEL EMP LANE 3						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 61. Registers 12h-15h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SEL EMP LANE x (where x = 1, 0, 2, or 3)	R/W	0h	These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in decibels (dB) is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 = 0 dB 1 = –1 dB 3 = –2 dB 7 = –4.1 dB 15 = –6.2 dB 31 = –8.2 dB 63 = –11.5 dB
1-0	0	W-0h	0h	Must write 0

8.5.3.6.2 Register 16h (address = 16h), JESD Analog Page (6A00h)

Figure 128. Register 16h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	JESD PLL MODE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 62. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	JESD PLL MODE	R/W	0h	These bits select the JESD PLL multiplication factor and must match the JESD MODE setting. 00 = 20X mode 01 = Not used 10 = 40X mode 11 = Not used See Table 13 for a programming summary of the DDC modes and JESD link configuration.

8.5.3.6.3 Register 17h (address = 17h), JESD Analog Page (6A00h)

Figure 129. Register 17h

7	6	5	4	3	2	1	0
0	PLL RESET	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 63. Register 17h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	PLL RESET	R/W	0h	Pulse this bit after powering up the device; see Table 66. 0 = Default 0 → 1 → 0 = The PLL RESET bit is pulsed.
5-0	0	W	0h	Must write 0

8.5.3.6.4 Register 1Ah (address = 1Ah), JESD Analog Page (6A00h)

Figure 130. Register 1Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FOVR CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 64. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	FOVR CHA	R/W	0h	This bit outputs the FOVR signal for channel A on the PDN pin. FOVR CHA EN (register 1Bh, bit 3) must be enabled for this bit to function. 0 = Normal operation 1 = The FOVR signal of channel A is available on the PDN pin
0	0	W	0h	Must write 0

8.5.3.6.5 Register 1Bh (address = 1Bh), JESD Analog Page (6A00h)

Figure 131. Register 1Bh

7	6	5	4	3	2	1	0
JESD SWING			0	FOVR CHA EN	0	0	0
R/W-0h			W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 65. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	JESD SWING	R/W	0h	These bits select the output amplitude V_{OD} (mV_{PP}) of the JESD transmitter (for all lanes). 0 = 860 mV_{PP} 1 = 810 mV_{PP} 2 = 770 mV_{PP} 3 = 745 mV_{PP} 4 = 960 mV_{PP} 5 = 930 mV_{PP} 6 = 905 mV_{PP} 7 = 880 mV_{PP}
4	0	W	0h	Must write 0
3	FOVR CHA EN	R/W	0h	This bit enables overwrites of the PDN pin with the FOVR signal from channel A. 0 = Normal operation 1 = PDN is overwritten
2-0	0	W	0h	Must write 0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Start-Up Sequence

The steps described in Table 66 are recommended as the power-up sequence with the ADS54J20 in 20X mode (LMFS = 8224).

Table 66. Initialization Sequence

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
1	Power-up the device	Bring up the supplies to IOVDD = 1.15 V, DVDD = AVDD = 1.9 V, and AVDD3V = 3.0 V.	—	These supplies can be brought up in any order.
2	Reset the device	**Hardware reset**		
		Apply a hardware reset by pulsing pin 48 (low → high → low).		A hardware reset clears all registers to their default values.
		Register writes are equivalent to a hardware reset.		—
		Write address 0-000h with 81h.	General register	Reset registers in the ADC and master pages of the analog bank.
				This bit is a self-clearing bit.
		Write address 4-001h with 00h and address 4-002h with 00h.	Unused page	Clear any unwanted content from the unused pages of the JESD bank.
		Write address 4-003h with 00h and address 4-004h with 68h.	—	Select the main digital page of the JESD bank.
		Write address 6-0F7h with 01h for channel A.	Main digital page (JESD bank)	Use the DIG RESET register bit to reset all pages in the JESD bank.
				This bit is a self-clearing bit.
		Write address 6-000h with 01h, then address 6-000h with 00h.		Pulse the PULSE RESET register bit for channel A.
3	Performance modes	Write address 0-011h with 80h.	—	Select the master page of the analog bank.
		Write address 0-059h with 20h.	Master page (analog bank)	Set the ALWAYS WRITE 1 bit.
		Write address 0-039h with C0h. Write address 0-03Ah with 40h. Write address 0-056h with 04h.		HIGH FREQ[3:0]. Set these register bits for better SFDR when input frequency > 400 MHz.
4	Program desired registers for decimation options and JESD link configuration	**Default register writes for DDC modes and JESD link configuration (LMFS = 8224).**		
		Write address 4-003h with 00h and address 4-004h with 69h.	—	Select the JESD digital page.
		Write address 6-000h with 80h.	JESD digital page (JESD bank)	Set the CTRL K bit for both channels by programming K according to the SYSREF signal later on in the sequence.
		JESD link is configured with LMFS = 8224 by default with no decimation.		See Table 13 for configuring the JESD digital page registers for the desired LMFS and programming appropriate DDC mode.
		Write address 4-003h with 00h and address 4-004h with 6Ah.	—	Select the JESD analog page.
		JESD link is configured with LMFS = 8224 by default with no decimation.	JESD analog page (JESD bank)	See Table 13 for configuring the JESD analog page registers for the desired LMFS and programming appropriate DDC mode.
		Write address 6-017h with 40h.		PLL reset.
		Write address 6-017h with 00h.		PLL reset.
		Write address 4-003h with 00h and address 4-004h with 68h.	—	Select the main digital page.
		JESD link is configured with LMFS = 8224 by default with no decimation.	Main digital page (JESD bank)	See Table 13 for configuring the main digital page registers for the desired LMFS and programming appropriate DDC mode.
		Write address 6-000h with 01h and address 6-000h with 00h.		Pulse the PULSE RESET register bit. All settings programmed in the main digital page take effect only after this bit is pulsed.

Table 66. Initialization Sequence (continued)

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
5	Set the value of K and the SYSREF signal frequency accordingly	Write address 4-003h with 00h and address 4-004h with 69h.	—	Select the JESD digital page.
		Write address 6-006h with XXh (choose the value of K).	JESD digital page (JESD bank)	See the *SYSREF Signal* section to choose the correct frequency for SYSREF.
6	JESD lane alignment	Pull the SYNCB pin (pin 63) low.	—	Transmit K28.5 characters.
		Pull the SYNCB pin high.		After the receiver is synchronized, initiate an ILA phase and subsequent transmissions of ADC data.

9.1.2 Hardware Reset

Figure 132 and Table 67 show the timing for a hardware reset.

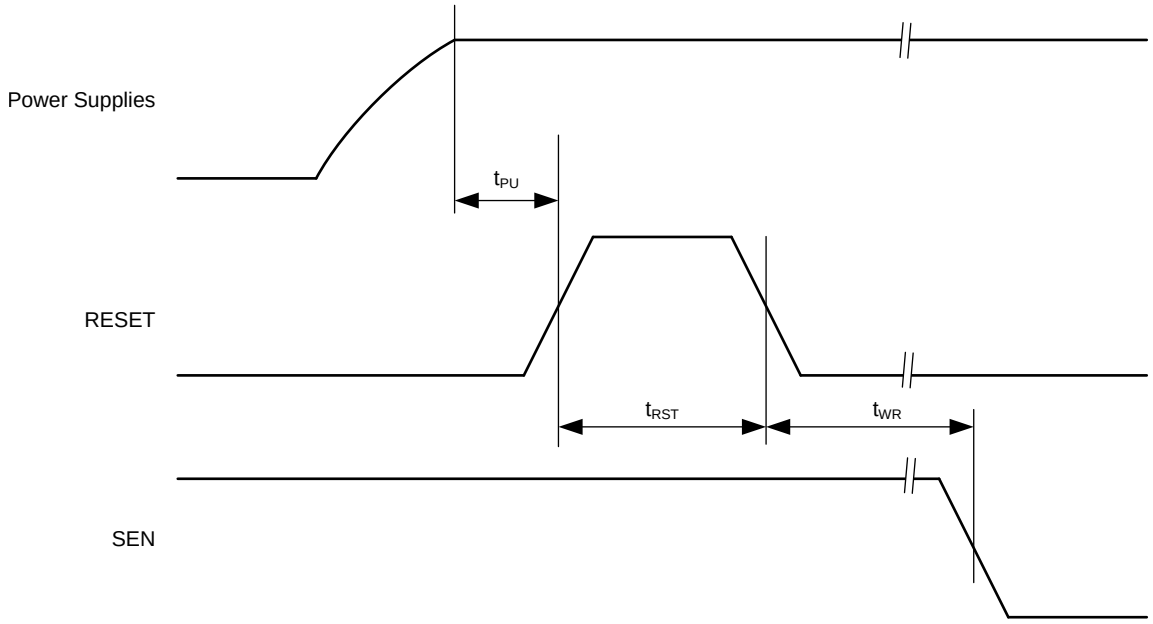


Figure 132. Hardware Reset Timing Diagram

Table 67. Timing Requirements for Figure 132

		MIN	TYP	MAX	UNIT
t_{PU}	Power-on delay from power-up to an active high RESET pulse	1			ms
t_{RST}	Reset pulse duration: active high RESET pulse duration	10			ns
t_{WR}	Register write delay from RESET disable to SEN active	100			ns

9.1.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter, as shown in Equation 4. The quantization noise is typically not noticeable in pipeline converters and is 74 dBFS for a 12-bit ADC. The thermal noise limits SNR at low input frequencies and the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20log\sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (4)$$

The SNR limitation resulting from sample clock jitter can be calculated by Equation 5:

$$SNR_{Jitter}[dBc] = -20log(2\pi \times f_{in} \times T_{Jitter}) \quad (5)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (130 f_S) is set by the noise of the clock input buffer and the external clock jitter. T_{Jitter} can be calculated by Equation 6:

$$T_{Jitter} = \sqrt{\left(T_{Jitter,\ Ext\_Clock\_Input}\right)^2 + \left(T_{Aperture\_ADC}\right)^2} \quad (6)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input. A faster clock slew rate also improves the ADC aperture jitter.

The ADS54J20 has a thermal noise of approximately 71.1 dBFS and an internal aperture jitter of 120 f_S. SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 133.

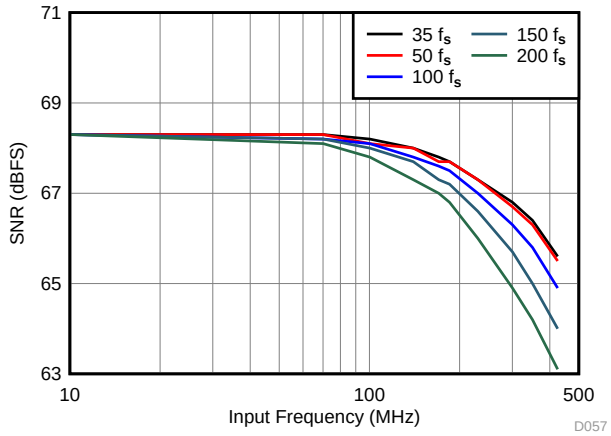
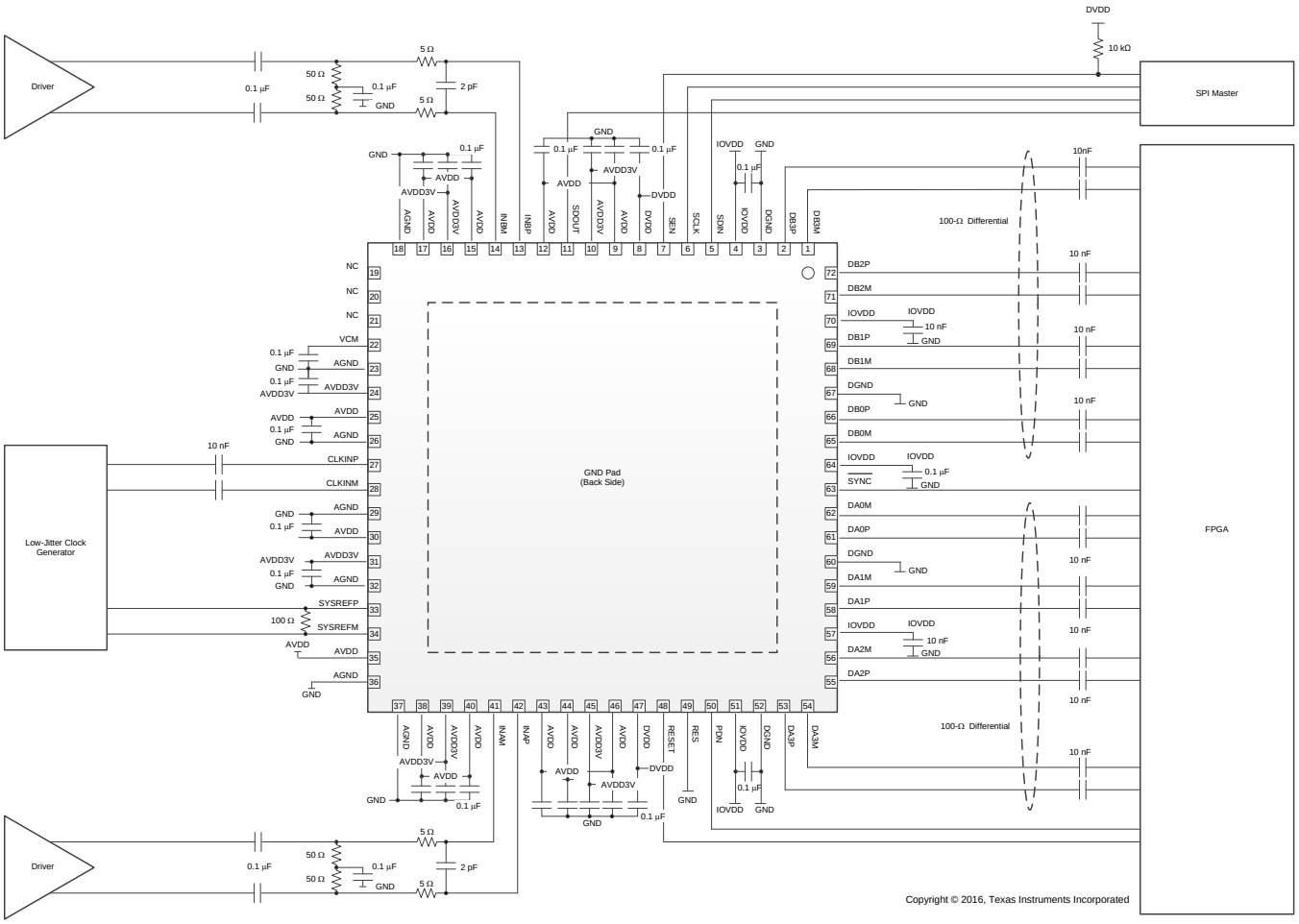


Figure 133. SNR versus Input Frequency and External Clock Jitter

9.2 Typical Application

The ADS54J20 is designed for wideband receiver applications demanding excellent dynamic range over a large input frequency range. A typical schematic for an ac-coupled receiver is shown in Figure 134.



NOTE: GND = AGND and DGND are connected in the PCB layout.

Figure 134. AC-Coupled Receiver

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Transformer-Coupled Circuits

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 300 MHz to achieve good phase and amplitude balances at the ADC inputs. When designing dc-driving circuits, the ADC input impedance must be considered. Figure 135 and Figure 136 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) across the ADC input pins.

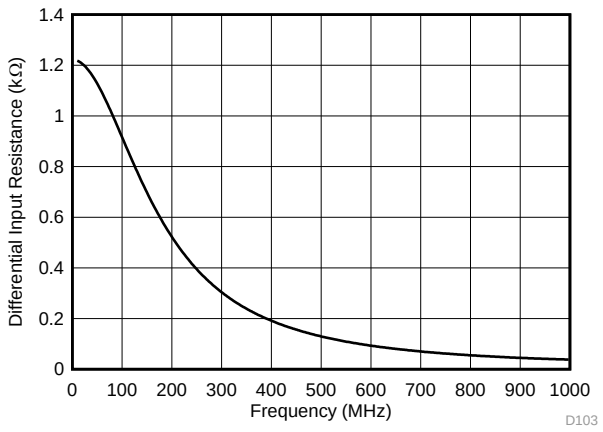


Figure 135. R_{IN} vs Input Frequency

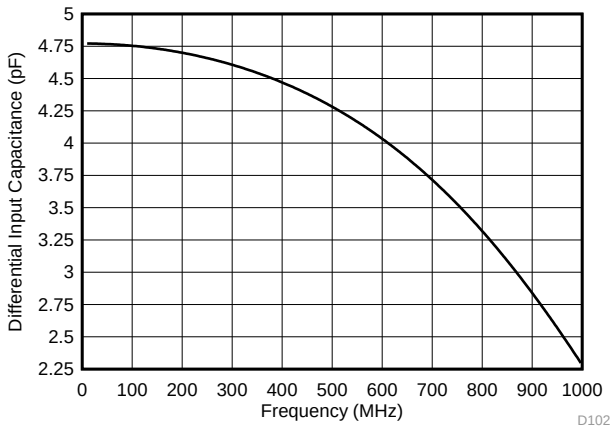


Figure 136. C_{IN} vs Input Frequency

By using the simple drive circuit of Figure 137, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

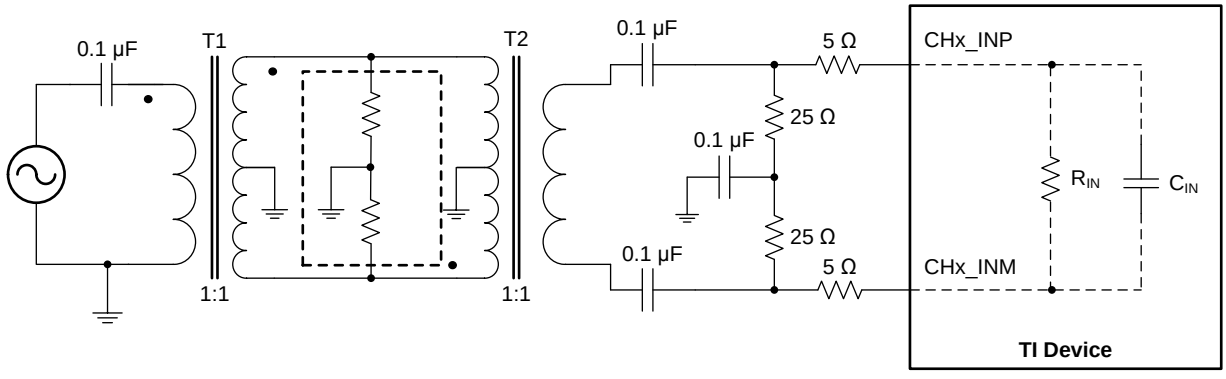


Figure 137. Input Drive Circuit

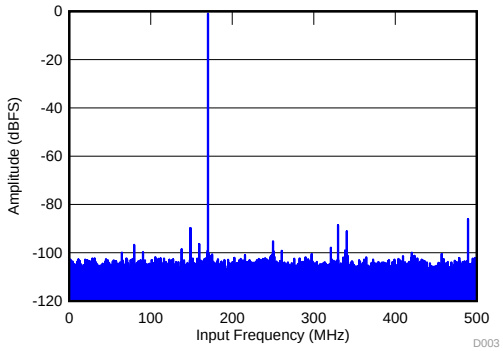
9.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 137.

Typical Application (continued)

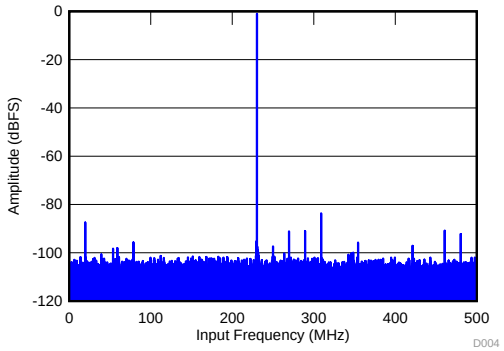
9.2.3 Application Curves

Figure 138 and Figure 139 show the typical performance at 170 MHz and 230 MHz, respectively.



SNR = 67.8 dBFS, SINAD = 67.7 dBFS,
SFDR = 86 dBc, THD = 81 dBc, IL spur = 88 dBc,
non HD2, HD3 spur = 89 dBc

Figure 138. FFT for 170-MHz Input Signal



SNR = 67.4 dBFS, SINAD = 67.2 dBFS,
IL spur = 87 dBc, SFDR = 84 dBc, THD = 82 dBc,
non HD2, HD3 spur = 90 dBc

Figure 139. FFT for 230-MHz Input Signal

10 Power Supply Recommendations

The device requires a 1.9-V nominal supply for DVDD, a 1.9-V nominal supply for AVDD, and a 3.0-V nominal supply for AVDD3V. There is no specific sequence for power-supply requirements during device power-up. AVDD, DVDD, and AVDD3V can power-up in any order.

11 Layout

11.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 140. The *ADS54J20EVM User's Guide* (SLAU687), provides a complete layout of the EVM. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as illustrated in the reference layout of Figure 140 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 140 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDDD3V), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

11.2 Layout Example

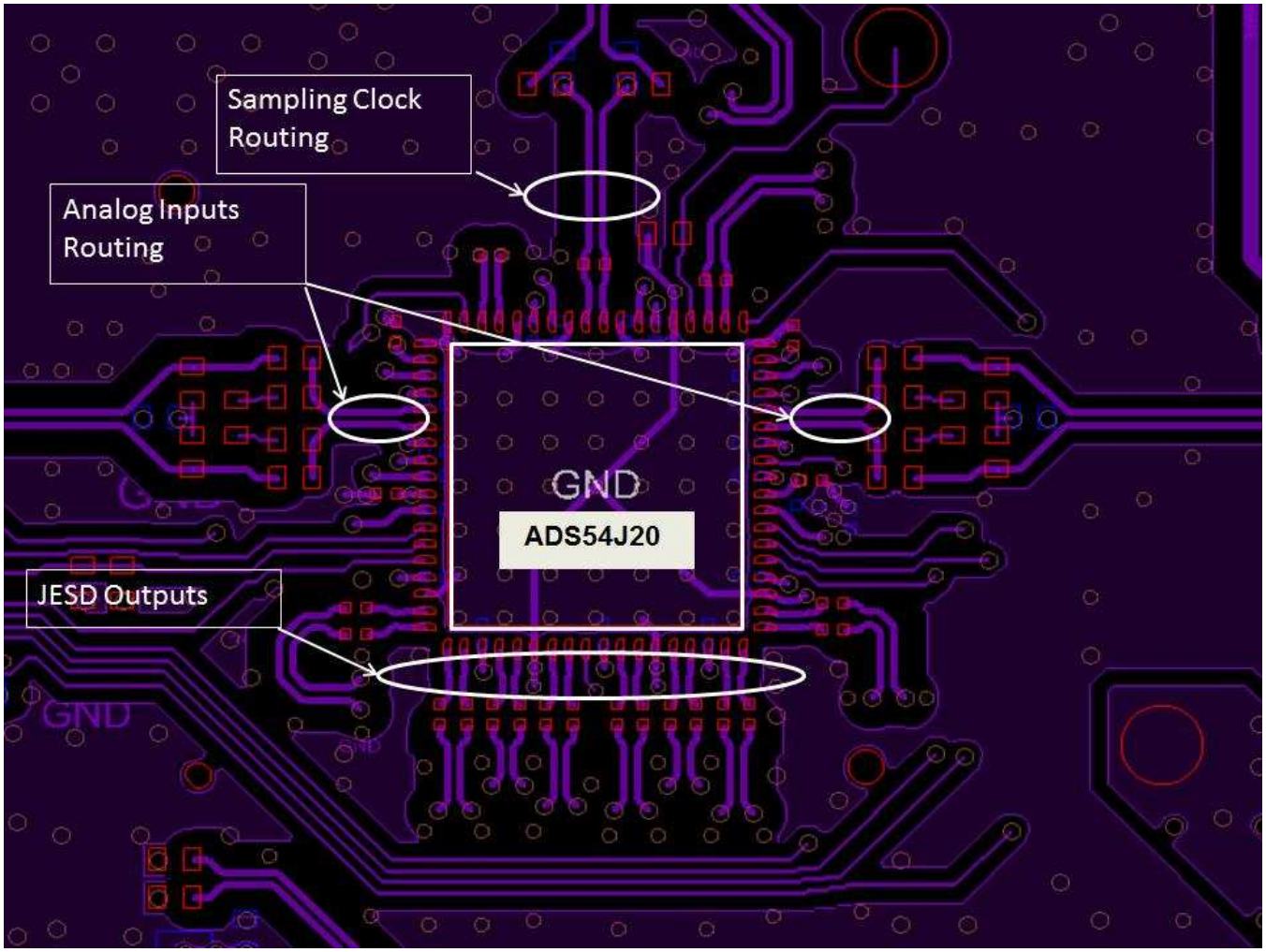


Figure 140. ADS54J20EVM Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

『ADS54J20EVMユーザー・ガイド』、SLAU687

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS54J20IRMP	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J20
ADS54J20IRMP.A	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J20
ADS54J20IRMPG4	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J20
ADS54J20IRMPG4.A	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J20
ADS54J20IRMPT	Active	Production	VQFN (RMP) | 72	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J20
ADS54J20IRMPT.A	Active	Production	VQFN (RMP) | 72	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J20

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

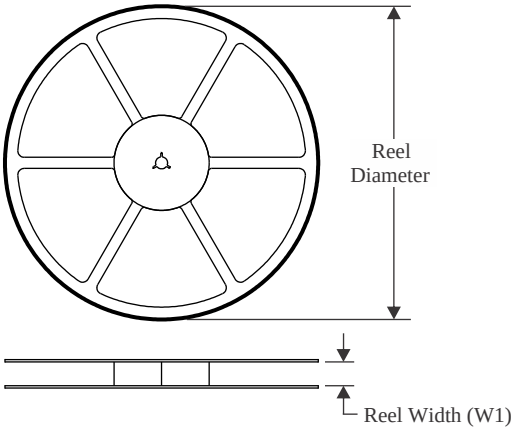
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

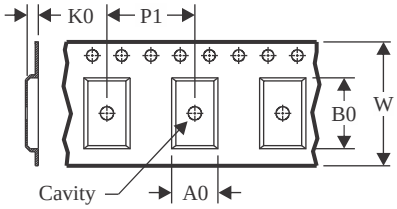
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

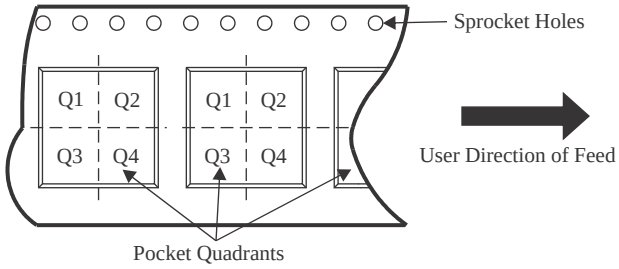


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

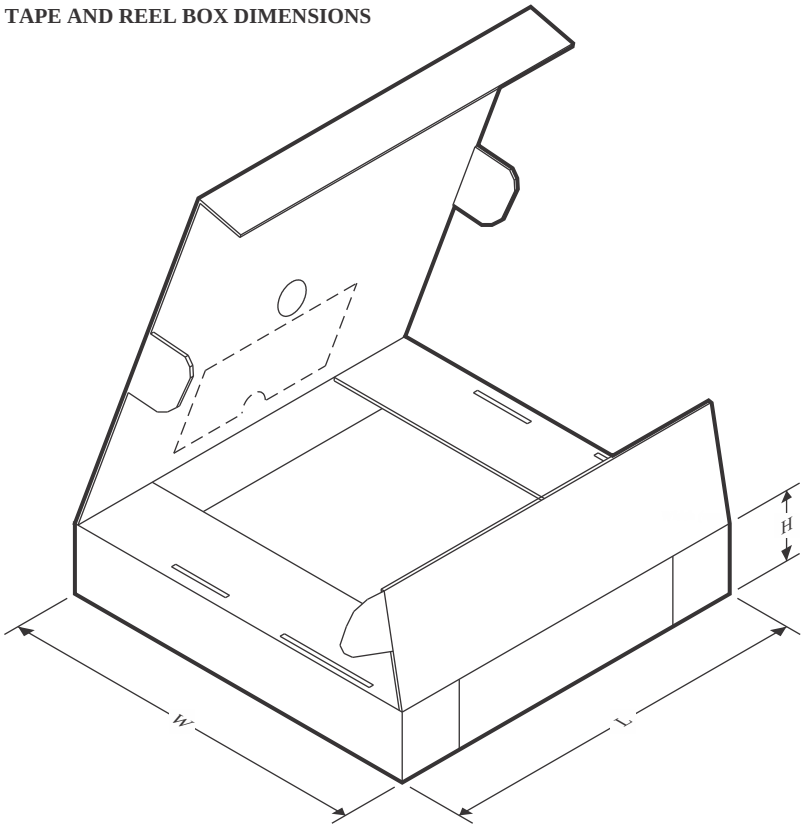
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS54J20IRMPT	VQFN	RMP	72	250	180.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2

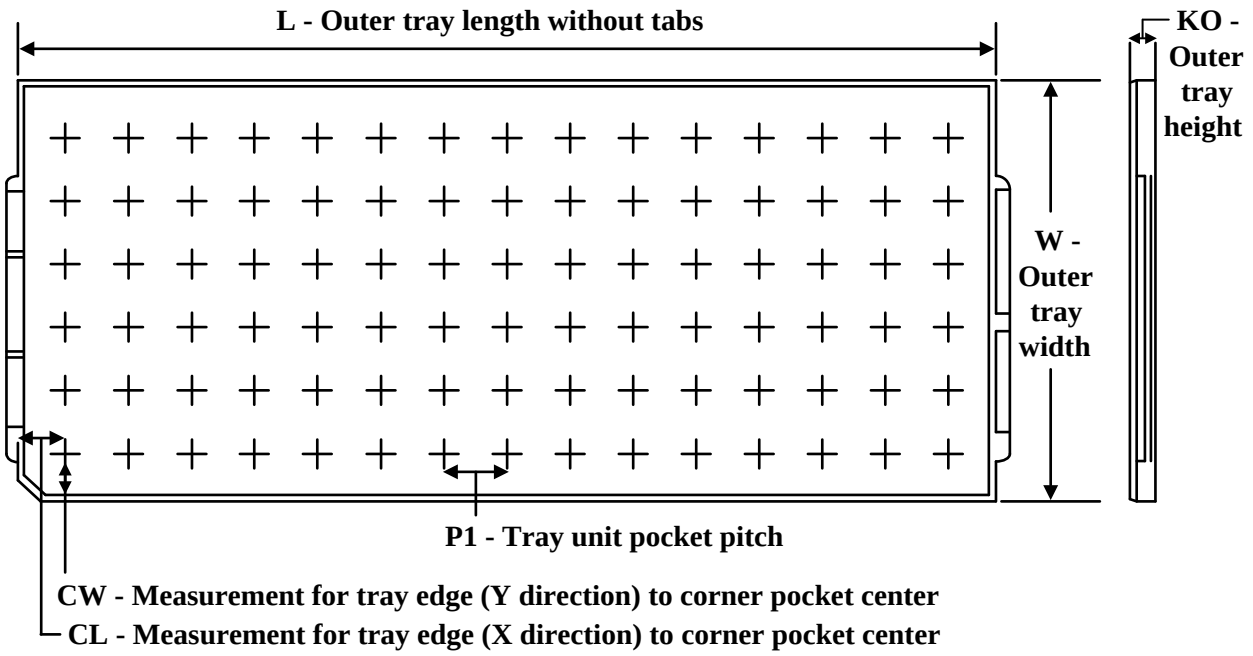
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS54J20IRMPT	VQFN	RMP	72	250	213.0	191.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

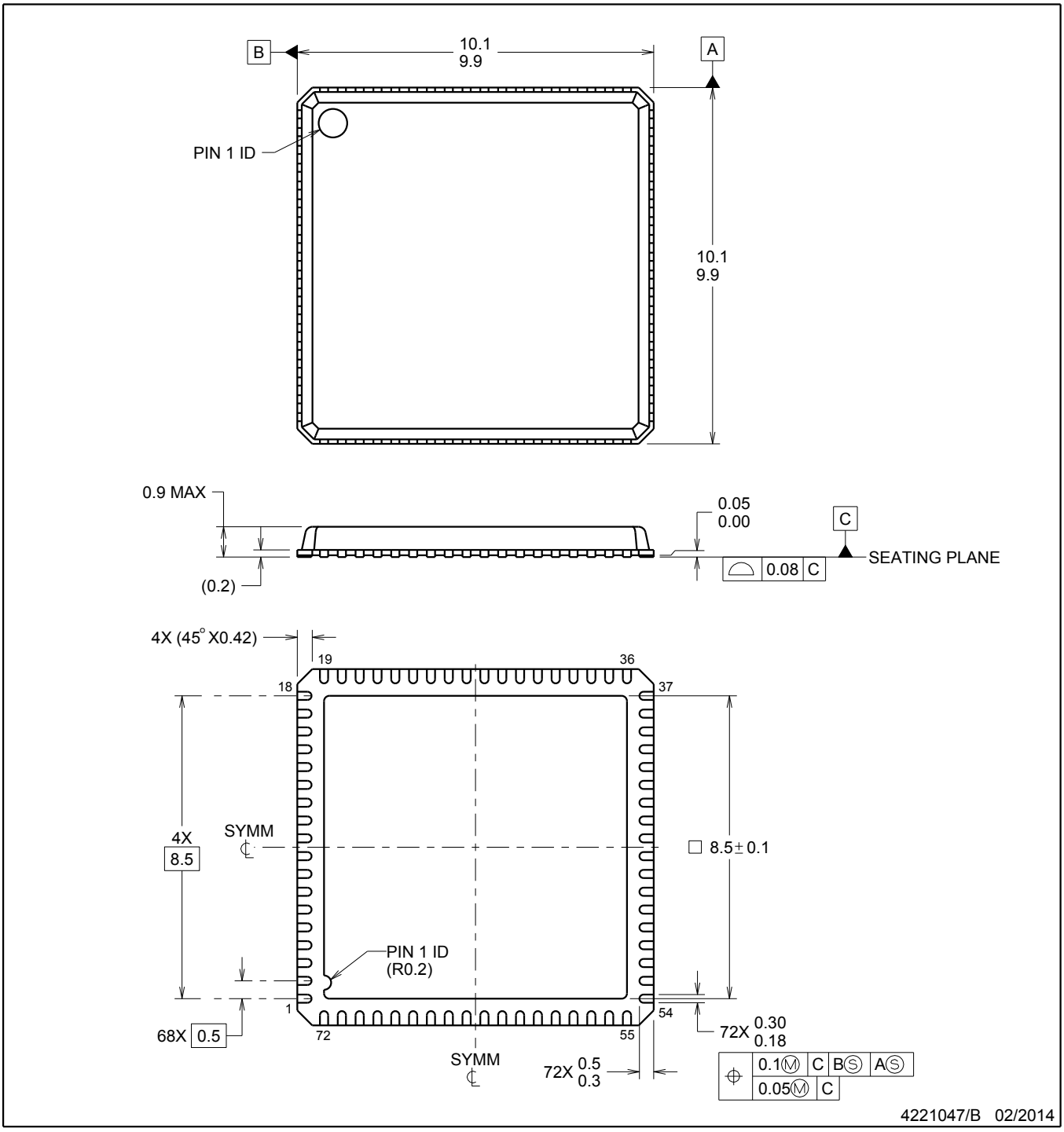
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS54J20IRMP	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADS54J20IRMP.A	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADS54J20IRMPG4	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADS54J20IRMPG4.A	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95

PACKAGE OUTLINE

RMP0072A

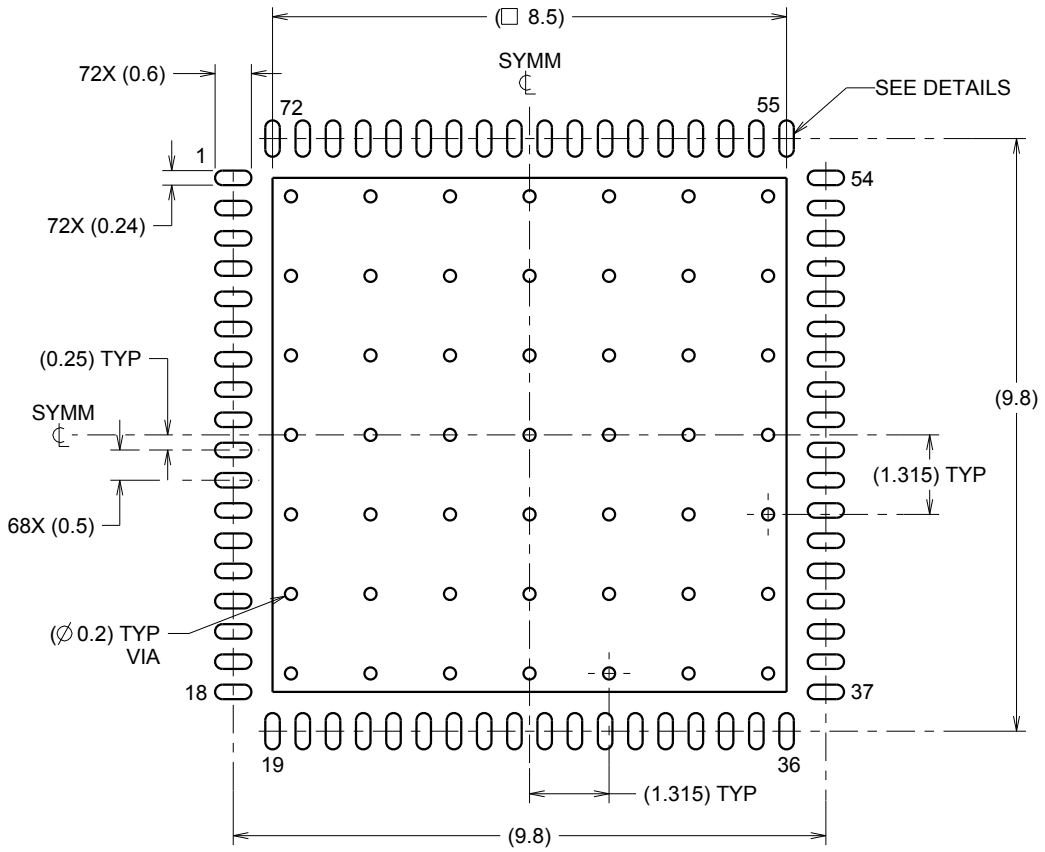
VQFN - 0.9 mm max height

VQFN

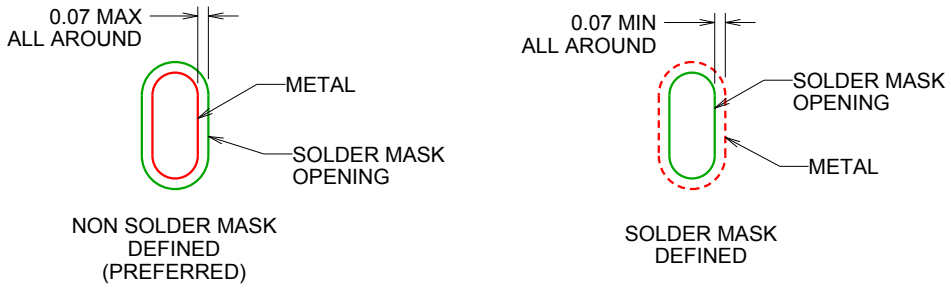


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

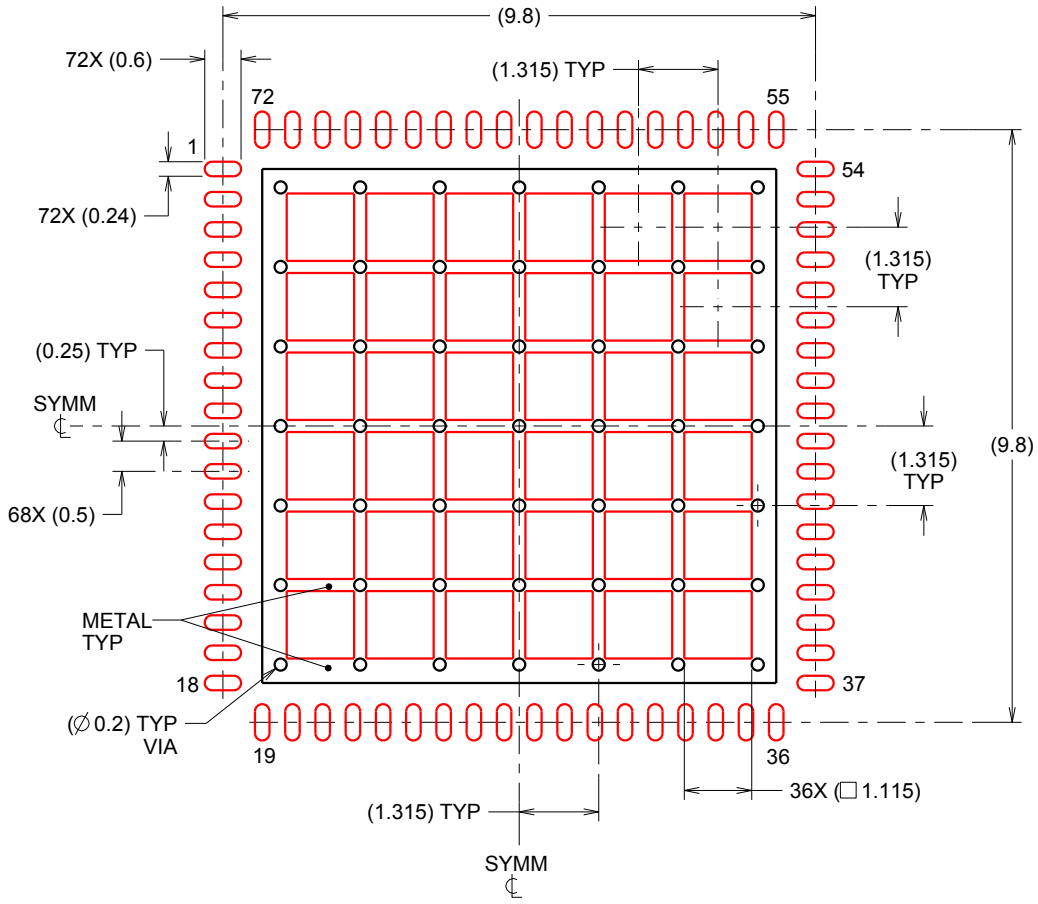


SOLDER MASK DETAILS

4221047/B 02/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4221047/B 02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265