Texas Instruments

ADS1287
JAJSHV5B – JUNE 2017 – REVISED AUGUST 2019

ADS1287 低消費電力、1000SPS、広帯域幅 アナログ/デジタル・コンバータ、プログラム可能なゲイン・アンプ搭載

1 特長

- 動作モードを選択可能
- 高分解能モード:
  - SNR: 113dB (1000SPS、ゲイン = 1)
  - 消費電力: 4.5mW
- 低消費電力モード
  - SNR: 110dB (1000SPS、ゲイン = 1)
  - 消費電力: 2.4mW
- THD: -115dB
- CMRR: 115dB
- 高インピーダンスのCMOS PGA
  - ゲイン: 1、2、4、8、16
- データ・レート: 62.5SPS～1000SPS
- 柔軟なデジタル・フィルタ:
  - Sinc + FIR + IIR (選択可能)
  - リニアおよび最小位相応答
  - プログラム可能なハイパス・フィルタ
- オフセットおよびゲインの較正
- 同期制御
- SPI互換のインターフェイス
- アナログ電源: 5Vまたは±2.5V
- デジタル電源: 2.5V～3.3V

2 アプリケーション

- エネルギー調査
- 受動的地震波観測
- ポータブル機器

3 概要

ADS1287デバイスは低消費電力のアナログ/デジタル・コンバータ(ADC)で、プログラム可能なゲイン・アンプ(PGA)と有限インパルス応答(FIR)デジタル・フィルタが内蔵されています。このADCは、高精度のデジタル化と低消費電力が要求される地震関連機器の厳しい要件に適しています。

このADCはゲインをプログラム可能で、高インピーダンスの相補形金属酸化膜半導体(CMOS)アンプが搭載されており、広い範囲の入力信号(±2.5V～±0.156V)でジオホン・センサやハイドロホン・センサをADCへ直接接続するために適しています。

このADCには4次の、本質的に安定したデルタ-シグマ(ΔΣ)変調器が内蔵されています。変調器のデジタル出力は内部のFIRデジタル・フィルタによってフィルタ処理とデシメーションが行われ、ADC変換結果が生成されます。

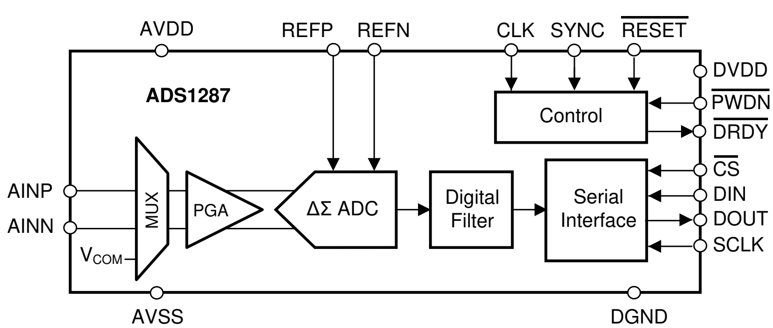
FIRデジタル・フィルタは、毎秒1000サンプル(SPS)までのデータ・レートに対応できます。ハイパス・フィルタ(HPF)により、DCおよび低周波数の成分は変換結果から除去されます。オンチップのゲインおよびオフセットのスケーリング・レジスタが、システム較正をサポートします。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS1287	VQFN (24)	5.00mm×4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

機能ブロック図



English Data Sheet: SBAS778

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (November 2017) から Revision B に変更 — **Page**

- Web にフルバージョンをリリースするためにドキュメントを 変更 1

2017年6月発行のものから更新 — **Page**

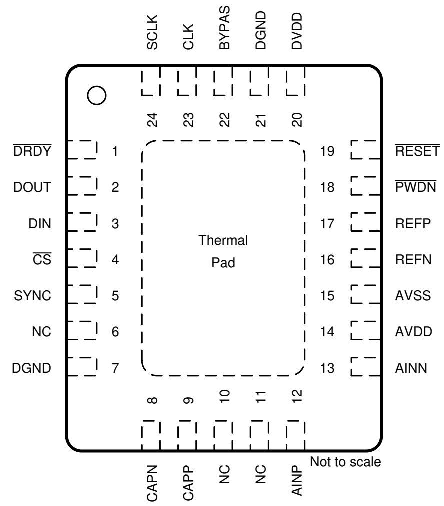
- Added second row to $t_{c(SC)}$ parameter 9
- Changed $t_{w(SCH)}$ and $t_{w(SCL)}$ parameters to be merged together, added second row to $t_{w(SCH)}$, $t_{w(SCL)}$ parameter 9
- Changed $t_{d(CLSY)}$ unit from 1 / f_{CLK} to ns 9
- Added unit to $t_{p(RSDR)}$ and $t_{p(PWDR)}$ parameters of *Switching Characteristics* table 10
- 変更 sinc filter block of *Digital Filter and Output Code Processing* figure from *Decimate by 8 to 128* to *Decimate by 4 to 128* to include low-power mode setting 26
- 追加 f_{MOD} = f_{CLK} / 8 for low-power mode to first paragraph of *Sinc Filter Stage* section 27
- 追加 sinc decimation ratio for low-power mode column and added high-resolution mode column header to *Sinc Filter Data Rates* table 27
- 変更 f_{MOD} description in Equation 9 27
- 追加 sinc decimation ratio for low-power mode column and added high-resolution mode column header to *FIR Filter Data Rates* table 28

5 概要（続き）

アンプ、変調器、デジタル・フィルタの合計消費電力は、高分解能モードで4.5mW (低消費電力モードで2.4mW)です。このADCは、小型の5mm×4mmのVQFNパッケージに格納されています。このADCは、-40℃～+85℃の温度範囲について完全に動作が規定されています。

6 Pin Configuration and Functions

RHF Package
5-mm × 4-mm, 24-Pin VQFN
Top View



Pin Functions

PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	$\overline{\text{DRDY}}$	Digital output	Data ready, active low
2	DOUT	Digital output	Serial data output
3	DIN	Digital input	Serial data input
4	$\overline{\text{CS}}$	Digital input	Serial interface select, active low
5	SYNC	Digital input	Synchronize, active high
6	NC	—	No connection
7	DGND	Ground	Digital ground
8	CAPN	Analog output	PGA negative output; connect a 10-nF C0G capacitor from CAPP to CAPN
9	CAPP	Analog output	PGA positive output; connect a 10-nF C0G capacitor from CAPP to CAPN
10	NC	—	No connection
11	NC	—	No connection
12	AINP	Analog input	Positive analog input
13	AINN	Analog input	Negative analog input
14	AVDD	Analog	Positive analog power supply
15	AVSS	Analog	Negative analog power supply
16	REFN	Analog input	Negative reference input
17	REFP	Analog input	Positive reference input
18	$\overline{\text{PWDN}}$	Digital input	Power-down, active low
19	$\overline{\text{RESET}}$	Digital input	Reset, active low
20	DVDD	Digital	Digital power supply
21	DGND	Ground	Digital ground (tie to digital ground plane)
22	BYPAS	Analog output	Sub-regulator bypass; connect a 1-µF capacitor to DGND
23	CLK	Digital input	Master clock input (1.024 MHz)
24	SCLK	Digital input	Serial interface clock input
Thermal pad		—	Electrically float the thermal pad. The thermal pad must be soldered to the PCB for optimum mechanical strength. PCB layout vias are optional.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AVSS	–0.3	6	V
	AVSS to DGND	–2.8	0.3	
	DVDD to DGND	–0.3	3.9	
Analog input voltage	AINx, REFx, CAPx	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK, DIN, DOUT, $\overline{DRDY}$, SYNC, $\overline{RESET}$, CLK, $\overline{PWDN}$, BYPAS	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous		10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVSS to DGND	–2.6		0	V
		AVDD to AVSS	4.75		5.25	
	Digital power supply	DVDD to DGND	2.25		3.6	V
PGA INPUT AND OUTPUT						
V_{IN}	Differential input voltage	$V_{IN} = V_{(AINP)} – V_{(AINN)}$	$–V_{REF}$ / Gain		V_{REF} / Gain	V
$V_{(AINx)}$	Absolute input voltage(1)		AVSS + 1		AVDD – 1.25	V
$V_{(CAPx)}$	Absolute output voltage		AVSS + 0.4		AVDD – 0.4	V
VOLTAGE REFERENCE INPUT						
V_{REF}	Differential reference input voltage	$V_{REF} = V_{(REFP)} – V_{(REFN)}$	2.45	2.5	2.55	V
$V_{(REFN)}$	Negative reference input voltage		AVSS – 0.1		$V_{(REFP)}$ – 2.45	V
$V_{(REFP)}$	Positive reference input voltage		$V_{(REFN)}$ + 2.45		AVDD + 0.1	V
CLOCK INPUT						
$f_{(CLK)}$	External clock frequency		0.4	1.024	1.05	MHz
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
	Operating ambient temperature		–45		125	°C

(1) Absolute input voltage is the signal voltage plus the common-mode voltage; see the *Programmable Gain Amplifier (PGA)* section.

7.4 Thermal Information

THERMAL METRIC(1)		ADS1287	UNIT
		RHF (VQFN)	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

maximum and minimum specifications apply from –40°C to +85°C; typical specifications are at 25°C; all specifications are at AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, $f_{(CLK)}$ = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, and f_{DATA} = 1000 SPS (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Input current	Chop disabled		10		pA
		Chop enabled		50		
	Input resistance	Common-mode, chop disabled		50		GΩ
		Differential-mode, chop disabled		100		
		Differential-mode, chop enabled		20		
	Input capacitance	Common-mode		20		pF
		Differential-mode		5		
PGA						
	Voltage noise density	High-resolution mode		15		nV/√Hz
		Low-power mode		25		
	1/f noise corner	Chop disabled		25		Hz
	Gain factors			1, 2, 4, 8, 16		V/V
	Differential output impedance	Nominal		1.7		kΩ
		Tolerance	–15%		15%	
	PGA output capacitor			10		nF
ADC						
	Resolution	FIR filter mode	31			Bits
	Voltage noise density	High-resolution mode		190		nV/√Hz
		Low-power mode		275		
f_{DATA}	Data rate	FIR filter mode		62.5, 125, 250, 500, 1000		SPS
SYSTEM PERFORMANCE						
SNR	Signal-to-noise ratio (see 表 1 through 表 4)	High-resolution mode, gain = 1	110	113		dB
		High-resolution mode, gain = 2	110	113		
		High-resolution mode, gain = 4	108	113		
		High-resolution mode, gain = 8	107	112		
		High-resolution mode, gain = 16	105	110		
		Low-power mode, gain = 1	106	110		
THD	Total harmonic distortion (1)	Gain = 1		–115	–105	dB
		Gain = 2, 4, 8, and 16		–115		
SFDR	Spurious-free dynamic range			115		dB
V_{IO}	Input offset voltage	T_A = 25°C	–300	±50	300	µV
		Chop disabled, T_A = 25°C		±300		
		After calibration (2)		±1		
	Input offset voltage drift			0.05		µV/°C
		Chop disabled		1		
	Gain error	High-resolution mode, T_A = 25°C	–0.8%	–0.3%	0.2%	
		Low-power mode, T_A = 25°C	–0.6%	–0.1%	0.4%	
	Gain error after calibration (2)			0.0005%		
	Gain drift	All gains		1		ppm/°C
	Gain match	All gains relative to gain = 1	–0.5%	±0.1%	0.5%	
	Calibration margin (3)		–106%		106%	

(1) Test signal: 31.25 Hz, –0.5 dBFS.
(2) Calibration accuracy is on the level of noise reduced by four (calibration averages 16 readings).
(3) Calibration margin is the maximum allowed input voltage range after calibration operations.

Electrical Characteristics (continued)

maximum and minimum specifications apply from –40°C to +85°C; typical specifications are at 25°C; all specifications are at AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, $f_{(CLK)}$ = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, and f_{DATA} = 1000 SPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE, continued						
CMRR	Common-mode rejection ratio	High-resolution mode, DC to 60 Hz	100	115		dB
		Low-resolution mode, DC to 60 Hz	95	110		
PSRR	Power-supply rejection ratio	Analog supplies, DC to 60 Hz	75	90		dB
		Digital supply, DC to 60 Hz	90	105		
VOLTAGE REFERENCE INPUT						
	Input impedance	High-resolution mode		320		kΩ
		Low-power mode		640		
DIGITAL FILTER RESPONSE						
	Pass-band ripple				±0.003	dB
	Pass band (–0.01 dB)			$0.375 \times f_{(DATA)}$		Hz
	Bandwidth (–3 dB)			$0.413 \times f_{(DATA)}$		Hz
	High-pass filter corner		0.1		10	Hz
	Stop-band attenuation (4)		135			dB
	Stop band			$0.500 \times f_{DATA}$		Hz
	Group delay	Minimum phase filter		$5 / f_{DATA}$		s
		Linear phase filter		$31 / f_{DATA}$		
	Settling time (latency)	Minimum phase filter		$62 / f_{DATA}$		s
		Linear phase filter		$62 / f_{DATA}$		
DIGITAL INPUT/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.2 × DVDD	V
V_{IH}	Logic input level, high		0.8 × DVDD		DVDD	V
V_{OL}	Logic output level, low	I_{OL} = 1 mA	DGND		0.2 × DVDD	V
V_{OH}	Logic output level, high	I_{OH} = 1 mA	0.8 × DVDD		DVDD	V
	Input current	$0 \le V_{DIGITAL\ IN} \le$ DVDD	–10		10	µA
POWER SUPPLY						
I_{AVDD}, I_{AVSS}	Analog supply current	High-resolution mode		750	1100	µA
		Low-power mode		330	480	
		Standby mode		1		
		Power-down mode		1		
I_{DVDD}	Digital supply current	High-resolution mode		240	320	µA
		Low-power mode		220	300	
		Standby mode (5)		25		
		Power-down mode (5)		1		
P_D	Power dissipation	High-resolution mode		4.5	6.6	mW
		Low-power mode		2.4	3.4	
		Standby mode (5)		90		µW
		Power-down mode (5)		10		

(4) Input frequencies are in the range of N × $f_{(CLK)}$ / 1024 ± $f_{(DATA)}$ / 2 (where *N* = 1, 2, 3, and so forth) intermodulated with the modulator chopper clock. At these frequencies, intermodulation components are –120 dBFS (typ).
(5) CLK input stopped.

7.6 Timing Requirements

over operating ambient temperature range and DVDD = 2.25 V to 3.6 V (unless otherwise noted)

		MIN	MAX	UNIT
SERIAL INTERFACE				
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge	40		ns
$t_{c(SC)}$	SCLK period	250		ns
	SCLK period specific to SYNC and RESET commands	2		1 / f_{CLK}
$t_{w(SCH)}$, $t_{w(SCL)}$	Pulse duration, SCLK high and low(1)	100		ns
	Pulse duration, SCLK high and low specific to SYNC and RESET commands	0.8		1 / f_{CLK}
$t_{su(DI)}$	Setup time, DIN valid before SCLK rising edge	50		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK rising edge	50		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	100		ns
$t_{d(SCCS)}$	Delay time, last SCLK rising edge to $\overline{CS}$ rising edge	24		1 / f_{CLK}
$t_{d(CMBT)}$	Delay time, after each byte within and between command sequences(2)	24		1 / f_{CLK}
SYNCHRONIZATION				
$t_{d(CLSY)}$	Delay time, CLK rising edge to SYNC rising edge(3)	30	–30	ns
$t_{w(SYH)}$, $t_{w(SYL)}$	Pulse duration, SYNC high or SYNC low	2		1 / f_{CLK}
RESET				
$t_{su(RSCL)}$	Setup time, $\overline{RESET}$ rising edge to a specific CLK rising edge	10		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	2		1 / f_{CLK}

(1) Holding SCLK low for 64 $\overline{DRDY}$ periods forces a serial interface reset.
(2) When reading conversion data, the byte-to-byte delay is not required ($t_{d(CMBT)}$).
(3) SYNC rising edge to CLK rising edge must not occur within the specified time window.

7.7 Switching Characteristics

over operating ambient temperature range, DVDD = 2.25 V to 3.6 V, and DOUT loading = 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE						
$t_{p(DRDO)}$	Propagation delay time, $\overline{DRDY}$ falling edge to valid data DOUT				100	ns
$t_{p(CSDOD)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven				60	ns
$t_{p(SCDO1)}$	Propagation delay time, SCLK falling edge to valid new DOUT				100	ns
$t_{p(SCDO2)}$	Propagation delay time, SCLK falling edge to valid old DOUT		0			ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT Hi-z				40	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high			4		1 / f_{CLK}
$t_{p(CMDR)}$	Propagation delay time, RDATA command to DRDY low (see 図 60)		0		1	1 / f_{DATA}

Switching Characteristics (continued)

over operating ambient temperature range, DVDD = 2.25 V to 3.6 V, and DOUT loading = 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONIZATION						
$t_{p(SYDR)}$	Propagation delay time, SYNC rising edge to DRDY falling edge	High-resolution mode, 62.5 SPS		1008.145		ms[(1)]
		High-resolution mode, 125 SPS		504.301		
		High-resolution mode, 250 SPS		252.379		
		High-resolution mode, 500 SPS		126.419		
		High-resolution mode, 1000 SPS		63.438		
		Low-power mode, 62.5 SPS		1008.390		
		Low-power mode, 125 SPS		504.548		
		Low-power mode, 250 SPS		252.625		
		Low-power mode, 500 SPS		126.665		
		Low-power mode, 1000 SPS		63.684		
		Sinc filter and high-resolution mode, 2000 SPS		2.755		
		Sinc filter and high-resolution mode, 4000 SPS		1.630		
		Sinc filter and high-resolution mode, 8000 SPS		0.942		
		Sinc filter and high-resolution mode, 16000 SPS		0.599		
		Sinc filter and high-resolution mode, 32000 SPS		0.427		
RESET						
$t_{p(RSDR)}$	Propagation delay time, $\overline{RESET}$ pin or reset command to $\overline{DRDY}$ falling edge			252.379		ms
POWER-DOWN MODE and STANDBY MODE WAKEUP						
$t_{p(PWDR)}$	Propagation delay time, exit power-down or standby mode to first data ready			252.379[(2)]		ms
POWER-UP						
$t_{p(PUCM)}$	Propagation delay time, power-on threshold voltage to communication ready			2^{16}		f_{CLK}
$t_{p(PUDR)}$	Propagation delay time, power-on threshold voltage to first data ready			$2^{16} / f_{CLK} + 252.379$		ms[(1)]

(1) f_{CLK} = 1.024 MHz.
(2) The exit power-down mode default setting is 250 SPS with the FIR filter mode. Subtract two f_{CLK} cycles for a WAKEUP command. The WAKEUP command is timed from the rising CLK edge after the eighth rising SCLK edge.

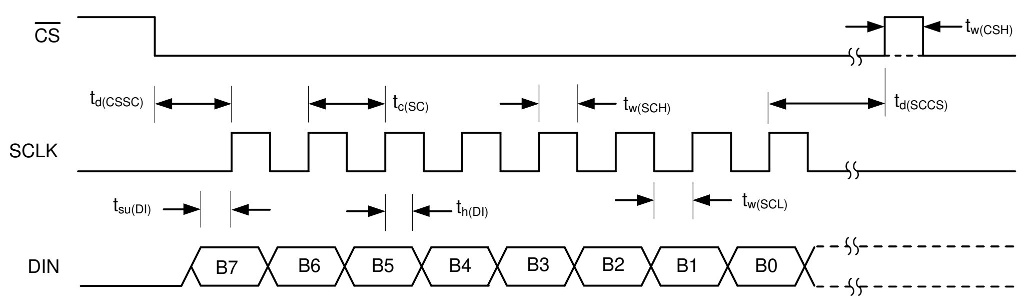


図 1. Serial Interface Timing Requirements

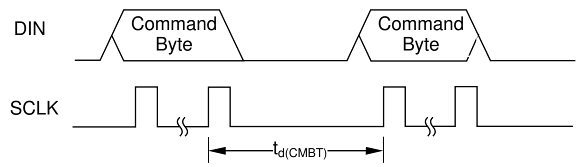


図 2. Serial Interface Command Timing Requirements

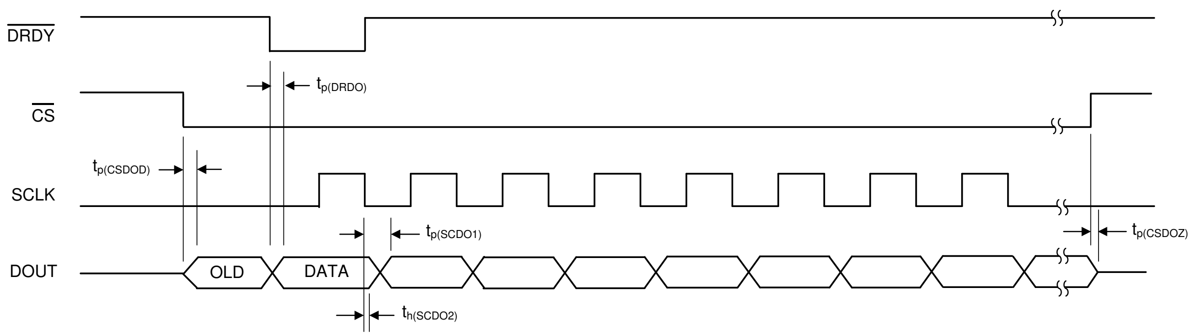


図 3. Serial Interface Switching Characteristics

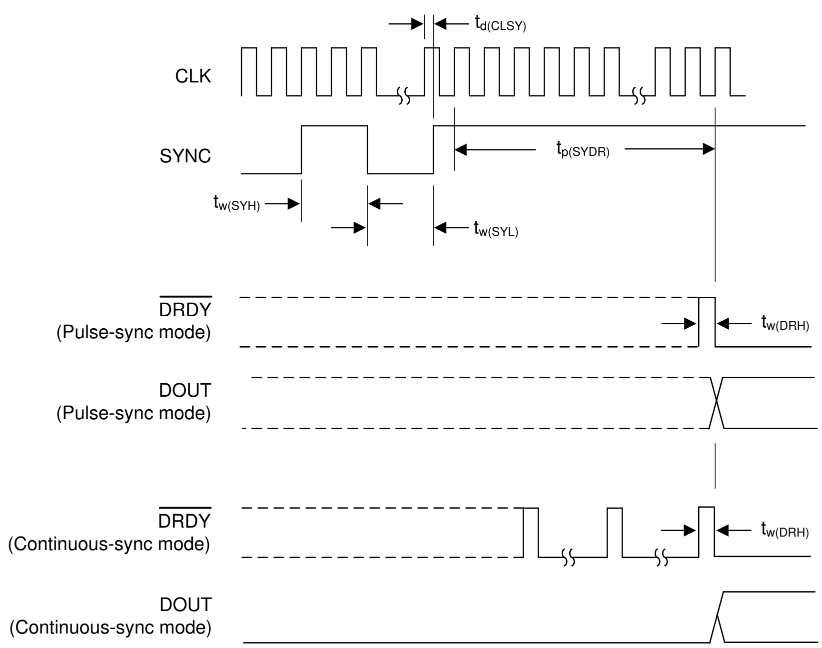


図 4. Synchronization Timing

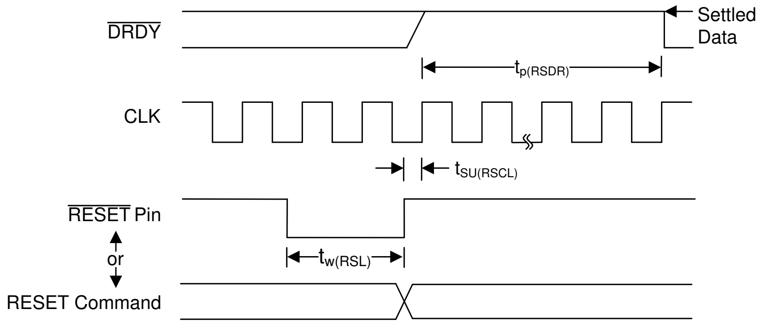


図 5. Reset Timing

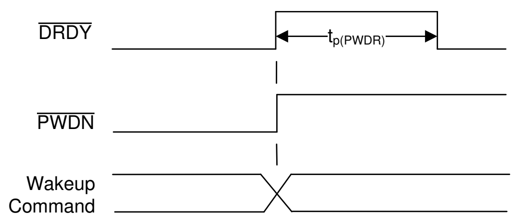


図 6. Power-Down and Standby Wake-Up Timing

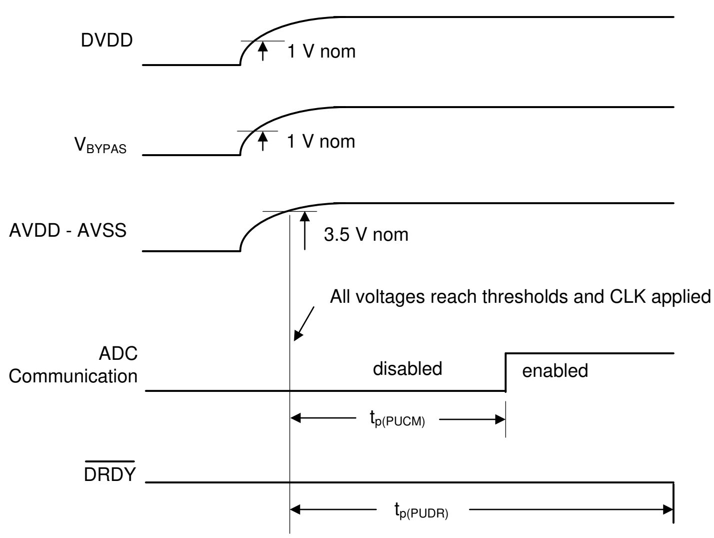
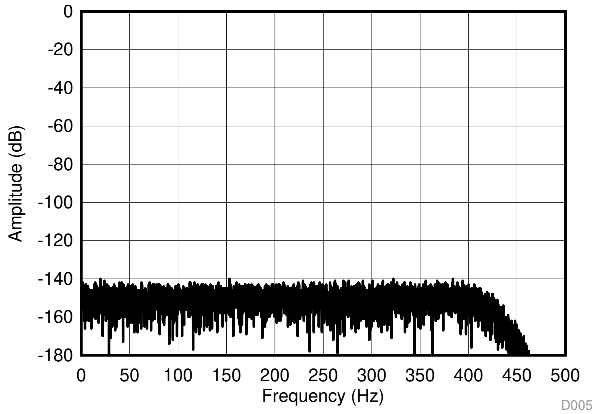


図 7. Power-Up Timing

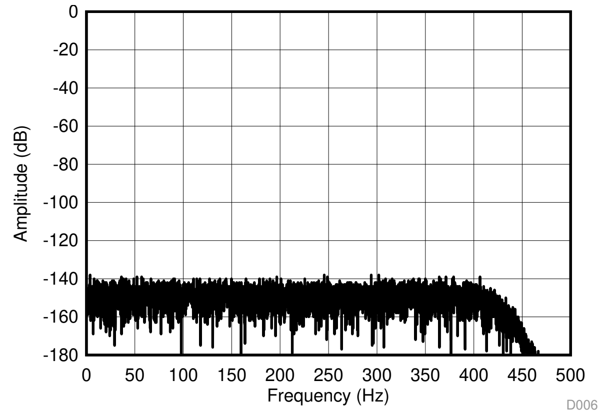
7.8 Typical Characteristics

at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, f_{CLK} = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, offset disabled, and f_{DATA} = 1000 SPS (unless otherwise noted)



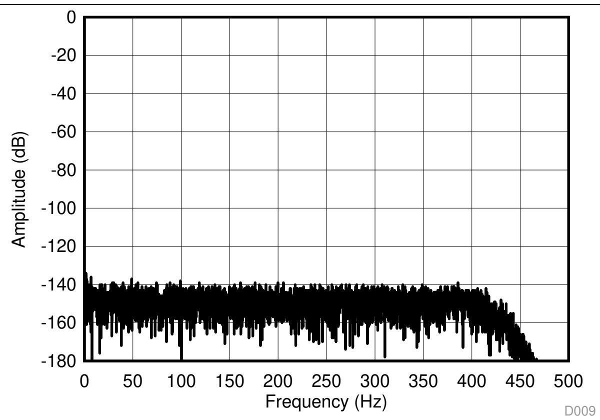
Shorted input, high-resolution mode,
gain = 1, 8192 points, SNR = 113.2 dB

図 8. Output Spectrum



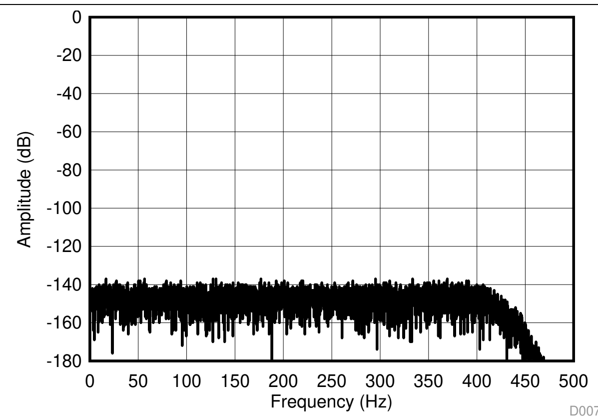
Shorted input, high-resolution mode,
gain = 8, 8192 points, SNR = 111.8 dB

図 9. Output Spectrum



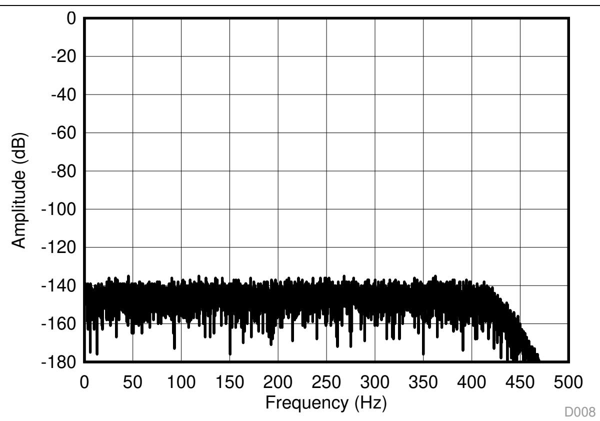
Shorted input, chop disabled, high-resolution mode,
gain = 8, 8192 points, SNR = 111.3 dB

図 10. Output Spectrum



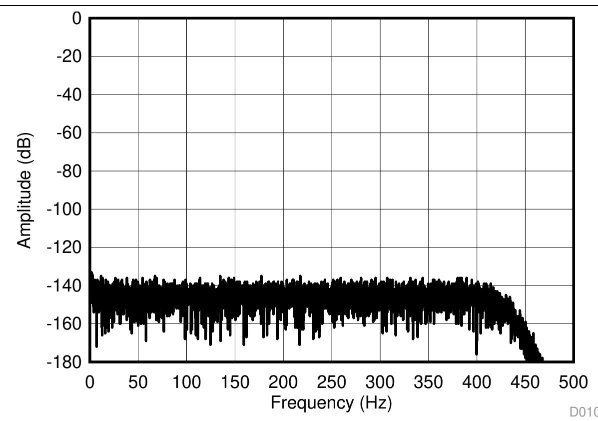
Shorted input, low-power mode, offset enabled,
gain = 1, 8192 points, SNR = 110.1 dB

図 11. Output Spectrum



Shorted input, low-power mode, offset enabled,
gain = 8, 8192 points, SNR = 108.4 dB

図 12. Output Spectrum

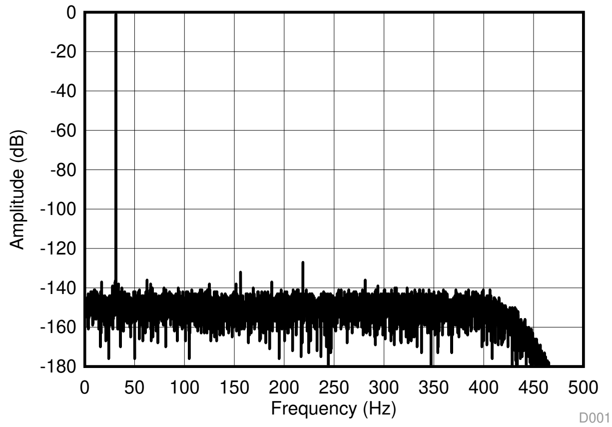


Shorted input, low-power mode, chop disabled,
gain = 8, 8192 points, SNR = 108.0 dB

図 13. Output Spectrum

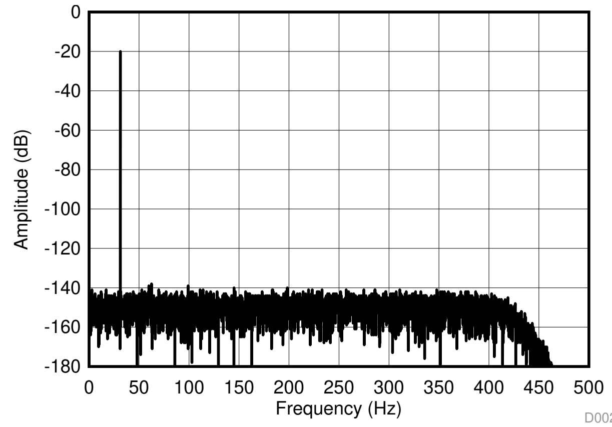
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, f_{CLK} = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, offset disabled, and f_{DATA} = 1000 SPS (unless otherwise noted)



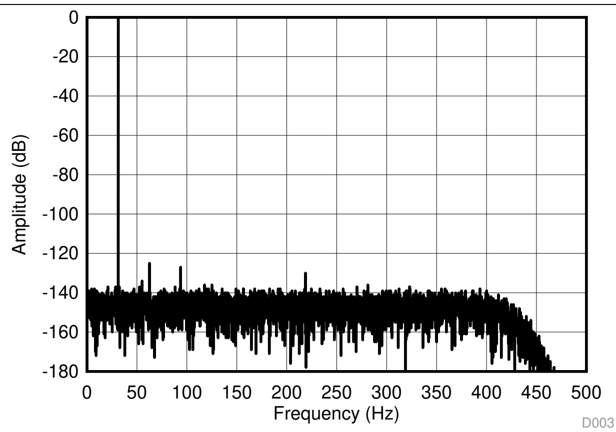
f_{IN} = 31.25 Hz, –0.5 dB, high-resolution mode, gain = 1, 8192 points

図 14. Output Spectrum



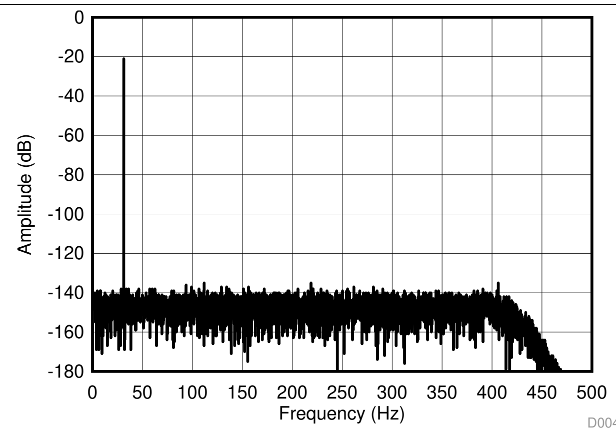
f_{IN} = 31.25 Hz, –20 dB, high-resolution mode, gain = 1, 8192 points

図 15. Output Spectrum



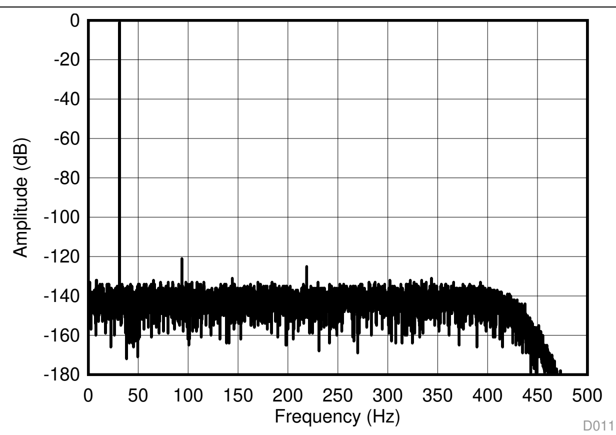
f_{IN} = 31.25 Hz, –0.5 dB, high-resolution mode, gain = 8, 8192 points

図 16. Output Spectrum



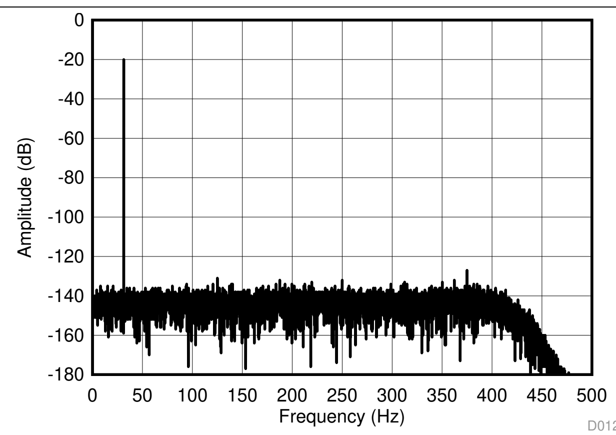
f_{IN} = 31.25 Hz, –20 dB, high-resolution mode, gain = 8, 8192 points

図 17. Output Spectrum



f_{IN} = 31.25 Hz, –0.5 dB, low-power mode, gain = 1, 8192 points

図 18. Output Spectrum

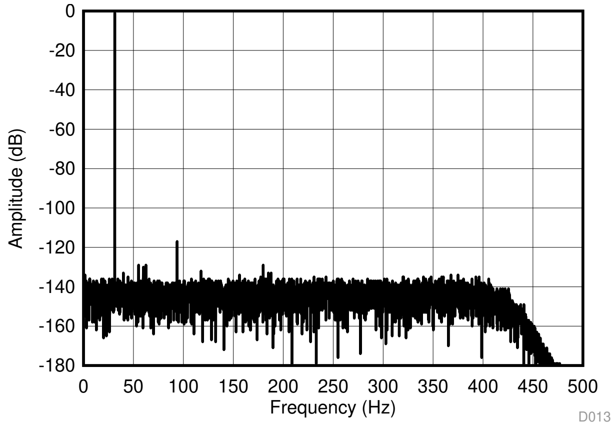


f_{IN} = 31.25 Hz, –20 dB, low-power mode, gain = 1, 8192 points

図 19. Output Spectrum

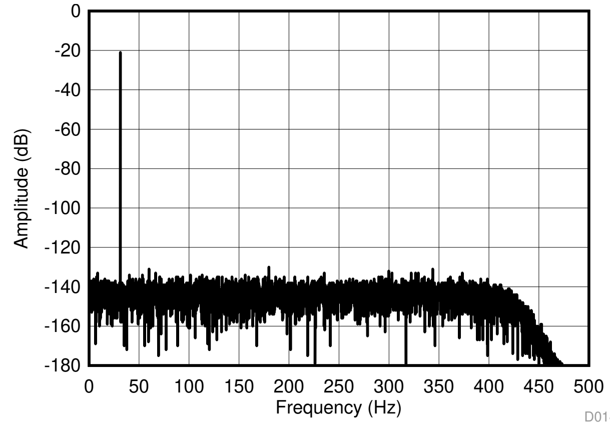
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, f_{CLK} = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, offset disabled, and f_{DATA} = 1000 SPS (unless otherwise noted)



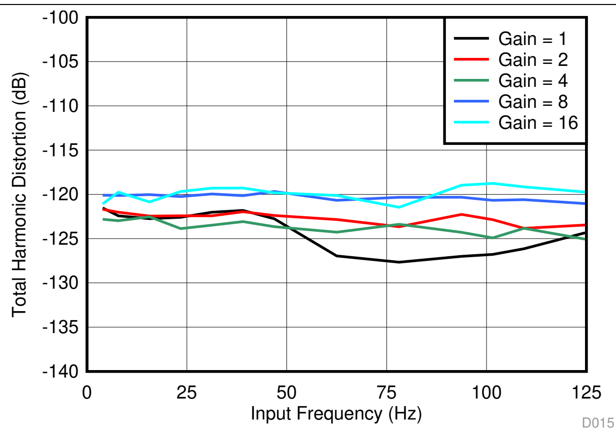
f_{IN} = 31.25 Hz, –0.5 dB, low-power mode, gain = 8, 8192 points

図 20. Output Spectrum



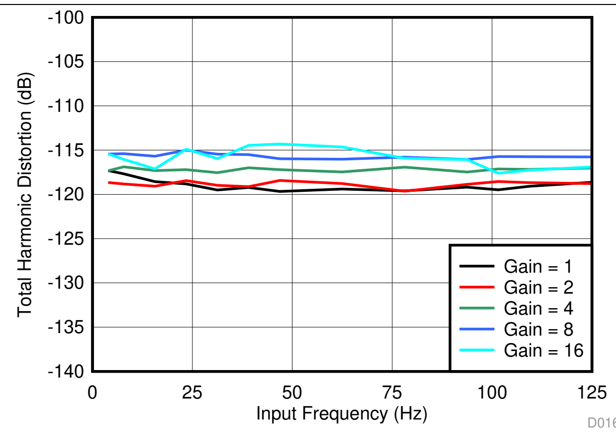
f_{IN} = 31.25 Hz, –20 dB, low-power mode, gain = 8, 8192 points

図 21. Output Spectrum



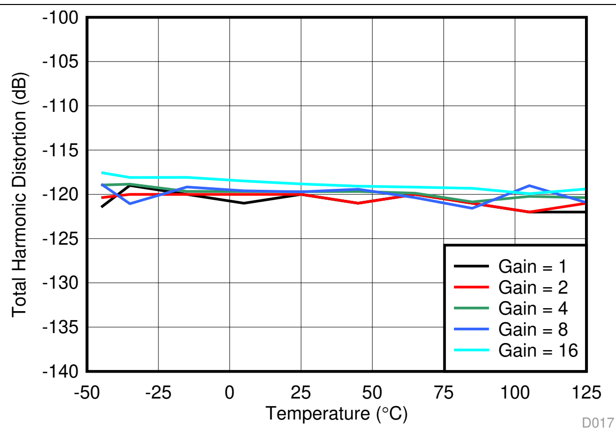
High-resolution mode, V_{IN} = –0.5 dB

図 22. THD vs Input Frequency



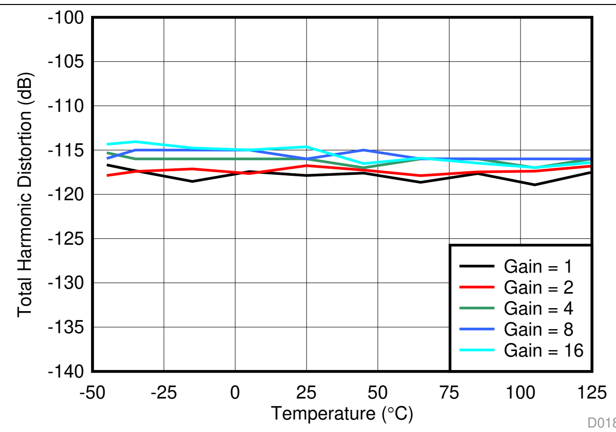
Low-power mode, V_{IN} = –0.5 dB

図 23. THD vs Input Frequency



f_{IN} = 31.25 Hz, –0.5 dB, high-resolution mode

図 24. THD vs Temperature

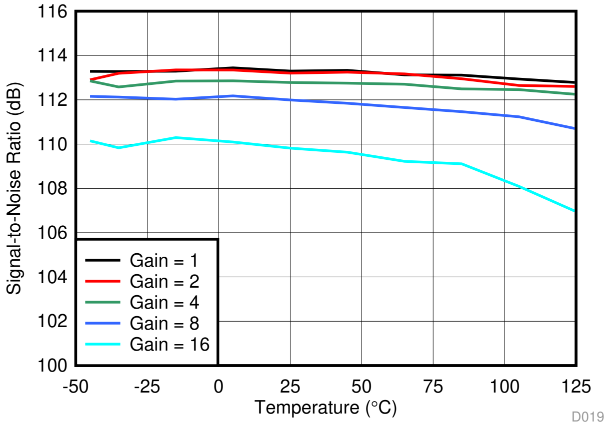


f_{IN} = 31.25 Hz, –0.5 dB, low-power mode

図 25. THD vs Temperature

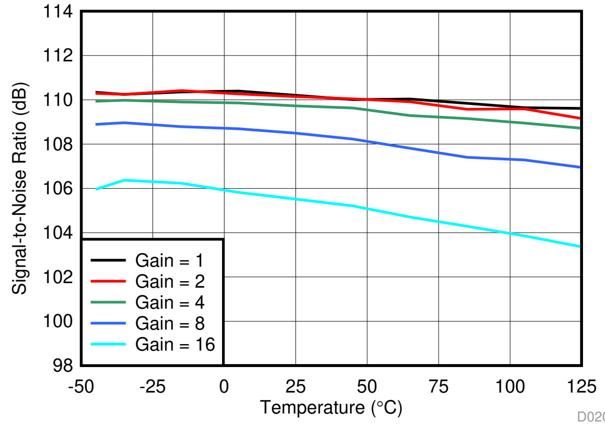
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, f_{CLK} = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, offset disabled, and f_{DATA} = 1000 SPS (unless otherwise noted)



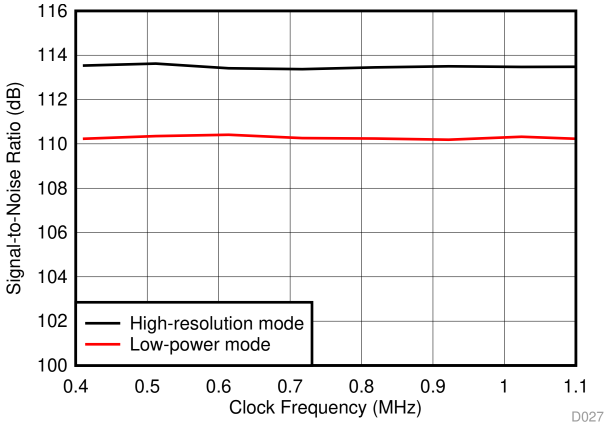
Shorted input, high-resolution mode

図 26. SNR vs Temperature



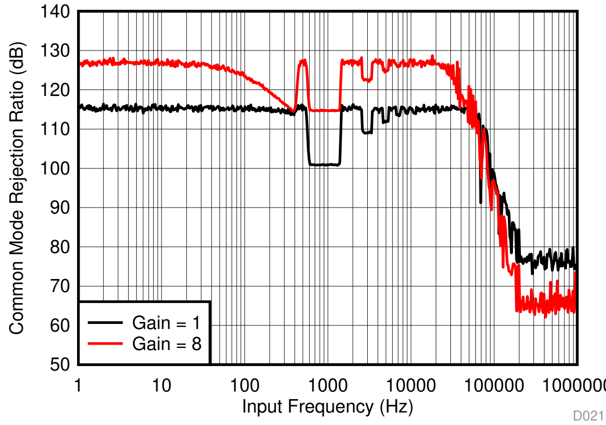
Shorted input, low-power mode

図 27. SNR vs Temperature



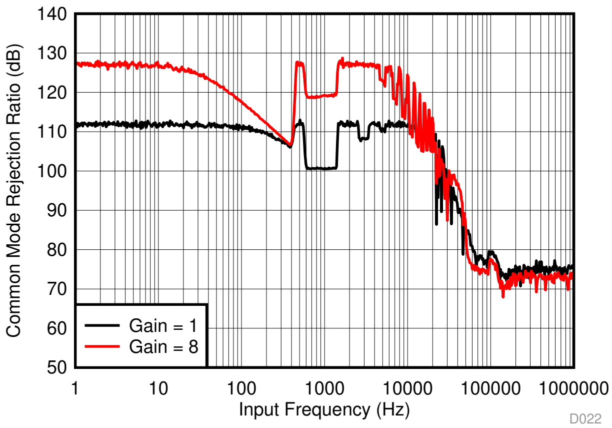
Shorted input

図 28. SNR vs Clock Frequency



High-resolution mode

図 29. CMRR vs Frequency



Low-power mode

図 30. CMRR vs Frequency

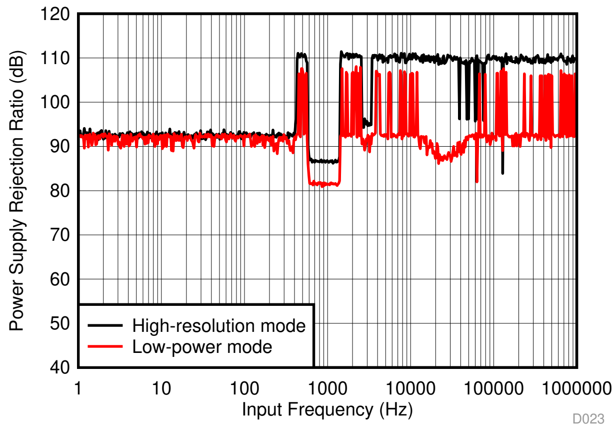
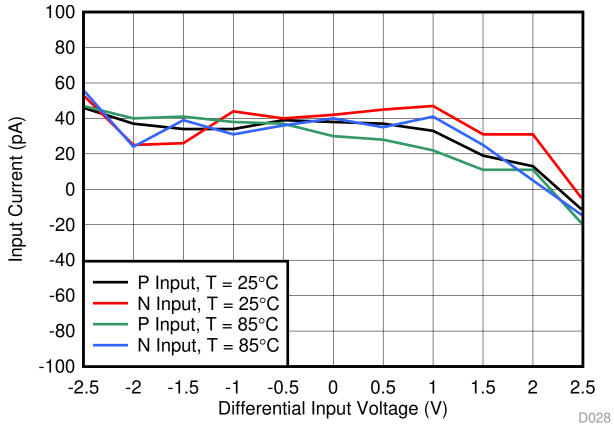


図 31. Analog Supply PSRR vs Frequency

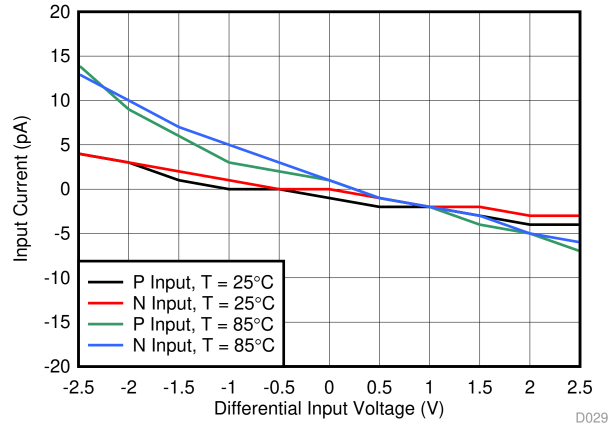
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, f_{CLK} = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, offset disabled, and f_{DATA} = 1000 SPS (unless otherwise noted)



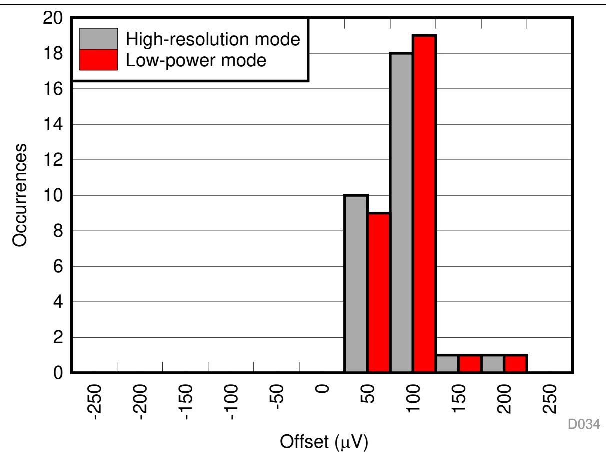
Chop enabled, gain = 1, high-resolution mode

図 32. Input Current vs Input Voltage



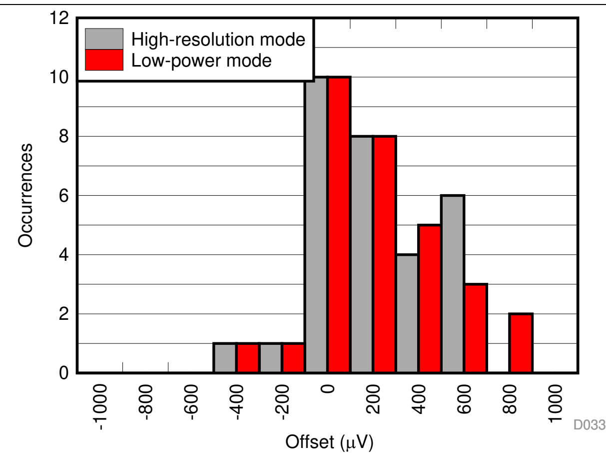
Chop disabled, gain = 1, high-resolution mode

図 33. Input Current vs Input Voltage



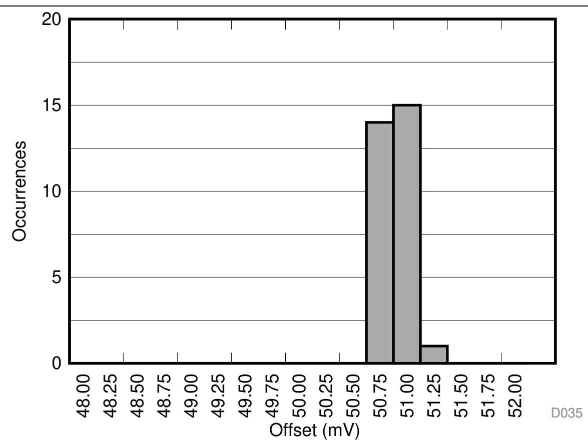
Chop enabled, gain = 1, 30 units

図 34. Offset Error Histogram



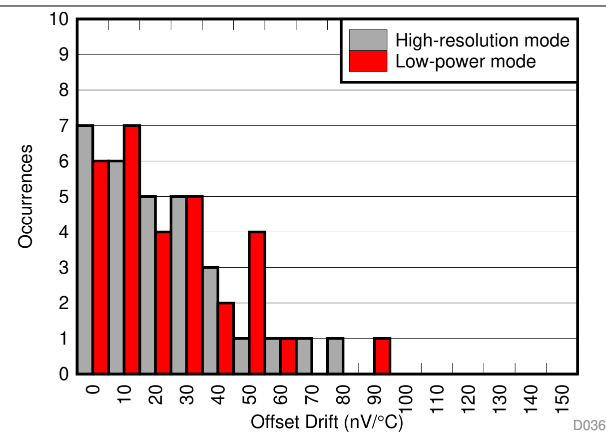
Chop disabled, gain = 1, 30 units

図 35. Offset Error Histogram



Offset enabled (50 mV), low-power mode,
gain = 1, 30 units

図 36. Offset Error Histogram

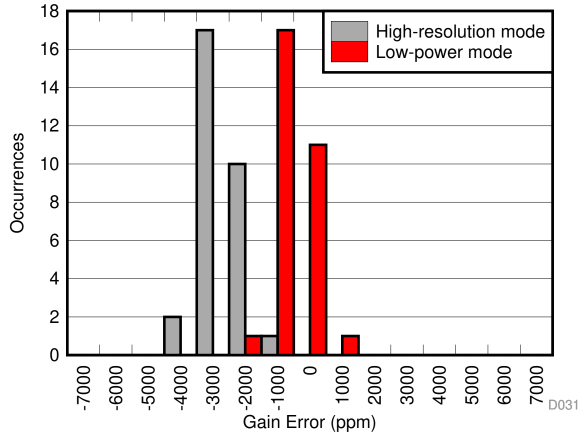


Chop enabled, gain = 1, 30 units

図 37. Offset Temperature Drift Histogram

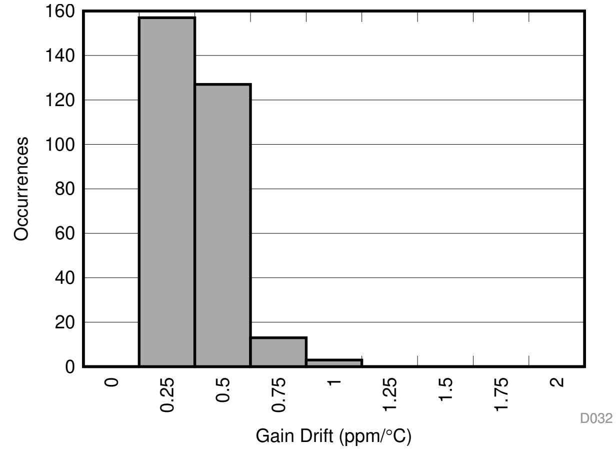
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, f_{CLK} = 1.024 MHz, $V_{(REFP)}$ = 0 V, $V_{(REFN)}$ = –2.5 V, gain = 1, high-resolution and low-power modes, chop enabled, offset disabled, and f_{DATA} = 1000 SPS (unless otherwise noted)



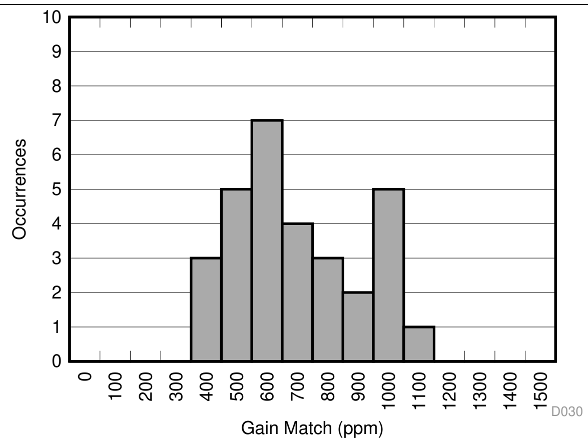
Gain = 1, 30 units

図 38. Gain Error Histogram



Gain = 1, 2, 4, 8 and 16 combined; 30 units; combined high-resolution and low-power modes

図 39. Gain Drift Histogram



Gain = 2, 4, 8, 16 match to gain = 1; 30 units

図 40. Gain Match Error Histogram

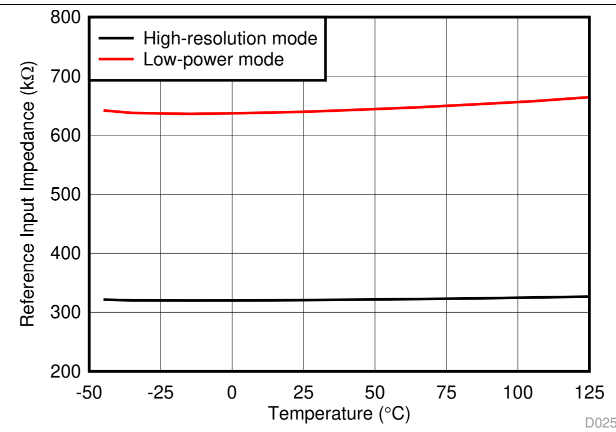


図 41. Reference Input Impedance vs Temperature

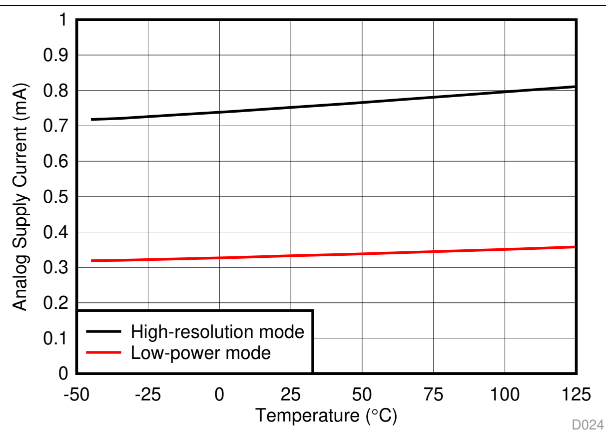
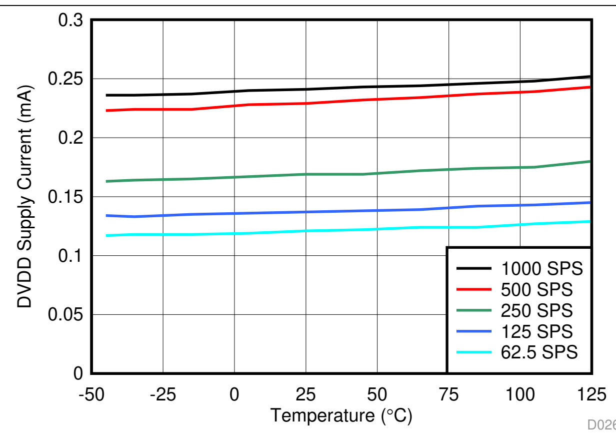


図 42. Analog Supply Current vs Temperature



High-resolution mode

図 43. Digital Supply Current vs Temperature

8 Parameter Measurement Information

8.1 Noise Performance

SNR and input-referred noise are related parameters that define the ADC effective resolution. Use 式 1 to calculate SNR from the input-referred noise data:

$$\mathrm{SNR} = 20\log \frac{\mathrm{FSR_{RMS}}}{\mathrm{N_{RMS}}}$$

where:

FSR_{RMS} = Full-scale range, root-mean-square = 2.5 V / ($\sqrt{2}$ · Gain)

N_{RMS} = Input-referred noise voltage (1)

表 1 through 表 4 list SNR and noise performance data. Noise performance data are listed for high-resolution and low-power modes, with and without chop enabled. The noise performance data are representative of typical ADC performance at T_A = 25°C. The data are the standard deviation of consecutive ADC conversion results with the ADC inputs shorted over the signal bandwidth of 0.1 Hz to 0.413 f_{DATA}. Repeated noise measurements can yield higher or lower noise results because of the statistical nature of noise.

Noise performance depends on several ADC operating parameters: high-resolution or low-power mode, data rate, PGA gain, and chop mode. Best noise performance is achieved by operating the ADC in high-resolution mode. Noise performance also depends on the data rate. For example, as the data rate decreases, the ADC bandwidth and thus total noise decreases. Using higher gain factors improves input-referred noise, but the calculated SNR decreases because of a 6-dB decrease of input range for each gain step. Chop mode improves noise performance by removing 1/f noise from the PGA. Chop mode is particularly important for lowest noise operation when used with low data rates or high gain. Chop mode is the recommended mode for geophone sensors.

表 1. High-Resolution Mode Noise Performance (Chop Enabled)(1)

f_{DATA} (SPS)	SNR (dB)					INPUT-REFERRED NOISE (μV_{RMS})				
	GAIN					GAIN				
	1	2	4	8	16	1	2	4	8	16
62.5	125	125	125	124	122	0.96	0.49	0.25	0.14	0.09
125	122	122	122	121	119	1.36	0.68	0.35	0.19	0.13
250	119	119	119	118	116	1.90	0.97	0.50	0.28	0.18
500	116	116	116	115	113	2.70	1.36	0.71	0.39	0.25
1000	113	113	113	112	110	3.85	1.95	1.00	0.55	0.36

(1) Typical performance data at T_A = 25°C. SNR data are rounded. Measurement bandwidth: 0.1 Hz to 0.413 f_{DATA}.

表 2. High-Resolution Mode Noise Performance (Chop Disabled)(1)

f_{DATA} (SPS)	SNR (dB)					INPUT-REFERRED NOISE (μV_{RMS})				
	GAIN					GAIN				
	1	2	4	8	16	1	2	4	8	16
62.5	125	125	123	120	114	0.99	0.52	0.31	0.23	0.23
125	122	122	121	119	114	1.36	0.70	0.39	0.26	0.22
250	119	119	118	116	113	1.90	0.97	0.54	0.34	0.26
500	116	116	116	114	111	2.70	1.38	0.73	0.43	0.32
1000	113	113	113	111	109	3.85	1.95	1.03	0.60	0.41

(1) Typical performance data at T_A = 25°C. SNR data are rounded. Measurement bandwidth: 0.1 Hz to 0.413 f_{DATA}.

表 3. Low-Power Mode Noise Performance (Chop Enabled, Offset Enabled)(1)

f_{DATA} (SPS)	SNR (dB)					INPUT-REFERRED NOISE (μV_{RMS})				
	GAIN					GAIN				
	1	2	4	8	16	1	2	4	8	16
62.5	123	123	122	121	118	1.33	0.66	0.36	0.20	0.14
125	120	119	119	118	115	1.86	0.96	0.50	0.29	0.20
250	117	116	116	115	112	2.65	1.36	0.70	0.41	0.29
500	113	113	113	112	109	3.81	1.91	1.01	0.58	0.40
1000	110	110	110	109	106	5.50	2.79	1.48	0.84	0.58

(1) Typical performance data at T_A = 25°C. SNR data are rounded. Measurement bandwidth: 0.1 Hz to 0.413 f_{DATA}.

表 4. Low-Power Mode Noise Performance (Chop Disabled, Offset Enabled) (1)

f_{DATA} (SPS)	SNR (dB)					INPUT-REFERRED NOISE (μV_{RMS})				
	GAIN					GAIN				
	1	2	4	8	16	1	2	4	8	16
62.5	122	122	121	118	113	1.36	0.71	0.40	0.29	0.24
125	119	119	118	116	112	1.90	0.97	0.53	0.36	0.29
250	116	116	115	114	110	2.67	1.38	0.74	0.46	0.35
500	113	113	113	111	108	3.75	1.93	1.02	0.62	0.46
1000	110	110	110	108	105	5.53	2.80	1.48	0.88	0.62

(1) Typical performance data at T_A = 25°C. SNR data are rounded. Measurement bandwidth: 0.1 Hz to 0.413 f_{DATA}.

9 Detailed Description

9.1 Overview

The ADS1287 is a low-power, high-resolution analog-to-digital converter (ADC) intended for energy exploration, low-power seismic-data acquisition nodes, and other exacting applications that require very low power consumption. The converter provides 31-bit resolution over data rates 62.5 SPS to 1000 SPS, and programmable gains of 1 to 16 that expand the measurement resolution; see the *Functional Block Diagram* section.

The ADC consists of an input multiplexer (MUX), a low-noise complementary metal oxide semiconductor (CMOS) programmable gain amplifier (PGA), a fourth order delta-sigma (ΔΣ) modulator, an infinite impulse response (IIR) high-pass filter (HPF), a finite-impulse-response (FIR) low-pass filter (LPF), and an SPI-compatible serial interface used for both device configuration and conversion data readback.

The signal multiplexer selects between the external input or internal short (via 400-Ω resistors). The internal short is used for offset calibration and to verify the ADC offset and noise performance. The input multiplexer is followed by a programmable-gain, CMOS PGA, featuring low noise. The available PGA gains are 1 V/V, 2 V/V, 4 V/V, 8 V/V, and 16 V/V. The PGA is chopped to reduce 1/f noise and input offset voltage. The PGA output is routed to the modulator and to the CAPP and CAPN pins. An external 10-nF capacitor connected to these pins filters the modulator sampling pulses and provides the ADC antialias filter.

The inherently-stable, fourth-order, ΔΣ modulator measures the differential input signal $V_{IN} = V_{(AINP)} - V_{(AINN)}$ against the differential reference $V_{REF} = V_{(REFP)} - V_{(REFN)}$. The ADC requires an external 2.5-V voltage reference. The modulator output data are processed by an integrated digital filter to provide the final conversion result.

The digital filter consists of a sinc filter followed by a programmable-phase, FIR low-pass filter and programmable-frequency, IIR high-pass filter. The HPF removes DC and low-frequency components from the conversion result.

Programmable gain and offset data registers calibrate the conversion result to remove offset and gain errors.

The SYNC input pin synchronizes the ADC. Synchronization has two programable modes of operation: pulse-synchronization and continuous-synchronization that accepts a synchronizing-clock input. The $\overline{RESET}$ input resets the ADC including the register settings.

Overview (continued)

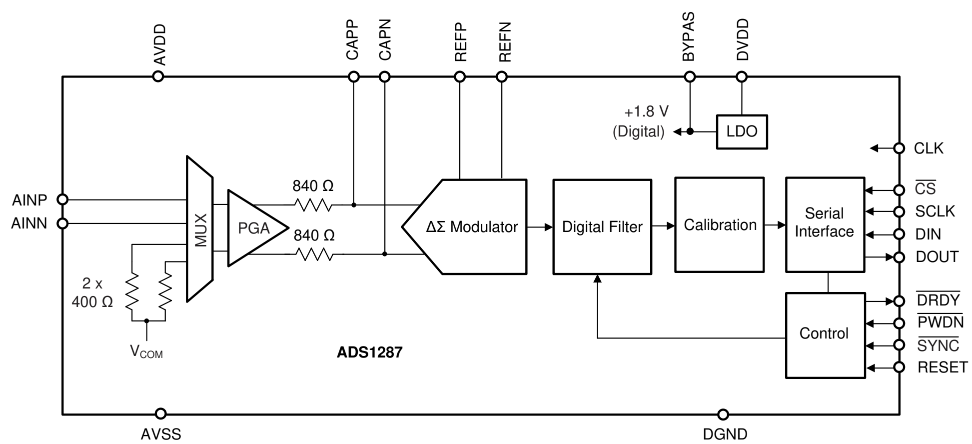
The PWDN input powers-down the ADC. The low-power STANDBY mode is engaged by software command.

RESET and SYNC control inputs are noise-resistant, Schmitt-trigger inputs to increase reliability in high-noise environments.

The ADC has an SPI-compatible serial interface. The interface is 4-wire and is used to read conversion data and to read and write device registers.

Power to the analog section is provided through AVDD and AVSS. DVDD is the digital and I/O supply. DVDD is sub-regulated to 1.8 V by an integrated, low-dropout regulator (LDO) to supply the digital core. The BYPAS pin is the LDO output and requires a 1-µF bypass capacitor.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Analog Input and Multiplexer

図 44 shows a diagram of the analog input circuit and multiplexer.

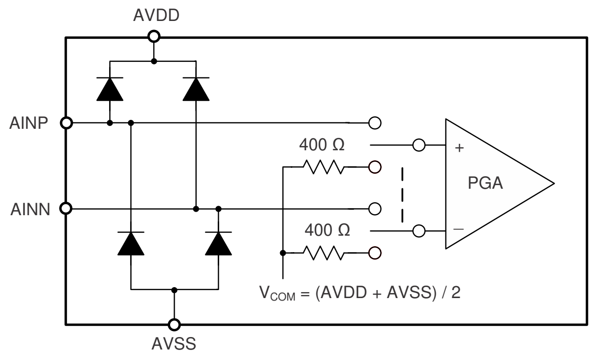


図 44. Analog Input and Multiplexer

Electrostatic discharge (ESD) diodes are incorporated to protect the ADC inputs from ESD exposure that can occur during device manufacturing and printed circuit board (PCB) assembly process when assembled in an ESD-controlled environment. For system-level ESD protection, external ESD protection devices are recommended to protect device inputs or outputs that may be exposed to ESD events.

If either input is taken below AVSS – 0.3 V, or above AVDD + 0.3 V, the internal protection diodes can conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the maximum input current to the specified value.

The input multiplexer selects between the external input or the internal (shorted) input. The internal short is via two 400-Ω resistors to analog mid-supply voltage (V_{COM}). The thermal noise of the resistors is equivalent to the noise produced by common geophones. Use the internal short connection to verify the ADC offset voltage and noise performance, and to provide an input to calibrate the ADC offset voltage. 表 5 summarizes the register selections of the multiplexer configurations related to 図 44.

表 5. Input Multiplexer Modes

MUX[1:0] REGISTER BITS	DESCRIPTION
00	External input (default)
01	Reserved
10	Internal short; PGA input connected to internal V_{COM} voltage via 400-Ω resistors
11	Reserved

9.3.2 Programmable Gain Amplifier (PGA)

The ADC incorporates a low-noise PGA in order to extend the ADC dynamic range. The PGA is a CMOS, differential-input and differential-output amplifier. The gain factor is programmable from 1 V/V to 16 V/V and is controlled by the GAIN[2:0] register bits. The PGA differentially drives the modulator via two 840-Ω internal resistors. Connect a 10-nF, C0G-dielectric capacitor between the CAPP and CAPN pins. The capacitor filters the modulator sampling glitches and also functions as a first-order antialias filter. 式 2 gives the corner frequency of the antialias filter:

$$f_C = 1/\ (2\pi \cdot 2 \cdot 1.7\ k\Omega \cdot 10\ nF) = 9.3\ kHz \quad (2)$$

As shown in 図 45, the PGA is composed of two amplifiers. The amplifiers are chopper-stabilized in order to reduce the PGA 1/f noise, offset, and offset drift. The PGA chop mode can be disabled when used with certain types of high-impedance sensors, such as hydrophones; see the *Chop Mode* section for more details.

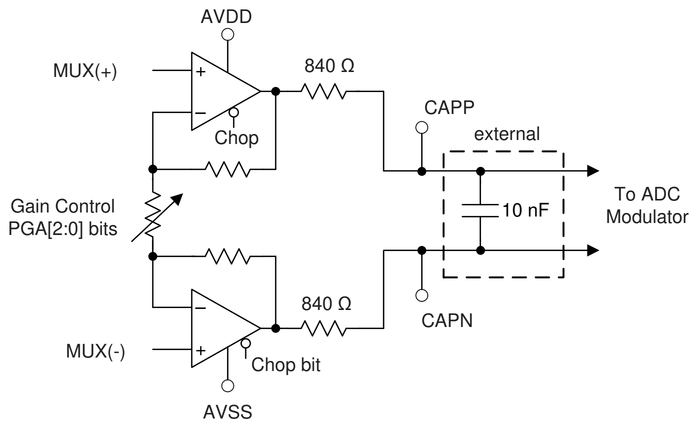


図 45. PGA Block Diagram

The PGA gain factors are programmable from 1 to 16 V/V. 表 6 shows the register bit setting for the PGA gain and corresponding input voltage range.

表 6. PGA Gain Factors

GAIN[2:0] REGISTER BITS	GAIN (V/V)	DIFFERENTIAL INPUT RANGE
000	1	±2.5 V
001	2	±1.25 V
010	4	±0.625 V
011	8	±0.3125 V
100	16	±0.15625 V
101 - 111	Reserved	—

To maintain linear operation, observe the specified PGA input and PGA output voltage range requirements. The absolute voltage is defined as the sum of the signal component plus offset voltage (common-mode voltage). 式 3 shows the specified absolute input voltage range:

$$AVSS + 1\ V < V_{(AINP)} \text{ and } V_{(AINN)} < AVDD - 1.25\ V \quad (3)$$

式 4 shows the specified absolute PGA output voltage range:

$$AVSS + 0.4\ V < V_{(CAPP)} \text{ and } V_{(CAPN)} < AVDD - 0.4\ V \quad (4)$$

式 5 shows that the PGA output voltage is equal to the absolute PGA input voltage plus and minus the differential input voltage times half the PGA gain factor minus 1:

$$\text{PGA output voltage} = V_{(CAPx)} = V_{(AINx)} \pm V_{IN} \cdot (Gain - 1) / 2 \quad (5)$$

9.3.3 Modulator

図 46 shows that the ΔΣ modulator is an inherently-stable, fourth-order, 2 + 2 pipelined structure. The modulator shapes the quantization noise to an area outside of the pass band, where the noise is removed by the digital filter.

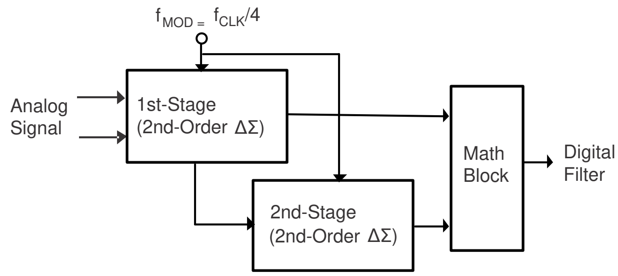


図 46. Modulator

The first stage of the modulator converts the analog input voltage into a pulse-code modulated (PCM) stream. When the input voltage to the modulator is equal to the reference voltage (V_{REF}), the density of the PCM data stream is at the highest 1 density. When the input voltage is zero, the PCM 1 density is 50%. At the FS and –FS inputs, the 1 density of the PCM streams is approximately 90% and 10%, respectively.

The modulator second stage produces a digital data stream designed to cancel the quantization noise of the first stage. The data streams of the two stages are mathematically combined to reduce overall quantization noise. The combined data are the input to the digital filter block.

9.3.3.1 Modulator Overrange

The ADS1287 modulator is inherently stable, and therefore, has predictable input overdrive recovery. If the input is overdriven to cause the modulator to produce a 1 density output in the range of 90% to 100% (10% and 0% for negative overdrive), the output codes may or may not clip resulting from the effect of the digital filter integration. Clipping depends on the duration of the input overdrive. When the input returns to the normal range from a long-duration overdrive (worst case), the modulator returns immediately to the normal 1 density range, but the action of the digital filter delays the return to the normal reading range because of the filter group delay.

In the extreme case of input overdrive (where the overdriven input exceeds the analog supply voltage + V_{ESD} diode drop), the internal ESD diodes begin to conduct, thus clipping the input signal. When the input overdrive is removed, the diodes recover quickly. Be sure to limit the input current to 10 mA (transient or continuous duty) if an overvoltage condition is possible.

9.3.4 Voltage Reference Inputs (REFP, REFN)

The ADC requires an external reference voltage for operation. The specified reference voltage is 2.5 V and is defined by 式 6 as the voltage between the REFP and REFN pins:

$$V_{REF} = V_{(REFP)} - V_{(REFN)} \quad (6)$$

図 47 shows the reference input circuit. The ADC samples the reference voltage to an internal capacitor. The sampled voltage is used in the ADC process. The constant sampling of the reference inputs results in transient currents that must be filtered by an external capacitor. Place a 0.1-µF ceramic capacitor directly between the REFP and REFN pins to filter the transient currents.

The input impedance of the reference input is determined by the average value of the transient currents. In applications where one voltage reference drives multiple ADCs, use individual capacitors at each ADC reference input. Reference voltage noise can degrade the overall noise performance. Therefore, the selection of the voltage reference must include the evaluation of noise.

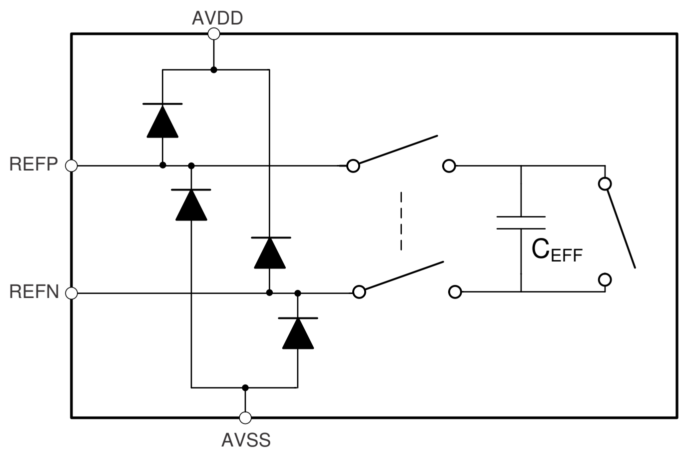


図 47. Simplified Reference Input Circuit

The ADC reference inputs are protected by internal ESD diodes. The voltage of reference inputs must stay within the range shown in 式 7 in order to prevent these diodes from conducting:

$$AVSS - 300\text{ mV} < V_{REFP} \text{ or } V_{REFN} < AVDD + 300\text{ mV} \quad (7)$$

If the voltage on the reference inputs exceeds this range, limit the reference input current to 10 mA or less. See the *Electrical Characteristics* section for the specified reference voltage range.

9.3.5 Digital Filter

The digital filter performs decimation and filtering of the modulator output to provide the final data output. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate. Lower data rates yield lower overall noise resulting from the reduction of bandwidth.

The digital filter is comprised of three filter stages, as shown in 図 48: a variable-decimation, sinc filter; a fixed-decimation FIR filter; and a programmable frequency high-pass, IIR filter (HPF).

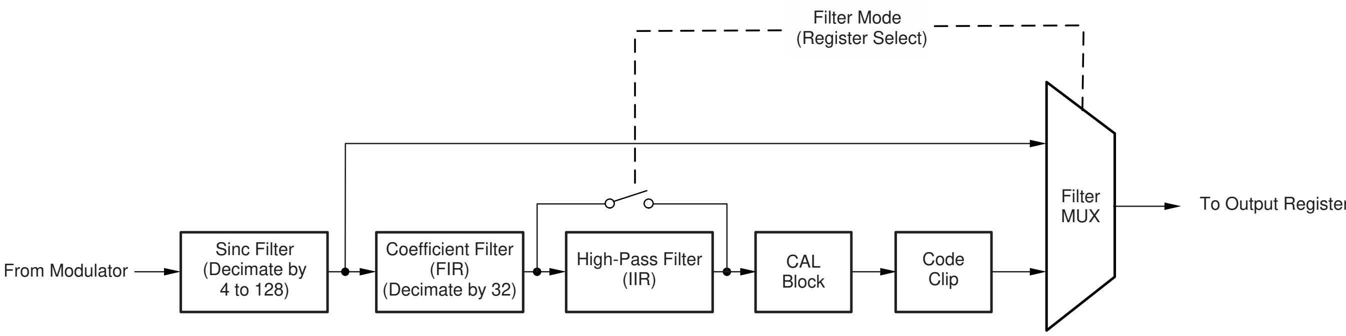


図 48. Digital Filter and Output Code Processing

The output data can be taken from one of the three filter blocks. The sinc filter option provides partially filtered data. The partially filtered sinc data are intended for use with external decimation filters. For complete internal filtering, activate both the sinc filter and FIR filter stages. The HPF can also be included to remove DC and low frequencies from the data. 表 7 shows the filter options.

表 7. Digital Filter Selection

FILTR[1:0] REGISTER BITS	DIGITAL FILTERS SELECTION
00	Reserved
01	Low-pass filter: sinc only
10	Low-pass filter: sinc + FIR (default)
11	Low-pass and high-pass filter: sinc + FIR + IIR

9.3.5.1 *Sinc Filter Stage*

The sinc filter (sinx/x) is a variable-decimation, fifth-order, low-pass filter. Data are supplied to this filter from the modulator at the rate of f_{MOD} = f_{CLK} / 4 (high-resolution mode), f_{CLK} / 8 (low-power mode). The sinc filter attenuates the high-frequency noise of the modulator. The sinc filter provides down-sampled, partially-filtered data to the FIR filter. The decimation ratio of the sinc filter is variable and determines the overall data rate. 表 8 shows that the decimation ratio of the sinc filter is programmed by the DR[2:0] register bits.

表 8. Sinc Filter Data Rates

DR[2:0] REGISTER BITS	SINC DECIMATION RATIO (N)		SINC DATA RATE (SPS)
	HIGH-RESOLUTION MODE	LOW-POWER MODE	
000	128	64	2,000
001	64	32	4,000
010	32	16	8,000
011	16	8	16,000
100	8	4	32,000
101 - 111	Reserved	Reserved	Reserved

式 8 shows the scaled Z-domain transfer function of the sinc filter.

$$H(Z) = \left[\frac{1 - Z^{-N}}{N(1 - Z^{-1})} \right]^5$$

where

- N = decimation ratio (8)

式 9 shows the frequency domain transfer function of the sinc filter.

$$|H(f)| = \left| \frac{\sin\left(\dfrac{\pi N \times f}{f_{MOD}}\right)}{N \sin\left(\dfrac{\pi \times f}{f_{MOD}}\right)} \right|^5$$

where

- N = Decimation ratio (see 表 8)
- f = Input signal frequency
- f_{MOD} = Modulator sampling frequency = f_{CLK} / 4 (high resolution mode), f_{CLK} / 8 (low-power mode) (9)

The frequency response of the sinc filter contains notches (or zeros) that occur at the output data rate frequency and multiples thereof. At these frequencies, the filter has zero gain. 図 49 shows the wide-band frequency response of the sinc filter and 図 50 shows the –3-dB response.

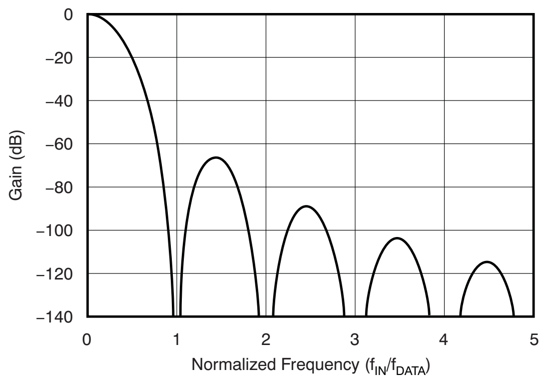


図 49. Sinc Filter Frequency Response

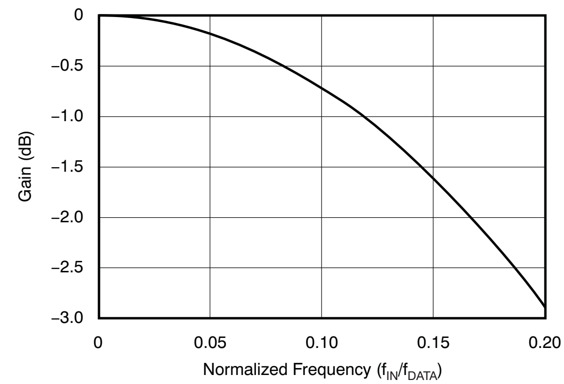


図 50. Sinc Filter –3-dB Response

9.3.5.2 FIR Filter Stage

The second stage of the ADS1287 digital filter is the FIR low-pass filter. Data are supplied to the FIR stage from the pre-filter, sinc stage. The FIR filter performs the final frequency response shaping. 図 51 shows that the FIR filter is composed of four sub-stages.

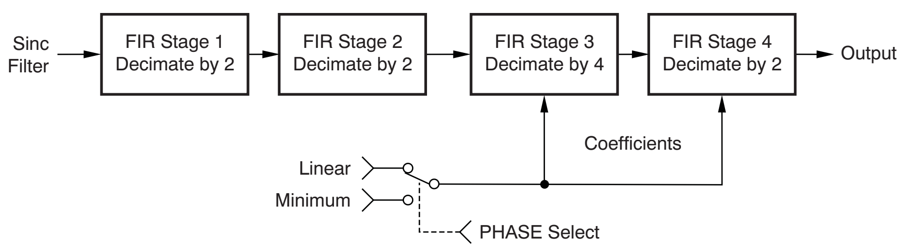


図 51. FIR Filter

The first two FIR stages are half-band filters with fixed decimation ratios equal to 2. The third stage decimates by a ratio equal to 4, and the fourth stage decimates by ratio equal to 2. The overall decimation ratio of the FIR stage is 32. Two coefficient sets are selectable by register bits for the third and fourth sections, one for the linear phase and one for the minimum phase response. 表 9 lists the data rates and combined decimation ratios of the sinc and FIR stage. 表 10 lists the filter coefficients that correspond to each FIR stage.

表 9. FIR Filter Data Rates

DR[2:0] REGISTER BITS	COMBINED DECIMATION RATIO (N)		FIR DATA RATE (SPS)
	HIGH-RESOLUTION MODE	LOW-POWER MODE	
000	4096	2048	62.5
001	2048	1024	125
010	1024	512	250
011	512	256	500
100	256	128	1000
101–111	Reserved	Reserved	Reserved

表 10. FIR Stage Coefficients

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
	LINEAR PHASE SCALING = 1 / 512	LINEAR PHASE SCALING = 1 / 8388608	SCALING = 1 / 134217728		SCALING = 1 / 134217728	
			LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_0	3	–10944	0	819	–132	11767
b_1	0	0	0	8211	–432	133882
b_2	–25	103807	–73	44880	–75	769961
b_3	0	0	–874	174712	2481	2940447
b_4	150	–507903	–4648	536821	6692	8262605
b_5	256	0	–16147	1372637	7419	17902757
b_6	150	2512192	–41280	3012996	–266	30428735
b_7	0	4194304	–80934	5788605	–10663	40215494
b_8	–25	2512192	–120064	9852286	–8280	39260213
b_9	0	0	–118690	14957445	10620	23325925
b_{10}	3	–507903	–18203	20301435	22008	–1757787
b_{11}		0	224751	24569234	348	–21028126
b_{12}		103807	580196	26260385	–34123	–21293602
b_{13}		0	893263	24247577	–25549	–3886901
b_{14}		–10944	891396	18356231	33460	14396783
b_{15}			293598	9668991	61387	16314388
b_{16}			–987253	327749	–7546	1518875
b_{17}			–2635779	–7171917	–94192	–12979500
b_{18}			–3860322	–10926627	–50629	–11506007
b_{19}			–3572512	–10379094	101135	2769794
b_{20}			–822573	–6505618	134826	12195551
b_{21}			4669054	–1333678	–56626	6103823
b_{22}			12153698	2972773	–220104	–6709466
b_{23}			19911100	5006366	–56082	–9882714
b_{24}			25779390	4566808	263758	–353347
b_{25}			27966862	2505652	231231	8629331
b_{26}			25779390	126331	–215231	5597927
b_{27}			19911100	–1496514	–430178	–4389168
b_{28}			12153698	–1933830	34715	–7594158
b_{29}			4669054	–1410695	580424	–428064
b_{30}			–822573	–502731	283878	6566217
b_{31}			–3572512	245330	–588382	4024593
b_{32}			–3860322	565174	–693209	–3679749
b_{33}			–2635779	492084	366118	–5572954
b_{34}			–987253	231656	1084786	332589
b_{35}			293598	–9196	132893	5136333
b_{36}			891396	–125456	–1300087	2351253
b_{37}			893263	–122207	–878642	–3357202
b_{38}			580196	–61813	1162189	–3767666
b_{39}			224751	–4445	1741565	1087392
b_{40}			–18203	22484	–522533	3847821
b_{41}			–118690	22245	–2490395	919792
b_{42}			–120064	10775	–688945	–2918303
b_{43}			–80934	940	2811738	–2193542
b_{44}			–41280	–2953	2425494	1493873
b_{45}			–16147	–2599	–2338095	2595051
b_{46}			–4648	–1052	–4511116	–79991
b_{47}			–874	–43	641555	–2260106
b_{48}			–73	214	6661730	–963855

表 10. FIR Stage Coefficients (continued)

COEFFICIENT	SECTION 1 LINEAR PHASE SCALING = 1 / 512	SECTION 2 LINEAR PHASE SCALING = 1 / 8388608	SECTION 3 SCALING = 1 / 134217728 LINEAR PHASE	SECTION 3 SCALING = 1 / 134217728 MINIMUM PHASE	SECTION 4 SCALING = 1 / 134217728 LINEAR PHASE	SECTION 4 SCALING = 1 / 134217728 MINIMUM PHASE
b_{49}			0	132	2950811	1482337
b_{50}			0	33	–8538057	1480417
b_{51}			0	0	–10537298	–586408
b_{52}					9818477	–1497356
b_{53}					41426374	–168417
b_{54}					56835776	1166800
b_{55}					41426374	644405
b_{56}					9818477	–675082
b_{57}					–10537298	–806095
b_{58}					–8538057	211391
b_{59}					2950811	740896
b_{60}					6661730	141976
b_{61}					641555	–527673
b_{62}					–4511116	–327618
b_{63}					–2338095	278227
b_{64}					2425494	363809
b_{65}					2811738	–70646
b_{66}					–688945	–304819
b_{67}					–2490395	–63159
b_{68}					–522533	205798
b_{69}					1741565	124363
b_{70}					1162189	–107173
b_{71}					–878642	–131357
b_{72}					–1300087	31104
b_{73}					132893	107182
b_{74}					1084786	15644
b_{75}					366118	–71728
b_{76}					–693209	–36319
b_{77}					–588382	38331
b_{78}					283878	38783
b_{79}					580424	–13557
b_{80}					34715	–31453
b_{81}					–430178	–1230
b_{82}					–215231	20983
b_{83}					231231	7729
b_{84}					263758	–11463
b_{85}					–56082	–8791
b_{86}					–220104	4659
b_{87}					–56626	7126
b_{88}					134826	–732
b_{89}					101135	–4687
b_{90}					–50629	–976
b_{91}					–94192	2551
b_{92}					–7546	1339
b_{93}					61387	–1103
b_{94}					33460	–1085
b_{95}					–25549	314
b_{96}					–34123	681
b_{97}					348	16

表 10. FIR Stage Coefficients (continued)

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
	LINEAR PHASE SCALING = 1 / 512	LINEAR PHASE SCALING = 1 / 8388608	SCALING = 1 / 134217728		SCALING = 1 / 134217728	
			LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{98}					22008	–349
b_{99}					10620	–96
b_{100}					–8280	144
b_{101}					–10663	78
b_{102}					–266	–46
b_{103}					7419	–42
b_{104}					6692	9
b_{105}					2481	16
b_{106}					–75	0
b_{107}					–432	–4
b_{108}					–132	0
b_{109}					0	0

As shown in 図 52, the FIR frequency response provides a flat pass-band response (±0.003 dB) to 0.375 f_{DATA}. 図 53 shows the transition band beginning from the edge of the pass band and ending at the beginning of the stop band. The stop-band response is typically –135 dB above the Nyquist frequency.

As with all oversampled systems, the pass-band response repeats at the underlying ADC sample rate. In this case, the response repeats at multiples of the modulator frequency ($N \cdot f_{MOD} – f_0$ and $N \cdot f_{MOD} + f_0$, where N = 1, 2, and so on, and f_0 = filter pass band). These image frequencies, if not filtered and otherwise present in the signal, fold back (or alias) into the pass band causing errors. A low-pass input filter reduces aliasing. For many applications, the single-pole filter provided at the PGA output is sufficient to suppress the aliased frequencies.

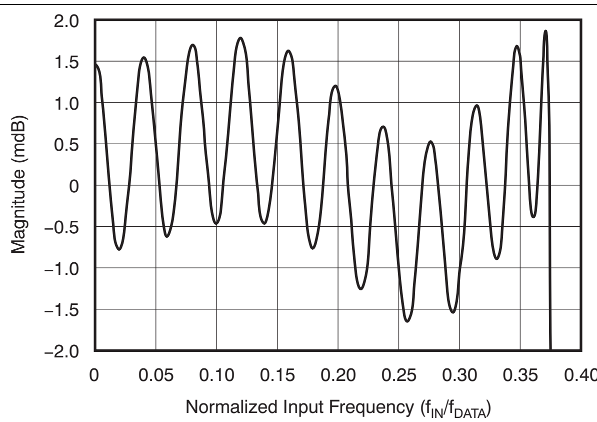


図 52. FIR Filter Pass-Band Magnitude Response

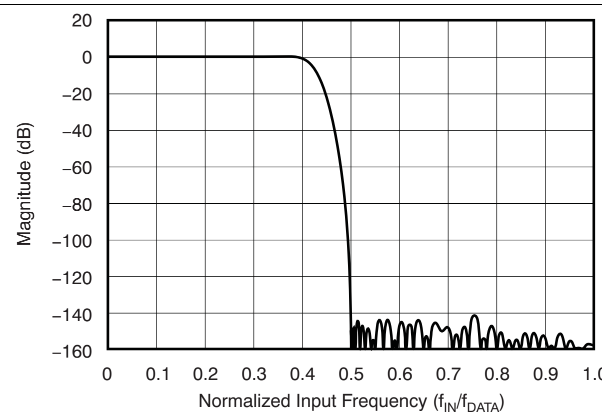


図 53. FIR Filter Transition Band Magnitude Response

9.3.5.3 Group Delay and Step Response

The FIR filter has selectable linear or minimum phase response. The pass-band, transition band, and stop-band responses of the linear and minimum phase filters are similar but differ in the respective phase response.

9.3.5.3.1 Linear Phase Response

Linear phase filters have the property that the input-to-output delay is constant across all input frequencies (that is, constant group delay). The constant delay property is independent of the nature of the input signal (pulsed or swept-tone). This filter provides low phase linearity error across frequency when analyzing multi-tone input signals. However, as shown in 図 54, the associated group delay is longer than that of the minimum phase filter. The specified number of conversions to result in fully settled data is the same for the linear and minimum filter profiles.

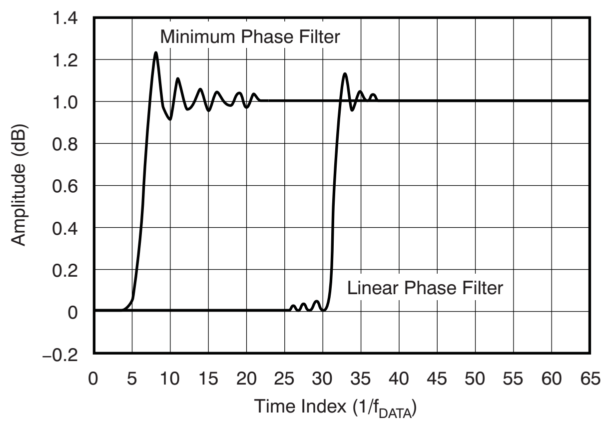


図 54. FIR Step Response

9.3.5.3.2 Minimum Phase Response

Compared to the linear phase filter, the minimum phase filter provides a shorter delay from the arrival of an input event to the event appearing in the data output. As shown in 図 55, the relationship (phase) is not constant versus frequency. 表 11 shows that the filter phase is selected by the PHS bit.

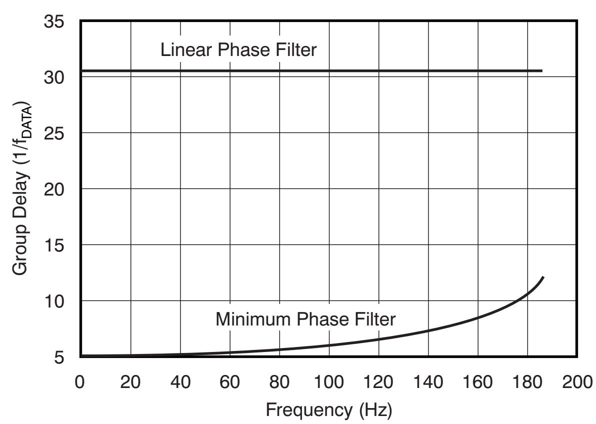


図 55. FIR Group Delay (f_{DATA} = 500 SPS)

表 11. FIR Phase Selection

PHS REGISTER BIT	FILTER PHASE
0	Linear
1	Minimum

9.3.5.4 HPF Stage

The last stage of the digital filter is a high-pass filter (HPF) implemented as a first-order, IIR structure. This filter stage blocks DC signals and rolls off low-frequency components below the cutoff frequency. 式 10 shows the transfer function for the filter:

$$HPF(Z) = \frac{2 - a}{2} \times \frac{1 - Z^{-1}}{1 - bZ^{-1}} \quad (10)$$

where

- *b* is calculated as shown in 式 11:

$$b = \frac{1 + (1 - a)^2}{2} \quad (11)$$

The high-pass filter corner frequency is programmed by the HPF[1:0] register bits, in hexadecimal. 式 12 is used to set the high-pass filter corner frequency. 表 12 lists example values for the high-pass filter.

$$HPF[1:0] = 65{,}536 \left[1 - \sqrt{1 - 2\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}} \right] \quad (12)$$

where

- HPF = High-pass filter register value (converted to hexadecimal)
- $\omega_N = 2\pi f_{HP} / f_{DATA}$ (normalized frequency, radians)
- f_{HP} = High-pass filter corner frequency (Hz)
- f_{DATA} = Data rate (Hz)

表 12. High-Pass Filter Value Examples

HPF1, HPF0	f_{HP} (Hz)	DATA RATE (SPS)
0337h	0.5	250
0337h	1.0	500
019Ah	1.0	1000

式 13 shows the HPF frequency domain transfer function. The HPF results in a small gain error that depends on the ratio of f_{HP} / f_{DATA}. For many common values of (f_{HP} / f_{DATA}), the gain error is negligible. 図 56 shows the gain error of the HPF.

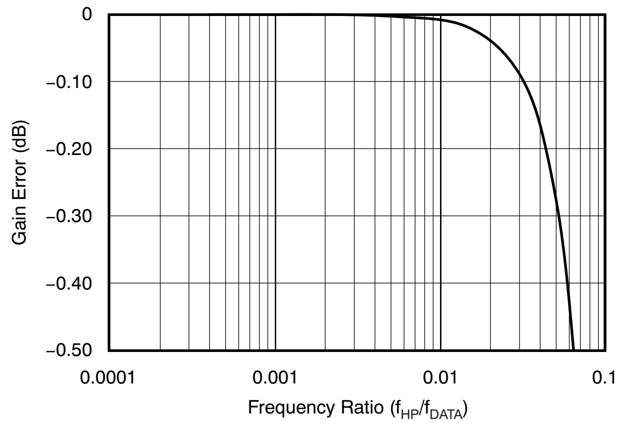


図 56. HPF Gain Error

$$\text{HPF Gain} = \frac{1 + \sqrt{1 - 2\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)}}{2 - \left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)} \qquad (13)$$

図 57 shows the first-order amplitude and phase response of the HPF. In the case of applied step input or after synchronizing, make sure to take the settling time of the filter into account.

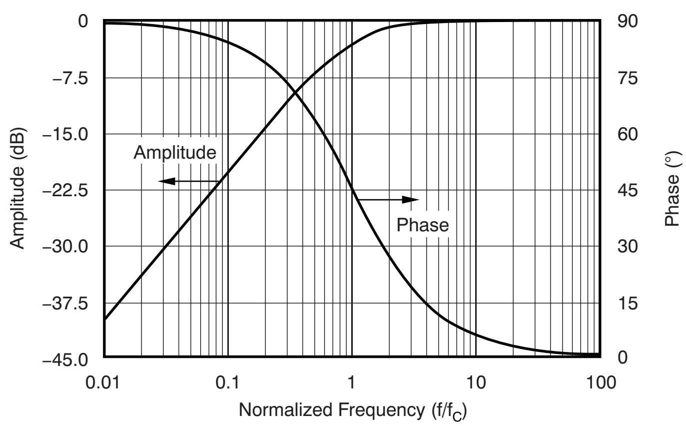


図 57. HPF Amplitude and Phase Response

9.3.6 Reset ($\overline{RESET}$ Pin and Reset Command)

The ADC is reset in one of three ways: at power-up, by the $\overline{RESET}$ pin, or by the RESET command. By pin, drive $\overline{RESET}$ low for at least 2 f_{CLK} cycles to force a reset. The ADC is held in reset until the pin is released high. By command, reset takes effect on the next rising f_{CLK} edge occurring after the eighth rising edge of SCLK. In order to ensure a functional reset by command, the SPI interface may itself require reset; see the *Serial Interface* section for details. When the ADC is reset, registers are reset to default values and the conversions are synchronized on the next rising edge of CLK. Reset timing is illustrated in 図 5, the *Timing Requirements* table, and the *Switching Characteristics* table.

9.3.7 Master Clock Input (CLK)

The ADC requires an external clock for operation. The nominal clock frequency is 1.024 MHz. The clock is applied to the CLK pin with an amplitude equal to the DVDD supply. As with many precision data converters, a high-quality clock free from glitches is essential to achieve rated performance. A crystal- or MEMS-type clock source is recommended because of good temperature stability and low jitter. Make sure to avoid ringing on the clock input; keep the clock PCB trace as short as possible and routed away from the analog inputs, the PGA output pins (CAPP, CAPN), and associated analog components. Use a 50-Ω series resistor to terminate the PCB trace impedance with the resistor placed close to the clock buffer.

9.4 Device Functional Modes

9.4.1 Operational Mode

The ADC has two modes of operation: high resolution and low power. High-resolution mode provides the lowest noise (maximum SNR performance), whereas low-power mode offers lower power consumption at the expense of increased noise. 表 13 summarizes noise performance, power consumption, and associated register setting for each mode. The three register bits, located in the ID/CFG and CONFIG0 registers, must all be set to the same value (all 0s or all 1s).

表 13. High-Resolution, Low-Power Modes

REGISTER BITS MODE2, MODE1, MODE0	OPERATIONAL MODE	SNR (dB)(1)	POWER (mW)
111	High resolution	113	4.5
000	Low power	110	2.4

(1) SNR at gain = 1, f_{DATA} = 1000 SPS.

9.4.2 Chop Mode

The chop mode modulates the PGA offset and 1/f noise to a frequency outside the ADC pass band where the offset and 1/f noise residue is removed by the digital filter. Small transient currents occur on the PGA inputs because of the stray capacitance associated with the internal chop switches. Although the average value of the transient currents results in high input impedance (> 20 GΩ), in some cases, the transient currents can interact with high-impedance sensors leading to degraded performance. For these applications, disable the chop mode. For common types of geophone sensors, chop mode is recommended. Chop mode is enabled by the CHOP bit of the CONFIG1 register (default is chop enabled).

9.4.3 Offset

As with most ΔΣ modulators, the ADC can produce low-level idle tones (typically 140 dB below the full-scale amplitude). The idle tones appear as low-frequency components in the output data when either no- or low-level signals are present. Typically, idle tones do not occur when high-level signals are present. The ADC incorporates an internal offset option that is intended to reduce the amplitudes of the tone. The offset is recommended for the low-power mode operation only and is not recommended for the high-resolution mode operation. Use the external offset circuit illustrated in the *Application Information* section for idle tone reduction in high-resolution mode operation.

The offset is enabled by the OFFSET bit of the ID_CFG register. The offset voltage is 50 mV. The 50-mV offset leads to 2% reduction of the input range that is restored by calibrating the offset voltage by use of the offset calibration registers. Offset correction is accomplished by performing offset calibration, or to provide nominal correction, write 029700h to the calibration registers.

9.4.4 Power-Down Mode

Power the ADC down by driving the $\overline{\text{PWDN}}$ pin low. In power-down mode, the ADC is powered off, including the internal LDO. In addition, the LDO output (BYPAS pin) connects to DVDD in order to prevent internal floating circuit nodes to ensure the ADC draws very low leakage current from the supplies. When powered down, the device outputs remain powered and the device inputs must not be allowed to float, otherwise DVDD leakage current can occur. The ADC register settings are reset in power-down mode; see 図 6 for power-down mode timing details.

9.4.5 Standby Mode

Standby is the software power-down mode. In standby mode, the analog and most of the digital circuit blocks are powered down while the serial interface and the register banks remain active. See the *Electrical Characteristics* table for the DVDD supply current in STANDBY mode. To engage standby mode, send the STANDBY command. To exit standby mode, send the WAKEUP command. 図 6 and the *Switching Characteristics* table show the timing. Standby mode is exited whenever $\overline{\text{CS}}$ is high.

The STANDBY, WAKEUP command sequence restores the previous synchronization timing that is lost as a result of register write operations (continuous-sync mode). See the *Continuous-Sync Mode* section for details on how to restore synchronization.

9.4.6 Synchronization

The ADC is synchronized by either the SYNC pin or by the SYNC command. Synchronization by pin occurs on the next rising edge of CLK after the rising edge of SYNC. Synchronization by command occurs on the next rising edge of CLK after the eighth bit of the command is received. The ADS1287 has two functional synchronization modes: pulse sync and continuous sync.

9.4.6.1 Pulse-Sync Mode

In pulse-sync mode, the ADC unconditionally synchronizes on the rising edge of SYNC. When the ADC synchronizes, the conversion in progress is stopped and a new conversion is started. The internal filter memory is reset at the start of the new conversion. As a result of the computational latency of the digital filter, the ADC suppresses the first 63 conversion results until the digital filter is fully settled. 図 4, the *Timing Requirements* table, and the *Switching Characteristics* table illustrate the SYNC input timing and conversion propagation delays.

The ADC also synchronizes at the occurrence of a register write operation and the previous synchronization is lost. To re-synchronize, pulse the SYNC pin (or send the SYNC command) at the desired time, after the register write operation.

9.4.6.2 Continuous-Sync Mode

In continuous-sync mode, the ADC synchronizes on the first rising edge of the SYNC pin after configuring the ADC to the continuous-sync mode. On the subsequent rising edges of SYNC, the ADC re-synchronizes only if the SYNC input period is not equal to an integer multiple of the data rate period by at least ±1 / f_{CLK} (that is, the SYNC period ≠ N /f_{DATA} ± 1 /f_{CLK}, where N = 1, 2, 3, and so forth). The period of SYNC can be indefinite. If the periods are not divisible by an integer, the ADC re-synchronizes. In this mode, a periodic synchronizing clock can be applied to the ADC, resulting in autonomous synchronization.

When synchronization occurs, $\overline{\text{DRDY}}$ continues to pulse but the ADC forces the data to zero until the data are settled (approximately 63 $\overline{\text{DRDY}}$ periods later). At the 63rd conversion, valid data are output. See 図 4 for an illustration of $\overline{\text{DRDY}}$ behavior. The phase relationship between SYNC and $\overline{\text{DRDY}}$ also depends on the data rate because of the slight dependence of filter group delay to data rate. 図 58 shows an example of the phase relationship between SYNC and $\overline{\text{DRDY}}$. The SYNC pin only can be used to control continuous-sync mode.

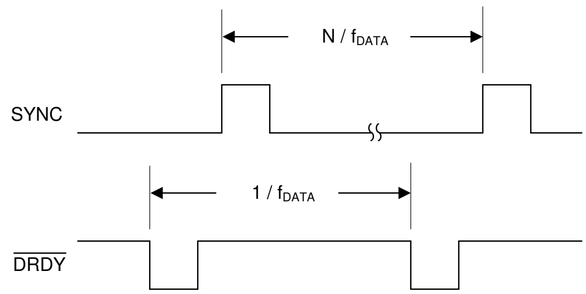


図 58. Continuous-Sync Mode

The ADC synchronizes at the occurrence of a register write operation resulting in loss of the previous synchronization. To re-establish the previous synchronization (in continuous-sync mode), send the STANDBY, WAKEUP command sequence. The re-synchronization sequence is valid provided the time between the STANDBY and WAKEUP commands is not equal to the data rate period by at least ± 1 / f_{CLK} period.

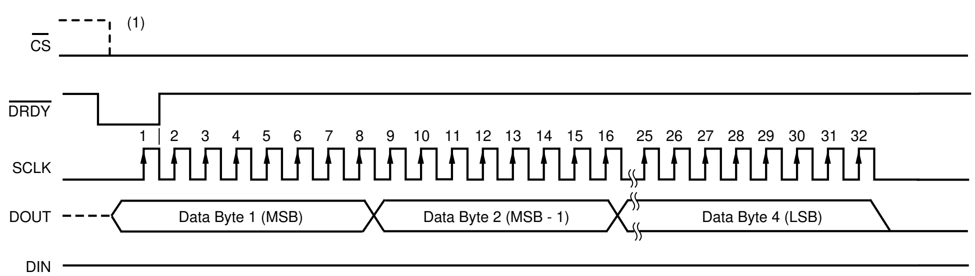
9.4.7 Reading Data

The ADC has two modes to read conversion data: read-data-continuous (RDATAC mode) and read-data-by-command (SDATAC mode).

9.4.7.1 Read-Data-Continuous Mode (RDATAC)

In read-data-continuous mode, conversion data are read without the need of a read data command. When $\overline{\text{DRDY}}$ asserts low (indicating new data), the MSB of data appears on DOUT. Read data by applying the serial interface clock on SCLK; see 図 3 for $\overline{\text{DRDY}}$ to DOUT timing.

As shown in 図 59, conversion data are read by first driving $\overline{\text{CS}}$ low and then shifting the data by applying the serial interface clock to SCLK. Latch the data on the rising edge of SCLK. On the first falling edge of SCLK, the ADC returns $\overline{\text{DRDY}}$ high. After all 32 bits of conversion data are read, further SCLK transitions result in DOUT driven low. If desired, the read operation can be stopped after 24 bits. A new read cycle is started when new conversion data are available. The data read operation must be completed four CLK periods prior to the next $\overline{\text{DRDY}}$ falling edge, otherwise the data are overwritten with new conversion data.

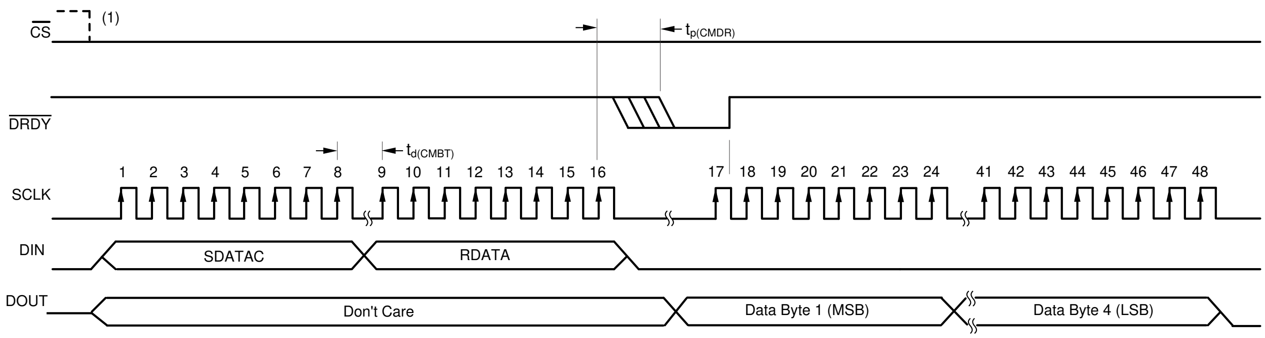


(1) DOUT is in tri-state mode when $\overline{\text{CS}}$ is high. SCLK arrows indicate when the data are latched.

図 59. Read-Data-Continuous Mode

9.4.7.2 Stop-Read-Data-Continuous-Mode (SDATAC)

In SDATAC mode, a command is required in order to read conversion data. Send the SDATAC command to first engage the mode. Send an RDATA command, as shown in 図 60, for each data retrieval operation. After the eighth SCLK rising edge of the RDATA command, conversion data are ready when the ADC drives $\overline{DRDY}$ low (see the *Switching Characteristics* table for $t_{P(CMDR)}$ timing). $t_{P(CMDR)}$ is dependent on the timing of the command relative to the conversion phase. When $\overline{DRDY}$ goes low, MSB conversion data appear on DOUT and the data shift operation can begin (see 図 3 for $\overline{DRDY}$ to DOUT timing). The RDATA command must be sent at least as often as the data rate or data are lost. Driving $\overline{CS}$ high cancels the SDATAC mode; therefore, the SDATAC mode must be reset if $\overline{CS}$ is taken high prior to each RDATA operation.



(1) If $\overline{CS}$ taken high, send the SDATAC command prior to the RDATA command. SCLK arrows indicate when the data are latched.

図 60. Read Data By Command Mode

9.4.8 Conversion Data Format

As shown in 表 14, the conversion data are 32 bits in binary two's complement format. The LSB of the data is a redundant sign bit: 0 for positive numbers and 1 for negative numbers. However, when the data are clipped to FS, the LSB = 1 and when the data are clipped to –FS, the LSB = 0. If desired, the data readback can be stopped after 24 bits. In sinc-filter mode, the data are numerically scaled by half.

表 14. Ideal Output Code Versus Input Signal

INPUT SIGNAL V_{IN}	32-BIT IDEAL OUTPUT CODE(1) FIR FILTER	32-BIT IDEAL OUTPUT CODE(1) SINC FILTER(2)
> V_{REF} / Gain	7FFFFFFFh	—(3)
V_{REF} / Gain	7FFFFFFEh	3FFFFFFFh
V_{REF} / (Gain · 2^{30})	00000002h	00000001h
0	00000000h	00000000h
–V_{REF} / (Gain · 2^{30})	FFFFFFFFh	FFFFFFFFh
–V_{REF} / (Gain · (2^{30}/ (2^{30} – 1)))	80000001h	C0000000h
< –V_{REF} / (Gain · (2^{30}/ (2^{30} – 1)))	80000000h	—(3)

(1) Excludes effects of noise, linearity, offset, and gain errors.
(2) As a result of the reduction in oversampling ratio (OSR) related to high data rates of the sinc filter mode, the available ADC resolution correspondingly reduces.
(3) When the full-scale range is exceeded in sinc filter mode, the conversion data exceeds half-scale code (3FFFFFFFh and C0000000h).

9.4.9 Offset and Full-Scale Calibration Registers

Offset and gain errors are corrected by the offset and full-scale calibration registers. As shown in 図 61, the conversion result is first subtracted by the offset register (OFC) and then multiplied by the correction factor derived from the full-scale register (FSC). These operations occur before the 32-bit clip stage. 式 14 shows the offset and full-scale correction.

$$\text{Final Output Data} = (\text{Input} - \text{OFC[2:0]}) \times \frac{\text{FSC[2:0]}}{400000\text{h}} \tag{14}$$

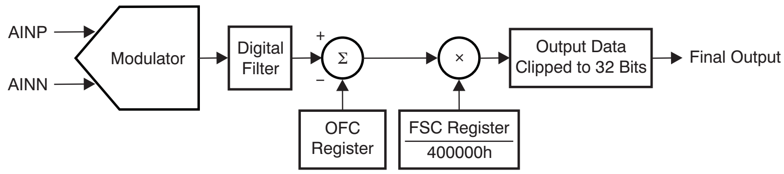


図 61. Calibration Block Diagram

The offset and full-scale registers are written directly by the user, or the values are determined automatically as a result of calibration operations. One set of offset and full-scale registers apply for all gain factors. Unique values, depending on system accuracy requirements, may be required for each gain to improve the gain-matching performance. The calibration operation is bypassed in the sinc filter mode.

9.4.9.1 OFC[2:0] Registers

表 15 shows that the offset calibration register is a 24-bit word composed of three 8-bit registers. The offset register is left-justified in order to align with the 32-bit conversion data. The offset value is in two's complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. The register data are subtracted from the conversion data. Register data equal to 00000h perform no offset correction (default).

表 15. Offset Calibration Word

REGISTER	BYTE	BIT ORDER							
OFC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
OFC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Although the offset calibration register can accommodate values from –FS to FS (as shown in 表 16), the post-calibrated input voltage cannot exceed 106% of the nominal input range.

表 16. Offset Calibration Values

OFC[2:0] REGISTERS	FINAL OUTPUT CODE (1)
00007Fh	FFFF8100h
000001h	FFFFFF00h
000000h	00000000h
FFFFFFh	00000100h
FFFF7Fh	00008100h

(1) Ideal post-calibration value with zero voltage input.

9.4.9.2 FSC[2:0] Registers

表 17 shows that the full-scale calibration register is a 24-bit word, composed of three 8-bit registers. The full-scale calibration value is 24-bit, straight-offset binary, normalized to a scale factor of 1.0 for a register value of 400000h.

表 17. Full-Scale Calibration Word

REGISTER	BYTE	BIT ORDER							
FSC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
FSC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

表 18 summarizes the scaling of the full-scale calibration register. A register value equal to 400000h (default value) yields a unity-gain scale factor. Although the full-scale calibration register value can be used to correct gain errors > 1 (gain scale factor < 1), the post-calibrated input voltage cannot exceed 106% of the nominal input range.

表 18. Full-Scale Calibration Register Values

FSC[2:0] REGISTERS	SCALE FACTOR
433333h	1.05
400000h	1.00
3CCCCCh	0.95

9.4.10 Calibration Command

The calibration commands (OFSCAL or GANCAL) perform calibration on demand. These commands compute the offset and gain correction register factors, respectively. The appropriate calibration voltage must be applied for calibration. Low data rates are able to provide more consistent calibration results resulting from lower noise compared to high data rates. If calibrating at system power-on, be sure the reference voltage is fully settled. Calibration is not available when operating in the sinc filter mode.

図 62 shows the calibration command sequence. Apply the appropriate calibration voltage to the ADC. After the input voltage stabilizes, send the SDATAC, SYNC, and RDATAC commands in sequence (allow 24 / f_{CLK} gaps between commands). $\overline{DRDY}$ is then driven low 64 data periods later. After $\overline{DRDY}$ is driven low, send the SDATAC command, then the calibration command (OFSCAL or GANCAL), followed by the RDATAC command. After 16 data periods, calibration completion is indicated when $\overline{DRDY}$ is driven low. The calibrated conversion data are available at this time. The SYNC input must remain high during the calibration sequence.

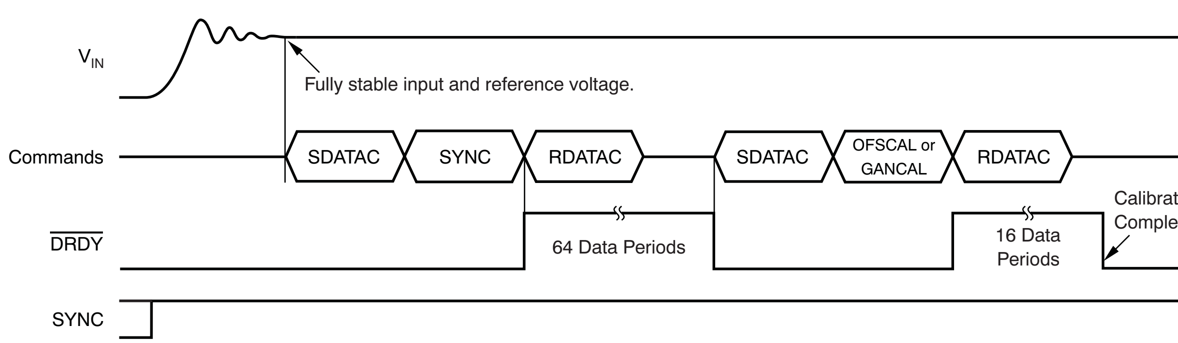


図 62. Calibration Command Sequence

9.4.10.1 OFSCAL Command

The OFSCAL command performs the offset calibration. To calibrate, apply a zero voltage input to the ADC or select the internal shorted input channel via the input multiplexer and allow the inputs to stabilize. Send the command sequence as illustrated in 図 62. The ADC averages 16 readings to reduce the effects of noise and then writes the 24-bit truncated result to the OFC register. During offset calibration, the full-scale correction is bypassed. The optional 50-mV internal offset can be calibrated using the calibration command in order to restore the full input voltage range.

9.4.10.2 GANCAL Command

The GANCAL command performs gain calibration. To calibrate, apply a positive full-scale DC input to the ADC and allow the inputs to stabilize. Send the command sequence as illustrated in 図 62. The ADC averages 16 readings to reduce the effects of noise and then computes a 24-bit scale factor value. This value is written to the FSC register.

9.4.11 User Calibration

ADC calibration can be performed by the user without using calibration commands. This procedure requires the user to apply the appropriate calibration voltage as with using calibration commands, but in this case the user computes the calibration values based on the conversion result and then writes the value to the calibration registers. The procedure for user calibration is as follows:

1. Set the OFSCAL[2:0] register = 0h, and GANCAL[2:0] = 400000h. These values set the offset and gain factors to 0 and 1, respectively.
2. Apply zero voltage or short the inputs (example: set the ADC mux to internal short). Wait for the input voltage and the ADC to settle for a minimum of 63 conversions and then begin averaging of a number of conversion results. Averaging conversions results in a more accurate calibration. Write the 24-bit averaged value to the OFC register.
3. Apply a DC or AC calibration voltage at least 5% below full-scale. Be sure not to be near or exceed 100% FSR otherwise the conversion data clips, resulting in erroneous calibration. Wait for the calibration voltage and the ADC to settle for a minimum of 63 conversions. Use 式 15 or 式 16 to compute the scale factor value.

式 15 shows the DC calibration voltage. Use the average value of the ADC data.

$$\text{FSC[2:0]} = 400000\text{h} \times \left(\frac{\text{Expected Output Code}}{\text{Actual Output Code}} \right) \tag{15}$$

式 16 shows the AC calibration voltage. Use an RMS value of the ADC data.

$$\text{FSC[2:0]} = 400000\text{h} \times \frac{\text{Expected RMS Value}}{\text{Actual RMS Value}} \tag{16}$$

9.5 Programming

9.5.1 Serial Interface

The serial interface is used to read conversion data and to read or write control register data. The interface is SPI compatible and consists of the following signals: $\overline{\text{CS}}$, SCLK, DIN, and DOUT.

9.5.1.1 Chip Select ($\overline{\text{CS}}$)

Chip select is an active-low input that enables the ADC serial interface for communication. $\overline{\text{CS}}$ must remain low for the duration of the ADC data transfer. When $\overline{\text{CS}}$ is high, SCLK activity is ignored, in-progress data transfer or commands are terminated, and DOUT (data output pin) enters a high-impedance state. When $\overline{\text{CS}}$ is driven high, the ADC terminates standby mode and also resets the mode to read data continuous (RDATAC); see the *Stop-Read-Data-Continuous-Mode (SDATAC)* section for more information.

9.5.1.2 Serial Clock (SCLK)

The serial interface clock (SCLK) is an input that is used to shift data into and out of the ADC. The ADC latches data on DIN at the rising edge of SCLK. Data are shifted out on DOUT at the falling edge of SCLK. Keep SCLK low when not active. The SCLK pin is a noise-resistant, Schmitt-trigger input that reduces the possibility of noise-induced false edges. However, keep SCLK as clean as possible to prevent possible glitches from inadvertently shifting the data.

Programming (continued)

9.5.1.3 Data Input (DIN)

The data input pin (DIN) is used to input register data and commands to the ADC. The ADC latches input data on the rising edge of SCLK. In read-data-continuous mode, keep DIN low when clocking out conversion data. The exception to keeping DIN low is to interrupt the read-data-continuous mode by sending the SDATAC command.

9.5.1.4 Data Output (DOUT)

The data output pin (DOUT) provides the ADC output data. Data are shifted out on the falling edge of SCLK and are read by the user on the following rising edge of SCLK. Keep the DOUT trace length to minimum to reduce the effects of inter-symboling noise effects within the ADC. When $\overline{\text{CS}}$ is high, DOUT is forced to hi-Z.

9.5.1.5 Serial Interface Timeout

When $\overline{\text{CS}}$ is low, the serial interface times-out (resets) if SCLK is held low for 64 $\overline{\text{DRDY}}$ cycles. Reset of the serial interface terminates commands in progress. When reset, the next SCLK pulse starts a new communication cycle. To prevent timeout and reset of the serial interface, provide at least one SCLK pulse for every 64 $\overline{\text{DRDY}}$ pulses.

9.5.1.6 Data Ready ($\overline{\text{DRDY}}$)

$\overline{\text{DRDY}}$ is an output that indicates when new conversion data are ready. $\overline{\text{DRDY}}$ is always actively driven regardless whether $\overline{\text{CS}}$ is high or low. When reading data in the read data continuous mode, the read operation must be completed four CLK periods prior to the next $\overline{\text{DRDY}}$ falling edge, or the data are overwritten by new conversion data.

During data readback, $\overline{\text{DRDY}}$ is driven high on the first falling edge of SCLK. 図 63 and 図 64 show the function of $\overline{\text{DRDY}}$ with and without data readback, respectively. If data are not retrieved (no SCLK provided), as shown in 図 64, $\overline{\text{DRDY}}$ pulses high for four f_{CLK} periods during the update time.

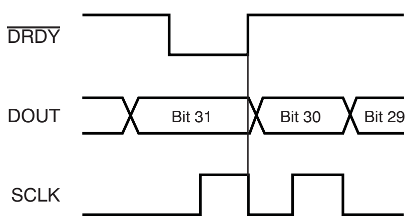


図 63. $\overline{\text{DRDY}}$ With Data Retrieval

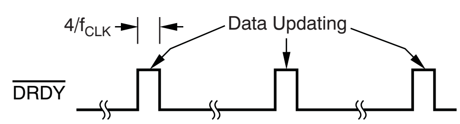


図 64. $\overline{\text{DRDY}}$ With No Data Retrieval

Programming (continued)

9.5.2 Commands

The commands listed in 表 19 control ADC operation. Most commands are stand-alone (that is, one byte in length); the register read and write command lengths are two bytes, plus additional data bytes that represent the actual register data.

表 19. Command Descriptions

COMMAND	TYPE	DESCRIPTION	1ST COMMAND BYTE(1)(2)	2ND COMMAND BYTE(3)
WAKEUP	Control	Wake-up from standby mode	0000 000X (00h or 01h)	
STANDBY	Control	Enter standby mode	0000 001X (02h or 03h)	
SYNC	Control	Synchronize ADC conversions	0000 010X (04h or 5h)	
RESET	Control	Reset the ADC	0000 011X (06h or 07h)	
RDATAC	Control	Read data continuous mode	0001 0000 (10h)	
SDATAC	Control	Stop read data continuous mode	0001 0001 (11h)	
RDATA	Data	Read data by command(4)	0001 0010 (12h)	
RREG	Register	Read *nnnnn* registers at address *rrrrr*(4)	001*r rrrr* (20h + 000*r rrrr*)	000*n nnnn* (00h + *n nnnn*)
WREG	Register	Write *nnnnn* registers at address *rrrrr*	010*r rrrr* (40h + 000*r rrrr*)	000*n nnnn* (00h + *n nnnn*)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	

(1) X = don't care.
(2) rrrrr = starting address for register read and write commands.
(3) nnnnn = number of registers to be read from or written to – 1. For example, to read from or write to three registers, set *nnnnn* = 2 (00010).
(4) Required to cancel read-data-continuous mode before sending a command.

$\overline{CS}$ must remain low for the duration of the command-byte sequence. Provide a 24 / f_{CLK} delay between commands, between bytes within a command, and from the last byte of a command prior to returning $\overline{CS}$ high. The required delay starts from the last SCLK rising edge of the preceding byte to the first SCLK rising edge of the following byte; see 図 2. The delay between data bytes is not necessary when reading conversion data.

9.5.2.1 WAKEUP: Wake Up Command

The WAKEUP command is used to exit standby mode and to resume normal operation. The STANDBY, WAKEUP sequence is illustrated in 図 65. 図 6 illustrates the time for new conversion data. After writing the ADC registers, the ADC restarts the filter cycle and, as a consequence, results in loss of the previous synchronization. In continuous synchronization mode, use the STANDBY, WAKEUP command sequence to restore the previous synchronization; see the *Continuous-Sync Mode* section for details.

9.5.2.2 STANDBY: Standby Mode Command

The STANDBY command engages standby mode. In standby, ADC conversions are stopped and the ADC enters a low-power mode. The register settings are retained in this mode. The ADC remains in standby mode until $\overline{CS}$ is taken high or the WAKEUP command is sent. For complete device shutdown, take the $\overline{PWDN}$ pin low. 図 65 shows the operation of the STANDBY, WAKEUP sequence.

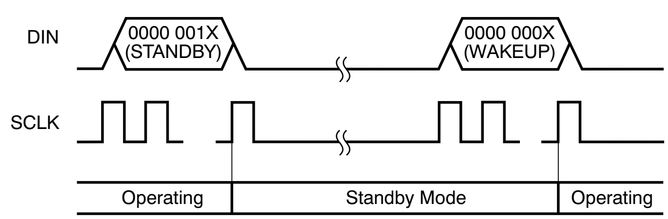


図 65. STANDBY Command Sequence

9.5.2.3 SYNC: Synchronize ADC Conversions

The SYNC command synchronizes the analog-to-digital conversion. Upon receiving the SYNC command, the read in progress is cancelled and the conversion process is restarted. In order to synchronize multiple ADCs, the command must be sent simultaneously to all devices. The SYNC pin must be held high when this command used. The SYNC command is also required in the calibration command sequence.

9.5.2.4 RESET: Reset Command

The RESET command resets the ADC. RESET sets the registers back to default, restarts the conversion process, and engages read-data-continuous mode. The RESET command is functionally equivalent to using the $\overline{\text{RESET}}$ pin, however toggle the $\overline{\text{CS}}$ pin prior to the RESET command to ensure that the serial interface is reset. See 図 5 for the RESET command timing.

9.5.2.5 RDATAC: Read Data Continuous Mode Command

The RDATAC command programs the read-data-continuous mode (default mode). In this mode, conversion data can be read directly by applying serial interface clocks (no read data command is necessary). Each time $\overline{\text{DRDY}}$ transitions low, new data are available to read; see the *Read-Data-Continuous Mode (RDATAC)* section for more details.

9.5.2.6 SDATAC: Stop Read Data Continuous Mode Command

The SDATAC command stops read-data-continuous mode. This mode is required before sending register read or write commands and before issuing the data read command (RDATA). $\overline{\text{CS}}$ high cancels the SDATAC mode. Send the RDATAC command to cancel SDATAC mode; see the *Stop-Read-Data-Continuous-Mode (SDATAC)* section for more details.

9.5.2.7 RDATA: Read Data Command

The RDATA command is necessary to read the conversion data in SDATAC mode. The RDATA command must be sent for each read of conversion data; see the *Stop-Read-Data-Continuous-Mode (SDATAC)* section for details.

9.5.2.8 RREG: Read Register Data Command

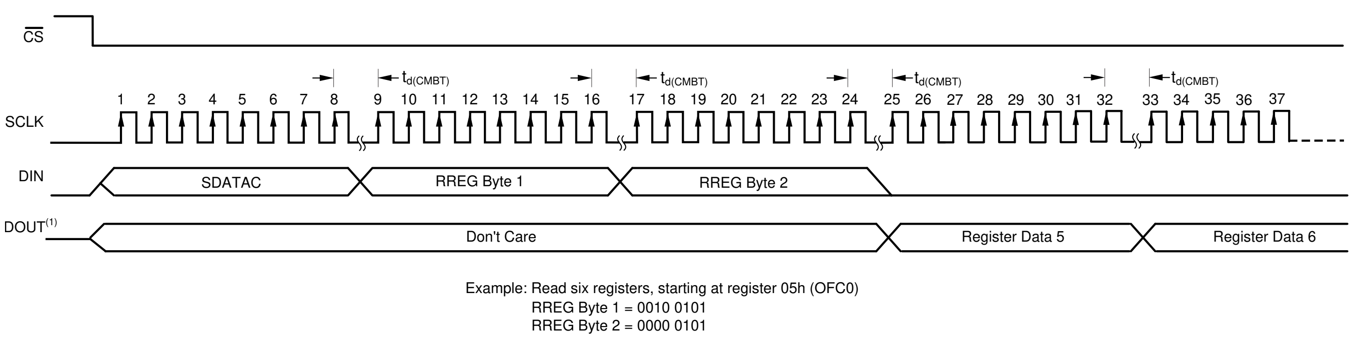
The RREG command is used to read a single register byte or to read multiple register bytes. The command consists of a two-byte argument followed by the output of register data. The first byte of the command is the register starting address, and the second byte specifies the number of registers to read minus one.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers to read minus one.

In the read register data example sequence shown in 図 66, with the 24th falling edge of SCLK, the first register data bit appears on DOUT. Read the first bit of register data on the 25th SCLK rising edge.

See the *Timing Requirements* table for the specification of the $t_{d(CMBT)}$ parameter.



(1) DOUT is in tri-state when $\overline{\text{CS}}$ is high.

図 66. Read Register Data

In read-data-continuous mode, the output data shift register is written with new conversion data just before DRDY transitions low. To avoid conflicting data between conversion data and register data, send the SDATAC command before reading register data. The SDATAC command disables loading of conversion data into the output data shift register. Keep CS low between the SDATAC command and the read register command because CS high cancels the SDATAC mode.

9.5.2.9 WREG: Write Register Data Command

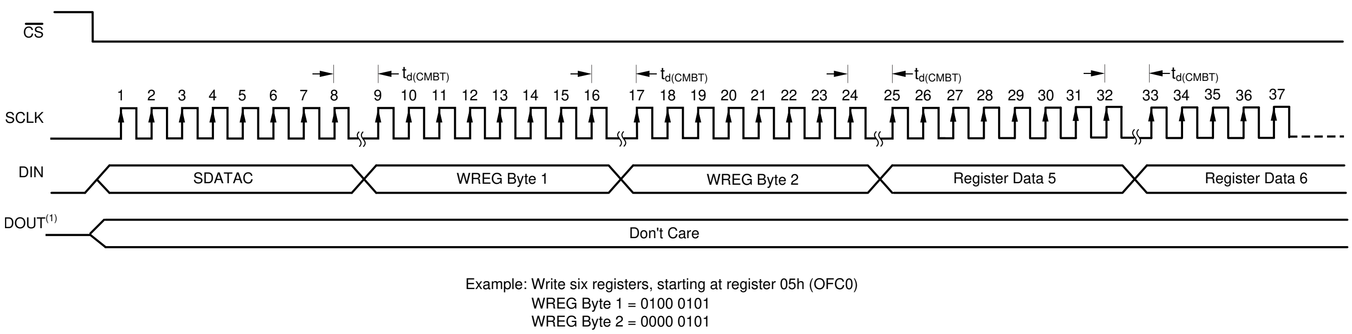
The WREG command writes a single register byte or writes multiple register bytes. The command consists of a two-byte argument followed by the register data to write. The first byte of the argument is the register starting address and the second byte specifies the number of registers to write minus one.

First command byte: 010r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers to write minus one.

Data bytes: one or more register data bytes, depending on the number of registers specified.

図 67 shows the WREG command. See the *Timing Requirements* table for the specification of the $t_{d(CMBT)}$ parameter.



(1) DOUT is in tri-state when CS is high.

図 67. Write Register Data

After writing to the ADC registers, the ADC synchronizes at the time of the write operation. ADC synchronization is re-established in pulse-sync mode by pulsing the SYNC pin at the desired time mark. In continuous-sinc mode, the previous synchronization is restored at any time by sending the STANDBY, WAKEUP command sequence; see the *Continuous-Sync Mode* section for details.

9.5.2.10 OFSCAL: Offset Calibration Command

The OFSCAL command performs an offset calibration. The inputs to the system (or ADC) must be zeroed and allowed to stabilize before sending this command. The offset calibration register is updated after this operation; see the *Calibration Command* section for more details.

9.5.2.11 GANCAL: Gain Calibration Command

The GANCAL command performs a gain calibration. The inputs to the system (or ADC) is a full-scale, DC calibration voltage. The gain calibration register is updated after the operation completes; see the *Calibration Command* section for more details.

9.6 Register Map

Collectively, the registers contain all the information needed to configure the device (such as data rate, filter mode, calibration, and so on). The registers are accessed by the read and write register commands (RREG and WREG, respectively). The registers are accessed either individually, or as a block by sending or receiving consecutive register data bytes. After the register write operation is completed, the conversion cycle restarts. Restart results in loss of the previous synchronization. Re-synchronize after writing the device registers; see the *Synchronization* section for details. 表 20 lists the ADS1287 registers.

表 20. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID/CFG	X0h	ID[3:0]				MODE[2:1](1)		OFFSET	RESERVED
01h	CONFIG0	52h	SYNC	MODE[0](1)	DR[2:0]			PHASE	FILTR[1:0]	
02h	CONFIG1	08h	BIAS(2)	RESERVED	MUX[1:0]		CHOP	GAIN[2:0]		
03h	HPF0	32h	HPF[7:0]							
04h	HPF1	03h	HPF[15:8]							
05h	OFC0	00h	OFC[7:0]							
06h	OFC1	00h	OFC[15:8]							
07h	OFC2	00h	OFC[23:16]							
08h	FSC0	00h	FSC[7:0]							
09h	FSC1	00h	FSC[15:8]							
0Ah	FSC2	40h	FSC[23:16]							

(1) The MODE[2:1] and MODE[0] bits must be set to all 1s or all 0s; see the *Operational Mode* section.
(2) The BIAS bit must be written to 1 after power-on or after reset.

9.6.1 Register Descriptions

表 21 lists the register access types for the ADS1287 registers.

表 21. ADS1287 Access Type Codes

Access Type	Code	Description
R	R	Read
R-W	R/W	Read or write
W	W	Write
-*n*		Value after reset or the default value

9.6.1.1 ID/CFG: ID, Configuration Register (address = 00h) [reset = x0h]

図 68. ID/CFG Register

7	6	5	4	3	2	1	0
ID[3:0]				MODE[2:1]		OFFSET	RESERVED
R-x				R/W-0h		R/W-0h	R/W-0h

表 22. ID/CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	ID[3:0]	R	---	**Factory-programmed identification bits (read-only).** The ID bits are subject to change without notification.
3:2	MODE[2:1]	R/W	0h	**Operating mode.** These bits must be set the same as the MODE[0] bit; see the CONFIG0 register. 00: Low-power mode 01: Reserved 10: Reserved 11: High-resolution mode
1	OFFSET	R/W	0h	**50-mV offset option.** See the *Offset* section. 0: Offset disabled (default) 1: Offset enabled
0	RESERVED	R/W	0h	**Reserved.** Always write 0.

9.6.1.2 CONFIG0: Configuration Register 0 (address = 01h) [reset = 52h]

図 69. CONFIG0 Register

7	6	5	4	3	2	1	0
SYNC	MODE[0]	DR[2:0]			PHASE	FILTR[1:0]	
R/W-0h	R/W-1h	R/W-2h			R/W-0h	R/W-2h	

表 23. CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC	R/W	0h	**Synchronization mode configuration bit.** 0: Pulse-sync mode (default) 1: Continuous-sync mode
6	MODE[0]	R/W	1h	**Operating mode bit.** This bit must be set in coordination with MODE2 and MODE1 bits; see 表 22. 0: Low-power mode 1: High-resolution mode
5:3	DR[2:0]	R/W	2h	**Data rate bits.** 000: 62.5 SPS 001: 125 SPS 010: 250 SPS (default) 011: 500 SPS 100: 1000 SPS
2	PHASE	R/W	0h	**FIR phase response bit.** 0: Linear phase (default) 1: Minimum phase
1:0	FILTR[1:0]	R/W	2h	**Digital filter configuration bits.** 00: Reserved 01: LPF sinc filter only 10: LPF sinc + LPF FIR filter (default) 11: LPF sinc + LPF FIR + HPF filter

9.6.1.3 CONFIG1: Configuration Register 1 (address = 02h) [reset = 08h]

図 70. CONFIG1 Register

7	6	5	4	3	2	1	0
BIAS	RESERVED	MUX[1:0]		CHOP	PGA[2:0]		
R/W-0h	R/W-0h	R/W-0h		R/W-1h	R/W-0h		

表 24. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIAS	R/W	0h	**ADC bias.** Always write 1 to this bit. 0: Bias disabled (default) 1: Bias enabled (always write 1)
6	RESERVED	R/W	0h	**Reserved.** Always write 0.
5:4	MUX[1:0]	R/W	0h	**Input MUX select bits.** 00: External input (default) 01: Reserved 10: Internal input short connection to V_{COM} 11: Reserved
3	CHOP	R/W	1h	**Chop enable bit.** See the *Chop Mode* section. 0: Chop disabled 1: Chop enabled (default)
2:0	PGA[2:0]	R/W	0h	**PGA gain select bits.** 000: Gain = 1 V/V (default) 001: Gain = 2 V/V 010: Gain = 4 V/V 011: Gain = 8 V/V 100: Gain = 16 V/V 101–111: Reserved

9.6.1.4 High-Pass Filter Corner Frequency (HPFx) Registers (address = 03h, 04h) [reset = 32h, 03h]

図 71. HPF0 Register

7	6	5	4	3	2	1	0
HPF[7:0]							
R/W-32h							

図 72. HPF1 Register

7	6	5	4	3	2	1	0
HPF[15:8]							
R/W-03h							

表 25. HPF0, HPF1 Registers Field Description

Bit	Field	Type	Reset	Description
7:0	HPF[15:0]	R/W	0332h	**High-pass filter corner frequency registers**. These two registers program the corner frequency of the high-pass filter; see the *HPF Stage* section for details.

9.6.1.5 Offset Calibration (OFCx) Registers (address = 05h, 06h, 07h) [reset = 00h, 00h, 00h]

図 73. OFC0 Register

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							

図 74. OFC1 Register

7	6	5	4	3	2	1	0
OFC[15:8]							
R/W-00h							

図 75. OFC2 Register

7	6	5	4	3	2	1	0
OFC[23:16]							
R/W-00h							

表 26. OFC0, OFC1, OFC2 Registers Field Description

Bit	Field	Type	Reset	Description
7:0	OFC[23:0]	R/W	000000h	**Offset calibration registers.** These three registers are the 24-bit offset calibration word. The offset calibration is in two's complement format. The ADC subtracts the offset value from the conversion result prior to the full-scale operation.

9.6.1.6 Full-Scale Calibration (FSCx) Registers (address = 08h, 09h, 0Ah) [reset = 00h, 00h, 40h]

図 76. FSC0 Register

7	6	5	4	3	2	1	0
FSCAL[7:0]							
R/W-00h							

図 77. FSC1 Register

7	6	5	4	3	2	1	0
FSCAL[15:8]							
R/W-00h							

図 78. FSC2 Register

7	6	5	4	3	2	1	0
FSCAL[23:16]							
R/W-40h							

表 27. FSC0, FSC1, FSC2 Registers Field Description

Bit	Field	Type	Reset	Description
7:0	FSCAL[23:0]	R/W	400000h	**Full-scale calibration registers.** These three registers are the 24-bit, full-scale calibration word. The full-scale calibration is in straight binary format. The ADC divides the register value by 400000h, then multiplies the conversion data. The scaling operation occurs after the offset operation.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS1287 is a high-resolution ADC optimized for low-power operation in seismic data acquisition equipment. Optimum performance requires special attention to the support circuitry and printed-circuit board (PCB) layout. As much as possible, locate noisy digital components (such as microcontrollers, oscillators, and so forth) in a PCB area away from the ADC and analog front-end components. Locating the digital components close to the power-entry point keeps the digital current return path short and separated from sensitive analog components.

10.2 Typical Applications

10.2.1 Geophone Application

図 79 illustrates a typical geophone application circuit. The application shows the ADC operating on a bipolar ±2.5-V analog supply voltage. The power-supply voltages are provided by low-dropout (LDO) regulators to provide well-regulated, low-noise supply voltages to the ADC. The ADC also operates using with a unipolar 5-V analog supply voltage. The 6-V zener diode between AVDD and AVSS clamps the ADC supply voltage if the inputs are driven when the ADC supply voltage is off.

Resistors R_1 and R_2 bias the floating geophone to mid-supply. The resistors also provide a return path for the ADC input current. To prevent pickup of PCB ground-related noise, connect the resistors together first, then connect to ground. For unipolar-supply operation, make this connection to a low-impedance 2.5-V voltage.

The geophone signal is filtered both differentially, by components C_3 and R_3 through R_6, and common-mode filtered by components C_1, C_2 and R_3, R_4. The differential filter removes normal-mode noise. The common-mode filters remove noise that is common to both inputs. The differential filter high-cut frequency is 10 times lower to minimize the effects of component mismatch of the common-mode filter that otherwise can lead to degraded differential-filter performance. Adjust the filter components according to the application requirements. The protection diodes protect the ADC inputs from system-level ESD transients and signal overrange events.

A low-noise, low-power, 2.5-V voltage reference drives the ADC reference input. The voltage reference ground terminal is connected to –2.5 V. R_9 and C_5 form an optional 2-Hz noise filter to reduce voltage reference noise. Capacitor C_6 filters the reference sampling glitches. Place the capacitor directly at the ADC pins. Multiple ADCs can share a single reference but place a 0.1-µF capacitor at each ADC reference input.

Capacitor C_4 (10 nF), located at the CAPP and CAPN pins, filters modulator sampling glitches. The capacitor also provides a antialiasing filter with a high cutoff corner frequency of approximately 9.5 kHz. Resistors R_7 and R_8 provide an offset voltage to the modulator for idle tone reduction when operating in high-resolution mode. Use the internal offset in low-power mode operation. The resistors are not needed in this case.

Typical Applications (continued)

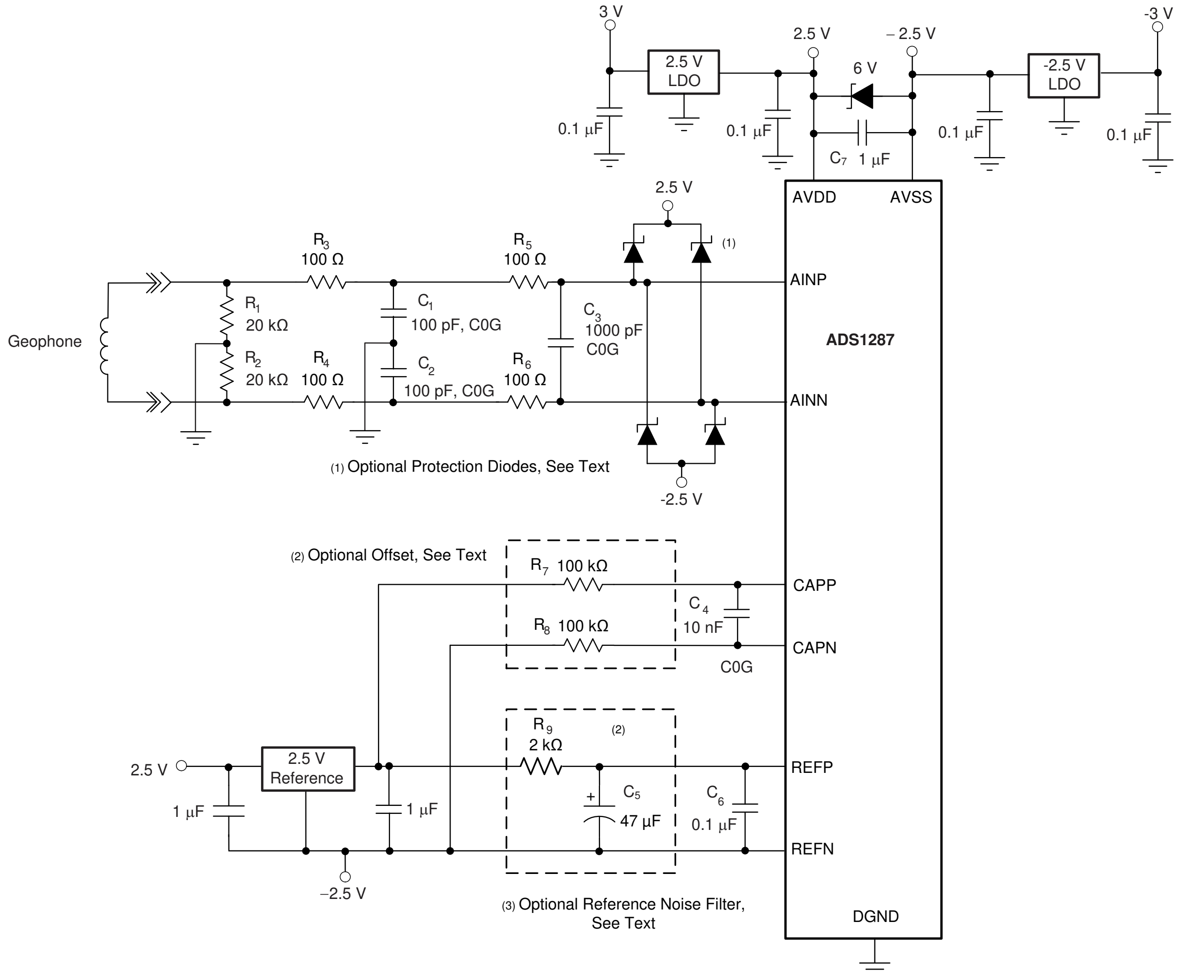


図 79. Geophone Analog Interface

Typical Applications (continued)

10.2.2 Digital Interface

図 80 shows the digital connections to a controller, such as a field programmable gate array (FPGA) or microcontroller. Place the digital bypass capacitors on DVDD and the LDO output (BYPAS) close to the device pins and directly to the ground plane. Connections to the RESET and PWDN pins are optional. If not used, tie the inputs to DVDD. Avoid ringing on the digital inputs of the ADC. For long PCB traces, use 47-Ω series termination resistors to help reduce ringing by controlling the trace impedance. Place the resistors at the source (output driver).

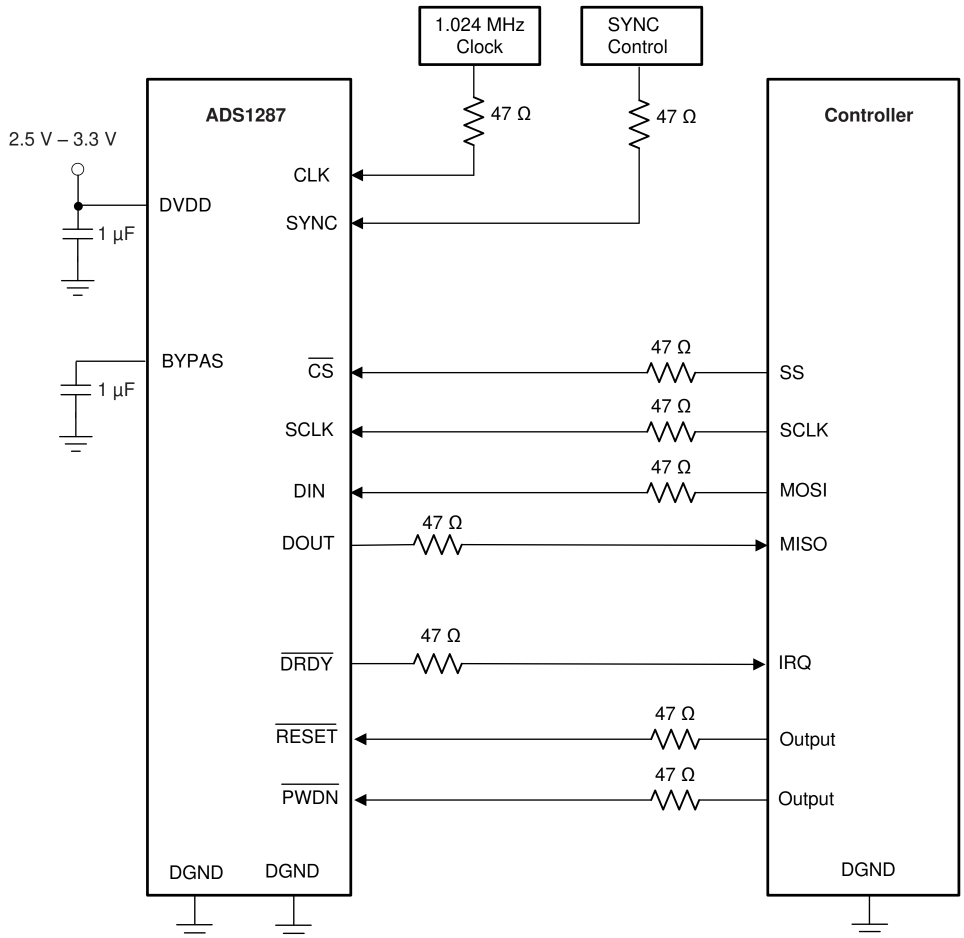


図 80. Digital Connections

10.3 Initialization Set Up

After reset or power-on, configure the ADC using the following procedure:

1. Reset the serial interface. Before beginning communication to the ADC, the serial interface may have to be recovered (undefined I/O power-up sequencing can cause a false SCLK to occur). To reset the interface, toggle the $\overline{CS}$ pin high to low, or toggle the $\overline{RESET}$ pin.
2. Configure the registers. For proper operation, the MODE[2:0] bits and the BIAS bit must be programmed appropriately; see the MODE[2:0] bits in 表 20.
3. Verify register data. For verification of device communications, read back the register data.
4. Set the data mode. After register configuration, configure the device for read-data-continuous mode by sending the RDATAC command.
5. Synchronize readings. After power-on, the ADCs are unsynchronized and conversions freely run. To synchronize the conversions in pulse-sync mode, take SYNC low and then high. In continuous-sync mode, apply the synchronizing clock to the SYNC pin under the operating constraint that the SYNC input period is equal to integer multiples of the ADC conversion period.
6. Read data. In read-data-continuous mode, the data are read after $\overline{DRDY}$ falls by shifting the data out directly (no command). If the stop-read-data-continuous mode is selected, read the data by sending the RDATA command. The RDATA command must be sent in this mode for each conversion result.

11 Power Supply Recommendations

The ADC has three power supplies: AVDD, AVSS, and DVDD.

11.1 Analog Power Supplies

The analog power supply can be either bipolar ±2.5 V (AVDD and AVSS) or unipolar 5 V (AVDD) with AVSS tied to ground.

11.2 Digital Power Supply

The DVDD supply range is 2.25 V to 3.6 V. DVDD is the I/O voltage and is also sub-regulated by the internal 1.8-V LDO to power the digital circuitry. The LDO output is the BYPAS pin. Connect a 1-µF capacitor from BYPAS to DGND and a 1-µF capacitor from DVDD to DGND. Make no other connection or load to the BYPAS pin.

11.3 Power-Supply Sequence

The power supplies can be sequenced in any order. At power-on, the difference of (AVDD – AVSS) and DVDD are monitored by internal comparators that are logical AND'd to produce the internal reset signal. After the power supplies have crossed the respective thresholds, 2^{16} f_{CLK} cycles are counted before the ADC exits the reset state and is ready for communication. New conversion data are available; see 図 7 and the *Switching Characteristics* table.

12 Layout

12.1 Layout Guidelines

In most cases, a single continuous ground plane connecting the analog and digital components is preferred. Use wide, low-impedance PCB traces or dedicated layers for the power-supply connections because the analog supply current is partially modulated by the input signal. Also use wide PCB traces or dedicated layers for REFP and REFN. If REFN and AVSS are connected together, use a Kelvin connection at the voltage regulator ground terminal. These practices help maintain good THD performance and minimal crosstalk errors when multiple ADCs are used.

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.5 Glossary

SLYZ022 — *TI Glossary*.

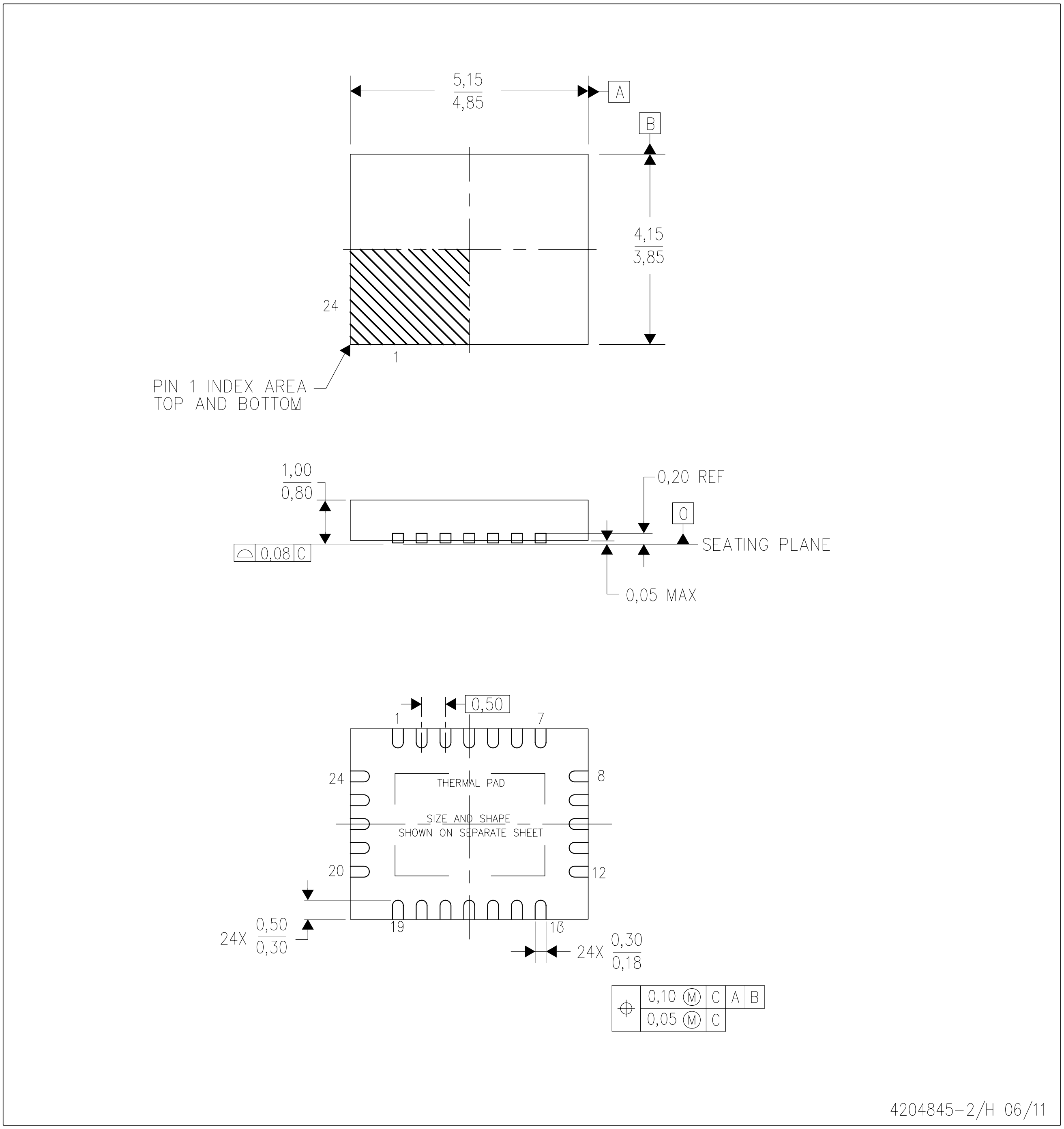
This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

MECHANICAL DATA

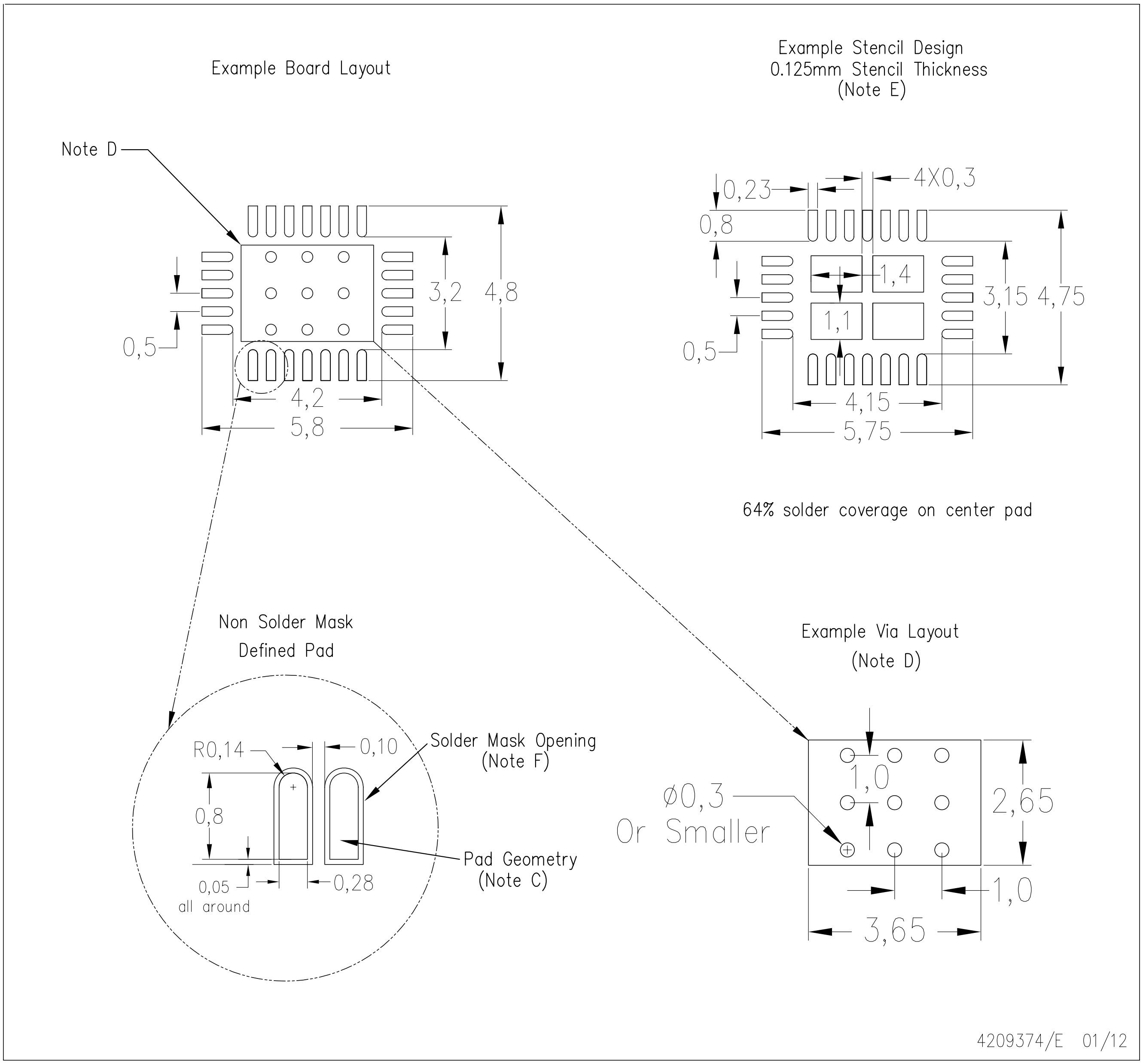
RHF (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

LAND PATTERN DATA

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

THERMAL PAD MECHANICAL DATA

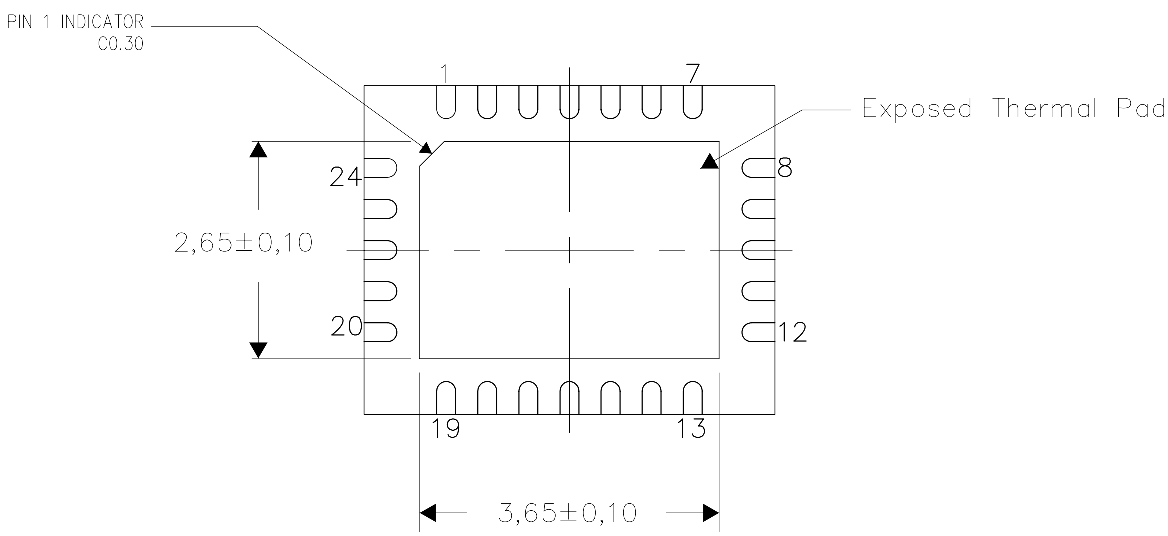
RHF (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

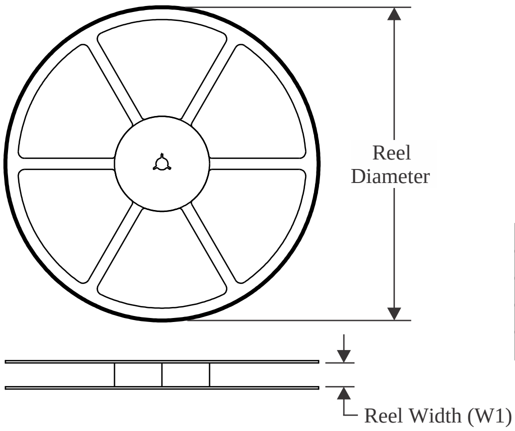
Exposed Thermal Pad Dimensions

4206360-3/J 01/12

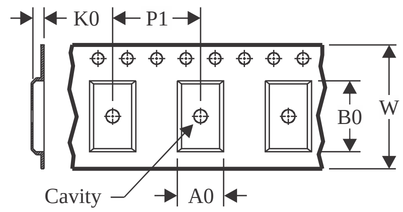
NOTE: All linear dimensions are in millimeters

TAPE AND REEL INFORMATION

REEL DIMENSIONS

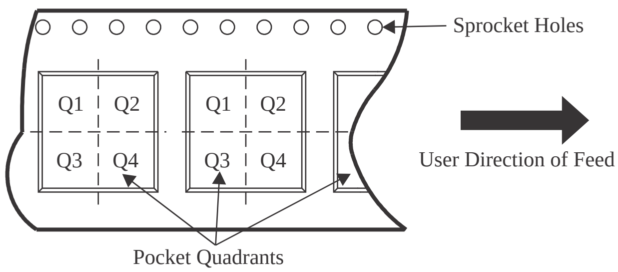


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

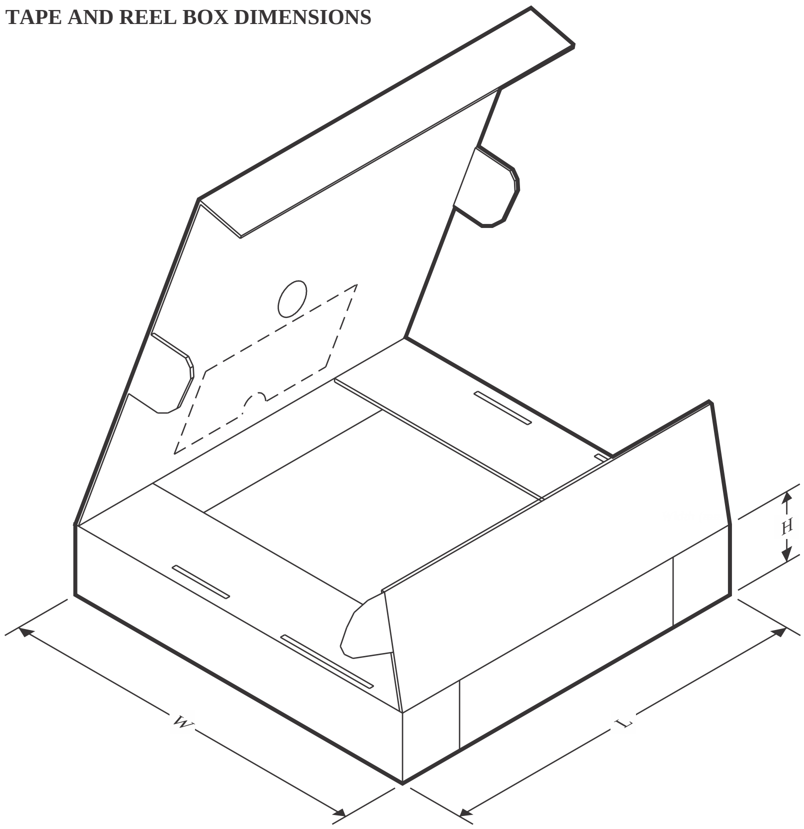
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1287IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1287IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1287IRHFR	VQFN	RHF	24	3000	346.0	346.0	33.0
ADS1287IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0

重要なお知らせと免責事項

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