ADS114S0x低消費電力、低ノイズ、高度統合、6および12チャネル、4kSPS、16ビット、デルタ-シグマADC、PGAおよび基準電圧搭載

1 特長

- 低消費電力: 280µA
- プログラマブル・ゲイン: 1～128
- プログラマブル・データ・レート: 2.5SPS～4kSPS
- 低レイテンシ・デジタル・フィルタによる50Hzおよび60Hzの同時リジェクション(20 SPS以下)
- 12個(ADS114S08)または 6個(ADS114S06)の個別選択可能な入力を持つアナログ・マルチプレクサ
- センサ励起のためのデュアル・マッチのプログラム可能電流源: 10µA～2000µA
- 内部リファレンス: 2.5V、最大ドリフト10ppm/℃
- 内部オシレータ: 4.096MHz、1.5%精度
- 内部温度センサ
- 機能拡張された障害検出回路
- セルフ・オフセットおよびシステム較正
- 4つの汎用I/O
- オプションCRC付きSPI互換インターフェイス
- アナログ電源: ユニポーラ(2.7V～5.25V)またはバイポーラ(±2.5V)
- デジタル電源: 2.7V～3.6V
- 動作温度範囲: -50℃～+125℃

2 アプリケーション

- センサ・トランスデューサおよびトランスミッタ: 温度、圧力、歪み、フロー
- PLCおよびDCSアナログ入力モジュール
- 温度コントローラ
- 人工気象室、産業用オーブン

3 概要

ADS114S06およびADS114S08は高精度の16ビット、デルタ-シグマ(ΔΣ)、アナログ/デジタル・コンバータ(ADC)です。低い消費電力と多くの内蔵機能で、小信号を測定するセンサ・アプリケーションのシステム・コストと部品点数を削減できます。

これらのADCは、ノイズの多い産業用環境で使用できるよう、50Hzまたは60Hzのリジェクションと低レイテンシの変換結果を実現する、構成可能なデジタル・フィルタを備えています。低ノイズのPGA (プログラマブル・ゲイン・アンプ)は、1～128のゲインを提供し、抵抗ブリッジや熱電対アプリケーション用に低レベルの信号を増幅します。また、プリント回路基板(PCB)の面積を削減する低ドリフトの2.5Vリファレンスを備えています。さらに、2つのプログラム可能な励起電流源(IDAC)により、高精度なRTDバイアスを簡単に実現できます。

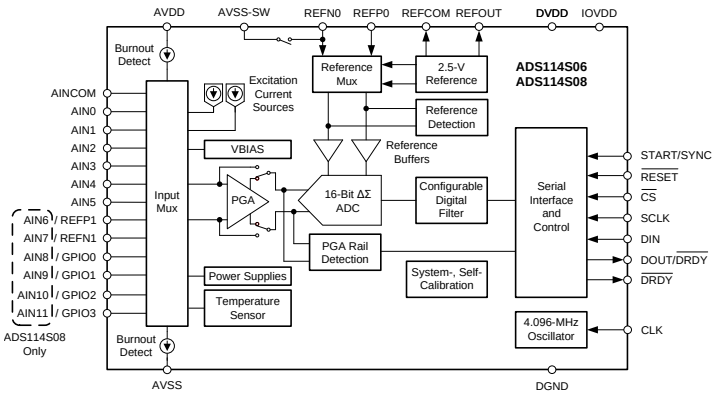
入力マルチプレクサは、ADS114S08では12個、ADS114S06では6個の入力をサポートしており、これらの入力は自由に組み合わせてADCに接続できるため、柔軟な設計が可能です。また、センサの過熱故障検出、熱電対用電圧バイアス、システム・モニタリング、4つの汎用I/Oを備えています。

リードレスVQFN-32またはTQFP-32パッケージで供給されます。

製品情報

発注型番	パッケージ (ピン)	本体サイズ
ADS114S0x	TQFP (32)	5.0mm×5.0mm
	VQFN (32)	5.0mm×5.0mm

機能ブロック図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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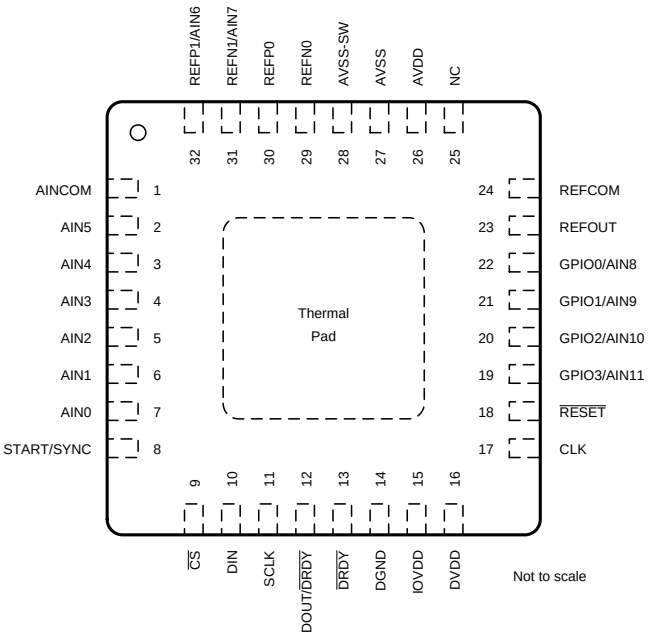
5 Device Family Comparison Table

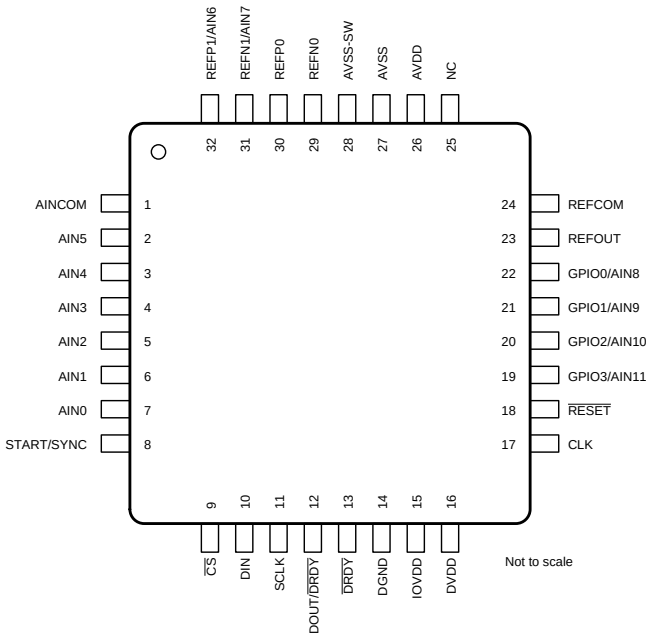
PRODUCT	RESOLUTION (Bits)	NUMBER OF INPUTS
ADS124S08	24	12 analog inputs
ADS124S06	24	6 analog inputs
ADS114S08	16	12 analog inputs
ADS114S06	16	6 analog inputs

6 Pin Configuration and Functions

RHB Package
32-Pin VQFN
Top View



PBS Package
32-Pin TQFP
Top View



NOTE: The analog input functions (AIN6–AIN11) are not available on pins 19 to 22, 31, and 32 for the ADS114S06.

Pin Functions

PIN		FUNCTION	DESCRIPTION(1)
NO.	NAME		
1	AINCOM	Analog input	Common analog input for single-ended measurements
2	AIN5	Analog input	Analog input 5
3	AIN4	Analog input	Analog input 4
4	AIN3	Analog input	Analog input 3
5	AIN2	Analog input	Analog input 2
6	AIN1	Analog input	Analog input 1
7	AIN0	Analog input	Analog input 0
8	START/SYNC	Digital input	Start conversion
9	$\overline{CS}$	Digital input	Chip select; active low
10	DIN	Digital input	Serial data input
11	SCLK	Digital input	Serial clock input
12	DOUT/$\overline{DRDY}$	Digital output	Serial data output combined with data ready; active low
13	$\overline{DRDY}$	Digital output	Data ready; active low
14	DGND	Digital ground	Digital ground
15	IOVDD	Digital supply	Digital I/O power supply. In case IOVDD is not tied to DVDD, connect a 100-nF (or larger) capacitor to DGND.
16	DVDD	Digital supply	Digital core power supply. Connect a 100-nF (or larger) capacitor to DGND.
17	CLK	Digital input	External clock input. Connect to DGND to use the internal oscillator.
18	$\overline{RESET}$	Digital input	Reset; active low
19	GPIO3/AIN11	Analog input/output	General-purpose I/O(2); analog input 11 (ADS114S08 only)
20	GPIO2/AIN10	Analog input/output	General-purpose I/O(2); analog input 10 (ADS114S08 only)
21	GPIO1/AIN9	Analog input/output	General-purpose I/O(2); analog input 9 (ADS114S08 only)
22	GPIO0/AIN8	Analog input/output	General-purpose I/O(2); analog input 8 (ADS114S08 only)
23	REFOUT	Analog output	Positive voltage reference output. Connect a 1-µF to 47-µF capacitor to REFCOM if the internal voltage reference is enabled.
24	REFCOM	Analog output	Negative voltage reference output. Connect to AVSS.
25	NC	—	Leave unconnected or connect to AVSS
26	AVDD	Analog supply	Positive analog power supply. Connect a 330-nF (or larger) capacitor to AVSS.
27	AVSS	Analog supply	Negative analog power supply
28	AVSS-SW	Analog supply	Negative analog power supply; low-side switch. Connect to AVSS.
29	REFN0	Analog input	Negative external reference input 0
30	REFP0	Analog input	Positive external reference input 0
31	REFN1/AIN7	Analog input	Negative external reference input 1; analog input 7 (ADS114S08 only)
32	REFP1/AIN6	Analog input	Positive external reference input 1; analog input 6 (ADS114S08 only)
Pad	Thermal pad	—	RHB package only. Thermal power pad. Connect to AVSS.

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.
(2) General-purpose inputs and outputs use logic levels based on the analog supply.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AVSS	–0.3	5.5	V
	AVSS to DGND	–2.8	0.3	
	DVDD to DGND	–0.3	3.9	
	IOVDD to DGND	–0.3	5.5	
Analog input voltage	AINx, GPIOx, REFPx, REFNx, REFCOM	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, START, $\overline{RESET}$, CLK	DGND – 0.3	IOVDD + 0.3	V
Input current	Continuous, AVSS-SW, REFN0, REFOUT	–100	100	mA
	Continuous, all other pins except power-supply pins	–10	10	
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AVSS	2.7		5.25	V
		AVSS to DGND	–2.625	0	0.05	
		AVDD to DGND	1.5		5.25	
	Digital core power supply	DVDD to DGND	2.7		3.6	V
	Digital IO power supply	IOVDD to DGND	DVDD		5.25	V
ANALOG INPUTS(1)						
$V_{(AINx)}$	Absolute input voltage(2)	PGA bypassed	AVSS – 0.05		AVDD + 0.05	V
		PGA enabled, gain = 1 to 16	AVSS + 0.15 + $\lvert V_{INMAX}\rvert \cdot$(Gain – 1) / 2		AVDD – 0.15 – $\lvert V_{INMAX}\rvert \cdot$(Gain –1) / 2	
		PGA enabled, gain = 32 to 128	AVSS + 0.15 + 15.5·$\lvert V_{INMAX}\rvert$		AVDD – 0.15 – 15.5·$\lvert V_{INMAX}\rvert$	
V_{IN}	Differential input voltage	$V_{IN} = V_{AINP} – V_{AINN}$	$–V_{REF}$ / Gain		V_{REF} / Gain	V
VOLTAGE REFERENCE INPUTS(3)						
V_{REF}	Differential reference input voltage	$V_{REF} = V_{(REFPx)} – V_{(REFNx)}$	0.5		AVDD – AVSS	V
$V_{(REFNx)}$	Absolute negative reference voltage	Negative reference buffer disabled	AVSS – 0.05		$V_{(REFPx)}$ – 0.5	V
		Negative reference buffer enabled	AVSS		$V_{(REFPx)}$ – 0.5	V
$V_{(REFPx)}$	Absolute positive reference voltage	Positive reference buffer disabled	$V_{(REFNx)}$ + 0.5		AVDD + 0.05	V
		Positive reference buffer enabled	$V_{(REFNx)}$ + 0.5		AVDD	V
EXTERNAL CLOCK SOURCE(4)						
f_{CLK}	External clock frequency		2	4.096	4.5	MHz
	Duty cycle		40%	50%	60%	
GENERAL-PURPOSE INPUTS (GPIOs)						
	Input voltage		AVSS – 0.05		AVDD + 0.05	V
DIGITAL INPUTS (Other than GPIOs)						
	Input voltage		DGND		IOVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–50		125	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA. Any of the available analog inputs (AINx) can be selected as either AIN_P or AIN_N by the input multiplexer.
(2) V_{INMAX} denotes the maximum differential input voltage, V_{IN}, that is expected in the application. $\lvert V_{INMAX}\rvert$ can be smaller than V_{REF} / Gain.
(3) REFPx and REFNx denote one of the two available external differential reference input pairs.
(4) An external clock is not required when the internal oscillator is used.

7.4 Thermal Information

THERMAL METRIC(1)		ADS114S06, ADS114S08		UNIT
		VQFN (RHB)	TQFP (PBS)	
		32 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.2	75.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	17.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	28.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	28.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –50°C to +125°C; Typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.7 V to 5.25 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, all gains, internal reference, internal oscillator, all data rates, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	PGA bypassed, AVSS + 0.1 V ≤ $V_{(AINx)}$ ≤ AVDD – 0.1 V		0.5		nA
		PGA enabled, all gains, $V_{(AINx)MIN}$ ≤ $V_{(AINx)}$ ≤ $V_{(AINx)MAX}$	–2	0.1	2	
	Absolute input current drift	PGA bypassed, AVSS + 0.1 V ≤ $V_{(AINx)}$ ≤ AVDD – 0.1 V		2		pA/°C
		PGA enabled, all gains, $V_{(AINx)MIN}$ ≤ $V_{(AINx)}$ ≤ $V_{(AINx)MAX}$		2		
	Differential input current	PGA bypassed, V_{CM} = AVDD / 2, $-V_{REF}$ ≤ V_{IN} ≤ V_{REF}		1		nA/V
		PGA enabled, all gains, V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain	–1	0.02	1	nA
	Differential input current drift	PGA bypassed, V_{CM} = AVDD / 2, $-V_{REF}$ ≤ V_{IN} ≤ V_{REF}		3		pA/°C
		PGA enabled, all gains, V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		1		
PGA						
	Gain settings			1, 2, 4, 8, 16, 32, 64, 128		
	Startup time	Enabling the PGA in conversion mode		190		µs
SYSTEM PERFORMANCE						
	Resolution (no missing codes)		16			Bits
DR	Data rate			2.5, 5, 10, 16.6, 20, 50, 60, 100, 200, 400, 800, 1000, 2000, 4000		SPS
INL	Integral nonlinearity (best fit)	PGA bypassed, V_{CM} = AVDD / 2		1	10	ppm_{FSR}
		PGA enabled, gain = 1 to 8, V_{CM} = AVDD / 2		2	15	
		PGA enabled, gain = 16 to 128, V_{CM} = AVDD / 2, T_A = –40°C to +85°C		3	15	
V_{IO}	Input offset voltage	T_A = 25°C, PGA bypassed	–120	20	120	µV
		T_A = 25°C, PGA enabled, gain = 1 to 8	–120 / Gain	20 / Gain	120 / Gain	
		T_A = 25°C, PGA enabled, gain = 16 to 128	–15	2	15	
		T_A = 25°C, PGA bypassed, after internal offset calibration	On the order of $noise_{PP}$ at the set DR and gain			
		T_A = 25°C, PGA enabled, gain = 1 to 128, after internal offset calibration	On the order of $noise_{PP}$ at the set DR and gain			
		T_A = 25°C, PGA bypassed, global chop enabled	–2	0.2	2	
		T_A = 25°C, PGA enabled, gain = 1 to 128, global chop enabled	–2	0.2	2	
	Offset drift	T_A = –40°C to +85°C, PGA bypassed	–75	10	75	nV/°C
		T_A = –40°C to +85°C, PGA enabled, gain = 1 to 128	–100	15	100	
		PGA bypassed	–75	10	75	
		PGA enabled, gain = 1 to 8	–200	15	200	
		PGA enabled, gain = 16 to 128	–150	15	150	
		PGA bypassed, global chop enabled	–10	2	10	
		PGA enabled, gain = 1 to 128, global chop enabled	–10	2	10	

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –50°C to +125°C; Typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.7 V to 5.25 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, all gains, internal reference, internal oscillator, all data rates, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE (continued)						
	Gain error(1)	T_A = 25°C, PGA bypassed		40	120	ppm
		T_A = 25°C, PGA enabled, gain = 1 to 32		40	120	
		T_A = 25°C, PGA enabled, gain = 64 and 128		40	200	
	Gain drift(1)	T_A = –40°C to +85°C, PGA bypassed		0.5	1	ppm/°C
		T_A = –40°C to +85°C, PGA enabled, gain = 1 to 128		0.5	2	
		PGA bypassed		0.5	1	
		PGA enabled, gain = 1 to 128		1	4	
	Noise (input-referred)		See the *Noise Performance* section			
NMRR	Normal-mode rejection ratio(2)	f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 10 SPS, $sinc^3$ filter	88			dB
		f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 10 SPS, $sinc^3$ filter, external f_{CLK} = 4.096 MHz	102			
		f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 20 SPS, low-latency filter	79			
		f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 20 SPS, low-latency filter, external f_{CLK} = 4.096 MHz	95			
		f_{IN} = 50 Hz (±1 Hz), DR = 50 SPS, $sinc^3$ filter	87			
		f_{IN} = 50 Hz (±1 Hz), DR = 50 SPS, $sinc^3$ filter, external f_{CLK} = 4.096 MHz	101			
		f_{IN} = 60 Hz (±1 Hz), DR = 60 SPS, $sinc^3$ filter	89			
		f_{IN} = 60 Hz (±1 Hz), DR = 60 SPS, $sinc^3$ filter, external f_{CLK} = 4.096 MHz	105			
CMRR	Common-mode rejection ratio	At dc	110	120		dB
		f_{CM} = 50 Hz or 60 Hz (±1 Hz), DR = 2.5 SPS to 10 SPS, $sinc^3$ filter	120	130		
		f_{CM} = 50 Hz or 60 Hz (±1 Hz), DR = 2.5 SPS, 5 SPS, 10 SPS, 20 SPS, low-latency filter	115	125		
PSRR	Power-supply rejection ratio	AVDD at dc	90	105		dB
		AVDD at 50 Hz or 60 Hz	100	115		
		DVDD at dc	100	115		

(1) Excluding error of voltage reference.
(2) See the *50-Hz and 60-Hz Line Cycle Rejection* section for more information.

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –50°C to +125°C; Typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.7 V to 5.25 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, all gains, internal reference, internal oscillator, all data rates, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE INPUTS						
	Absolute input current	Reference buffers disabled, external V_{REF} = 2.5 V, REFP1/REFN1 inputs	-6	4	6	µA/V
		Reference buffers enabled, external V_{REF} = 2.5 V, REFP1/REFN1 inputs	–15	5	15	nA
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Output voltage			2.5		V
	Accuracy	T_A = 25°C, TQFP package	–0.05%	±0.01%	0.05%	
		T_A = 25°C, VQFN package	–0.1%	±0.01%	0.1%	
	Temperature drift	T_A = –40°C to +85°C		2.5	8	ppm/°C
		T_A = –50°C to +125°C		3	10	
	Output current	AVDD = 2.7 V to 3.3 V, sink and source	–5		5	mA
		AVDD = 3.3 V to 5.25 V, sink and source	–10		10	
	Short-circuit current limit	Sink and source		70	100	mA
PSRR	Power-supply rejection ratio	AVDD at dc		85		dB
	Load regulation	AVDD = 2.7 V to 3.3 V, load current = –5 mA to 5 mA		8		µV/mA
		AVDD = 3.3 V to 5.25 V, load current = –10 mA to 10 mA		8		
	Startup time	1-µF capacitor on REFOUT, 0.001% settling		5.9		ms
	Capacitive load stability	Capacitor on REFOUT	1		47	µF
	Reference noise	f = 0.1 Hz to 10 Hz, 1-µF capacitor on REFOUT		9		μV_{PP}
INTERNAL OSCILLATOR						
f_{CLK}	Frequency			4.096		MHz
	Accuracy		–1.5%		1.5%	
EXCITATION CURRENT SOURCES (IDACS)						
	Current settings			10, 50, 100, 250, 500, 750, 1000, 1500, 2000		µA
	Compliance voltage(3)	10 µA to 750 µA, 0.1% deviation	AVSS		AVDD – 0.4	V
		1 mA to 2 mA, 0.1% deviation	AVSS		AVDD – 0.6	
	Accuracy (each IDAC)	T_A = 25°C, 10 µA to 100 µA	–5%	±0.7%	5%	
		T_A = 25°C, 250 µA to 2 mA	–3%	±0.5%	3%	
	Current mismatch between IDACs	T_A = 25°C, 10 µA to 100 µA		0.15%	0.8%	
		T_A = 25°C, 250 µA to 750 µA		0.10%	0.6%	
		T_A = 25°C, 1 mA to 2 mA		0.07%	0.4%	
	Temperature drift (each IDAC)	10 µA to 750 µA		20	120	ppm/°C
		1 mA to 2 mA		10	80	
	Temperature drift matching between IDACs	10 µA to 100 µA		3	25	ppm/°C
		250 µA to 2 mA		2	15	
	Startup time	With internal reference already settled. From end of WREG command to current flowing out of pin.		22		µs

(3) The IDAC current does not change by more than 0.1% from the nominal value when staying within the specified compliance voltage.

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –50°C to +125°C; Typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.7 V to 5.25 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, all gains, internal reference, internal oscillator, all data rates, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS VOLTAGE						
V_{BIAS}	Output voltage settings			(AVDD + AVSS) / 2, (AVDD + AVSS) / 12		V
	Output impedance			350		Ω
	Startup time	Combined capacitive load on all selected analog inputs C_{LOAD} = 1 µF, 0.1% settling		2.8		ms
BURNOUT CURRENT SOURCES (BOCS)						
	Current settings			0.2, 1, 10		µA
	Accuracy	0.2 µA, sinking or sourcing		±8%		
		1 µA, sinking or sourcing		±4%		
		10 µA, sinking or sourcing		±2%		
PGA RAIL DETECTION						
	Positive rail threshold	Referred to the output of the PGA		AVDD – 0.15		V
	Negative rail threshold	Referred to the output of the PGA		AVSS + 0.15		V
REFERENCE DETECTION						
	Threshold 1			0.3		V
	Threshold 2			1/3·(AVDD – AVSS)		V
	Threshold 2 accuracy		–3%	±1%	3%	
	Pull-together resistance			10		MΩ
SUPPLY VOLTAGE MONITORS						
	Accuracy	(AVDD – AVSS) / 4 monitor		±1%		
		DVDD / 4 monitor		±1%		
TEMPERATURE SENSOR						
	Output voltage	T_A = 25°C		129		mV
	Temperature coefficient			403		µV/°C
LOW-SIDE POWER SWITCH						
R_{ON}	On-resistance			1	3	Ω
	Current through switch				75	mA
GENERAL-PURPOSE INPUT/OUTPUTS (GPIOs)						
V_{IL}	Logic input level, low		AVSS – 0.05		0.3 AVDD	V
V_{IH}	Logic input level, high		0.7 AVDD		AVDD + 0.05	V
V_{OL}	Logic output level, low	I_{OL} = 1 mA	AVSS		0.2 AVDD	V
V_{OH}	Logic output level, high	I_{OH} = 1 mA	0.8 AVDD		AVDD	V
DIGITAL INPUT/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.3 IOVDD	V
V_{IH}	Logic input level, high		0.7 IOVDD		IOVDD	V
V_{OL}	Logic output level, low	I_{OL} = 1 mA	DGND		0.2 IOVDD	V
V_{OH}	Logic output level, high	I_{OH} = 1 mA	0.8 IOVDD		IOVDD	V
	Input current	DGND ≤ $V_{Digital\ Input}$ ≤ IOVDD	–1		1	µA

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –50°C to +125°C; Typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.7 V to 5.25 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, all gains, internal reference, internal oscillator, all data rates, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENT (AVDD = 3.3 V, External Reference, Internal Reference Disabled, Reference Buffers Disabled, IDACs Disabled, VBIAS Disabled, Flags Disabled, Internal Oscillator, All Data Rates, V_{IN} = 0 V)						
I_{AVDD}	Analog supply current	Power-down mode		0.1	1.5	µA
		Standby mode, PGA bypassed		70		
		Conversion mode, PGA bypassed		85		
		Conversion mode, PGA enabled, gain = 1, 2		120	135	
		Conversion mode, PGA enabled, gain = 4, 8		140	155	
		Conversion mode, PGA enabled, gain = 16, 32		165	180	
		Conversion mode, PGA enabled, gain = 64		200		
		Conversion mode, PGA enabled, gain = 128		250		
ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 3.3 V)						
I_{AVDD}	Analog supply current	Internal 2.5-V reference, no external load		185	280	µA
		Positive reference buffer		35	60	
		Negative reference buffer		25	40	
		VBIAS buffer, no external load		10		
		IDAC overhead, 10 µA to 250 µA		20	35	
		IDAC overhead, 500 µA to 750 µA		30		
		IDAC overhead, 1 mA		40		
		IDAC overhead, 1.5 mA		50		
		IDAC overhead, 2 mA		65		
		PGA rail detection and reference detection circuit		10		
DIGITAL SUPPLY CURRENT (DVDD = IOVDD = 3.3 V, All Data Rates, SPI Not Active)						
I_{DVDD} + I_{IOVDD}	Digital supply current	Power-down mode, internal oscillator		0.1		µA
		Standby mode, internal oscillator		185		
		Conversion mode, internal oscillator		225	300	
		Conversion mode, external f_{CLK} = 4.096 MHz		195		
POWER DISSIPATION (AVDD = DVDD = IOVDD = 3.3 V, Internal Reference Enabled, Reference Buffers Disabled, IDACs Disabled, VBIAS Disabled, Flags Disabled, Internal Oscillator, All Data Rates, V_{IN} = 0 V, SPI Not Active)						
P_D	Power dissipation	Conversion mode, PGA enabled, gain = 1		1.75		mW

7.6 Timing Characteristics

over operating ambient temperature range, DVDD = 2.7 V to 3.6 V, IOVDD = DVDD to 5.25 V, and DOUT/$\overline{\text{DRDY}}$ load = 20 pF || 100 kΩ to DGND (unless otherwise noted)

		MIN	MAX	UNIT(1)
SERIAL INTERFACE				
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{\text{CS}}$ falling edge	20		ns
$t_{d(SCCS)}$	Delay time, $\overline{\text{CS}}$ rising edge after final SCLK falling edge	20		ns
$t_{w(CSH)}$	Pulse duration, $\overline{\text{CS}}$ high	30		ns
$t_{c(SC)}$	SCLK period	100		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	40		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	40		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	15		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	20		ns
$t_{d(CMD)}$	Delay time, between bytes or commands	0		ns
$\overline{\text{RESET}}$ PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RESET}}$ low	4		t_{CLK}
$t_{d(RSSC)}$	Delay time, first SCLK rising edge after $\overline{\text{RESET}}$ rising edge (or 7th SCLK falling edge of RESET command)	4096		t_{CLK}
START/SYNC PIN				
$t_{w(STH)}$	Pulse duration, START/SYNC high	4		t_{CLK}
$t_{w(STL)}$	Pulse duration, START/SYNC low	4		t_{CLK}
$t_{su(STDR)}$	Setup time, START/SYNC falling edge (or 7th SCLK falling edge of STOP command) before $\overline{\text{DRDY}}$ falling edge to stop further conversions (continuous conversion mode)	32		t_{CLK}
READING CONVERSION DATA WITHOUT RDATA COMMAND				
$t_{h(SCDR)}$	Hold time, SCLK low before $\overline{\text{DRDY}}$ falling edge(2)	28		t_{CLK}
$t_{d(DRSC)}$	Delay time, SCLK rising edge after $\overline{\text{DRDY}}$ falling edge(2)	4		t_{CLK}

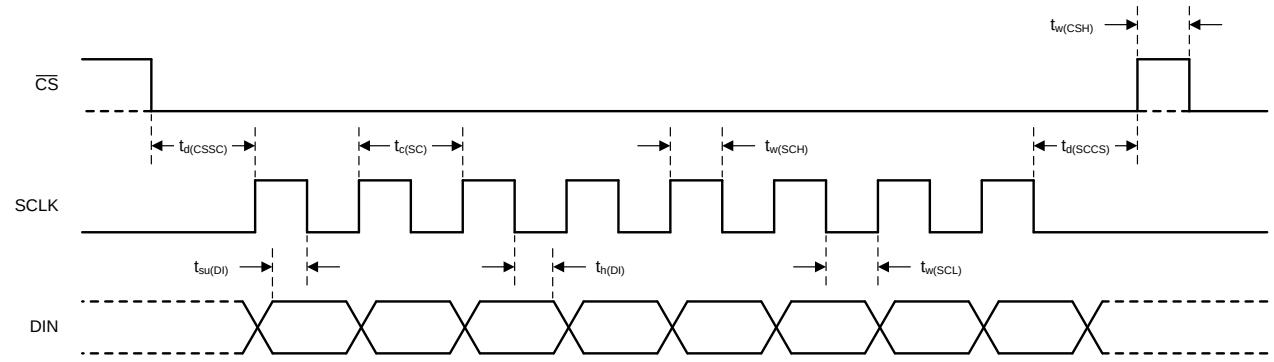
(1) $t_{CLK} = 1 / f_{CLK}$.
(2) Only applicable when reading data without the RDATA command. All commands can be send without any SCLK to $\overline{\text{DRDY}}$ signal timing restrictions.

7.7 Switching Characteristics

over operating ambient temperature range, DVDD = 2.7 V to 3.6 V, IOVDD = DVDD to 5.25 V, and DOUT/$\overline{\text{DRDY}}$ load = 20 pF || 100 kΩ to DGND (unless otherwise noted)

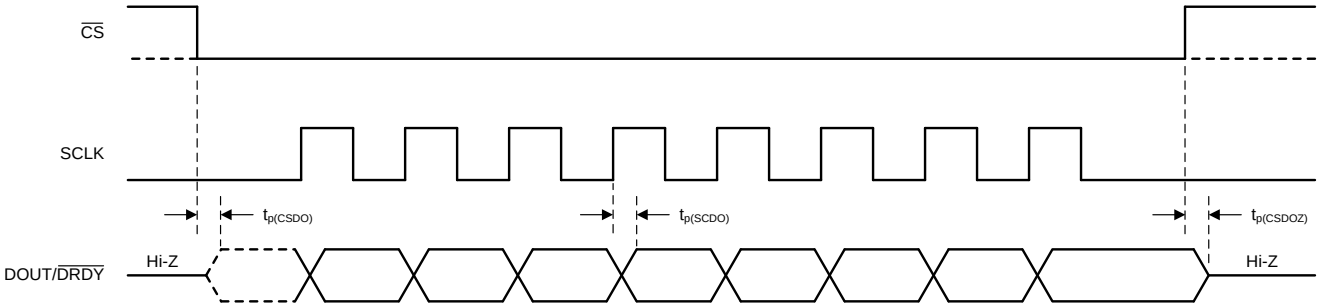
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
$t_{p(CSDO)}$	Propagation delay time, $\overline{\text{CS}}$ falling edge to DOUT driven		0		25	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT		3		30	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{\text{CS}}$ rising edge to DOUT high impedance		0		25	ns
$t_{p(STDR)}$	Propagation delay time, START/SYNC rising edge (or first SCLK rising edge of any command or data read) to $\overline{\text{DRDY}}$ rising edge				2	t_{CLK}
$t_{w(DRH)}$	Pulse duration, $\overline{\text{DRDY}}$ high		24			t_{CLK}
$t_{p(GPIO)}$	Propagation delay time, last SCLK falling edge of WREG command to GPIOx output valid		3		100	ns
	SPI timeout per 8 bit(2)		2^{15}			t_{CLK}

(1) $t_{CLK} = 1 / f_{CLK}$
(2) The SPI interface resets when an entire byte is not sent within the specified timeout time.



NOTE: Single-byte communication is shown. Actual communication can be multiple bytes.

図 1. Serial Interface Timing Requirements



NOTE: Single-byte communication is shown. Actual communication can be multiple bytes.

図 2. Serial Interface Switching Characteristics

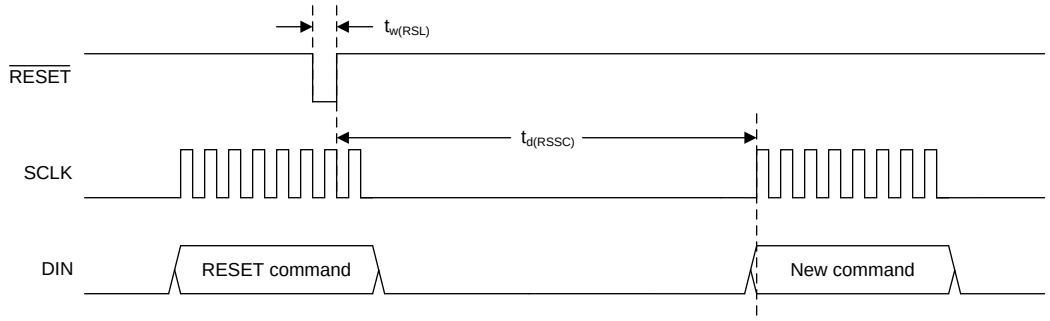


図 3. $\overline{RESET}$ Pin and RESET Command Timing Requirements

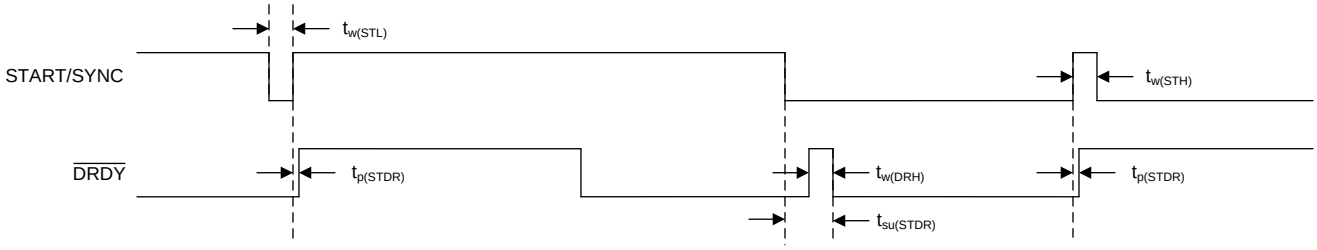


図 4. START/SYNC Pin Timing Requirements

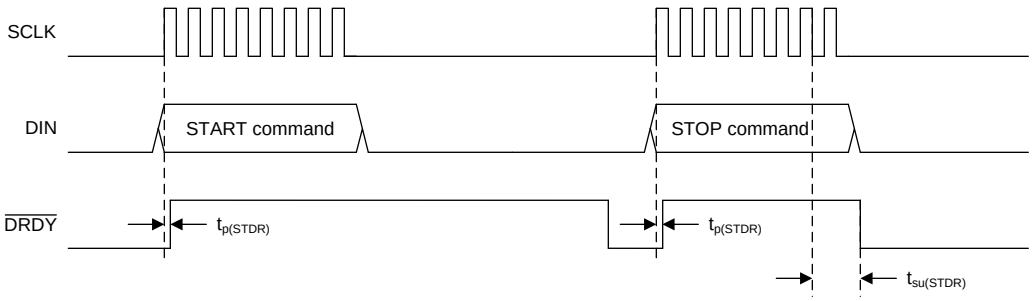


図 5. START Command Timing Requirements

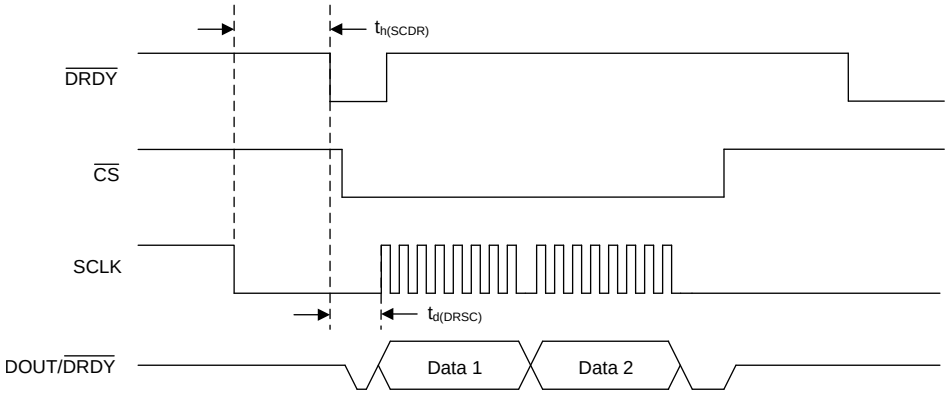


図 6. Read Data Direct (Without an RDATA Command) Timing Requirements

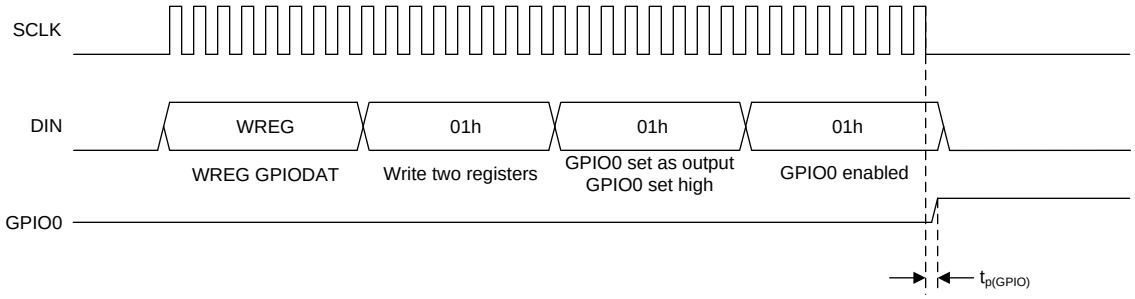
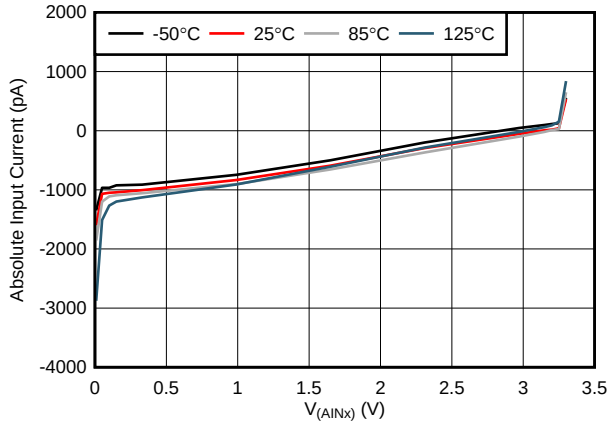


図 7. GPIO Switching Characteristics

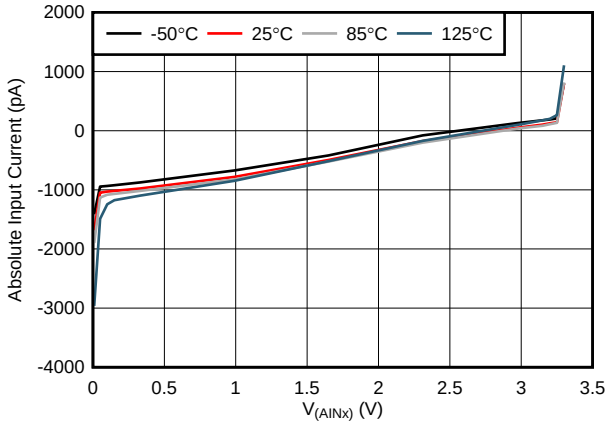
7.8 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, using internal V_{REF} = 2.5 V, internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)



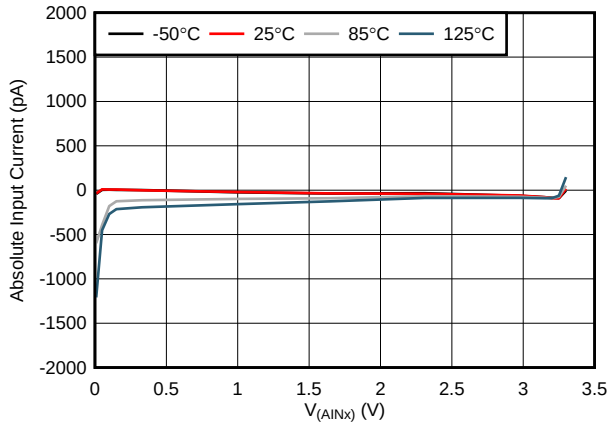
PGA bypassed, DR = 20 SPS, V_{IN} = 0 V

図 8. Absolute Input Current vs Absolute Input Voltage



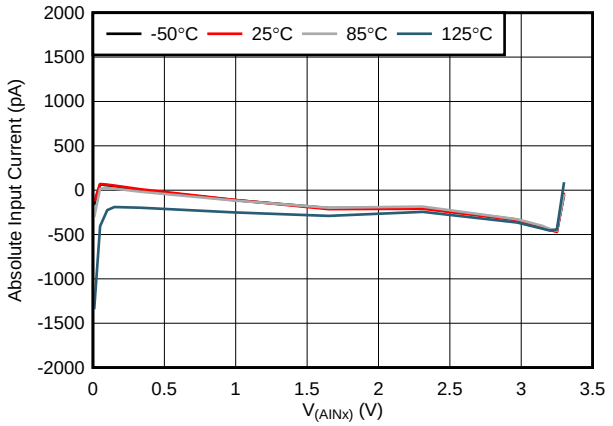
PGA bypassed, DR = 4 kSPS, V_{IN} = 0 V

図 9. Absolute Input Current vs Absolute Input Voltage



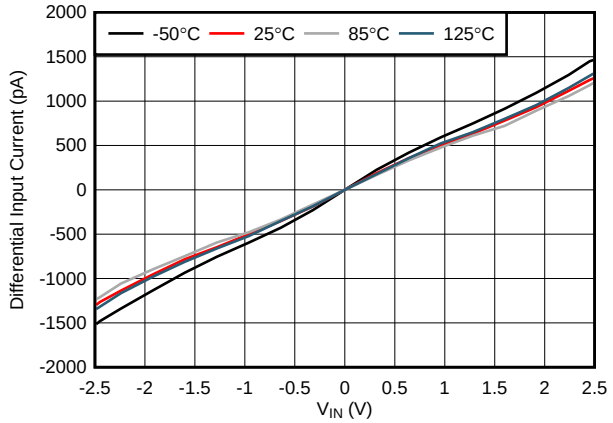
PGA enabled, gain = 1, DR = 20 SPS, V_{IN} = 0 V

図 10. Absolute Input Current vs Absolute Input Voltage



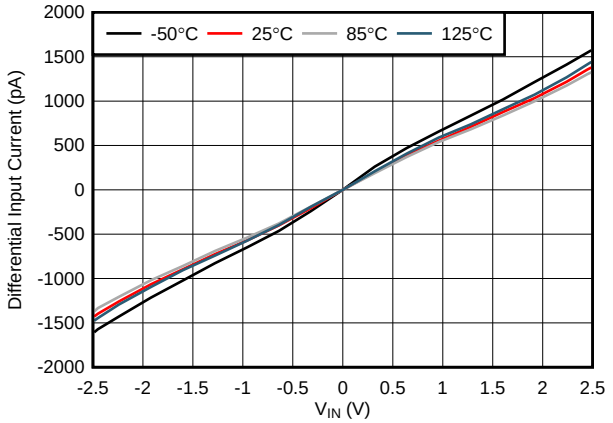
PGA enabled, gain = 1, DR = 4 kSPS, V_{IN} = 0 V

図 11. Absolute Input Current vs Absolute Input Voltage



PGA bypassed, DR = 20 SPS, V_{CM} = 1.65 V

図 12. Differential Input Current vs Differential Input Voltage

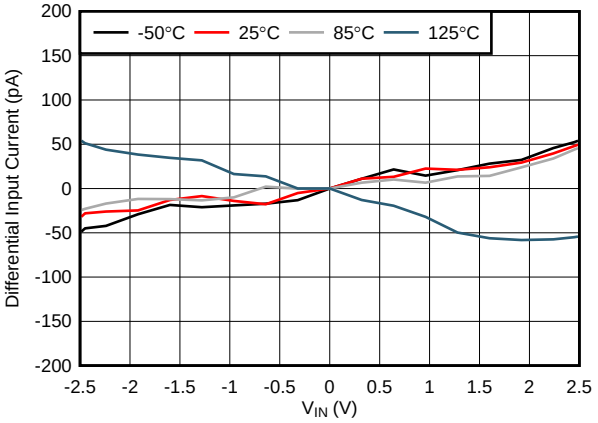


PGA bypassed, DR = 4 kSPS, V_{CM} = 1.65 V

図 13. Differential Input Current vs Differential Input Voltage

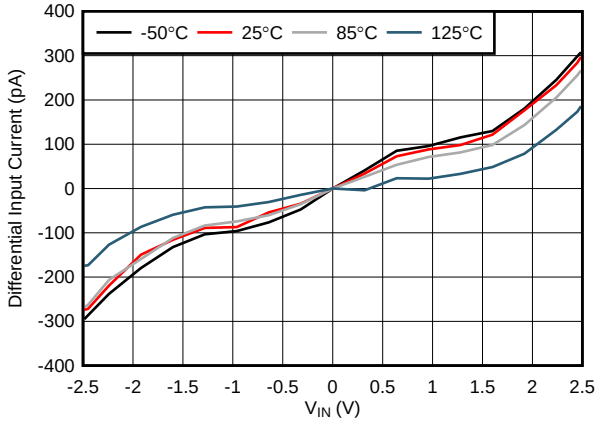
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, using internal V_{REF} = 2.5 V, internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)



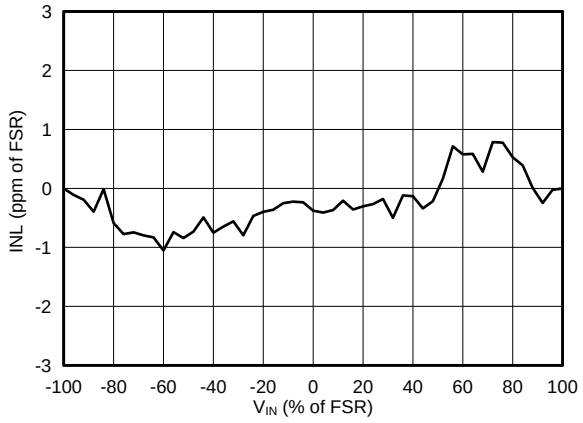
PGA enabled, DR = 20 SPS, V_{CM} = 1.65 V

図 14. Differential Input Current vs Differential Input Voltage



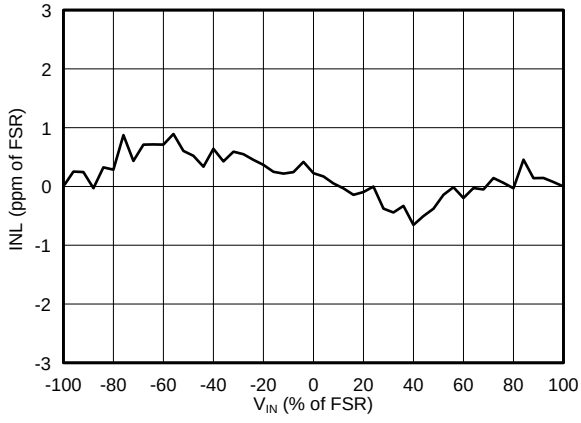
PGA enabled, DR = 4 kSPS, V_{CM} = 1.65 V

図 15. Differential Input Current vs Differential Input Voltage



PGA bypassed, gain = 1

図 16. INL vs Differential Input Voltage



PGA enabled, gain = 1

図 17. INL vs Differential Input Voltage

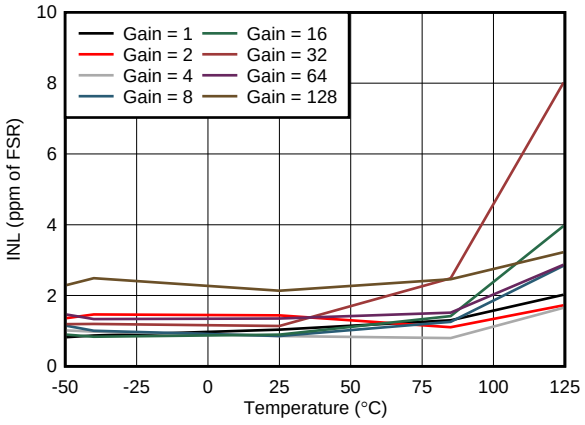


図 18. INL vs Temperature

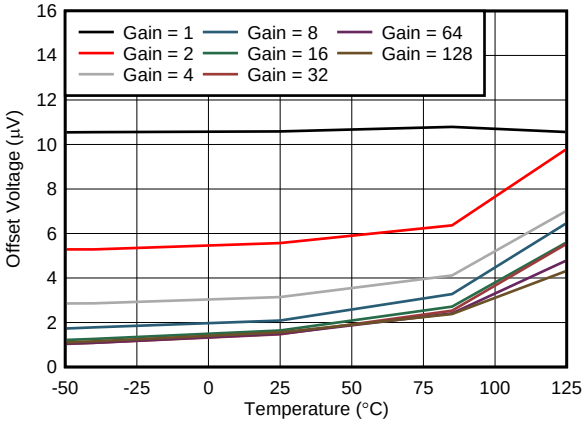


図 19. Offset Voltage vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, using internal V_{REF} = 2.5 V, internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

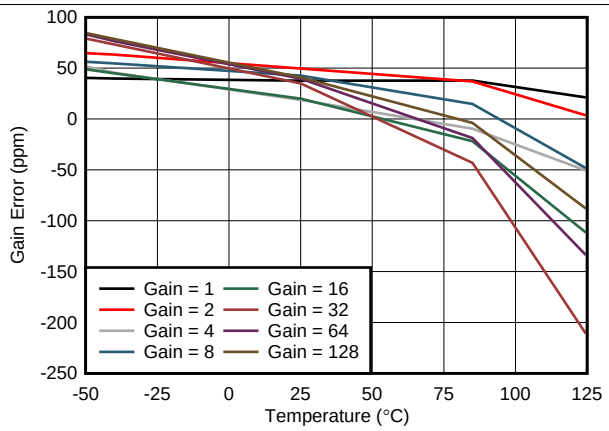


図 20. Gain Error vs Temperature

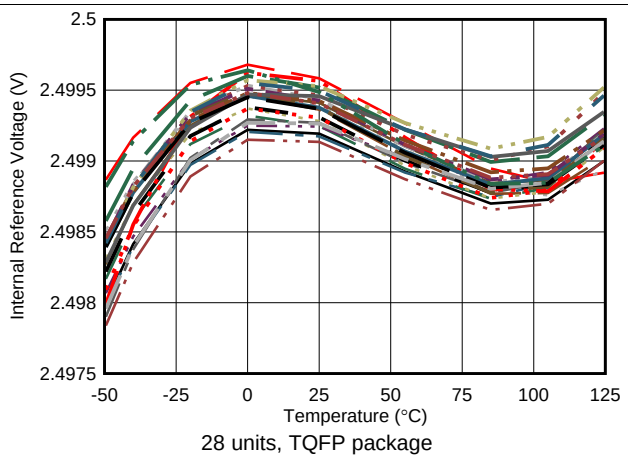


図 21. Internal Reference Voltage vs Temperature

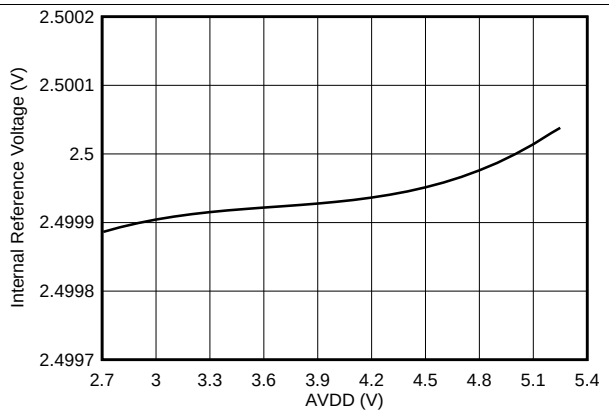


図 22. Internal Reference Voltage vs AVDD

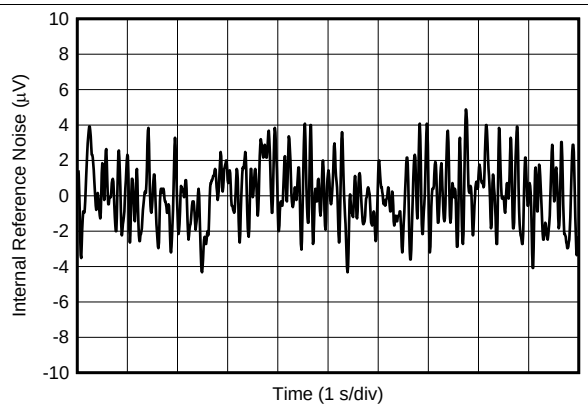


図 23. Internal Reference Voltage Noise

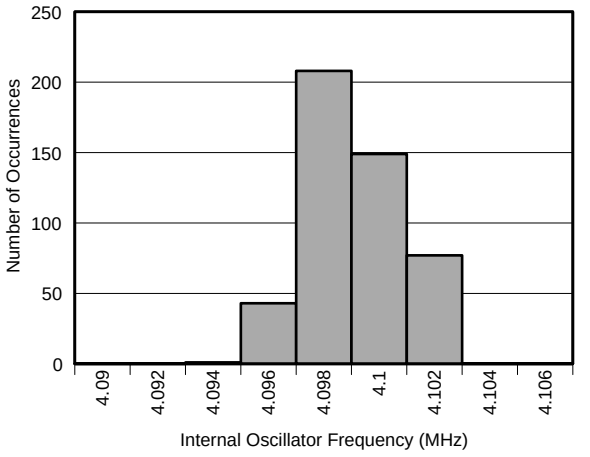


図 24. Internal Oscillator Frequency Histogram

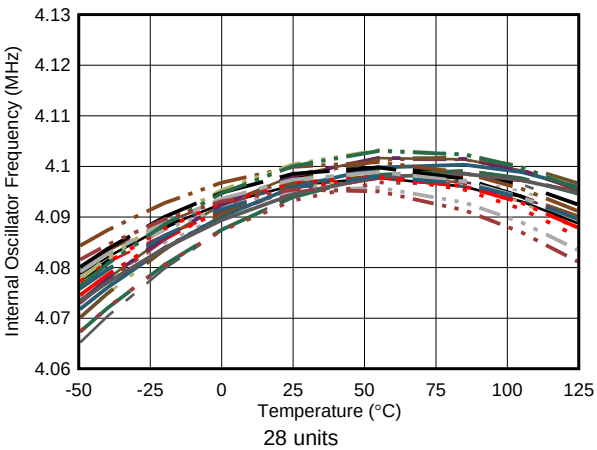


図 25. Internal Oscillator Frequency vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, using internal V_{REF} = 2.5 V, internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

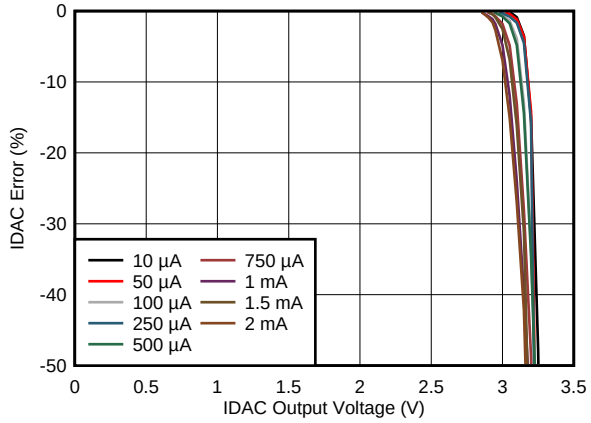


図 26. IDAC Accuracy vs Compliance Voltage

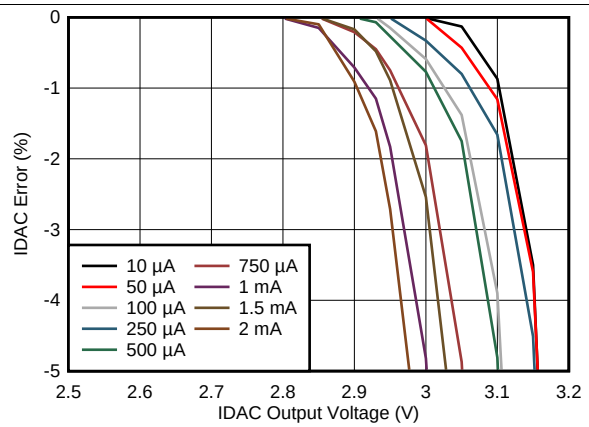
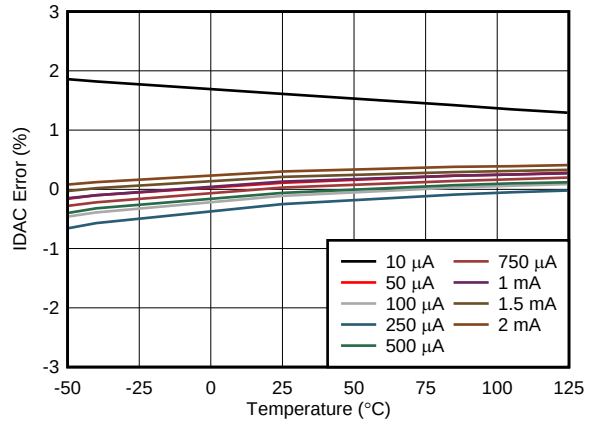


図 27. IDAC Accuracy vs Compliance Voltage



IDAC output voltage = 1.65 V

図 28. IDAC Accuracy vs Temperature

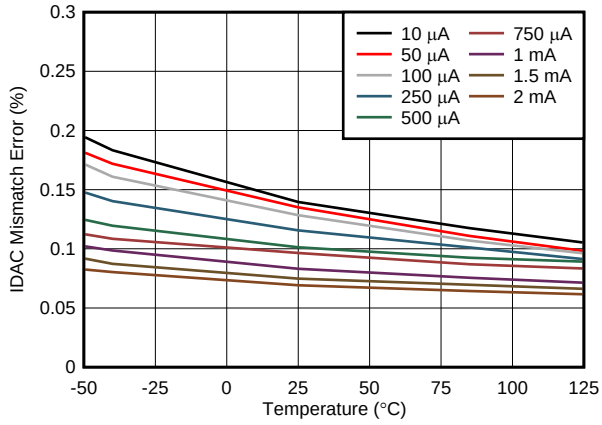


図 29. IDAC Matching vs Temperature

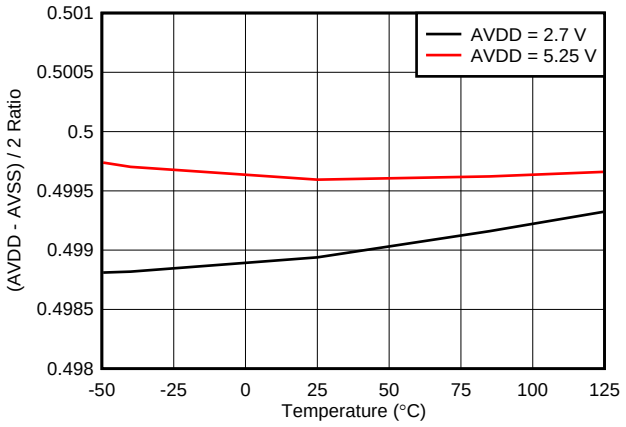


図 30. VBIAS Voltage [(AVDD – AVSS) / 2] vs Temperature

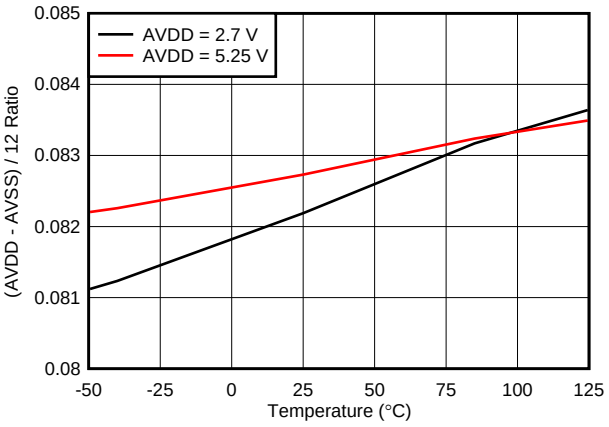


図 31. VBIAS Voltage [(AVDD – AVSS) / 12] vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, using internal V_{REF} = 2.5 V, internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

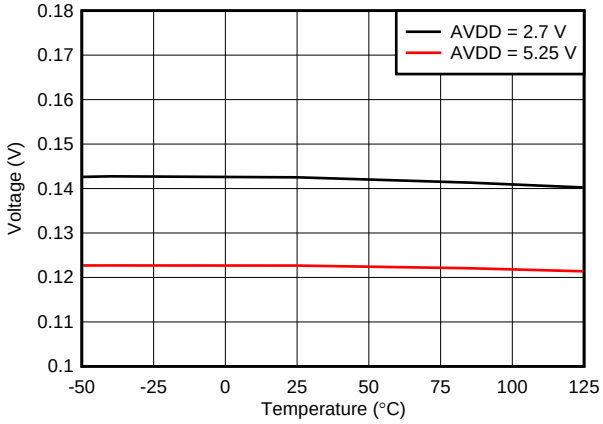


図 32. PGA Rail Detection, PGAN_RAILP, PGAP_RAILP Threshold From AVDD

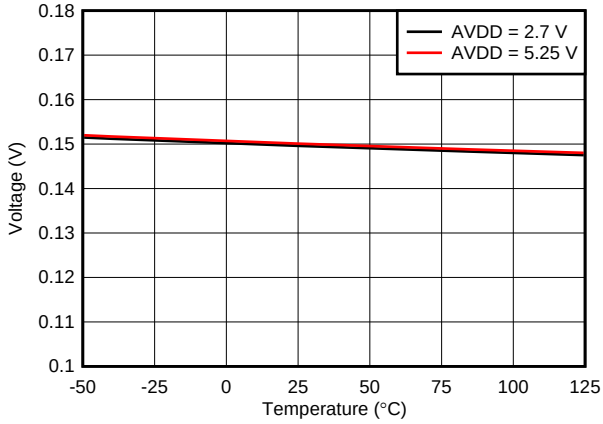


図 33. PGA Rail Detection, PGAN_RAILN, PGAP_RAILN Threshold From AVSS

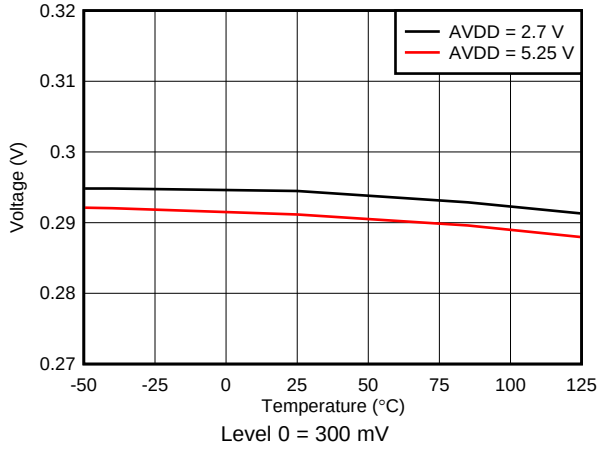


図 34. Reference Threshold Voltage, Level 0

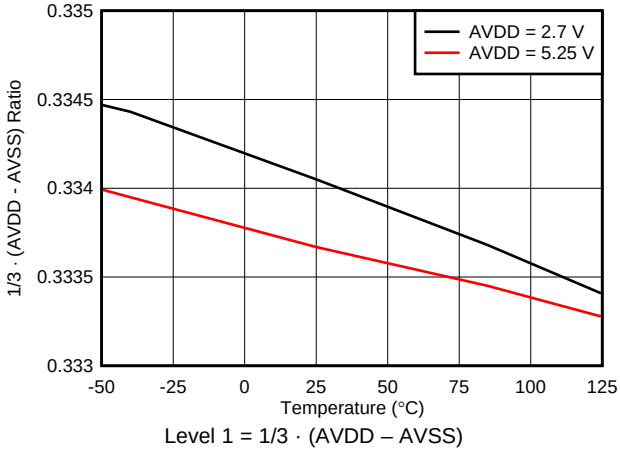


図 35. Reference Threshold Voltage, Level 1

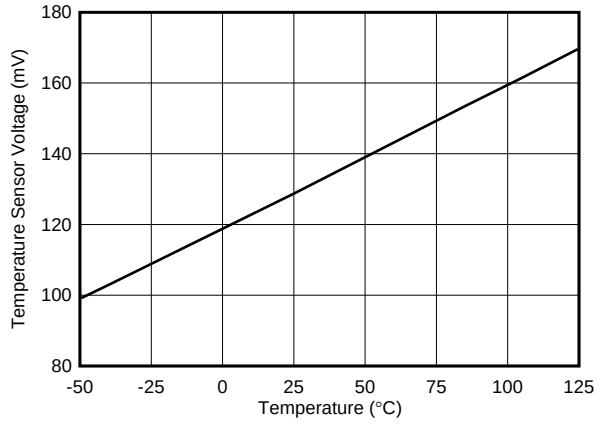


図 36. Temperature Sensor Voltage vs Temperature

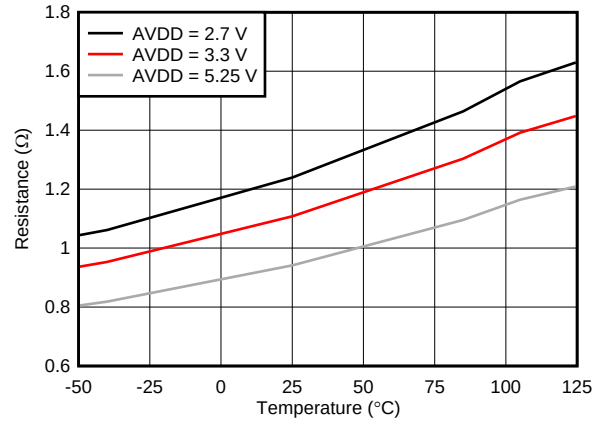


図 37. Low-Side Switch R_{ON} vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, using internal V_{REF} = 2.5 V, internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

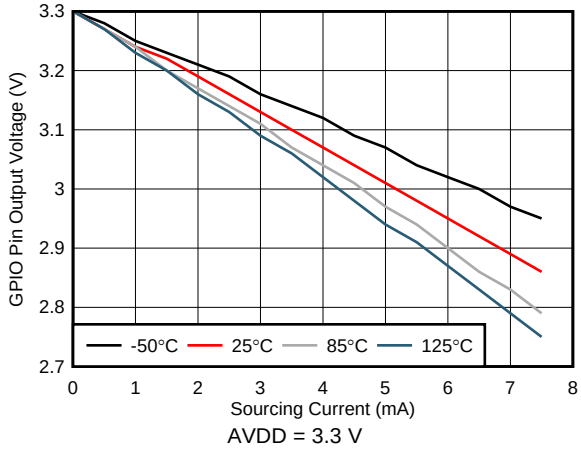


図 38. GPIO Pin Output Voltage vs Sourcing Current

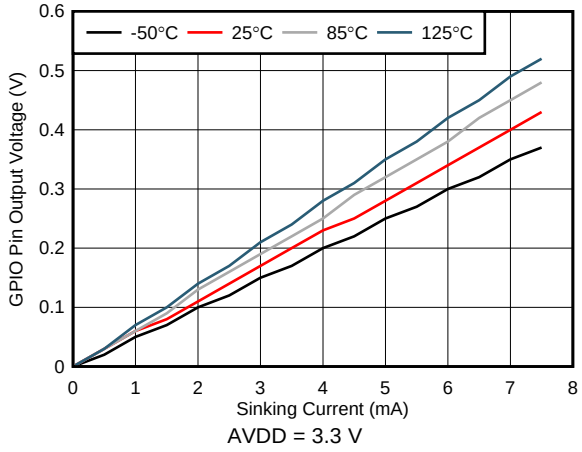


図 39. GPIO Pin Output Voltage vs Sinking Current

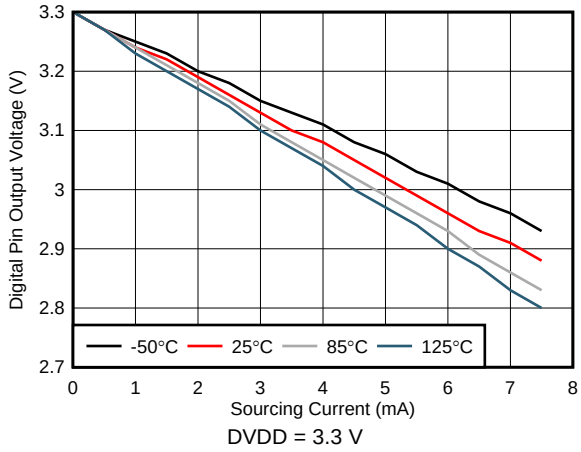


図 40. Digital Pin Output Voltage vs Sourcing Current

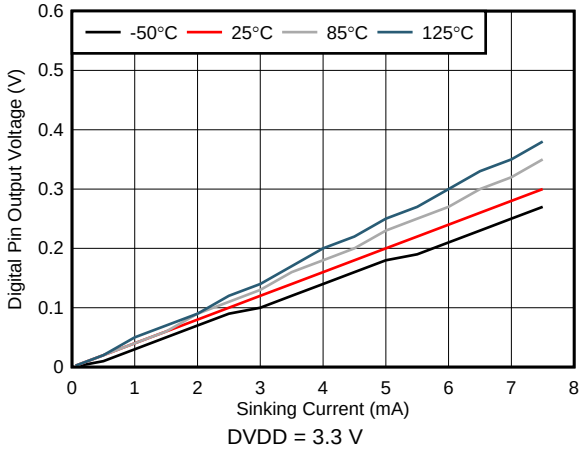


図 41. Digital Pin Output Voltage vs Sinking Current

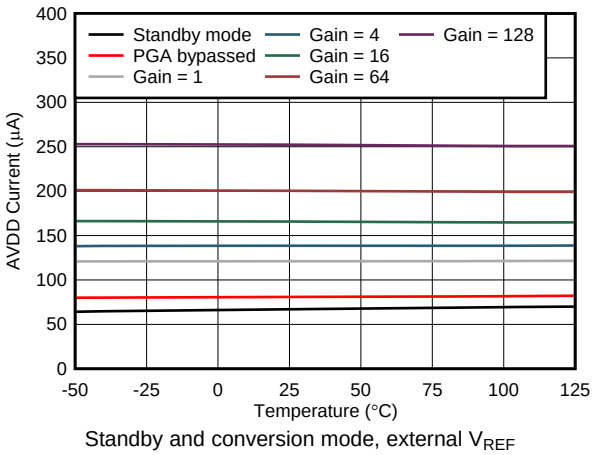


図 42. Analog Supply Current vs Temperature

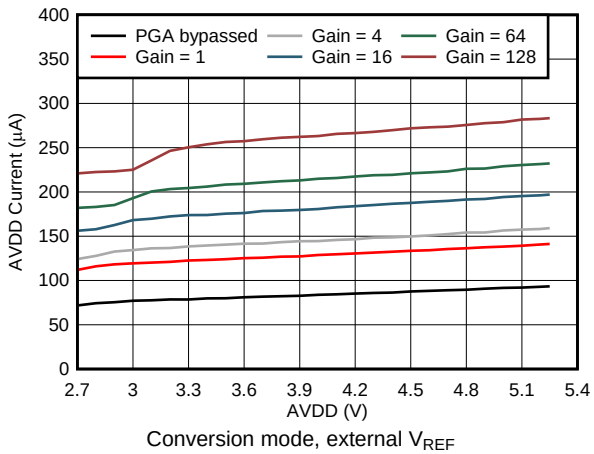


図 43. Analog Supply Current vs AVDD

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, DVDD = IOVDD = 3.3 V, using internal V_{REF} = 2.5 V, internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

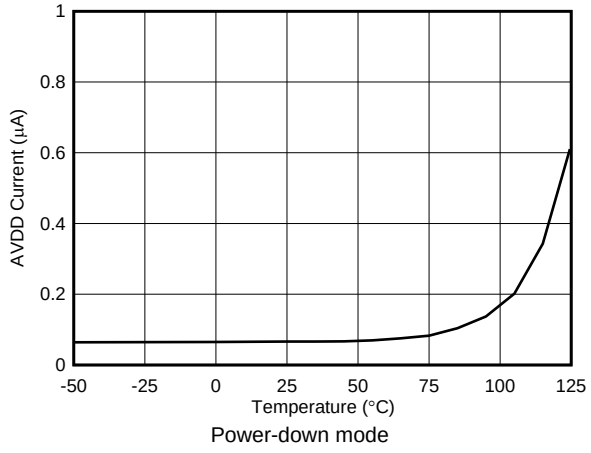


図 44. Analog Supply Current vs Temperature

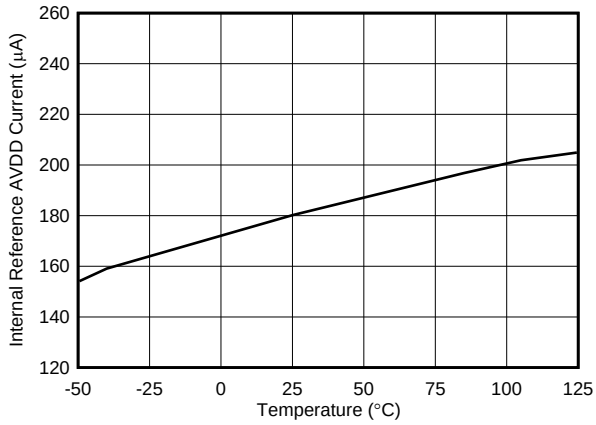


図 45. Internal Reference AVDD Current vs Temperature

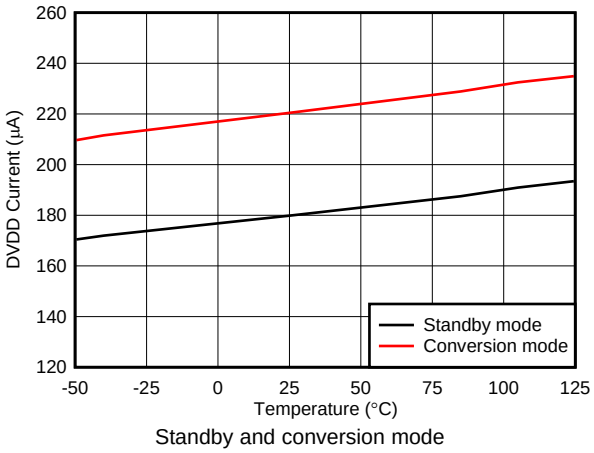


図 46. Digital Supply Current vs Temperature

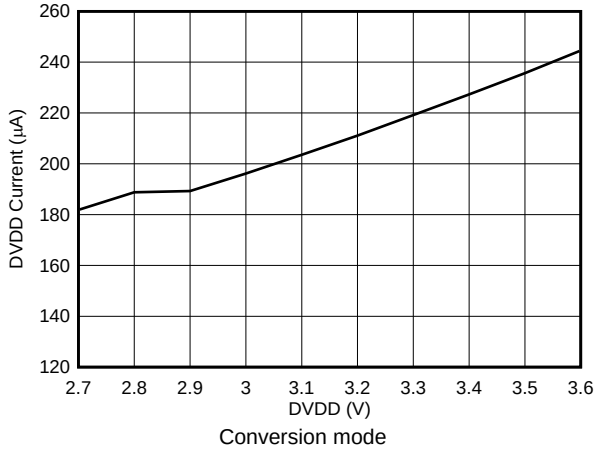


図 47. Digital Supply Current vs DVDD

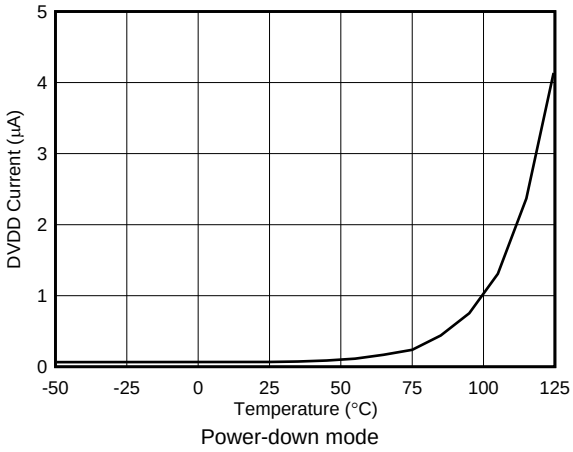


図 48. Digital Supply Current vs Temperature

8 Parameter Measurement Information

8.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called the *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

表 1 to 表 4 summarize the device noise performance. 表 1 and 表 2 list the ADC measurement noise using the $sinc^3$ digital filter at different data rates and different PGA settings, and 表 3 and 表 4 list the ADC measurement noise using the low-latency digital filter. Data are representative of typical noise performance at T_A = 25°C using the internal 2.5-V reference. Data shown are based on 512 consecutive samples from a single device with inputs internally shorted. 表 1 and 表 3 list the input-referred root mean square noise in units of μV_{RMS} for the conditions shown. Note that peak-to-peak (μV_{PP}) values are shown in parentheses. 表 2 and 表 4 list the corresponding data in effective resolution calculated from μV_{RMS} values using 式 1. Noise-free resolution is calculated from μV_{PP} values using 式 2.

The input-referred noise (表 1 and 表 3) only changes marginally when using an external low-noise reference, such as the REF5025. To calculate effective resolution and noise-free resolution when using a reference voltage other than 2.5 V, use 式 1 and 式 2:

$$\text{Effective Resolution} = \ln[(2 \cdot V_{REF} / \text{Gain}) / V_{RMS\text{-}Noise}] / \ln(2) \quad (1)$$

$$\text{Noise-Free Resolution} = \ln[(2 \cdot V_{REF} / \text{Gain}) / V_{PP\text{-}Noise}] / \ln(2) \quad (2)$$

表 5 to 表 8 repeat the measurements of 表 1 to 表 4 but use the global chop feature of the device. The global chop feature averages two measurement of the ADC with the inputs swapped. This feature significantly reduces the input offset of the device, and reduces noise in the measurement.

Noise performance with the PGA bypassed are identical to the noise performance of the device with gain = 1 in 表 1 to 表 8.

表 1. Noise in μV_{RMS} (μV_{PP}) with $Sinc^3$ Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	GAIN							
	1	2	4	8	16	32	64	128
2.5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
10	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
16.6	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
20	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
50	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
60	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
100	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
200	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.90)
400	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.5)	0.60 (1.3)
800	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (2.2)	0.60 (2.0)
1000	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.5)	1.2 (2.4)	0.60 (2.2)
2000	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (4.0)	1.2 (3.5)	0.60 (2.8)
4000	76.3 (95)	38.1 (45)	19.1 (24)	9.5 (13)	4.8 (7.1)	2.4 (5.2)	1.2 (5.0)	0.80 (4.9)

表 2. Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with Sinc^3 Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	GAIN							
	1	2	4	8	16	32	64	128
2.5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
10	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.6	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
20	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
50	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
60	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
100	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
200	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.3)
400	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.7)	16 (14.9)
800	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.1)	16 (14.3)
1000	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.0)	16 (14.1)
2000	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.3)	16 (14.4)	16 (13.8)
4000	16 (15.7)	16 (15.7)	16 (15.7)	16 (15.6)	16 (15.4)	16 (14.9)	16 (13.9)	16 (13.0)

表 3. Noise in μV_{RMS} (μV_{PP}) with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	GAIN							
	1	2	4	8	16	32	64	128
2.5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
10	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
16.6	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
20	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
50	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
60	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.90)
100	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.4)	0.60 (1.3)
200	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.9)	0.60 (1.7)
400	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.8)	1.2 (2.9)	0.60 (2.3)
800	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (4.0)	1.2 (3.8)	0.60 (3.2)
1000	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (5.1)	1.2 (4.3)	0.60 (3.8)
2000	76.3 (83)	38.1 (80)	19.1 (32)	9.5 (17)	4.8 (11)	2.4 (6.7)	1.2 (6.6)	1.0 (6.5)
4000	103 (629)	38.1 (404)	24 (160)	12 (70)	6.4 (39)	3.3 (21)	3.1 (21)	2.6 (20)

表 4. Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	GAIN							
	1	2	4	8	16	32	64	128
2.5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
10	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.6	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
20	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
50	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
60	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.4)
100	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.8)	16 (14.9)
200	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.3)	16 (14.5)
400	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.8)	16 (14.7)	16 (14.0)
800	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.2)	16 (14.3)	16 (13.6)
1000	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.8)	16 (14.9)	16 (14.2)	16 (13.3)
2000	16 (15.9)	16 (14.9)	16 (15.3)	16 (15.2)	16 (14.8)	16 (14.5)	16 (13.5)	15.2 (12.6)
4000	16 (13.0)	16 (12.6)	15.7 (12.9)	16 (13.1)	15.6 (13.0)	15.5 (12.9)	14.4 (11.9)	13.6 (10.9)

表 5. Noise in μV_{RMS} (μV_{PP}) with $Sinc^3$ Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)(1)	GAIN							
	1	2	4	8	16	32	64	128
2.5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
10	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
16.6	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
20	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
50	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
60	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
100	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
200	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.75)
400	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.90)
800	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.4)	0.60 (1.3)
1000	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.6)	0.60 (1.5)
2000	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.5)	1.2 (2.1)	0.60 (2.1)
4000	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (5.0)	2.4 (4.0)	1.2 (3.3)	0.60 (3.2)

(1) The actual data conversion period changes with the $sinc^3$ filter and global chop mode enabled; see 表 19 for details.

表 6. Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with Sinc^3 Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)(1)	GAIN							
	1	2	4	8	16	32	64	128
2.5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
10	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.6	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
20	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
50	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
60	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
100	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
200	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.7)
400	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.4)
800	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.7)	16 (14.9)
1000	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.6)	16 (14.7)
2000	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.9)	16 (15.2)	16 (14.2)
4000	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.9)	16 (15.3)	16 (14.5)	16 (13.6)

(1) The actual data conversion period changes with the sinc^3 filter and global chop mode enabled; see 表 19 for details.

表 7. Noise in μV_{RMS} (μV_{PP}) with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	GAIN							
	1	2	4	8	16	32	64	128
2.5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
5	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
10	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
16.6	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
20	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
50	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.60)
60	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.67)
100	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.2)	0.60 (0.80)
200	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.3)	0.60 (1.0)
400	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (1.8)	0.60 (1.7)
800	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.4)	1.2 (2.5)	0.60 (2.3)
1000	76.3 (76.3)	38.1 (38.1)	19.1 (19.1)	9.5 (9.5)	4.8 (4.8)	2.4 (2.8)	1.2 (2.4)	0.60 (2.5)
2000	76.3 (76.3)	38.1 (48)	19.1 (23)	9.5 (13)	4.8 (7.0)	2.4 (5.6)	1.2 (5.2)	0.7 (3.9)
4000	76.3 (275)	38.1 (190)	19.1 (100)	9.5 (55)	4.8 (28)	2.4 (15)	1.2 (13)	2.2 (12)

表 8. Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	GAIN							
	1	2	4	8	16	32	64	128
2.5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
10	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.6	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
20	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
50	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
60	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.8)
100	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.6)
200	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.9)	16 (15.2)
400	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.4)	16 (14.5)
800	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (14.9)	16 (14.0)
1000	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.8)	16 (15.0)	16 (13.9)
2000	16 (16)	16 (15.7)	16 (15.7)	16 (15.6)	16 (15.4)	16 (14.8)	16 (13.9)	15.9 (13.3)
4000	16 (14.1)	16 (13.7)	16 (13.6)	16 (13.5)	16 (13.4)	16 (13.4)	15.0 (12.7)	14.1 (11.5)

9 Detailed Description

9.1 Overview

The ADS114S06 and ADS114S08 are precision 16-bit, delta-sigma (ΔΣ) ADCs with an integrated analog front end (AFE) to simplify precision sensor connections. The ADC provides output data rates from 2.5 SPS to 4000 SPS for flexibility in resolution and data rates over a wide range of applications. The low-noise and low-drift architecture make these devices suitable for precise measurement of low-voltage sensors, such as load cells and temperature sensors.

The ADS114S0x incorporate several features that simplify precision sensor measurements. Key integrated features include:

- Low-noise, CMOS PGA with integrated signal fault detection
- Low-drift, 2.5-V voltage reference
- Two sets of buffered external reference inputs with reference voltage level detection
- Dual, matched, sensor-excitation current sources (IDACs)
- Internal 4.096-MHz oscillator
- Temperature sensor
- Four general-purpose input/output pins (GPIOs)
- A low-resistance switch (when connected to AVSS) can be used to disconnect bridge sensors to reduce current consumption

As described in the *Functional Block Diagram* section, these devices provide 13 (ADS114S08) or 7 (ADS114S06) analog inputs that are configurable as either single-ended inputs, differential inputs, or any combination of the two. Many of the analog inputs have additional features as programmed by the user. The analog inputs can be programmed to enable the following extended features:

- Two sensor excitation current sources: all analog input pins (and REFP1 and REFN1 on the ADS114S06)
- Sensor biasing voltage (VBIAS): pins AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AINCOM
- Four GPIO pins: AIN8, AIN9, AIN10, AIN11 (ADS114S08 only, the ADS114S06 has dedicated GPIOs)
- Sensor burn-out current sources: analog input pins selected for ADC input

Following the input multiplexer (MUX), the ADC features a high input-impedance, low-noise, programmable gain amplifier (PGA), eliminating the need for an external amplifier. The PGA gain is programmable from 1 to 128 in binary steps. The PGA can be bypassed to allow the input range to extend 50 mV below ground or above supply. The PGA has output voltage monitors to verify the integrity of the conversion result.

An inherently stable delta-sigma modulator measures the ratio of the input voltage to the reference voltage to provide the ADC result. The ADC operates with the internal 2.5-V reference, or with up to two external reference inputs. The external reference inputs can be continuously monitored for low (or missing) voltage. The REFOUT pin provides the buffered 2.5-V internal voltage reference output that can be used to bias external circuitry.

The digital filter provides two filter modes, $sinc^3$ and low-latency, allowing optimization of settling time and line-cycle rejection. The third-order sinc filter offers simultaneous 50-Hz and 60-Hz line-cycle rejection at data rates of 2.5 SPS, 5 SPS, and 10 SPS, 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and 60-Hz rejection at data rates of 20 SPS and 60 SPS. The low-latency filter provides settled data with 50-Hz and 60-Hz line-cycle rejection at data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS, 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and 60-Hz rejection at a data rate of 60 SPS.

Two programmable excitation current sources provide bias to resistive sensors [such as resistance temperature detectors (RTDs) or thermistors]. The ADC integrates several system monitors for read back, such as temperature sensor and supply monitors. Four GPIO pins are available as either dedicated pins (ADS114S06) or combined with analog input pins (ADS114S08).

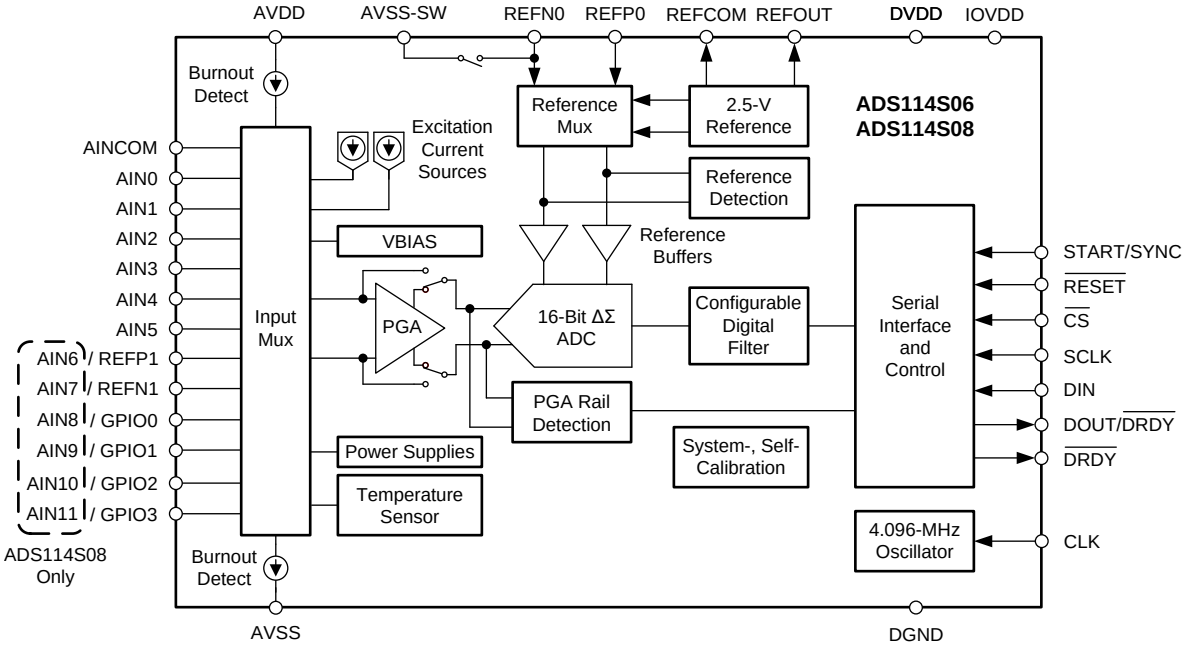
The ADS114S0x system clock is either provided by the internal low-drift, 4.096-MHz oscillator or an external clock source on the CLK input.

Overview (continued)

The SPI-compatible serial interface is used to read the conversion data and also to configure and control the ADC. The serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$. The conversion data are provided with an optional CRC code for improved data integrity. The dual function DOUT/$\overline{DRDY}$ output indicates when conversion data are ready and also provides the data output. The serial interface can be implemented with as little as three connections by tying $\overline{CS}$ low. Start ADC conversions with either the START/SYNC pin or with commands. The ADC can be programmed for a continuous conversion mode or to perform single-shot conversions.

The AVDD analog supply operates with bipolar supplies from ±1.5 V to ±2.625 V or with a unipolar supply from 2.7 V to 5.25 V. For unipolar-supply operation, use the VBIAS voltage to bias isolated (floating) sensors. The digital supplies operate with unipolar supplies only. The DVDD digital power supply operates from 2.7 V to 3.6 V and the IOVDD supply operates from DVDD to 5.25 V.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Multiplexer

The ADS114S0x contains a flexible input multiplexer; see 図 49. Select any of the six (ADS114S06) or 12 (ADS114S08) analog inputs as the positive or negative input for the PGA using the MUX_P[3:0] and MUX_N[3:0] bits in the input multiplexer register (02h). In addition, AINCOM can be selected as the positive or negative PGA input. AINCOM is treated as a regular analog input, as is AINx. Use AINCOM in single-ended measurement applications as the common input for the other analog inputs.

The multiplexer also routes the excitation current sources to drive resistive sensors (bridges, RTDs, and thermistors) and can provide bias voltages for unbiased sensors (unbiased thermocouples for example) to analog input pins.

The ADS114S0x also contain a set of system monitor functions measured through the multiplexer. The inputs can be shorted together at mid-supply [(AVDD + AVSS) / 2] to measure and calibrate the input offset of the analog front-end and the ADC. The system monitor also includes a temperature sensor that provides a measurement of the device temperature. The system monitor can also measure the analog and digital supplies, measuring [(AVDD – AVSS) / 4] for the analog supply or DVDD / 4 for the digital supply. Finally, the system monitor contains a set of burn-out current sources that pull the inputs to either supply if the sensor has burned out and has a high impedance so that the ADC measures a full-scale reading.

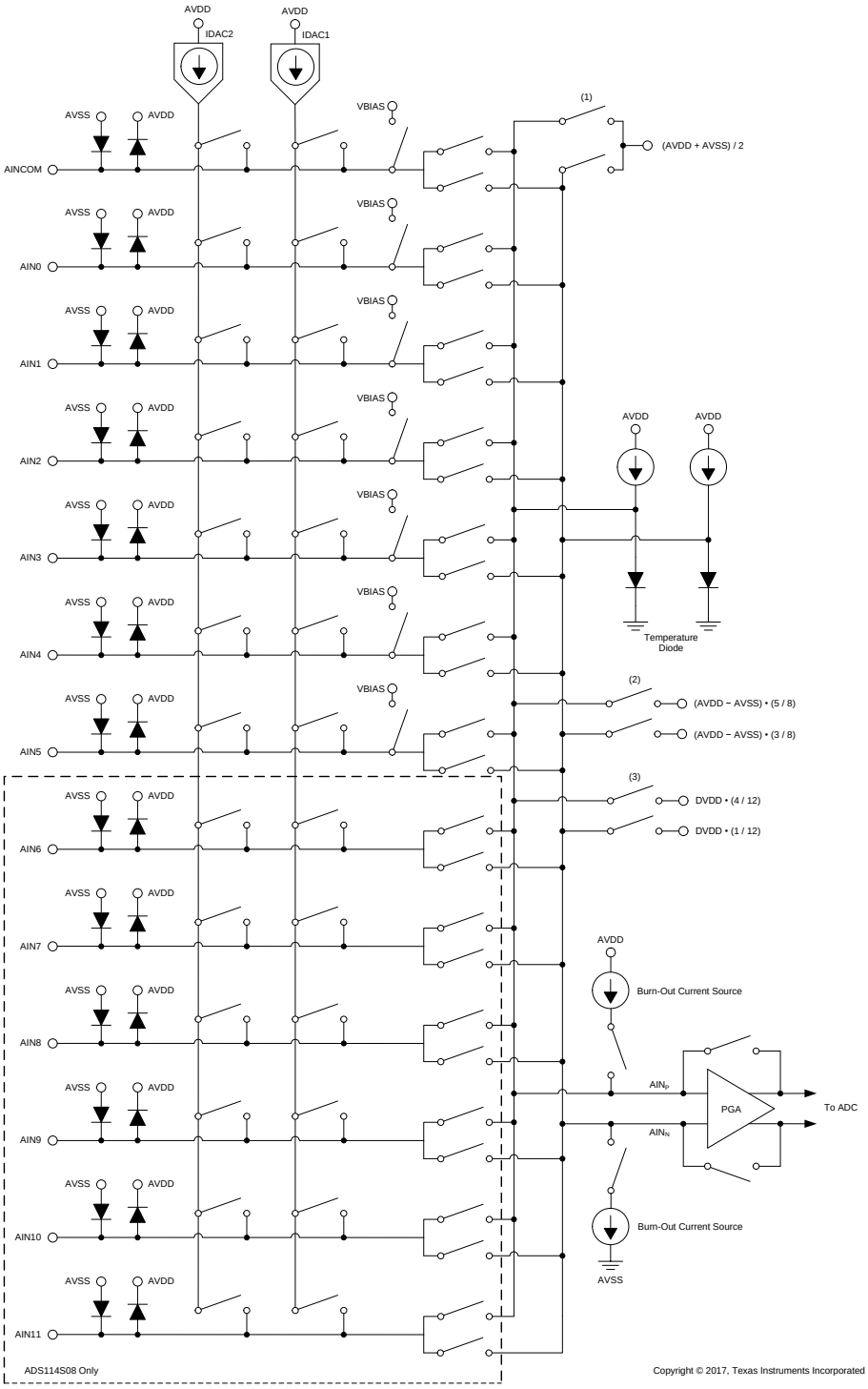
The multiplexer implements a break-before-make circuit. When changing the multiplexer channels using the MUX_P[3:0] and MUX_N[3:0] bits, the device first disconnects the PGA inputs from the analog inputs and connects them to mid-supply for $2 \cdot t_{CLK}$. In the next step, the PGA inputs connect to the selected new analog input channels. This break-before-make behavior ensures the ADC always starts from a known state and that the analog inputs are not momentarily shorted together.

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by 式 3:

$$AVSS - 0.3\ V < V_{(AINx)} < AVDD + 0.3\ V \quad (3)$$

External Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unselected input on the device can affect conversions taking place on other input pins.

Feature Description (continued)



(1) AIN_P and AIN_N are connected together to (AVDD + AVSS) / 2 for offset measurement.

(2) Measurement for the analog supply equivalent to (AVDD – AVSS) / 4.

(3) Measurement for the analog supply equivalent to DVDD / 4.

図 49. Analog Input Multiplexer

Feature Description (continued)

9.3.2 Low-Noise Programmable Gain Amplifier

The ADS114S06 and ADS114S08 feature a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). 図 50 shows a simplified diagram of the PGA. The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the gain of the PGA. The PGA input is equipped with an electromagnetic interference (EMI) filter and an antialiasing filter on the output.

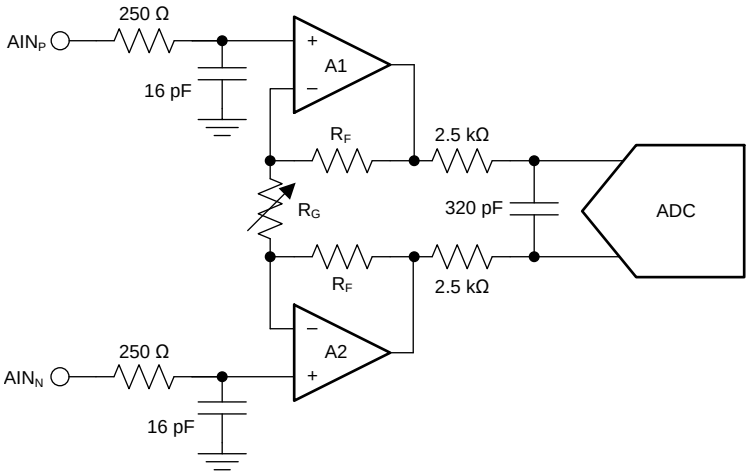


図 50. Simplified PGA Diagram

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128 using the GAIN[2:0] bits in the gain setting register (03h). Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in 式 4:

$$FSR = \pm V_{REF} / Gain \quad (4)$$

表 9 shows the corresponding full-scale ranges when using the internal 2.5-V reference.

表 9. PGA Full-Scale Range

GAIN SETTING	FSR
1	±2.5 V
2	±1.25 V
4	±0.625 V
8	±0.313 V
16	±0.156 V
32	±0.078 V
64	±0.039 V
128	±0.020 V

The PGA must be enabled with the PGA_EN[1:0] bits of the gain setting register (03h). Setting these bits to 00 powers down and bypasses the PGA. A setting of 01 enables the PGA. The 10 and 11 settings are reserved and must not be written to the device.

With the PGA enabled, gains 64 and 128 are established in the digital domain. When the device is set to 64 or 128, the PGA is set to a gain of 32, and additional gain is established with digital scaling. The input-referred noise does still improve compared to the gain = 32 setting because the PGA is biased with a higher supply current to reduce noise.

9.3.2.1 PGA Input-Voltage Requirements

As with many amplifiers, the PGA has an absolute input voltage range requirement that cannot be exceeded. The maximum and minimum absolute input voltages are limited by the voltage swing capability of the PGA output. The specified minimum and maximum absolute input voltages (V_{AINP} and V_{AINN}) depend on the PGA gain, the maximum differential input voltage (V_{INMAX}), and the tolerance of the analog power-supply voltages (AVDD and AVSS). Use the maximum voltage expected in the application for V_{INMAX}. The absolute positive and negative input voltages must be within the specified range, as shown in 式 5:

$$AVSS + 0.15\ V + |V_{INMAX}| \cdot (Gain - 1) / 2 < V_{AINP}, V_{AINN} < AVDD - 0.15\ V - |V_{INMAX}| \cdot (Gain - 1) / 2$$

where

- V_{AINP}, V_{AINN} = absolute input voltage
- $V_{INMAX} = V_{AINP} - V_{AINN}$ = maximum differential input voltage (5)

As mentioned in the previous section, PGA gain settings of 64 and 128 are scaled in the digital domain and are not implemented with the amplifier. When using the PGA in gains of 64 and 128, set the gain in 式 5 to 32 to calculate the absolute input voltage range.

The relationship between the PGA input to the PGA output is shown graphically in 図 51. The PGA output voltages (V_{OUTP}, V_{OUTN}) depend on the PGA gain and the input voltage magnitudes. For linear operation, the PGA output voltages must not exceed AVDD – 0.15 V or AVSS + 0.15 V. Note that the diagram depicts a positive differential input voltage that results in a positive differential output voltage.

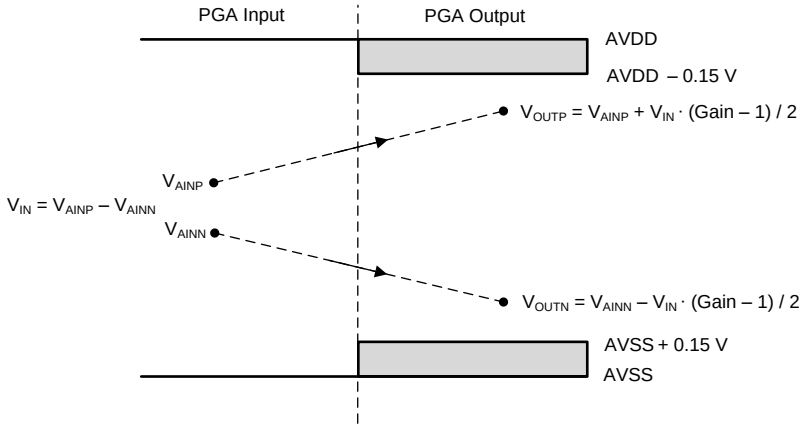


図 51. PGA Input/Output Range

Download the ADS1x4S0x design calculator from www.ti.com. This calculator can be used to determine the input voltage range of the PGA.

9.3.2.2 PGA Rail Flags

The PGA rail flags (FL_P_RAILP, FL_P_RAILN, FL_N_RAILP, and FL_N_RAILN) in the status register (01h) indicate if the positive or negative output of the PGA is closer to the analog supply rails than 150 mV. Enable the PGA output rail detection circuit using the FL_RAIL_EN bit in the excitation current register 1 (06h). A flag going high indicates that the PGA is operating outside the linear operating or absolute input voltage range. PGA rail flags are discussed in more detail in the *PGA Output Voltage Rail Monitors* section.

9.3.2.3 Bypassing the PGA

At a gain of 1, the device can be configured to disable and bypass the low-noise PGA. Disabling the PGA lowers the overall power consumption and also removes the restrictions of 式 5 for the input voltage range. If the PGA is bypassed, the ADC absolute input voltage range extends beyond the AVDD and AVSS power supplies, allowing input voltages at or below ground. The absolute input voltage range when the PGA is bypassed is shown in 式 6:

$$AVSS - 0.05\ V < V_{AINP}, V_{AINN} < AVDD + 0.05\ V \quad (6)$$

In order to measure single-ended signals that are referenced to AVSS ($AIN_P = V_{IN}$, AIN_N = AVSS), the PGA must be bypassed. The PGA is bypassed and powered down by setting the PGA_EN[1:0] bits to 00 in the gain setting register (03h).

For signal sources with high output impedance, external buffering may still be necessary. Note that active buffers introduce noise and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

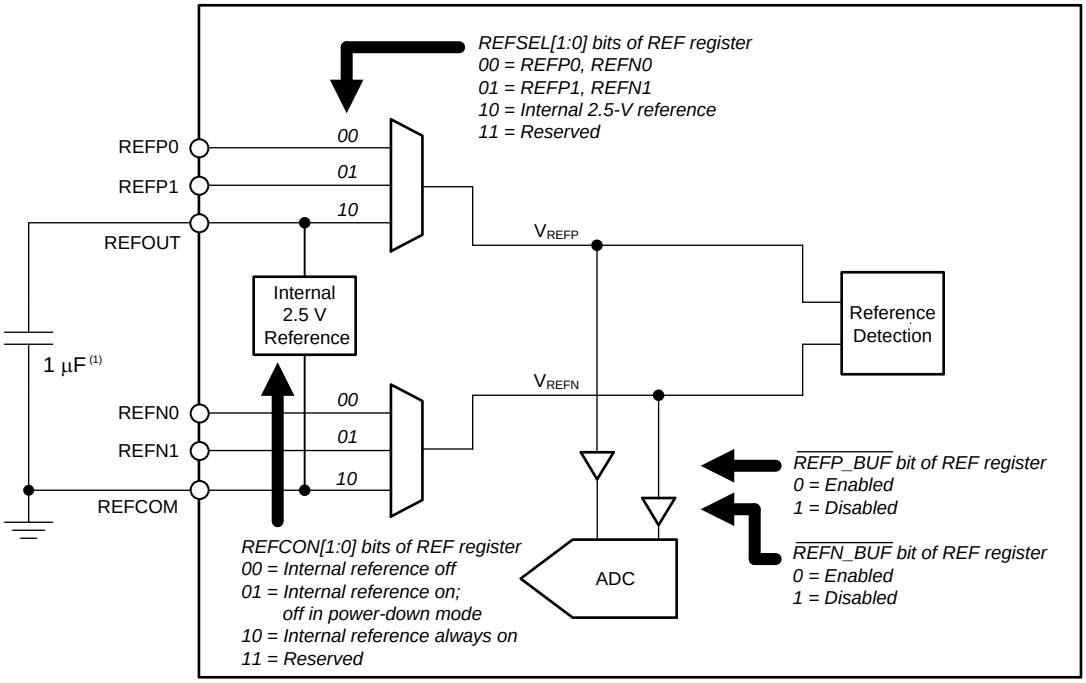
9.3.3 Voltage Reference

The devices require a reference voltage for operation. The ADS114S0x offers an integrated low-drift 2.5-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the ADS114S08 offers two differential reference input pairs (REFP0, REFN0 and REFP1, REFN1). The differential reference inputs allow freedom in the reference common-mode voltage. REFP0 and REFN0 are dedicated reference inputs, whereas REFP1 and REFN1 are shared with inputs AIN6 and AIN7 (respectively) on the ADS114S08. The specified external reference voltage range is 0.5 V to AVDD. The reference voltage is shown in 式 7, where $V_{(REFPx)}$ and $V_{(REFNx)}$ are the absolute positive and absolute negative reference voltages.

$$V_{REF} = V_{(REFPx)} - V_{(REFNx)} \quad (7)$$

The polarity of the reference voltage internal to the ADC must be positive. The magnitude of the reference voltage together with the PGA gain establishes the ADC full-scale differential input range as defined by FSR = $\pm V_{REF}$ / Gain.

図 52 shows the block diagram of the reference multiplexer. The ADC reference multiplexer selects between the internal reference and two external references (REF0 and REF1). The reference multiplexer is programmed with the REFSEL[1:0] bits in the reference control register (05h). By default, the external reference pair REFP0, REFN0 is selected.



(1) The internal reference requires a minimum 1-µF capacitor connected from REFOUT to REFCOM.

図 52. Reference Multiplexer Block Diagram

The ADC also contains an integrated reference voltage monitor. This monitor provides continuous detection of a low or missing reference during the conversion cycle. The reference monitor flags (FL_REF_L0 and FL_REF_L1) are set in the STATUS byte and described in the *Reference Monitor* section.

9.3.3.1 Internal Reference

The ADC integrates a precision, low-drift, 2.5-V reference. The internal reference is enabled by setting REFCON[1:0] to 10 (reference is always on) or 01 (reference is on, but powers down in power-down mode) in the reference control register (05h). By default, the internal voltage reference is powered down. To select the internal reference for use with the ADC, set the REFSEL[1:0] bits to 10. The REFOUT pin provides a buffered reference output voltage when the internal reference voltage is enabled. The negative reference output is the REFCOM pin, as shown in 図 52. Connect a capacitor in the range of 1 µF to 47 µF between REFOUT and REFCOM. Larger capacitor values help filter more noise at the expense of a longer reference start-up time.

The capacitor is not required if the internal reference is not used. However, the internal reference must be powered on if using the IDACs.

The internal reference requires a start-up time that must be accounted for before starting a conversion, as shown in 表 10.

表 10. Internal Reference Settling Time

REFOUT CAPACITOR	SETTLING ERROR	SETTLING TIME (ms)
1 µF	0.01%	4.5
	0.001%	5.9
10 µF	0.01%	4.9
	0.001%	6.3
47 µF	0.01%	5.5
	0.001%	7.0

9.3.3.2 External Reference

The ADS114S0x provides two external reference inputs selectable through the reference multiplexer. The reference inputs are differential with independent positive and negative inputs. REFP0 and REFN0 or REFP1 and REFN1 can be selected as the ADC reference. REFP1 and REFN1 are shared inputs with analog pins AIN6 and AIN7 in the ADS114S08.

Without buffering, the reference input impedance is approximately 250 kΩ. The reference input current can lead to possible errors from either high reference source impedance or through reference input filtering. To reduce the input current, use either internal or external reference buffers. In most applications external reference buffering is not necessary.

Connect a 100-nF bypass capacitor across the external reference input pins. Follow the specified absolute and differential reference voltage requirements.

9.3.3.3 Reference Buffers

The device has two individually selectable reference input buffers to lower the reference input current. Use the REFP_BUF and REFN_BUF bits in the reference control register (05h) to enable or disable the positive and negative reference buffers respectively. Note that these bits are active low. Writing a 1 to REFP_BUF or REFN_BUF disables the reference buffers.

The reference buffers are recommended to be disabled when the internal reference is selected for measurements. When the external reference input is at the supply voltage (REFPx at AVDD or REFNx at AVSS), the reference buffer is recomended to be disabled.

9.3.4 Clock Source

The ADS114S0x system clock is either provided by the internal low-drift 4.096-MHz oscillator or an external clock source on the CLK input. Use the CLK bit within the data rate register (04h) to select the internal 4.096-MHz oscillator or an external clock source.

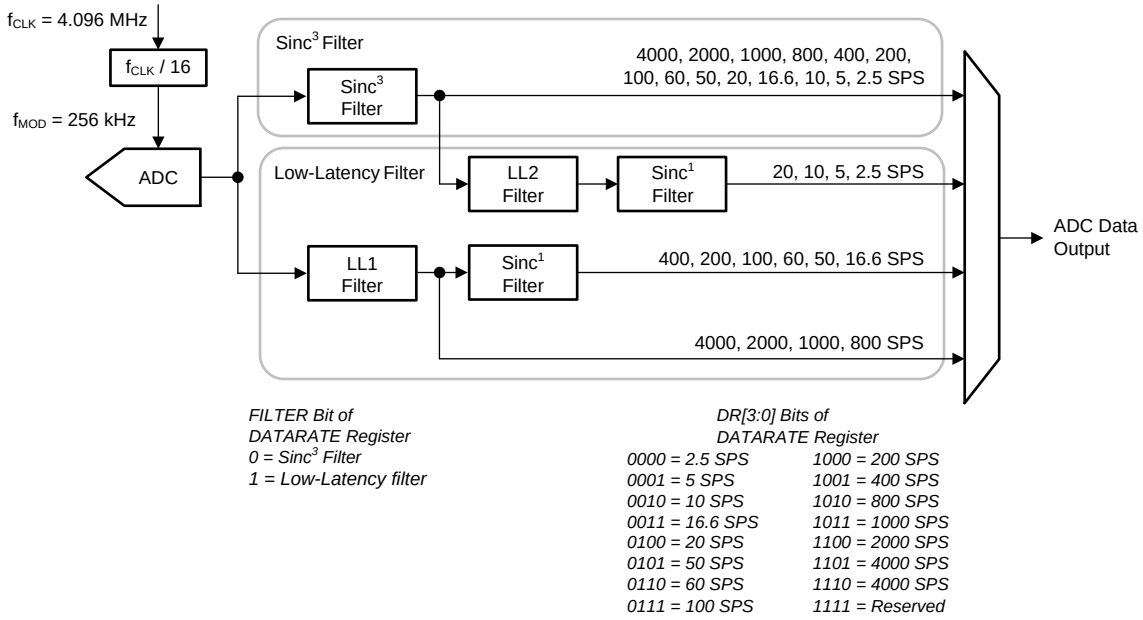
The device defaults to using the internal oscillator. If the device is reset (from either the $\overline{\text{RESET}}$ pin, or the RESET command), then the clock source returns to using the internal oscillator even if an external clock is selected.

9.3.5 Delta-Sigma Modulator

A delta-sigma ($\Delta\Sigma$) modulator is used in the devices to convert the analog input voltage into a pulse code modulated (PCM) data stream. The modulator runs at a modulator clock frequency of $f_{MOD} = f_{CLK} / 16$, where f_{CLK} is either provided by the internal 4.096-MHz oscillator or the external clock source.

9.3.6 Digital Filter

The devices offer digital filter options for both filtering and decimation of the digital data stream coming from the delta-sigma modulator. The implementation of the digital filter is determined by the data rate and filter mode setting. 図 53 shows the digital filter implementation. Choose between a third-order sinc filter ($sinc^3$) and a low-latency filter (low-latency filter with multiple components) using the FILTER bit in the data rate register (04h).



NOTE: LL filter = low-latency filter.

図 53. Digital Filter Architecture

Regardless of the FILTER type setting, the oversampling ratio is the same for each given data rate, meaning that the device requires a set number of modulator clocks to output a single ADC conversion data. The output data rate is selected using the DR[3:0] bits in the data rate register and is shown in 表 11.

表 11. ADC Data Rates and Digital Filter Oversampling Ratios

NOMINAL DATA RATE (SPS)(1)	DATA RATE REGISTER DR[3:0]	OVERSAMPLING RATIO(2)
2.5	0000	102400
5	0001	51200
10	0010	25600
16.6	0011	15360
20	0100	12800
50	0101	5120
60	0110	4264
100	0111	2560
200	1000	1280
400	1001	640
800	1010	320
1000	1011	256
2000	1100	128
4000	1101	64

(1) Valid for the internal oscillator or an external 4.096-MHz clock.
(2) The oversampling ratio is f_{MOD} divided by the data rate; $f_{MOD} = f_{CLK} / 16$.

9.3.6.1 Low-Latency Filter

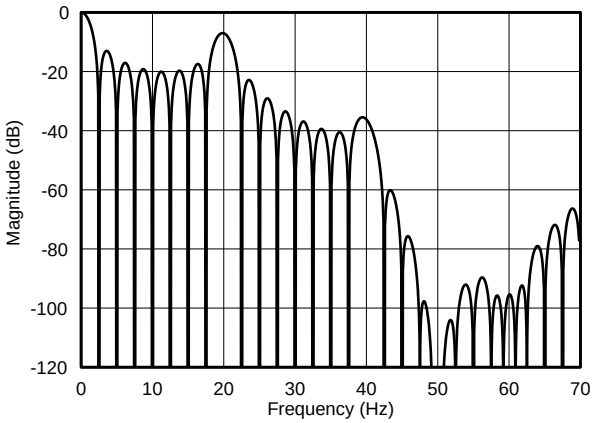
The low-latency filter is selected when the FILTER bit is set to 0 in the data rate register (04h). The filter is a finite impulse response (FIR) filter that provides settled data, given that the analog input signal has settled to the final value before the conversion is started. The low-latency filter is especially useful when multiple channels must be scanned in minimal time.

9.3.6.1.1 Low-Latency Filter Frequency Response

The low-latency filter provides many data rate options for rejecting 50-Hz and 60-Hz line cycle noise. At data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS, the filter rejects both 50-Hz and 60-Hz line frequencies. At data rates of 16.6 SPS and 50 SPS, the filter has a notch at 50 Hz. At a 60-SPS data rate, the filter has a notch at 60 Hz.

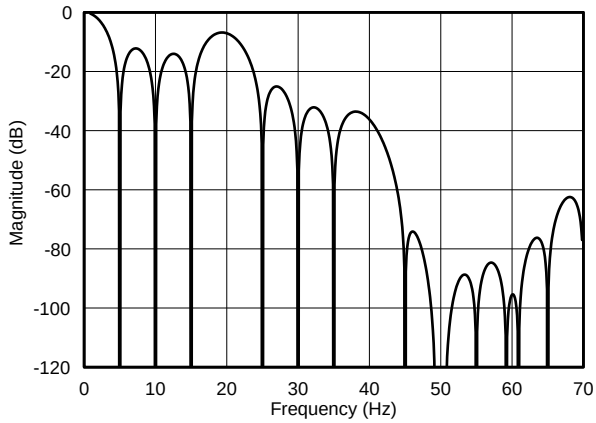
For detailed frequency response plots showing line cycle noise rejection, download the ADS1x4S0x design calculator from www.ti.com.

図 54 to 図 68 show the frequency response of the low-latency filter for different data rates. 表 12 gives the bandwidth of the low-latency filter for each data rate.



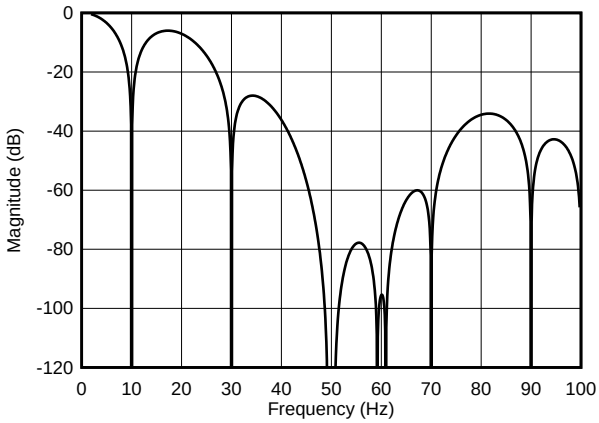
f_{CLK} = 4.096 MHz, low-latency filter

図 54. Low-Latency Filter Frequency Response, Data Rate = 2.5 SPS



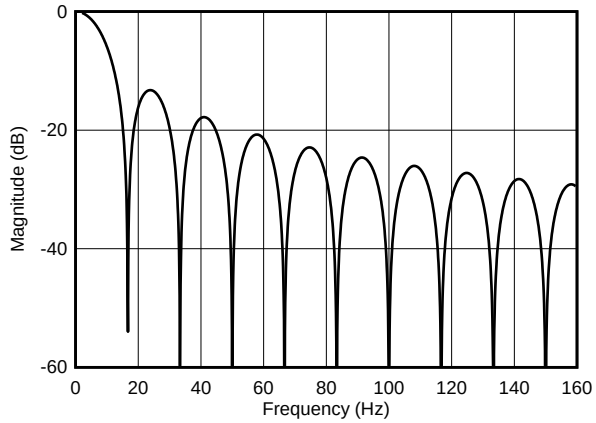
f_{CLK} = 4.096 MHz, low-latency filter

図 55. Low-Latency Filter Frequency Response, Data Rate = 5 SPS



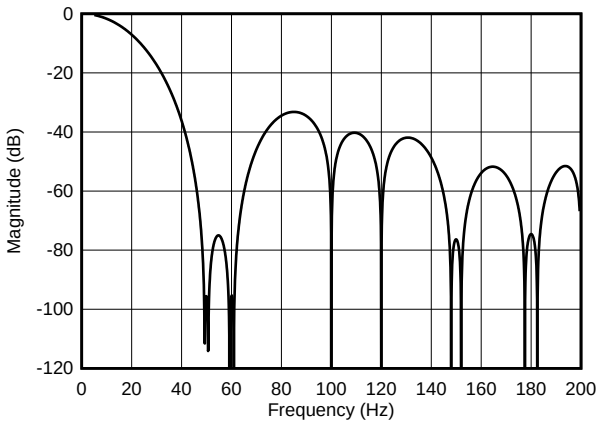
f_{CLK} = 4.096 MHz, low-latency filter

図 56. Low-Latency Filter Frequency Response, Data Rate = 10 SPS



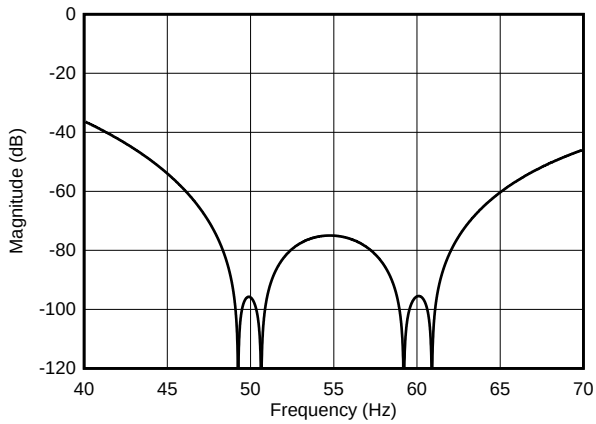
f_{CLK} = 4.096 MHz, low-latency filter

図 57. Low-Latency Filter Frequency Response, Data Rate = 16.6 SPS



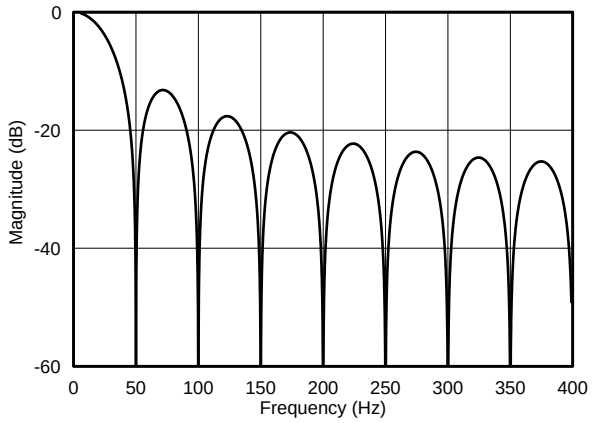
f_{CLK} = 4.096 MHz, low-latency filter

図 58. Low-Latency Filter Frequency Response, Data Rate = 20 SPS



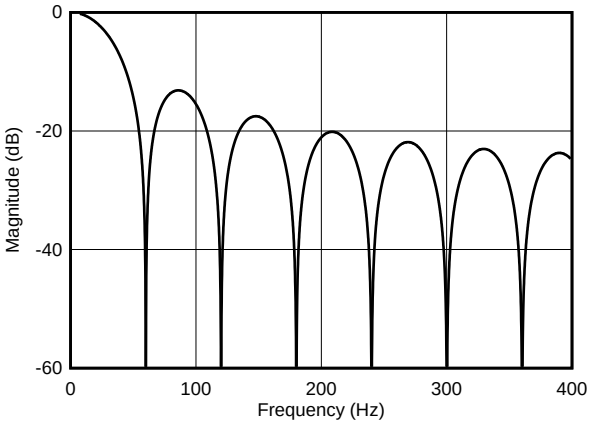
f_{CLK} = 4.096 MHz, low-latency filter

図 59. Low-Latency Filter Frequency Response, Data Rate = 20 SPS, Zoomed to 50 Hz and 60 Hz



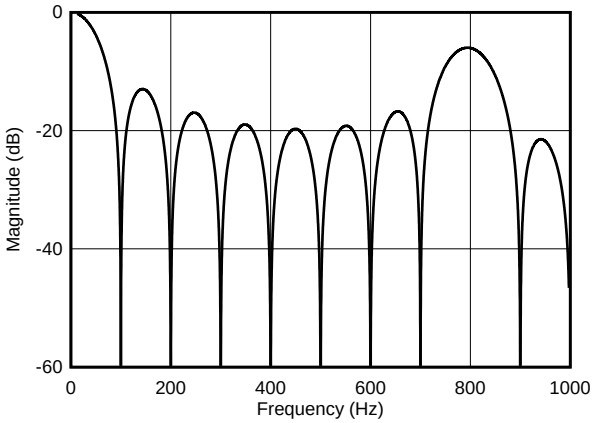
f_{CLK} = 4.096 MHz, low-latency filter

図 60. Low-Latency Filter Frequency Response, Data Rate = 50 SPS



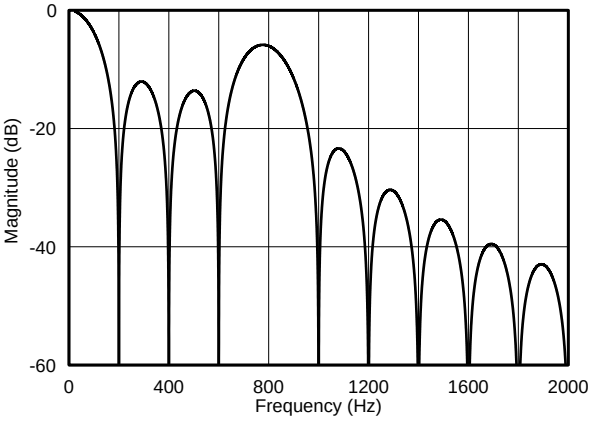
f_{CLK} = 4.096 MHz, low-latency filter

図 61. Low-Latency Filter Frequency Response, Data Rate = 60 SPS



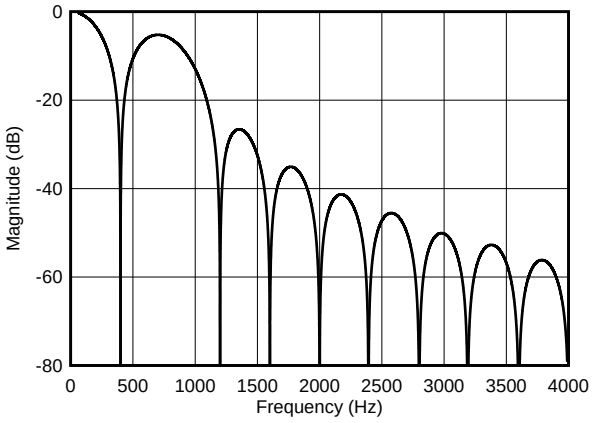
f_{CLK} = 4.096 MHz, low-latency filter

図 62. Low-Latency Filter Frequency Response, Data Rate = 100 SPS



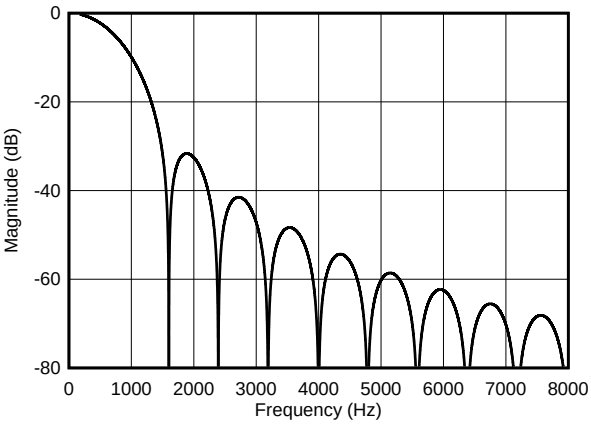
f_{CLK} = 4.096 MHz, low-latency filter

図 63. Low-Latency Filter Frequency Response, Data Rate = 200 SPS



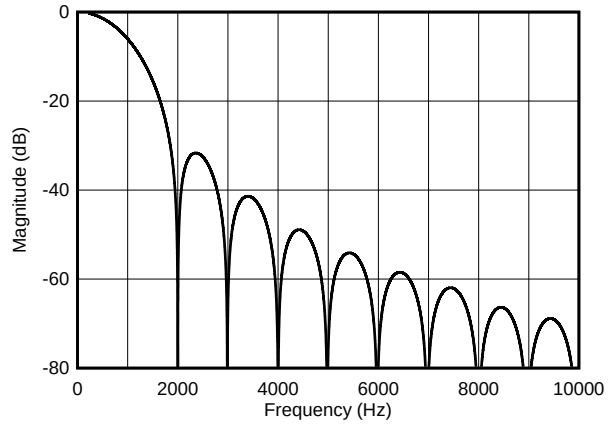
f_{CLK} = 4.096 MHz, low-latency filter

図 64. Low-Latency Filter Frequency Response, Data Rate = 400 SPS



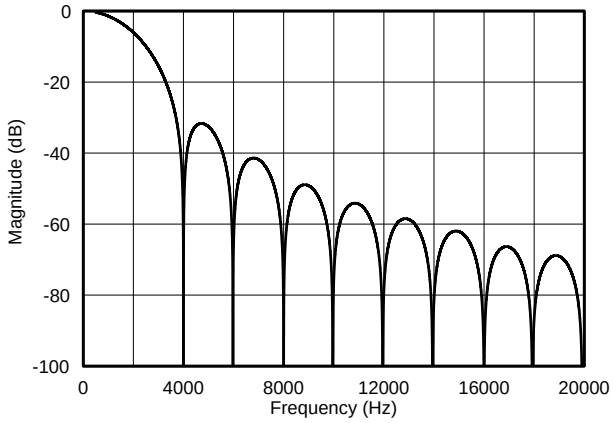
f_{CLK} = 4.096 MHz, low-latency filter

図 65. Low-Latency Filter Frequency Response, Data Rate = 800 SPS



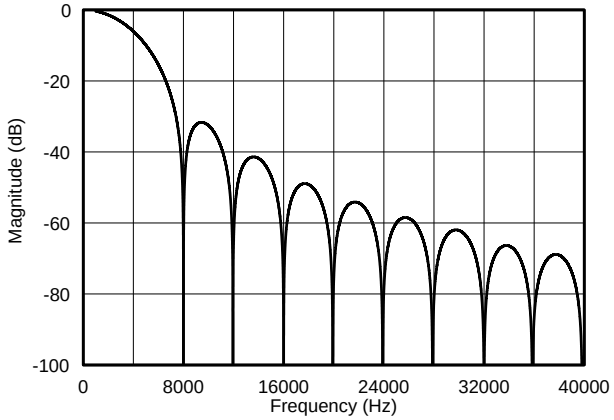
f_{CLK} = 4.096 MHz, low-latency filter

図 66. Low-Latency Filter Frequency Response, Data Rate = 1 kSPS



f_{CLK} = 4.096 MHz, low-latency filter

図 67. Low-Latency Filter Frequency Response, Data Rate = 2 kSPS



f_{CLK} = 4.096 MHz, low-latency filter

図 68. Low-Latency Filter Frequency Response, Data Rate = 4 kSPS

表 12. Low-Latency Filter Bandwidth

NOMINAL DATA RATE (SPS)(1)	–3-dB BANDWIDTH (Hz)(1)
2.5	1.1
5	2.2
10	4.7
16.6	7.4
20	13.2
50	22.1
60	26.6
100	44.4
200	89.9
400	190
800	574
1000	718
2000	718
4000	718

(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.

The low-latency filter notches and output data rate scale proportionally with the clock frequency. For example, a notch that appears at 20 Hz when using a 4.096-MHz clock appears at 10 Hz if a 2.048-MHz clock is used. Note that the internal oscillator can vary over temperature as specified in the *Electrical Characteristics* table. The data rate, conversion time, and filter notches consequently vary by the same percentage. Consider using an external precision clock source if a digital filter notch at a specific frequency with a tighter tolerance is required.

9.3.6.1.2 Data Conversion Time for the Low-Latency Filter

The amount of time required to receive data from the ADC depends on more than just the nominal data rate of the device. The data period also depends on the mode of operation and other configurations of the device. When the low-latency filter is enabled, the data settles in one data period. However, a small amount of latency exists to set up the device, calculate the conversion data from the modulator samples, and other overhead that adds time to the conversion. For this reason, the first conversion data takes longer than subsequent data conversions.

表 13 shows the conversion times for the low-latency filter for each ADC data rate and various conversion modes.

表 13. Data Conversion Time for the Low-Latency Filter

NOMINAL DATA RATE(1) (SPS)	FIRST DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE(2)		SECOND AND SUBSEQUENT CONVERSIONS FOR CONTINUOUS CONVERSION MODE	
	ms(3)	NUMBER OF t_{MOD} PERIODS(3)	ms(4)	NUMBER OF t_{MOD} PERIODS(4)
2.5	406.504	104065	400	102400
5	206.504	52865	200	51200
10	106.504	27265	100	25600
16.6	60.254	15425	60	15360
20	56.504	14465	50	12800
50	20.156	5160	20	5120
60	16.910	4329	16.66	4264
100	10.156	2600	10	2560
200	5.156	1320	5	1280
400	2.656	680	2.5	640
800	1.406	360	1.25	320
1000	1.156	296	1	256
2000	0.656	168	0.5	128
4000	0.406	104	0.25	64

(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.
(3) Time does not include the programmable delay set by the DELAY[2:0] bits in the gain setting register. The default setting is an additional $14 \cdot t_{MOD}$, where $t_{MOD} = t_{CLK} \cdot 16$.
(4) Subsequent readings in continuous conversion mode do not have the programmable delay time.

9.3.6.2 Sinc^3 Filter

The sinc^3 digital filter is selected when the FILTER bit is set to 0 in the data rate register (04h). Compared to the low-latency filter, the sinc^3 filter has improved noise performance but has a three-cycle latency in the data output.

9.3.6.2.1 Sinc^3 Filter Frequency Response

The low-pass nature of the sinc^3 filter establishes the overall frequency response. The frequency response is given by 式 8:

$$\left| H(f) \right| = \left| H_{Sinc3}(f) \right| = \left| \frac{\sin\left(\frac{16\,\pi f \cdot OSR}{f_{CLK}}\right)}{OSR \times \sin\left(\frac{16\,\pi f}{f_{CLK}}\right)} \right|^3 \quad (8)$$

where

- f = signal frequency
- f_{CLK} = ADC clock frequency
- OSR = oversampling ratio

The sinc^3 filter offers simultaneous 50-Hz and 60-Hz line cycle rejection at data rates of 2.5 SPS, 5 SPS, and 10 SPS. The sinc^3 filter offers only 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and only 60-Hz rejection at data rates of 20 SPS and 60 SPS. The sinc^3 digital filter response scales with the data rate and has notches at multiples of the data rate. 図 69 shows the sinc^3 digital filter frequency response normalized to the data rate. As an example, 図 70 shows the frequency response when the data rate is set to 10 SPS, and 図 71 illustrates a close-up of the filter rejection of 50-Hz and 60-Hz line frequencies. For more detailed frequency response plots, download the ADS1x4S0x design calculator from www.ti.com.

表 14 gives the bandwidth of the sinc^3 filter for each data rate.

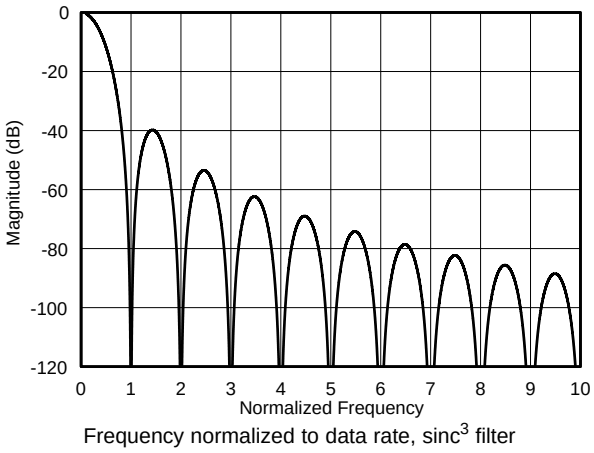


図 69. Sinc^3 Filter Frequency Response, Normalized to Data Rate

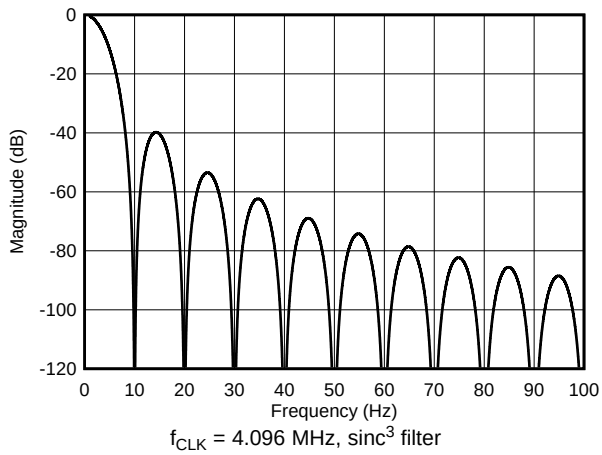


図 70. Sinc^3 Filter Frequency Response, Data Rate = 10 SPS

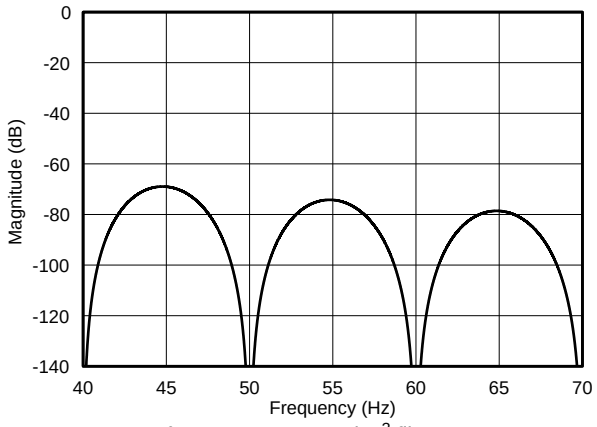


図 71. Sinc^3 Filter Frequency Response, Data Rate = 10 SPS, Zoomed to 50 Hz and 60 Hz

表 14. Sinc^3 Filter –3-dB Bandwidth

NOMINAL DATA RATE (SPS)(1)	–3-dB BANDWIDTH (Hz)(1)
2.5	0.65
5	1.3
10	2.6
16.6	4.4
20	5.2
50	13.1
60	15.7
100	26.2
200	52.3
400	105
800	209
1000	262
2000	523
4000	1046

(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.

As mentioned in the previous section, filter notches and output data rate scale proportionally with the clock frequency and the internal oscillator can change frequency with temperature.

9.3.6.2.2 Data Conversion Time for the Sinc^3 Filter

Similar to the low-latency filter, the sinc^3 filter requires different amounts of time to complete a conversion. By nature, the sinc^3 filter normally takes three conversion to settle. In both single-shot conversion mode and continuous conversion mode, the first two conversions are suppressed so that only settled data are output by the ADC.

表 15 shows the conversion times for the sinc^3 filter for each ADC data rate and various conversion modes.

表 15. Data Conversion Time for the Sinc^3 Filter

NOMINAL DATA RATE(1) (SPS)	FIRST DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE(2)		SECOND AND SUBSEQUENT CONVERSIONS FOR CONTINUOUS CONVERSION MODE	
	ms(3)	NUMBER OF t_{MOD} PERIODS(3)	ms(4)	NUMBER OF t_{MOD} PERIODS(4)
2.5	1200.254	307265	400	102400
5	600.254	153665	200	51200
10	300.254	76865	100	25600
16.6	180.254	46145	60	15360
20	150.254	38465	50	12800
50	60.254	15425	20	5120
60	50.223	12857	16.66	4264
100	30.254	7745	10	2560
200	15.254	3905	5	1280
400	7.754	1985	2.5	640
800	4.004	1025	1.25	320
1000	3.156	808	1	256
2000	1.656	424	0.5	128
4000	0.906	232	0.25	64

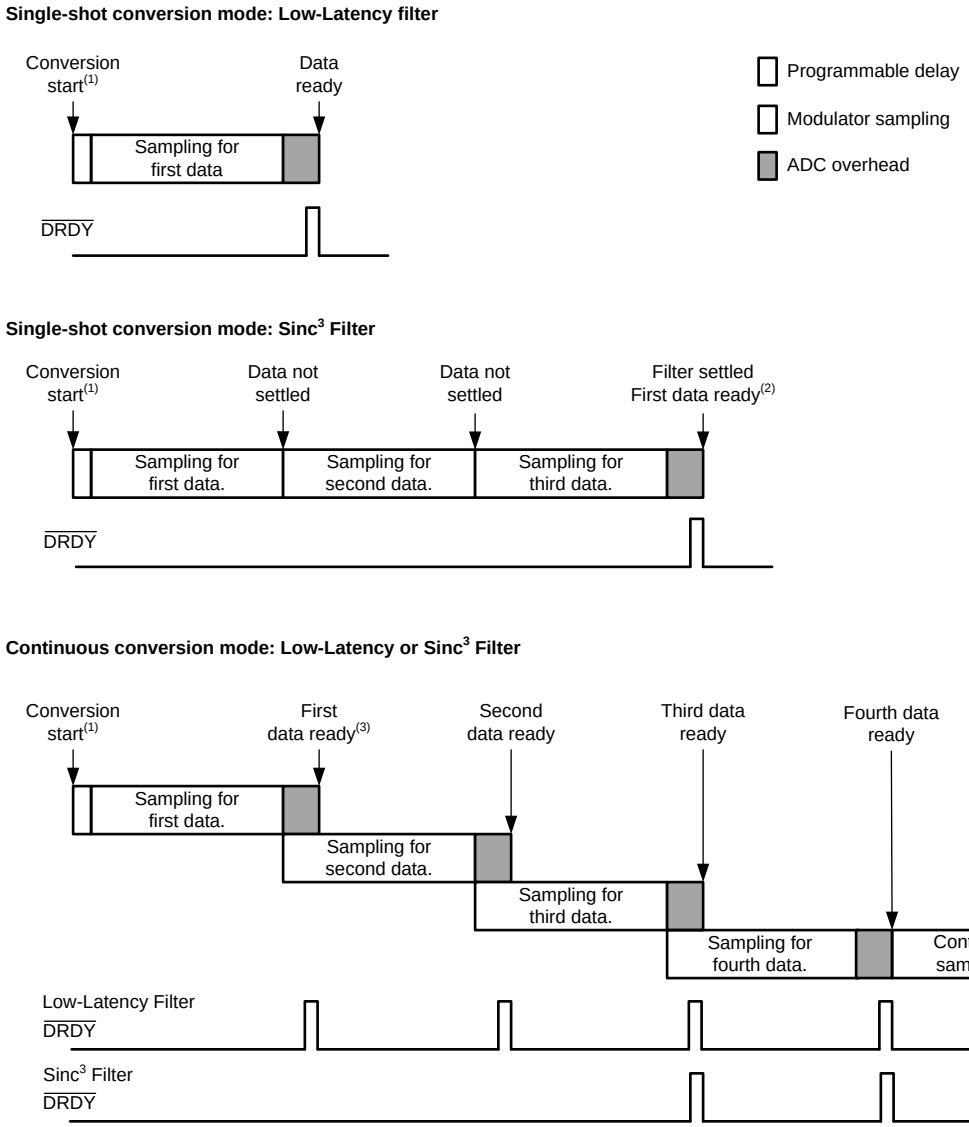
(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.
(3) Time does not include the programmable delay set by the DELAY[2:0] bits in the gain setting register. The default setting is an additional $14 \cdot t_{MOD}$, where $t_{MOD} = t_{CLK} \cdot 16$.
(4) Subsequent readings in continuous conversion mode do not have the programmable delay time.

9.3.6.3 Note on Conversion Time

Each data period consists of time required for the modulator to sample the analog inputs. However, there is additional time required before the samples become an ADC conversion result. First, there is a programmable conversion delay (described in the *Programmable Conversion Delay* section) that is added before the conversion starts. This delay allows for additional settling time for input filtering on the analog inputs and for the antialiasing filter after the PGA. The default programmable conversion delay is $14 \cdot t_{MOD}$. Also, overhead time is needed to convert the modulator samples into an ADC conversion result. This overhead time includes any necessary offset or gain compensation after the digital filter accumulates a data result.

The first conversion when the device is in continuous conversion mode (just as in single-shot conversion mode) includes the programmable conversion delay, the modulator sampling time, and the overhead time. The second and subsequent conversions are the normal data period (period as given by the inverse of the data rate).

図 72 shows the time sequence for the ADC in both continuous conversion and single-shot conversion modes. The sequence is the same regardless of the filter setting. However, when the low-latency filter settles for each data, the sinc^3 filter does not settle until the third data.



(1) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.

(2) In sinc^3 filter mode, the first two data outputs are suppressed to allow for the measurement data to settle.

(3) In sinc^3 filter mode, there is no overhead time for the first two data, which are not available to be read.

図 72. Single-Shot Conversion Mode and Continuous Conversion Mode Sequences

9.3.6.4 50-Hz and 60-Hz Line Cycle Rejection

If the ADC connection leads are in close proximity to industrial motors and conductors, coupling of 50-Hz and 60-Hz power line frequencies can occur. The coupled noise interferes with the signal voltage, and can lead to inaccurate or unstable conversions. The digital filter provides enhanced rejection of power-line-coupled noise for data rates of 60 SPS and less. Program the filter to tradeoff data rate and conversion latency versus the desired level of line cycle rejection. 表 16 and 表 17 summarize the ADC 50-Hz and 60-Hz line-cycle rejection based on ±1-Hz and ±2-Hz tolerance of power-line to ADC clock frequency. The best possible power-line rejection is provided by using an accurate ADC clock.

表 16. Low-Latency Filter, 50-Hz and 60-Hz Line Cycle Rejection

DATA RATE (SPS)(1)	LOW-LATENCY DIGITAL FILTER LINE CYCLE REJECTION (dB)			
	50 Hz ± 1 Hz	60 Hz ± 1 Hz	50 Hz ± 2 Hz	60 Hz ± 2 Hz
2.5	–113.7	–95.4	–97.7	–92.4
5	–111.9	–95.4	–87.6	–81.8
10	–111.5	–95.4	–85.7	–81.0
16.6	–33.8	–20.9	–27.8	–20.8
20	–95.4	–95.4	–75.5	–80.5
50	–33.8	–15.5	–27.6	–15.1
60	–13.4	–35.0	–12.6	–29.0

(1) f_{CLK} = 4.096 MHz.

表 17. Sinc^3 Filter, 50-Hz and 60-Hz Line Cycle Rejection

DATA RATE (SPS)(1)	SINC^3 DIGITAL FILTER LINE CYCLE REJECTION (dB)			
	50 Hz ± 1 Hz	60 Hz ± 1 Hz	50 Hz ± 2 Hz	60 Hz ± 2 Hz
2.5	–108.7	–113.4	–107.2	–112.1
5	–103.2	–107.8	–90.1	–95.0
10	–101.8	–106.4	–84.6	–89.4
16.6	–101.6	–63.0	–83.4	–62.4
20	–53.5	–106.1	–53.5	–88.0
50	–101.4	–46.7	–82.9	–45.3
60	–40.3	–105.1	–37.8	–87.2

(1) f_{CLK} = 4.096 MHz.

9.3.6.5 Global Chop Mode

The device uses a very low-drift PGA and modulator in order to provide very low input voltage offset drift. However, a small amount of offset voltage drift sometimes remains in normal measurement. The ADC incorporates a global chop option to reduce the offset voltage and offset voltage drift to very low levels. When the global chop is enabled, the ADC performs two internal conversions to cancel the input offset voltage. The first conversion is taken with normal input polarity. The ADC reverses the internal input polarity for a second conversion. The average of the two conversions yields the final corrected result, removing the offset voltage. The global chop mode is enabled using the G_CHOP bit in the data rate register (04h). 図 73 shows a block diagram of the global chop implementation. The combined PGA and ADC internal offset voltage is modeled as V_{OFS}.

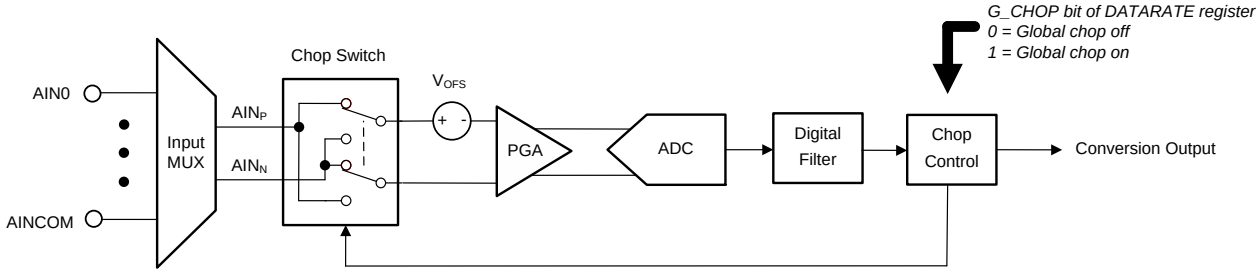


図 73. ADC Global Chop Block Diagram

The first conversion result is available after the ADC takes two separate conversions with settled data. When using the low-latency filter, data settles in a single conversion. When the global chop mode is enabled, the first conversion result appears after a time period of approximately two conversions. When using the $sinc^3$ filter, data settles in three conversions. If the global chop mode is enabled, the first conversion result appears after a time period of approximately six conversions.

In continuous conversion mode with the global chop mode enabled, subsequent conversions complete in half the time as the first conversion completed. Data for alternating inputs are pipelined so that averaging appears on each ADC data cycle. Conversion times using the global chop mode are given in 表 18 and 表 19.

表 18. Data Conversion Time for Global Chop Mode Using the Low-Latency Filter

NOMINAL DATA RATE(1) (SPS)	FIRST DATA CONVERSION PERIOD FOR GLOBAL CHOP MODE(2)		SECOND AND SUBSEQUENT CONVERSION PERIODS FOR GLOBAL CHOP MODE	
	ms(3)	NUMBER OF t_{MOD} PERIODS(3)	ms(3)	NUMBER OF t_{MOD} PERIODS(3)
2.5	813.008	208130	406.504	104065
5	413.008	105730	206.504	52865
10	213.008	54530	106.504	27265
16.66	120.508	30850	60.254	15425
20	113.008	28930	56.504	14465
50	40.313	10320	20.156	5160
60	33.820	8658	16.910	4329
100	20.313	5200	10.156	2600
200	10.313	2640	5.156	1320
400	5.313	1360	2.656	680
800	2.813	720	1.406	360
1000	2.313	592	1.156	296
2000	1.313	336	0.656	168
4000	0.813	208	0.406	104

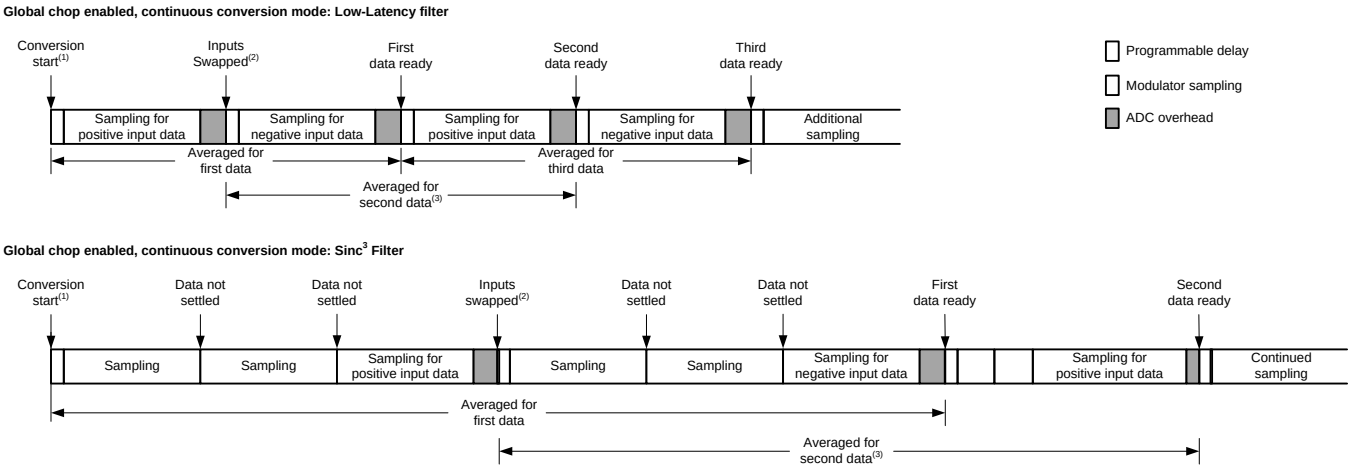
(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.
(3) Time does not include the programmable delay set by the DELAY[2:0] bits in the gain setting register. Global chop mode requires two conversions, doubling the additional time. The default setting adds an extra 28 · t_{MOD} (where $t_{MOD} = t_{CLK} \cdot 16$) to this column.

表 19. Data Conversion Time for Global Chop Mode Using the Sinc^3 Filter

NOMINAL DATA RATE(1) (SPS)	FIRST DATA CONVERSION PERIOD FOR GLOBAL CHOP MODE(2)		SECOND AND SUBSEQUENT CONVERSION PERIODS FOR GLOBAL CHOP MODE	
	ms(3)	NUMBER OF t_{MOD} PERIODS(3)	ms(3)	NUMBER OF t_{MOD} PERIODS(3)
2.5	2400.508	614530	1200.254	307265
5	1200.508	307330	600.254	153665
10	600.508	153730	300.254	76865
16.66	360.508	92290	180.254	46145
20	300.508	76930	150.254	38465
50	120.508	30850	60.254	15425
60	100.445	25714	50.223	12857
100	60.508	15490	30.254	7745
200	30.508	7810	15.254	3905
400	15.508	3970	7.754	1985
800	8.008	2050	4.004	1025
1000	6.313	1616	3.156	808
2000	3.313	848	1.656	424
4000	1.813	464	0.906	232

(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.
(3) Time does not include the programmable delay set by the DELAY[2:0] bits in the gain setting register. Global chop mode requires two conversions, doubling the additional time. The default setting adds an extra 28 · t_{MOD} (where t_{MOD} = t_{CLK} · 16) to this column.

In global chop mode, sequences are similar to taking consecutive single-shot conversions and swapping the input on each conversion. Output data are averaged using the last two data read operations by the ADC with the inputs swapped. 図 74 shows the time sequence for the ADC using global chop mode.



(1) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.
(2) When the first data are collected, the inputs are swapped.
(3) Measurements are averaged after the inputs are swapped for each conversion.

図 74. Global Chop Enabled Conversion Mode Sequences

Because the digital filter must settle after reversing the inputs, the global chop mode data rate is less than the nominal data rate, depending on the digital filter and programmed settling delay. However, if the data rate in use has 50-Hz and 60-Hz frequency response notches, the null frequencies remain unchanged.

The global chop mode also reduces the ADC noise by a factor of $\sqrt{2}$ because two conversions are averaged. In some cases, the programmable conversion delay must be increased, DELAY[2:0] in the gain setting register (03h), to allow for settling of external components.

9.3.7 Excitation Current Sources (IDACs)

The ADS114S0x incorporates two integrated, matched current sources (IDAC1, IDAC2). The current sources provide excitation current to resistive temperature devices (RTDs), thermistors, diodes, and other resistive sensors that require constant current biasing. The current sources are programmable to output values between 10 μA to 2000 μA using the IMAG[3:0] bits in the excitation current register 1 (06h). Each current source can be connected to any of the analog inputs AINx as well as the REFP1 and REFN1 inputs for the ADS114S06. Both current sources can also be connected to the same pin. The routing of the IDACs is configured by the I1MUX[3:0] and I2MUX[3:0] bits in the excitation current register 2 (07h). In three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *Typical Application* section for more details). 図 75 details the IDAC connection through the input multiplexer.

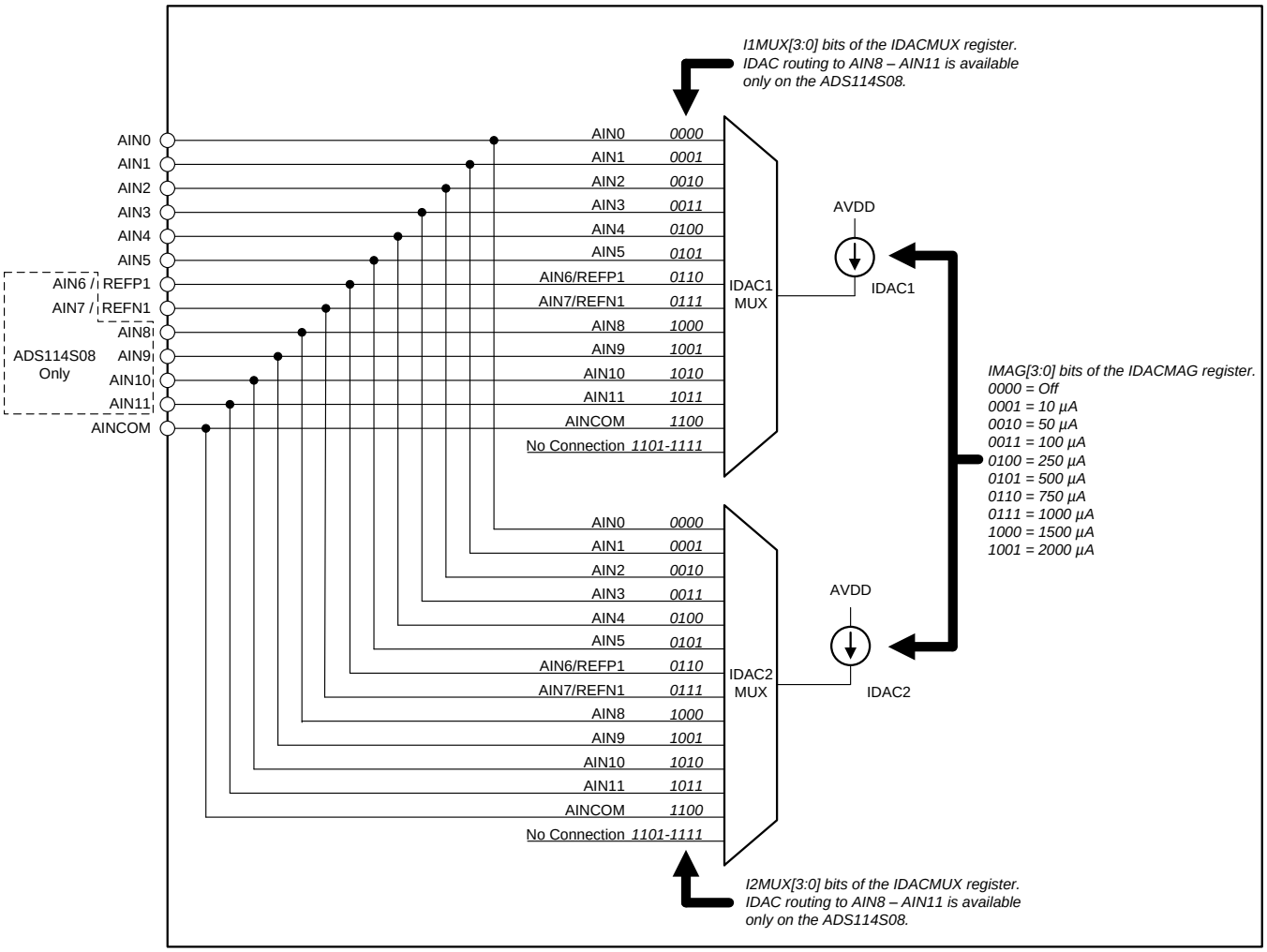


図 75. IDAC Block Diagram

The internal reference must be enabled for IDAC operation. As a current source, the IDAC requires voltage headroom to the positive supply to operate. This voltage headroom is the compliance voltage. When driving resistive sensors and biasing resistors, take care not to exceed the compliance voltage of the IDACs, otherwise the specified accuracy of the IDAC current may not be met. For IDAC compliance voltage specifications, see the *Electrical Characteristics* table.

9.3.8 Bias Voltage Generation

The ADS114S0x provides an internal bias voltage generator, VBIAS, that can be set to two different levels, (AVDD + AVSS) / 2 and (AVDD + AVSS) / 12 by using the VB_LEVEL bit in the sensor biasing register (08h). The bias voltage is internally buffered and can be established on the analog inputs AIN0 to AIN5 and AINCOM using the VB_AINx bits in the sensor biasing register (08h). A typical use case for VBIAS is biasing unbiased thermocouples to within the common-mode voltage range of the PGA. A block diagram of the VBIAS voltage generator and connection diagram is shown in 図 76.

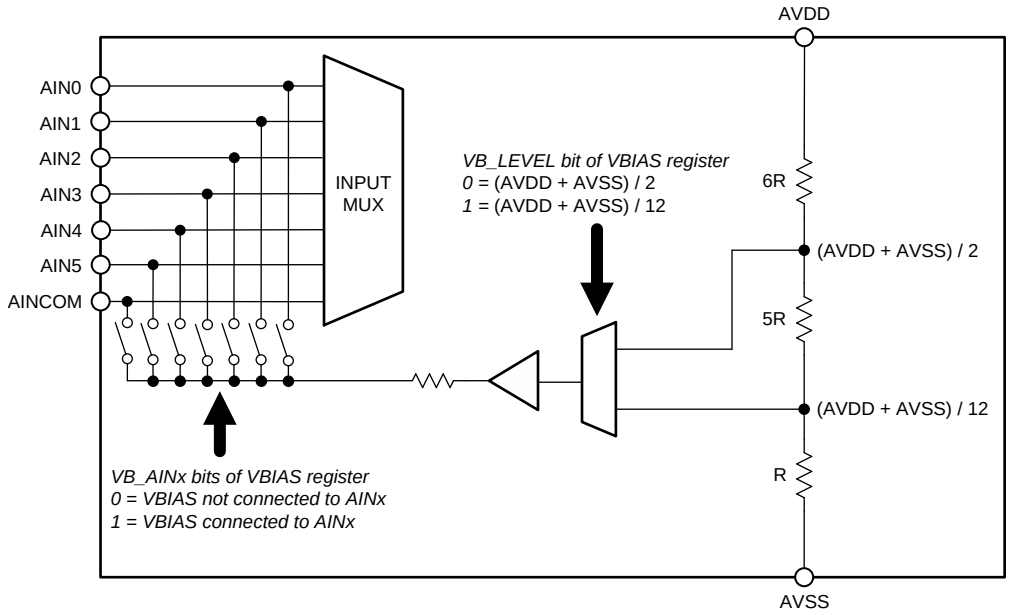


図 76. VBIAS Block Diagram

The start-up time of the VBIAS voltage depends on the pin load capacitance. The total capacitance includes any capacitance connected from VBIAS to AVDD, AVSS, and ground. 表 20 lists the VBIAS voltage settling times for various external load capacitances. Ensure the VBIAS voltage is fully settled before starting a conversion.

表 20. VBIAS Settling Time

LOAD CAPACITANCE	SETTLING TIME
0.1 µF	280 µs
1 µF	2.8 ms
10 µF	28 ms

9.3.9 System Monitor

The ADS114S0x provides a set of system monitor functions. These functions measure the device temperature, analog power supply, digital power supply, or use current sources to detect sensor malfunction. System monitor functions are enabled through the SYS_MON[2:0] bits of the system control register (09h).

9.3.9.1 Internal Temperature Sensor

On-chip diodes provide temperature-sensing capability. Enable the internal temperature sensor by setting SYS_MON[2:0] = 010 in the system control register (09h). The temperature sensor outputs a voltage proportional to the device temperature as specified in the *Electrical Characteristics* table.

When measuring the internal temperature sensor, the analog inputs are disconnected from the ADC and the output voltage of the temperature sensor is routed to the ADC for measurement using the selected PGA gain, data rate, and voltage reference. If enabled, PGA gain must be limited to 4 for the temperature sensor measurement to remain within the allowed absolute input voltage range of the PGA. As a result of the low device junction-to-PCB thermal resistance ($R_{\theta JB}$), the internal device temperature closely tracks the printed circuit board (PCB) temperature.

9.3.9.2 Power Supply Monitors

The ADS114S0x provides a means for monitoring both the analog and digital power supply (AVDD and DVDD). The power-supply voltages are divided by a resistor network to reduce the voltages to within the ADC input range. The reduced power-supply voltage is routed to the ADC input multiplexer. The analog (V_{ANLMON}) and digital (V_{DIGMON}) power-supply readings are scaled by 式 9 and 式 10, respectively:

$$V_{ANLMON} = (AVDD – AVSS) / 4 \quad (9)$$

$$V_{DIGMON} = (DVDD – DGND) / 4 \quad (10)$$

Enable the supply voltage monitors using the SYS_MON[2:0] bits in the system control register (09h). Setting SYS_MON[2:0] to 011 measures V_{ANLMON}, and setting SYS_MON[2:0] to 100 measures V_{DIGMON}.

When the supply voltage monitor is enabled, the analog inputs are disconnected from the ADC and the PGA gain is set to 1, regardless of the GAIN[2:0] bit values in the gain setting register (03h). Supply voltage monitor measurements can be done with either the PGA enabled or PGA disabled via the PGA_EN[1:0] register. To obtain valid power supply monitor readings, the reference voltage must be larger than the power-supply measurements shown in 式 9 and 式 10.

9.3.9.3 Burn-Out Current Sources

To help detect a possible sensor malfunction, the ADS114S0x provides selectable current sources to function as burn-out current sources (BOCS) using the SYS_MON[2:0] bits in the system control register (09h). Current sources are set to values of 0.2 µA, 1 µA, and 10 µA with SYS_MON[2:0] settings of 101, 110, and 111, respectively.

When enabled, one BOCS sources current to the selected positive analog input (AIN_P) and the other BOCS sinks current from the selected negative analog input (AIN_N). With an open-circuit in a burned out sensor, these BOCSs pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading can indicate a shorted sensor. Distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. The voltage drop across the external filter resistance and the residual resistance of the multiplexer can cause the output to read a value higher than zero.

The ADC readings of a functional sensor can be corrupted when the burn-out current sources are enabled. The burn-out current sources are recommended to be disabled when performing the precision measurement, and only enabling them to test for sensor fault conditions. If the global chop mode is enabled, disable this mode before making a measurement with the burn-out current sources.

9.3.10 Status Register

The ADS114S0x has a one-byte status register that contains flags to indicate if a fault condition has occurred. This byte can be read out from the status register (01h), or can be prepended to each data read as the first byte when reading data from the ADC. To prepend the STATUS byte to each conversion result, set the SENDSTAT bit to 1 in the system control register (09h).

The STATUS byte data field and field description are found in 図 94 and 表 27. The following sections describe various flagged fault conditions that are indicated in the STATUS byte.

Flags for the PGA output voltage rail monitors and reference monitor are set after each conversion. Reading the STATUS byte reads the flags latched during the last conversion cycle.

9.3.10.1 POR Flag

After the power supplies are turned on, the ADC remains in reset until DVDD, IOVDD, and the analog power supply (AVDD – AVSS) voltage exceed the respective power-on reset (POR) voltage thresholds. If a POR event has occurred, the FL_POR flag (bit 7 of the STATUS byte) is set. This flag indicates that a POR event has occurred and has not been cleared. This flag is cleared with a user register write to set the bit to 0. The power-on reset is described further in the *Power-On Reset* section.

9.3.10.2 $\overline{RDY}$ Flag

The $\overline{RDY}$ flag indicates that the device has started up and is ready to receive a configuration change. During a reset or POR event, the device is resetting the register map and may not be available. The $\overline{RDY}$ flag is shown with bit 6 of the STATUS byte.

9.3.10.3 PGA Output Voltage Rail Monitors

The PGA contains an integrated output-voltage monitor. If the level of the PGA output voltage exceeds AVDD – 0.15 V or drops below AVSS + 0.15 V, a flag is set to indicate that the output has gone beyond the output range of the PGA. Each PGA output V_{OUTN} and V_{OUTP} can trigger an overvoltage or undervoltage flag, giving a total of four flags. The PGA output voltage rail monitors are enabled with the FL_REF_EN bit of excitation current register 1. The PGA output voltage rail monitor block diagram is shown in 図 77. If the PGA is bypassed, then the rail monitor is still operational and is sensing the connection at the input of the ADC.

The PGA output voltage rail monitors are:

- FL_P_RAILP (bit 5 of the STATUS byte): V_{OUTP} has exceeded AVDD – 0.15 V
- FL_P_RAILN (bit 4 of the STATUS byte): V_{OUTP} dropped below AVSS + 0.15 V
- FL_N_RAILP (bit 3 of the STATUS byte): V_{OUTN} has exceeded AVDD – 0.15 V
- FL_N_RAILN (bit 2 of the STATUS byte): V_{OUTN} dropped below AVSS + 0.15 V

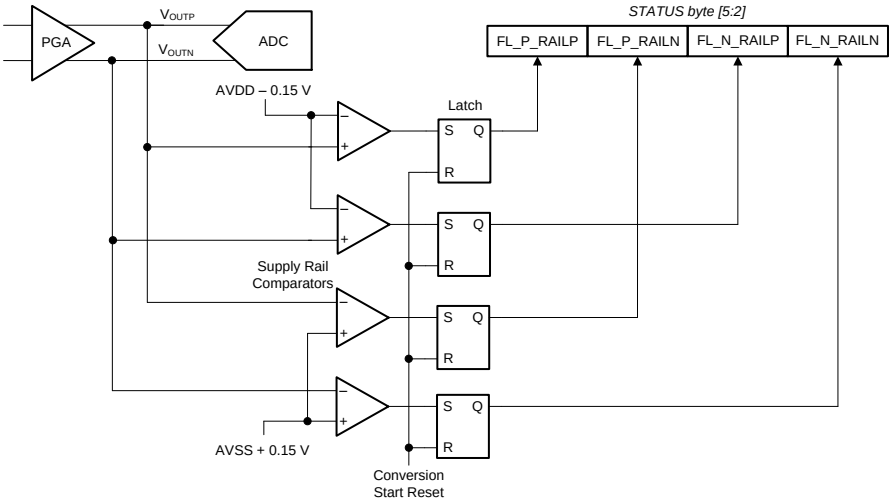


図 77. PGA Output Voltage Rail Monitors

図 78 shows an example of a PGA output voltage rail monitor overrange event and the respective behavior of the flags. A fault is latched during a conversion cycle. The flags are updated (set or cleared) only at the end of a conversion cycle.

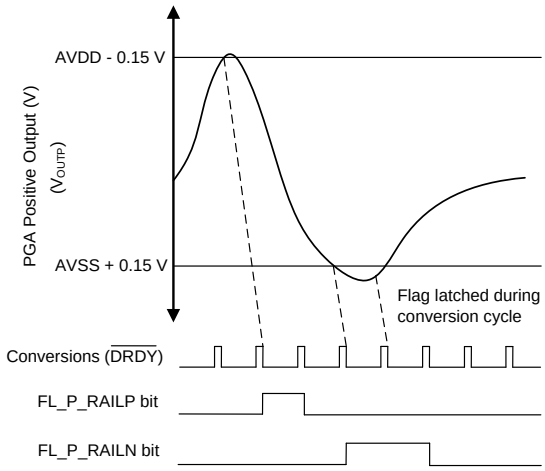


図 78. PGA Output Voltage Rail Monitor Timing

9.3.10.4 Reference Monitor

The user can select to continuously monitor the ADC reference inputs for a shorted or missing reference voltage. The reference detection circuit offers two thresholds, the first threshold is 300 mV and the second threshold is 1/3 · (AVDD – AVSS). The reference detection circuit measures the differential reference voltage and sets a flag latched after each conversion in the STATUS byte if the voltage is below the threshold. A reference voltage less than 300 mV can indicate a potential short on the reference inputs or, in case of a ratiometric RTD measurement, a broken wire between the RTD and the reference resistor. A reference voltage between 300 mV and 1/3 · (AVDD – AVSS) can indicate a broken sensor excitation wire in a 3-wire RTD setup.

Additionally, a resistor of 10 MΩ can be connected between the selected REFPx and REFNx inputs. The resistor can be used to detect a floating reference input. With a floating input, the resistor pulls both reference inputs to the same potential so that the reference detection circuit can detect this condition. The pull-together reference resistor is not recommended to be continuously connected to active reference inputs. This resistor lowers the input impedance of the reference inputs and can contribute gain error to the measurement.

The reference detection circuits must be enabled with the FL_REF_EN[1:0] bits of the reference control register (05h). The FL_REF_L0 flag (bit 0 of the STATUS byte) indicates if the reference voltage is lower than 0.3 V. The FL_REF_L1 flag (bit 1 of the STATUS byte) indicates if the reference voltage is lower than 1/3 · (AVDD – AVSS). A diagram of the reference detection circuit is shown in 図 79. A reference monitor fault is latched at each conversion cycle and the flags in the status register are updated at the falling edge of $\overline{DRDY}$.

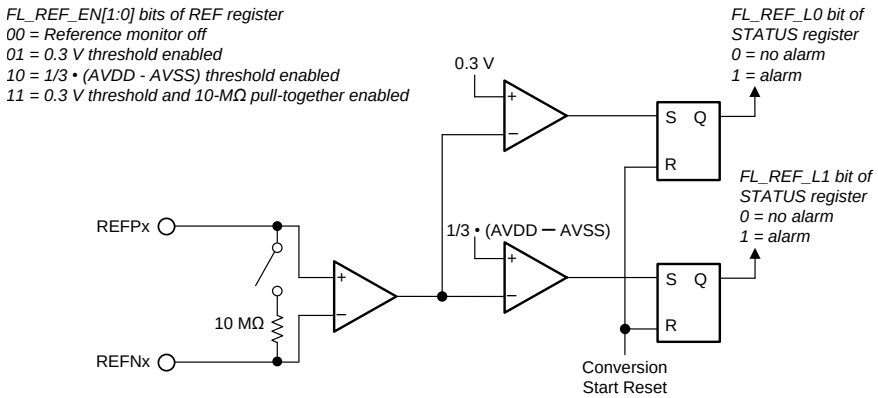


図 79. Reference Monitor Block Diagram

9.3.11 General-Purpose Inputs and Outputs (GPIOs)

The ADS114S06 offers four dedicated general-purpose input and output (GPIO) pins, and the ADS114S08 offers four pins (AIN8 to AIN11) that serve a dual purpose as either analog inputs or GPIOs.

Two registers control the function of the GPIO pins. Use the CON[3:0] bits of the GPIO configuration register (11h) to configure a pin as a GPIO pin. The upper four bits (DIR[3:0]) of the GPIO data register (10h) configure the GPIO pin as either an input or an output. The lower four bits (DAT[3:0]) of the GPIO data register contain the input or output GPIO data. If a GPIO pin is configured as an input, the respective DAT[x] bit reads the status of the pin; if a GPIO pin is configured as an output, write the output status to the respective DAT[x] bit. For more information about the use of GPIO pins, see the *Configuration Registers* section.

図 80 shows a diagram of how these functions are combined onto a single pin. Note that when the pin is configured as a GPIO, the corresponding logic is powered from AVDD and AVSS. When the devices are operated with bipolar analog supplies, the GPIO outputs bipolar voltages. Care must be taken to not load the GPIO pins when used as outputs because large currents can cause droop or noise on the analog supplies. GPIO pins use Schmitt triggered inputs, with hysteresis to make the input more resistance to noise; see the *Electrical Characteristics* table for GPIO thresholds.

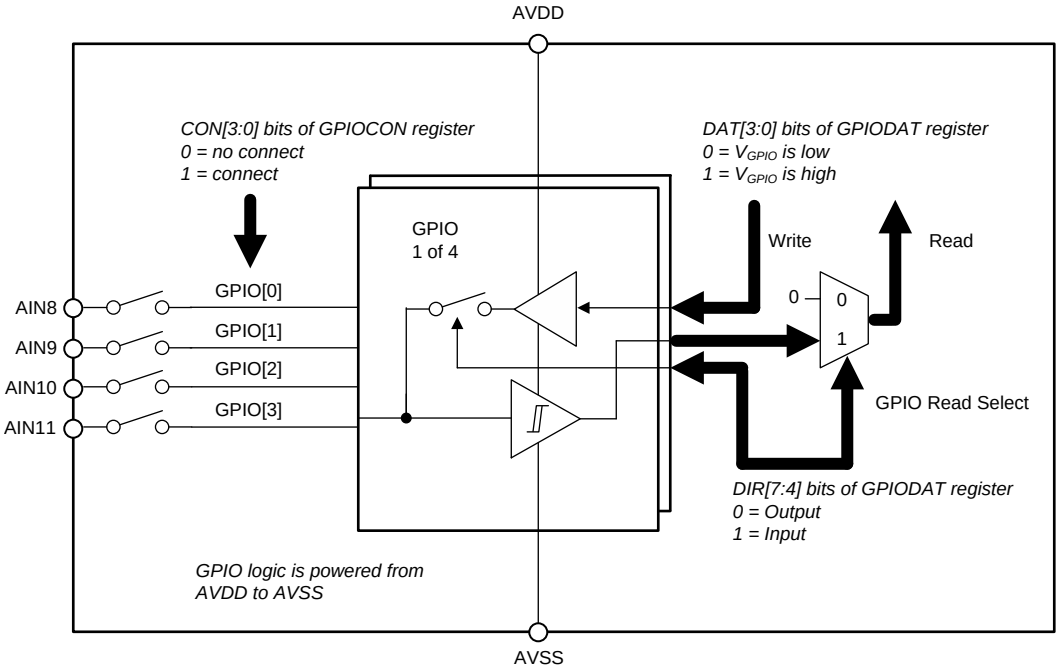


図 80. GPIO Block Diagram

For connections of unused GPIO pins, see the *Unused Inputs and Outputs* section.

9.3.12 Low-Side Power Switch

A low-side power switch with low on-resistance connected between REFN0 and AVSS-SW is integrated in the devices. This power switch can be used to reduce system power consumption in resistive bridge sensor applications by powering down the bridge circuit between conversions. When the PSW bit in the excitation current register 1 (06h) is set to 1, the switch closes. The switch automatically opens when the POWERDOWN command is issued. The switch is opened by setting the PSW bit to 0. By default, the switch is open. Connect AVSS-SW to AVSS.

9.3.13 Cyclic Redundancy Check (CRC)

A cyclic redundancy check (CRC) is enabled by setting the CRC bit to 1 in the system control register (10h). When CRC mode is enabled, the 8-bit CRC is appended to the conversion result. The CRC is calculated for the 16-bit conversion result and the STATUS byte when enabled.

In CRC mode, the checksum byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) of the data bytes by a CRC polynomial. For conversion data, use three data bytes. The CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X + 1$.

The nine binary coefficients of the polynomial are: 100000111. To calculate the CRC, divide (XOR operation) the data bytes (excluding the CRC) with the polynomial and compare the calculated CRC values to the ADC CRC value. If the values do not match, a data transmission error has occurred. In the event of a data transmission error, read the data again.

The following list shows a general procedure to compute the CRC value:

1. Left-shift the initial 16-bit data value (24-bit data when the STATUS byte is enabled) by 8 bits, with zeros padded to the right, creating a new 24-bit data value (the starting data value).
2. Align the MSB of the CRC polynomial (100000111) to the left-most, logic-one value of the data.
3. Perform an XOR operation on the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter-length value. The bits of the data values that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result.
4. When the XOR result is less than 100000000, the procedure ends, yielding the 8-bit CRC value. Otherwise, continue with the XOR operation shown in step 2, using the current data value. The number of loop iterations depends on the value of the initial data.

9.3.14 Calibration

The ADC incorporates offset and gain calibration commands, as well as user-offset and full-scale (gain) calibration registers to calibrate the ADC. The ADC calibration registers are 16 bits wide. Use calibration to correct internal ADC errors or overall system errors. Calibrate by sending calibration commands to the ADC, or by direct user calibration. In user calibration, the user calculates and writes the correction values to the calibration registers. The ADC performs self or system-offset calibration, or a system gain calibration. Perform offset calibration before system gain calibration. After power-on, wait for the power supplies and reference voltage to fully settle before calibrating.

As shown in 図 81, the value of the offset calibration register is subtracted from the filter output and then multiplied by the full-scale register value divided by 4000h. The data are then clipped to a 16-bit value to provide the final output.

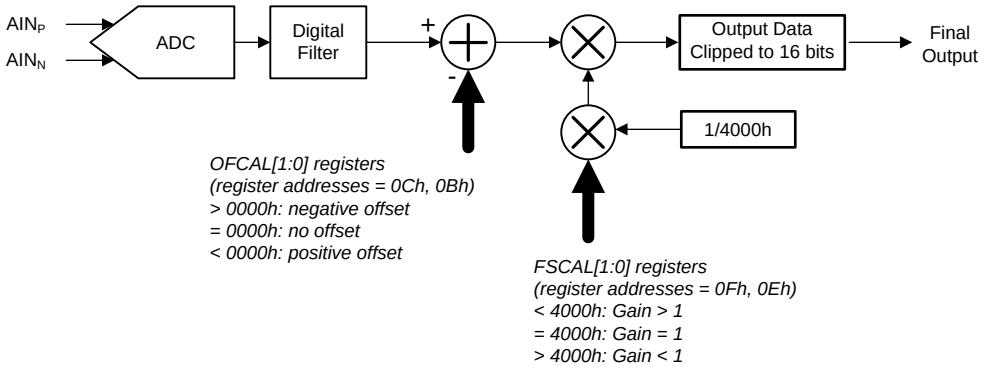


図 81. ADC Calibration Block Diagram

Calibration commands cannot be used when the device is in standby mode (when the START/SYNC pin is low, or when the STOP command is issued).

9.3.14.1 Offset Calibration

The offset calibration word is 16 bits, consisting of two 8-bit registers, as shown in the two registers starting with offset calibration register 1. The offset value is twos complement format with a maximum positive value equal to 7FFFh, and a maximum negative value equal to 8000h. This value is subtracted from each output reading as an offset correction. A register value equal to 0000h has no offset correction. If global chop mode is enabled, the offset calibration register is disabled. 表 21 shows example settings of the offset register.

表 21. Offset Calibration Register Values

OFC REGISTER VALUE	OFFSET CALIBRATED OUTPUT CODE(1)
0001h	FFFFh
0000h	0000h
FFFFh	0001h

(1) Ideal output code with shorted input, excluding ADC noise and offset voltage error.

The user can select how many samples (1, 4, 8, or 16) to average for self or system offset calibration using the CAL_SAMP[1:0] bits in the system control register (09h). Fewer readings shorten the calibration time but also provide less accuracy. Averaging more readings takes longer but yields a more accurate calibration result by reducing the noise level.

Two commands can be used to perform offset calibration. SFOCAL is a self offset calibration that internally sets the input to mid-scale using the SYS_MON[2:0] = 001 setting and takes a measurement of the offset. SYOCAL is a system offset calibration where the user must input a null voltage to calibrate the system offset. After either command is issued, the OFC register is updated.

After an offset calibration is performed, the device starts a new conversion and $\overline{\text{DRDY}}$ falls to indicate a new conversion has completed.

9.3.14.2 Gain Calibration

The full-scale (gain) calibration word is 16 bits consisting of two 8-bit registers, as shown in the two registers starting with gain calibration register 1. The gain calibration value is straight binary, normalized to a unity-gain correction factor at a register value equal to 4000h. 表 22 shows register values for selected gain factors. Do not exceed the PGA input range limits during gain calibration.

表 22. Gain Calibration Register Values

FSC REGISTER VALUE	GAIN FACTOR
4333h	1.05
4000h	1.00
3CCCh	0.95

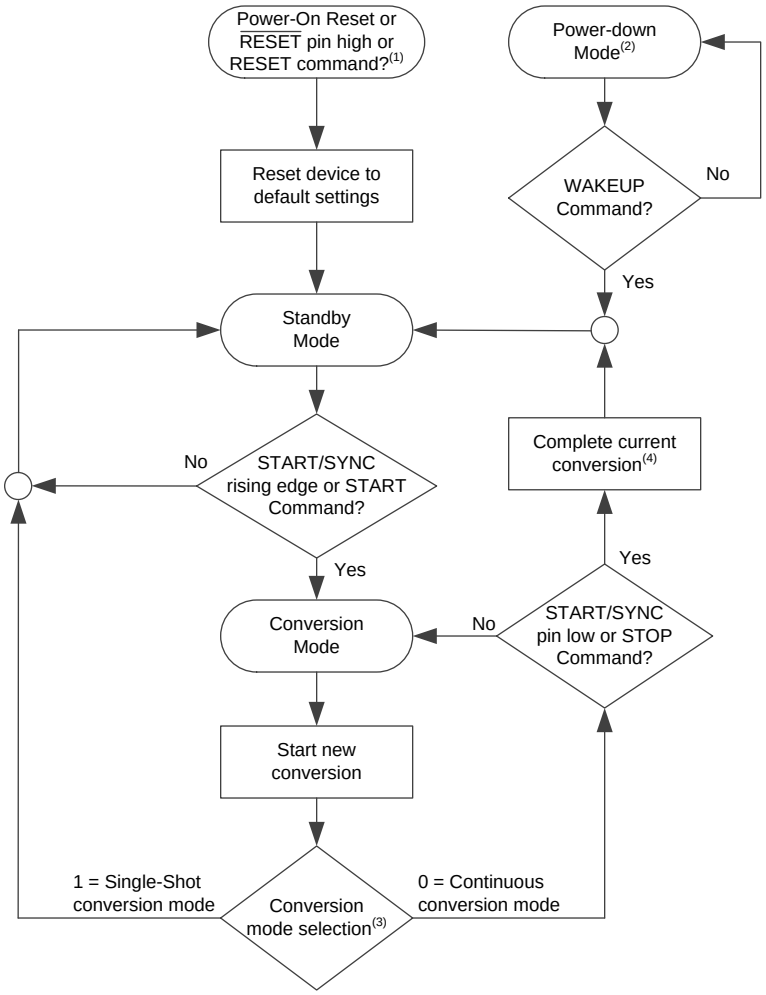
All gains of the ADS114S0x are factory trimmed to meet the gain error specified in the *Electrical Characteristics* table at T_A = 25°C. When the gain drift of the devices over temperature is very low, there is typically no need for self gain calibration.

The SYGCAL command initiates a system gain calibration, where the user sets the input to full-scale to remove gain error. After the SYGCAL is issued, the FSC register is updated. As with the offset calibration, the CAL_SAMP[1:0] bits determine the number of samples used for a gain calibration.

As with an offset calibration, the device starts a new conversion after a gain calibration and $\overline{\text{DRDY}}$ falls to indicate a new conversion has completed.

9.4 Device Functional Modes

The device operates in three different modes: power-down mode, standby mode, and conversion mode. 図 82 shows a flow chart of the different operating modes and how the device transitions from one mode to another.



(1) Any reset (power-on, command, or pin), immediately resets the device.

(2) A POWERDOWN command aborts an ongoing conversion and immediately puts the device into power-down mode.

(3) The conversion mode is selected with the MODE bit in the data rate register.

(4) The rising edge of the START/SYNC pin or the START command starts a new conversion without completing the current conversion.

図 82. Operating Flow Chart

9.4.1 Reset

The ADS114S0x is reset in one of three ways:

- Power-on reset
- $\overline{\text{RESET}}$ pin
- RESET command

When a reset occurs, the configuration registers reset to default values and the device enters standby mode. The device then waits for the rising edge of the START/SYNC pin or a START command to enter conversion mode. Note that if the device had been using an external clock, the reset sets the device to use the internal oscillator as a default configuration. See the *Timing Characteristics* section for reset timing information.

Device Functional Modes (continued)

9.4.1.1 Power-On Reset

The ADS114S0x incorporates a power-on reset circuit that holds the device in reset until all supplies reach approximately 1.65 V. The power-on reset also ensures that the device starts operating in a known state in case a brown-out event occurs, when the supplies have dipped below the minimum operating voltages. When the device completes a POR sequence, the FL_POR flag in the status register is set high to indicate that a POR has occurred.

Begin communications with the device 2.2 ms after the power supplies reach minimum operating voltages. The only exception is polling the status register for the $\overline{\text{RDY}}$ bit. If the user polls the $\overline{\text{RDY}}$ bit, then use an SCLK rate of half the maximum-specified SCLK rate to get a proper reading when the device is making internal configurations. This 2.2-ms POR time is required for the internal oscillator to start up and the device to properly set internal configurations. After the internal configurations are set, the device sets the $\overline{\text{RDY}}$ bit in the device status register (01h). When this bit is set to 0, user configurations can be programmed into the device. 図 83 shows the power-on reset timing sequence for the device.

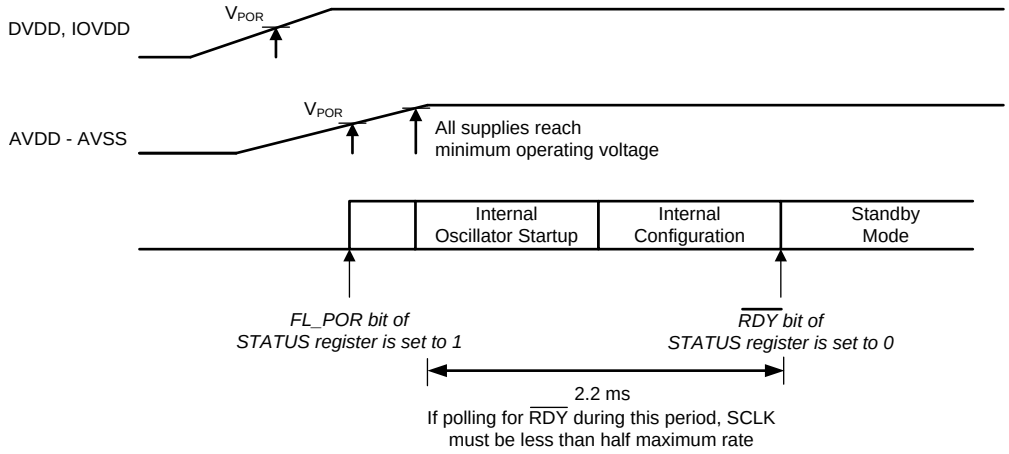


図 83. Power-On Reset Timing Sequence

9.4.1.2 $\overline{\text{RESET}}$ Pin

Reset the ADC by taking the $\overline{\text{RESET}}$ pin low for a minimum of $4 \cdot t_{CLK}$ cycles, and then returning the pin high. After the rising edge of the $\overline{\text{RESET}}$ pin, a delay time of $t_{d(RSSC)}$ is required before sending the first serial interface command or starting a conversion. See the *Timing Characteristics* section for reset timing information.

9.4.1.3 Reset by Command

Reset the ADC by using the RESET command (06h or 07h). The command is decoded on the seventh SCLK falling edge. After sending the RESET command, a delay time of $t_{d(RSSC)}$ is required before sending the first serial interface command or starting a conversion. See the *Timing Characteristics* section for reset timing information.

9.4.2 Power-Down Mode

Power-down mode is entered by sending the POWERDOWN command. In this mode, all analog and digital circuitry is powered down for lowest power consumption regardless of the register settings. Only the internal voltage reference can be configured to stay on during power-down mode in case a faster start-up time is required. All register values retain the current settings during power-down mode. The configuration registers can be read and written in power-down mode. A WAKEUP command must be issued in order to exit power-down mode and to enter standby mode.

When the POWERDOWN command is issued, the device enters power-down mode $2 \cdot t_{CLK}$ after the seventh SCLK falling edge of the command. For lowest power consumption (on DVDD and IOVDD), stop the external clock when in power-down mode. The device does not gate the external clock when in power-down mode. Selecting the internal oscillator before sending the POWERDOWN command is recommended.

Device Functional Modes (continued)

To release the device from POWERDOWN, issue the WAKEUP command to enter standby mode. The device then waits for the rising edge of the START/SYNC pin or a START command to go into conversion mode.

When in power-down mode, the device responds to the RREG, RDATA, and WAKEUP commands. The WREG and RESET commands can also be sent, but are ignored until a WAKEUP command is sent and the internal oscillator resumes operation.

9.4.3 Standby Mode

The device powers up in standby mode and automatically enters this mode whenever there is no ongoing conversion. When the STOP command is sent (or the START/SYNC pin is taken low) in continuous conversion mode, or when a conversion completes in single-shot conversion mode, the device enters standby mode.

Standby mode offers several different options and features to lower the power consumption:

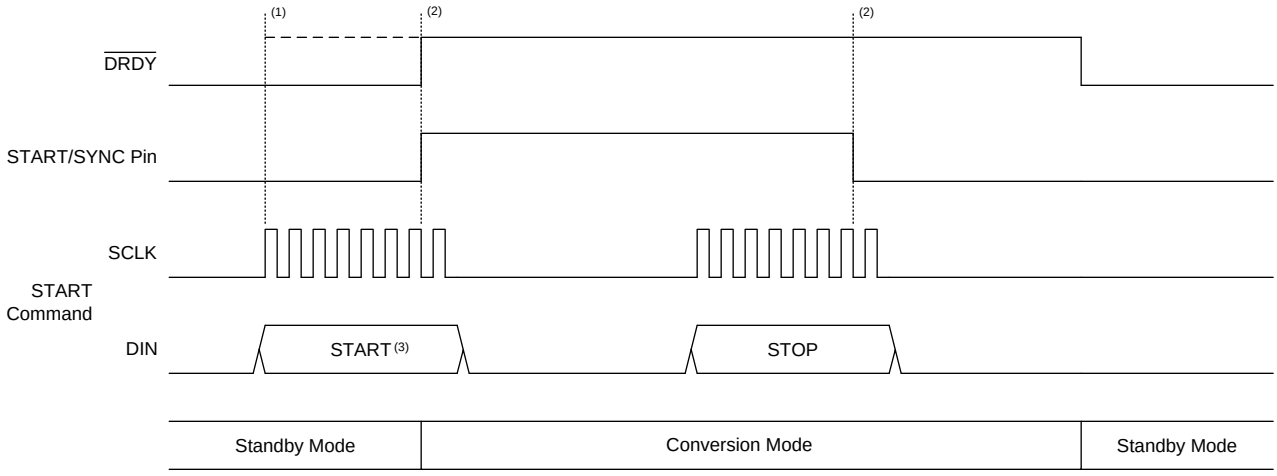
- The PGA can be powered down by setting PGA_EN[1:0] to 00 in the gain setting register (03h).
- The internal voltage reference can be powered down by setting REFCON[1:0] to 00 in the reference control register (05h). This setting also turns off the IDACs.
- The digital filter is held in reset state.
- The clock to the modulator and digital core is gated to decrease dynamic switching losses.

If powered down in standby mode, the PGA and internal reference can require extra time to power up. Extra delay may be required between power up of the PGA or the internal reference, and the start of conversions. In particular, the reference power up time is dependent on the capacitance between REFOUT and REFCOM.

Calibration commands are not decoded when the device is in standby mode.

9.4.4 Conversion Modes

The ADS114S0x offers two conversion modes: continuous conversion and single-shot conversion mode. Continuous-conversion mode converts indefinitely until stopped by the user. Single-shot conversion mode performs one conversion after the START/SYNC pin is taken high or after the START command is sent. Use the MODE bit in the data rate register (04h) to program the conversion mode. 図 84 shows how the START/SYNC pin and the START command are used to control ADC conversions.



(1) $\overline{\text{DRDY}}$ rises at the first SCLK rising edge or the rising edge of the START/SYNC pin.

(2) START and STOP commands take effect 2 · t_{CLK} after the seventh SCLK falling edge. The conversion starts 2 · t_{CLK} after the START/SYNC rising edge.

(3) To synchronize a conversion, the STOP command must be issued prior to the START command. STOP and START commands can be issued without a delay between the commands.

図 84. Conversion Start and Stop Timing

Device Functional Modes (continued)

ADC conversions are controlled by the START/SYNC pin or by serial commands. For the device to start converting in continuous conversion or single-shot conversion mode, a START command must be sent or the START/SYNC pin must be taken high. If using commands to control conversions, keep the START/SYNC pin low to avoid possible contentions between the START/SYNC pin and commands.

Conversions can be synchronized to perform a conversion at a particular time. To synchronize the conversion with the START/SYNC pin, take the pin low. The rising edge of the START/SYNC pin starts a new conversion. Similarly, a conversion can be synchronized using the START command. If the device is in standby mode, issue a START command. If the device is in conversion mode, issue a STOP command followed by a START command. The STOP and START commands can be consecutive. A new conversion starts on the seventh SCLK falling edge of the START command.

9.4.4.1 Continuous Conversion Mode

The device is configured for continuous conversion mode by setting the MODE bit to 0 in the data rate register (04h). A START command must be sent or the START/SYNC pin must be taken high for the device to start converting continuously. When controlling the device with commands, hold the START/SYNC pin low. Taking the START/SYNC pin low or sending the STOP command stops the device from converting after the currently ongoing conversion completes, indicated by the falling edge of $\overline{\text{DRDY}}$. The device enters standby mode thereafter.

For information on the exact timing of single-shot conversion mode data, see 表 13 and 表 15.

9.4.4.2 Single-Shot Conversion Mode

The device is configured for single-shot conversion mode by setting the MODE bit to 1 in the data rate register (04h). A START command must be sent or the START/SYNC pin must be taken high for the device to start a single conversion. After the conversion completes, the device enters standby mode again. To start a new conversion, the START command must be sent again or the START/SYNC pin must be taken low and then high again.

When the device uses the sinc^3 filter, ADC data requires three conversion cycles to settle. When the sinc^3 filter is enabled, a single-shot conversion suppresses the first two ADC conversions and provides the third conversion as the output data so that the user receives settled data. Because three conversions are required for settled data, the conversion time in single-shot conversion mode is approximately three times the normal data period. When the device uses the low-latency filter, the ADC data settles in a single conversion. In single-shot conversion mode with the low-latency filter, the data period is closer to the normal data period.

For information on the exact timing of single-shot conversion mode data, see 表 13 and 表 15.

9.4.4.3 Programmable Conversion Delay

When a new conversion is started, the ADC provides a delay before the actual start of the conversion. This timed delay is provided to allow for the integrated analog anti-alias filter to settle. In some cases more delay is required to allow for external settling effects. The delay time can be configured to automatically delay the start of a conversion after a START command is sent, the START/SYNC pin is taken high, or a WREG command is sent to change any configuration register from address 03h to 07h is issued (as described in the *WREG* section). The programmable conversion delay is intended to accommodate the analog settling time on the inputs (for example, when changing a multiplexer channel). Use the DELAY[2:0] bits in the gain setting register (03h) to program a delay time ranging from $1 \cdot t_{MOD}$ to $4096 \cdot t_{MOD}$ (where $t_{MOD} = 16 \cdot t_{CLK}$). The default programmable conversion delay setting is $14 \cdot t_{MOD}$.

9.5 Programming

9.5.1 Serial Interface

The ADC has an SPI-compatible, bidirectional serial interface that is used to read the conversion data as well as to configure and control the ADC. Only SPI mode 1 (CPOL = 0, CPHA = 1) is supported. The serial interface consists of five control lines: $\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$ but can be used with only four or even three control signals. If the ADS114S08 or ADS114S06 is the only device connected to the SPI bus, then the $\overline{CS}$ input can be tied low so that only SCLK, DIN, and DOUT/$\overline{DRDY}$ are required to communicate with the device.

9.5.1.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is an active low input that enables the ADC serial interface for communication and is useful when multiple devices share the same serial bus. $\overline{CS}$ must be low during the entire data transaction. When $\overline{CS}$ is high, the serial interface is reset, SCLK input activity is ignored (blocking input commands), and the DOUT/$\overline{DRDY}$ output enters a high-impedance state. ADC conversions are not affected by the state of $\overline{CS}$. In situations where multiple devices are present on the bus, the dedicated $\overline{DRDY}$ pin can provide an uninterrupted monitor of the conversion status and is not affected by $\overline{CS}$. If the serial bus is not shared with another peripheral, $\overline{CS}$ can be tied to DGND to permanently enable the ADC interface and DOUT/$\overline{DRDY}$ can be used to indicate conversion status. These changes reduce the serial interface from five I/Os to three I/Os.

9.5.1.2 Serial Clock (SCLK)

The serial interface clock is a noise-filtered, Schmidt-triggered input used to clock data into and out of the ADC. Input data to the ADC are latched on the falling SCLK edge and output data from the ADC are updated on the rising SCLK edge. Return SCLK low after the data sequence is complete. Even though the SCLK input has hysteresis, keep SCLK as clean as possible to prevent unintentional SCLK transitions. Avoid ringing and voltage overshoot on the SCLK input. Place a series termination resistor at the SCLK drive pin to help reduce ringing.

9.5.1.3 Serial Data Input (DIN)

The serial data input pin (DIN) is used with SCLK to send data (commands and register data) to the device. The device latches data on DIN on the SCLK falling edge. The device never drives the DIN pin. During data readback, when no command is intended, keep DIN low.

9.5.1.4 Serial Data Output and Data Ready (DOUT/$\overline{DRDY}$)

The DOUT/$\overline{DRDY}$ pin is a dual-function output. The pin functions as the digital data output and the ADC data-ready indication.

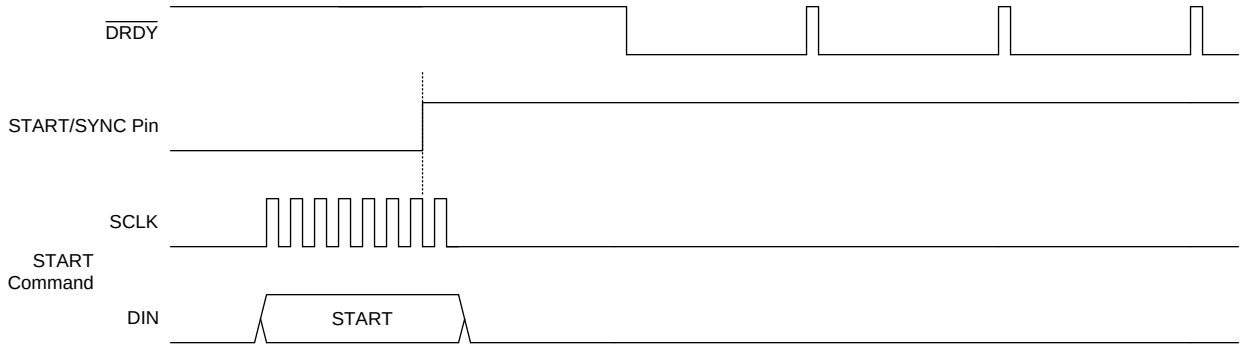
First, this pin is used with SCLK to read conversion and register data from the device. Conversion or register data are shifted out on DOUT/$\overline{DRDY}$ on the SCLK rising edge. DOUT/$\overline{DRDY}$ goes to a high-impedance state when $\overline{CS}$ is high.

Second, the DOUT/$\overline{DRDY}$ pin indicates availability of new conversion data. DOUT/$\overline{DRDY}$ transitions low at the same time that the $\overline{DRDY}$ pin goes low to indicate new conversion data are available. Both signals can be used to detect if new data are ready. However, because DOUT/$\overline{DRDY}$ is disabled when $\overline{CS}$ is high, use the dedicated $\overline{DRDY}$ pin when monitoring conversions on multiple devices on the SPI bus.

Programming (continued)

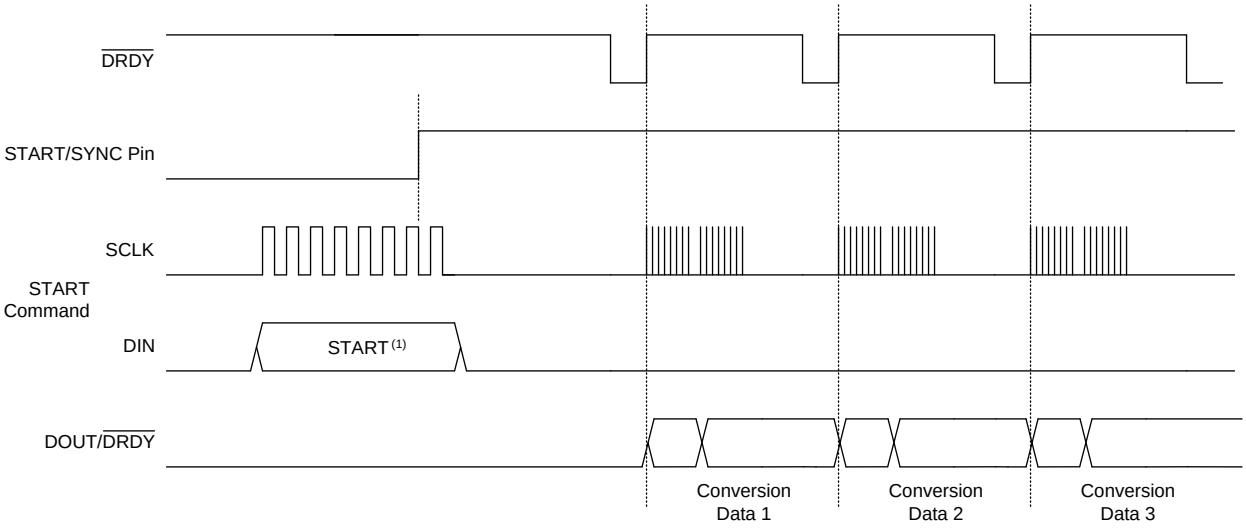
9.5.1.5 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ pin is an output that transitions low to indicate when conversion data are ready for retrieval. Initially, $\overline{DRDY}$ is high at power-on. When converting, the state of $\overline{DRDY}$ depends on whether the conversion data are retrieved or not. In continuous conversion mode after $\overline{DRDY}$ goes low, $\overline{DRDY}$ is driven high on the first SCLK rising edge. If data are not read, $\overline{DRDY}$ remains low and then pulses high 24 · t_{CLK} before the next $\overline{DRDY}$ falling edge. The data must be retrieved before the next $\overline{DRDY}$ update, otherwise the data are overwritten by new data and any previous data are lost. 図 85 shows the $\overline{DRDY}$ operation without data retrieval. 図 86 shows the $\overline{DRDY}$ operation with data retrieval after each conversion completes.



(1) $\overline{DRDY}$ returns high with the rising edge of the first SCLK after a data ready indication.

図 85. $\overline{DRDY}$ Operation Without Data Retrieval



(1) $\overline{DRDY}$ returns high with the rising edge of the first SCLK after a data ready indication.

図 86. $\overline{DRDY}$ Operation With Data Retrieval

9.5.1.6 Timeout

The ADS114S0x offers a serial interface timeout feature that is used to recover communication when a serial interface transmission is interrupted. This feature is especially useful in applications where $\overline{CS}$ is permanently tied low and is not used to frame a communication sequence. The SPI interface resets when no valid 8 bits are received within 2^{15} · t_{CLK}. The timeout feature is enabled by setting the TIMEOUT bit to 1 in the system control register (09h).

Programming (continued)

9.5.2 Data Format

The devices provide 16 bits of data in binary twos complement format. The size of one code (LSB) is calculated using 式 11.

$$1\ \text{LSB} = (2 \cdot V_{REF} / \text{Gain}) / 2^{16} = +\text{FS} / 2^{15} \quad (11)$$

A positive full-scale input [$V_{IN} \geq (+\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

表 23 summarizes the ideal output codes for different input signals.

表 23. Ideal Output Code vs Input Signal

INPUT SIGNAL, $V_{IN} = V_{AINP} - V_{AINN}$	IDEAL OUTPUT CODE(1)
≥ FS ($2^{15} - 1$) / 2^{15}	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

Mapping of the analog input signal to the output codes is shown in 図 87.

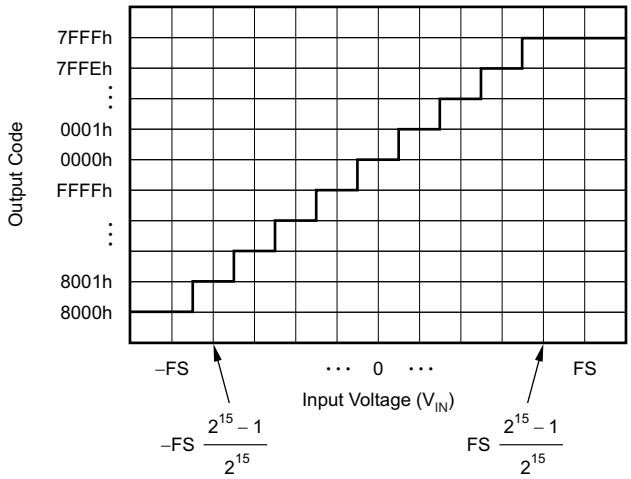


図 87. Code Transition Diagram

9.5.3 Commands

Commands are used to control the ADC, access the configuration registers, and retrieve data. Many of the commands are stand-alone (that is, single-byte). The register write and register read commands, however, are multibyte, consisting of two command bytes plus the register data byte or bytes. The commands are listed in 表 24.

表 24. Command Definitions

COMMAND	DESCRIPTION	FIRST COMMAND BYTE	SECOND COMMAND BYTE
Control Commands			
NOP	No operation	0000 0000 (00h)	—
WAKEUP	Wake-up from power-down mode	0000 001x (02h, 03h)(1)	—
POWERDOWN	Enter power-down mode	0000 010x (04h, 05h)(1)	—
RESET	Reset the device	0000 011x (06h, 07h)(1)	—
START	Start conversions	0000 100x (08h, 09h)(1)	—
STOP	Stop conversions	0000 101x (0Ah, 0Bh)(1)	—
Calibration Commands			
SYOCAL	System offset calibration	0001 0110 (16h)	—
SYGCAL	System gain calibration	0001 0111 (17h)	—
SFOCAL	Self offset calibration	0001 1001 (19h)	—
Data Read Command			
RDATA	Read data by command	0001 001x (12h / 13h)(1)	—
Register Read and Write Commands			
RREG	Read *nnnnn* registers starting at address *rrrrr*	001r rrrr(2)	000n nnnn(3)
WREG	Write *nnnnn* registers starting at address *rrrrr*	010r rrrr(2)	000n nnnn(3)

(1) x = don't care.
(2) r rrrr = starting register address.
(3) n nnnn = number of registers to read or write – 1.

Commands can be sent at any time, either during a conversion or when conversions are stopped. However, if register read or write commands are in progress when conversion data are ready, the ADC blocks loading of conversion data to the output shift register. The $\overline{CS}$ input pin can be taken high between commands; or held low between consecutive commands. $\overline{CS}$ must stay low for the entire command sequence. Complete the command, or terminate the command before completion by taking $\overline{CS}$ high. Only send the commands that are listed in 表 24.

9.5.3.1 NOP

NOP is a no-operation command. The NOP command is used to clock out data without clocking in a command.

9.5.3.2 WAKEUP

Issue the WAKEUP command to exit power-down mode and to place the device into standby mode.

When running off the external clock, the external clock must be running before sending the WAKEUP command, otherwise the command is not decoded.

9.5.3.3 POWERDOWN

Sending the POWERDOWN command aborts a currently ongoing conversion and puts the device into power-down mode. The device goes into power-down mode $2 \cdot t_{CLK}$ after the seventh SCLK falling edge of the command.

For lowest power consumption on DVDD and IOVDD, stop the external clock when in power-down mode. The device does not gate the external clock. When running off the external clock, provide at a minimum two additional t_{CLK}s after the POWERDOWN command is issued, otherwise the device does not enter power-down mode. Because an external clock can be gated for lower power consumption, selecting the internal oscillator before sending the POWERDOWN command is recommended.

During power-down mode, the only commands that are available are RREG, RDATA, and WAKEUP.

9.5.3.4 RESET

The RESET command resets the digital filter and sets all configuration register values to default settings. A RESET command also puts the device into standby mode. When in standby mode, the device waits for a rising edge on the START/SYNC pin or a START command to resume conversions. After sending the RESET command, a delay time of $t_{d(RSSC)}$ is required before sending the first serial interface command or starting a conversion. See the *Timing Characteristics* section for reset timing information.

Note that if the device had been using an external clock, the reset sets the device to use the internal oscillator as a default configuration.

9.5.3.5 START

When the device is configured for continuous conversion mode, issue the START command for the device to start converting. Every time a conversion completes, the device automatically starts a new conversion until the STOP command is sent.

In single-shot conversion mode, the START command is used to start a single conversion. After the conversion completes, the device enters standby mode.

Tie the START/SYNC pin low when the device is controlled through the START and STOP commands. The START command is not decoded if the START/SYNC pin is high. If the device is already in conversion mode, the command has no effect.

9.5.3.6 STOP

The STOP command is used in continuous conversion mode to stop the device from converting. The current conversion is allowed to complete. After $\overline{\text{DRDY}}$ transitions low, the device enters standby mode. The command has no effect in single-shot conversion mode.

Hold the START/SYNC pin low when the device is controlled through START and STOP commands.

9.5.3.7 SYOCAL

The SYOCAL command initiates a system offset calibration. For a system offset calibration, the inputs must be externally shorted to a voltage within the input range, ideally near the mid-supply voltage of (AVDD + AVSS) / 2. The OFC registers are updated when the command completes. Calibration commands must be issued in conversion mode.

9.5.3.8 SYGCAL

The SYGCAL command initiates the system gain calibration. For a system gain calibration, the input must be externally set to full-scale. The FSC registers are updated after this operation. Calibration commands must be issued in conversion mode.

9.5.3.9 SFOCAL

The SFOCAL command initiates a self offset calibration. The device internally shorts the inputs to mid-supply and performs the calibration. The OFC registers are updated after this operation. Calibration commands must be issued in conversion mode.

9.5.3.10 RDATA

The RDATA command is used to read conversion data from the device at any time without concern of data corruption when the $\overline{\text{DRDY}}$ or DOUT/$\overline{\text{DRDY}}$ signal cannot be monitored. The conversion result is read from a buffer so that a new data conversion does not corrupt the conversion read.

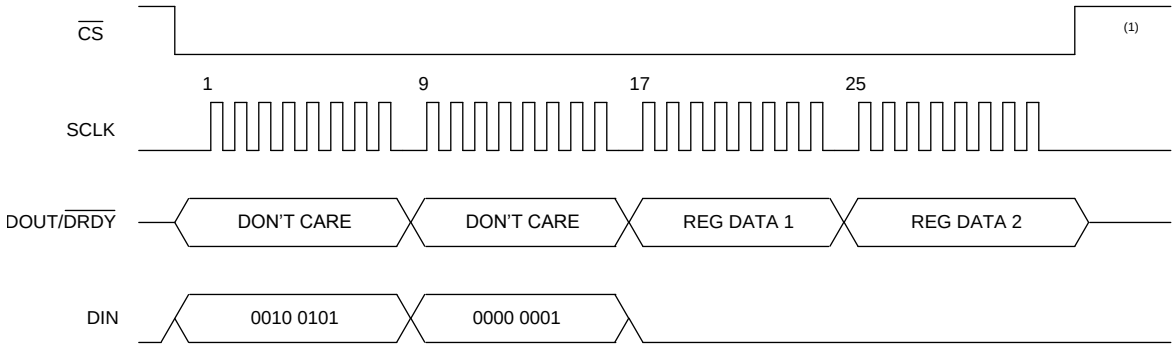
9.5.3.11 RREG

Use the RREG command to read the device register data. Read the register data one register at a time, or read a block of register data. The starting register address can be any register in the register map. The RREG command consists of two bytes. The first byte specifies the starting register address: 001r rrrr, where *r rrrr* is the starting register address. The second command byte is the number of registers to read (minus 1): 000n nnnn, where *n nnnn* is the number of registers to read minus 1.

After the read command is sent, the ADC responds with one or more register data bytes, most significant bit first. If the byte count exceeds the last register address, the ADC begins to output zero data. During the register read operation, any conversion data that becomes available is not loaded to the output shift register to avoid data contention. However, the conversion data can be retrieved later by the RDATA command. After the register read command has started, further commands are blocked until one of the following conditions are met:

- The read operation is completed
- The read operation is terminated by taking $\overline{\text{CS}}$ high
- The read operation is terminated by a serial interface timeout
- The ADC is reset by toggling the $\overline{\text{RESET}}$ pin

図 88 depicts a two-register read operation example. As shown, the commands required to read data from two registers starting at register REF (address = 05h) are: command byte 1 = 25h and command byte 2 = 01h. Keep DIN low after the two command bytes are sent.



(1) $\overline{\text{CS}}$ can be set high or kept low between commands. If kept low, the command must be completed.

図 88. Read Register Sequence

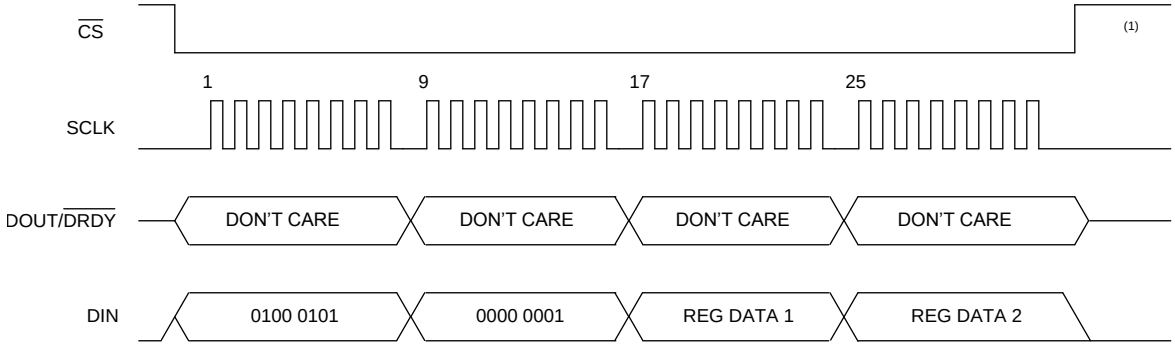
9.5.3.12 WREG

Use the WREG command to write the device register data. The register data are written one register at a time or as a block of register data. The starting register address is any register in the register map.

The WREG command consists of two bytes. The first byte specifies the starting register address: 010r rrrr, where *r rrrr* is the starting register address The second command byte is the number of registers to write (minus 1): 000n nnnn, where *n nnnn* is the number of registers to write minus 1. The following byte (or bytes) is the register data, most significant bit first. If the byte count exceeds the last register address, the ADC ignores the data. After the register write command has started, further commands are blocked until one of the following conditions are met:

- The write operation is completed
- The write operation is terminated by taking $\overline{CS}$ high
- The write operation is terminated by a serial interface timeout
- The ADC is reset by toggling the $\overline{RESET}$ pin

図 89 depicts a two-register write operation example. As shown, the required commands to write data to two registers starting at register REF (address = 05h) are: command byte 1 = 45h and command byte 2 = 01h.



(1) $\overline{CS}$ can be set high or kept low between commands. If kept low, the command must be completed.

図 89. Write Register Sequence

Writing new data to certain configuration registers resets the digital filter and starts a new conversion if a conversion is in progress. Writing to the following registers triggers a new conversion:

- Channel configuration register (02h)
- Gain setting register (03h)
- Data rate register (04h)
- Reference control register (05h), bits [5:0]
- Excitation current register 1 (06h), bits [3:0]
- Excitation current register 2 (07h)
- System control register (09h), bits [7:5]

When the device is configured with WREG, the first data ready indication occurs after the new conversion completes with the new configuration settings. The previous conversion data are cleared at restart; therefore read the previous data before the register write operation. A WREG to the previously mentioned registers only starts a new conversion if the register data are new (differs from the previous register data) and if a conversion is in progress. If the device is in standby mode, the device sets the configuration according to the WREG data, but does not start a conversion until the START/SYNC pin is taken high or a START command is issued.

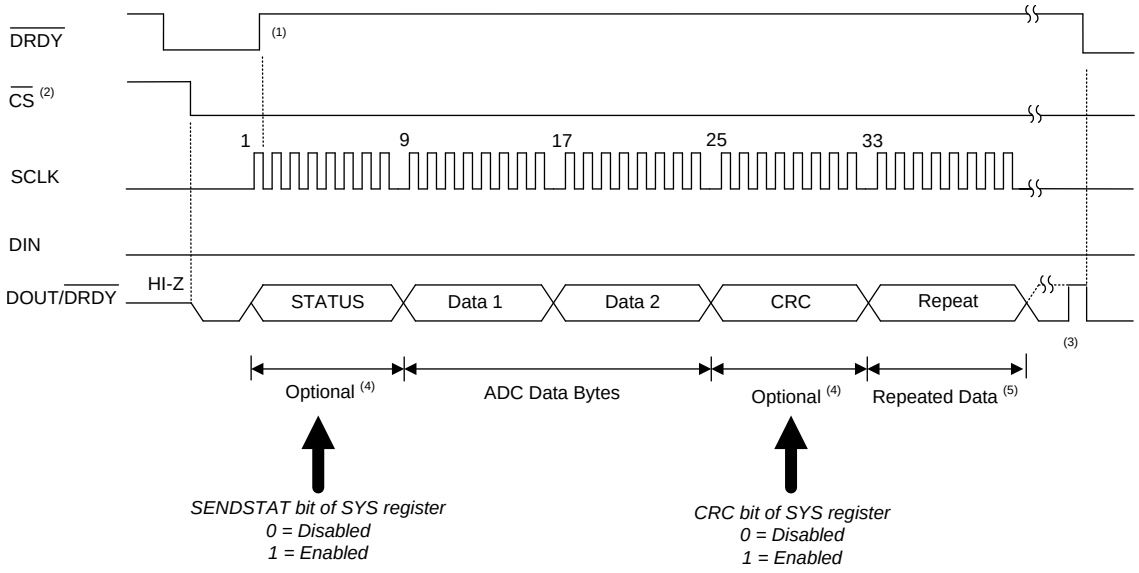
9.5.4 Reading Data

ADC data are read by two methods: read data direct or read data by command. The ADC writes new conversion data to the output shift register and the internal data-holding register. Data are read either from the output shift register (in direct mode) or read from the data-holding register (in command mode). Reading data from the data-holding register (command mode) does not require synchronizing the start of data readback to $\overline{\text{DRDY}}$.

9.5.4.1 Read Data Direct

In this method of data retrieval, ADC conversion data are shifted out directly from the output shift register. No command is necessary. Read data direct requires that no serial activity occur from the falling edge of $\overline{\text{DRDY}}$ to the readback, or the data are invalid. The serial interface is full duplex in the read data direct mode; meaning that commands are decoded during the data readback. If no command is intended, keep DIN low during readback. If an input command is sent during readback, the ADC executes the command, and data corruption can result. Synchronize the data readback to $\overline{\text{DRDY}}$ or to DOUT/$\overline{\text{DRDY}}$ to make sure the data are read before the next $\overline{\text{DRDY}}$ update, or the old data are overwritten with new data.

As shown in 図 90, the ADC data field is 2, 3, or 4 bytes long. The data field consists of an optional STATUS byte, three bytes of conversion data, and an optional CRC byte. After all bytes are read, the data-byte sequence (including the STATUS byte and CRC byte, if selected) is repeated when continued SCLKs are sent. The byte sequence repeats starting with the first byte. In order to help verify error-free communication, read the same data multiple times in each conversion interval or use the optional CRC byte.



(1) $\overline{\text{DRDY}}$ returns high on the first SCLK falling edge.

(2) $\overline{\text{CS}}$ can be tied low. If $\overline{\text{CS}}$ is low, DOUT/$\overline{\text{DRDY}}$ asserts low at the same time as $\overline{\text{DRDY}}$.

(3) Complete data retrieval before new data are ready ($28 \cdot t_{CLK}$ before the next falling edge of DOUT/$\overline{\text{DRDY}}$ and $\overline{\text{DRDY}}$).

(4) The STATUS and CRC bytes are optional.

(5) The byte sequence, including selected optional bytes, repeats by continuing SCLK.

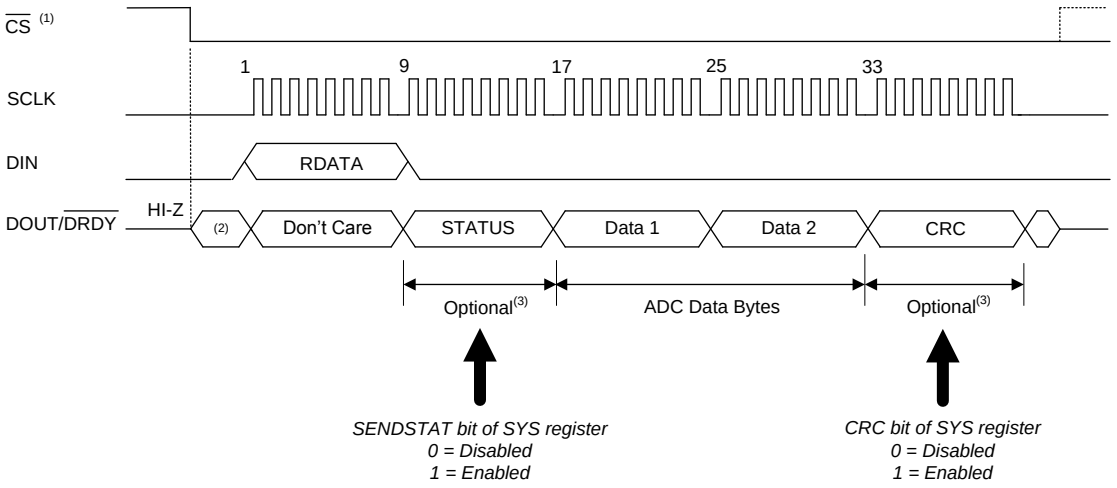
図 90. Read Data Direct

9.5.4.2 Read Data by RDATA Command

When the RDATA command is sent, the data are retrieved from the ADC data-holding register. Read data at any time without the risk of data corruption because the command method does not require synchronizing to DRDY. Polling of DRDY to determine when ADC data are ready can still be used.

図 91 shows the read data by command sequence. The output data MSB begins on the first SCLK rising edge after the command. The output data field can be 2, 3, or 4 bytes long. The data field consists of an optional STATUS byte, three bytes of conversion data, and an optional CRC byte. An RDATA command must be sent for each read operation. The ADC does not respond to commands until the read operation is complete, or terminated by taking CS high.

After all bytes are read, the data-byte sequence (including the STATUS byte and CRC byte, if selected) is repeated by continuing SCLK.



(1) CS can be tied low. If CS is low, DOUT/DRDY asserts low with DRDY.

(2) DOUT/DRDY is driven low with DRDY. If a read operation occurs after the DRDY falling edge, then DOUT/DRDY can be high or low.

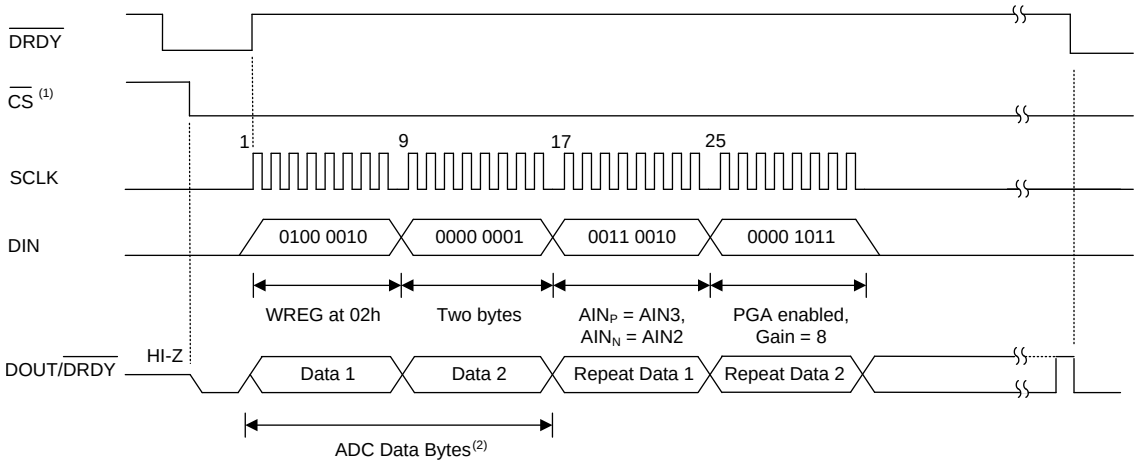
(3) The STATUS and CRC bytes are optional.

図 91. Read Data by Command

9.5.4.3 Sending Commands When Reading Data

The device serial interface is capable of full-duplex operation when reading conversion data and not using the RDATA command. In full-duplex operation, commands are decoded at the same time that conversion data are read. Commands can be sent on any 8-bit data boundary during a data read operation. When a RREG or RDATA command is recognized, the current data read operation is aborted and the conversion data are corrupted, unless the command is sent when the last byte of the conversion result is retrieved. The device starts to output the requested data on DOUT/DRDY at the first SCLK rising edge after the command byte. To read data without interruption, keep DIN low when clocking out data.

A WREG command can be sent without corrupting an ongoing read operation. Sending a WREG command when reading data minimizes the time between reading the data and setting the device configuration for the next conversion. 図 92 shows an example for sending a WREG command to write two configuration registers when reading conversion data by using read data direct mode. After the command is clocked in, the device resets the digital filter and starts converting with the new register settings as long as the device is in continuous conversion mode. The digital filter is reset and conversions are restarted after each data byte is received. In this example, the digital filter is reset when the first byte is received, decoding the input multiplexer and again when the PGA is set. The WREG command can be sent on any of the 8-bit boundaries. The example in 図 92 has the STATUS and CRC bytes disabled.



(1) CS can be tied low. If CS is low, DOUT/DRDY asserts low at the same time as DRDY.

(2) The output data buffer is cyclical and the original data byte is re-issued when the fourth DIN byte is clocked in.

図 92. Issuing a WREG Command When Reading Back ADC Data

9.5.5 Interfacing with Multiple Devices

When connecting multiple devices to a single SPI bus, SCLK, DIN, and DOUT/DRDY can be safely shared by using a dedicated chip-select (CS) line for each SPI-enabled device. When CS transitions high for the respective device, DOUT/DRDY enters a tri-state mode. Therefore, DOUT/DRDY cannot be used to indicate when new data are available if CS is high. Only the dedicated DRDY pin indicates that new data are available because the DRDY pin is actively driven even when CS is high.

In some cases, the DRDY pin cannot be interfaced to the microcontroller. This scenario can occur if there are insufficient GPIO channels available on the microcontroller or if the serial interface must be galvanically isolated and thus the amount of channels must be limited. In order to evaluate when a new conversion of one of the devices is ready, the microcontroller can periodically drop CS to the respective device and poll the state of the DOUT/DRDY pin.

When CS goes low, the DOUT/DRDY pin immediately drives either high or low. If the DOUT/DRDY line drives low, new data are available. If the DOUT/DRDY line drives high, no new data are available. This procedure requires that DOUT/DRDY is forced high after reading each conversion result and before taking CS high. To make sure DOUT/DRDY is taken high, send a RREG command to read a register where the least significant bit is 1.

Retrieving data using direct read mode requires knowledge of the $\overline{\text{DRDY}}$ falling edge timing to avoid data corruption. Use the RDATA command so that valid data can be retrieved from the device at any time without concern of data corruption by a new data ready.

9.6 Register Map

9.6.1 Configuration Registers

The ADS114S0x register map consists of 18, 8-bit registers. These registers are used to configure and control the device to the desired mode of operation. Access the registers through the serial interface by using the RREG and WREG register commands. After power-on or reset, the registers default to the initial settings, as shown in the *Default* column of 表 25.

Data can be written as a block to multiple registers using a single WREG command. If data are written as a block, the data of certain registers take effect immediately when data are shifted in. Writing new data to certain registers results in a restart of conversions that are in progress. The registers that result in a conversion restart are discussed in the *WREG* section.

表 25. Configuration Register Map

ADDR	REGISTER	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	xxh	RESERVED					DEV_ID[2:0]		
01h	STATUS	80h	FL_POR	$\overline{\text{RDY}}$	FL_P_RAILP	FL_P_RAILN	FL_N_RAILP	FL_N_RAILN	FL_REF_L1	FL_REF_L0
02h	INPMUX	01h	MUXP[3:0]				MUXN[3:0]			
03h	PGA	00h	DELAY[2:0]			PGA_EN[1:0]		GAIN[2:0]		
04h	DATARATE	14h	G_CHOP	CLK	MODE	FILTER	DR[3:0]			
05h	REF	10h	FL_REF_EN[1:0]		$\overline{\text{REFP\_BUF}}$	$\overline{\text{REFN\_BUF}}$	REFSEL[1:0]		REFCON[1:0]	
06h	IDACMAG	00h	FL_RAIL_EN	PSW	0	0	IMAG[3:0]			
07h	IDACMUX	FFh	I2MUX[3:0]				I1MUX[3:0]			
08h	VBIAS	00h	VB_LEVEL	VB_AINC	VB_AIN5	VB_AIN4	VB_AIN3	VB_AIN2	VB_AIN1	VB_AIN0
09h	SYS	10h	SYS_MON[2:0]			CAL_SAMP[1:0]		TIMEOUT	CRC	SENDSTAT
0Ah	RESERVED	00h	RESERVED							
0Bh	OFCAL0	00h	OFC[7:0]							
0Ch	OFCAL1	00h	OFC[15:8]							
0Dh	RESERVED	00h	RESERVED							
0Eh	FSCAL0	00h	FSC[7:0]							
0Fh	FSCAL1	40h	FSC[15:8]							
10h	GPIODAT	00h	DIR[3:0]				DAT[3:0]			
11h	GPIOCON	00h	0	0	0	0	CON[3:0]			

9.6.1.1 Device ID Register (address = 00h) [reset = xxh]

図 93. Device ID (ID) Register

7	6	5	4	3	2	1	0
RESERVED					DEV_ID[2:0]		
R-xxh					R-xh		

LEGEND: R = Read only; -n = value after reset; -x = variable

表 26. Device ID (ID) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	xxh	**Reserved** Values are subject to change without notice
2:0	DEV_ID[2:0]	R	xh	**Device identifier** Identifies the model of the device. 000 : Reserved 001 : Reserved 010 : Reserved 011 : Reserved 100 : ADS114S08 (12 channels, 16 bits) 101 : ADS114S06 (6 channels, 16 bits) 110 : Reserved 111 : Reserved

9.6.1.2 Device Status Register (address = 01h) [reset = 80h]

図 94. Device Status (STATUS) Register

7	6	5	4	3	2	1	0
FL_POR	$\overline{\text{RDY}}$	FL_P_RAILP	FL_P_RAILN	FL_N_RAILP	FL_N_RAILN	FL_REF_L1	FL_REF_L0
R/W-1h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 27. Device Status (STATUS) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FL_POR	R/W	1h	**POR flag** Indicates a power-on reset (POR) event has occurred. 0 : Register has been cleared and no POR event has occurred. 1 : POR event occurred and has not been cleared. Flag must be cleared by user register write (default).
6	$\overline{\text{RDY}}$	R	0h	**Device ready flag** Indicates the device has started up and is ready for communication. 0 : ADC ready for communication (default) 1 : ADC not ready
5	FL_P_RAILP	R	0h	**Positive PGA output at positive rail flag**(1) Indicates the positive PGA output is within 150 mV of AVDD. 0 : No error (default) 1 : PGA positive output within 150 mV of AVDD
4	FL_P_RAILN	R	0h	**Positive PGA output at negative rail flag**(1) Indicates the positive PGA output is within 150 mV of AVSS. 0 : No error (default) 1 : PGA positive output within 150 mV of AVSS
3	FL_N_RAILP	R	0h	**Negative PGA output at positive rail flag**(1) Indicates the negative PGA output is within 150 mV of AVDD. 0 : No error (default) 1 : PGA negative output within 150 mV of AVDD
2	FL_N_RAILN	R	0h	**Negative PGA output at negative rail flag**(1) Indicates the negative PGA output is within 150 mV of AVSS. 0 : No error (default) 1 : PGA negative output within 150 mV of AVSS
1	FL_REF_L1	R	0h	**Reference voltage monitor flag, level 1**(2) Indicates the external reference voltage is lower than 1/3 of the analog supply voltage. Can be used to detect an open-excitation lead in a 3-wire RTD application. 0 : Differential reference voltage ≥ 1/3 · (AVDD – AVSS) (default) 1 : Differential reference voltage < 1/3 · (AVDD – AVSS)
0	FL_REF_L0	R	0h	**Reference voltage monitor flag, level 0**(2) Indicates the external reference voltage is lower than 0.3 V. Can be used to indicate a missing or floating external reference voltage. 0 : Differential reference voltage ≥ 0.3 V (default) 1 : Differential reference voltage < 0.3 V

(1) The PGA rail monitors are enabled with the FL_RAIL_EN bit in excitation current register 1 (06h).
(2) The reference monitors are enabled with the FL_REF_EN[1:0] bits of the reference control register (05h).

9.6.1.3 Input Multiplexer Register (address = 02h) [reset = 01h]

図 95. Input Multiplexer (INPMUX) Register

7	6	5	4	3	2	1	0
MUXP[3:0]				MUXN[3:0]			
R/W-0h				R/W-1h			

LEGEND: R/W = Read/Write; *-n* = value after reset

表 28. Input Multiplexer (INPMUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MUXP[3:0]	R/W	0h	**Positive ADC input selection** Selects the ADC positive input channel. 0000 : AIN0 (default) 0001 : AIN1 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6 (ADS114S08 only) 0111 : AIN7 (ADS114S08 only) 1000 : AIN8 (ADS114S08 only) 1001 : AIN9 (ADS114S08 only) 1010 : AIN10 (ADS114S08 only) 1011 : AIN11 (ADS114S08 only) 1100 : AINCOM 1101 : Reserved 1110 : Reserved 1111 : Reserved
3:0	MUXN[3:0]	R/W	1h	**Negative ADC input selection** Selects the ADC negative input channel. 0000 : AIN0 0001 : AIN1 (default) 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6 (ADS114S08 only) 0111 : AIN7 (ADS114S08 only) 1000 : AIN8 (ADS114S08 only) 1001 : AIN9 (ADS114S08 only) 1010 : AIN10 (ADS114S08 only) 1011 : AIN11 (ADS114S08 only) 1100 : AINCOM 1101 : Reserved 1110 : Reserved 1111 : Reserved

9.6.1.4 Gain Setting Register (address = 03h) [reset = 00h]

図 96. Gain Setting (PGA) Register

7	6	5	4	3	2	1	0
DELAY[2:0]			PGA_EN[1:0]		GAIN[2:0]		
R/W-0h			R/W-0h		R/W-0h		

LEGEND: R/W = Read/Write; *-n* = value after reset

表 29. Gain Setting (PGA) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DELAY[2:0]	R/W	0h	**Programmable conversion delay selection** Sets the programmable conversion delay time for the first conversion after a WREG when a configuration change resets of the digital filter and triggers a new conversion(1). 000 : 14 · t_{MOD} (default) 001 : 25 · t_{MOD} 010 : 64 · t_{MOD} 011 : 256 · t_{MOD} 100 : 1024 · t_{MOD} 101 : 2048 · t_{MOD} 110 : 4096 · t_{MOD} 111 : 1 · t_{MOD}
4:3	PGA_EN[1:0]	R/W	0h	**PGA enable** Enables or bypasses the PGA. 00 : PGA is powered down and bypassed. Enables single-ended measurements with unipolar supply (Set gain = 1(2)) (default) 01 : PGA enabled (gain = 1 to 128) 10 : Reserved 11 : Reserved
2:0	GAIN[2:0]	R/W	0h	**PGA gain selection** Configures the PGA gain. 000 : 1 (default) 001 : 2 010 : 4 011 : 8 100 : 16 101 : 32 110 : 64 111 : 128

(1) For details on which bits and registers trigger a new conversion, see the *WREG* section.
(2) When bypassing the PGA, the user must also set GAIN[2:0] to 000.

9.6.1.5 Data Rate Register (address = 04h) [reset = 14h]

図 97. Data Rate (DATARATE) Register

7	6	5	4	3	2	1	0
G_CHOP	CLK	MODE	FILTER	DR[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-4h			

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

表 30. Data Rate (DATARATE) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	G_CHOP	R/W	0h	**Global chop enable** Enables the global chop function. When enabled, the device automatically swaps the inputs and takes the average of two consecutive readings to cancel the offset voltage. 0 : Disabled (default) 1 : Enabled
6	CLK	R/W	0h	**Clock source selection** Configures the clock source to use either the internal oscillator or an external clock. 0 : Internal 4.096-MHz oscillator (default) 1 : External clock
5	MODE	R/W	0h	**Conversion mode selection** Configures the ADC for either continuous conversion or single-shot conversion mode. 0 : Continuous conversion mode (default) 1 : Single-shot conversion mode
4	FILTER	R/W	1h	**Digital filter selection** Configures the ADC to use either the $sinc^3$ or the low-latency filter. 0 : $Sinc^3$ filter 1 : Low-latency filter (default)
3:0	DR[3:0]	R/W	4h	**Data rate selection** Configures the output data rate(1). 0000 : 2.5 SPS 0001 : 5 SPS 0010 : 10 SPS 0011 : 16.6 SPS 0100 : 20 SPS (default) 0101 : 50SPS 0110 : 60 SPS 0111 : 100 SPS 1000 : 200 SPS 1001 : 400 SPS 1010 : 800 SPS 1011 : 1000 SPS 1100 : 2000 SPS 1101 : 4000 SPS 1110 : 4000 SPS 1111 : Reserved

(1) Data rates of 60 Hz or less can offer line-cycle rejection; see the *50-Hz and 60-Hz Line Cycle Rejection* section for more information.

9.6.1.6 Reference Control Register (address = 05h) [reset = 10h]

図 98. Reference Control (REF) Register

7	6	5	4	3	2	1	0
FL_REF_EN[1:0]		$\overline{\text{REFP\_BUF}}$	$\overline{\text{REFN\_BUF}}$	REFSEL[1:0]		REFCON[1:0]	
R/W-0h		R/W-0h	R/W-1h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; *-n* = value after reset

表 31. Reference Control (REF) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	FL_REF_EN[1:0]	R/W	0h	**Reference monitor configuration** Enables and configures the reference monitor. 00 : Disabled (default) 01 : FL_REF_L0 monitor enabled, threshold 0.3 V 10 : FL_REF_L0 and FL_REF_L1 monitors enabled, thresholds 0.3 V and 1/3 · (AVDD – AVSS) 11 : FL_REF_L0 monitor and 10-MΩ pull-together enabled, threshold 0.3 V
5	$\overline{\text{REFP\_BUF}}$	R/W	0h	**Positive reference buffer bypass** Disables the positive reference buffer. Recommended when $V_{(REFPx)}$ is close to AVDD. 0 : Enabled (default) 1 : Disabled
4	$\overline{\text{REFN\_BUF}}$	R/W	1h	**Negative reference buffer bypass** Disables the negative reference buffer. Recommended when $V_{(REFNx)}$ is close to AVSS. 0 : Enabled 1 : Disabled (default)
3:2	REFSEL[1:0]	R/W	0h	**Reference input selection** Selects the reference input source for the ADC. 00 : REFP0, REFN0 (default) 01 : REFP1, REFN1 10 : Internal 2.5-V reference(1) 11 : Reserved
1:0	REFCON[1:0]	R/W	0h	**Internal voltage reference configuration**(2) Configures the behavior of the internal voltage reference. 00 : Internal reference off (default) 01 : Internal reference on, but powers down in power-down mode 10 : Internal reference is always on, even in power-down mode 11 : Reserved

(1) Disable the reference buffers when the internal reference is selected for measurements.
(2) The internal voltage reference must be turned on to use the IDACs.

9.6.1.7 Excitation Current Register 1 (address = 06h) [reset = 00h]

図 99. Excitation Current Register 1 (IDACMAG)

7	6	5	4	3	2	1	0
FL_RAIL_EN	PSW	0	0	IMAG[3:0]			
R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 32. Excitation Current Register 1 (IDACMAG) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FL_RAIL_EN	R/W	0h	**PGA output rail flag enable** Enables the PGA output voltage rail monitor circuit. 0 : Disabled (default) 1 : Enabled
6	PSW	R/W	0h	**Low-side power switch** Controls the low-side power switch. The low-side power switch opens automatically in power-down mode. 0 : Open (default) 1 : Closed
5:4	RESERVED	R	0h	**Reserved** Always write 0h
3:0	IMAG[3:0]	R/W	0h	**IDAC magnitude selection** Selects the value of the excitation current sources. Sets IDAC1 and IDAC2 to the same value. 0000 : Off (default) 0001 : 10 µA 0010 : 50 µA 0011 : 100 µA 0100 : 250 µA 0101 : 500 µA 0110 : 750 µA 0111 : 1000 µA 1000 : 1500 µA 1001 : 2000 µA 1010 - 1111 : Off

9.6.1.8 Excitation Current Register 2 (address = 07h) [reset = FFh]

図 100. Excitation Current Register 2 (IDACMUX)

7	6	5	4	3	2	1	0
I2MUX[3:0]				I1MUX[3:0]			
R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; *-n* = value after reset

表 33. Excitation Current Register 2 (IDACMUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I2MUX[3:0]	R/W	Fh	**IDAC2 output channel selection** Selects the output channel for IDAC2. 0000 : AIN0 0001 : AIN1 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6 (ADS114S08), REFP1 (ADS114S06) 0111 : AIN7 (ADS114S08), REFN1 (ADS114S06) 1000 : AIN8 (ADS114S08 only) 1001 : AIN9 (ADS114S08 only) 1010 : AIN10 (ADS114S08 only) 1011 : AIN11 (ADS114S08 only) 1100 : AINCOM 1101 - 1111 : Disconnected (default)
3:0	I1MUX[3:0]	R/W	Fh	**IDAC1 output channel selection** Selects the output channel for IDAC1. 0000 : AIN0 0001 : AIN1 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6 (ADS114S08 only), REFP1 (ADS114S06) 0111 : AIN7 (ADS114S08 only), REFN1 (ADS114S06) 1000 : AIN8 (ADS114S08 only) 1001 : AIN9 (ADS114S08 only) 1010 : AIN10 (ADS114S08 only) 1011 : AIN11 (ADS114S08 only) 1100 : AINCOM 1101 - 1111 : Disconnected (default)

9.6.1.9 Sensor Biasing Register (address = 08h) [reset = 00h]

図 101. Sensor Biasing (VBIAS) Register

7	6	5	4	3	2	1	0
VB_LEVEL	VB_AINC	VB_AIN5	VB_AIN4	VB_AIN3	VB_AIN2	VB_AIN1	VB_AIN0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

表 34. Sensor Biasing (VBIAS) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VB_LEVEL	R/W	0h	**VBIAS level selection** Sets the VBIAS output voltage level. VBIAS is disabled when not connected to any input. 0 : (AVDD + AVSS) / 2 (default) 1 : (AVDD + AVSS) / 12
6	VB_AINC	R/W	0h	**AINCOM VBIAS selection(1)** Enables VBIAS on the AINCOM pin. 0 : VBIAS disconnected from AINCOM (default) 1 : VBIAS connected to AINCOM
5	VB_AIN5	R/W	0h	**AIN5 VBIAS selection(1)** Enables VBIAS on the AIN5 pin. 0 : VBIAS disconnected from AIN5 (default) 1 : VBIAS connected to AIN5
4	VB_AIN4	R/W	0h	**AIN4 VBIAS selection(1)** Enables VBIAS on the AIN4 pin. 0 : VBIAS disconnected from AIN4 (default) 1 : VBIAS connected to AIN4
3	VB_AIN3	R/W	0h	**AIN3 VBIAS selection(1)** Enables VBIAS on the AIN3 pin. 0 : VBIAS disconnected from AIN3 (default) 1 : VBIAS connected to AIN3
2	VB_AIN2	R/W	0h	**AIN2 VBIAS selection(1)** Enables VBIAS on the AIN2 pin. 0 : VBIAS disconnected from AIN2 (default) 1 : VBIAS connected to AIN2
1	VB_AIN1	R/W	0h	**AIN1 VBIAS selection(1)** Enables VBIAS on the AIN1 pin. 0 : VBIAS disconnected from AIN1 (default) 1 : VBIAS connected to AIN1
0	VB_AIN0	R/W	0h	**AIN0 VBIAS selection(1)** Enables VBIAS on the AIN0 pin. 0 : VBIAS disconnected from AIN0 (default) 1 : VBIAS connected to AIN0

(1) The bias voltage can be selected for multiple analog inputs at the same time.

9.6.1.10 System Control Register (address = 09h) [reset = 10h]

図 102. System Control (SYS) Register

7	6	5	4	3	2	1	0
SYS_MON[2:0]			CAL_SAMP[1:0]		TIMEOUT	CRC	SENDSTAT
R/W-0h			R/W-2h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

表 35. System Control (SYS) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	SYS_MON[2:0]	R/W	0h	**System monitor configuration**(1) Enables a set of system monitor measurements using the ADC. 000 : Disabled (default) 001 : PGA inputs shorted to (AVDD + AVSS) / 2 and disconnected from AINx and the multiplexer; gain set by user 010 : Internal temperature sensor measurement; PGA must be enabled (PGA_EN[1:0] = 01); gain set by user(2) 011 : (AVDD – AVSS) / 4 measurement; gain set to 1(3) 100 : DVDD / 4 measurement; gain set to 1(3) 101 : Burn-out current sources enabled, 0.2-µA setting 110 : Burn-out current sources enabled, 1-µA setting 111 : Burn-out current sources enabled, 10-µA setting
4:3	CAL_SAMP[1:0]	R/W	2h	**Calibration sample size selection** Configures the number of samples averaged for self and system offset and system gain calibration. 00 : 1 sample 01 : 4 samples 10 : 8 samples (default) 11 : 16 samples
2	TIMEOUT	R/W	0h	**SPI timeout enable** Enables the SPI timeout function. 0 : Disabled (default) 1 : Enabled
1	CRC	R/W	0h	**CRC enable** Enables the CRC byte appended to the conversion result. When enabled, CRC is calculated across the 16-bit conversion result (plus the STATUS byte if enabled). 0 : Disabled (default) 1 : Enabled
0	SENDSTAT	R/W	0h	**STATUS byte enable** Enables the STATUS byte prepended to the conversion result. 0 : Disabled (default) 1 : Enabled

(1) With system monitor functions enabled, the AINx multiplexer switches are open for the (AVDD + AVSS) / 2 measurement, the temperature sensor, and the supply monitors.
(2) When using the internal temperature sensor, gain must be 4 or less to keep the measurement within the PGA input voltage range.
(3) The PGA gain is automatically set to 1 when the supply monitors are enabled, regardless of the setting in GAIN[2:0].

9.6.1.11 Reserved Register (address = 0Ah) [reset = 00h]

図 103. Reserved Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

LEGEND: R/W = Read/Write; *-n* = value after reset

表 36. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESERVED	R	00h	**Reserved** Always write 00h

9.6.1.12 Offset Calibration Register 1 (address = 0Bh) [reset = 00h]

図 104. Offset Calibration Register 1 (OFCAL0)

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; *-n* = value after reset

表 37. Offset Calibration Register 1 (OFCAL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC[7:0]	R/W	00h	Bits [7:0] of the offset calibration value.

9.6.1.13 Offset Calibration Register 2 (address = 0Ch) [reset = 00h]

図 105. Offset Calibration Register 2 (OFCAL1)

7	6	5	4	3	2	1	0
OFC[15:8]							
R/W-00h							

LEGEND: R/W = Read/Write; *-n* = value after reset

表 38. Offset Calibration Register 2 (OFCAL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC[15:8]	R/W	00h	Bits [15:8] of the offset calibration value.

9.6.1.14 Reserved Register (address = 0Dh) [reset = 00h]

図 106. Reserved Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

LEGEND: R/W = Read/Write; *-n* = value after reset

表 39. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESERVED	R	00h	**Reserved** Always write 00h

9.6.1.15 Gain Calibration Register 1 (address = 0Eh) [reset = 00h]

図 107. Gain Calibration Register 1 (FSCAL0)

7	6	5	4	3	2	1	0
FSC[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; *-n* = value after reset

表 40. Gain Calibration Register 1 (FSCAL0) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FSC[7:0]	R/W	00h	Bits [7:0] of the gain calibration value.

9.6.1.16 Gain Calibration Register 2 (address = 0Fh) [reset = 40h]

図 108. Gain Calibration Register 2 (FSCAL1)

7	6	5	4	3	2	1	0
FSC[15:8]							
R/W-40h							

LEGEND: R/W = Read/Write; *-n* = value after reset

表 41. Gain Calibration Register 2 (FSCAL1) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FSC[15:8]	R/W	40h	Bits [15:8] of the gain calibration value.

9.6.1.17 GPIO Data Register (address = 10h) [reset = 00h]

図 109. GPIO Data (GPIODAT) Register

7	6	5	4	3	2	1	0
DIR[3:0]				DAT[3:0]			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; *-n* = value after reset

表 42. GPIO Data (GPIODAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DIR[3:0]	R/W	0h	**GPIO direction** Configures the selected GPIO as an input or output. 0 : GPIO[x] configured as output (default) 1 : GPIO[x] configured as input
3:0	DAT[3:0]	R/W	0h	**GPIO data** Contains the data of the GPIO inputs or outputs. 0 : GPIO[x] is low (default) 1 : GPIO[x] is high

9.6.1.18 GPIO Configuration Register (address = 11h) [reset = 00h]

図 110. GPIO Configuration Register

7	6	5	4	3	2	1	0
0	0	0	0	CON[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 43. GPIO Configuration (GPIOCON) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	**Reserved** Always write 0h
3:0	CON[3:0]	R/W	0h	**GPIO pin configuration** Configures the GPIO[x] pin as an analog input or GPIO. CON[x] corresponds to the GPIO[x] pin. 0 : GPIO[x] configured as analog input (default)(1) 1 : GPIO[x] configured as GPIO

(1) On the ADS114S06, the GPIO pins default as disabled. Set the CON[3:0] bits to enable the respective GPIO pins.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS114S06 and ADS114S08 are precision, 16-bit, ΔΣ ADCs that offer many integrated features to simplify the measurement of the most common sensor types (including various types of temperature, flow, and bridge sensors). Primary considerations when designing an application with the ADS114S0x include analog input filtering, establishing an appropriate reference, and setting the absolute input voltage for the internal PGA. Connecting and configuring the serial interface appropriately is another concern. These considerations are discussed in the following sections.

10.1.1 Serial Interface Connections

The principle serial interface connections for the ADS114S0x are shown in 図 111.

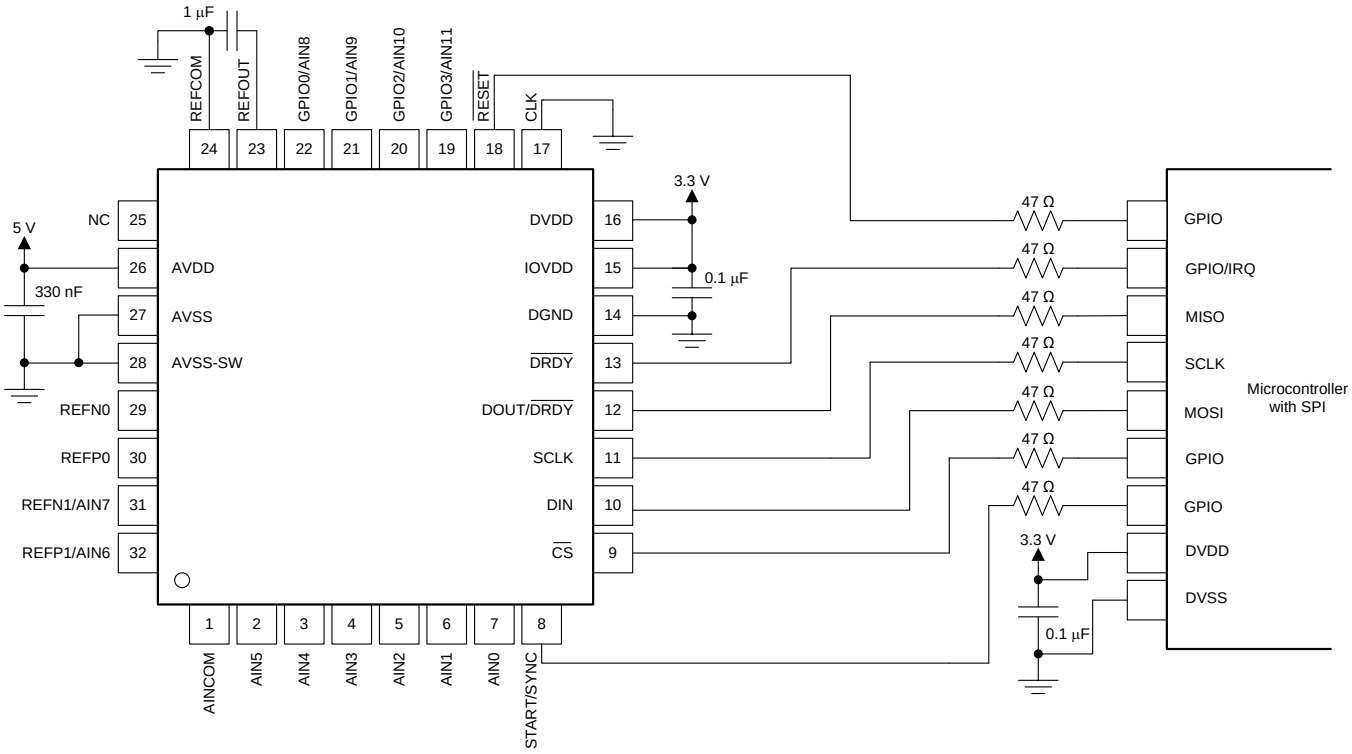


図 111. Serial Interface Connections

Most microcontroller SPI peripherals can interface with the ADS114S0x. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the devices are found in the *Serial Interface* section.

Place 47-Ω resistors in series with all digital input and output pins ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

Application Information (continued)

10.1.2 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components are folded back and show up in the actual frequency band of interest below half the sampling frequency. Note that inside a ΔΣ ADC, the input signal is oversampled at the modulator frequency, f_{MOD} and not at the output data rate. The filter response of the digital filter repeats at multiples of f_{MOD}, as shown in 図 112. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

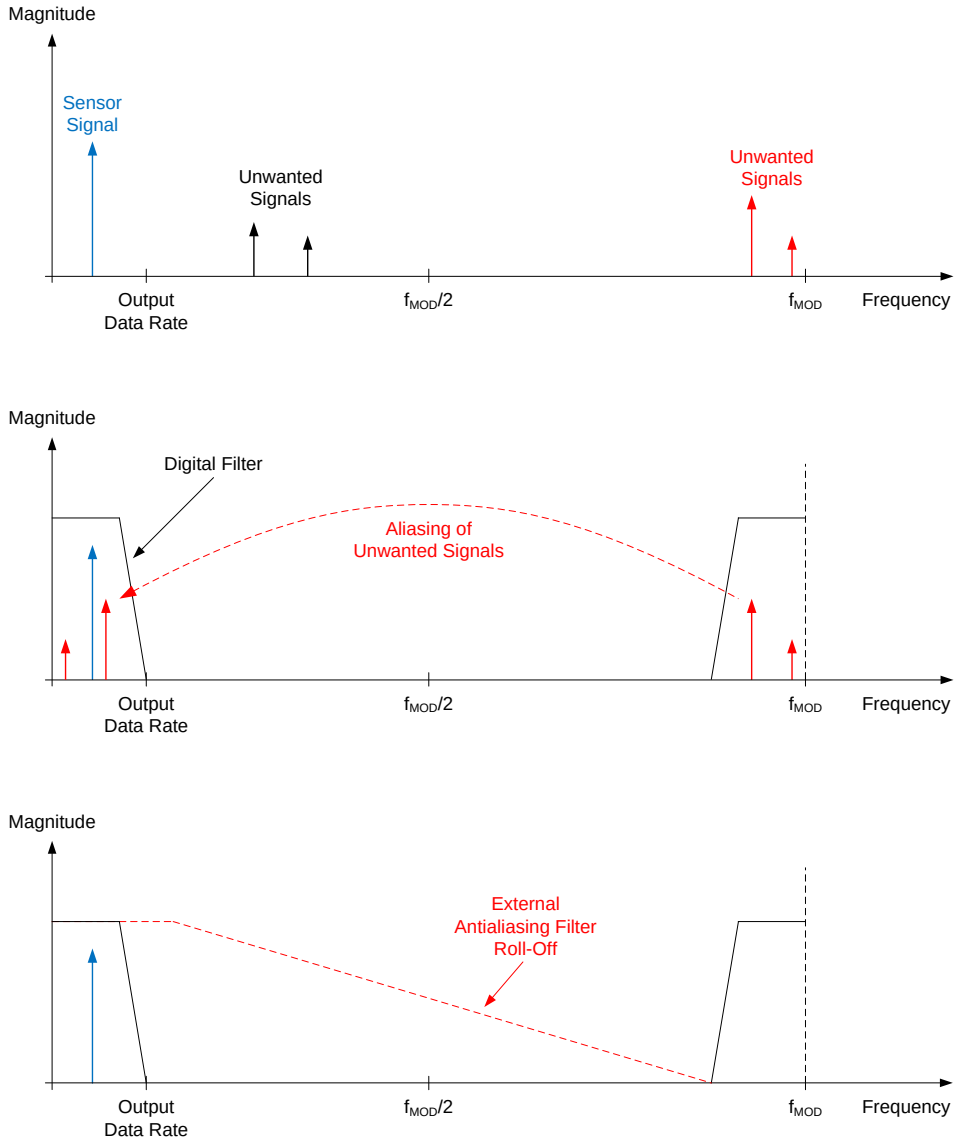


図 112. Effect of Aliasing

Application Information (continued)

Many sensor signals are inherently band limited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either eliminate aliasing, or to reduce the effect of aliasing to a level below the noise floor of the sensor. Ideally, any signal beyond f_{MOD} / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS114S0x attenuates signals to a certain degree, as illustrated in the filter response plots in the *Digital Filter* section. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10 times higher is generally a good starting point for a system design.

Internal to the device, prior to the PGA inputs, is an EMI filter; see 図 50. The cutoff frequency of this filter is approximately 40 MHz and helps reject high-frequency interference.

10.1.3 External Reference and Ratiometric Measurements

The full-scale range of the ADS114S0x is defined by the reference voltage and the PGA gain (FSR = ±V_{REF} / Gain). An external reference can be used instead of the integrated 2.5-V reference to adapt the FSR to the specific system needs. An external reference must be used if V_{IN} > 2.5 V. For example, an external 5-V reference and an AVDD = 5 V are required in order to measure a single-ended signal that can swing between 0 V and 5 V.

The reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement, the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. Because current noise and drift are common to both the sensor measurement and the reference, these components cancel out in the ADC transfer function. The output code is only a ratio of the sensor element and the value of the reference resistor. The value of the excitation current source itself is not part of the ADC transfer function.

The example in the *Typical Application* section describes a system that uses a ratiometric measurement. One excitation current source is used to drive a reference resistor and an RTD. The ADC measurement represents a ratiometric measurement between the RTD value and a known reference resistor value.

10.1.4 Establishing a Proper Input Voltage

The ADS114S0x can be used to measure various types of input signal configurations: single-ended, pseudo-differential, and fully-differential signals (which can be either unipolar or bipolar). However, configuring the device properly for the respective signal type is important.

Signals where the negative analog input is fixed and referenced to analog ground (V_{AINN} = 0 V) are commonly called *single-ended signals*. The input voltage of a single-ended signal consequently varies between 0 V and V_{IN}. If the PGA is disabled and bypassed, the input voltage of the ADS114S08 can be as low as 50 mV below AVSS and as large as 50 mV above AVDD. Therefore, set the PGA_EN bits to 10 in the gain setting register (03h) to measure single-ended signals when a unipolar analog supply is used (AVSS = 0 V). Only a gain of 1 is possible in this configuration. Measuring a 0-mA to 20-mA or 4-mA to 20-mA signal across a load resistor of 100 Ω referenced to GND is a typical example. The ADS114S0x can directly measure the signal across the load resistor using a unipolar supply, the internal 2.5-V reference, and gain = 1 when the PGA is bypassed.

If gain is needed to measure a single-ended signal, the PGA must be enabled. In this case, a bipolar supply is required for the ADS114S0x to meet the input voltage requirement of the PGA. Signals where the negative analog input (AIN_N) is fixed at a voltage other the 0 V are referred to as *pseudo-differential signals*. The input voltage of a pseudo-differential signal varies between V_{AINN} and V_{AINN} + V_{IN}.

Application Information (continued)

Fully-differential signals in contrast are defined as signals having a constant common-mode voltage where the positive and negative analog inputs swing 180° out-of-phase but have the same amplitude.

The ADS114S0x can measure pseudo-differential and fully-differential signals both with the PGA enabled or bypassed. However, the PGA must be enabled in order to measure any input with a gain greater than 1. The input voltage must meet the input and output voltage restrictions of the PGA, as explained in the *PGA Input-Voltage Requirements* section when the PGA is enabled. Setting the input voltage at or near (AVSS + AVDD) / 2 in most cases satisfies the PGA input voltage requirements.

Signals where both the positive and negative inputs are always ≥ 0 V are called *unipolar signals*. These signals can in general be measured with the ADS114S0x using a unipolar analog supply (AVSS = 0 V). As mentioned previously, the PGA must be bypassed in order to measure single-ended, unipolar signals when using a unipolar supply.

A signal is called *bipolar* when either the positive or negative input can swing below 0 V. A bipolar analog supply (such as AVDD = 2.5 V, AVSS = –2.5 V) is required in order to measure bipolar signals with the ADS114S0x. A typical application task is measuring a single-ended, bipolar, ±10-V signal where AIN_N is fixed at 0 V and AIN_P swings between –10 V and 10 V. The ADS114S0x cannot directly measure this signal because the 10-V signal exceeds the analog power-supply limits. However, one possible solution is to use a bipolar analog supply (AVDD = 2.5 V, AVSS = –2.5 V), gain = 1, and a resistor divider in front of the ADS114S0x. The resistor divider must divide the voltage down to ≤ ±2.5 V to be able to measure the voltage using the internal 2.5-V reference.

10.1.5 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog and reference inputs floating, or connect the inputs to mid-supply or to AVDD. Connecting unused analog or reference inputs to AVSS is possible as well, but can yield higher leakage currents than the previously mentioned options. REFN0 is an exception; this pin can be accidently shorted to AVSS through the internal low-side switch. Leave the REFN0 pin floating when not in use or tie the pin to AVSS.

GPIO pins operate on levels based on the analog supply. Do not float GPIO pins that are configured as digital inputs. Tie unused GPIO pins that are configured as digital inputs to the appropriate levels, AVDD or AVSS, including when in power-down mode. Tie unused GPIO output pins to AVSS through a pulldown resistor and set the output to 0 in the GPIO data register. For unused GPIO pins on the ADS114S06, leave the GPIOCON register set to the default register values and connect these GPIO pins in the same manner as for an unused analog input.

Do not float unused digital inputs; excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, IOVDD or DGND, even when in power-down mode. Connections for unused digital inputs are listed below.

- Tie the $\overline{CS}$ pin to DGND if $\overline{CS}$ is not used
- Tie the CLK pin to DGND if the internal oscillator is used
- Tie the START/SYNC pin to DGND to control conversions by commands
- Tie the $\overline{RESET}$ pin to IOVDD if the $\overline{RESET}$ pin is not used
- If the $\overline{DRDY}$ output is not used, leave the $\overline{DRDY}$ pin unconnected or tie the $\overline{DRDY}$ pin to IOVDD using a weak pullup resistor

Application Information (continued)

10.1.6 Pseudo Code Example

The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC in order to take subsequent readings from the ADS114S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin is used to indicate availability of new conversion data.

```
Power-up so that all supplies reach minimum operating levels;
Delay for a minimum of 2.2 ms to allow power supplies to settle and power-up reset to complete;

Configure the SPI interface of the microcontroller to SPI mode 1 (CPOL = 0, CPHA =1);
If the CS pin is not tied low permanently, configure the microcontroller GPIO connected to CS as an
output;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt
input;

Set CS to the device low;
Delay for a minimum of t(CSSC);
Send the RESET command (06h) to make sure the device is properly reset after power-up; //Optional
Delay for a minimum of 4096 · tCLK;
Read the status register using the RREG command to check that the RDY bit is 0; //Optional
Clear the FL_POR flag by writing 00h to the status register; //Optional
Write the respective register configuration with the WREG command;
For verification, read back all configuration registers with the RREG command;
Send the START command (08h) to start converting in continuous conversion mode;
Delay for a minimum of t(SCCS);
Clear CS to high (resets the serial interface);
Loop
    {
    Wait for DRDY to transition low;
    Take CS low;
    Delay for a minimum of t(CSSC);
    Send the RDATA command;
    Send 16 SCLK rising edges to read out conversion data on DOUT/DRDY;
    Delay for a minimum of t(SCCS);
    Clear CS to high;
    }
Take CS low;
Delay for a minimum of t(CSSC);
Send the STOP command (0Ah) to stop conversions and put the device in standby mode;
Delay for a minimum of t(SCCS);
Clear CS to high;
```

10.2 Typical Application

図 113 shows a fault-protected, filtered, 3-wire RTD application circuit with hardware-based, lead-wire compensation. Two IDAC current sources provide the lead-wire compensation. One IDAC current source (IDAC1) provides excitation to the RTD element. The ADC reference voltage (pins AIN6 and AIN7) is derived from the voltage across resistor R_{REF} sourcing the same IDAC1 current, providing ratiometric cancellation of current-source drift. The other current source (IDAC2) has the same current setting, providing cancellation of lead-wire resistance by generating a voltage drop across lead-wire resistance R_{LEAD2} equal to the voltage drop of R_{LEAD1}. Because the R_{RTD} voltage is measured differentially at ADC pins AIN1 and AIN2, the voltages across the lead wire resistance cancel. Resistor R_{BIAS} level-shifts the RTD signal to within the ADC specified input range. The current sources are provided by two additional pins (AIN5 and AIN3) that connect to the RTD through blocking diodes. The additional pins are used to route the RTD excitation currents around the input filter resistors, avoiding the voltage drop otherwise caused by the filter resistors R_{F1} and R_{F4}. The diodes protect the ADC inputs in the event of a miswired connection. The input filter resistors limit the input fault currents flowing into the ADC.

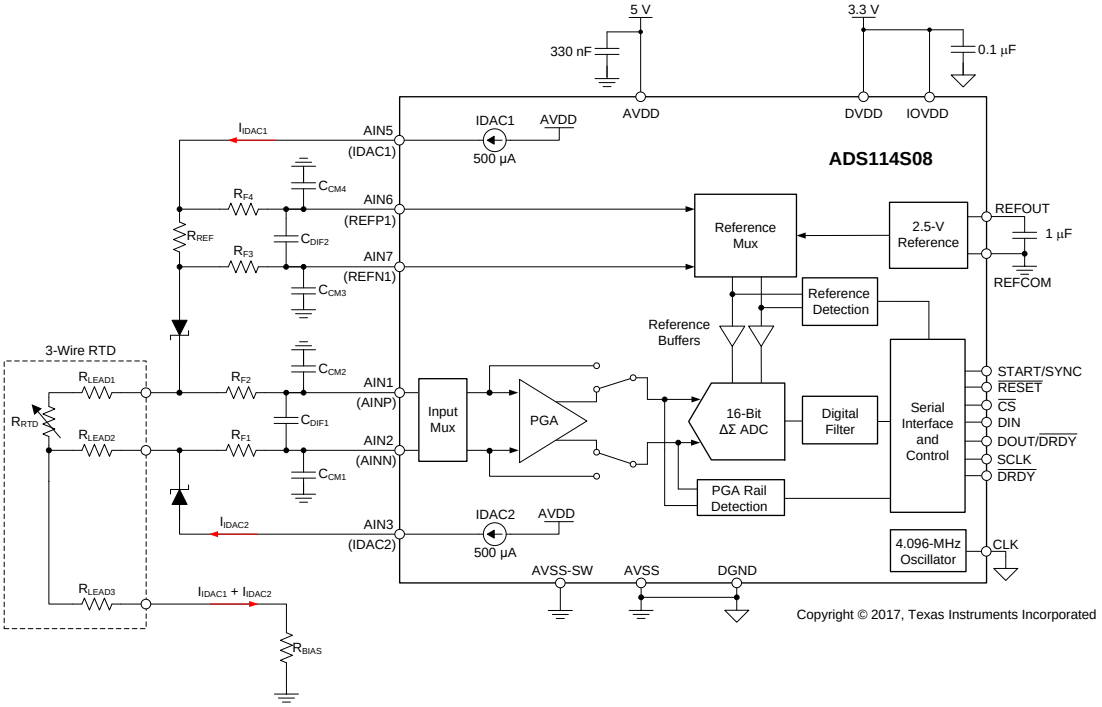


図 113. 3-Wire RTD Application

10.2.1 Design Requirements

表 44 shows the design requirements of the 3-wire RTD application.

表 44. Design Requirements

DESIGN PARAMETER	VALUE
ADC supply voltage	4.75 V (minimum)
RTD sensor type	3-wire Pt100
RTD resistance range	20 Ω to 400 Ω
RTD lead resistance range	0 Ω to 10 Ω
RTD self heating	1 mW
Accuracy(1)	±0.1 Ω

(1) T_A = 25°C. After offset and full-scale calibration.

10.2.2 Detailed Design Procedure

The key considerations in the design of a 3-wire RTD circuit are the accuracy, the lead wire compensation, and the sensor self-heating. As the design values of 表 45 show, several values of excitation currents are available. The resolution is expressed in units of noise-free resolution (NFR). Noise-free resolution is resolution with no code flicker. The selection of excitation currents trades off resolution against sensor self-heating. In general, measurement resolution improves with increasing excitation current. Increasing the excitation current beyond 1000 µA results in no further improvement in resolution for this example circuit. The design procedure is based on a 500-µA excitation current, because this level of current results in very low sensor self-heating (0.4 mW).

表 45. RTD Circuit Design Parameters

I_{IDAC} (µA)	NFR (bits)	P_{RTD} (mW)	V_{RTD} (V)	Gain (V/V)	V_{REFMIN} (1) (V)	V_{REF} (2) (V)	R_{REF} (kΩ)	$V_{AINNLIM}$ (3) (V)	$V_{AINPLIM}$ (4) (V)	R_{BIAS} (kΩ)	V_{RTDN} (5) (V)	V_{RTDP} (6) (V)	V_{IDAC1} (7) (V)
50	16.8	0.001	0.02	32	0.64	0.70	18	0.6	4.1	7.10	0.7	0.7	1.9
100	17.8	0.004	0.04	32	1.28	1.41	14.1	0.9	3.8	5.10	1.0	1.1	2.8
250	18.8	0.025	0.10	16	1.60	1.76	7.04	1.1	3.7	2.30	1.2	1.3	3.3
500	19.1	0.100	0.20	8	1.60	1.76	3.52	1.0	3.8	1.10	1.1	1.3	3.4
750	18.9	0.225	0.30	4	1.20	1.32	1.76	0.8	4.0	0.57	0.9	1.2	2.8
1000	19.3	0.400	0.40	4	1.60	1.76	1.76	0.9	3.9	0.50	1.0	1.4	3.5
1500	19.1	0.900	0.60	2	1.20	1.32	0.88	0.6	4.2	0.23	0.7	1.3	3.0
2000	18.3	1.600	0.80	1	0.80	0.90	0.45	0.3	4.5	0.10	0.4	1.2	2.4

(1) V_{REFMIN} is the minimum reference voltage required by the design.
(2) V_{REF} is the design target reference voltage allowing for 10% overrange.
(3) $V_{AINNLIM}$ is the absolute minimum input voltage required by the ADC.
(4) $V_{AINPLIM}$ is the absolute maximum input voltage required by the ADC.
(5) V_{RTDN} is the design target negative input voltage.
(6) V_{RTDP} is the design target positive input voltage.
(7) V_{IDAC1} is the design target IDAC1 loop voltage.

Initially, R_{LEAD1} and R_{LEAD2} are considered to be 0 Ω. Route the IDAC1 current through the external reference resistor, R_{REF}. IDAC1 generates the ADC reference voltage, V_{REF}, across the reference resistor. This voltage is defined by 式 12:

$$V_{REF} = I_{IDAC1} \cdot R_{REF} \quad (12)$$

Route the second current (IDAC2) to the second RTD lead.

Program the IDAC value by using the IDACMAG register; however, only the IDAC1 current flows through the reference resistor and RTD. The IDAC1 current excites the RTD to produce a voltage proportional to the RTD resistance. The RTD voltage is defined by 式 13:

$$V_{RTD} = R_{RTD} \cdot I_{IDAC1} \quad (13)$$

The ADC amplifies the RTD signal voltage (V_{RTD}) and measures the resulting voltage against the reference voltage to produce a proportional digital output code, as shown in 式 14 through 式 16.

$$\text{Code} \propto V_{RTD} \cdot \text{Gain} / V_{REF} \quad (14)$$

$$\text{Code} \propto (R_{RTD} \cdot I_{IDAC1}) \cdot \text{Gain} / (I_{IDAC1} \cdot R_{REF}) \quad (15)$$

$$\text{Code} \propto (R_{RTD} \cdot \text{Gain}) / R_{REF} \quad (16)$$

As shown in 式 16, the RTD measurement depends on the value of the RTD, the PGA gain, and the reference resistor R_{REF}, but not on the IDAC1 value. Therefore, the absolute accuracy and temperature drift of the excitation current does not matter.

The second excitation current (IDAC2) provides a second voltage drop across the second RTD lead resistance, R_{LEAD2}. The second voltage drop compensates the voltage drop caused by I_{DAC1} and R_{LEAD1}. The leads of a 3-wire RTD typically have the same length; therefore, the lead resistance is typically identical. Taking the lead resistance into account ($R_{LEADx} \neq 0$), the differential voltage (V_{IN}) across ADC inputs AIN8 and AIN9 is shown in 式 17:

$$V_{IN} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) - I_{IDAC2} \cdot R_{LEAD2} \quad (17)$$

If $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$, the expression for V_{IN} reduces to 式 18:

$$V_{IN} = I_{IDAC1} \cdot R_{RTD} \quad (18)$$

In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated as long as the lead resistance values and the IDAC values are matched.

Using 式 13, the value of RTD resistance (400 Ω, maximum) and the excitation current (500 µA) yields an RTD voltage of V_{RTD} = 500 µA · 400 Ω = 0.2 V. Use the maximum gain of 8 in order to limit the corresponding loop voltage of IDAC1. Gain = 8 requires a minimum reference voltage V_{REFMIN} = 0.2 V · 8 = 1.6 V. To provide margin for the ADC operating range, increase the target reference voltage by 10% (V_{REF} = 1.6 V · 1.1 = 1.76 V). Calculate the value of the reference resistor, as shown in 式 19:

$$R_{REF} = V_{REF} / I_{IDAC1} = 1.76 \text{ V} / 500 \text{ µA} = 3.52 \text{ k}\Omega \quad (19)$$

For this example application, 3.5 kΩ is chosen for R_{REF}. For best results, use a precision reference resistor R_{REF} with a low temperature drift (< 10 ppm/°C). Any change in R_{REF} is reflected in the measurement as a gain error.

The next step in the design is determining the value of the R_{BIAS} resistor, in order to level shift the RTD voltage to meet the ADC absolute input-voltage specification. The required level-shift voltage is determined by calculating the minimum absolute voltage ($V_{AINNLIM}$) as shown in 式 20:

$$AVSS + 0.15 + V_{RTDMAX} \cdot (Gain – 1) / 2 \le V_{AINNLIM}$$

where

- V_{RTDMAX} = maximum differential RTD voltage = 0.2 V
- Gain = 8
- AVSS = 0 V (20)

The result of the equation requires a minimum absolute input voltage (V_{RTDN}) > 0.85 V. Therefore, the RTD voltage must be level shifted by a minimum of 0.85 V. To meet this requirement, a target level-shift value of 1 V is chosen to provide extra margin. Calculate the value of R_{BIAS} as shown in 式 21:

$$R_{BIAS} = V_{AINN} / (I_{IDAC1} + I_{IDAC2}) = 1 \text{ V} / (2 \cdot 500 \text{ µA}) = 1 \text{ k}\Omega \quad (21)$$

After the level-shift voltage is determined, verify that the positive RTD voltage (V_{RTDP}) is less than the maximum absolute input voltage ($V_{AINPLIM}$), as shown in 式 22:

$$V_{AINPLIM} \le AVDD – 0.15 – V_{RTDMAX} \cdot (Gain – 1) / 2$$

where

- V_{RTDMAX} = maximum differential RTD voltage = 0.2 V
- Gain = 8
- AVDD = 4.75 V (minimum) (22)

Solving 式 22 results in a required V_{RTDP} of less than 3.9 V. Calculate the V_{RTDP} input voltage by 式 23:

$$V_{AINP} = V_{RTDN} + I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) = 1 \text{ V} + 500 \text{ µA} \cdot (400 \Omega + 10 \Omega) = 1.2 \text{ V} \quad (23)$$

Because 1.2 V is less than the 3.9-V maximum input voltage limit, the absolute positive and negative RTD voltages are within the ADC specified input range.

The next step in the design is to verify that the IDACs have enough voltage headroom (compliance voltage) to operate. The loop voltage of the excitation current must be less than the supply voltage minus the specified IDAC compliance voltage. Calculate the voltage drop developed across each IDAC current path to AVSS. In this circuit, IDAC1 has the largest voltage drop developed across its current path. The IDAC1 calculation is sufficient to satisfy IDAC2 because the IDAC2 voltage drop is always less than IDAC1 voltage drop. The sum of voltages in the IDAC1 loop is shown in 式 24:

$$V_{IDAC1} = [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{BIAS})] + [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1} + R_{REF})] + V_D$$

where

- V_D = external blocking diode voltage (24)

The equation results in a loop voltage of V_{IDAC1} = 3.0 V. The worst-case current source compliance voltage is: (AVDD – 0.4 V) = (4.75 V – 0.4 V) = 4.35 V. The V_{IDAC1} loop voltage is less than the specified current source compliance voltage (3.0 V < 4.35 V).

Many applications benefit from using an analog filter at the inputs to remove noise and interference from the signal. Filter components are placed on the ADC inputs (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}), as well as on the reference inputs (R_{F3}, R_{F4}, C_{DIF2}, C_{CM3}, and C_{CM4}). The filters remove both differential and common-mode noise. The application shows a differential input noise filter formed by R_{F1}, R_{F2} and C_{DIF1}, with additional differential mode capacitance provided by the common-mode filter capacitors, C_{CM1} and C_{CM2}. Calculate the differential

–3-dB cutoff frequency as shown in 式 25:

$$f_{DIF} = 1 / [2\pi \cdot (R_{F1} + R_{F2}) \cdot (C_{DIF1} + C_{CM1} || C_{CM2})] \quad (25)$$

The common-mode noise filter is formed by components R_{F1}, R_{F2}, C_{CM1}, and C_{CM2}. Calculate the common-mode signal –3-dB cutoff frequency, as shown in 式 26:

$$f_{CM} = 1 / (2\pi \cdot R_{F1} \cdot C_{CM1}) = 1 / (2\pi \cdot R_{F2} \cdot C_{CM2}) \quad (26)$$

Mismatches in the common-mode filter components convert common-mode noise into differential noise. To reduce the effect of mismatch, use a differential mode filter with a corner frequency that is at least 10 times lower than the common-mode filter corner frequency. The low-frequency differential filter removes the common-mode converted noise. The filter resistors (R_{Fx}) also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AINx) of the device to safe levels when an overvoltage occurs on the inputs.

Filter resistors lead to an offset voltage error due to the dc input current leakage flowing into and out of the device. Remove this voltage error by system offset calibration. Resistor values that are too large generate excess thermal noise and degrade the overall noise performance. The recommended range of the filter resistor values is 100 Ω to 10 kΩ. The properties of the capacitors are important because the capacitors are connected to the signal; use high-quality C0G ceramics or film-type capacitors.

For consistent noise performance across the full range of RTD measurements, match the corner frequencies of the input and reference filter. See the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Application Report* (SBAA201) for detailed information on matching the input and reference filter.

10.2.2.1 Register Settings

The register settings for this design are shown in 表 46.

表 46. Register Settings

REGISTER	NAME	SETTING	DESCRIPTION
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Bh	PGA enabled, PGA Gain = 8
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	06h	Positive and negative reference buffers enabled, REFP1 and REFN1 reference inputs selected, internal reference always on
06h	IDACMAG	05h	IDAC magnitude set to 500 µA
07h	IDACMUX	35h	IDAC2 set to AIN3, IDAC1 set to AIN5
08h	VBIAS	00h	
09h	SYS	10h	
0Ah	OFCAL0 (1)	xxh	
0Bh	OFCAL1	xxh	
0Ch	OFCAL2	xxh	
0Dh	FSCAL0 (1)	xxh	
0Eh	FSCAL1	xxh	
0Fh	FSCAL2	xxh	
10h	GPIODAT	00h	
11h	GPIOCON	00h	

(1) A two-point offset and gain calibration removes errors from the R_{REF} tolerance. The results are used for the OFC and FSC registers.

10.2.3 Application Curves

To test the accuracy of the acquisition circuit, a series of calibrated high-precision discrete resistors are used as an input to the system. Measurements are taken at T_A = 25°C. 図 114 displays the resistance measurement over an input span from 20 Ω to 400 Ω. Any offset error is generally attributed to the offset of the ADC, and the gain error can be attributed to the accuracy of the R_{REF} resistor and the ADC. The R_{REF} value is also calibrated to reduce the gain error contribution.

Precision temperature measurement applications are typically calibrated to remove the effects of gain and offset errors that generally dominate the total system error. The simplest calibration method is a linear, or two-point calibration that applies an equal and opposite gain and offset term to cancel the measured system gain and offset error. In this particular tested application, the gain and offset error was very small, and did not require additional calibration other than the self offset and gain calibration provided by the device. The resulting measured resistance error is shown in 図 115.

The results in 図 115 are converted to temperature accuracy by dividing the results by the RTD sensitivity (α) at the measured resistance. Over the full resistance input range, the maximum total measured error is ±0.0190 Ω. 式 27 uses the measured resistance error and the RTD sensitivity at 0°C to calculate the measured temperature accuracy.

$$\text{Error (°C)} = \text{Error } (\Omega) / \alpha_{@0°C} = \pm 0.0190\ \Omega / 0.39083\ \Omega / °C = \pm 0.049°C \quad (27)$$

図 116 displays the calculated temperature accuracy of the circuit assuming a linear RTD resistance to temperature response. This figure does not include any linearity compensation of the RTD, but 図 116 does remove offset and gain error, which can be calibrated with the OFC and FSC registers.

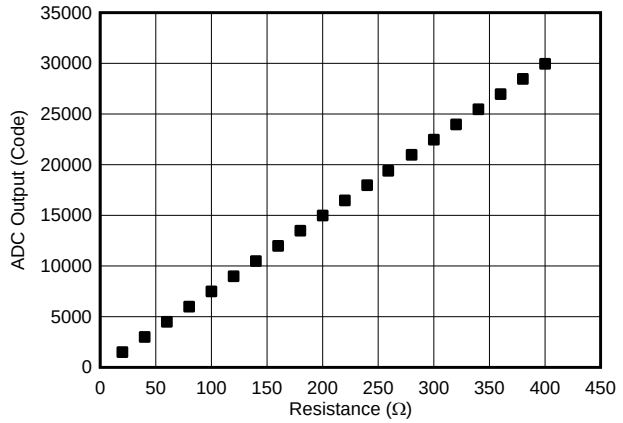


図 114. ADC Output Code vs Equivalent RTD Resistance

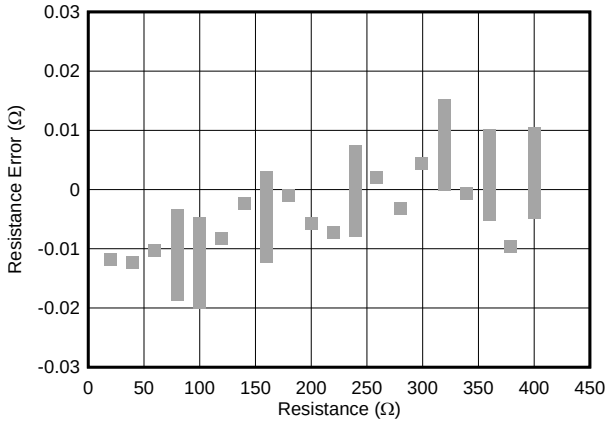


図 115. Measured Resistance Error vs Equivalent RTD Resistance

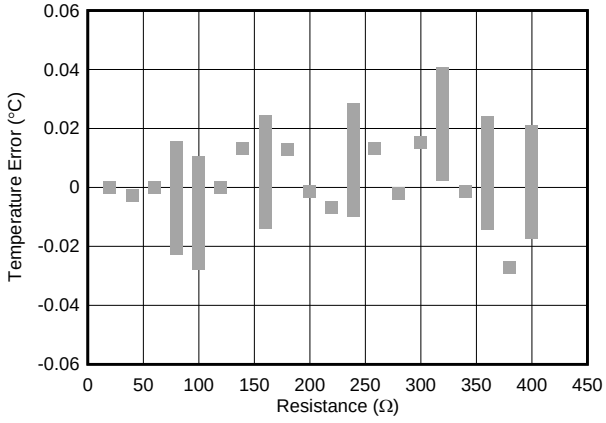


図 116. Equivalent Temperature Error vs Equivalent RTD Resistance

10.3 Do's and Don'ts

- Do partition the analog, digital, and power-supply circuitry into separate sections on the PCB.
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.

Do's and Don'ts (continued)

- Do verify that the analog input voltages are within the specified PGA input voltage range under all input conditions.
- Do float unused analog input pins to minimize input leakage current on all other analog inputs. Connecting unused pins to AVDD is the next best option.
- Do provide current limiting to the analog inputs in case overvoltage faults occur.
- Do use a low-dropout linear regulator (LDO) to reduce ripple voltage generated by switch-mode power supplies. Reducing ripple is especially important for AVDD where the supply noise can affect the performance.
- Don't cross analog and digital signals.
- Don't allow the analog and digital power supply voltages to exceed 5.5 V under any condition, including during power-up and power-down.

Do's and Don'ts (continued)

図 117 shows the do's and don'ts of the ADC circuit connections.

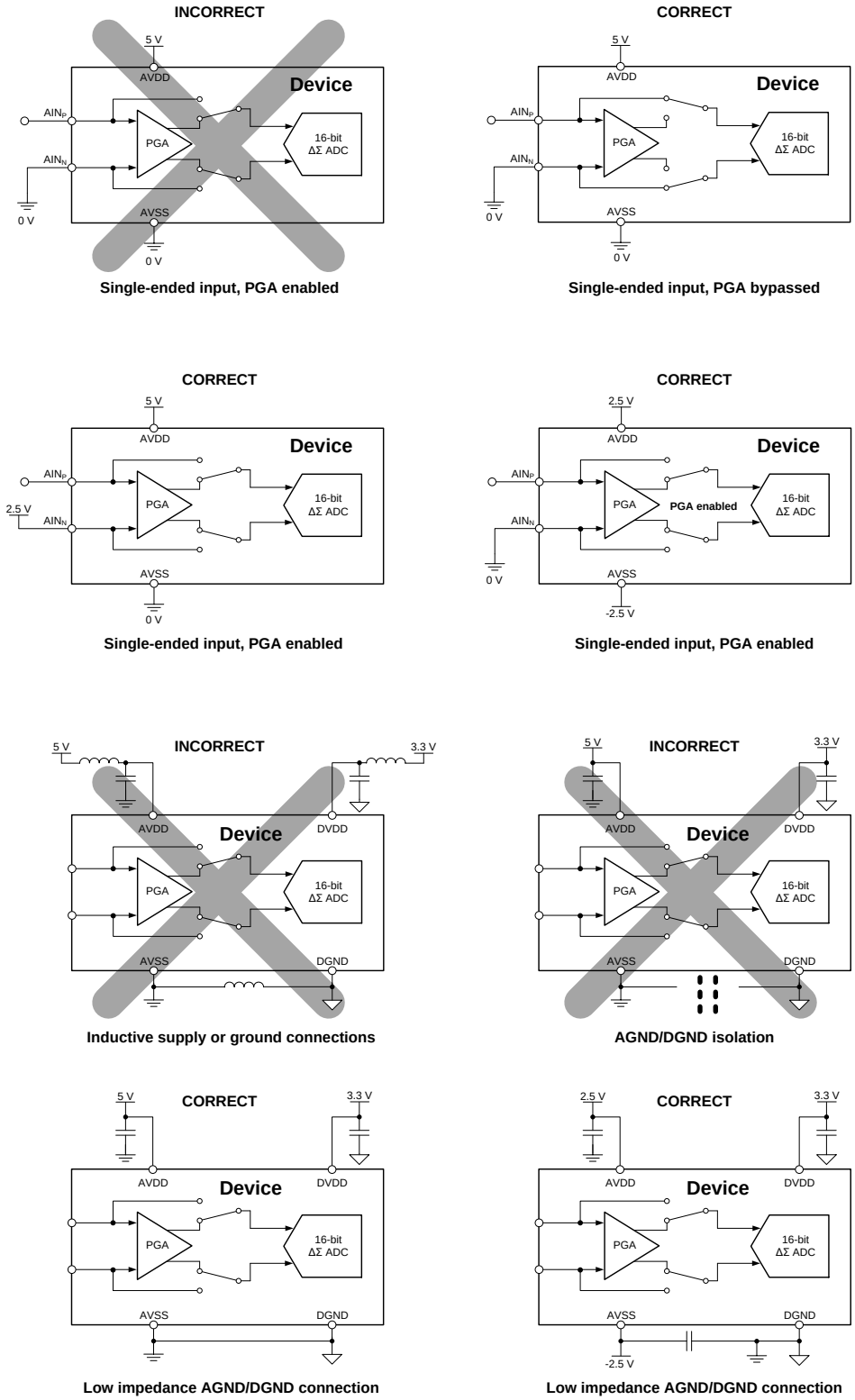


図 117. Do's and Don'ts Circuit Connections

11 Power Supply Recommendations

11.1 Power Supplies

The ADS114S0x requires three power supplies: analog (AVDD, AVSS), digital core (DVDD, DGND), and digital I/O (IOVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supplies. DVDD is used to power the digital circuits of the devices. IOVDD sets the digital I/O levels (with the exception of the GPIO levels that are set by the analog supply of AVDD and AVSS). IOVDD must be equal to or larger than DVDD.

11.2 Power-Supply Sequencing

AVDD and DVDD may be powered up in any order. However, IOVDD is recommended to be powered up before or at the same time as DVDD. If DVDD comes up before IOVDD, a reset of the device using the $\overline{\text{RESET}}$ pin or the RESET command may be required.

11.3 Power-On Reset

An internal POR is released after all three supplies exceed approximately 1.65 V. Each supply has an individual POR circuit. A brownout condition on any of the three supplies triggers a reset of the complete device.

11.4 Power-Supply Decoupling

Good power-supply decoupling is important to achieve best performance. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-μF capacitor to DGND. 図 118 and 図 119 show typical power-supply decoupling examples for unipolar and bipolar analog supplies, respectively. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. Use multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. To reduce inductance on the supply pins, avoid the use of vias for connecting the capacitors to the supply pins. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Connect analog and digital grounds together as close to the device as possible.

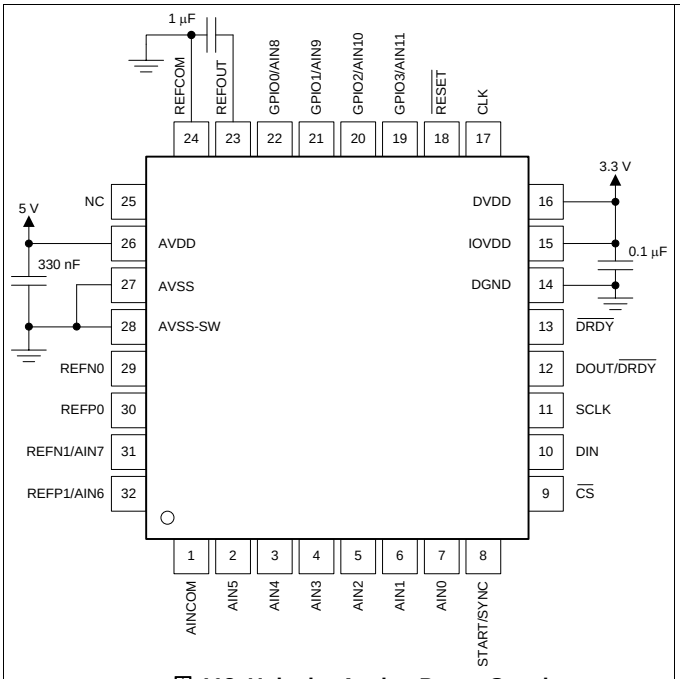


図 118. Unipolar Analog Power Supply

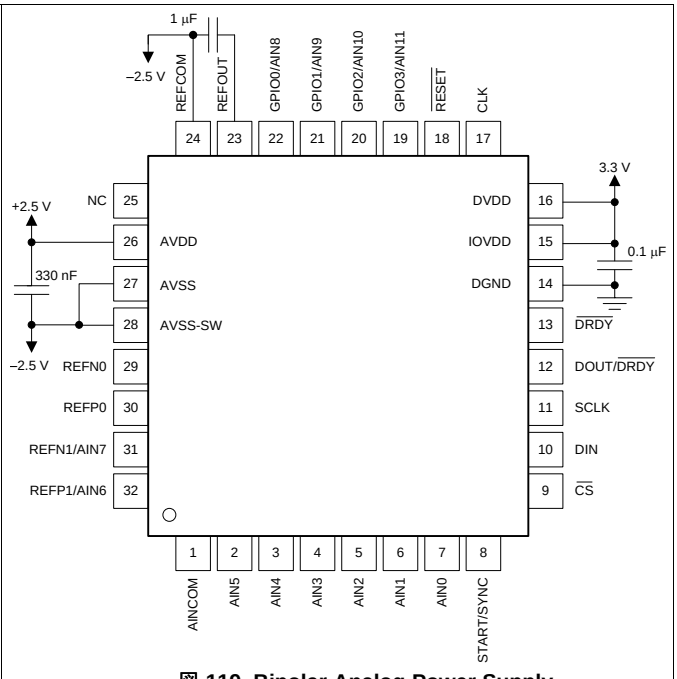


図 119. Bipolar Analog Power Supply

12 Layout

12.1 Layout Guidelines

Employing best design practices is recommended when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in 図 120. Although 図 120 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

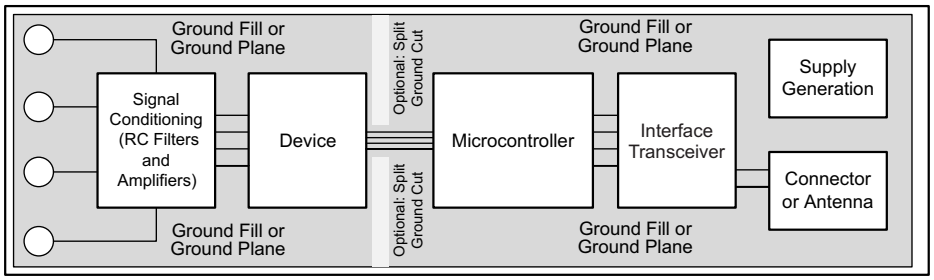


図 120. System Component Placement

The following basic recommendations for layout of the ADS114S0x help achieve the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital lines away from analog lines. This prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but this (splitting) is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents will flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic themocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines (such as AIN0, AIN1 and AIN2, AIN3). The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO) that have stable properties and low noise characteristics.

12.2 Layout Example

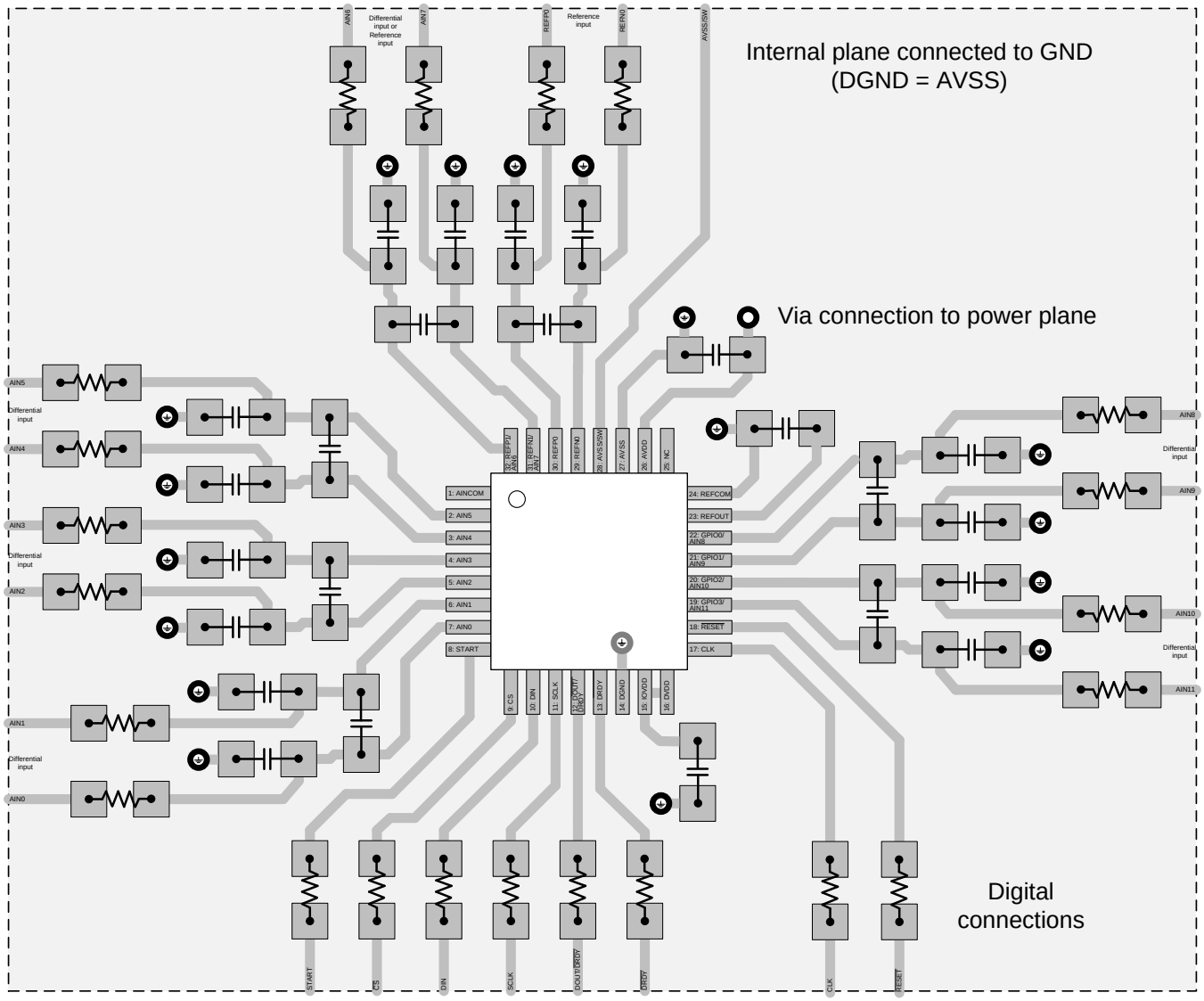


図 121. ADS114S0x Layout Example

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 開発サポート

『ADS1x4S0x 設計カルキュレータ』

13.2 ドキュメントのサポート

13.2.1 関連資料

関連資料については、以下を参照してください：

- *『REF50xx 低ノイズ、超低ドリフト係数、高精度基準電圧』*
- *『ADS1148およびADS1248を使用したRTDレシオメトリック測定およびフィルタリング』アプリケーション・レポート*
- *『3線式RTD測定システムのリファレンス・デザイン、-200℃～850℃』*

13.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 47. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
ADS114S06	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
ADS114S08	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.6 商標

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All other trademarks are the property of their respective owners.

13.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS114S06IPBS	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S06
ADS114S06IPBS.A	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S06
ADS114S06IPBS.B	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S06
ADS114S06IPBSR	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S06
ADS114S06IPBSR.A	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S06
ADS114S06IPBSR.B	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S06
ADS114S06IRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S06
ADS114S06IRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S06
ADS114S06IRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S06
ADS114S06IRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S06
ADS114S06IRHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S06
ADS114S06IRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S06
ADS114S08IPBS	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IPBS.A	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IPBS.B	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IPBSG4	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IPBSG4.A	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IPBSG4.B	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS114S08IPBSR	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IPBSR.A	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IPBSR.B	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	114S08
ADS114S08IRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBTG4	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBTG4.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08
ADS114S08IRHBTG4.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	ADS 114S08

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

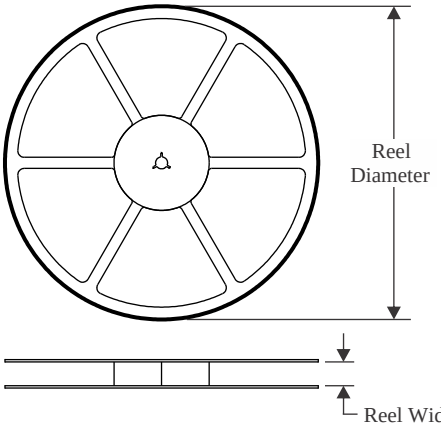
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

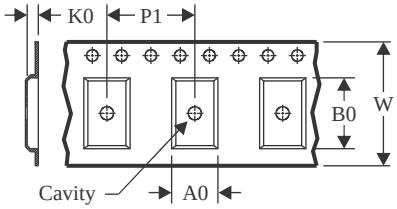
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

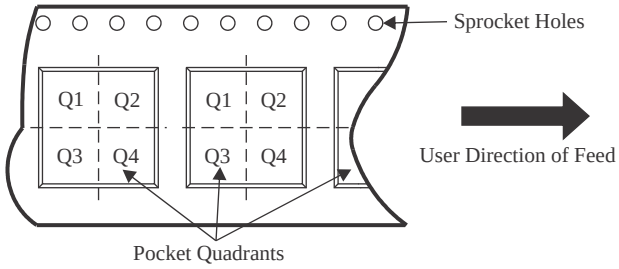


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

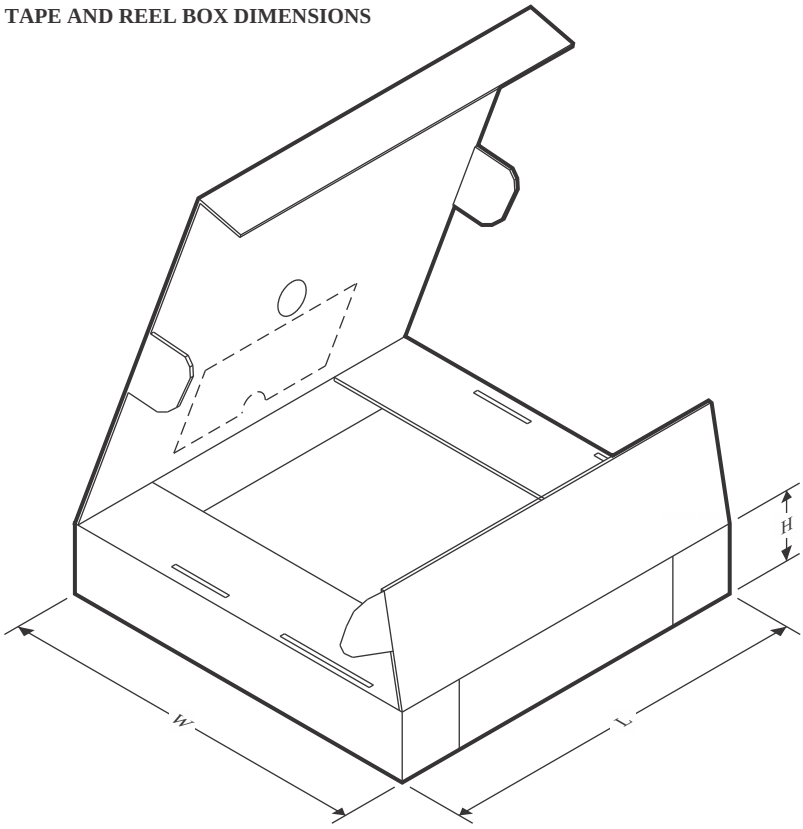
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS114S06IPBSR	TQFP	PBS	32	1000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS114S06IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS114S06IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS114S08IPBSR	TQFP	PBS	32	1000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS114S08IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS114S08IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS114S08IRHBTG4	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

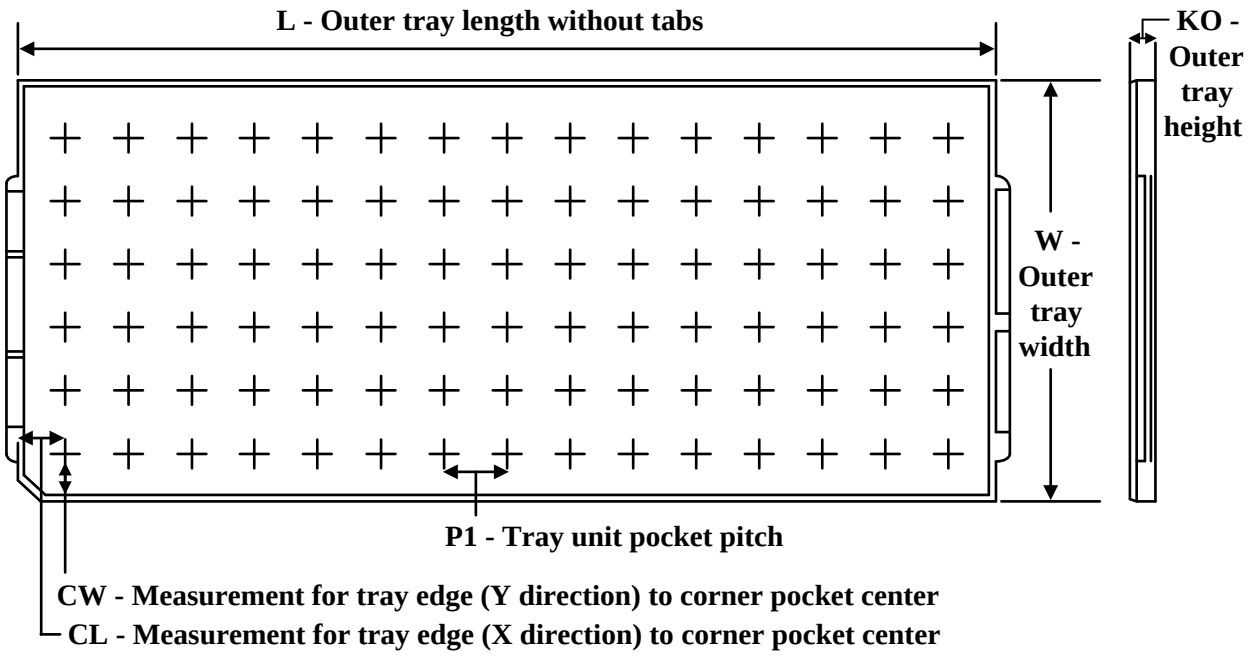
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS114S06IPBSR	TQFP	PBS	32	1000	350.0	350.0	43.0
ADS114S06IRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
ADS114S06IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS114S08IPBSR	TQFP	PBS	32	1000	350.0	350.0	43.0
ADS114S08IRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
ADS114S08IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS114S08IRHBTG4	VQFN	RHB	32	250	210.0	185.0	35.0

TRAY

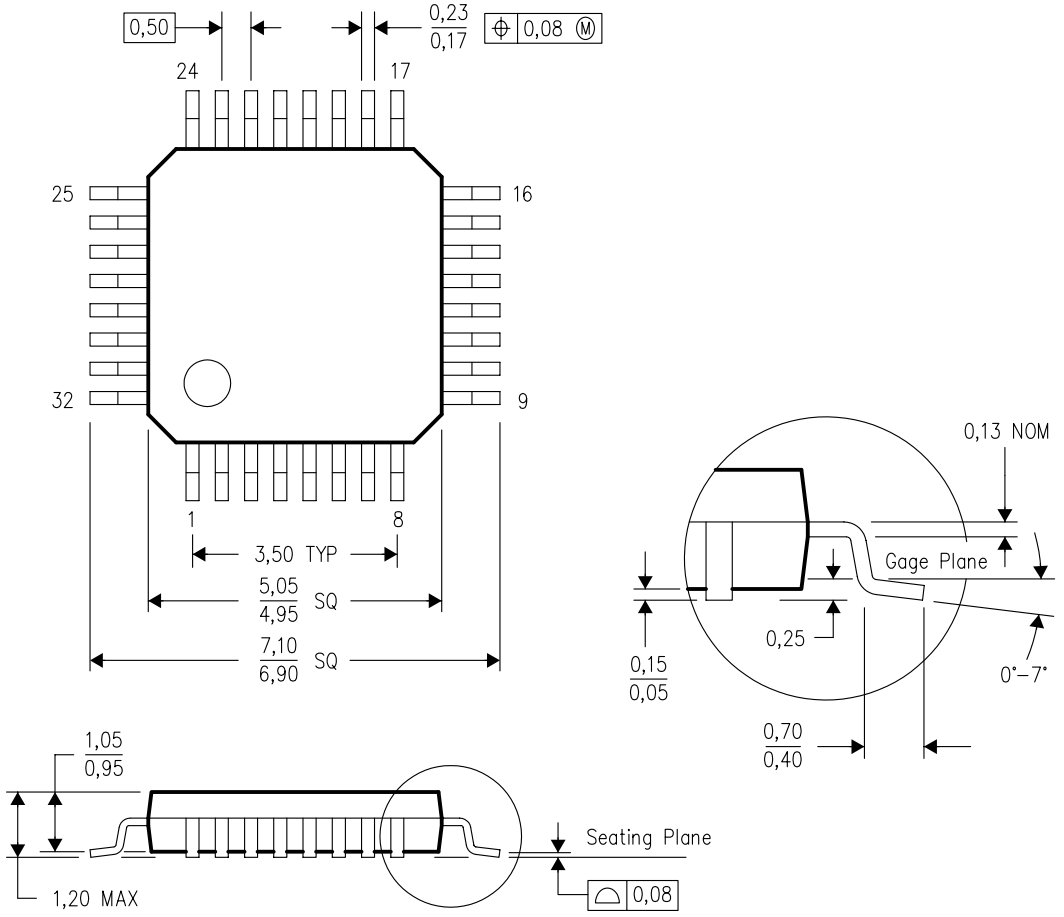


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS114S06IPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S06IPBS.A	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S06IPBS.B	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S08IPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S08IPBS.A	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S08IPBS.B	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S08IPBSG4	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S08IPBSG4.A	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS114S08IPBSG4.B	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25

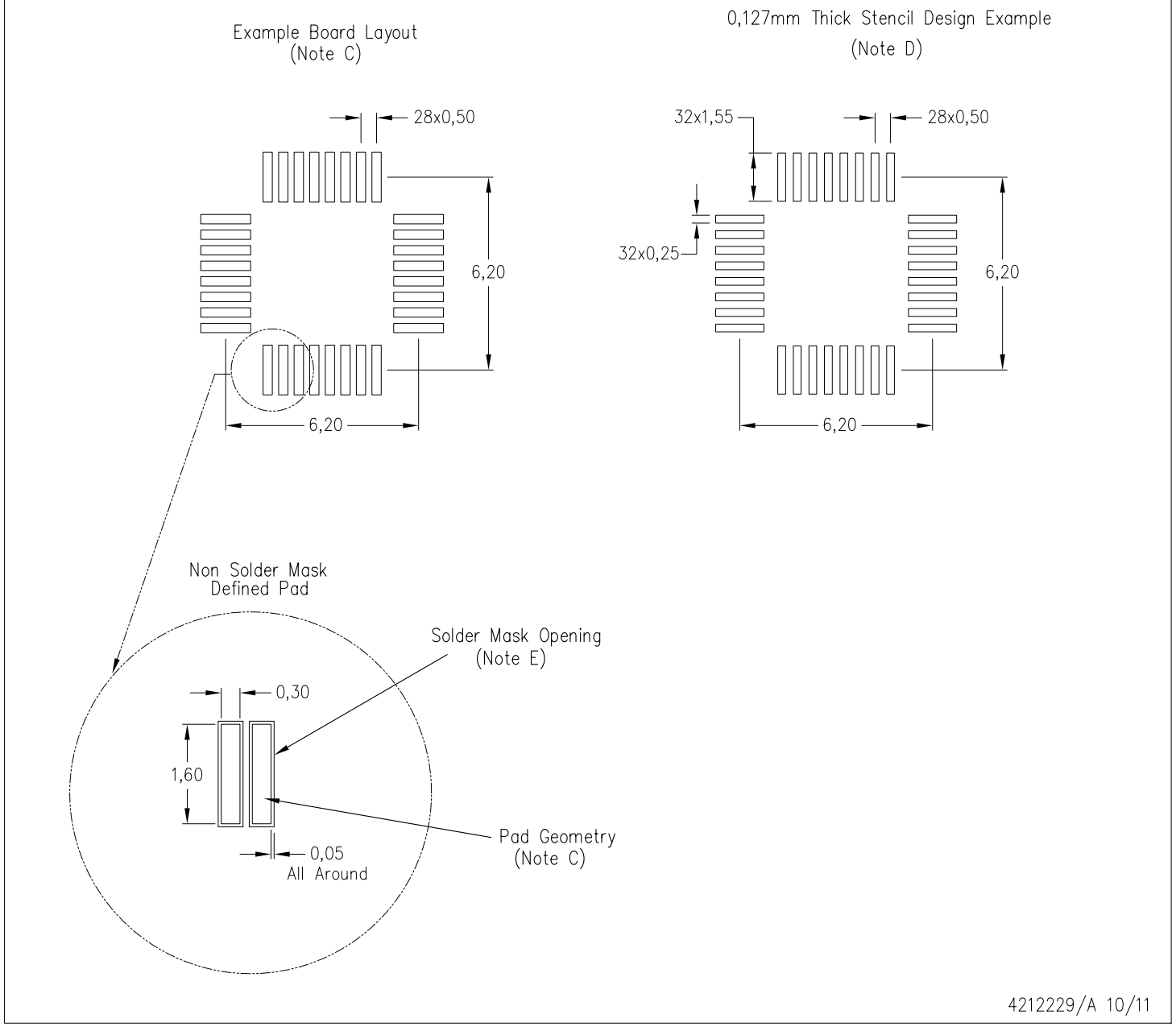
PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



4087735/B 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

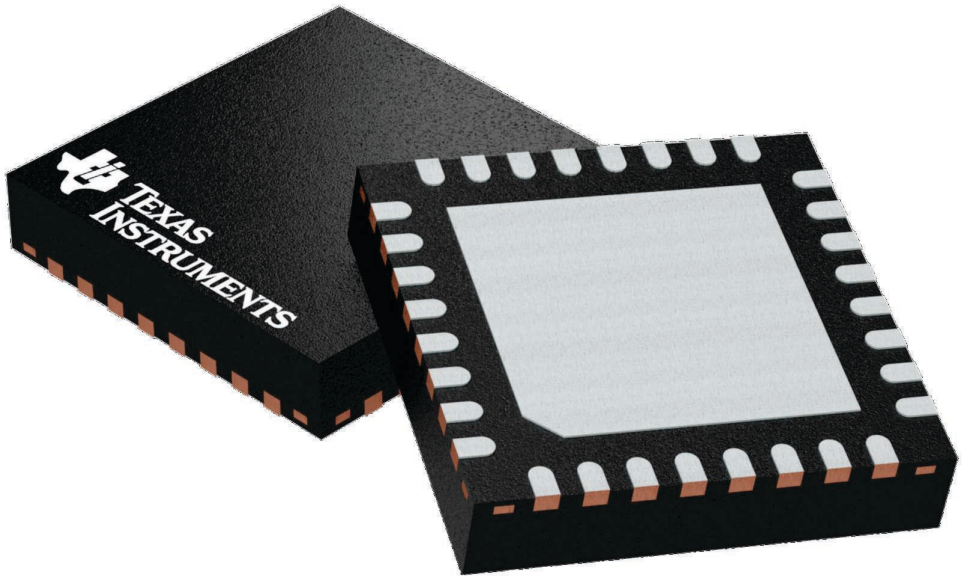
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

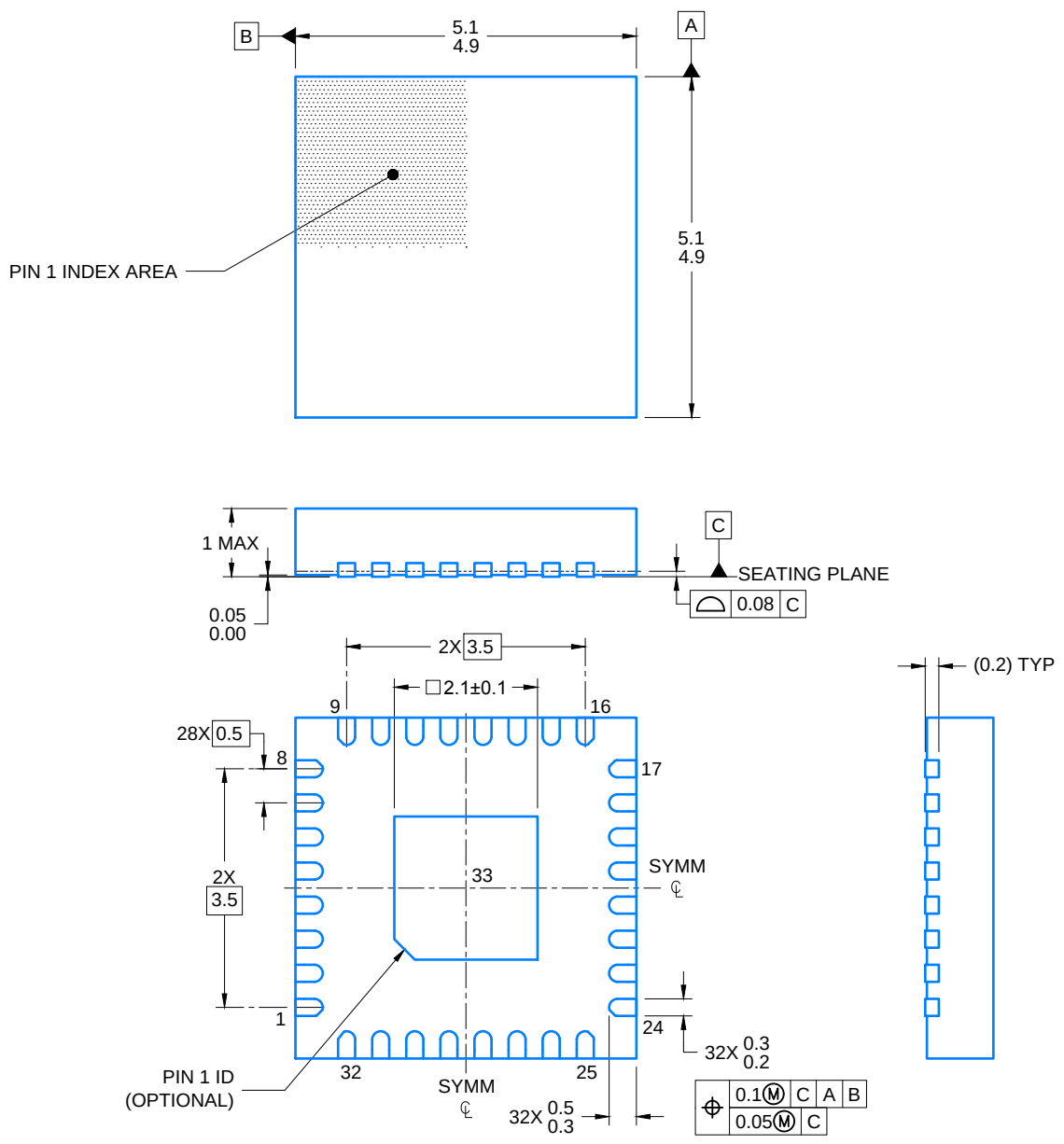
4224745/A

PACKAGE OUTLINE

RHB0032M

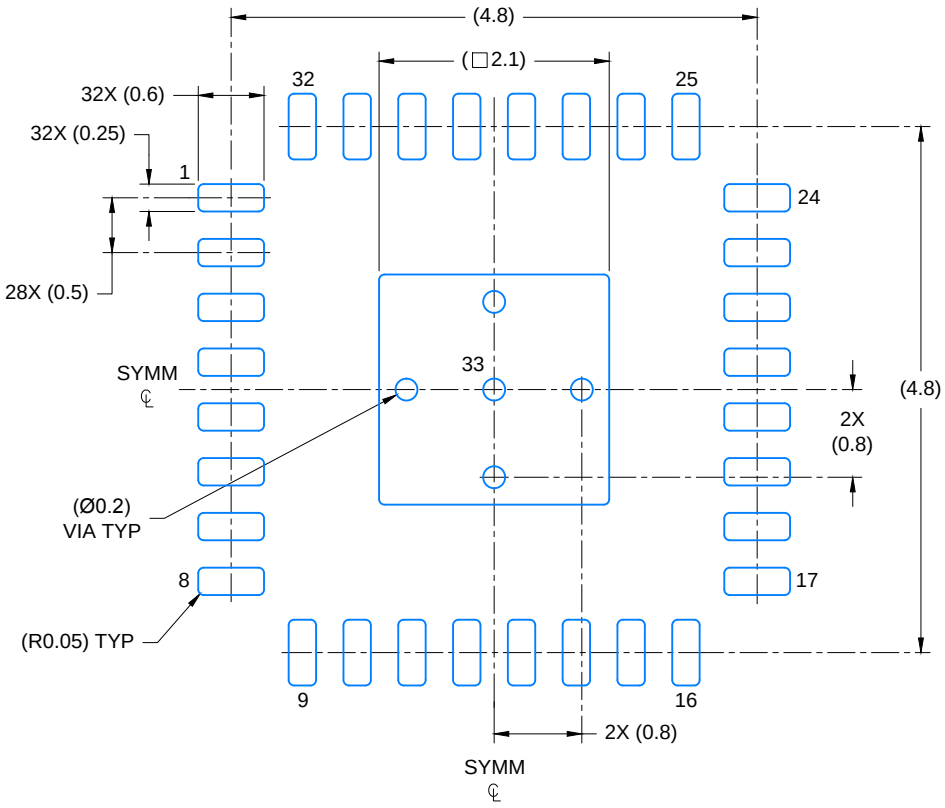
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

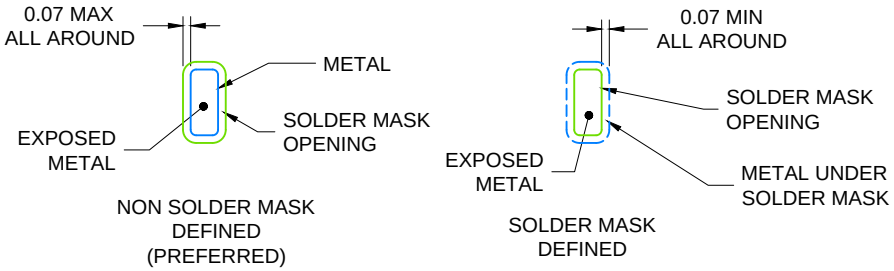


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

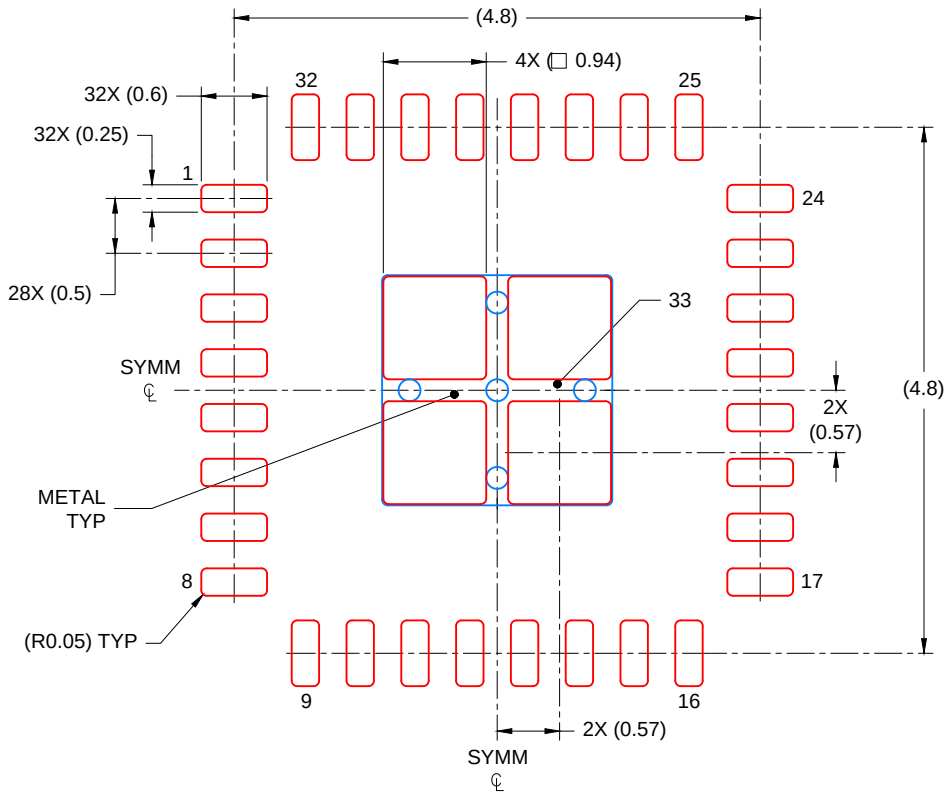


SOLDER MASK DETAILS

4223725/A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4223725/A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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